Trench formation and corner rounding in vertical GaN power devices

Citation: Zhang, Yuhao et al. "Trench Formation and Corner Rounding in Vertical GaN Power Devices." Applied Physics Letters 110, 19 (May 2017): 193506

As Published: https://doi.org/10.1063/1.4983558

Publisher: American Institute of Physics (AIP)

Persistent URL: http://hdl.handle.net/1721.1/116060

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

Trench formation and corner rounding in vertical GaN power devices

Yuhao Zhang, Min Sun, Zhihong Liu, Daniel Piedra, Jie Hu, Xiang Gao, and Tomás Palacios

Citation: Appl. Phys. Lett. **110**, 193506 (2017); doi: 10.1063/1.4983558
View online: https://doi.org/10.1063/1.4983558
View Table of Contents: http://aip.scitation.org/toc/apl/110/19
Published by the American Institute of Physics

Trench formation and corner rounding in vertical GaN power devices

Yuhao Zhang,[1,a)] Min Sun,[1] Zhihong Liu,[2] Daniel Piedra,[1] Jie Hu,[1] Xiang Gao,[3] and Tomás Palacios[1]

[1]*Microsystems Technology Laboratories, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*
[2]*Singapore-MIT Alliance for Research and Technology, Singapore 138602, Singapore*
[3]*IQE RF LLC, Somerset, New Jersey 08873, USA*

(Received 1 February 2017; accepted 3 May 2017; published online 11 May 2017)

Trench formation and corner rounding are the key processes to demonstrate high-voltage trench-based vertical GaN devices. In this work, we developed a damage-free corner rounding technology combining Tetramethylammonium hydroxide wet etching and piranha clean. By optimizing the inductively coupled plasma dry etching conditions and applying the rounding technology, two main trench shapes were demonstrated: flat-bottom rounded trench and tapered-bottom rounded trench. TCAD simulations were then performed to investigate the impact of trench shapes and round corners on device blocking capability. GaN trench metal-insulator-semiconductor barrier Schottky rectifiers with different trench shapes were fabricated and characterized. A breakdown voltage over 500 V was obtained in the device with flat-bottom rounded trenches, compared to 350 V in the device with tapered-bottom rounded trenches and 150 V in the device with non-rounded trenches. Both experimental and simulation results support the use of rounded flat-bottom trenches to fabricate high-voltage GaN trench-based power devices. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4983558]

Gallium nitride (GaN)-based devices are excellent candidates for high-voltage and high-power applications, due to the superior physical properties of GaN compared to Si, SiC, and GaAs. Recently, GaN vertical devices have attracted increased attention, due to their advantages over GaN lateral devices, including high breakdown voltage (*BV*) and current capability for a given chip size, and superior thermal performance.[1] Recent demonstrations of high-performance vertical GaN diodes[2–4] and transistors[5,6] have made vertical structures very promising for GaN power devices.

Among the demonstrated vertical GaN power devices, trench-based structures have achieved the best performance for advanced Schottky rectifiers and power transistors. Figure 1 presents the simplified schematics of four trench-based vertical GaN devices recently reported. The trench metal-insulator-semiconductor barrier Schottky (TMBS) rectifiers [Fig. 1(a)] utilized the trench structure to shield the high electric field (E-field) at the Schottky contact and demonstrated a greatly enhanced reverse blocking characteristics for Schottky rectifiers.[7] The trench fin GaN field-effect transistors (FETs) [Fig. 1(b)] have sub-micron GaN fins with all-around gates and achieved normally off operation without the need for p-GaN.[8] The trench metal-oxide-semiconductor FETs (MOSFETs)[6,9–11] [Fig. 1(c)] and trench current aperture vertical electron transistors (CAVETs)[12,13] [Fig. 1(d)] combined the trench structure with MOS or two-dimensional-electron-gas (2DEG) channels, respectively, and demonstrated a *BV* close to 2 kV (Refs. 12 and 14) with normally off operation.

Trench formation and corner rounding are the key technologies to demonstrate these high-voltage trench-based vertical GaN devices. As the device peak E-field is typically located near the trench corners or bottoms, the trench shape and bottom morphology are determining factors for device *BV*. On the other hand, due to the relatively high bond energy (8.92 eV/atom) of GaN, high ion energy is typically required in the dry etching for deep trenches, resulting in rough surfaces and sharp corners in the trench. To prevent surface leakage and E-field crowding, the sidewall smoothening and corner rounding are essential.[15,16] The conventional corner rounding process technology for Si and SiC devices typically requires high temperature (over 1000 °C) annealing,[15,16] which would deteriorate GaN material quality and device

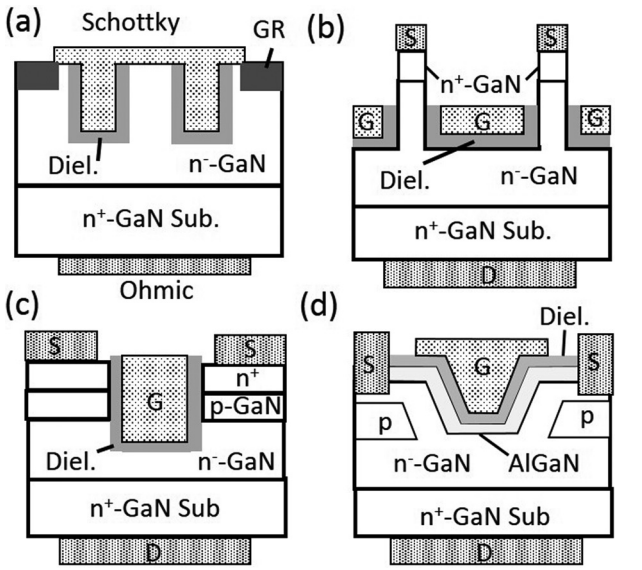

FIG. 1. Simplified schematics for (a) GaN trench metal-insulator-semiconductor (MIS) barrier Schottky rectifiers, (b) GaN trench fin FETs, (c) GaN trench MOSFETs, and (d) GaN trench CAVETs (GR represents guard ring and Diel. represents dielectrics).

[a)]Electronic mail: yhzhang@mit.edu.

performance. Therefore, the optimization of trench shapes and the development of a damage-free corner rounding process are greatly needed for vertical GaN power devices.

In this work, we developed a corner rounding process by utilizing the Tetramethylammonium hydroxide (TMAH) wet etching and piranha clean. By varying different dry etching conditions with the corner rounding technology, we demonstrated different bottom morphologies in rounded GaN trenches. Technology computer-aided design (TCAD) simulations were performed to reveal the impact of these trench shapes on device *BV* and E-field distributions. GaN TMBS rectifiers with different trench shapes were then fabricated and characterized. Both experimental and simulation results suggested the rounded flat-bottom trench as an optimized structure for high-voltage device applications.

The wafer structure used in this work consists of n^--GaN layers grown on 2-in. Si or n^+-GaN substrates. The trench formation process technology was developed in GaN-on-Si wafers and trench-based devices were then fabricated utilizing GaN-on-GaN wafers. The trench structures were formed in an inductively coupled plasma (ICP) etching system. The etching was performed at an ICP power of 150 W, a bias power of 30–75 W, a chamber temperature of 40 °C and pressure of 0.6 Pa. Cl_2/BCl_3 gas combination was used for the ICP etching with a flow rate of 20 sccm for Cl_2 and different rates (5–20 sccm) for BCl_3. The etching utilized 50 nm Ni as hard masks. Compared with conventional oxide masks, the use of a metal hard mask allows for a much smoother etch sidewall, due to the lack of oxide edge erosion under high ion energies.[17] In the dry etching, the trench was not aligned to specific crystalline directions. The width and depth of the trenches were both around 2 μm.

TMAH wet etching (25% concentration) at 85 °C for 70 min with a following piranha clean for 10 min was found effective in removing the etch damage and rounding the trench corners. Figures 2(a)–2(c) show the cross-sectional scanning electron microscopy (SEM) images of the trench structure right after dry etching [Fig. 2(a)], with a following TMAH wet etching [Fig. 2(b)], and with an additional piranha clean [Fig. 2(c)]. The trench right after the dry etching shows rough surfaces with the sidewall tapered angle being around 70°. Due to its anisotropic etching, TMAH preferentially etches the side slopes and therefore eliminate the surface damage caused by the dry etching.[10,17] This surface smoothing is found to also significantly reduce the surface leakage current.[17] As shown in Figs. 2(b) and 2(c), the Ni mask residues produced during the dry etching and TMAH treatment can be effectively removed by piranha clean. A simple ultrasonic clean in acetone was unable to remove these residues. The final rounded trench shows smooth vertical sidewalls and flat bottom, with a corner rounding radius of about 200 nm. It should also be noted that in the formation of sub-micron trenches, we found that the trench structures aligned along the [1120] direction have smoother surface than those in the [1100] direction.[8] This is due to the different etch rate of TMAH on GaN along different orientations. This etch rate difference is typically small, inducing a roughness difference of ~20 nm for a 60-minute hot TMAH treatment. Thus, this orientation dependence of sidewall smoothness is not significant in the formation of micron-sized trenches.

The trench bottom morphology can be controlled by the dry etching conditions. A less anisotropic dry etching could enhance the lateral etching, reduce the tapered angle of dry etching sidewalls, and produce a tapered trench bottom after the TMAH wet etching. In the Cl_2/BCl_3 based ICP etching, the less anisotropic etching can be realized by either reducing the bias power or increasing the BCl_3/Cl_2 ratio.[18] As shown in Figures 2(d)–2(f), the dry etching with lower bias power and higher BCl_3 flow rate produced a pointed trench bottom; the following TMAH and piranha clean converted the pointed bottom into a tapered bottom (tapered angle ~30°) with a rounded bottom corner.

Figure 3 summarizes the rounded trench shapes corresponding to different dry etching conditions, i.e., various bias powers and BCl_3/Cl_2 ratios. From Figs. 3(a)–3(c), it can be shown that for a high bias power, the rounded trench shape is not sensitive to the BCl_3/Cl_2 ratio, having flat bottoms for different gas ratios. In contrast, for low bias power, as Figs. 3(d)–3(f) show, the increase in BCl_3/Cl_2 ratio could gradually expand the corner regions and the tapered slopes (tapered angle ~30°) and finally change the flat bottom into a tapered one in the rounded trenches.

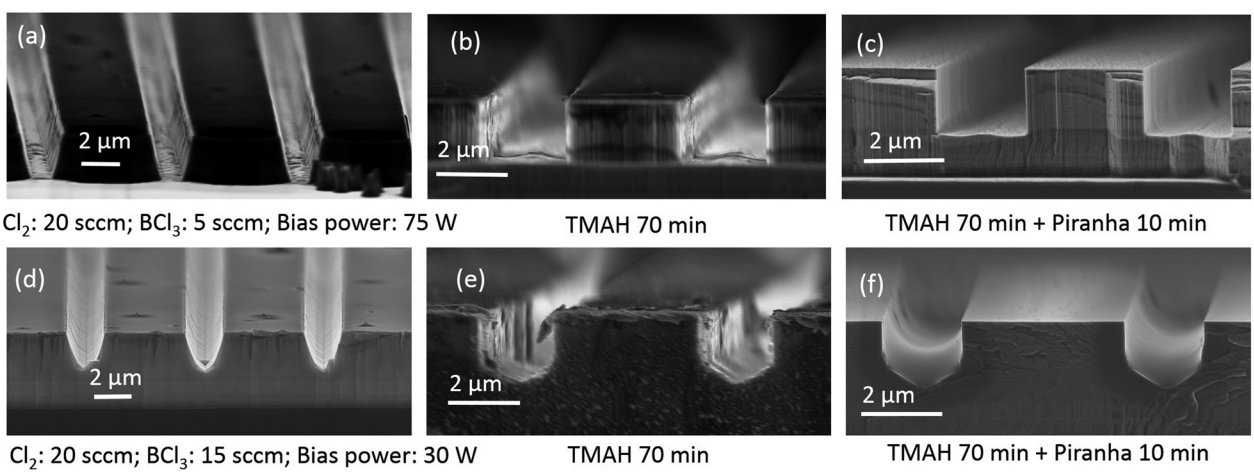

FIG. 2. Cross-sectional SEM images of the trench structures right after dry etching, with a following TMAH wet etching, and with an additional piranha clean, for two different conditions of initial dry etching.

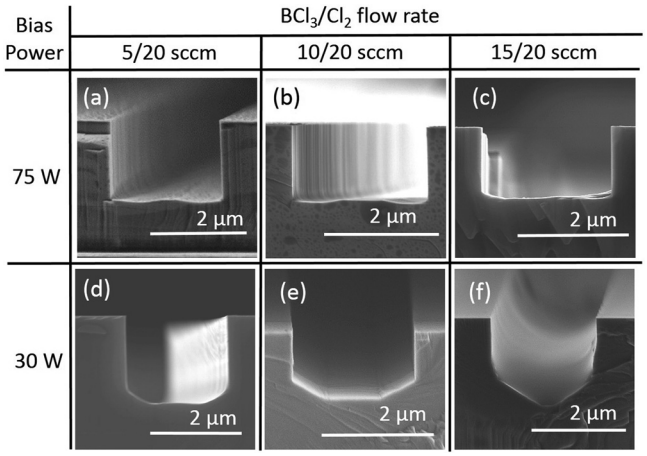

FIG. 3. Cross-sectional SEM images of the rounded trench structures corresponding to six different conditions of initial dry etching, with various bias power and different BCl_3/Cl_2 flow rate. All the trenches have been rounded by TMAH treatment and piranha clean. All the trenches have a width of 2 μm and a depth of 1–2 μm.

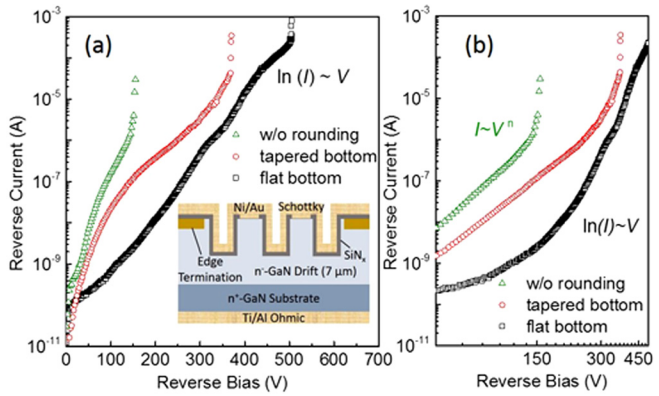

FIG. 5. (a) Reverse *I-V* characteristics of TMBS rectifiers with non-rounded trenches, rounded flat-bottom trenches and rounded tapered-bottom trenches, in a semi-log plot. (Inset) Schematic structure of the fabricated GaN TMBS rectifiers. (b) Reverse *I-V* characteristics in a log-log plot.

To study the blocking capability of rounded trenches with different shapes, two-dimensional E-field distribution was simulated for a trench-based device unit-cell using the Silvaco ATLAS simulator. The simulation models are similar to the ones in our previous work.[1,19] As shown in Fig. 4, the unit-cell consists of a 7 μm n^--GaN (Si: 2×10^{16} cm^{-3}), an n^+-GaN substrate, and a 250 nm SiN_x covering the GaN trench. Although the simulated unit cell has only a top and a bottom electrode (e.g., for TMBS rectifiers), the simulated E-field distribution at a high reverse bias also applies to the trench-based normally off transistors, when they are in the off-state with a zero gate bias and large reverse drain biases. In the unit-cell, three representative trench shapes were simulated: a non-rounded trench [corresponding to Fig. 2(a)], a rounded trench with a flat bottom [corresponding to Fig. 2(c)] and a rounded trench with a tapered bottom [corresponding to Fig. 2(f)], where the rounding radius of all rounded corners was set as 200 nm and the trench depth was set as 2 μm. For simplicity's sake, the trench shapes shown in Figs. 2(d) and 2(e) were not simulated, as they can be regarded as transitional structures between the flat-bottom and tapered-bottom structures. Also, they have more corners than the flat-bottom or tapered-bottom trenches, which would increase the risk of E-field crowding and early breakdown. Figure 4 shows the simulated E-field distribution at a high reverse bias for the three representative trenches. The non-rounded trench shows the highest peak E-fields in GaN and dielectrics located around the sharp corners, while the rounded trench with a flat bottom shows the lowest peak E-fields. The rounded trench with a tapered bottom has an E-field crowding at the bottom rounded corner, indicating an inferior blocking capability to the rounded trench with a flat bottom.

To experimentally verify the impact of trench shapes on device blocking characteristics, TMBS rectifiers incorporating the three representative trench shapes were fabricated. After the formation of deep trenches in GaN-on-GaN wafers, a 250 nm SiN_x layer was deposited by plasma-enhanced chemical vapor deposition. Openings were created on the mesa top surfaces, followed by formation of the top Ni/Au Schottky contact and bottom Ti/Al Ohmic contact. The mesa width, trench width and trench depth are all 2 μm. Figure 5 shows the representative reverse *I–V* characteristics of the three TMBS rectifiers with (a) non-rounded trench, (b) flat-bottom rounded trench and (c) tapered-bottom rounded trench, with the etching processes corresponding to Figs. 2(a), 2(c), and 2(f), respectively. The device

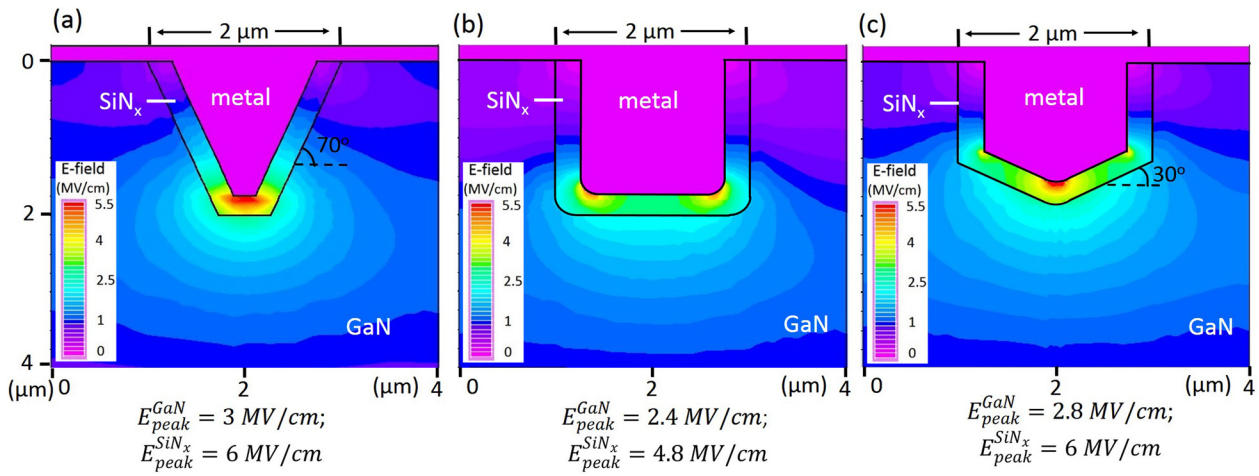

FIG. 4. Simulated E-field distribution in the top part of a device unit-cell (the bottom electrode, n^+-GaN substrate and a part of n^--GaN are not shown), at a reverse bias of 600 V, for three different trench shapes: (a) non-rounded trench, (b) rounded trench with a flat bottom, and (c) rounded trench with a tapered bottom.

without the corner rounding process shows high leakage current and an early breakdown at −150 V due to the sharp corners and surface damage within the trenches. The leakage current I increases with V^n [Fig. 5(b)], indicating the leakage mechanism was dominated by the trap-assisted space charge limited current (SCLC).[4,20] The dominant traps are probably located at the etching sidewalls and their interfaces with dielectrics.[17] The device with rounded flat-bottom trenches shows the lowest leakage current and highest BV (∼500 V) among the three trench structures, which agrees well with the simulation results. In this device, the leakage current I exhibits a linear relationship of $\ln(I) \propto V$ [Fig. 5(a)], indicating the leakage mechanism was dominated by variable-range-hopping (VRH) through dislocations.[20] This VRH mechanism was typically found in vertical GaN pn diodes, where the peak E-field is in the bulk GaN.[20] This indicates that, in the TMBS rectifiers with rounded flat-bottom trenches, the leakage current is mostly determined by the peak E-field in bulk GaN rather than dielectrics or dielectrics/GaN interfaces. The device with rounded tapered-bottom trenches shows a medium BV of ∼350 V, with a leakage current mechanism as a combination of trap-assisted SCLC and VRH. Finally, it should be noted that, with the optimized trench shapes, further improvement of the blocking capability of trench structures can be achieved by enhancement of dielectric quality, insertion of implanted field rings near the trench bottoms,[7] or introduction of carbon-doped GaN/p-GaN hybrid blocking layers.[12]

In conclusion, we developed a damage-free corner rounding technology combining TMAH wet etching and piranha clean. By varying dry etching conditions and applying the corner rounding process, we demonstrated two main rounded trench shapes: flat-bottom rounded trench and tapered-bottom rounded trench. TCAD simulation was conducted to investigate the impact of trench shapes on device blocking capability. GaN TMBS rectifiers were then fabricated and characterized, with a good agreement achieved between experimental and simulation results. The flat-bottom rounded trench has been revealed as an optimum trench shape for high-voltage vertical GaN power devices.

The authors gratefully acknowledge the funding support by the ARPA-E SWITCHES Program monitored by Dr. T. Heidel and Dr. I. Kizilyalli.

[1]Y. Zhang, M. Sun, Z. Liu, D. Piedra, H.-S. Lee, F. Gao, T. Fujishima, and T. Palacios, IEEE Trans. Electron Devices **60**, 2224 (2013).
[2]K. Nomoto, Z. Hu, B. Song, M. Zhu, M. Qi, R. Yan, V. Protasenko, E. Imhoff, J. Kuo, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, in *Proceedings of the 2015 IEEE International Electron Devices Meeting IEDM*, *Washington, DC, USA, 7–9 December, 2015* (2015), pp. 9.7.1–9.7.4.
[3]Y. Zhang, D. Piedra, M. Sun, J. Hennig, A. Dadgar, L. Yu, and T. Palacios, IEEE Electron Device Lett. **38**, 248 (2017).
[4]Y. Zhang, M. Sun, D. Piedra, M. Azize, X. Zhang, T. Fujishima, and T. Palacios, IEEE Electron Device Lett. **35**, 618 (2014).
[5]H. Nie, Q. Diduck, B. Alvarez, A. P. Edwards, B. M. Kayes, M. Zhang, G. Ye, T. Prunty, D. Bour, and I. C. Kizilyalli, IEEE Electron Device Lett. **35**, 939 (2014).
[6]T. Oka, T. Ina, Y. Ueno, and J. Nishii, Appl. Phys. Express **8**, 54101 (2015).
[7]Y. Zhang, M. Sun, Z. Liu, D. Piedra, M. Pan, X. Gao, Y. Lin, A. Zubair, L. Yu, and T. Palacios, in *Proceedings of the 2016 IEEE International Electron Devices Meeting IEDM*, *San Francisco, CA, USA, 3–7 December 2016* (2016), pp. 10.2.1–10.2.4.
[8]M. Sun, Y. Zhang, X. Gao, and T. Palacios, IEEE Electron Device Lett. **38**, 509 (2017).
[9]H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, Appl. Phys. Express **1**, 11105 (2008).
[10]M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, Appl. Phys. Express **1**, 21104 (2008).
[11]R. Li, Y. Cao, M. Chen, and R. Chu, IEEE Electron Device Lett. **37**, 1466 (2016).
[12]D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda, in *Proceedings of 2016 IEEE International Electron Devices Meeting IEDM*, *San Francisco, CA, USA, 3–7 December 2016* (2016), pp. 10.1.1–10.1.4.
[13]D. Ji, M. A. Laurent, A. Agarwal, W. Li, S. Mandal, S. Keller, and S. Chowdhury, IEEE Trans. Electron Devices **64**, 805 (2017).
[14]T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, Appl. Phys. Express **7**, 21002 (2014).
[15]S. Matsuda, T. Sato, H. Yoshimura, Y. Takegawa, A. Sudo, I. Mizushima, Y. Tsunashima, and Y. Toyoshima, in *Proceedings of the 1998 IEEE International Electron Devices Meeting IEDM, San Francisco, CA, USA, 6–9 December 1998* (1998), pp. 137–140.
[16]A. Takatsuka, Y. Tanaka, K. Yano, T. Yatsuo, Y. Ishida, and K. Arai, Jpn. J. Appl. Phys. **48**, 41105 (2009).
[17]Y. Zhang, M. Sun, H. Wong, Y. Lin, P. Srivastava, C. Hatem, M. Azize, D. Piedra, L. Yu, T. Sumitomo, N. A. de Braga, R. V. Mickevicius, and T. Palacios, IEEE Trans. Electron Devices **62**, 2155 (2015).
[18]R. J. Shul, L. Zhang, A. G. Baca, C. G. Willison, J. Han, S. J. Pearton, and F. Ren, J. Vac. Sci. Technol. **18**, 1139 (2000).
[19]Y. Zhang, K. H. Teo, and T. Palacios, IEEE Trans. Electron Devices **63**, 2340 (2016).
[20]Y. Zhang, H. Wong, M. Sun, S. Joglekar, L. Yu, N. A. Braga, R. V. Mickevicius, and T. Palacios, in *Proceedings of the 2015 IEEE International Electron Devices Meeting IEDM, Washington, DC, USA, 7–9 December 2015* (2015), pp. 35.1.1–35.1.4.