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This paper demonstrates the compensation of the intrinsic positive charges in Al_2O_3 gate dielectric by fluorine ions in GaN metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs). Negatively-charged fluorine ions diffused into the oxide from the AlGaN barrier during the 250 °C atomic layer deposition compensate the intrinsic positive charge present in the Al_2O_3. This compensation is key to control the threshold voltage (V_{th}) of enhancement-mode (E-mode) transistors. A comprehensive analytical model for the V_{th} of fluorinated MOS-HEMTs was established and verified by experimental data. This model allows the calculation of the different charge components in order to optimize the transistor structure for E-mode operation. Using the proposed charge compensation, the V_{th} increases with gate dielectric thickness, exceeding 3.5 V for gate dielectrics 25 nm thick. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4815923]

AlGaN/GaN high-electron-mobility transistors (HEMTs) have great potential for the next generation of power electronics. Standard AlGaN/GaN HEMTs are depletion-mode (D-mode) devices. However, enhancement-mode (E-mode) HEMTs with a threshold voltage (V_{th}) ~ 3 V[1] are highly desirable to simplify circuit design and to enable fail-safe operation[2] in power electronics. In order to achieve this, E-mode metal-oxide-semiconductor HEMTs (MOS-HEMTs) have been developed by combining a MOS gate structure with various techniques, including gate-recess,[3,4] dual-gate integration,[2] tri-gate structure,[5] fluorine plasma treatment,[6] among others. In addition, the use of a gate oxide suppresses the gate leakage,[2,5,7] improves the two-dimensional electron gas (2-DEG) transport characteristics[7] and device stability,[8] and should also facilitate a more positive V_{th} by capacitance modulation.[9] However, the gate oxide in GaN MOS-HEMTs has been shown recently to affect the V_{th} not only as a result of the lower gate capacitance of the increased gate-to-channel spacing, but also through interface and bulk charges/traps.[10] It has been shown that the V_{th} in GaN MOS-HEMT structures hardly increases, in fact sometimes it decreases, with the deposition of a thick Al_2O_3 gate oxide,[11] due to the presence of positive interface charges[11,12] and positive oxide bulk charges.[13] This has become a great challenge in the design of high-V_{th} E-mode MOS-HEMTs.[1] There is, therefore, a need for developing a technology to compensate the positive charges in the MOS structure.

In this work, we study the incorporation of fluorine ions in the gate dielectric of E-mode fluorinated MOS-HEMTs, and its impact on the threshold voltage modulation by the gate oxide thickness. A V_{th} higher than 3.5 V and an increase in V_{th} with increasing gate oxide thickness has been demonstrated experimentally. A comprehensive analytical model has also been proposed to quantify the contribution of different charges and fluorine effects to the high V_{th} of MOS-HEMTs and justify the experimental data. Detailed analysis of capacitance-voltage (C-V) and secondary-ion mass spectrometry (SIMS) measurements were used to clarify the origin of the different charges in the proposed model. These results support the use of fluorine and other charge-compensating ions in the gate dielectric layer to fabricate high-performance E-mode MOS-HEMTs.

The HEMT structure used in this work was a commercial wafer grown on a 6 in. Si substrate by metal-organic chemical vapor deposition. It consists of a 3 nm GaN cap/18 nm $Al_{0.26}Ga_{0.72}N$/1.2 μm i-GaN/2.8 μm buffer/p-type Si (111) substrate. The device fabrication starts with mesa isolation and Ti/Al/Ni/Au ohmic contact formation. Then the gate region of the devices was treated by CF_4 plasma in an electron-cyclotron-resonance (ECR) reactive ion etching (ECR-RIE) system at an ECR power of 150 W and an RF power of 20 W for three different times: 150 s, 160 s, and 170 s. These three plasma times introduce enough fluorine ions into the transistor structure to convert devices from depletion mode to enhancement mode, without severe 2-DEG mobility degradation and channel damage. The 3 nm GaN cap and the top 10 to 11.5 nm of the $Al_{0.26}Ga_{0.72}N$ layer were etched by the CF_4 plasma (150 s to 170 s), as measured by atomic force microscopy (Figure 1(a)). The etching depth was further verified by C-V and SIMS measurements (details shown in Figure 4). This etching is consistent with previous reports.[14,15] After CF_4 plasma treatment, the surface of the gate region was cleaned through a two-step process: a UV-ozone step at 260 °C for 10 min, followed by an HCl clean for 1 min. Al_2O_3 gate dielectrics with thickness of 8 nm, 15 nm, 20 nm, and 25 nm were then deposited by atomic layer deposition (ALD) at 250 °C. A Ni/Au gate electrode was then deposited covering the fluorinated region. Finally, the samples were annealed at 400 °C for 5 min in N_2 ambient to heal potential channel damage and activate the fluorine ions.[6] Transistors with a source-gate spacing of 1.5 μm, gate length of 3 μm and gate-drain spacing of 9 μm (Figure 1(b)), as well as circular MOS diodes with a

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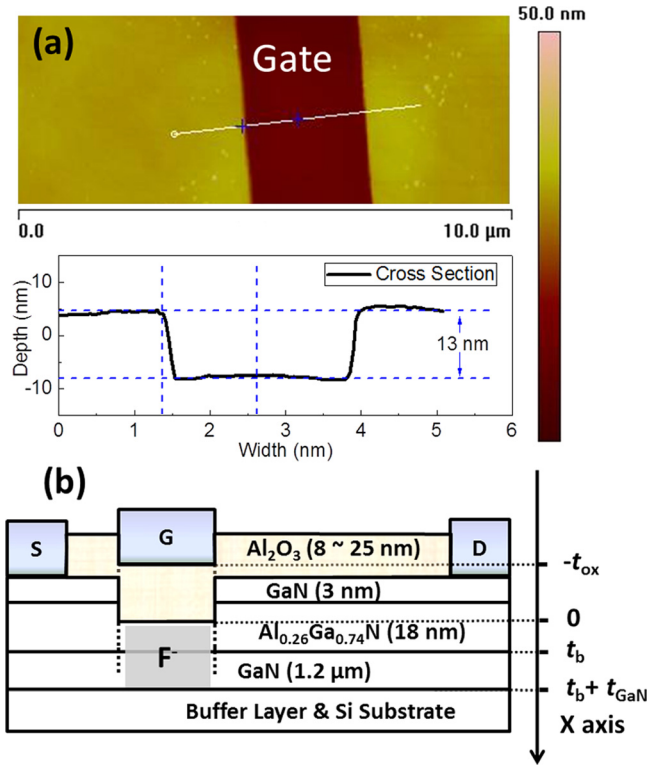

FIG. 1. (a) Atomic force microscope image of the gate region in a HEMT structure after 150 s CF_4 plasma treatment. The depth profile of the cutline reveals an etched depth of ~13 nm. (b) Schematic of the fabricated E-mode MOS-HEMT by fluorine plasma treatment.

diameter of 180 μm were fabricated in the same sample. In addition to the fluorinated devices, transistors and diodes with identical geometry and layer but without the fluorination step were also fabricated as a reference (standard).

Figures 2(a) and 2(b) show the transfer characteristics of standard and 150 s-plasma-treated MOS-HEMTs with different gate oxide thickness. In the literature, many different methods to extract the threshold voltage have been proposed, including transconductance extrapolation[5] and current extrapolation under linear[16] and saturation[2,3,17] operating conditions. However, these methods could suffer from uncertainties, since the current or transconductance characteristics can deviate from ideal straight line behavior in the threshold region.[17] Thus, in this work, a constant-current method, widely used for MOSFETs[17] and HEMTs,[18] was adopted to extract and compare the V_{th} of different devices. Here, the V_{th} is defined as the gate voltage when drain current reaches 10 μA/mm at $V_{ds} = 1$ V in the subthreshold region.[18] The transistor V_{th} defined in this way was found to be independent of V_{ds} (measured from $V_{ds} = 1$ V to $V_{ds} = 10$ V) and consistent with the capacitance turn-around point extracted from *C-V* curves of MOS diodes[10] (A typical *C-V* curve of the fluorinated MOS diodes is shown in Figure 4(a)).

The V_{th} of MOS-HEMTs as a function of oxide thickness for four fluorine treatment times (0, 150, 160, and 170 s) is summarized in Figure 3. As can be seen, a V_{th} that increases with gate oxide thickness was achieved for fluorinated MOS-HEMTs. This is opposite to the behavior of E-mode devices fabricated through gate recess, where the V_{th} hardly increases as the gate dielectric thickness is increased due to the fixed positive charges in Al_2O_3.[1]

The V_{th} dependence with oxide thickness and fluorine time in the fluorinated devices is far from linear, indicating a comprehensive analytical V_{th} model, including different charges and fluorine effect quantitatively is needed. By modifying the electrostatic V_{th} model for a standard MOS-HEMT,[10] the V_{th} for fluorinated MOS-HEMTs can be expressed as

$$V_{th} = \frac{\Phi_b}{q} - \frac{\Delta E_c}{q} - \frac{\Phi_f}{q} - \frac{qt_{ox}^2}{2\varepsilon_{ox}}\overline{n_{ox}} - \frac{qt_{ox}}{\varepsilon_{ox}} Q_{Al_2O_3/AlGaN} - q\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_{AlGaN}}\right) Q_{AlGaN/GaN} - \varphi_{Fluorine}, \quad (1)$$

where Φ_b is the metal barrier height for Ni on Al_2O_3 (i.e., 3.5 eV[10,12]), ΔE_c is the conduction band offset between Al_2O_3 and GaN (i.e., 2.1 eV[10,12]), Φ_f is the conduction band distance from the Fermi-level in GaN (~0.2 eV[10]). t is the thickness, ε is the permittivity, and the subscripts ox and b refer to the oxide (Al_2O_3) and barrier layer (AlGaN), respectively. $\overline{n_{ox}}$ is the average oxide bulk charge (per unit volume). $Q_{Al_2O_3/AlGaN}$ and $Q_{AlGaN/GaN}$ are the interface charge density at the Al_2O_3/AlGaN interface (more details below) and the AlGaN/GaN-channel interface ($+7 \times 10^{12}$ cm^{-2}, estimated by gated-Hall measurements of the 2-DEG sheet charge density).

$q\varphi_{Fluorine}$ is the conduction band shift induced by the fluorine plasma treatment. It has been reported that the main contributing factor to this band shift is not the change in the surface potential, but rather the negative fixed charges due to fluorine ions inside AlGaN/GaN heterostructures.[18,19] In this

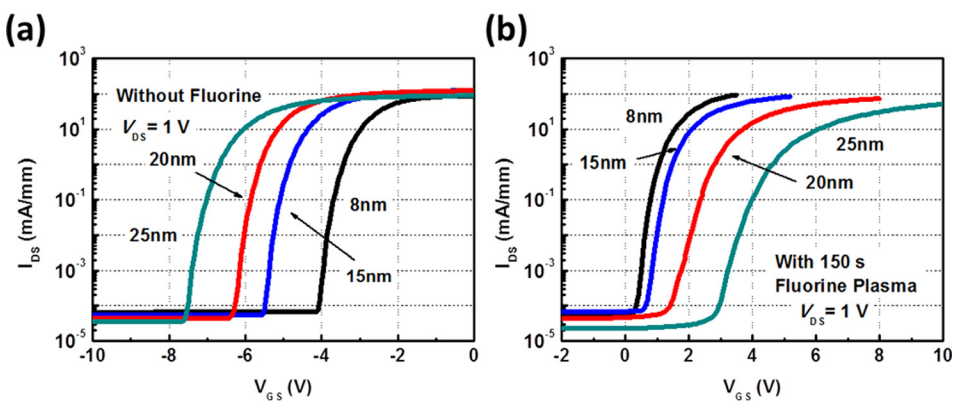

FIG. 2. The transfer characteristics of standard (a) and F-treated (b) MOS-HEMTs as a function of the gate oxide thickness. In the F-treated devices, the CF_4 plasma was applied for 150 s.

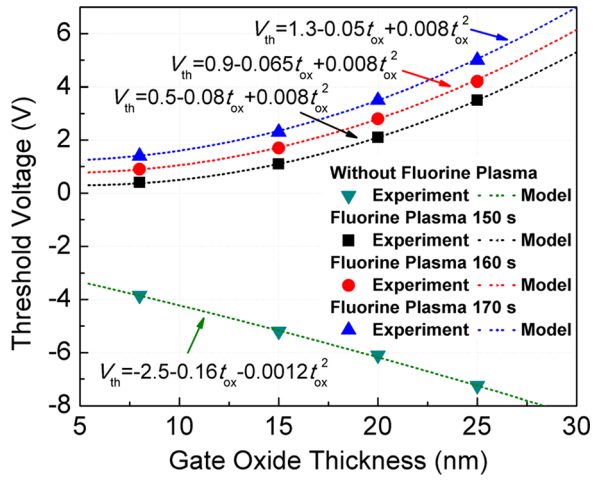

FIG. 3. V_{th} of standard and fluorinated MOS-HEMTs with the gate oxide thickness of 8 nm, 15 nm, 20 nm, and 25 nm by 150 s, 160 s, and 170 s fluorine plasma treatment measured in experiments (dots) and fitted by analytical models (dashed lines).

work, $\varphi_{\text{Fluorine}}$ is assumed to be the result of only negative fluorine charges. If we set the origin of the x axis ($x = 0$) at the Al_2O_3/AlGaN interface as shown in Figure 1(b), then $\varphi_{\text{Fluorine}}$ can be expressed as

$$\begin{aligned}\varphi_{\text{Fluorine}} &= \int_0^{t_b} q\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{x}{\varepsilon_{\text{AlGaN}}}\right) n_F(x)dx \\ &+ \int_{t_b}^{t_b+t_{\text{GaN}}} q\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_{\text{AlGaN}}} + \frac{x}{\varepsilon_{\text{GaN}}}\right) n_F(x)dx \\ &= \frac{qt_{ox}}{\varepsilon_{ox}} \int_0^{t_b+t_{\text{GaN}}} n_F(x)dx + \varphi(F) = \frac{qt_{ox}}{\varepsilon_{ox}} Q(F) + \varphi(F),\end{aligned} \tag{2}$$

where $n_F(x)$ is the effective fluorine negative charge density (per unit volume) in the AlGaN and GaN; $Q(F)$ is defined as a fluorine equivalent interface charge (per area) located at the AlGaN/Al_2O_3 interface calculated by integration of the fluorine negative charge in the bulk GaN and AlGaN; $q\varphi(F)$ is defined as a constant band bending only dependent on density of fluorine charge and distribution, but independent of the gate oxide thickness. By incorporating Eq. (2) into Eq. (1), we get

$$\begin{aligned}V_{th} = &\frac{\Phi_b}{q} - \frac{\Delta E_c}{q} - \frac{\Phi_f}{q} - \frac{qt_b}{\varepsilon_{\text{AlGaN}}} Q_{\text{AlGaN/GaN}} - \varphi(F) \\ &- \frac{q}{\varepsilon_{ox}}[Q_{\text{AlGaN/GaN}} + Q_{\text{Al}_2\text{O}_3/\text{AlGaN}} + Q(F)]t_{ox} \\ &- \frac{q\overline{n_{ox}}}{2\varepsilon_{ox}} t_{ox}^2.\end{aligned} \tag{3}$$

Equation (3) indicates that V_{th} can be described by a quadratic polynomial of the gate oxide thickness t_{ox} with the constant term and the first-order term directly dependent on fluorine plasma time. This relationship was verified by the excellent parabolic fitting achieved to the experimental V_{th} vs. t_{ox} for fluorinated MOS-HEMTs with different fluorine plasma time, as shown in Figure 3. On the other hand, a similar analytical model[10] without the fluorine-related terms was adopted to fit the experimental results on standard MOS-HEMTs. An excellent agreement between model and experiments was also achieved in this case, as shown in Figure 3. The schematic charge distribution and energy band diagram of the fluorinated MOS-HEMTs were shown in Figure 4. The fluoride-induced band bending $q|\varphi(F)|$, total equivalent Al_2O_3/nitride interface charges ($Q_{\text{Al}_2\text{O}_3/\text{AlGaN}} + Q(F)$ for fluorinated MOS-HEMTs and $Q_{\text{Al}_2\text{O}_3/\text{GaN}}$ for standard MOS-HEMTs) and average oxide bulk charge $\overline{n_{ox}}$ derived from fitting the model to the experimental results are summarized in Table I.

As shown in Table I, a large positive charge $Q_{\text{Al}_2\text{O}_3/\text{GaN}}$ was found at the oxide/nitride interface in standard MOS-HEMTs, which is consistent with previous reports.[10–12] In fluorinated MOS-HEMTs, negatively-charged fluorine ions inside the AlGaN/GaN layers, $Q(F)$, compensated the effect of positive interface charge, $Q_{\text{Al}_2\text{O}_3/\text{AlGaN}}$, making the equivalent total interface charge $Q_{\text{Al}_2\text{O}_3/\text{AlGaN}} + Q(F)$ become negative.

The interface charge ($Q_{\text{Al}_2\text{O}_3/\text{AlGaN}}$ or $Q_{\text{Al}_2\text{O}_3/\text{GaN}}$) has three different components:[10,11,20,21] (1) the sum of spontaneous and piezoelectric polarization charges, Q_P; (2) the contribution of the negatively charged oxide/AlGaN interface traps, Q_{it}; and, (3) the positively-charged ionized

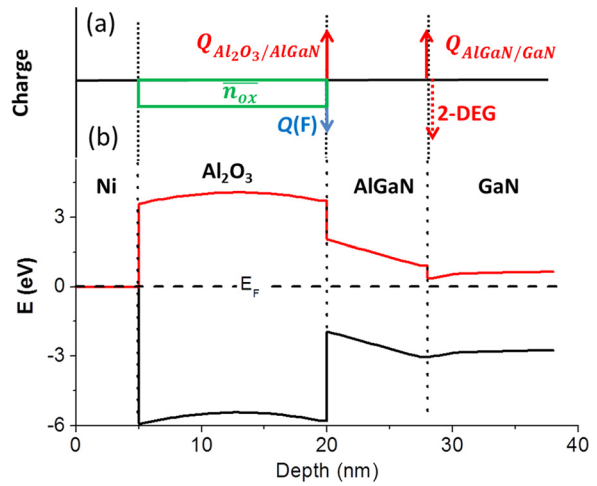

FIG. 4. (a) Schematic charge distribution in the fluorinated MOS-HEMT based on our analytical models for V_{th} calculation. (b) Energy band diagram of the fluorinated MOS-HEMT calculated by using the TCAD simulator—Silvaco Atlas based on our model.

TABLE I. Fluoride-induced band bending $q|\varphi(F)|$, total oxide/semiconductor interface charges ($Q_{\text{Al}_2\text{O}_3/\text{AlGaN}} + Q(F)$ for fluorinated MOS-HEMTs, $Q_{\text{Al}_2\text{O}_3/\text{GaN}}$ for standard MOS-HEMTs), and average bulk oxide charge $\overline{n_{ox}}$ as a function of fluorine plasma time for fluorinated and standard MOS-HEMTs, as derived from the analytical model.

Fluorine plasma time (s)	$q\|\varphi(F)\|$ (eV)	$Q_{\text{Al}_2\text{O}_3/\text{AlGaN}} + Q(F)$ ($Q_{\text{Al}_2\text{O}_3/\text{GaN}}$) ($\text{cm}^{-2}$)	$\overline{n_{ox}}$ (cm^{-3})
0	0	7.08×10^{12}	1.1×10^{18}
150	0.4	-3.46×10^{12}	-7.1×10^{18}
160	0.7	-4.12×10^{12}	-7.1×10^{18}
170	1.0	-4.78×10^{12}	-7.1×10^{18}

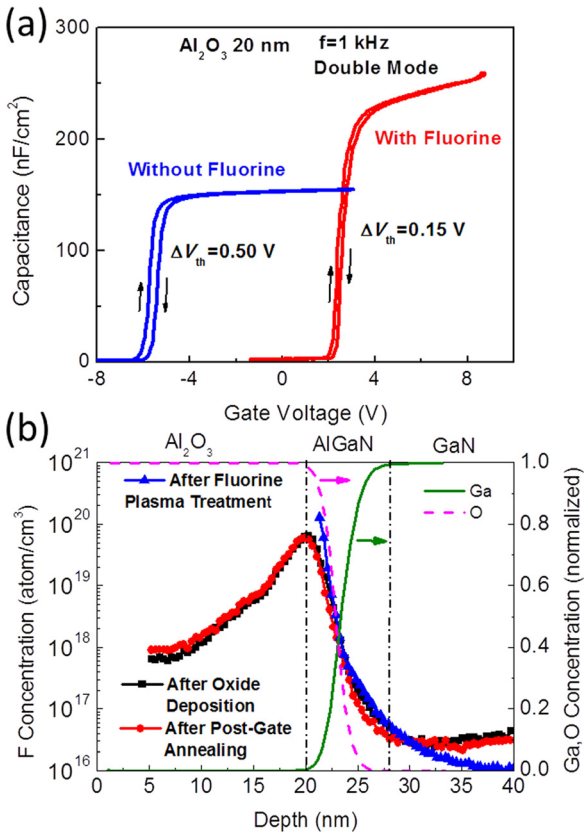

FIG. 5. (a) *C-V* characteristics of MOS diodes with 20 nm Al_2O_3 gate oxide untreated and treated by 150 s fluorine plasma. (b) F profile measured by SIMS in the MOS samples corresponding to different device fabrication steps. Ga and O profile (normalized by each peak concentration, respectively) indicated an AlGaN thickness of ~8 nm, which is consistent with the AFM results shown in Figure 1(a). It should be noted that it is difficult to accurately characterize the ^{19}F profile in the first ~5 nm oxide due to the interference with ^{19}[HO], of the same nominal mass; the ^{19}[HO] compound is probably formed by H adsorption on an oxide surface.

surface donors, Q_d. While Q_P and Q_d are difficult to separate experimentally, Q_{it} can be estimated from the *C-V* characterization of MOS capacitors.[10,21,22] Figure 5(a) shows the typical *C-V* characteristics of standard and plasma-treated MOS capacitors. As can be seen, the hysteresis ΔV_{th} in the *C-V* curve of fluorinated MOS capacitor is smaller than the hysteresis of a standard MOS capacitor. Using $Q_{it} \approx C_{MOS} \cdot \Delta V_{th}/q$,[22] the Q_{it} in fluorinated MOS-HEMTs was estimated as $\sim -2.3 \times 10^{11}\,\mathrm{cm}^{-2}$, which is one-order of magnitude smaller than the total equivalent interface charges $Q_{Al_2O_3/AlGaN} + Q(F)$ shown in Table I, indicating that Q_{it} is not a major contribution to interface charges. A detailed analysis for the fluorine passivation of interface states will be presented in a future paper.

A constant bulk oxide charge, $\overline{n_{ox}}$, is sufficient in our model to get excellent agreement with the experimental data for fluorinated MOS-HEMTs. This charge density, $-7.1 \times 10^{18}\,\mathrm{cm}^{-3}$, is much more negative than the intrinsic bulk oxide charge density revealed in our standard MOS-HEMTs ($+1.1 \times 10^{18}\,\mathrm{cm}^{-3}$) or reported by other groups for ALD-grown Al_2O_3 on GaN[10] and other III-V,[13] indicating the presence of additional charges. The SIMS measurements shown in Figure 5(b) indicate that these additional charges are due to fluorine ions diffusing into the gate oxide during the ALD process at 250 °C. The post-gate annealing at 400 °C almost did not change the fluorine distribution in the structure. The fluorine ions passivated the intrinsic positive oxide charges and formed negative charges during high-temperature ALD and annealing possibly by virtue of the strong electronegativity of F. If we use the Gaussian characteristics to approximate the fluorine concentration distribution measured by SIMS, and then the total fluorine ion amount can be integrated and compared with the average bulk oxide charge revealed by our model. In this way, the "activation percentage" of the negatively charged fluorine ions in Al_2O_3 gate oxide was estimated to be 40–50%. The dynamic and microscopic picture of F-induced charge diffusion and incorporation into the oxide still require a more detailed study.

In conclusion, fluorine ions introduced in the gate dielectric during the ALD deposition compensate the intrinsic positive charge of Al_2O_3, enabling the accurate control of V_{th} by changing the gate oxide thickness. A comprehensive analytical model for the V_{th} modulation was proposed and verified by experimental data to quantitatively study the negative charge introduced in the dielectric by the fluorination process. The proposed fluorine plasma treatment before the ALD gate oxide deposition can be utilized in combination with other E-mode MOS-HEMT technologies, such as gate recess, tri-gate, and band engineering, to compensate the positive charges in the Al_2O_3 gate dielectric and achieve a more positive V_{th}.

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[1]S. G. Khalil, R. Chu, R. Li, D. Wong, S. Newell, X. Chen, M. Chen, D. Zehnder, S. Kim, A. Corrion, B. Hughes, and K. Boutros, in *Proceedings of the 42th European Solid-State Device Research Conference, Bordeaux, France, 17–21 Sept.* (IEEE, 2012), pp. 310–313.
[2]B. Lu, O. Saadat, and T. Palacios, IEEE Electron Device Lett. **31**, 990 (2010).
[3]M. Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, T. Imada, A. Yamada, and N. Hara, IEEE Electron Device Lett. **31**, 189 (2010).
[4]H. Kambayashi, Y. Satoh, S. Ootomo, T. Kokawa, T. Nomura, S. Kato, and T. P. Chow, Solid-State Electron. **54**, 660 (2010).
[5]B. Lu, E. Matioli, and T. Palacios, IEEE Electron Device Lett. **33**, 360 (2012).
[6]C. T. Chang, T. H. Hsu, E. Y. Chang, Y. C. Chen, H. D. Trinh, and K. J. Chen, Electron. Lett. **46**, 1280 (2010).
[7]Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, and V. Sahmuganathan, Appl. Phys. Lett. **95**, 223501 (2009).
[8]V. Adivarahan, J. Yang, A. Koudymov, G. Simin, and M. A. Khan, IEEE Electron Device Lett. **26**, 535 (2005).
[9]R. Wang, Y. Cai, C. W. Tang, K. M. Lau, and K. J. Chen, IEEE Electron Device Lett. **27**, 793 (2006).
[10]M. Ťapajna and J. Kuzmík, Appl. Phys. Lett. **100**, 113509 (2012).
[11]S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena, Appl. Phys. Lett. **99**, 193504 (2011).
[12]M. Esposto, S. Krishnamoorthy, D. N. Nath, S. Bajaj, T. H. Hung, and S. Rajan, Appl. Phys. Lett. **99**, 133503 (2011).
[13]B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, Appl. Phys. Lett. **96**, 152908 (2010).
[14]R. Chu, C. S. Suh, M. H. Wong, N. Fichtenbaum, D. Brown, L. McCarthy, S. Keller, F. Wu, J. S. Speck, and U. K. Mishra, IEEE Electron Device Lett. **28**, 781 (2007).
[15]R. Chu, L. Shen, N. Fichtenbaum, D. Brown, S. Keller, and U. K. Mishra, IEEE Electron Device Lett. **29**, 297 (2008).

[16]B. Lu, M. Sun, and T. Palacios, IEEE Electron Device Lett. **34**, 369 (2013).
[17]A. Ortiz-Condea, F. J. García Sáncheza, J. J. Liou, A. Cerdeirac, M. Estrada, and Y. Yue, Microelectron. Reliab. **42**, 583 (2002).
[18]C. Ma, H. Chen, C. Zhou, S. Huang, L. Yuan, J. Roberts, and K. J. Chen, J. Appl. Phys. **110**, 114514 (2011).
[19]S. Huang, H. Chen, and K. J. Chen, Appl. Phys. Lett. **96**, 233510 (2010).
[20]M. Fagerlind, F. Allerstam, E. Ö. Sveinbjörnsson, N. Rorsman, A. Kakanakova-Georgieva, A. Lundskog, U. Forsberg, and E. Janzén, J. Appl. Phys. **108**, 014508 (2010).
[21]C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, Jpn. J. Appl. Phys. Part 1 **50**, 021001 (2011).
[22]S. Huang, S. Yang, J. Roberts, and K. J. Chen, Jpn. J. Appl. Phys. Part 1 **50**, 110202 (2011).