Development of an Isolated Flyback Converter Employing Boundary-Mode Operation and Magnetic Flux Sensing Feedback
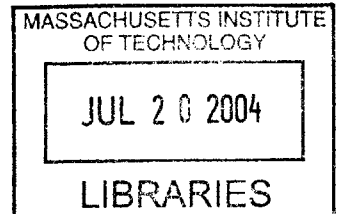
by

Mayur V. Kenia

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering

at the Massachusetts Institute of Technology May 26, 2004

Copyright 2004 Mayur V. Kenia. All rights reserved.

Author_____

Department of Electrical Engineering and Computer Science
May 17, 2004

Certified by_____   _____
Tony Bonte
VI-A Company Thesis Supervisor

Certified by_____   _____
David Perreault
M.I.T. Thesis Supervisor

Accepted by_____   _____
Arthur C. Smith
Chairman, Department Committee on Graduate Theses

Development of an Isolated Flyback Converter Employing Boundary-Mode Operation and Magnetic Flux Sensing Feedback

by

Mayur V. Kenia

Abstract

This thesis focuses on the marriage of magnetic-flux-sensing feedback and boundary-mode operation in a flyback converter to create a simple, small, low-cost, isolated, and tightly regulated power supply. Although each technique has been implemented before, the marriage of these two concepts is new. The union of these two techniques is powerful in terms of simplifying the overall design. The same signal, the flyback pulse on the bias winding, controls the feedback loop and the turn-on of the switch. In the process of building an isolated power supply, a complete understanding of the benefits and disadvantages of various operational modes along with other design options are explored. The flyback converter was built using discrete parts including op-amps, comparators, and other analog building blocks. The goal was to create a proof of concept board to test the overall effectiveness of the new topology in a simple, quick manner.

MIT Thesis Supervisor: David Perreault

VI-A Thesis Supervisor: Tony Bonte

Table of Contents

Table of Figures

1 Introduction

Modern technology continues to move towards smaller more densely packed board solutions. Higher component density places pressures on all parts of a design to either miniaturize components or build simpler solutions. One area that pushes toward smaller more efficient designs is the power delivery market. With the advent of more functional blocks and size constraints in new technology, the importance of good power design is essential. Increased amounts of circuitry require more power along with various voltage levels. The processor may require 3V while another electronic subsystem requires 5V. At the same time, the power solution must not waste too much energy during conversion since lost energy is converted to heat that must eventually be removed with large heat sinks or fans. Thus the need to develop efficient, small, and simple power supplies has become a key goal of many power electronic designers. Component sizes have become smaller, but larger gains are made on the power side removing components from a design completely.

One area being pushed in both size and simplicity is the design of isolated power supplies. Isolated power supplies require more external components and complexity to ensure true isolation and regulation of the output. For example, opto-couplers have been historically used to traverse the isolation boundary and close the feedback loop for regulation. The use of opto-couplers increases design complexity by requiring board space and many discrete components including the opto-coupler [1].

Simplicity, small solution size, isolation, and tight output regulation have not been effectively combined into one solution, and typically require tradeoffs in one for another. The thesis presents an isolated power supply solution that addresses the collective constraints in an elegant manner.

1.1 Flyback Background

The flyback converter is a type of switching converter known as an indirect converter, one that stores all converted energy in an intermediate stage before transferring it to the output. The converter is derived and based on the buck-boost converter shown in Figure 1-1. If one examines the inductor in Figure 1-1, a set of coupled inductors can replace the single inductor without changing the operation of the circuit.
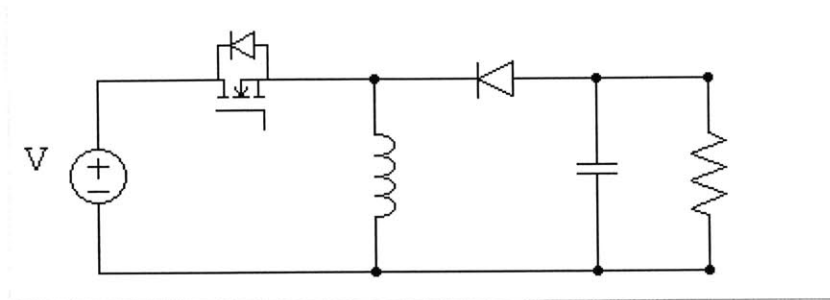
Figure 1-1: Buck-Boost Topology.

If the coupled inductors are separated and rearranged, the flyback converter is created. The flyback converter is shown in Figure 1-2 below.
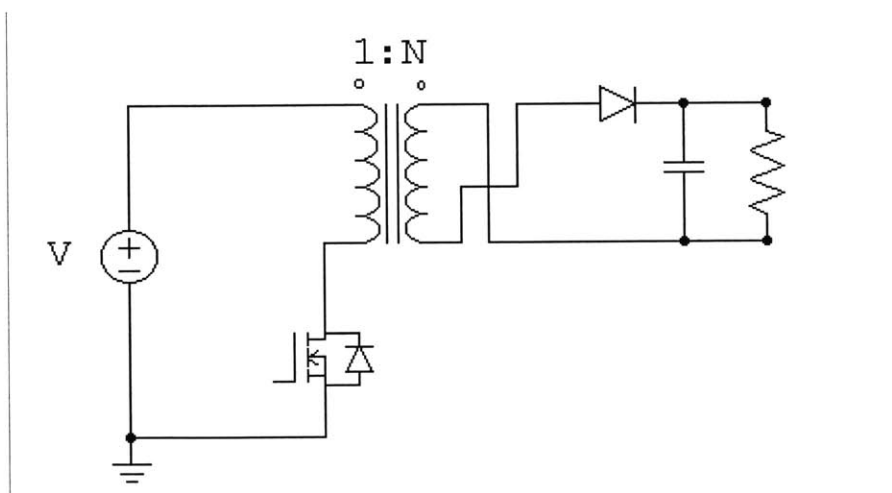
Figure 1-2: Flyback Topology.

The operation of the flyback converter is similar to the buck-boost except for the differences related to using a transformer instead of an inductor as the intermediate energy storage stage. For example, the flyback converter is able to regulate the output voltage at either negative or positive polarity with respect to the input voltage depending on the phasing of the output winding with respect to the primary. In the buck-boost

topology the output voltage must have a polarity opposite to the input voltage to ensure volt-second balance across the inductor. In addition, the transformer's turns ratio provides a simple way to produce output voltages that are highly scaled with respect to the input voltage, i.e. either step-up or step-down. The input-output relationship of the two converters with respect to duty cycle is shown in figure 1-3. The flyback has an additional multiplier of N; the turns ratio provides a handle on transforming across wide DC levels at reasonable duty cycles.

$$\frac{Vout}{Vin} = -\frac{D}{(1-D)} \qquad\qquad \frac{Vout}{Vin} = N \times \frac{D}{(1-D)}$$

Buck-Boost   Flyback

Figure 1-3: Input to output relationships

1.2 Isolation

Another very important feature of flyback converters resides in their ability to provide isolation between the input and output. Offline power supplies and supplies for commercial applications such as telecommunications require galvanic isolation. Isolation is required not only electrically but also mechanically. Agencies like the IEC, VDE, and UL set specifications for the required level of isolation in various types of equipment. The main reason for isolation is for safety to prevent any kind of shock hazard when using a piece of equipment. Many types of equipment operate from large input voltages that increase the potential for shock if the user is subjected to input voltage levels. In addition to providing safety, isolation is used to separate sections of a system from one another. For example, sensitive low power circuitry needs to be isolated from high power circuitry to ensure proper operation and measurements [6].

In the case of switching power supplies, the transformer provides the main form of isolation between input and output. The isolation inherent in the transformer is both electrical and mechanical. The windings within the transformer have insulation layers to prevent shorts between windings. One drawback of isolation through the transformer is that the output is completely separate from the input side circuitry. In order to provide regulation of the output voltage, the primary side control circuitry needs information about the output. Therefore isolation through the transformer requires some sort of

9

method for crossing the isolation boundary to feedback control information. A popular method for crossing the isolation boundary is with an opto-coupler. An opto-coupler sends information optically across the isolation boundary. Other methods of sending information across the boundary exist with each having its own level of accuracy.

The thesis investigates another form of crossing the isolation boundary known as magnetic flux sensing. The method is introduced in a later section and its advantages over other methods are discussed.

1.3 Areas of Investigation

Designing a flyback converter requires a wide expanse of understanding across a variety of components and disciplines. For example, the power components include a transformer, switch, output diode, and capacitor. Entire books have been dedicated to transformer design and optimization for specific applications. In addition to the power components, flyback design requires control theory understanding along with the principles of switching power supply theory.

The thesis focuses more on the novel concepts introduced in designing an isolated boundary mode flyback converter using magnetic flux sensing feedback. Additional time would have allowed more time in examining optimizations related to power components, efficiency losses, and an integrated circuit level controller implementation. Instead a rough overview in various areas such as understanding efficiency losses is covered, while more in depth discussion covers the ideas of building a boundary mode controller and the challenges in designing a simple, accurate, and isolated control scheme.

2 Operational Modes

2.1 Operational Characteristics

Many different flavors of flyback converters exist. A flyback converter can be implemented with or without isolation depending on the requirements of the design. In addition to isolation, a flyback can operate in various operational modes; including continuous conduction mode (CCM), boundary conduction mode (BCM), or discontinuous conduction mode (DCM).

2.1.1 Continuous Conduction Mode (CCM)

In continuous conduction mode (CCM), the magnetizing inductance of the transformer starts from a nonzero current condition when the switch turns on and requires cycle-to-cycle energy storage in the transformer. CCM flyback circuits are typically implemented in fixed frequency applications. Figure 2-1 shows both the primary and secondary currents in CCM. The secondary current does not return to zero, and hence requires the transformer to store energy across cycles. Also when the load current is varied in a CCM flyback, the DC energy stored in the transformer responds accordingly. For example if a higher amount of load current is drawn from the output, the controller will ensure that the transformer moves to a higher current level from which it starts and ends during each cycle. The amount of energy transferred to the load increases since the inductor stores energy according to $\frac{1}{2} LI^2$.
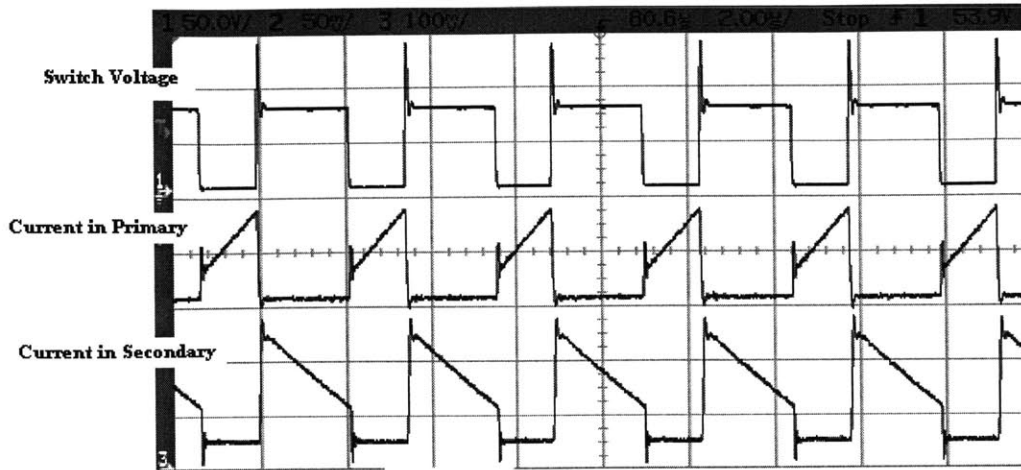
Figure 2-1: Current waveforms in fixed frequency CCM.

2.1.1.1 Steady State Equations

The following section details some basic operational equations that are used throughout this paper to understand, model, and compare CCM operation to other operational modes.

$$\text{Duty Cycle} = \frac{Vout + Vd}{Vin \bullet N + Vout + Vd} \approx \frac{Vout}{Vin \bullet N + Vout}$$

Frequency = constant, set externally

$$\text{Switch peak current and turn on current} = \frac{Iout \cdot N}{1 - D} + \frac{Vin \cdot D}{2 \cdot Lpri \cdot f}$$

$$\text{Diode turn on and off currents} = \frac{IswPk}{N}$$

Short hand abbreviations used throughout the paper:

D = Duty Cycle   Vin = Input voltage

N = Transformer turns ratio   Vout = Output voltage

f = frequency of operation   Vd = Diode forward voltage

Lpri = Transformer primary inductance   Iout = Output current load

IswPk = Switch peak current

12

2.1.1.2 Steady State Data

The data below shows confirmation of the equations presented above. Figure 2-2 shows the switch peak current measured and predicted. The first predicted curve has no correction for efficiency, but the second predicted curve assumes 80% efficiency.
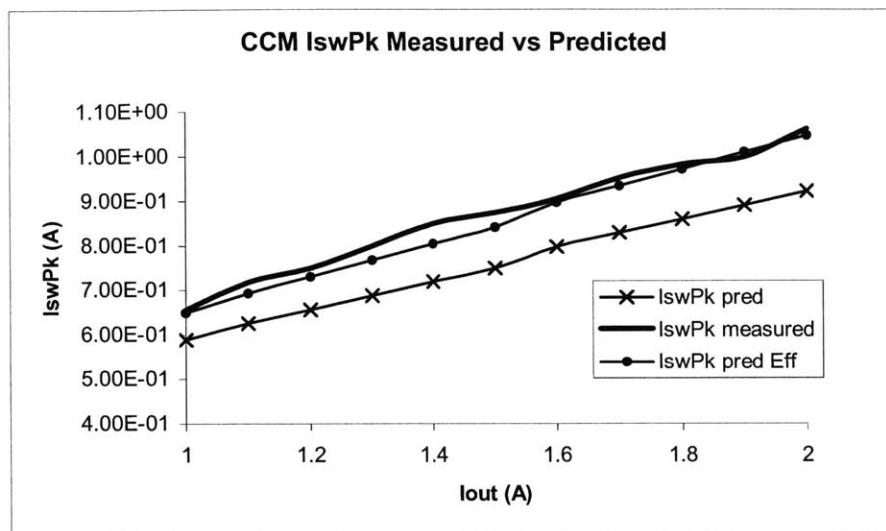
Figure 2-2: CCM Switch peak current measured versus equation model for 48Vin, 5Vout, a turns ratio of 0.2, and a duty ratio of 0.34.

Figure 2-3 presents the diode on current in CCM mode from one amp to two. The data shows that the modeled switch peak current is a good representation of the output diode current. No correction for efficiency is needed here because the measured diode current is very close to the output current with very few losses in between. The equations used to model the diode current are predicted using the output current levels.

13

CCM Idiode On- Measured vs Predicted
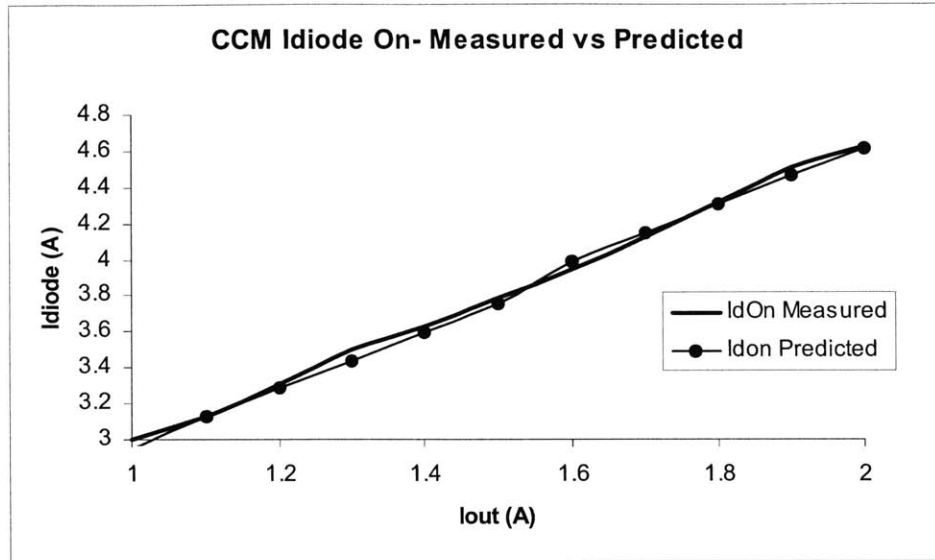
Figure 2-3: CCM Diode peak on current measured versus equation model at 48Vin, 5Vout, a turns ratio of 0.2, and a duty ratio of 0.34.

2.1.2 Boundary Conduction Mode (BCM)

Another operational mode of interest for this thesis is known as boundary conduction mode. The name boundary conduction mode comes from the fact that the controller operates right on the boundary between CCM and DCM. In other words, the switch turns on and stores just enough charge to replenish the load during the time the switch opens. Thus the switch turns on again as soon as all the energy is transferred to the output. The controller ensures that there is very little time when the transformer has no energy stored as flux, known as dead time. Figure 2-4 shows typical current waveforms describing boundary mode operation.

14
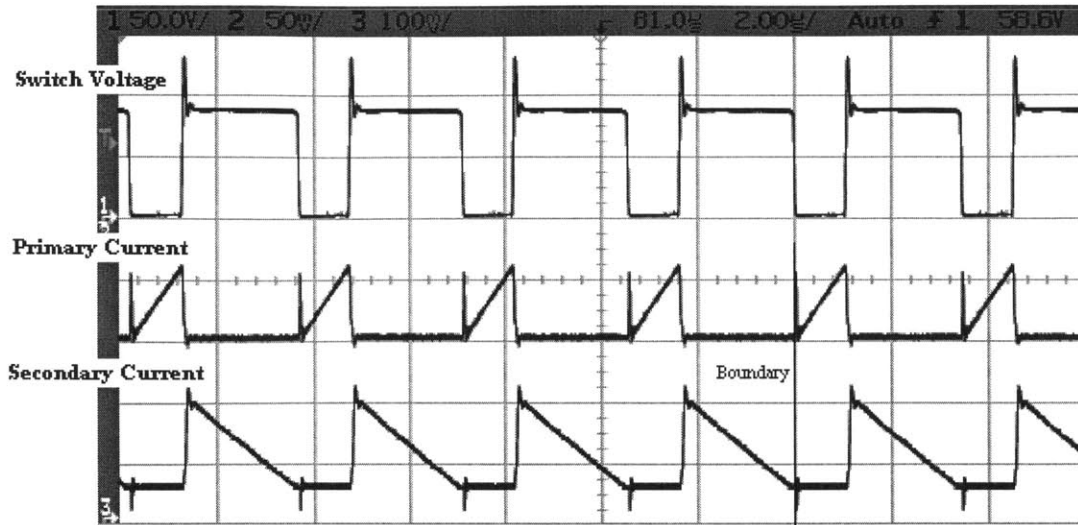
Figure 2-4: Current waveforms in boundary-mode

The point where the switch is turned on and current begins to ramp in the primary occurs as soon as the current returns to zero in the secondary. Depending on the load and the input voltage, the primary current must reach a different level to ensure output regulation. Since switching occurs after all the energy is transferred, the operating frequency is dependent on line and load conditions.

2.1.2.1 Steady State Equations

$$\text{Duty Cycle} = \frac{Vout + Vd}{Vin \cdot N + Vout + Vd} \approx \frac{Vout}{Vin \cdot N + Vout}$$

$$\text{Frequency} = \frac{D \cdot Vin \cdot (1 - D)}{2 \cdot Iout \cdot N \cdot Lpri}$$

$$\text{Switch peak current} = \frac{2 \cdot Iout \cdot N}{1 - D}$$

2.1.2.2 Steady State Data

The data presented in the graphs below show confirmation that the equations above accurately predict the measured features of the BCM circuit. Figure 2-5 presents data showing the frequency of the BCM board measured versus predicted frequency values. The second predicted curve assumes 80% efficiency to more closely match the

15

measured data. The efficiency is incorporated because the equations were derived assuming power conservation from input to output.
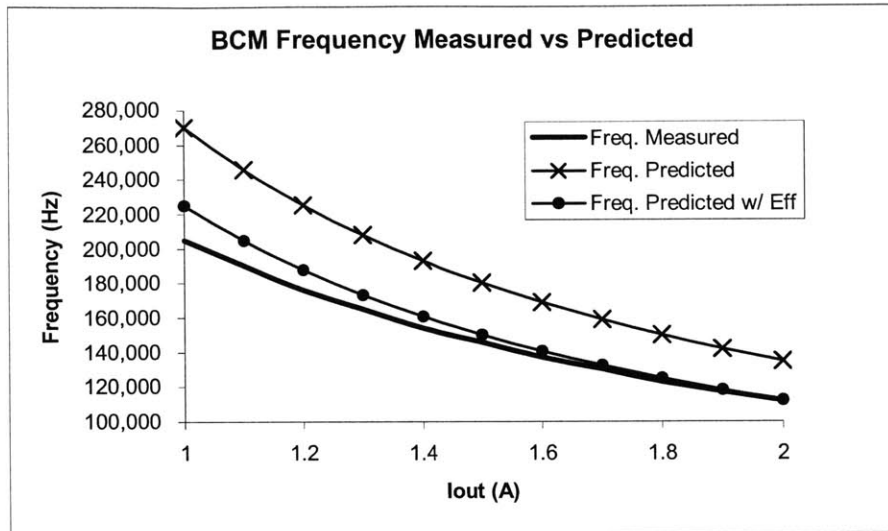
Figure 2-5: BCM frequency measured versus equation model at 48Vin, 5Vout, a turns ratio of 0.2, and a duty ratio of 0.34.

Figure 2-6 below show the switch peak current from one amp to two amps for the BCM board. It presents both the measured and predicted curves for peak switch current. The second predicted curve assumes 80% efficiency to more accurately represent the actual switch peak currents.
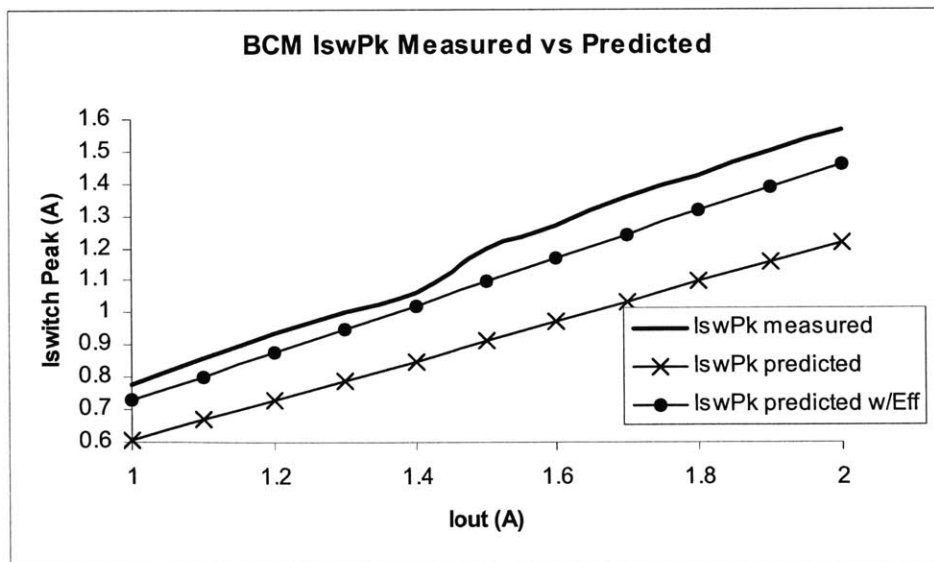
Figure 2-6: BCM Switch peak current measured versus equation model at 48Vin, 5Vout, turns ratio of 0.2, and a duty ratio of 0.34.

2.1.3 Discontinuous Conduction Mode (DCM)

In discontinuous conduction mode (DCM) stored transformer energy and current start and return to zero in each cycle. In discontinuous mode the transformer never has to store energy across cycles. In other words, the energy stored in the primary when the switch turns on is completely transferred to the output through the secondary after the switch opens. The time when the switch is open and energy is not transferred to the load is known as dead time. Figure 2-7 shows DCM operation and the notion of dead time.
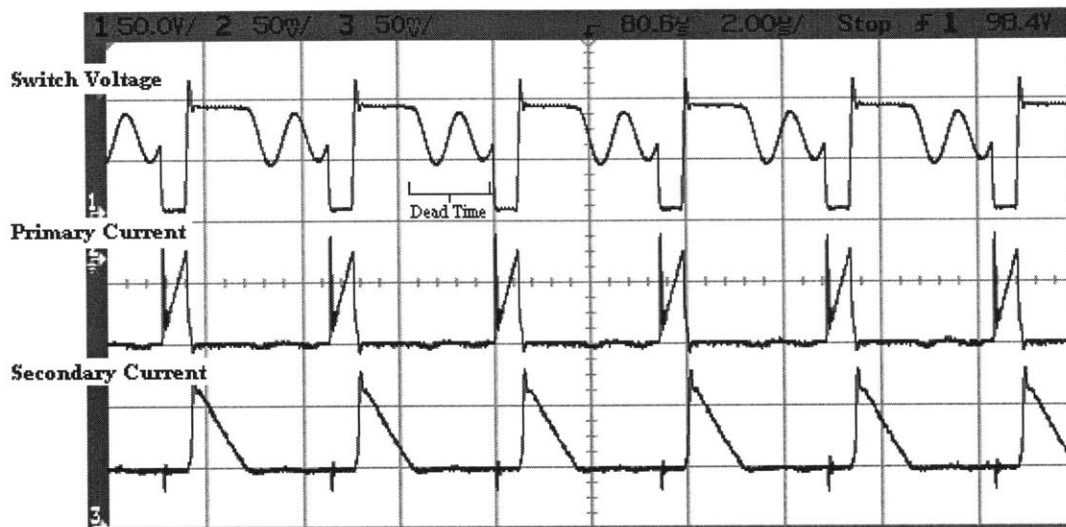
Figure 2-7: Current and switch waveforms in DCM.

DCM mode can be implemented in a variety of ways. For example, DCM flybacks are typically built with a fixed frequency of operation, but they are also designed with fixed switch on times.

2.1.4 Typical Implementations

The three operational modes describe the different strategies that can be used to control a flyback converter. A large majority of flyback converters built are fixed frequency and operated in DCM for their entire line and load range [1]. Fixed frequency operation is desirable for input and output filtering along with EMI issues. Filtering is easier because the filters do not have to cover a wide frequency range. In addition, known

17

frequency operation identifies the source and frequencies of EMI that the switcher will generate over is line and load range.

Flyback controllers can operate exclusively in one operational mode for their line and load range, but can also switch between modes of operation. For example, a flyback converter can be designed to operate in CCM for high loads and then transition to DCM for light loads. This transition point is set through the design of the converter. Another combination viable involves BCM and DCM. A flyback can be designed to operate in BCM for high loads and enter DCM at light loads. In BCM the flyback operates at a variable frequency that is varies with the output load for a given input voltage and output voltage. Entering DCM allows the flyback to deal with light loads without operating at high frequencies. If the flyback remained in BCM, then the operational frequency would increase to infinity to handle lighter output loads.

DCM operation is very similar to BCM operation because the transformer is not required to store energy across cycles. This fact leads the two operational modes to share similar operational characteristics, advantages, and disadvantages. For this reason a comparison of CCM and BCM would provide more insight into the advantages and disadvantages of each operational strategy. A clearer understanding of the differences would result in a better sense of the tradeoffs related to choosing one operational method over the other.

2.2 Comparison of CCM and BCM

During the process of comparison, advantages and disadvantages of both types of topologies will be studied and compared. Many advantages are thought to exist with the boundary-mode of operation, making it a better design option, but these suppositions need to be fully explored. The two main areas of comparison will be in terms of loss mechanisms and operational advantages.

2.2.1 Loss mechanisms

Four basic loss mechanisms are studied and detailed to compare the two operational modes. The mechanisms include conduction losses, switching losses, diode loss, and transformer losses. The losses will be supported by data from calculations based

18

on running a board at 48 volts in and 5 volts out at two-output current levels of one and two amps. The turns ratio of the transformer is 0.2. The current levels are set here to ensure that both boards remain in their respective mode and do not enter DCM. In addition, similar components in the flyback circuit will be used including diode, MOSFET, current sense resistor, and transformer. The goal of this comparison is to get a first order understanding of all the major loss mechanisms inherent to each operational strategy. The calculated losses are not exact. For example typical numbers for FET on resistance were used to calculate power loss. The value for FET on resistance was set at 0.07 Ohms. The data used operational data used in the calculations is presented in figure 2-8.

BCM/CCM Comparison Data

	Load	Vin (V)	Iin (A)	Vout (V)	Duty Cycle	Isw at Turn On (A)	Isw at Turn Off (A)	Freq. (Hz)	Idiode-On (A)	Idiode-Off (A)		Irms Sw (A)	Irms Diode (A)
BCM	1A	48.05	0.128	5.003	0.35	0	0.76	224,000	3.54	0		0.260	1.648
	2A	48.01	0.264	5.001	0.35	0	1.46	119,000	6.94	0		0.499	3.230
CCM	1A	47.9	0.13	4.968	0.35	0.096	0.644	291,000	2.94	0.26		0.244	1.457
	2A	47.91	0.263	5.034	0.35	0.41	0.988	289,000	4.66	2		0.440	2.851

Figure 2-8: BCM/CCM Operational data

2.2.1.1 Conduction Losses

Conduction losses are the first area of comparison. Conduction losses are grouped as DC losses incurred across resistances in the power path. For example, I^2R losses occur across both the on resistance of the MOSFET and across the current sense resistance. It is important to note that in determining the correct value of the loss terms here, the current used in calculating the loss must be the RMS current. For example for the RMS equation for the switch current is presented below in figure 2-9 and 2-10. The first equation assumes a periodic and linearly increasing switch current that resets to zero at the beginning of each cycle. The second equation assumes some residual dc current level that the switch current starts from at the beginning of each cycle.

19

$$RMS = I_{pk} \cdot \sqrt{\frac{D}{3}}$$
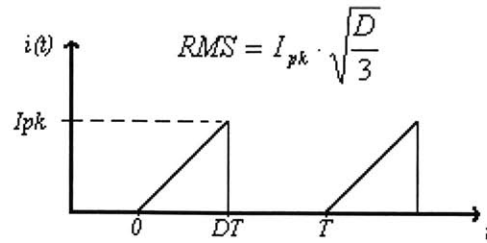
Figure 2-9: RMS conversion for BCM current waveforms.

$$RMS = I\sqrt{D} \cdot \sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2}$$
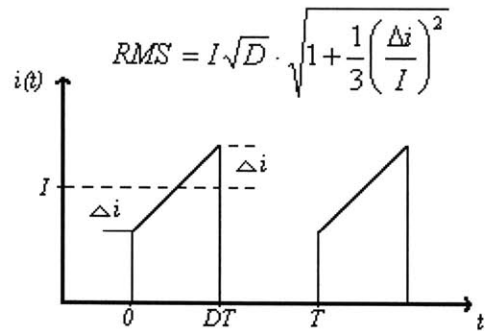
Figure 2-10: RMS conversion for CCM current waveforms.

In terms of the two application boards, both the resistances and the respective losses are detailed in the chart below.

MOSFET On Resistance   .07 Ohm
Current Sense Resistance   .1   Ohm

	Current Load	FET On Resistance Loss (W)	Sense Resistance Loss (W)		Total Loss (W)
BCM	1A	4.73E-03	6.76E-03		1.15E-02
	2A	1.74E-02	2.49E-02		4.23E-02
CCM	1A	4.17E-03	5.95E-03		1.01E-02
	2A	1.36E-02	1.94E-02		3.29E-02

Figure 2-11: Conduction power loss data.

The power loss figures in the chart above were calculated using both the resistance data and the data summarized in Figure 2-11 above. The RMS current values were used to calculate losses using the simple formula I^2R. The data above shows that the conduction losses in both the switch and sense resistance are higher for BCM than CCM. The power loss data makes sense since the RMS current levels are higher for BCM control strategy.

20

2.2.1.2 Switching Losses

Another important loss mechanism is switching losses. Switching losses are characterized by the losses that are directly related to the frequency at which the circuit switches. Three important switching loss mechanisms that were investigated include MOSFET switching loss, transition losses occurring in the switch and diode, and finally leakage inductance losses.

The first loss mechanism is related to switching the MOSFET on and off. Switching a FET on requires enough energy to charge the gate capacitance. The charge stored in the gate of the FET must then be discharged once the FET turns on. Unfortunately the charge used to charge the FET is not recycled and is lost during each cycle. This loss mechanism can become very significant at higher frequencies of operation. The switching loss can be written as $Q_g V_{gs} f$. Q_g is the total gate charge, V_{gs} is the gate to source voltage, and f is the switching frequency. The chart in figure 2-12 presents the MOSFET switching loss data for the BCM and CCM board. The gate drive of the MOSFET charges the gate to 10V during each cycle.

MOSFET Total Gate Charge (C)   4.20E-08
Gate-Source Voltage (V)   10

	Current Load	frequency (Hz)	Switching Loss (W)
BCM	1A	224,000	0.094
	2A	119,000	0.050
CCM	1A	291,000	0.122
	2A	289,000	0.121

Figure 2-12: MOSFET switching loss data.

The data in the chart shows that the switching loss is higher in the CCM board. In addition, it shows that while the CCM switching loss data stays constant over load, the BCM MOSFET loss actually decreases with increasing load as the frequency lowers. BCM MOSFET switching loss will always be lower than the CCM board as long as its operational frequency is lower than a similar CCM board. It is also important to note that for the same given transformer and input/output conditions, the boundary mode will

always operate at a lower frequency. The comparison of the case where the transformer is optimized for each operational mode is less clear.

The second switching loss results from transition loss across both the switch and the diode. For example, at switch turn on, the voltage across the switch collapses as current in the switch increases. In other words, the current does not begin to rise after the voltage across the switch collapses. Instead the two changes overlap and the crossover between voltage and current leads to power loss. The power loss is a function of frequency because the overlap between voltage and current is fixed and a function of the components. In a similar manner, transition losses are incurred on both the turn on and off of the switch and the diode. It was difficult to determine a good way to accurately measure transition losses. The problem arises in the fact that the measurement losses related to transition losses were much smaller than other losses from the conduction losses and other loss mechanisms. Instead a roughly theoretical comparison will be made here between the two switching strategies.

Figure 2-13 shows the transition data that was used to theoretically determine loss data. The data is listed in the chart in figure 2-14 to show the transition levels in both the current and voltage.

Transition Times

| Turn On time | 50ns |
| Turn Off time | 50ns |

	Current Load	frequency (Hz)	Isw-On (A)	Isw-Off (A)	Idiode-On (A)	Idiode-Off (A)	Vsw On (V)	Vsw Off (V)
BCM	1A	224,000	0-0	0.76-0	0-3.54	0-0	53-0	0-76
	2A	119,000	0-0	1.46-0	0-6.94	0-0	53-0	0-76
CCM	1A	291,000	0-0.096	0.644-0	0-2.94	.26-0	76-0	0-76
	2A	289,000	0-0.41	0.988-0	0-4.66	2-0	76-0	0-76

Figure 2-13. Switch and diode transition data.

Power Loss Calculations

	Sw Turn On Loss	Sw Turn Off Loss	Diode Turn On Loss	Diode Turn Off Loss	Switching Power Loss (W)	Switching Power Loss (W) for ton=toff=50ns
BCM	0	9.63*toff	.59*ton	0	(.59*ton+9.63*toff)*224,000	0.115
	0	18.49*toff	1.16*ton	0	(1.16*ton+1.49*toff)*119,000	0.016
CCM	1.22*ton	8.16*toff	.49*ton	.043*toff	(1.71*ton+8.2*toff)*291,000	0.144
	5.19*ton	12.52*toff	.78*ton	.33*toff	(5.97*ton+12.85*toff)*289,000	0.272

Figure 2-14. Switch, diode, and total transition power loss data.

The figure above presents the theoretical power loss data. It is once again important to note that the data is to provide a first order understanding of the transition loss data since it is very hard to measure it individually. In addition, the final column gives an example for what the transition loss would be for a given transition loss time.

The data shows that the transition loss for the CCM board is worse. The first reason for the increase in transition loss is the higher operating frequency. In addition, the CCM board switches from a non-zero current at switch turn on and the diode still has some DC current in it when it turns off. The BCM board does not incur transition losses at switch turn on and diode turn off because the currents are zero at these transition points. The transition loss is accentuated in the CCM board at high currents because, the operating frequency of the BCM board decreases at higher load currents.

The third switching loss mechanism is a result of primary leakage inductance in the transformer. Leakage inductance is the term given to inductance inherent in the transformer that is not linked between primary and secondary. Leakage inductance exists on both the primary and secondary side. In order to calculate the leakage inductance present on the primary, the secondary of the transformer must be shorted out. The resulting inductance on the primary side is the leakage inductance on the primary. In order to calculate the secondary inductance a similar method is used where the primary is shorted. The primary leakage inductance typically is in the range of 1-5% of the primary inductance. In terms of the transformer used in the comparison, the leakage inductance was 1uH. The loss mechanism related to the leakage inductance is related to the primary current stored in the primary leakage inductance when the switch is on. When the switch turns off, the primary leakage energy must be dissipated. The amount of energy stored in the leakage inductance on the primary can be written as $\frac{1}{2}L_l I_{pk}^2$. The actual energy

spent dissipating the leakage energy is higher and related to the snubbing circuitry used. The actual energy lost is a multiple of the leakage inductance energy stored. Both modes have the same snubbing circuitry, so it is equivalent to just look at the leakage energy for the comparison. In order to make the leakage energy relate to power, the energy formula is multiplied by the frequency of operation to give the following power loss formula $\frac{1}{2} L_l I_{pk}^{2} f$.

Leakage Inductance (H)				1.00E-06
	Current Load	frequency (Hz)	Isw Peak (A)	Switching Loss (W)
BCM	1A	224,000	0.76	0.065
	2A	119,000	1.46	0.127
CCM	1A	291,000	0.644	0.060
	2A	289,000	0.988	0.141

Figure 2-15: Leakage inductance power loss.

Figure 2-15 above shows that the leakage power loss is much higher for CCM at high current load, but lower than BCM at low current load. The distinction makes sense because at light load, the BCM board has a higher switch peak current and an operating frequency close to that of CCM. Interestingly enough, the power loss at 2A is lower for the BCM board despite having the higher peak current because of the advantage gained from a lower operating frequency.

2.2.1.3 Diode Loss

The next area of comparison results from forward diode voltage. The diode loss is the largest loss mechanism in the step down application because of the high secondary peak currents. In addition, since the output voltage is of the same order as the diode forward drop, the result is a large percentage power loss. For example, at 2A out we can estimate the diode loss at 1W if the forward drop is 0.5V. Thus for a 10W output power application, the power loss of the diode is 10% of the total power delivered! The equation for power loss through the diode is: $P_D \approx I_{DAVG} \bullet V_F$ [5].

V_F is the forward voltage of the diode. The forward voltage, however, changes with instantaneous forward diode current. Using available diode data, one can use the

value of V_F at the average forward current level. I_{DAVG} represents the average current flowing through the diode. The figure below presents data on the power loss due to the diode forward voltage. The calculated values are based on measured forward drop voltages on the diode at DC currents. Then the diode forward current was averaged to be whatever the output current was in the setup. Thus both BCM and CCM had the same diode power loss numbers.

	Current Load	Diode Forward Voltage	Power Loss (W)
BCM	1A	0.40	0.40
	2A	0.53	1.06
CCM	1A	0.40	0.40
	2A	0.53	1.06

Figure 2-16: Diode forward power loss.

2.2.1.4 Transformer Losses

Transformer losses make up the final relatively large loss mechanism in the flyback application studied. The loss through the transformer can be separated into two parts: one that is related to the core loss and the second that is through copper loss.

Core loss is a function of the flux swing in the transformer, the frequency of operation, and the volume of the core. Transformer manufacturers provide core loss data for the specific cores used in their transformers. In addition, they provide simple formulas that model their loss data to provide a first order representation of the core loss for the given application. The loss formula, known as the Steinmetz equation, is of the form $= C \times F_{sw}^{d} \times B^{p} \times V$ [6], [8], [14]. C, d, and p are three constants that are given with the core data to allow calculation of core loss. In the core data available, the power of the flux swing is higher than that of the frequency. B is the ac flux change in the transformer, F is the frequency of switching, and V is the volume of the core. The equation models core loss for sinusoidal excitations only. In the following calculations for loss, the fundamental component of the switching frequency is used to approximate the core loss.

The figure 2-17 below presents the core loss data for the transformer used in the comparison of the two operating strategies.

Transformer Parameters

C	1.30E-16					
d	2					
p	2.5					
Volume	.51cm^3					

	Current Load	Frequency (Hz)	B swing (p-p) Gauss	Core Loss (W)
BCM	1A	224,000	1,630	0.063
	2A	119,000	3,070	0.089
CCM	1A	291,000	1,260	0.055
	2A	289,000	1,250	0.056

Figure 2-17: Core loss data calculated.

The core loss data was calculated using the constants provided by the manufacturer and the core loss equation presented above. From the data above it shows that the core loss is higher in the BCM board despite operating at a lower frequency. Thus the relative emphasis is much higher on the flux swing than that of the frequency. BCM requires a much higher flux swing because of the fact that the transformer does not operate at a DC flux level in the transformer. Note, however, that the calculation methods considered are not necessarily very accurate for flux patterns with substantial DC bias and/or non-sinusoidal flux swings. A more accurate method of predicting core loss with non-sinusoidal waveforms is presented in both [13] and [14]. Due to time constraints and for the sake of simplicity, the simple Steinmetz loss equation was used instead.

Copper loss is the second form of loss incurred in the transformer. The transformer is made up a number of turns of copper wire that has a finite parasitic resistance that becomes a loss mechanism. Again the RMS currents must be used along with the winding resistances to calculate the conduction loss in the transformer. The loss data is presented in the figure 2-18 below.

Transformer Parameters

Rprimary   0.231

Rsec   0.015

	Current Load	Irms Sw (A)	Irms Diode (A)	Copper Loss (W)
BCM	1A	0.260	1.648	0.056
	2A	0.499	3.230	0.214
CCM	1A	0.244	1.457	0.046
	2A	0.440	2.851	0.167

Figure 2-18: Copper loss data for the transformer.

The above copper loss data shows that the conduction loss in the transformer is higher for BCM. Overall, both copper loss and core loss are lower in CCM operation.

2.2.1.5 Loss Mechanism Conclusion

Four mechanisms dominate the loss picture for the flyback application studied in this paper. Of the four loss mechanisms, the diode accounts for about half the accountable loss. When comparing CCM and BCM, certain losses are higher for one than the other. For example, in terms of conduction loss, the BCM board shows higher loss because of its higher relative RMS current levels. On the other hand in terms of switching loss, the loss here is higher for CCM since the strategy operates at a higher frequency resulting in a larger loss. The diode accounts for a significant chunk of the power loss for the flyback circuits. It was not clear whether CCM or BCM resulted in higher diode losses. Finally, the transformer has lower copper loss and copper loss in CCM mode because of the smaller flux swing.

In conclusion, despite the comparison between the two operating strategies, it is hard to clearly pick one as more efficient. Each strategy has its advantage in one loss mechanism, but falls behind in another loss mechanism. One good example is the difference between switching loss and conduction loss. Thus it is clearly hard to pick CCM over BCM or vice versa based solely on efficiency.

2.2.2 Operational Comparison

BCM differs from CCM operation due to the fact that switching occurs only after all the energy stored in the primary of the transformer is transferred to the secondary. This difference alone provides considerable insight to the differences in operation and ultimately to the advantages of one topology over the other.

One key advantage gained from switching at a known condition on each cycle is that an oscillator is not required. An onboard oscillator is necessary in the CCM board to tell the switch when to turn on again. The BCM board will only switch when the current in the transformer reaches zero and hence there is no need for a separate oscillator. However, startup circuitry is required to get the converter started.

A second operational difference is how the two topologies deal with current limit or short circuit conditions. The BCM board is inherently better suited for short circuit operation because it only switches once the current reaches zero in the secondary. The problem arises because when the output is shorted, the secondary winding of the transformer has a lower voltage to satisfy volt-second balance. The lower voltage requires more time to reset the inductor. In addition, most controllers also have some minimum on time that is a result of blanking spikes associated with switch turn on. Thus the current in the transformer has the possibility of running away since the current doesn't reset and the minimum on time prevents the switch current monitoring circuitry from turning off the switch immediately. In addition, the CCM board will continue to switch until the high DC currents in the transformer place enough stress on the components in the circuit to cause failure. Therefore the CCM designed board must incorporate careful design in regard to short circuit protection and cannot rely on a maximum switch current limit alone.

Startup operation is another difference that relates to the presence of an oscillator. The CCM board can rely on the oscillator to start the system since it guarantees switch turn on at a set frequency. On the other hand the BCM board must incorporate some sort of kick start circuitry to get the circuit switching or a some sort of long term timer which triggers the system to switch after a prolonged off time. One could argue that this function is very similar to an oscillator, but the requirements for this timer are much more relaxed and simple.

28

The final operation difference relates to the fact that switching occurs at zero current at switch-turn-on and diode-turn-off in BCM. For example, the task of blanking the signal into the current sense amplifier measuring current through the switch is reduced in BCM. Current spikes at switch turn on are larger in CCM then compared to BCM. In CCM the switch current starts from a nonzero level so the current spike also starts from the same level and gets closer to the peak switch level as shown in figure 2-19. Thus, less headroom is available in CCM to sensitivity from the turn on spike. As the figure shows, the spike in CCM is more likely to cause a false turn-off because the DC current at turn-on offsets the spike higher.
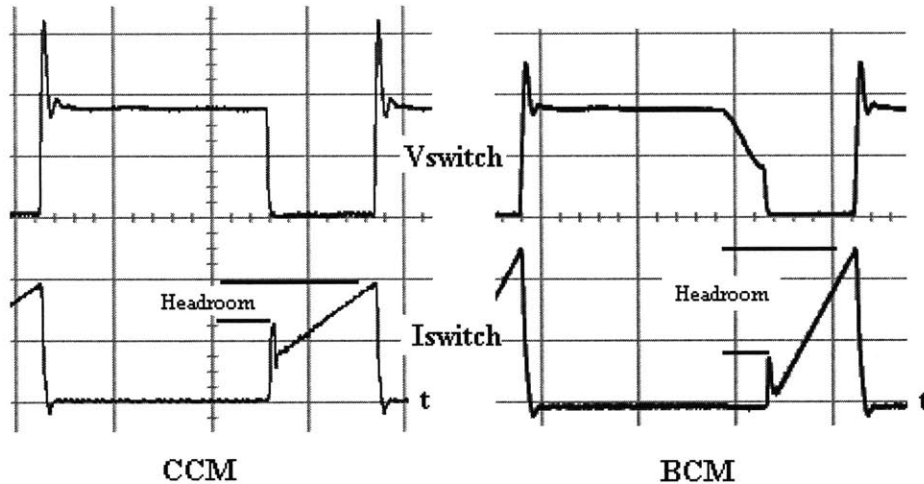
Figure 2-19: Headroom available when blanking current spike at switch turn on.

In addition, a similar advantage relates from the fact that the diode turns off at zero current in BCM. The soft switching of the output diode reduces EMI generated by the turn off of the output diode and requires little or no snubbing on the diode.

For the reasons listed above, BCM provides some advantages over CCM operation in practical circuit applications.

3 Feedback Techniques

3.1 Introduction

Another way in which flyback controllers differ from one another originates from how they gather feedback information. If the flyback is to be isolated and controlled from the primary side, then the output information must be transferred from the secondary side to the primary side of the circuit. The primary side is where the control circuitry is usually located and may or may not be referenced to the same dc level. Creative techniques must be devised to glean information from the secondary side to create the closest representation of the output voltage.

3.2 Direct Feedback

In the simple case where no isolation from input to output exists, feedback information can be obtained directly since the primary and secondary are referenced to the same dc level. Output voltage information can be obtained using a resistive divider connected to the output and then sent to the error amplifier in the controller.

If the flyback converter is isolated, the direct method of obtaining output information is no longer available. Creative techniques must be developed to cross the isolation boundary. One method is using opto-coupled feedback. In this technique, information from the output is converted into an error correction signal that is optically passed across the isolation boundary. A variety of unique feedback techniques are possible using opto-coupling to cross the isolation boundary. Load regulation within ±1% is possible with opto-coupled feedback.

3.3 Isolated Feedback

Another method of gathering output information gathers information on the primary side. The technique is known as magnetic flux sensing and requires an extra winding on the transformer called the bias winding. The bias winding is wound with the same phasing or opposite phasing as the secondary side. The extra winding provides a sample of the voltage across the secondary when energy is transferred to the load. Using this method, crossing the isolation boundary is accomplished using the bias winding of

30

the transformer. This method requires sampling the information and converting it into a voltage that accurately represents the output since it can only be obtained on the flyback pulse. Precision in output regulation will be limited by the accuracy of the sampling method, diode forward voltage drop variation over load and transformer coupling over load. Previous implementations of sampling have achieved $\pm 2\% - \pm 3\%$ regulation in a CCM setup and with error correction have been able to provide $\pm 1\%$ regulation [2].

After comparison of component count, cost, and size, the decision was made to close the feedback loop using isolated magnetic flux sensing. Before providing details of the chosen method of feedback, it is important to present some background in regards to the different types of isolated sensing techniques.

Building an isolated power supply requires that all aspects of the primary circuitry are separate from that of the secondary. In other words, the ground connection must be separate between the two sides so that any dc level on either side is floating with respect to the other. The requirement for isolation affects the feedback connection directly. In developing a method for closing the feedback loop, a method must be devised to cross the isolation boundary between the primary and the secondary.

3.3.1 Opto-coupled Feedback

Historically isolated feedback power supplies mainly used opto-couplers to cross the isolation boundary. The light emitting diode of the opto-coupler resides on the secondary side, while the photo-transistor is on the primary side. The opto-coupler is operated in linear mode using an amplifier with a voltage reference. In figure 3-1 below is a typical circuit implementation of a power supply feedback connection using an opto-coupler.

31
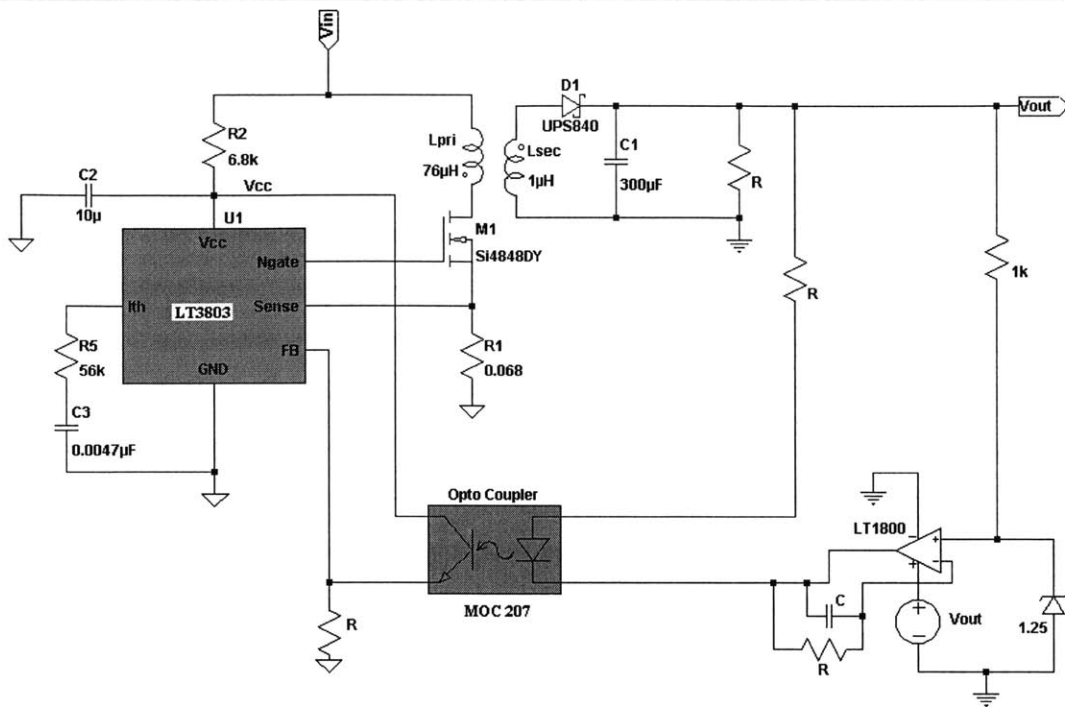
Figure 3-1: Flyback circuit using an opto-coupler as feedback control.

Two typical methods of closing the feedback loop exist when using opto-couplers. Both connections require an error amplifier and a reference on the secondary side of the circuit to generate error signals that ultimately control the turn-off of the switch. The way each method differs depends on whether or not it uses or bypasses the error amplifier inside the controller on the primary side.

For example, in the first method shown in the figure 3-1, the feedback connection makes use of the error amplifier in the power controller. The error signal generated by the error amplifier on the secondary drives a follower configuration on the primary that serves as the feedback signal. The feedback signal then drives the error amplifier inside the controller.

Another method of closing the isolation loop bypasses the error amplifier inside the controller. Figure 3-2 shows the configuration below where the opto-coupler error signal drives the common emitter gain stage controlling the V_C pin directly. The feedback pin is grounded forcing the internal error amplifier in the controller to swing to its maximum output. Then the common emitter stage sinks the output current to right level moving the V_C pin to the right voltage ensuring regulation.

32

Each method has its own advantages and disadvantages in regards to DC gain, ease of compensation, and bandwidth [1].
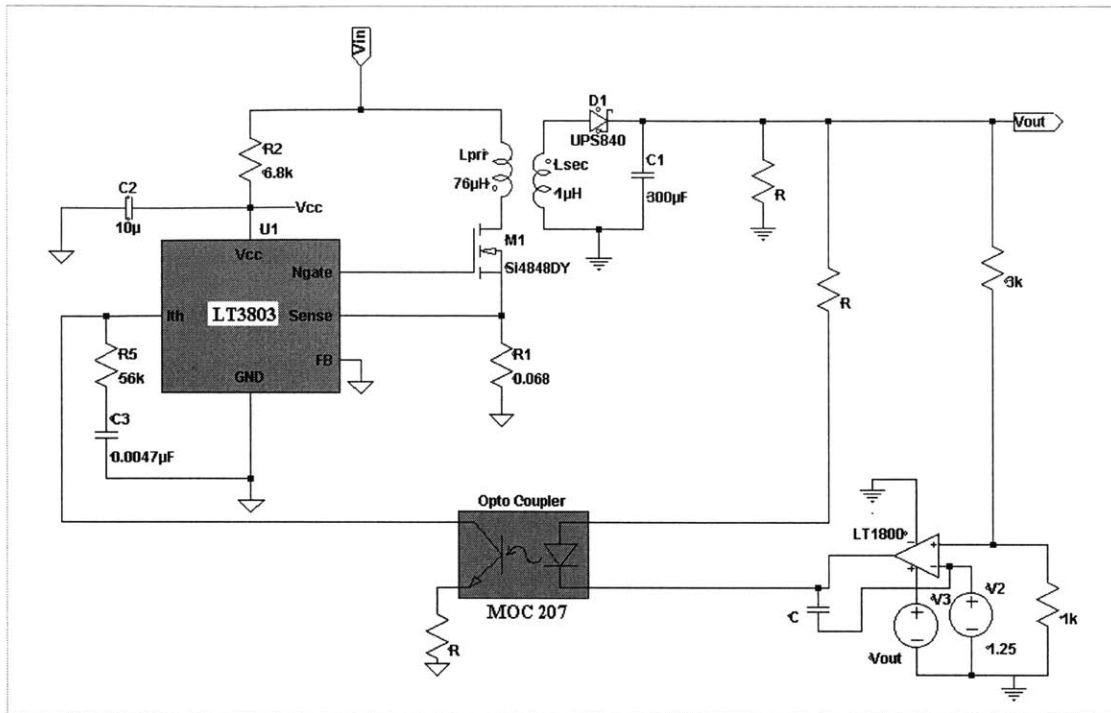
Figure 3-2: Flyback circuit using opto coupler to control the V_c/ Ith pin.

3.3.2 Magnetic Flux Sensing Feedback

A second way of closing feedback in an isolated flyback is using magnetic flux sensing feedback. The first integrated circuits that incorporated the necessary circuitry to tightly regulate ($\pm 1\%$) output voltages in an isolated flyback power supply using magnetic flux-sensing were the Linear Technology 1103/1105 current-mode controllers. The 1103/1105 parts were targeted for offline power regulation. The technique was used in the 1103/1105 for the control of fixed frequency flyback circuits. The method improved on previously available flux sensing performance of $\pm 5\% - \pm 10\%$ regulation. The 1103/1105 corrected for errors inherent in the flyback waveform. Figure 3-3 is the typical flyback pulse seen in a fixed frequency flyback topology.

33
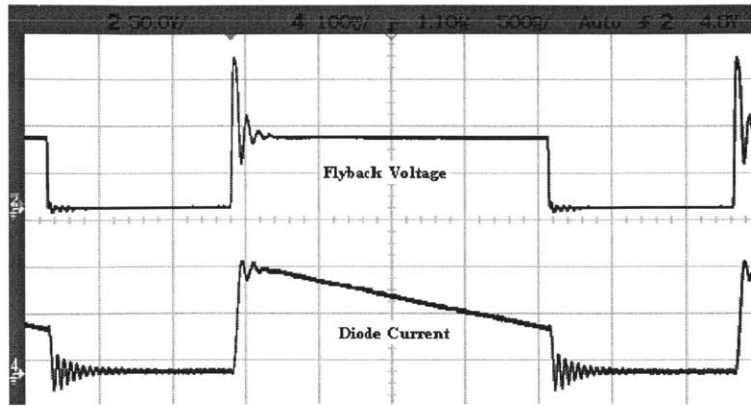
Figure 3-3: Fixed frequency diode current and flyback voltage.

The initial section of the flyback waveform shows the effect of leakage ring at the switch node. The inductance in the primary and parasitic capacitance at the switch node form a resonant L-C tank circuit that rings while the energy stored in the leakage inductance is dissipated after the switch turns off. The voltage level on the flyback pulse after the leakage ring is a combination of the output voltage, the forward drop of the diode, turns ratio of the transformer, and parasitic drop across resistance and leakage inductance on the secondary side of the output. A constant voltage forms across the leakage inductance since the slope of the current in the secondary during this period is constant. Finally, the parasitic resistances associated with the secondary winding, the diode, and the output capacitance can be lumped together as, R_{eqpar}. The voltage on the bias winding can be represented as follows:

$$V_{flyback} = \frac{\left(V_{out} + V_{diode} + V_{secondary,leakage} + I_{sec} * R_{eqpar}\right)}{N_{turns}}$$

Therefore, the linear ramp in the flyback waveform can be explained using the equation above and the waveform for current through the diode. The current in the secondary decreases linearly as the energy stored in the primary is transferred. The linear drop in current multiplied with the equivalent resistance of the parasitics results in a linearly dropping voltage that adds to the output voltage, diode forward drop, and leakage voltage drop. Hence the flyback voltage shows a linearly decreasing slope that corresponds to the diode current. If the error terms related to the diode forward drop, leakage forward drop,

34

and the secondary resistances are taken out of the flyback waveform, then an accurate picture of the output voltage can be formed.

The 1103/1105 sensed the flyback waveform on the bias winding and sampled the point right before the voltage flyback signal collapsed. The point at this corner represents the most accurate representation of the output voltage and the smallest forward voltage drop in the diode. Using this point alone without error correction for load current, the output was regulated down to $\pm 2\% - \pm 3\%$. Both the leakage forward drop and the diode forward drop are DC terms that are simply removed with DC offset in the feedback resistors. Finally after the addition of load correction circuitry, regulation was obtained down to $\pm 1\%$ [2] using the voltage obtained at the corner of the flyback pulse. The load correction corrected for the drop across the R_{eqpar} term that exhibited voltage across it.

Magnetic flux sensing applied in the 1103/1105 dealt with a fixed frequency flyback that operated in CCM or DCM. The proposed variable frequency boundary mode part simplifies the design introduced in the 1103/1105. When the flyback operates in boundary mode, the switch turns on when all the energy stored in the primary is completely transferred to the secondary. The complete transfer of energy also means that the secondary current reaches zero before the switch turns on again. Figure 3-4 shows the flyback waveform and the output diode waveform in boundary operation.
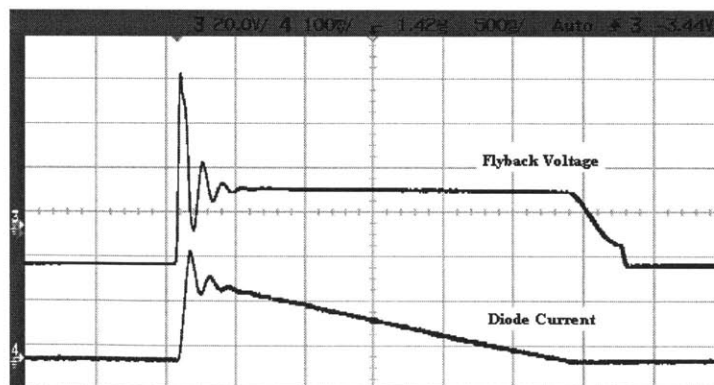

Figure 3-4: Flyback voltage & diode current in boundary mode.

The waveform still exhibits the leakage spike along with the linear ramp down in voltage. Importantly since the current in the secondary is zero at the point right before the flyback collapses, then the voltage at the corner is just the output voltage plus the forward drop of

the diode and the forward drop across the leakage inductance. Ideally, then no error correction is required to deal with the effect of changing load, just an offset is needed! Boundary mode operation helps improve upon the method introduced in the 1103/1105 parts.

The proposed isolated boundary mode flyback converter plans on using magnetic flux sensing feedback to both simplify the design and provide tight regulation of the output voltage. Before explaining the implementation of magnetic flux sensing in boundary mode, it is important to compare magnetic flux sensing to opto-coupling to fully understand the benefits and disadvantages of choosing one over the other.

3.3.3 Opto-coupled Feedback versus Magnetic Flux Sensing Feedback

The following chart presents a comparison of opto-coupling with magnetic flux sensing feedback.

Feature	Opto-Coupling	Magnetic-Flux Sensing
Size	More	Less
Average Cost	More	Less
Accuracy	More	Less
Bandwidth	Similar	Similar
External Components	More	Less

Figure 3-5 Opto-Coupling and Magnetic-Flux Sensing Comparison Chart.

For the reasons highlighted in the chart above and in the preceding analysis, magnetic flux sensing was chosen as the design approach for the proposed boundary conduction mode board.

3.4 Implementation of Magnetic Flux Sensing Feedback

3.4.1 Theory

The method chosen for closing the feedback loop was using magnetic flux sensing feedback. Initially, it was important to prove the ability to get rough regulation using the technique on a boundary board built using an off-the-shelf IC. It was hoped that using

36

this simple boundary mode part, insight would be gained in peculiarities in using the technique in a boundary mode application. Also it was important to see how the part would operate if the feedback was closed roughly using a first order flux-sensing technique.

The design problem faced initially was choosing the best method to accurately catch the voltage level at the corner of the flyback pulse. The voltage at the corner would be the most accurate representation of the output and would have a slight offset resulting from the forward voltage drop of the diode.

Two methods of capturing the voltage at this corner point were compared. The first uses a simple level detector that would trip when the flyback voltage waveform dropped below a certain point. It was proposed that this point could be V_{in} or some ratio of the flyback voltage. The method would require having two circuits tracking the flyback waveform. One circuit would have a slower bandwidth and the other would have the trip level detection. The trip level detector circuit would be used to trigger the first circuit to hold the value when it tripped. Timing would have to be set just right to ensure that the tracking circuit captured the voltage at the corner of the flyback waveform. In addition, the trip level would have to be set optimally across all load and line conditions. This methodology was studied but was not built or evaluated in the lab.

The next method takes advantage of the fast change in the flyback waveform that occurs when the flyback waveform collapses. This technique employs a dV/dt detector that tracks the flyback waveform, but holds the value when a large dV/dt change occurs. Using a dV/dt detector does not require accurate timing and trips consistently on fast changes in voltage. In addition, trip levels do not have to be set, and the detector operates the same across both line and load since it trips on voltage changes not absolute levels. Due to its simplicity and ease of implementation, the dV/dt detector was used to capture the voltage at the corner of the flyback waveform [1].

Once a method for holding the voltage at the corner of the flyback waveform was devised, another method was needed to transfer this held voltage to the error amplifier to serve as the feedback signal. In the implementation outlined here, a track and hold

amplifier would allow the ability to hold the output voltage signal when the flyback waveform collapsed. Another piece of circuitry would be required to grab the held voltage from the track and hold waveform. A sample and hold circuit would be used to get this piece of information. In the following discussion, relatively good results were obtained using just the track and hold waveform to close the feedback loop. An additional sample and hold was not implemented here, but left for another stage of the design.

3.4.2 Circuit Implementation:

The circuit implementation for magnetic flux sensing feedback requires a couple of functional pieces including leakage blanking, a track and hold amplifier, and a sample and hold circuit. In order to test the idea of magnetic flux sensing, an operational boundary flyback board was needed. The Siemens TDA4862 power factor controller was used to create a functional, regulating boundary mode flyback [11]. The controller included functionality to operate in discontinuous mode operation and switch on a zero current in the inductor. The siemens part was used in the following circuit in figure 3-6 to operate as a BCM flyback controller. The part worked in the application and regulated within 1% across line and load. The following circuit was then used to test the idea of magnetic flux sensing feedback and gather the data shown in the following sections.
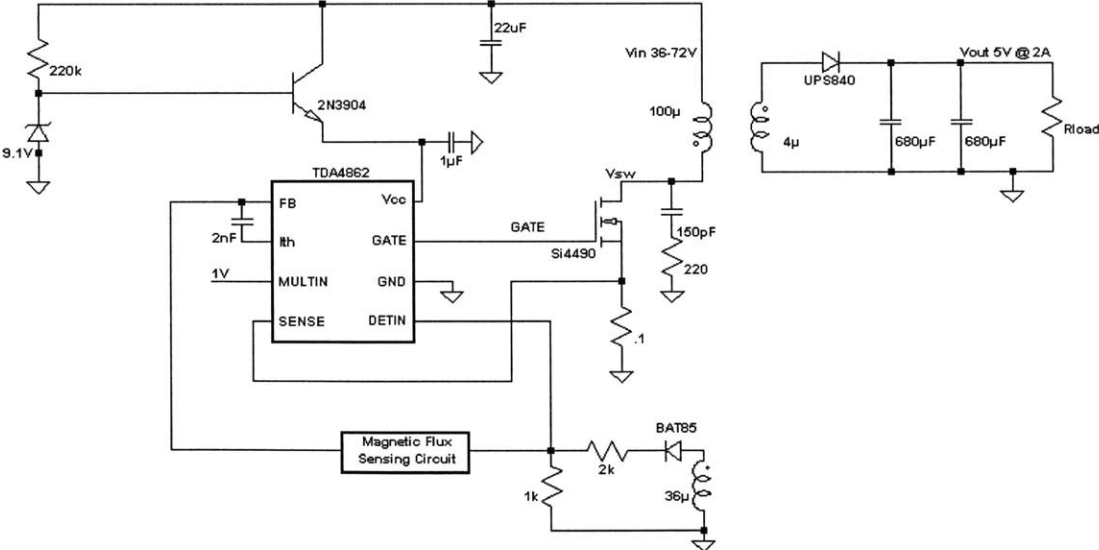

Figure 3-6: Siemens part used to create BCM flyback testing circuit.

The leakage blanking circuitry is important in removing the initial ring present on the flyback waveform. The initial blanking is important because the dV/dt, that triggers the hold circuitry, would trip on the leakage ring if it were not removed. In addition the leakage ring adds a non-linear error to the tracking portion of the amplifier. Blanking is accomplished using a shunt transistor connected to ground that is controlled by a one shot circuit triggered off the falling edge of the gate drive signal. Then the processed waveform is sent to the track and hold amplifier. The schematic of the track and hold amplifier is shown below. It consists of two op-amps, a current buffer transistor, dV/dt detector schottky, mirrored current load, and a hold capacitor. Figure 3-7 shows the initial design of the track and hold dV/dt detector circuit.
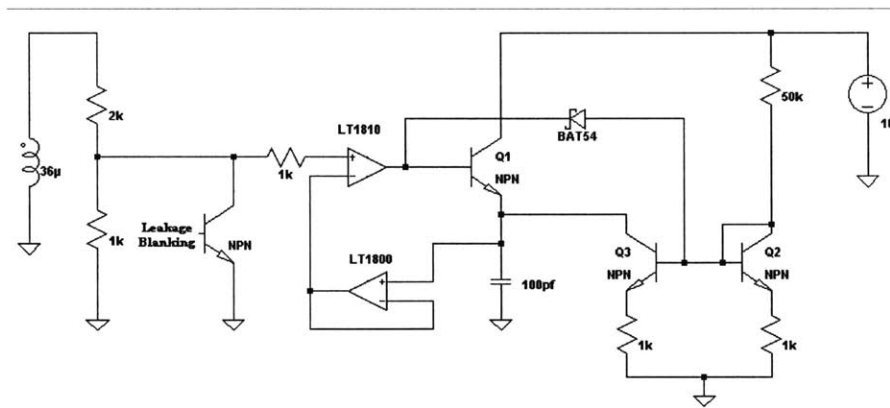

Figure 3-7: Track and hold circuit with leakage blanking.

A good track and hold circuit typically has a high slew rate to track the flyback waveform when it goes high and suddenly falls, and a large bandwidth to quickly respond to the flyback waveform edges that are made up of higher order harmonics. Finally, since the track and hold uses a feedback connection large gain from input to output is necessary to ensure precise tracking with very little offset.

Looking at the schematic, the first transistor before the LT1810 op-amp provides the leakage blanking function needed to prevent false trip of the dV/dt detector. Next, the LT1810 op-amp drives the npn-transistor buffer to provide the current drive necessary to charge up the hold capacitor. Then the voltage on the capacitor is sent back to the

negative input of the LT1810 op-amp through a buffered LT1800 op-amp. A buffered op-amp reduces the loss on the hold cap associated with input bias current into the LT1810 and that due to the diode clamps that exist across the inputs of the LT1810. If the buffered op-amp were not used, then the diode clamps on the LT1810 would pull current from the hold capacitor to within two diode clamps of the input voltage. Also connected at the hold capacitor is a current load. The current load allows the capacitor to slew its voltage down to follow the slope of the flyback waveform since LT1810 can not slew current from the hold cap through the npn current buffer. Finally, a schottky diode is connected between the output of the LT1810 and the base of the current mirror load. The schottky plays the role of the $\frac{dV}{dt}$ detector. When the op-amp tracks the flyback waveform, the collapse of the flyback waveform forces the op-amp to rail negative to pull current from the hold capacitor. When the op-amp goes low, the schottky turns on and becomes forward biased. The schottky steers current through the 50K Ohm resistor to the output of the op-amp away from the current mirror effectively turning the mirror off. This in turn allows the hold capacitor to hold its voltage as nothing remains to pull charge from its plates. Since the trigger occurs at the sudden change in voltage, the voltage on the capacitor represents the voltage at corner of the flyback waveform.

Waveforms of the track and hold circuitry provide a better idea of how the circuit works. The waveform in figure 3-8 shows the input to the track and hold with the leakage ring blanking.
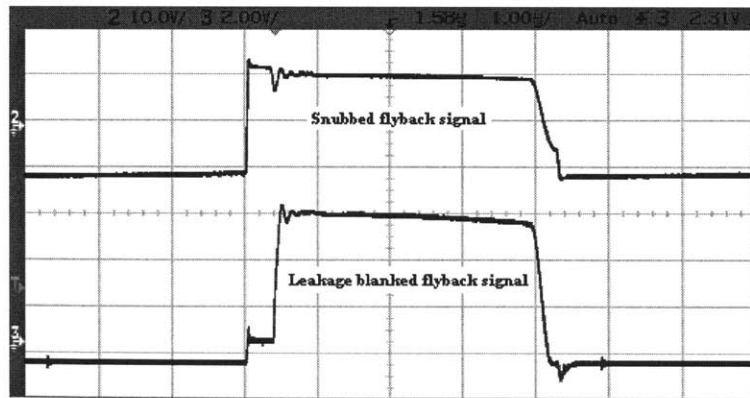

Figure 3-8: Input to track and hold with leakage ring blanking.

The next waveform, figure 3-9 shows the output of the op-amp driving the current buffer transistor during the tracking part of the flyback cycle. The fall of the op amp output voltage coincides with the fall in the flyback pulse and triggers the hold function of the circuit.
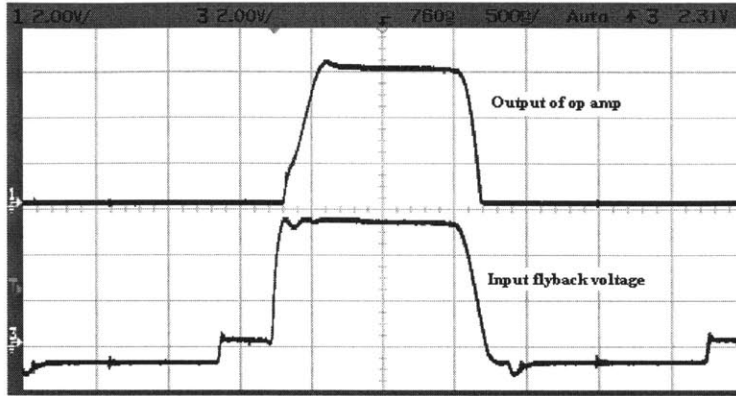
Figure 3-9: Output of op amp.

Then the final waveform, figure 3-10, shows the voltage on the hold capacitor. It shows the tracking portion of the flyback pulse along with the held voltage that represents the output voltage.

Figure 3-10: Voltage on the hold cap.

A complete schematic with components used can be found in the appendix. Also, the LT1810 was chosen for its fast slew rate capability and large bandwidth both of which are required in building a good track and hold circuit.

3.4.3 Debugging Issues / Modifications

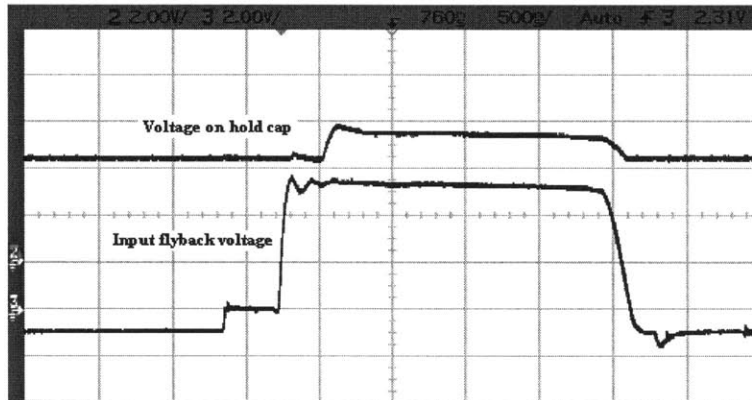During the process of building the track and hold amplifier a number of issues were encountered that required modifications to the circuitry initially presented. The first issue involved oscillations on the output of the LT1810 op-amp driving the current buffer transistor. Figure 3-11 shows the oscillations as a sine wave superimposed on the output of the op-amp. The oscillations occurred in the 4-8 MHz range.
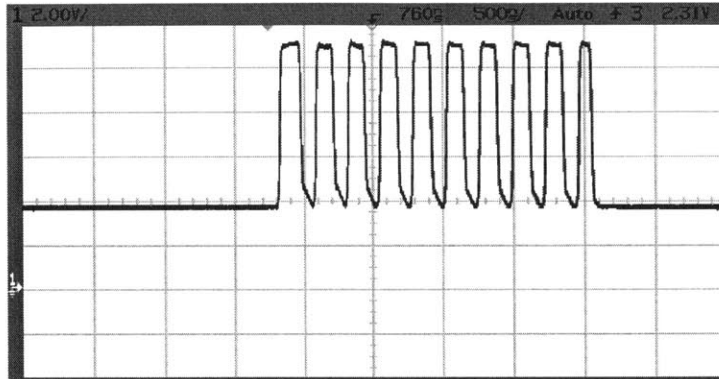
Figure 3-11: Oscillations on the output of driving op-amp.

The oscillations showed the need for compensation since the track and hold used two op-amps with considerable gain and bandwidths connected in feedback. The solution involved a simple dominant pole compensation strategy using a capacitor and resistor from the output of the first op-amp and its negative terminal. The compensation network is shown below in figure 3-12. The oscillations were removed and the output of the first op-amp leaving only slight peaking at initial turn on.

Figure 3-12: Track & hold circuit with compensation added.

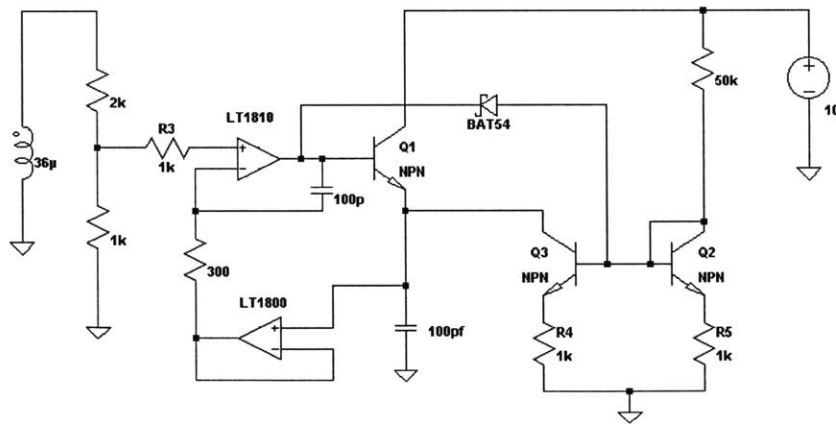The next fix dealt with sizing the current load. Initially the current load was very light and did not allow the hold capacitor to fall quickly. This resulted in the driving op-amp to trip and turn off before the flyback waveform collapsed. The hold capacitor waveform was moving so slow that that it would trip the driving op-amp low because its negative input would have a slope much higher than that of the positive input flyback pulse. The fix for this was simple and required the current load to be large enough to track the downward slope of the flyback waveform. Also, the current load must be large enough otherwise the track and hold does not truly track the flyback pulse. Incorrect tracking would then introduce error in the held value on the hold capacitor.

3.4.4 Adjustments

Two key adjustment levers are available on the implementation of the track and hold amplifier. The first is the size of the current load. The current load must be large enough for a given hold capacitor to ensure the tracking of the flyback waveform during current conduction in the secondary. In other words, the current load must be large enough to track the downward slope resulting from the current falling in the secondary, but does not have to be large enough to track the collapse of the flyback waveform.

Another adjustment point is the size of the hold capacitor. The sizing of the hold capacitor determines the level of voltage change during the hold portion of the cycle when the cap loses charge to leakage and to small bias currents of the buffering op-amp. In addition, the size of the capacitor determines the relative sizing of the current load as previously discussed. Another force determining capacitance size is the fact that the solution must be implemented in an IC. An IC cannot support large capacitors and tends to require even smaller capacitance values for a sot-23 application. It is also important to note that since the thesis chooses to build a board level solution, a smaller capacitor would make the hold capacitor much more sensitive to noise. Thus it was chosen to use a capacitor in the range of 100pf-500pf for the board level solution.

43

3.4.5 Open Loop Tracking Data

The next step in building the circuitry required taking measurements of the precision of the held voltage on the capacitor across both line and load along with the output voltage of the Siemens part. Figure 3-13 below shows the connection.
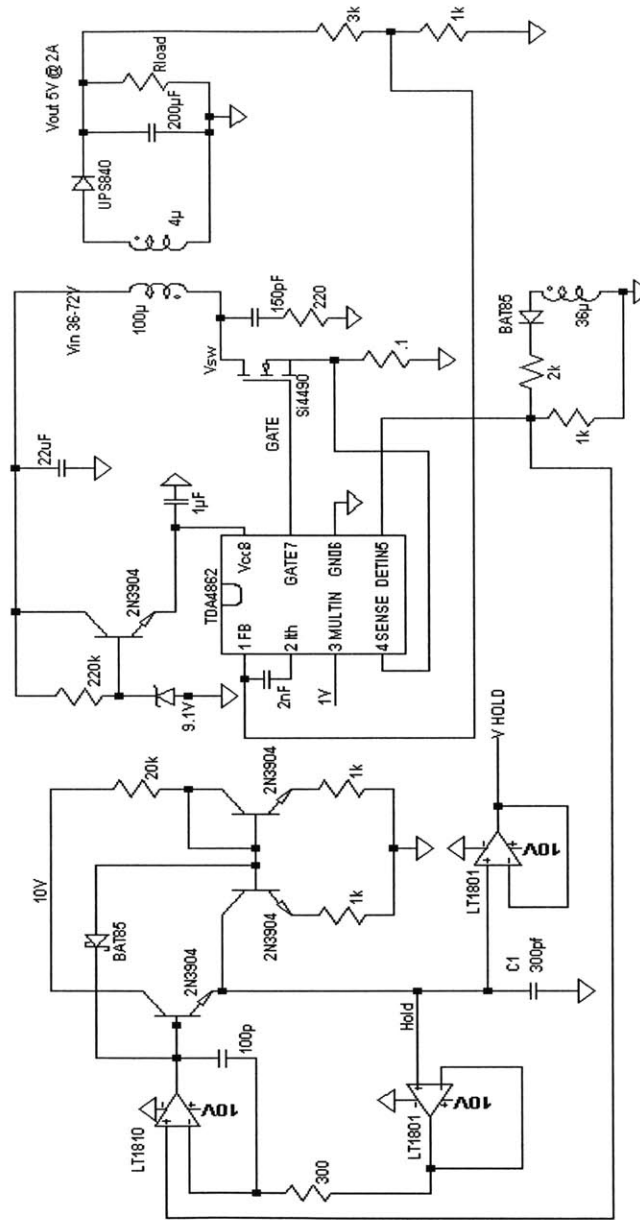
Figure 3-13: Track and hold connection to Siemens part

Output voltage load regulation of the Siemens part alone was within ±1.3% at both 36 and 75V at the input, while the hold cap load regulation was ±2.3% at 36Vin and ±1.7% at 75V! Figures 3-14 and 3-15 show load regulation at these two input levels.
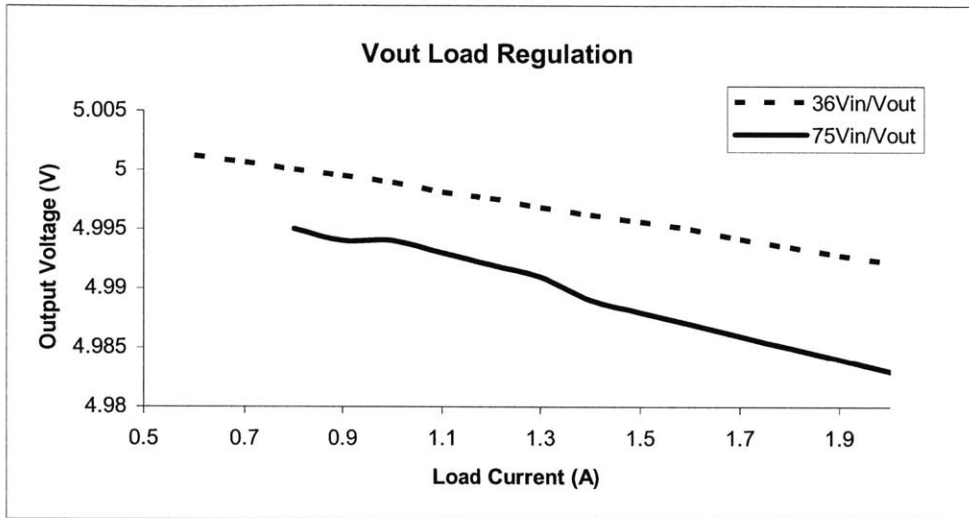
Figure 3-14: Siemens output load regulation.
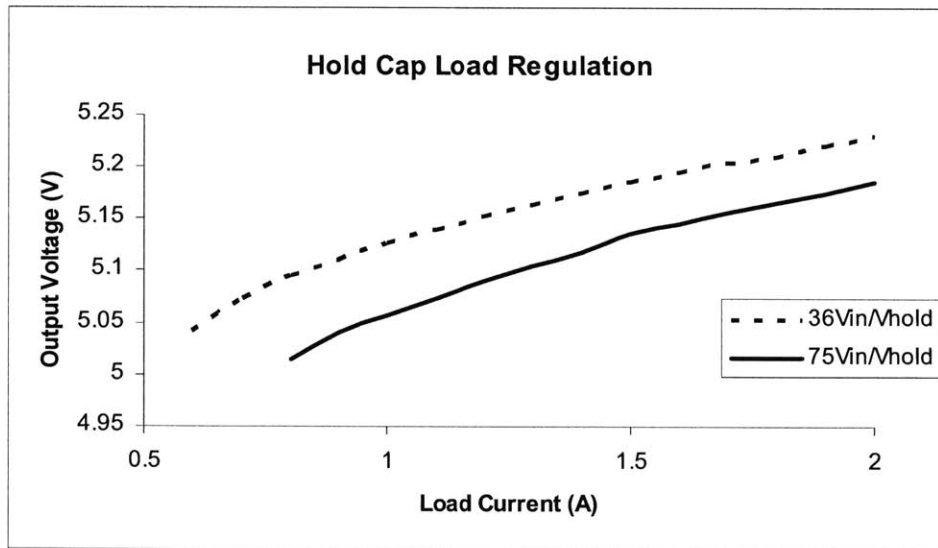
Figure 3-15: Hold cap load regulation on Siemens board.

Line and load regulation for both the output and the hold cap was less than ±1%! Figure 3-16 below presents the data below.
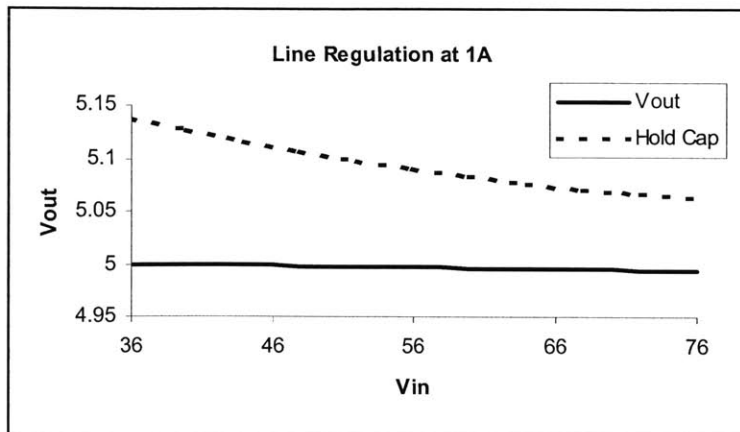
Figure 3-16 Line regulation of both the output and hold cap.

3.4.6 Closed Loop Regulation with Track and Hold Circuit

The data above showed considerable promise since the voltage levels regulated over both line and load. The next step involved connecting the track and hold amplifier output as feedback on Siemens boundary board. Figure 3-17 show the connection of feedback using the track and hold amplifier to close the loop.
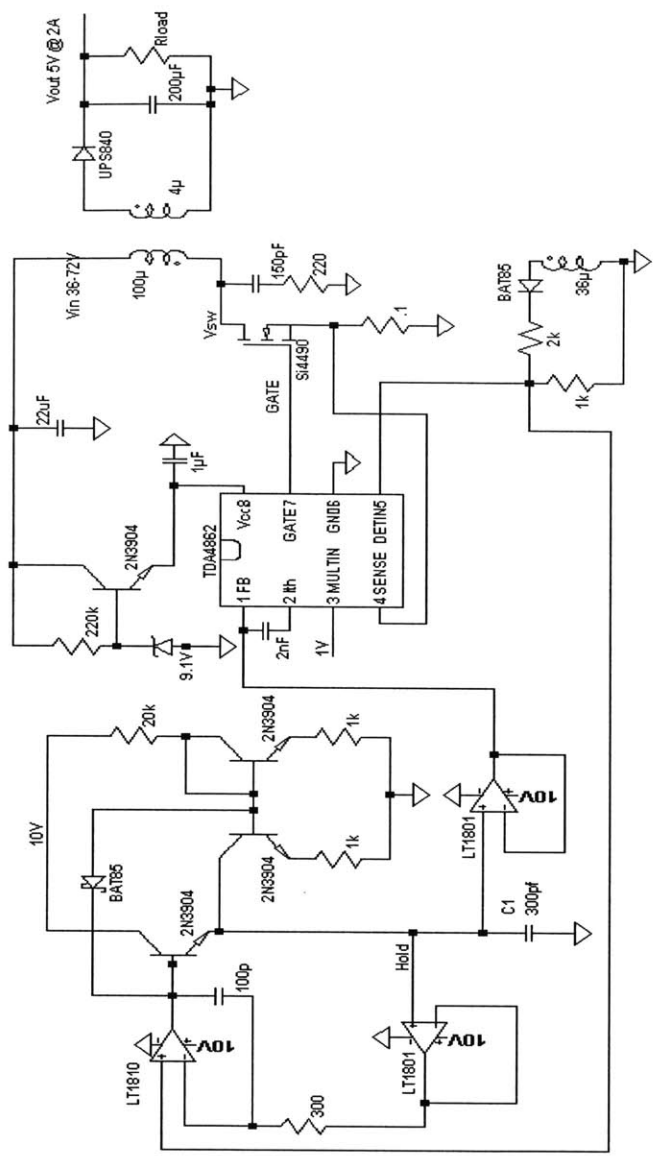
Figure 3-17: Feedback connection with the track & hold amplifier.

The goal was to observe whether the output would regulate from the hold capacitor voltage and how accurately the output voltage would regulate over line and load compared to the open loop measurements. After making the connection, the loop was able to regulate using the output voltage from the hold capacitor. Load regulation was measured at both 36 and 75 volts in and the output showed regulation of $\pm 2.3\%$ and line regulation less than $\pm 1\%$! Figures 3-18 and 3-19 present the data for both load and line regulation. Line regulation was checked with one amp of load current.
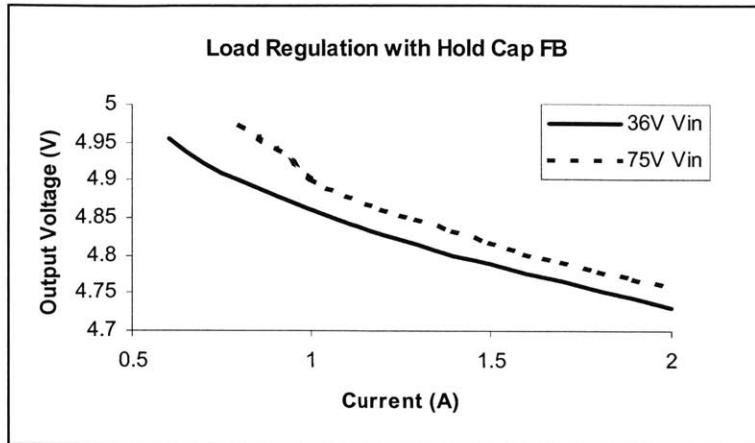
Figure 3-18: Load regulation using the hold cap as feedback.
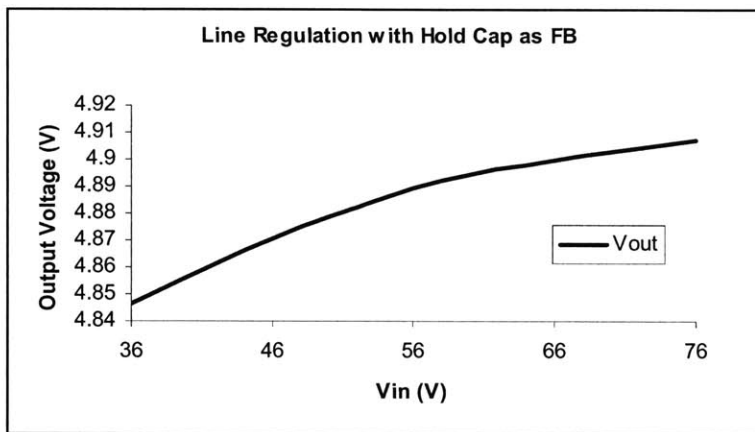
Figure 3-19: Line regulation using the hold cap as feedback at one amp.

3.4.7 Track and Hold Error Discussion

It is important to clarify that the voltage signal used in the previous section to close the feedback loop was the track and hold waveform. The waveform included both the held voltage on the capacitor along with the tracked part of the flyback pulse. Figure 3.8 shows the waveform on the hold capacitor. The tracked portion was an error term since the flyback pulse gets larger at higher output current levels and it includes all the error terms discussed earlier. In addition, the voltage level measured in all the data above was using a voltmeter that averages the input signal to give an output voltage level. The remarkably good regulation over line and load was a little too precise given this error term.

Upon further inspection of the flyback waveform with direct feedback connection to the output, it was observed that the flyback waveform corner moved with load. The corner moved about 230mV over load from 400mA to 2A at 36Vin. The next step was determining what was causing this movement across load conditions. The output flyback voltage at the point when it is held is simply:

$$V_{flyback} = \frac{\left(V_{out} + V_{diode} + V_{secondary,leakage} \right)}{N_{turns}}$$

The drop across the parasitic resistance decreases to zero since the current goes to zero at this point. The output voltage could not be the source, because the data taken before showed that the output regulated within $\pm 1.3\%$. The next point of error tested was the diode. If the diode forward drop was changing over load then it could have become a source of error. If the diode voltage drop was constant across load then it could be adjusted out using the feedback resistors treating it as an offset.

A heat gun was used to test the theory that the movement in the flyback was caused by the diode. According to the hypothesis, as load increased the diode was heating up and leading to a lower average forward drop and thus a flyback waveform that moved down over load. On a cycle by cycle basis the current in the diode would be at the same level across load since the hold point occurred at close to zero current. The difference was that at higher loads the diode was heating up because it was carrying a higher average forward current. A heat gun was used to artificially increase the diode temperature to see if it would modulate the point where the flux in the flyback waveform collapsed. The flyback waveform drifted down as the diode was heated at an output current of 700mA. It was hard to get accurate data of how hot the diode had become as a function of load current, but it was clear that the diode was the source of error.

The reason for relatively good regulation characteristics with a track and hold waveform with two error terms was that they worked to cancel one another. During the tracking portion of the flyback, a positive error was added as load current increased and the track and hold pulse became larger, and the diode forward drop movement introduced a negative error as load current increased. The diode movement provided compensation for the tracking error that increased with load!

3.4.8 Conclusion

The results from the rough connection of magnetic flux sensing feedback in the Siemens boundary board provided proof that the feedback method could produce tight regulation. Without any real load correction for the diode or circuitry to sample and hold the held voltage on the capacitor, regulation was reached within $\pm 2.3\%$. Also it was decided to work on building a controller for the complete solution before adding extra circuitry like a sample and hold.

4 Control Theory & Controller

After understanding the challenges and requirements of magnetic flux sensing feedback, the next step was to begin building a BCM flyback converter from discrete building blocks. The goal of the thesis was to prove that an isolated boundary mode controller with magnetic flux sensing feedback could be built, and to understand the challenges and dynamics associated with designing one. Before bread boarding any solution, further thought and design of a high level block diagram was necessary. In addition, a method of dealing with light load operation needed to be developed. Then dynamic operation of the converter over load could be examined and modeled.

4.1 Characterization of Boundary Board

4.1.1 High-level Overview

In section 2, the different operational strategies were examined. In the case of BCM, switch control was not dependent on an oscillator, but on energy transfer. The switch turns on when the current in the secondary reaches zero. Therefore, a method needed to be devised to signal when energy transfer was complete.

A zero current detector was used to determine the transition point. A zero current detector indirectly monitors the secondary current and signals when it reaches zero. The detector detects zero secondary current by monitoring the flyback voltage. The flyback voltage collapses exactly when the secondary current reaches zero. The detector can use the bias winding to monitor the flyback voltage on the primary side.

With a zero current detector, much of the controller and block diagram is very similar to CCM or DCM solutions. A high-level block diagram of a BCM flyback is presented below in figure 4-1.
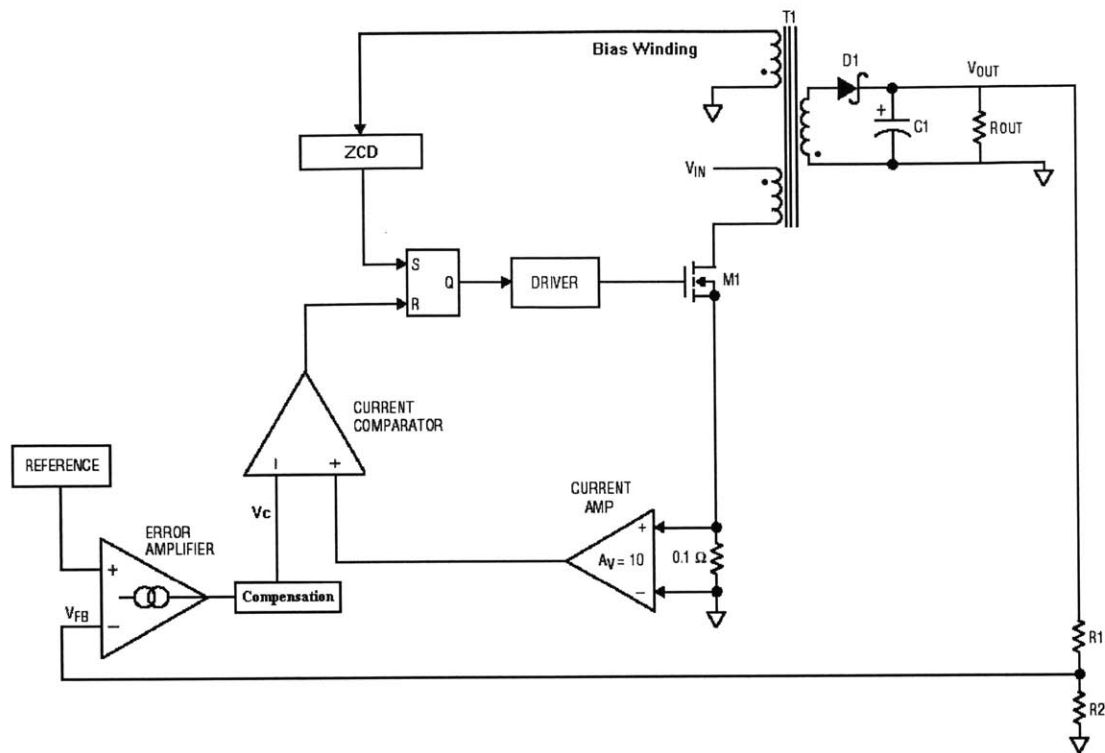
51

Figure 4-1: High-level block diagram of BCM flyback circuit.

The block diagram is shown with the basic flyback circuit. The one thing to note is that the transformer is shown with three windings; primary, secondary, and bias winding. The bias winding is a third winding with similar phasing to the output winding that allows isolated sensing of the secondary winding. The bias winding provides information, during the flyback pulse, to the zero current detector that controls when the switch turns on again.

The other pieces of the solution include the major feedback loop, the logic, current sense amplifier, switch current comparator, and the gate drive to turn on the switch. The feedback network monitors the output voltage and compares it to some reference voltage at the error amplifier to generate an error signal. The error amplifier is created using a gm-amplifier that generates a current proportional to the difference in voltages at its input. The current from the error amplifier is then converted to a voltage (V_c) through the compensation network. The V_c voltage sets one input to the current comparator, and the other is set by the switch current amplifier. The V_c voltage sets the trip level for the current comparator that controls switch turn off. Through the control

path, the V_c voltage commands a specific peak switch current. Then the zero current detector (ZCD) then sends the signal to turn on the switch again.

As presented above, BCM control is simplified without the requirement of an oscillator to set switch turn on. However, a startup circuit is required in BCM to initialize the states in the logic to get the converter switching.

4.1.2 Implementing Isolation

The next level of the block diagram involves implementing isolation. The isolation requires that all the primary circuitry be electrically isolated from the secondary. This means that the output voltage cannot be directly monitored and the grounds of the two sides must be separated. In section 3, the method of isolation was introduced using the bias winding. In the figure 4-2, a block diagram implementing isolation is presented.

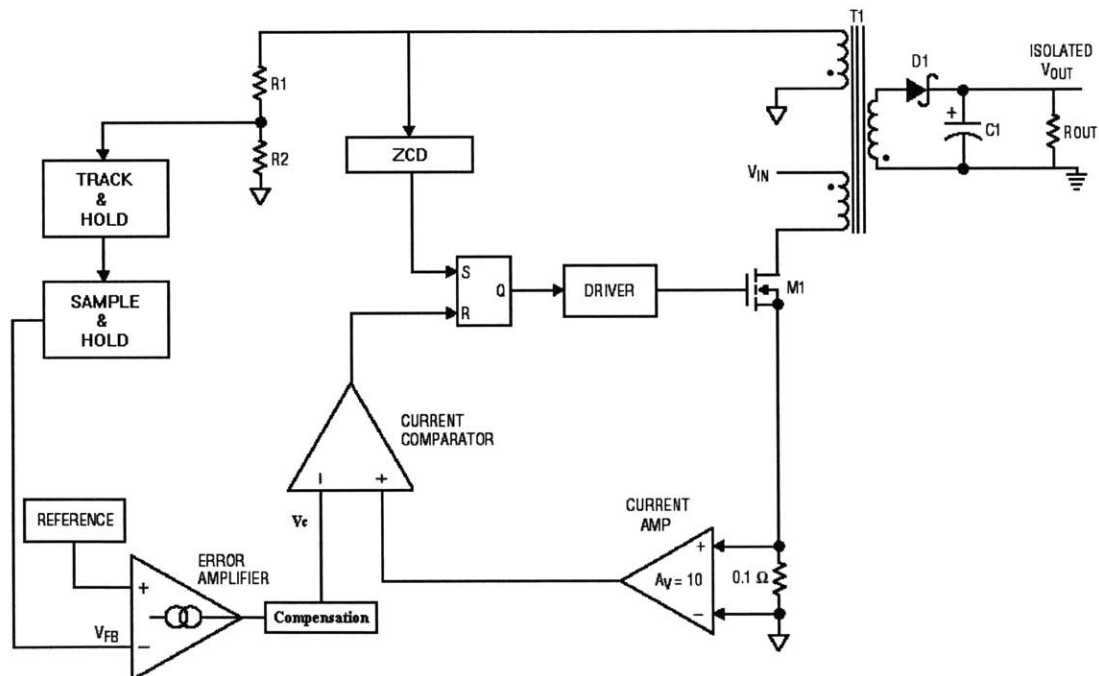Figure 4-2: High-level block diagram with isolation of output from input.

The first piece of the isolation requires using the bias winding for output voltage sensing and zero current detection. The flyback pulse generated on the winding is sent through a track and hold circuit to capture the flyback pulse voltage at the point right before it collapses. The method of sensing was introduced in section 3.4. A sample and

53

hold circuit samples the held voltage and transfers it to the gm-amp. Once the voltage signal is transferred, the control sequence is similar to the non-isolated case. Thus other than changing dynamics, DC operation of the circuit remains the same using the isolated sensing scheme.

4.2 Light Load Implementation: DCM

The next operational piece of the controller must deal with light load operation. In BCM, the operating frequency changes as a function of the output load. For example at light loads, the operating frequency in theory can reach infinity. In a practical system allowing the operating frequency to fluctuate too much is unfavorable. Therefore at light loads, the flyback enters DCM to limit the operating frequency range. There are many additional reasons for limiting the operating frequency, but due to the scope of the paper they will not be addressed here [12].

Light load operation is necessary to keep the operating frequency below a certain level. In the flyback converter, DCM is entered by adding varying amounts of delay between when zero current is detected and when the switch turns on again. The delay can be added in many ways. For example, delay can be added in a quadratic manner with movement in V_c or can be added linearly with V_c. In addition, switch current levels can be manipulated along with the delay.

The two handles available in DCM are switch peak current and delay [12]. One constraint on switch peak current is that it has a minimum clamp level. The switch current level relates to the width of the flyback pulse. The flyback pulse width is important because information about the output is sampled from it, and the sampling circuitry has a maximum bandwidth. Therefore, the switch current has a minimum switch current level below which it cannot go. In the case where switch current reaches its minimum, the only other handle available is delay.

It is important to note that delay and switch current change directly as a function of V_c. Therefore different values of V_c command different levels of delay and switch current. Feedback ensures that the output remains regulated, thus V_c moves to the right point where the switch current and delay commanded regulate the output voltage at that specific output current level.

54

The way in which switch peak current and delay are manipulated with V_c affects operational aspects of the converter. For example, the two affect how flat or steep the frequency versus load curve is. The frequency versus load curve is an important characteristic of the converter. The challenge then is to determine how different ways of combining delay and switch current affect frequency of operation.

When manipulating switch current and delay with V_c, it is also important to monitor the V_c versus I_{OUT} curve. The curve can be generated using the delay and switch current information over V_c. This curve is the transfer function between V_c and the commanded output current. The slope of this curve will determine the DC gain of the modulator. It is important to keep the V_c versus I_{OUT} curve across the entire load range smooth without any discontinuities. Discontinuities here affect the loop dynamics and the overall stability of the system. The slope of the V_c versus I_{OUT} curve is directly related to the DC gain of the modulator from control to output. Further discussion of this role will continue in the next section.

Three methods of adding delay and manipulating switch current were investigated while conducting measurements. Data models and characteristics for switch current (I_{swPk}) and delay are presented below for each of the three options. The three methods were modeled in excel.

4.2.1 Linear Delay after I_{swPk} Clamped

The first method linearly added delay once the switch current reached its clamped level. The method is described visually in the graph presented below in figure 4-3.
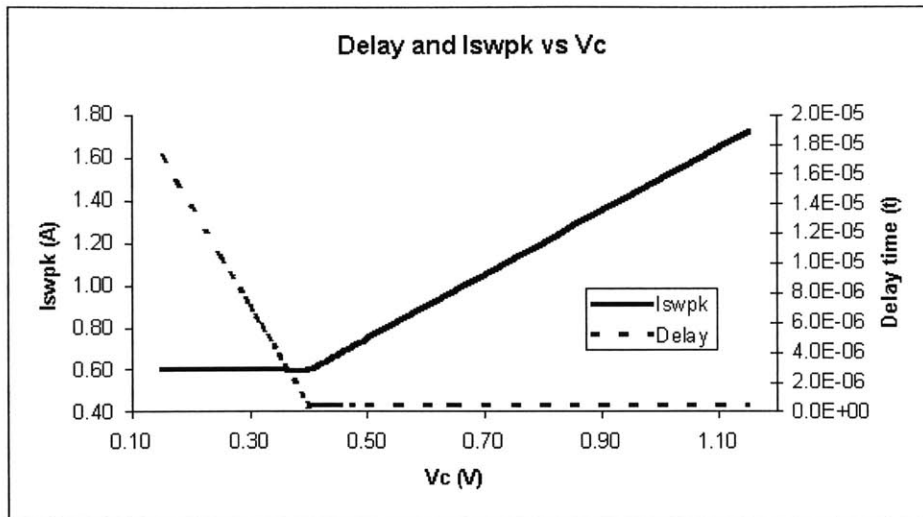
Figure 4-3: Delay & I_{swPk} vs. V_c for linear delay once I_{swPk} clamped.

Figure 4-3 shows how the switch current and the amount of delay added changes with the given value of V_c. Switch current and delay versus V_c can be used to determine how I_{OUT} changes with V_c. In addition, the combinations of switch current and delay for each value of V_c can then be related to frequency for a given transformer and input and output voltage combination. Figure 4-4 shows the frequency versus output current data for a transformer with a 5:1 turns ratio and a primary inductance of 100uH. The input voltage is 48V, while the output voltage is 5V.
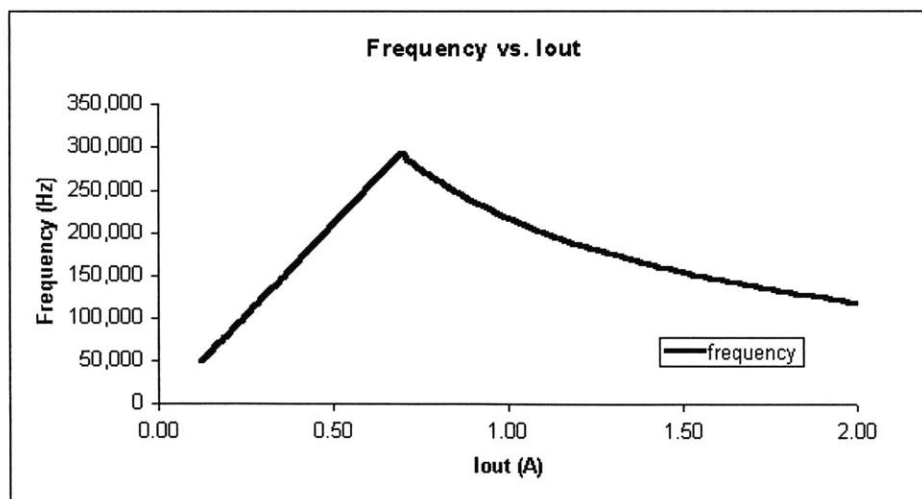

Figure 4-4: Frequency vs. I_{OUT} for linear delay once I_{swPk} clamped.

56

The frequency versus output current shows a sudden change when the converter enters DCM. Figure 4-5 below shows the resulting data another way with V_c versus output current. The I_{OUT} versus V_c curve relates directly to the effective DC gain of the system since the slope of the curve multiplied by the output impedance of the converter gives one the DC gain from control to output. The curve below shows a sudden change in slope at around the point where it enters DCM. The sudden change in slope will result in a sudden change in the DC gain curve.
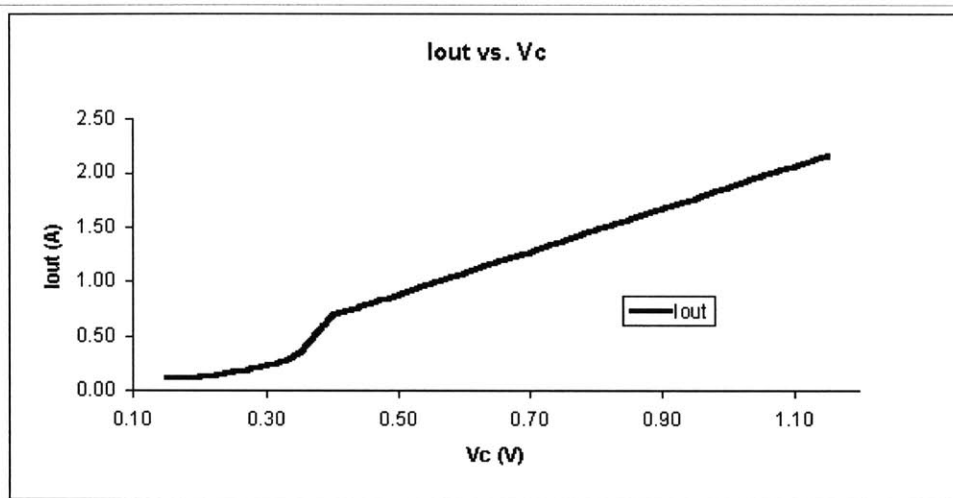

Figure 4-5: I_{OUT} vs. V_c for linear delay once I_{swPk} clamped.

4.2.2 Linear Delay before I_{swPk} Clamped

The next method linearly added delay before the switch current reached its clamp. Delay was added before the switch becomes clamped to smooth out the transition between BCM and DCM. Figure 4-6 graphically shows how delay is added with V_c.
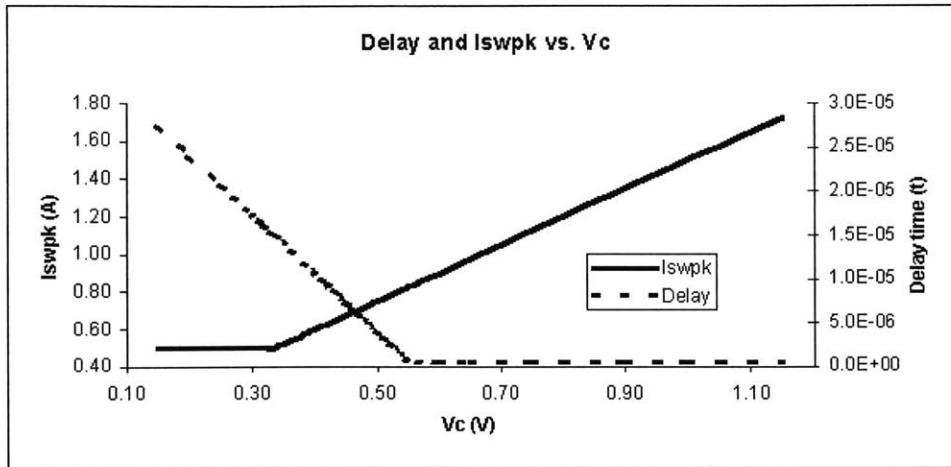
Figure 4-6: Delay & I_{swPk} vs. V_c for linear delay before I_{swPk} clamped.

Once again, the information presented in figure 4-6 was used to create a curve comparing frequency versus output current. The frequency curve helped to understand the impact of adding delay in this method. The transformer model used and the input to output voltage levels were the same as those explained in the previous example.
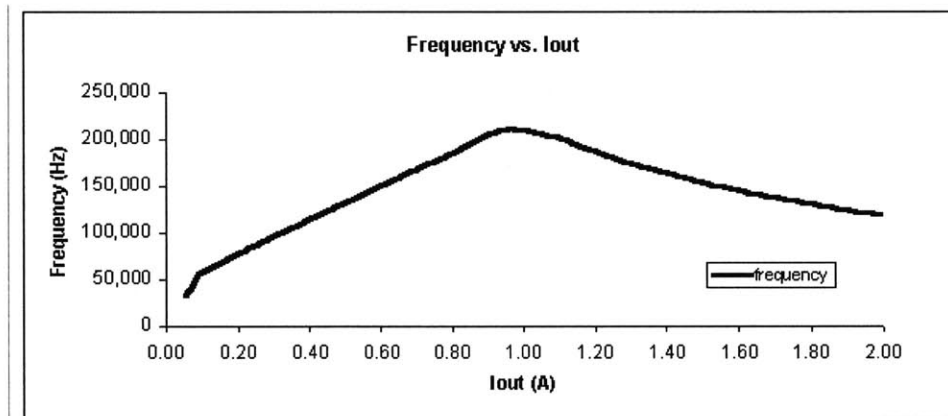

Figure 4-7: Frequency vs. I_{OUT} for linear delay before I_{swPk} clamped.

Figure 4-7 above shows the resulting frequency versus output current. The frequency curve changes slope again at a certain point which corresponds to the transition between BCM and DCM. The transition in this case is much more gradual than that of the previous example. Figure 4-8 shows the output current data plotted against V_c. The graph again shows the change in slope that occurs as delay is added to the converter. The change in slope is a little smoother, but still sharp. The change in slope directly relates to

the DC gain of the system. A more gradual curve across V_c would be preferable and more stable.
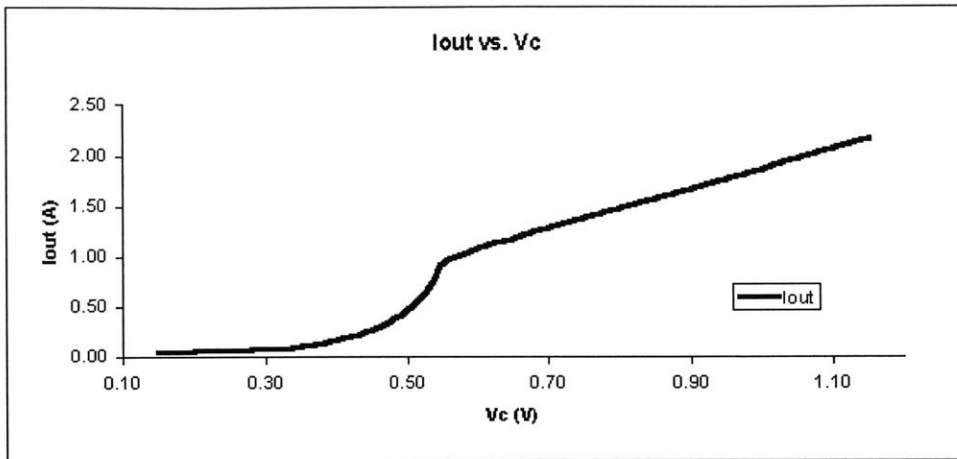

Figure 4-8: I_{OUT} vs. V_c for linear delay before I_{swPk} clamped.

4.2.3 Quadratic Delay before IswPk Clamped

The third method added delay with a quadratic slope before the switch current reached its clamped level. The addition of delay and switch current with V_c is shown in figure 4-9 below.
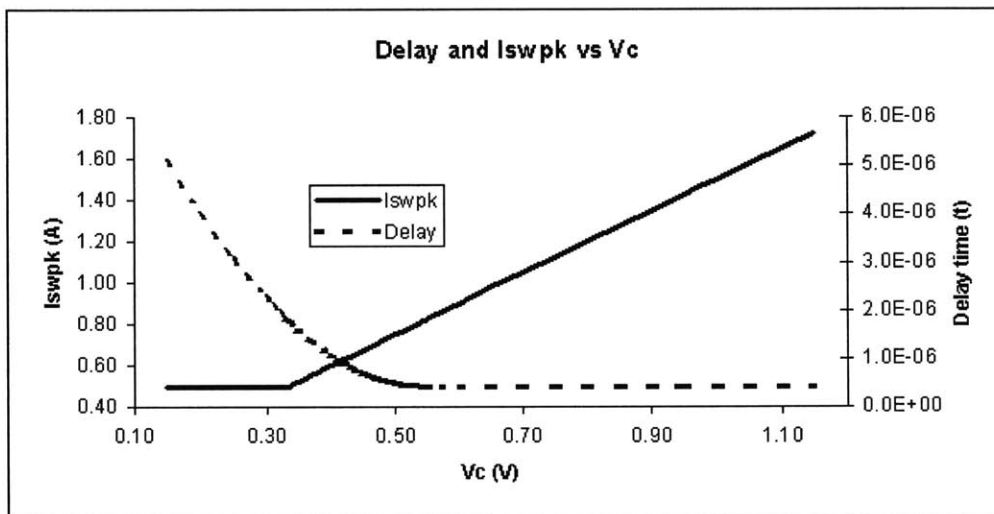

Figure 4-9: Delay & I_{swPk} vs. V_c for quadratic delay before I_{swPk} clamped.

The effect of adding delay in this manner was compared to the previous two methods by using the same input to output voltage ratio and transformer. The resulting frequency versus output current is shown in figure 4-10.
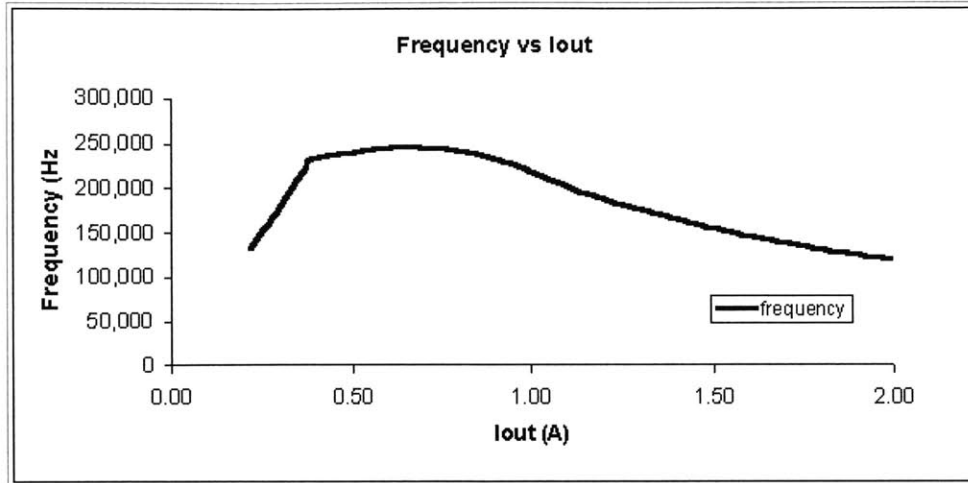
Figure 4-10: Frequency vs. I_{OUT} for quadratic delay before IswPk clamped.

The frequency curve presented above shows a nice flattening affect at the point where the converter changes between BCM and DCM. The frequency picture remains relatively flat until the switch current becomes clamped. In the next figure, output current is plotted against V_c. Figure 4-11 shows the curve below. The curve shows a very slight change in slope at the point where the converter transitions between BCM and DCM. The overall slope looks fairly consistent until the converter reaches very low output currents. The DC gain of the system will show a smoother characteristic since the transition is much more gradual.
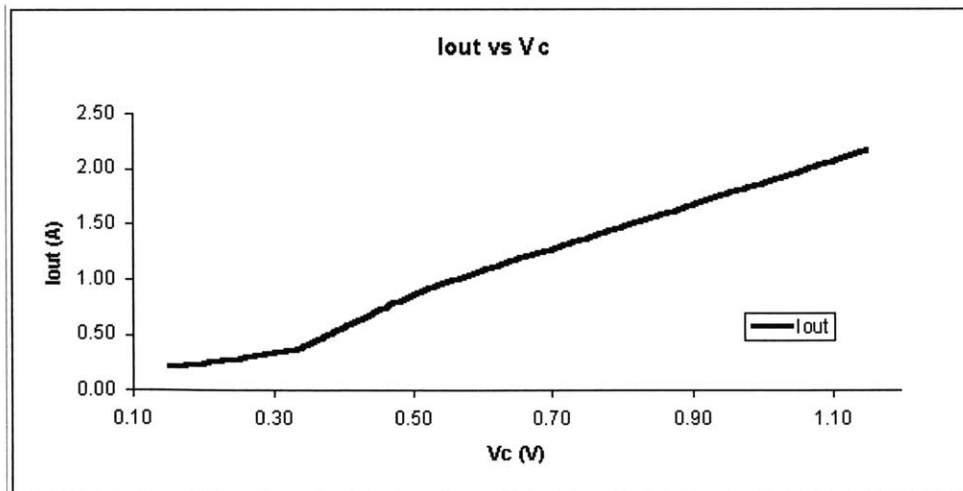

Figure 4-11: I_{OUT} vs. Vc for quadratic delay before I_{swPk} clamped.

4.2.4 Conclusion to Slope Delay Insertion

From the following discussion, it appears there are many ways to change delay and IswPk with V_c when entering DCM. The flexibility can lead to a wide variety of options. Each option has its own impact on the frequency of operation across load current along with DC gain. The graphs shown for each delay method examined key operating characteristics impacted by adding delay a certain way. The slope of output current versus V_c relates directly to the DC gain of the system. Sudden changes in the slope of this curve will negatively impact loop stability. Sudden changes in slope add peaking in the magnitude response of the loop and make it harder to compensate the system to avoid oscillations. In section 5, an actual implementation of one of the methods will be shown with its resulting impact on the converter's dynamic characteristics.

It is important to realize that the goal of the thesis was to develop a simple solution that could eventually be integrated into a SOT-23 package. More complicated strategies for adding delay or changing I_{swPk} were not investigated as much as the simpler and more achievable strategies.

4.3 Feedback Loop

A good understanding of the converter dynamics and overall loop dynamics was important to understand the impacts of choosing one form of delay addition versus another. Also the loop dynamics played a key role when trying to compensate the system and maximize the converter's bandwidth. Understanding the high-level block diagram was the first step in tackling the loop dynamics. In figure 4-12, a rough picture of the loop is presented.
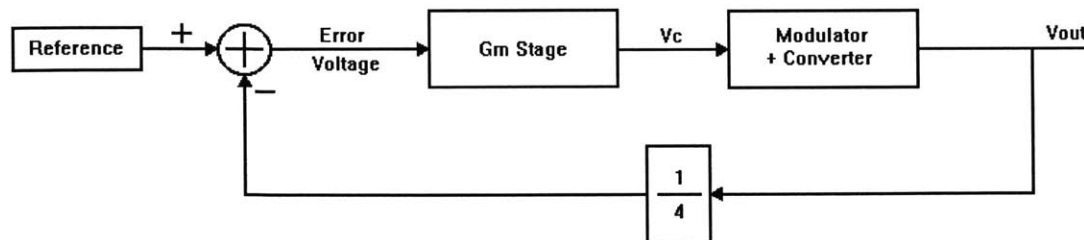

Figure 4-12: High-level block diagram of the overall control loop.

The figure shows the block diagram with two major forward blocks. One is the gm or transconductance stage and the other is the modulator. The modulator and converter represent the flyback converter and its dynamics. The input to the system is the reference voltage. An error signal is created when a fraction of the output voltage is compared to the reference. At this point the error signal drives the gm stage that then drives the modulator. The output is regulated because of negative feedback around the loop assuming the loop is stable. The voltage signal at the output of the gm stage is called V_c. The modulator then takes the control signal V_c and converts it to an output current. Next the output current is averaged across the output capacitors and load to become an output voltage. The output voltage is divided down and fed back to close the loop.

4.3.1 Transconductance (Gm) Stage

The first part of the loop is the transconductance, or gm, stage. The gm stage takes the difference between the fraction of the output voltage and the reference and generates a proportional current. The current generated in proportion to this error signal is then converted back to a voltage through the compensation network. The compensation network consists of the output impedance of the gm-amp and any additional resistors and capacitors placed on the output of the gm-amp. The resistor and capacitors set where poles and zeroes of the transconductance stage are located. For example, if just a capacitor is placed at the output of the gm amp, a pole is created at the frequency f =

$\dfrac{1}{2 \cdot \pi \cdot R_{outgm} \cdot C_Y}$. R_{outgm} is the output impedance of the gm-amp. Additional poles and

zeroes can be added. The type of compensation used to compensate the entire system was similar to that shown in figure 4-13.
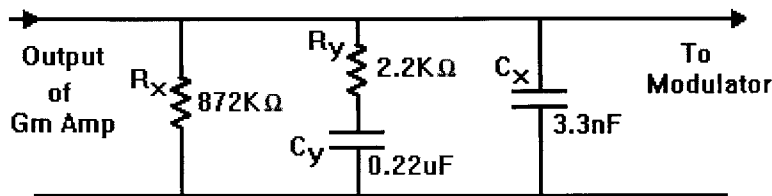

Figure 4-13: Example of one type of compensation network used with a gm amp having output resistance Rx shown above.

The compensation network created here consists of two poles and a zero. The first pole is a combination of the output impedance of the gm-amp and the large capacitor in the R-C series combination. Then the zero is created with the resistor and the capacitor in R-C series. The final pole is created with the resistor in the R-C series and the small capacitor in parallel to everything. The calculations for the compensation network above are presented below.

The following approximation allows one to quickly determine the poles and zeroes because the values of the resistors and capacitors are conveniently spread out in value. Separation between the individual values allows a certain combination of resistor and capacitor to dominate at certain frequencies.

The first pole calculated is: $f_{p1} = \dfrac{1}{2\pi \cdot R_X \cdot C_Y} = \dfrac{1}{872k\Omega \cdot 0.22\mu F \cdot 2\pi} = 0.83 Hz.$

The calculation for the zero is: $f_{z1} = \dfrac{1}{2\pi \cdot R_Y \cdot C_Y} = \dfrac{1}{2.2k\Omega \cdot 0.22\mu F \cdot 2\pi} = 329 Hz.$

The calculation for the final pole is: $f_{p2} = \dfrac{1}{2\pi \cdot R_Y \cdot C_X} = \dfrac{1}{2.2k\Omega \cdot 3.3nF \cdot 2\pi} = 22 kHz.$

Another important feature of the gm-amp is that most of the DC gain for the entire loop comes from the gm stage. The rest of the DC gain comes from the modulator and converter block. The gm stage magnifies the error between the reference and the divided down output voltage. The level of magnification of the error impacts the regulation of the output. The output regulation is a function of the total DC gain available. For example with a smaller DC gain, a larger error signal is necessary to move the converter to the correct operating point. When the system has low DC gain the output voltage must move more to create the right error signal.

A better way to think about the importance of the gm stage is the idea that a specific value of V_c corresponds to a specific output current level when the output voltage is regulated. Small movements in the output voltage are amplified through the gm stage to move to the correct value of V_c. If the gm stage did not have enough gain, then the output would have to move a larger amount to move the V_c voltage to the right level.

The more the output voltage must move across output current levels the worse output regulation across load becomes.

Venable results:

The next step was examining the actual transfer function of the gm stage. The gm stage was built using a LTC38301 and used the pin outs just connected to the gm stage. The data sheet for the part reports that the dc gain for the gm-amp was typically 55db and the output impedance is on the order of 870kohms. The bode plot in figure 4-14 shows the transfer function of the gm-amp with the exact compensation network described in the section above. From the plot the poles are approximately located at 1.5Hz and 19 kHz, and the zero is located at 327Hz. Also from the graph, the DC gain is approximately 50dB. The data then matches the data predicted for where the poles and zeroes should be located.
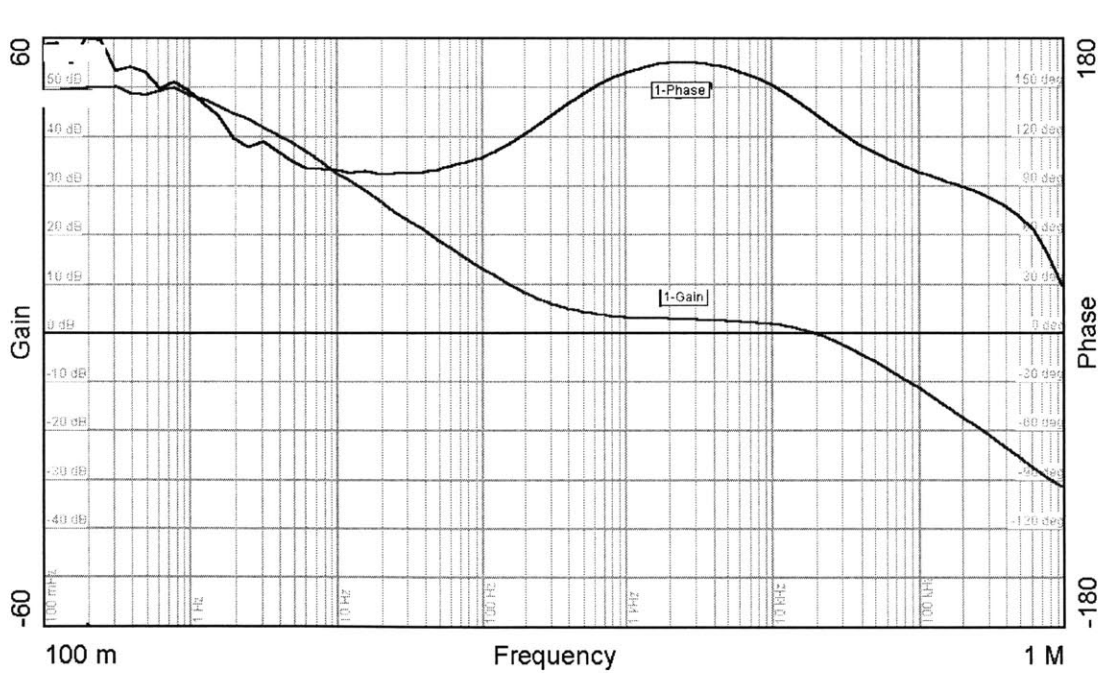

Figure 4-14: Bode plot of transconductance transfer function with compensation.

4.3.2 Modulator and Converter

The next piece of the loop is the modulator and converter. The modulator consists of the converter control loop from control to output. In the case of the flyback

converter, it is driven with a signal corresponding to the peak switch current. The control signal commands some current in the switch. Once this current level is reached, the switch opens and the energy is transferred to the output to recharge the output capacitors and supply the load. In this process, a smaller loop is closed around the primary inductor to command the correct amount of switch current. Therefore regardless of the input voltage, the converter reaches the same peak current level commanded by V_c. The current sense amplifier and the switch current comparator close the minor loop around the switch current. Control of the switch current in this manner gives rise to the name current-mode control. Figure 4-15 shows the block diagram of the minor current loop in the modulator.
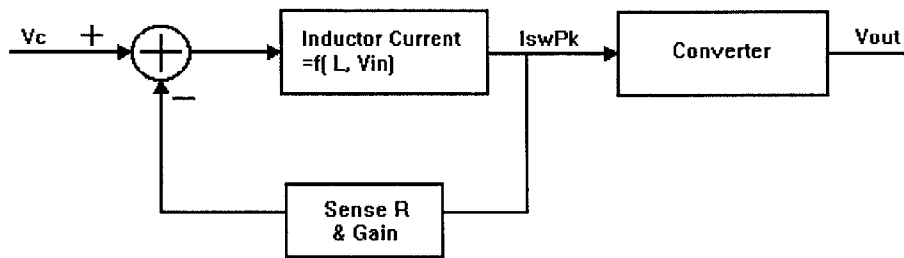

Figure 4-15: Diagram describing the modulator with minor loop for switch current.

The transfer function labeled "Converter" in figure 4-15 is the toughest to understand. This transfer function represents the dynamics from a control voltage to the output voltage. Luckily some work has been done on developing models to understand the operation of switching converters operating in CCM and DCM. Two methods known as average state space modeling and average circuit modeling allow examination and modeling of switch mode power supplies [6].

The flyback converter can be modeled as if it is operating in discontinuous mode since no energy is stored in the transformer across cycles. Since no energy is stored across cycles, the energy commanded in the switch is immediately transferred to the output. Therefore the average circuit model consists of just the output diode and the output network of the flyback. The diode must be averaged to get the average model of the DCM flyback circuit. The model is presented in figure 4-16 below with the average value for the diode shown in figure 4-17. The diode current is averaged in a running fashion across a cycle to obtain its average model [6].
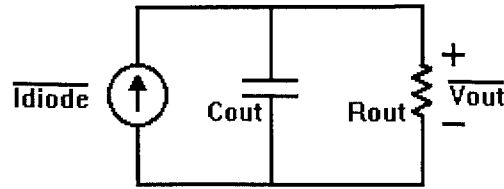
65

Figure 4-16: Average DCM flyback model.

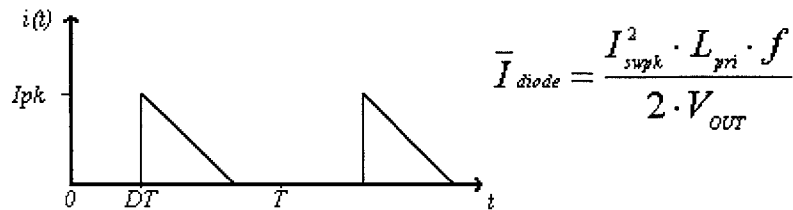$$\overline{I}_{diode} = \frac{I^2_{swpk} \cdot L_{pri} \cdot f}{2 \cdot V_{OUT}}$$

Figure 4-17: Average model for the diode in the DCM flyback model.

The converter dynamics can be modeled simply as a first order system. The inductor is effectively ignored because the system does not store charge across cycles and the bandwidth of the system will be much lower than the location of the pole created by the inductor in the transformer. The next step in predicting the converter dynamics linearizes the model presented above. Linearization is accomplished using Taylor expansion of the average current with respect to V_{OUT} and I_{swPk}. It is important to note that the frequency also changes. In order to be complete, a more accurate model for frequency must be used.

Frequency can be represented as: $f = \dfrac{1}{t_{on} + t_{off} + t_{delay}}$.

The flyback converter designed has two basic modes of operation. One where no delay is added and the converter operates in boundary mode, and then the mode where delay is added and the converter operates in discontinuous mode. For example in boundary mode, the frequency term does not have a delay term.

Therefore frequency can be represented as: $f = \dfrac{1}{t_{on} + t_{off}} = \dfrac{Vin \cdot Vout}{L_{pri} \cdot I_{swpk} \cdot (Vout + Vin \cdot N)}$.

Using this term for frequency the average model for the diode can be simplified to:

$$\bar{I}_{AvgDiode} = \frac{I_{swpk} \cdot Vin}{2 \cdot (Vout + Vin \cdot N)} \cdot$$

Linearizing the average diode current using a Taylor series expansion up to linear terms results in an expression as follows:

$$\tilde{I}_{AvgDiode} = \frac{V_{IN}}{2 \cdot (V_{OUT} + V_{IN} \cdot N)} \tilde{I}_{swpk} - \frac{I_{swpk} \cdot V_{IN}}{2 \cdot (V_{OUT} + V_{IN} \cdot N)^2} \tilde{V}_{OUT} \cdot$$

With the linearized model presented above, a circuit model can be created to understand dynamic operation of the flyback converter in BCM [6]. The model predicts a current source dependent on small changes about I_{swPk}, and another source dependent on output voltage that can be treated as a resistor across the output. The modeled resistance in parallel with the output impedance of the load becomes the output impedance of the converter in BCM. In addition, the DC gain of the system can be predicted and modeled at various line and load conditions with the models above.

Figure 4-18 shows a bode plot of the input to output characteristics of the modulator. The bode plot corresponds with a first order system with a single pole role off and matches the model introduced above.
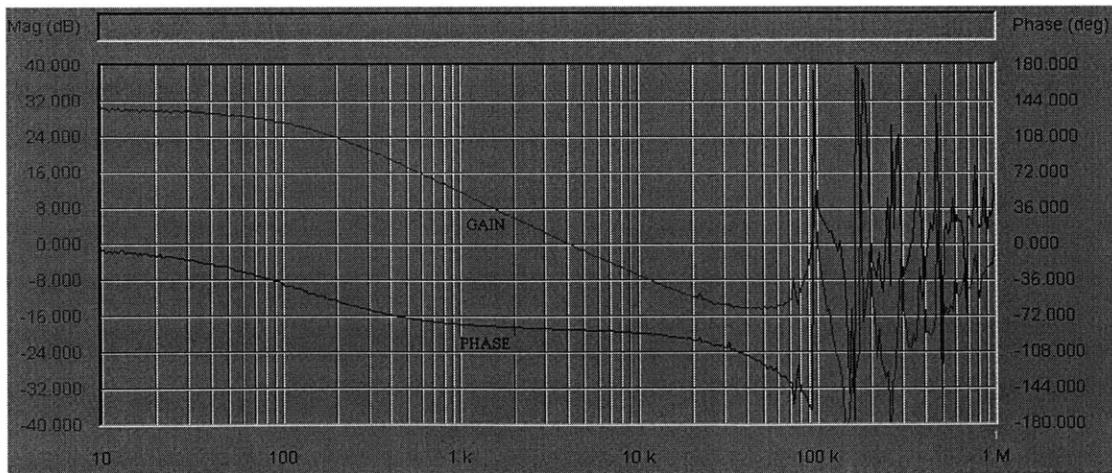

Figure 4-18: Measured bode plot of the modulator and converter from input to output.

In DCM the frequency changes as delay is added and the model for frequency must include this effect. Another linearized average circuit model must be derived for DCM. The resulting model for this mode of operation is not presented here, but can be determined in a similar fashion. The combination of the two models effectively models the dynamic operation of the converter.

4.3.3 Compensating the Loop response

The next step was compensating the feedback loop around the flyback converter. The compensation network has a large impact on the dynamic performance of the converter. The bandwidth of the system depends on how the loop is compensated. In addition, the ability to respond to load transients is directly dependent on how the loop is compensated.

Stability of the loop response sets where the loop can be compensated. Stability is related to the phase margin of the loop. The converter and the gm-amp introduce poles and zeros that place limits on the compensation scheme. In addition, the converter is a switching system, so another effect on phase is introduced. According to Nyquist, the loop must cross over before the switching frequency otherwise issues such as aliasing are introduced. If information is allowed through the loop around this point, the information will be incorrect. In other words, phase margin around the switching frequency degrades and stability is unattainable if the loop gain crosses unity near the switching frequency.

It is important to remember that stability must hold across the entire load and line range. The final compensation network chosen must be checked across the entire line and load range because DC gain and output impedance move with load current.

4.3.3.1 Bode plots

Figure 4-19 shows an example of the converter loop bode plot with direct feedback. The bode plot shows the magnitude and phase. The output impedance of the converter and the output capacitance introduces a low frequency pole. Then another pole is introduced from the compensation network. The magnitude exhibits a two-pole role off at low frequencies. The two-pole role off introduces almost 180 degrees of phase shift, making it hard to cross over with sufficient phase margin. Then a zero, from the

compensation network, is introduced near crossover to add phase margin to the system. Finally, another high frequency pole, from the compensation network, is introduced to roll off the magnitude additionally at high frequency. This helps to prevent any high frequency dynamics from affecting the loop response.
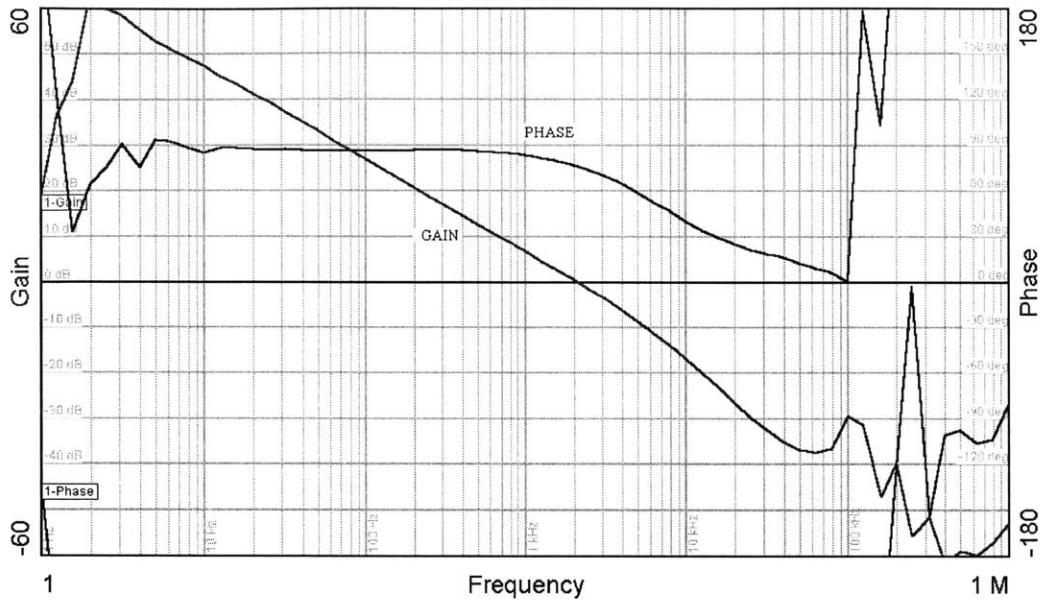

Figure 4-19: Bode plot of the control loop from control to output.

4.3.3.2 Transient Response

The transient response provides another way of determining the phase margin and bandwidth of the system. The type of response shown when viewing the transient response is directly related to both the phase margin and bandwidth of the system. For example a lightly damped response is typical of systems with forty-five degrees of phase margin or less. A phase margin of more than forty-five degrees results in a well damped response to a step change.

Transient response was tested on the flyback converter by changing the load between minimum current at 100mA to maximum current at 2A. A square wave was used to pulse a MOSFET on the output that allowed quick transitions between the two output current levels. In the figure below, transient response measurement was done on the flyback converter system. The graph in figure 4-20 shows the output voltage when the load changes between .1A and 2A.
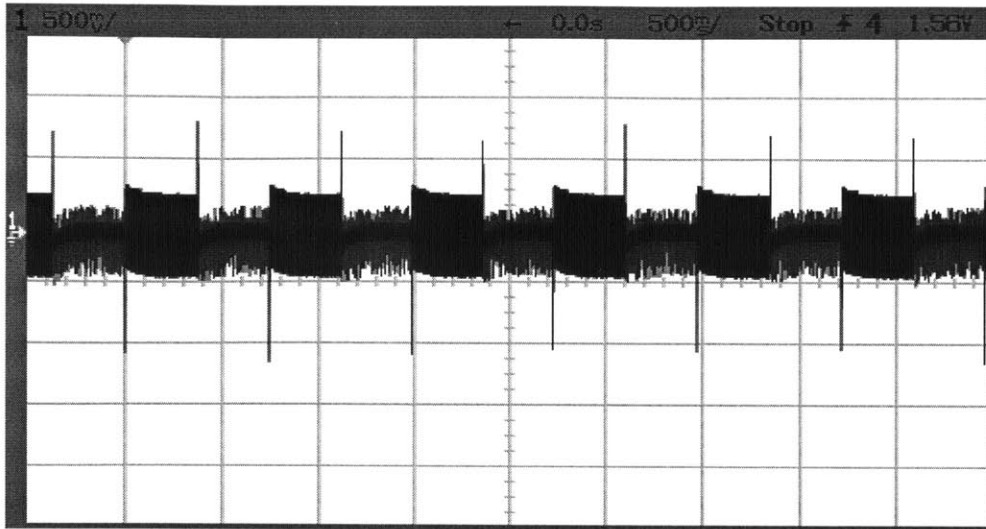
69

Figure 4-20: Transient response in isolated flyback conversion from 0.1A to 2A with vertical sale 500mV/div and horizontal scale 500ms/div.

The response in figure 4-20 has two key features, the amount of output voltage change before the converter responds and returns to regulation, and the way it returns back to regulation. The first effect is a function of the bandwidth of the system and the amount of output capacitance. For example when a load transient from minimum current to maximum current occurs, the output voltage drops because the converter is only delivering enough current to satisfy the lower current level. When the load moves to 2A, the only place that can deliver energy is the output capacitors. The output capacitors pull on their reserve charge to meet the load requirement. The controller is restricted in how quickly it can respond according to its bandwidth. Therefore, the output voltage falls until the controller responds to the higher current level. Figure 4-21 shows the output falling during a transient from 0.1A to 2A.
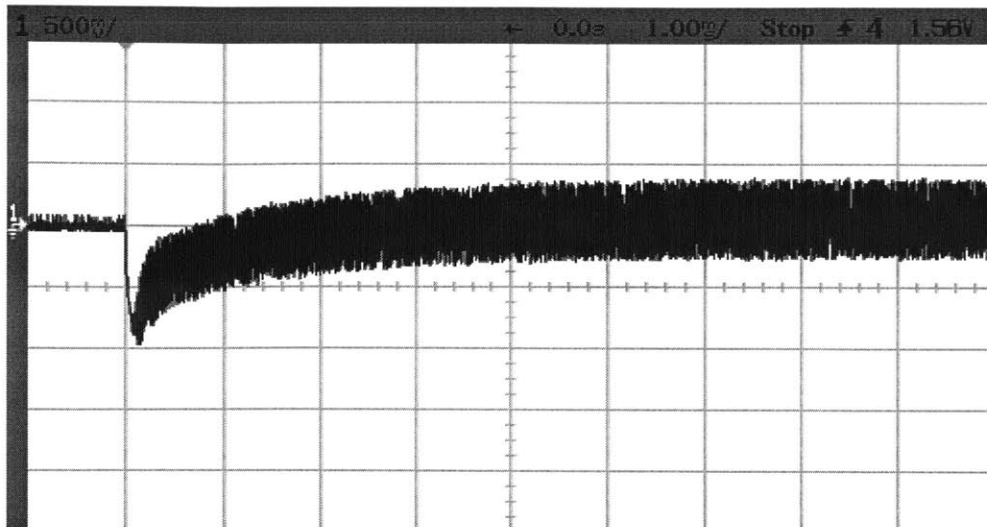
Figure 4-21 Output voltage transient from 0.1A to 2A load setting with vertical scale 500mV/div and horizontal scale 1ms/div.

The second feature of the transient response is based on the phase margin of the system. A well damped response is a function of higher than 45 degrees of phase while a lightly-damped response is a function of around 45 degrees of phase or less. The transient response at .1A to 2A shows a first order response that corresponds well with greater than 45 degrees of phase margin.

Next, the output capacitance was doubled to see the effect on the transient response. Figure 4-22 below shows the transient response with double the output capacitance and the effect on the output voltage. The effect is quite visible as the amount of output voltage drop is halved and the amount of ripple across output voltage is reduced!
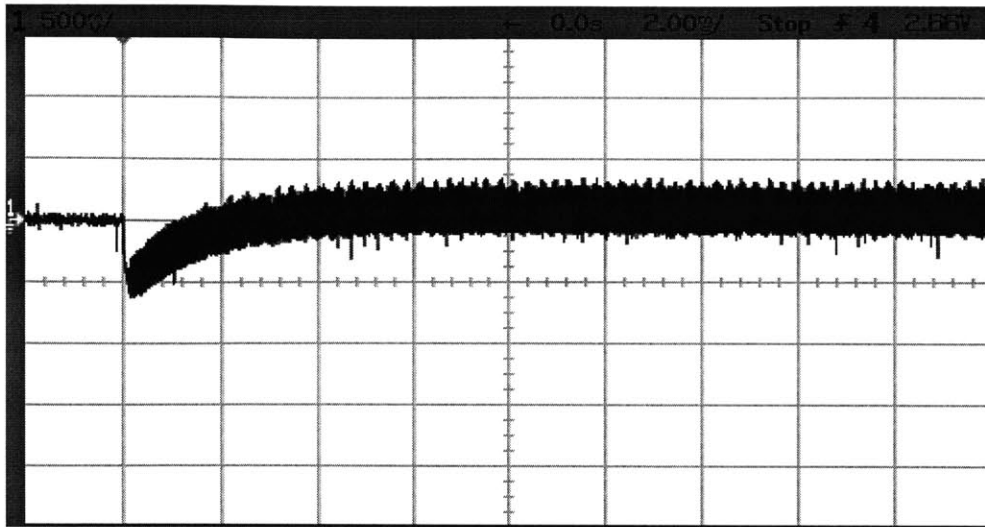
Figure 4-22 Transient response from .1A to 2A with double the output capacitance with vertical sale of 500mV/div and horizontal scale 2ms/div.

4.3.3.3 Effect of Isolated vs. Direct Feedback

The next interesting aspect of the compensation research on the converter was looking at the effect of connecting feedback in an isolated manner versus direct connection to the output. The isolated circuitry incorporates both a track and hold followed by a sample and hold to acquire information about the output to close the feedback loop. The bode plot below in figure 4-23 shows the close loop response with direct feedback and isolated feedback using the sample and hold.
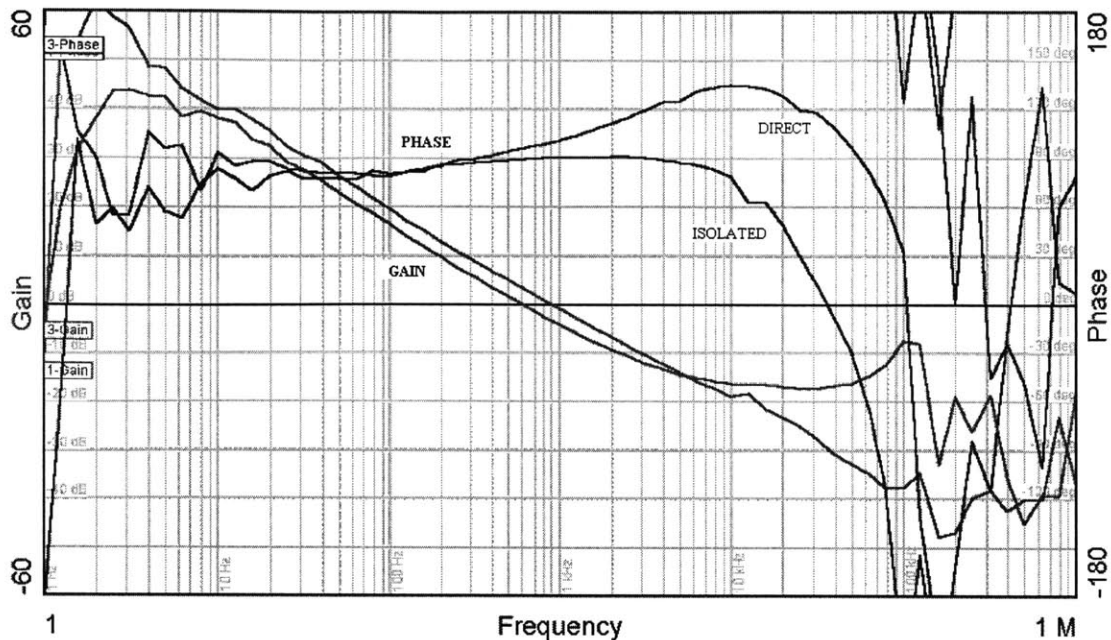
Figure 4-23 Bode plot showing loop response with isolated feedback and direct at 2A.

The important feature of these two loop responses is the phase plots. Both loop responses were taken at two amps out at 48Vin with the switching frequency at 113 kHz. The direct feedback phase curve is the one that shows a higher amount of phase across frequency, while the one beneath it is the phase associated with isolated feedback. Both phase curves show a sudden steep drop in phase around a certain frequency. The sudden loss of phase could be compared to a time delay, since phase changes dramatically, while the magnitude does not. The sudden phase drop off can be explained by the sampling effects of the switching system [15]. In the direct feedback case, the phase begins to drop off at about half the switching frequency. In comparison, the isolated feedback setup begins to lose phase at one fourth the switching frequency. The direct feedback phase curve hits -45° of phase at about the switching frequency, while the isolated feedback phase reaches -45° at about half the switching frequency.

The method of collecting output information and ultimately closing the feedback loop determines how the Nyquist frequency affects the phase response. In the direct feedback case, the converter acts on the output information once every switching cycle. On the other hand in the isolated case, the converter must wait two cycles to act on output information. The track and hold samples the output information once every cycle, but this

73

information does not get to the gm-amp until it is sampled. The sample and hold circuitry does not transfer the data from the track and hold until the switch turns on again. Therefore, the feedback connection with the sample and hold exhibits another layer of sampling delay resulting in phase loss at a lower frequency.

When determining loop compensation and overall transient performance, the compensation scheme must take into account the extra amount of phase loss in the isolated case. The extra phase loss associated with the Nyquist frequency places an extra constraint on the maximum achievable bandwidth. The maximum achievable bandwidth then places constraints on the transient response.

4.4 Control Theory Conclusion

Important areas of the controller and the control theory have been presented. Each of the areas covered here are important in understanding how the flyback will operate when it is in BCM and when it enters DCM. The next section begins to explain the board level implementation of the flyback in discrete components. In addition, it presents data which supports the data and information presented in this section.

5 Proof-of-Concept Board

The next step in developing the proposed converter was building a proof-of-concept board that integrated all the parts to create a regulated power supply. Experimentation with the Siemens part provided a good medium to understand boundary mode control of a flyback converter. Closed loop regulation along with tight output regulation was shown possible with the Siemens part. After attaining favorable results using the Siemens part, it was important to now build a full-blown implementation of the proposed controller. The controller needed to integrate a method of dealing with light loads. In addition, a complete proof-of-concept board needed to be built to provide the next-level of understanding and testing towards a working IC solution.

5.1 High-Level Block Diagram

A high-level block diagram of the isolated flyback is presented in figure 5-1 below. The high-level block diagram makes it much easier to understand the flow of information required to build a working solution. Each block was built using discrete components such as op-amps, comparators, and logic building blocks. In addition, a few of the pieces include transistor level design because adequate IC components were unavailable at the time.
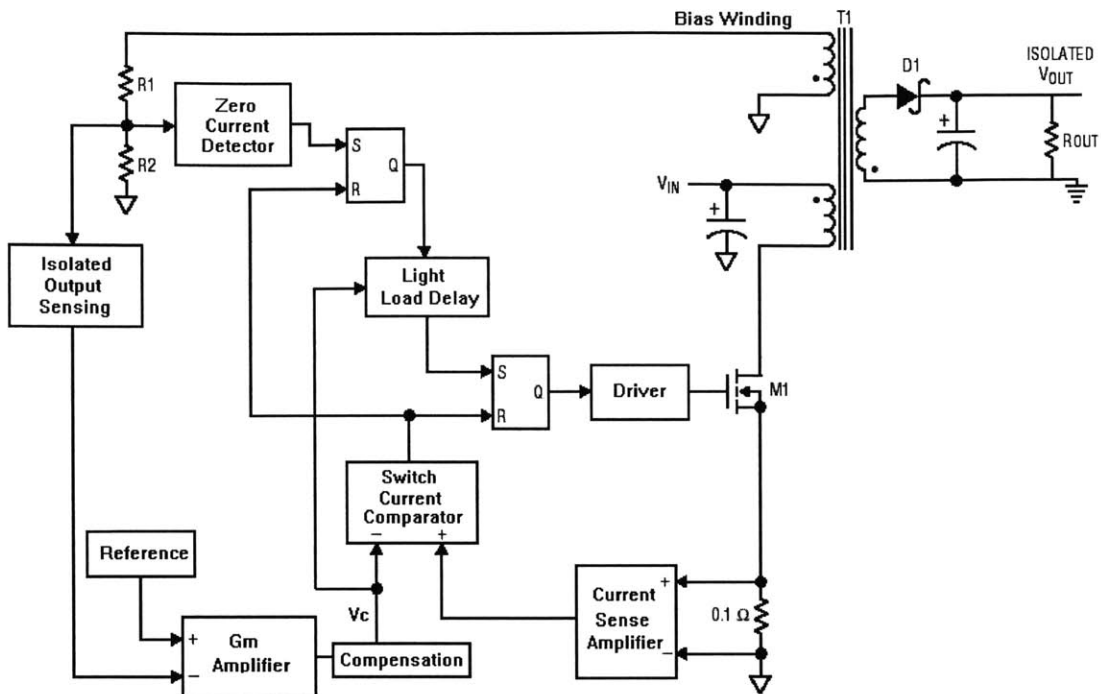
Figure 5-1: High level block diagram of proof-of-concept board.

The block diagram introduced above provides a simplified view of the entire proof-of-concept board. The actual circuit implementation will be given in the next section where each block will be described. Figure 5-2 shows the built proof-of-concept board. The picture provides a sense of comparison between the block diagram in figure 5-1 and the actual implementation.
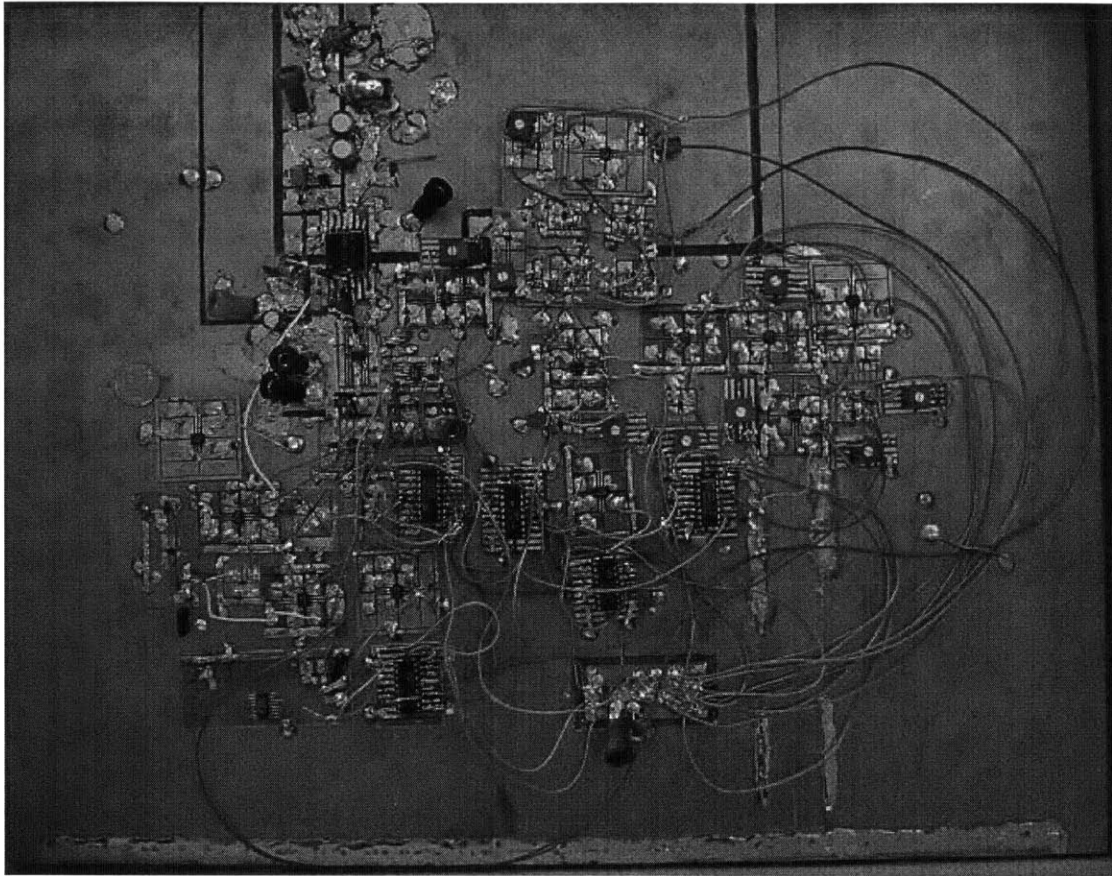
Figure 5-2: Built proof-of-concept board in final form.

5.2 Detailed Circuit Implementation

The following sections detail the various pieces of the final, working proof-of-concept board. The circuit descriptions represent the chosen topologies used to obtain the data and results which are presented in the final sections.

5.2.1 Flyback Application Circuit

The first and most important piece was the flyback applications circuit. The application circuit included the transformer, switch, output diode, input and output capacitors, and current sense resistor. The application circuit was required to operate from an input voltage of 36 to 72V and regulate at an output voltage of 5V across a load range of zero to two amps. Figure 5-3 shows the application circuit.
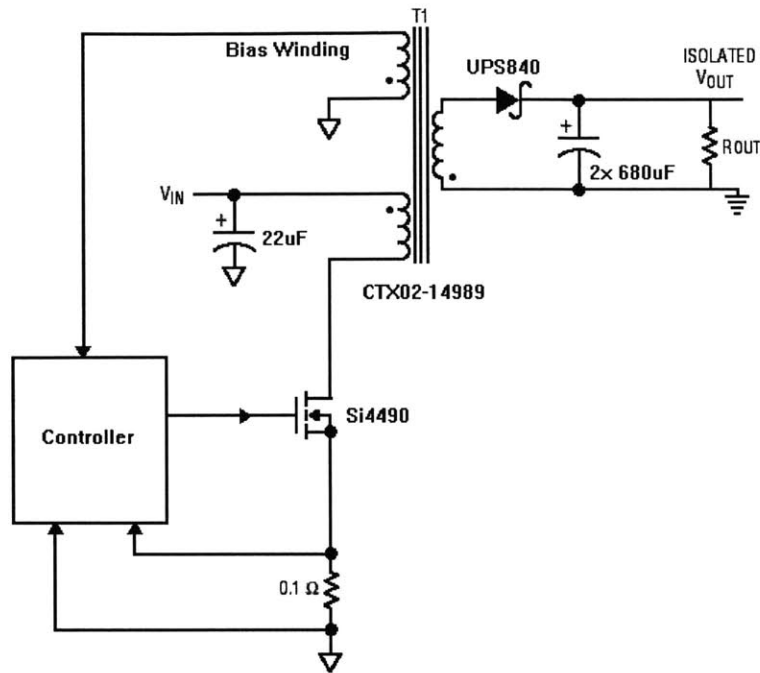
Figure 5-3: Flyback application circuit with components used.

The transformer used was the CTX02-14989 (Cooper Electronics, FL). This transformer has one input winding, a secondary output winding, and a third bias winding. The turns ratio is 5:1:3. In addition, the primary inductance is approximately 100uH. The switch chosen was the Si4490 N-Channel MOSFET. The FET featured a V_{DS} of 200V with a continuous drain current of up to 2.5 amps. The output schottky diode used was the UPS840 with an 8A average rectified forward current rating and a 40V reverse voltage rating. Next, a current sense resistor of 100mOhms was used. Finally two 680uF SANYO 6.3V electrolytic output capacitors were used each with an ESR of 13mOhms above 150 kHz. The input capacitor used was a 22uF SANYO 100V electrolytic capacitor.

5.2.2 Current Sense Amplifier

The current sense amplifier was required to magnify the current information provided by the current sense resistance. Accurate current information was required to ensure correct cycle by cycle switch current. The current sense amplifier consisted of three stages. The first stage was amplification. Then a one volt offset was added to the

current sense signal. The final piece of the amplifier was a blanking circuitry to remove current spikes occurring during the turn-on transition of the switch.

The complete circuit schematic is presented below in figure 5-4. The amplification stage was built using the LT1810 high-speed op-amp. The amplifier magnified the signal a factor of 10. Then a one volt offset voltage was added using a simple op-amp adder with the LT1801 op-amp. Then a pull-down 2N3904 blanked the magnified current sense signal. A one-shot logic block triggered the turn-on of the 2N3904. Turn-on of the primary switch triggered the one-shot logic block.
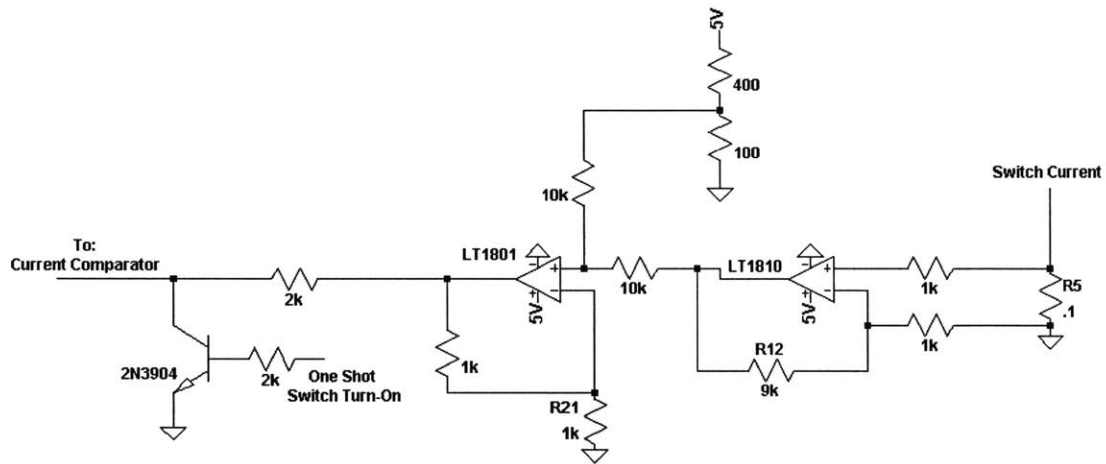

Figure 5-4: Current sense amplifier stage.

5.2.3 Isolated Output Voltage Sensing

The next important piece of circuitry was the isolated output voltage sensing. The circuitry extracted output voltage information using the bias winding. The circuitry consisted of two major parts. The first part was the track & hold amplifier that was first introduced in section three. The next piece took the held information and transferred it to the transconductance amplifier. Figure 5-5 highlights this two stage approach.
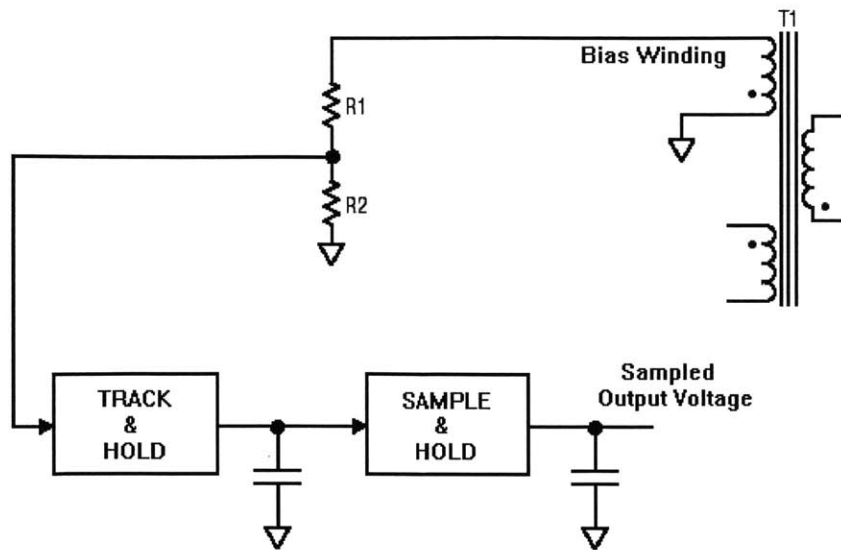
Figure 5-5: Block diagram of isolated sensing technique.

5.2.3.1 Track & Hold (T&H)

The track and hold amplifier shown below in figure 5-6 was essentially the same circuit described in section 3.4.2 of the thesis.
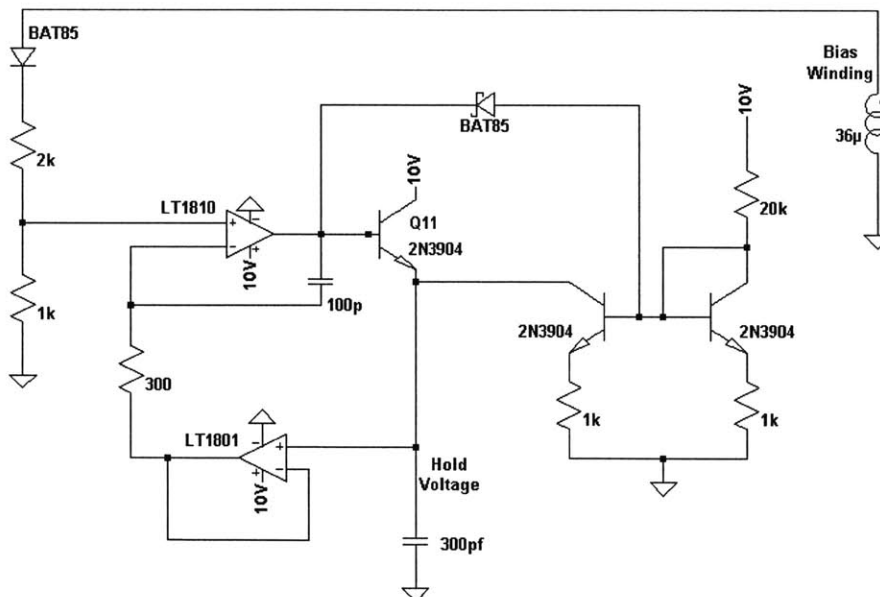

Figure 5-6: Track & hold amplifier with compensation.

5.2.3.2 Sample & Hold (S&H)

The sample and hold circuitry simply transferred the information held by the T&H stage. The sample and hold function was accomplished using the LTC203 analog switch and an op-amp buffer. The complete implementation is presented in figure 5-7 below.
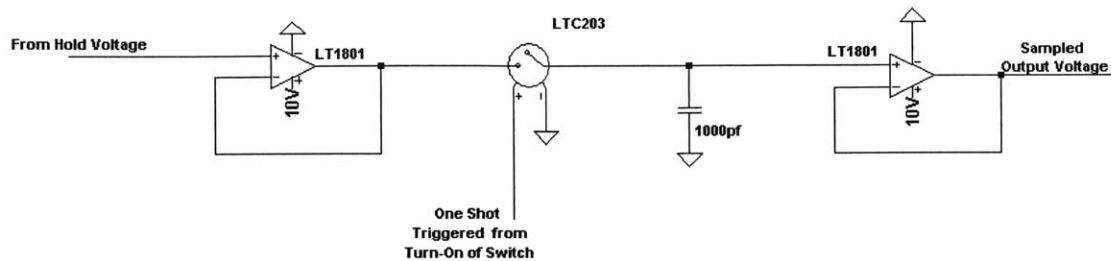

Figure 5-7: Sample & hold circuit implementation.

The LTC203 is modeled in the diagram above as a voltage-controlled switch. The turn-on of the primary switch triggered the sample and hold. Once the LTC203 was triggered, the held information was transferred to the input of the transconductance stage using a LT1801 op-amp buffer.

5.2.4 Voltage Reference

A voltage reference was required to provide an accurate and regulated reference. The reference was compared with a divided down representation of the output voltage. The voltage reference was built using the LT1431 voltage reference and set to 1.25V. Figure 5-8 shows the application circuit using the LT1431.
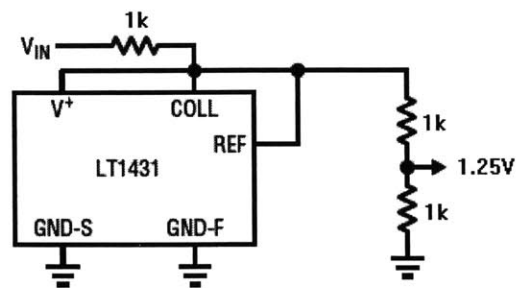

Figure 5-8: LT1431 1.25V voltage reference application circuit.

5.2.5 Transconductance (Gm) Amplifier

The next step was building a transconductance amplifier that would serve as the error amplifier for the controller. In section 4, the LT38301 served as the gm-amp for the design. After much testing and debugging it was determined that additional circuitry on the IC introduced noise on the output of the gm-amp. Therefore, a discrete gm-amp was built using individual transistors.

The gm-amplifier was built using discrete NPN transistors to provide a certain level of output impedance and transconductance. The transconductance of the gm amplifier would ultimately set the level of output regulation across both line and load. In addition, the output of the gm-amp would set the switch current levels for various line and load conditions. These different output levels needed to be generated from slight differences in the output voltage. The amount of transconductance in the gm-amp would determine how much output voltage change was required to change the switch current level a certain amount. Figure 5-9 show the transistor level schematic of the gm-amp. The gm-amp also includes a high side voltage clamp to ensure that the switch current does not exceed a certain amount. In addition, the gm-amp amp included the compensation network. The final compensation network consisted of two capacitors and a resistor. Finally a one volt offset is added to the output voltage level of the gm-amp to match the offset added by the switch current amplifier.
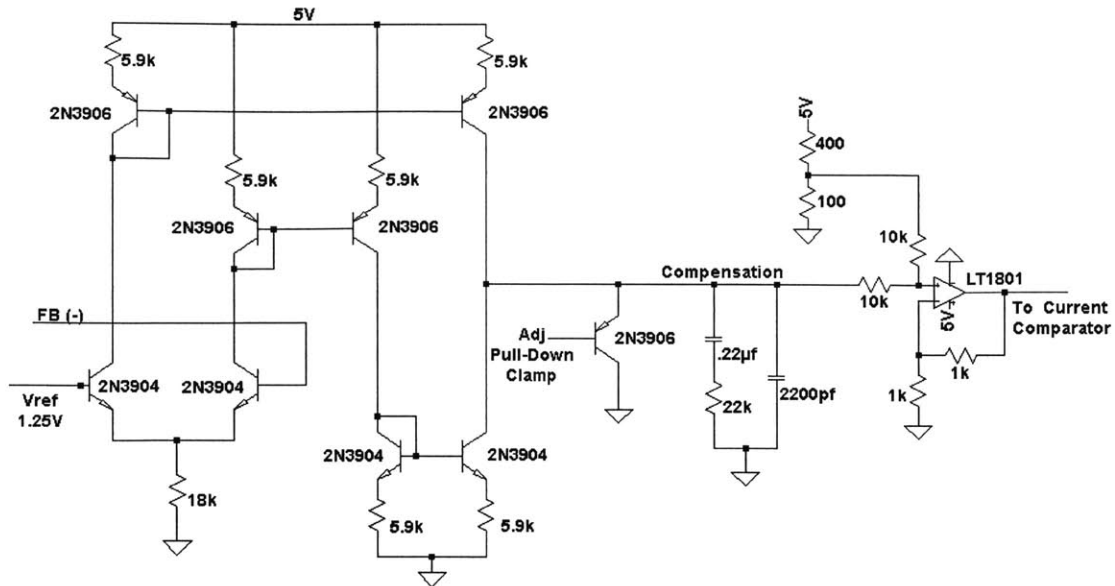
Figure 5-9: Gm-Amp with clamp network, compensation and voltage offset.

5.2.6 Switch Current Comparator

The next block was the switch current comparator. Figure 5-10 shows the switch current comparator block. The switch current comparator generates a signal that turns off the primary switch once the switch current reaches a level set by the gm-amp. The comparator compares the signal coming from the output of the gm-amp and compares it to the current sense amplifier output. When the switch current reaches the right level, the comparator triggers a one-shot logic block. The one shot then sends information which eventually turns off the switch. The LT1720 was used as the comparator.
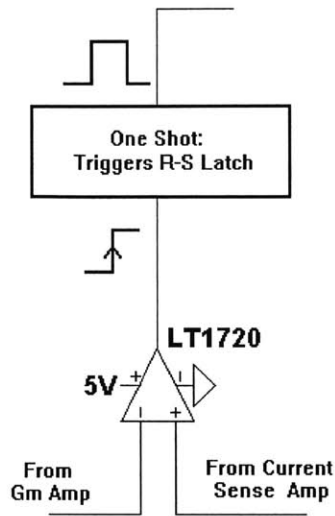
Figure 5-10: Current comparator.

5.2.7 Zero Current Detector

The zero current detector served a major role in triggering switch-turn on. In BCM operation, the switch only turns on after all the energy stored in the primary of the transformer is transferred to the output. The zero current detector served as the circuitry that signaled the completion of transferal of that energy. The detector monitored the bias winding information and turned on when the flyback voltage collapsed below a set level using a comparator. The LT1720 comparator was used as the comparator that triggered the one-shot logic block. Figure 5-11 shows the zero current detector.
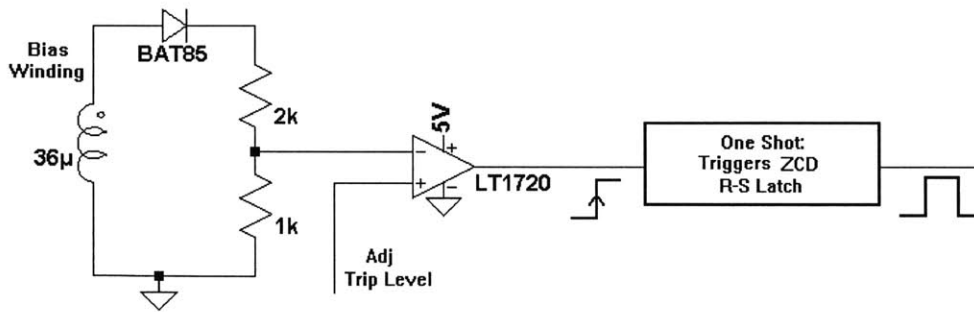

Figure 5-11: Zero current detector circuit block.

5.2.8 Zero Current Detect R-S Latch

The one shot information from the zero current detector was integrated into a R-S latch. The R-S latch was necessary because during light-load DCM operation, the flyback

voltage would ring once the voltage collapsed and output energy was transferred. The R-S latch prevented retriggering of the zero-current detector due to the ring on the bias-winding. The R-S latch was built using the 74HC109N logic IC. Figure 5-12 shows the input and outputs through the zero current detect R-S latch. The output of the zero current detector triggers turn-on of the linear-delay circuit.
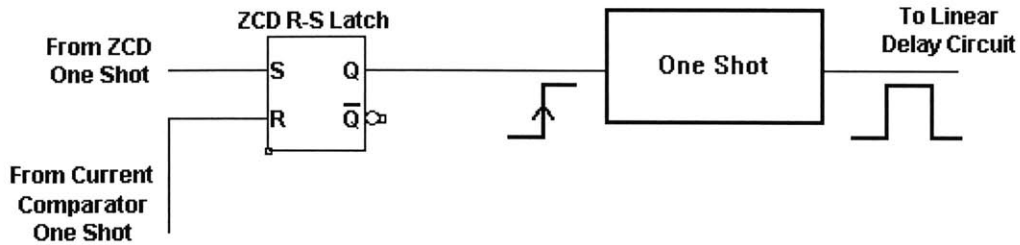

Figure 5-12: Input and output connections to zero current detect R-S latch.

5.2.8 Light Load Delay Circuit

The implemented light-load delay circuit consisted of a couple op-amp blocks and transistor pieces. The gm-amp voltage was used to set the trip level for a linear timing ramp circuit. A constant current source charged up a capacitor to create a constant linear voltage ramp. The voltage ramp served as one input into the LT1720 comparator, while the other input served as the trip voltage. Changing the trip voltage higher would relate to a longer amount of time before the comparator would transition high. The transition of the comparator then triggered a one-shot that would reset the switch control R-S latch and the zero current detect R-S latch. Figure 5-13 shows the complete light-load delay circuit.
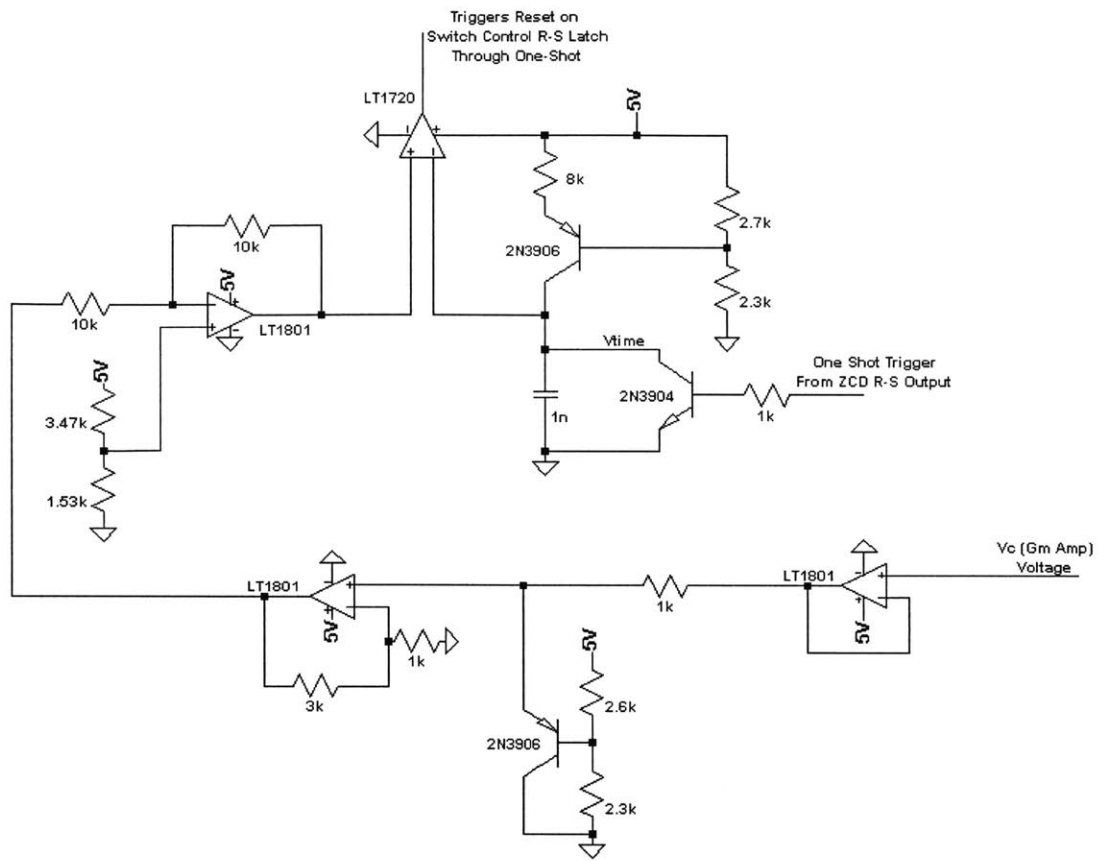
Figure 5-13: Linear-slope delay circuit.

The voltage from the gm-amp was buffered using an LT1801 and then clamped. The clamp was necessary because at high output current levels light load operation was not required. Only at low output current levels was the delay circuit necessary. After clamping, the voltage was gained up and then subtracted from a constant voltage. The output of the subtraction served as the trip voltage. The circuit created a trip voltage that would increase as the V_c voltage decreased.

The next pieces generated a voltage slope that would allow the trip voltage from the previous discussion to directly relate to delay time. A constant current source linearly charged up a capacitor to create a linear voltage ramp. The capacitor was reset every cycle using a 2N3904 triggered using the output of the zero current detector. The scheme described generated a linear-slope delay that increased as V_c decreased below a certain level.

5.2.9 Switch Control R-S Latch

The following R-S latch sends the logic signal to the switch driver that controls the switch. The reset signal for the latch is generated from the switch current comparator. The delay circuit generates the set signal for the latch. Figure 5-14 shows both the inputs and the output to the latch. The 74HC109N logic IC served as the RS latch.
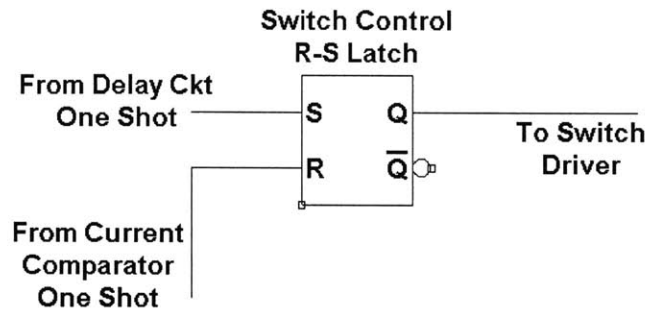

Figure 5-14: Switch control R-S Latch with inputs labeled.

5.2.10 Switch Driver

The LTC1693 was used as the N-channel MOSFET gate driver. The logic control signal was generated using the output of the switch control R-S latch. Figure 5-15 shows the implementation of the gate driver.
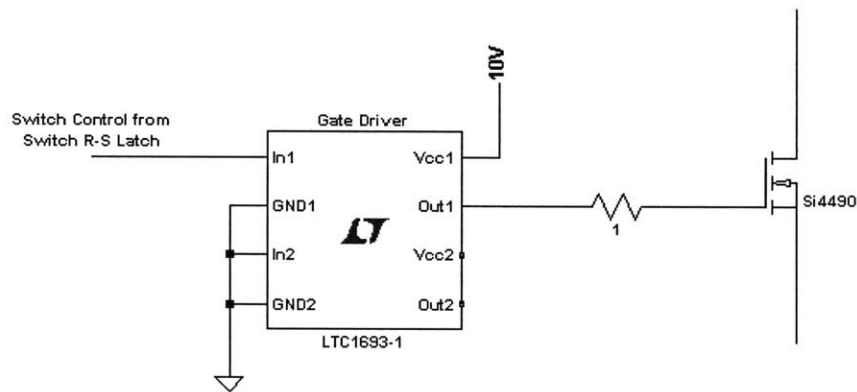

Figure 5-15: LTC1693 MOSFET gate driver controlled by switch R-S Latch.

5.2.11 One Shot Logic

The 74HC123 logic IC was used to create one shot pulses for various transition levels throughout the concept board.
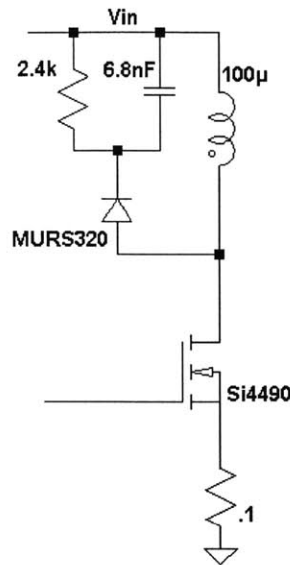
5.2.12 Primary Side Switch Snubber

Figure 5-16: Primary-side R-C switch snubber.

The primary-side switch snubber is shown above in figure 5-16. The snubber was built using a diode in series with the parallel combination of a resistor and capacitor. The resistor and capacitor values used in the snubber were calculated using formula's presented in Linear Technology application note 19. The R-C snubber served to clamp the voltage across the switch below its V_{DS} breakdown level.

5.3 Layout considerations

The proof-of-concept board was built entirely on copper-clad. The copper-clad board provided an excellent medium for testing, building, and modifying each piece as the design was built. In addition, the copper-clad served as an excellent ground plane.

5.3.1 Major Power Path

A very important piece of the building process was laying out the major power path. The major power path consisted of the application circuit shown in section 5.2.1. It was important to keep the path of high power very short and tight to minimize noise and power losses. The converter switched fairly large currents at high frequencies. Any stray inductance in the power path or ground path would ring with the switching of current and

generate huge voltages. In addition, if proper control of the applications circuit was to be achieved, the switching power could not interfere with the low-power control circuitry. Therefore extra time and energy was devoted to ensuring that the power path was tight and short from the input voltage to ground and the same from output voltage to ground.

5.3.2 Ground Loops

Another important consideration was minimizing the effect of any ground loops. Ground loops occur when there is an imbalance in ground potentials at different point in the ground plane. Differentials in ground voltages can create ground currents that flow from higher ground potentials to lower ones. These ground currents can cause measurement errors in the control circuitry and ringing in the ground plane. In order to minimize ground loop affects, all the input voltage supplies were grounded using a star ground approach. In addition, the use of copper-clad created a very low impedance ground plane [10].

5.3.3 Local Bypassing

The next major consideration was applying adequate local bypassing on all power supply points. The power for the various op-amps and logic blocks was locally bypassed close to the inputs of the ICs. In addition, the power rails were bypassed at their connection to the copper board. The bypassing was important to prevent the switch ring and other switching from affecting the various pieces of the controller circuitry.

5.4 Data & Measurement

5.4.1 Operational Measurements

The next step in completing the proof-of-concept board was to take measurements of various operational aspects of the functional converter. It was important to take measurements that would relate to the theory and ideas presented in section four. The curves here relate to the models presented in the linear delay section of 4.2.

The first curve measured was the frequency versus I_{OUT}. The following curve shown below in figure 5-17 shows the frequency over operation. The frequency curve

shows peaky behavior at around the point where the transition between BCM and DCM occurs. The measured frequency behavior does not show a smooth transition between the two operational modes, suggesting a linear addition of slope delay.
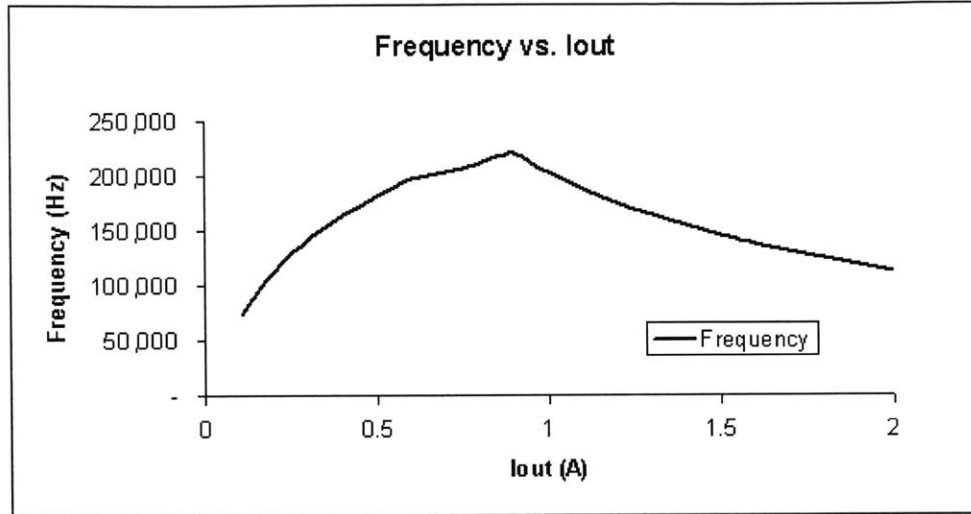

Figure 5-17: Measured frequency versus I_{OUT}.

The I_{swPk} versus V_c and the delay versus V_c will provide a better way of interpreting the frequency data. It will also provide a comparison point for the excel models introduced in section 4.2. Figure 5-18 below shows the measured delay and I_{swPk} versus V_c.
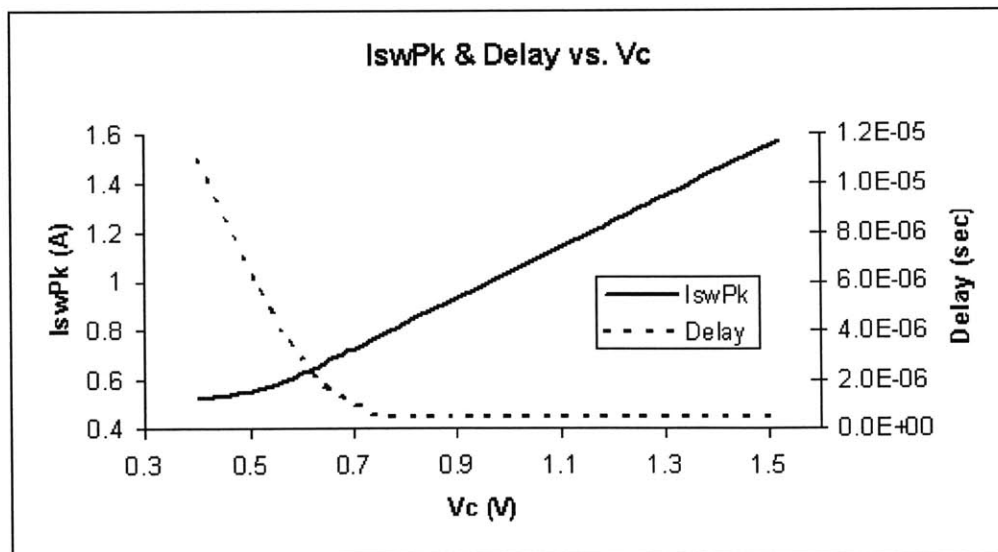

Figure 5-18: Measured I_{swPk} & delay versus V_c.

The two curves show how the two handles on operation were manipulated with Vc in the final implementation. The switch current does not reach its clamp level before delay is added. In addition, the delay is added in a linear slope. The net result is what is seen in the frequency data that is very similar to the results shown from section 4.2.2.

Another important operational curve is how V_c moves with I_{OUT}. The following curve relates back to the DC gain of the system and the transfer function of the modulator. Figure 5-19 shows I_{OUT} versus V_c measured.
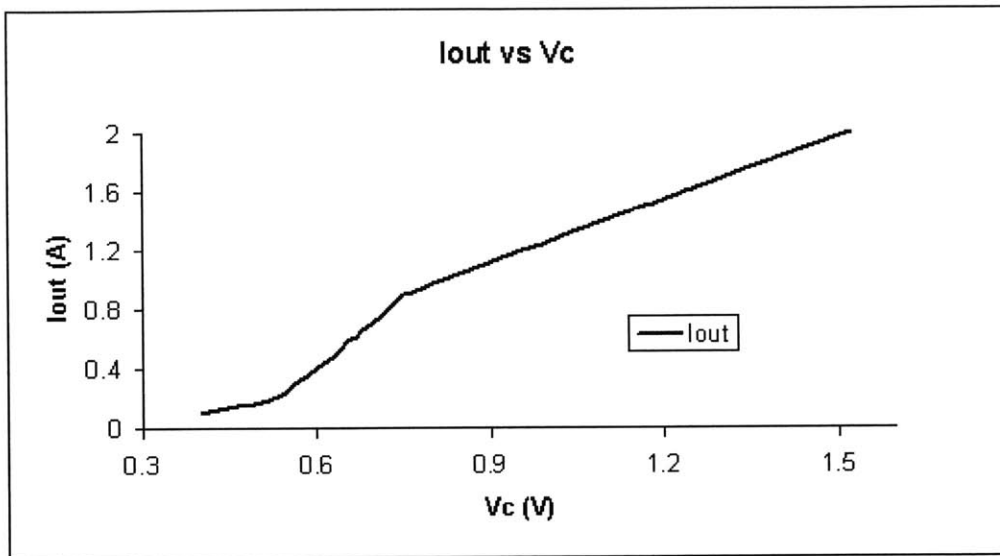

Figure 5-19: Measured data of IOUT versus Vc.

The curve presented above shows a sudden slope change around the value of V_c where the transition between BCM and DCM occurs. The slope change is about a 2x change that corresponds very well with the case introduced in section 4.2.2. The sudden change in slope will reflect in the dynamic behavior of the converter when DC gain is plotted over load current. Another important thing to note is that the converter frequency jittered when the load current placed the converter right at the transition.

5.4.2 Dynamic Characteristics

Dynamic characteristics were the next important aspect of the converter's operation. The dynamic curves showed more about how the converter operated with load changes and also how stable the converter was. In addition, the dynamics should correspond to the operational measurements of the previous section. Before continuing

the compensation network used should be shown. The compensation network was determined using an iterative approach that examined both the bode plots of the loop and the transient response of the system. The two aspects were used to settle on the following compensation scheme at the output of the gm-amp. Figure 5-20 below shows the chosen compensation scheme. Also, the amount of output capacitance on the final design was two 680uF capacitors in parallel.
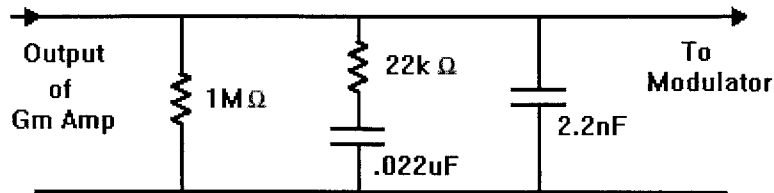

Figure 5-20: Final compensation scheme.

5.4.2.1 Bode Plots of the Loop Response

The first measured piece of the dynamic picture of the converter was the bode plots. Bode measurement were made using the Venable, a loop gain measurement system. The Venable injects signals into the converter and measures input to output changes in the signal to determine loop characteristics. The signal was injected using a small resistance inserted in the top of the divider to the gm-amp. The bode plots were taken at various load currents to ensure that the converter had sufficient phase margin once the compensation network was determined. The first bode plot was taken at light load of 0.1A and an input voltage of 48V. The bode plot is shown below in figure 5-21 with a phase margin of $55.2°$ at crossover and a bandwidth of 269Hz.
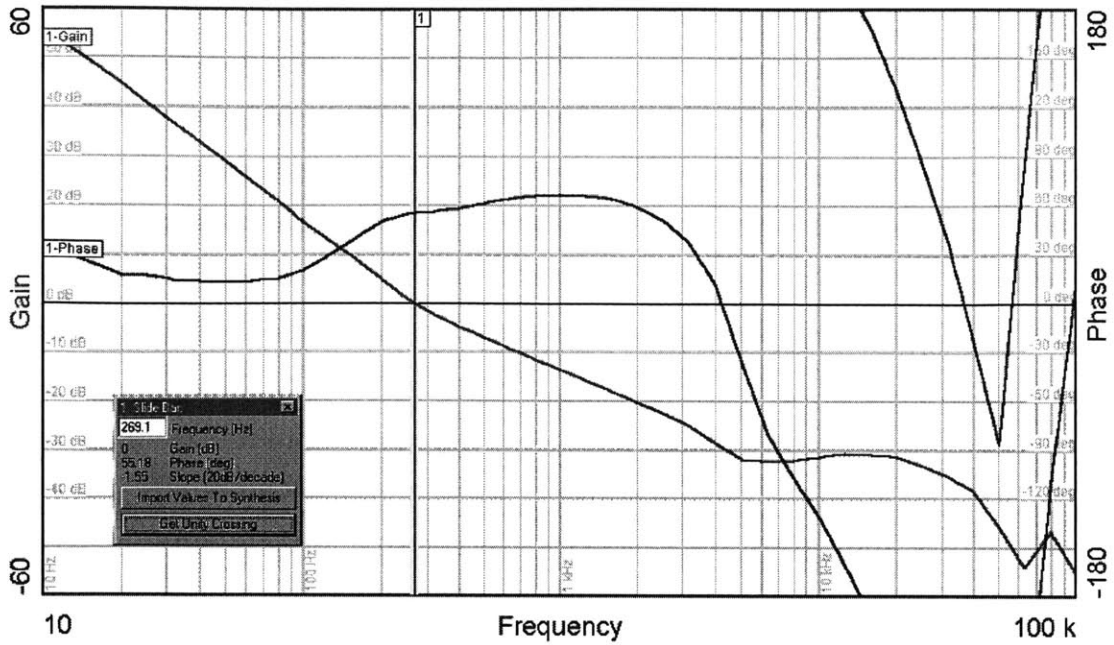
Figure 5-21: Bode plot of the loop response at 48Vin and 0.1A of load current.

The next bode plot is at 1A and 48V at the input. The following loop response shows a bandwidth of 829.4 kHz with a phase margin of 59.4°. The loop response is shown in figure 5-22.
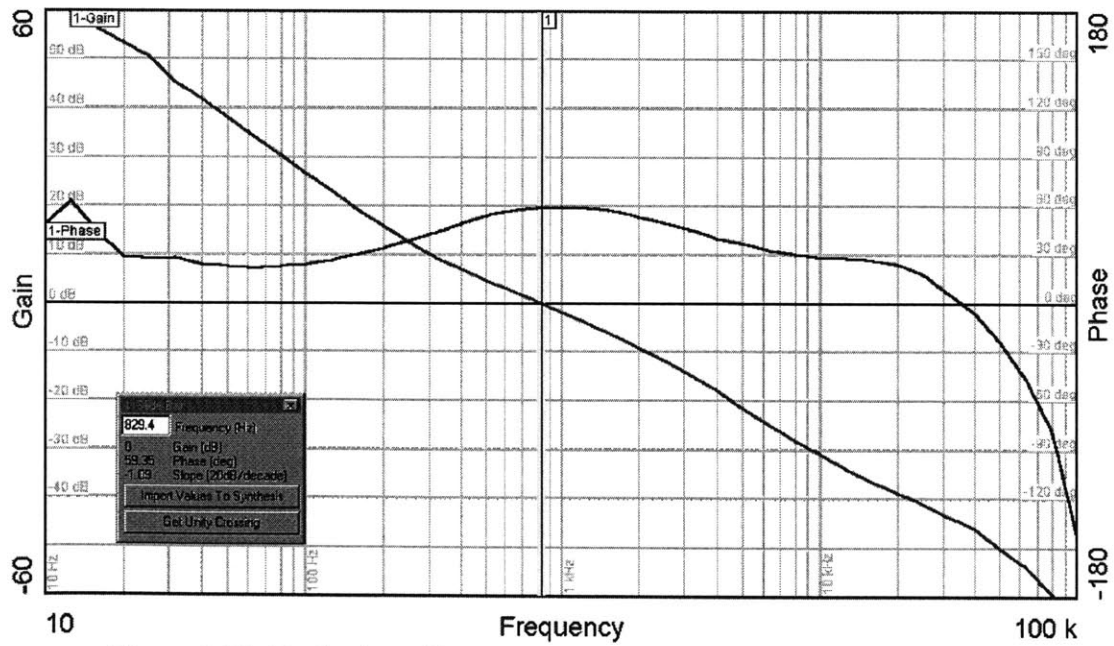

Figure 5-22: Bode plot of loop response at 1A of load current and 48Vin.

The next bode plot was taken at 2A of load current with an input voltage of 48V. Figure 5-23 shows the plot with a bandwidth of 692 Hz and a phase margin of 57.3°.
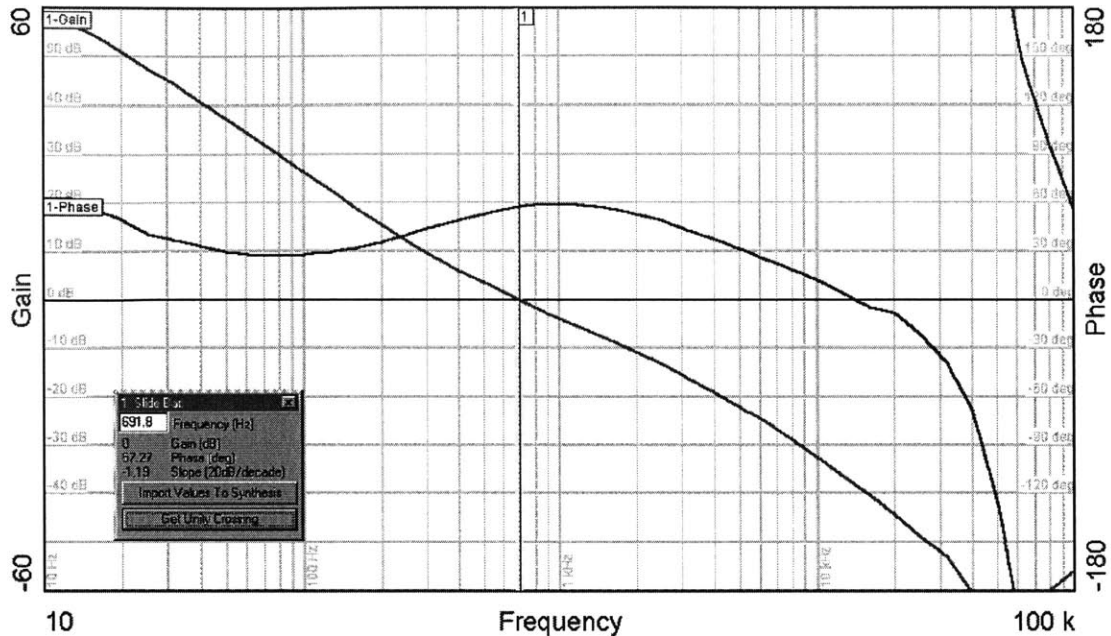

Figure 5-23: Bode plot of loop response at 2A of output current and 48Vin.

5.4.2.2 Output Impedance of the Modulator

The output impedance of the converter was measured next using the Venable. The output impedance was measured by measuring the input to output characteristics of the modulator. The modulator showed a first order response with a one pole role off that corresponded nicely with the first-order model introduced in section 4.3.2. The output pole that causes the first order role off is a function of the output impedance and the output capacitance. Therefore the output impedance of the converter across load can be determined if the output capacitance and the pole location is known. Figure 5-24 shows the extracted output impedance data over load for the built converter with two 680uF output capacitors.
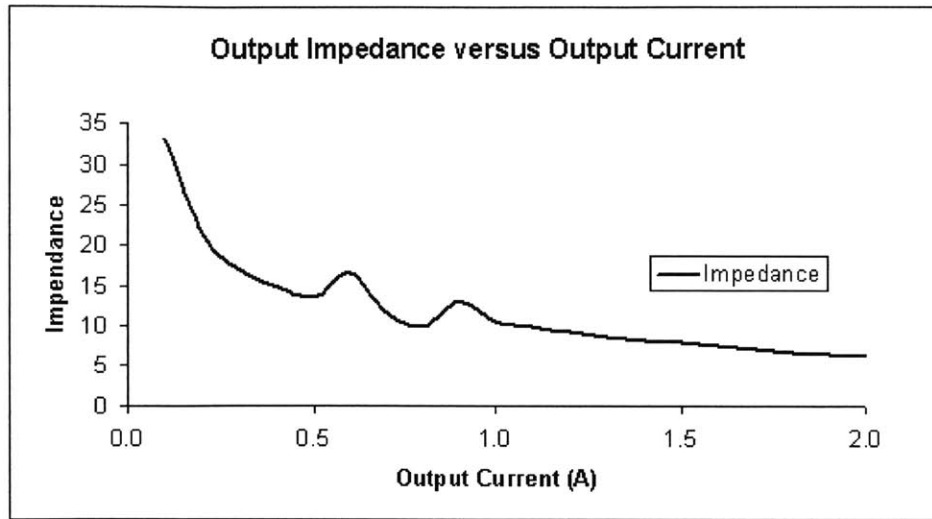
Output Impedance versus Output Current

Figure 5-24: Measured output impedance of the modulator versus output current.

The peaking in the impedance curve is a reflection of the frequency behavior of the system. The next step was to determine a good model for the impedance over load measured. The model created used the circuit model generated in section 4.3.2. Figure 5-25 shows the model plotted against the actual measured output impedance. The model predicts the output impedance very closely down to about an amp. At an amp the measured output impedance curve rises and dips as the converter enters DCM. The model does, however, predict the output impedance below an amp. The model that was introduced in section 4.3.2 was only valid in BCM because it assumed that there was no delay in the frequency term. When the converter enters DCM, delay is also introduced into the frequency term requiring a new model for DCM with the specific type of delay added.
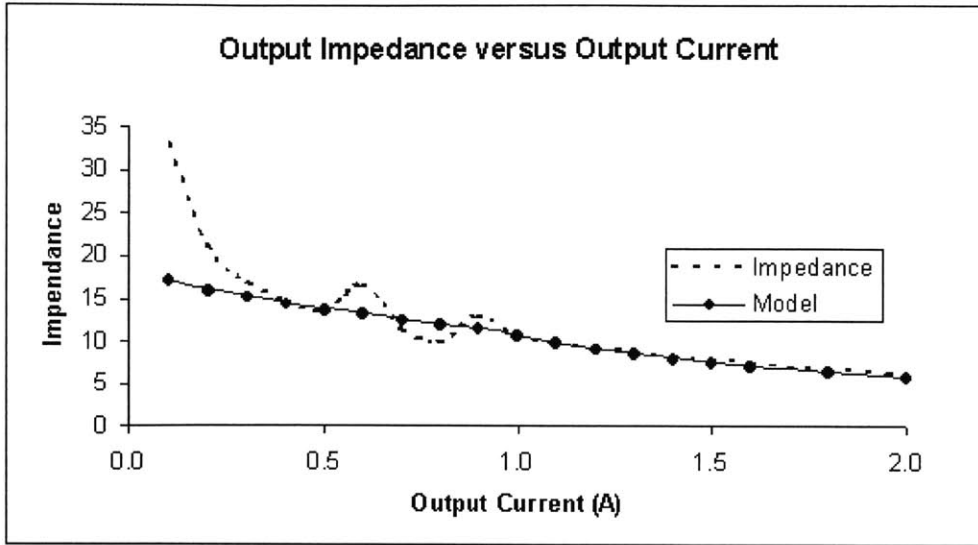
Figure 5-25: Output impedance measured with BCM impedance model.

5.4.2.3 DC Gain of the Modulator

The next interesting characteristic of the dynamic performance was the DC gain of the modulator. The DC gain was measured using the Venable and recorded across the load current range. Figure 5-26 shows the DC gain measured at 48Vin for the converter across load range.
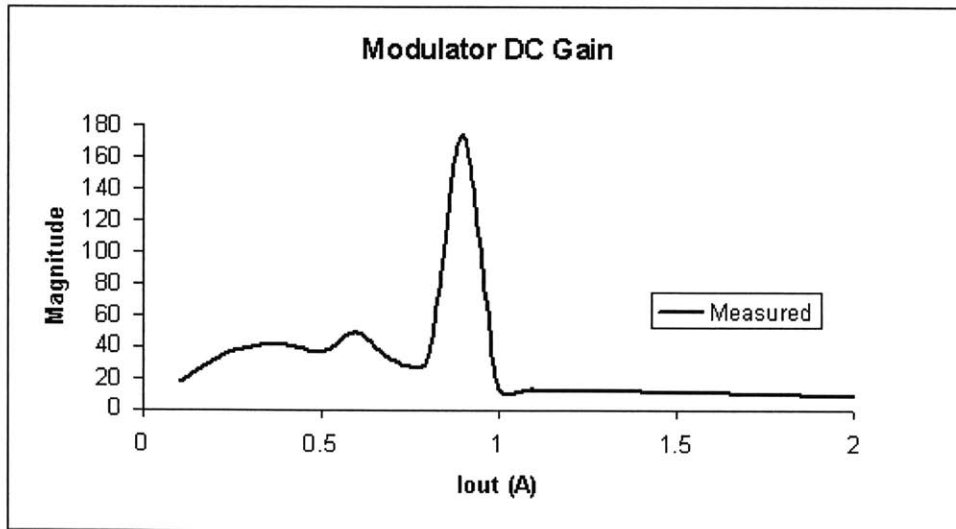

Figure 5-26: Modulator DC gain measured at 48Vin

The DC gain shows a huge spike in magnitude around the transition point between BCM and DCM operation. The spike can result in instabilities in the loop

response if it suddenly reduces phase margin of the total system. The overall impact of the spike was minimized with the compensation scheme used and the fact that the system showed enough phase margin at crossover.

The next step was to determine if the models introduced in 4.3.2 accurately modeled the DC gain characteristics. Figure 5-27 below shows both the measured DC gain with the model predicted by the circuit model in section 4.3.2. The graph shows that the model works at the high current levels but does not follow the measured curve when the converter transitions between BCM and DCM. The model introduced in 4.3.2 only worked for BCM operation.
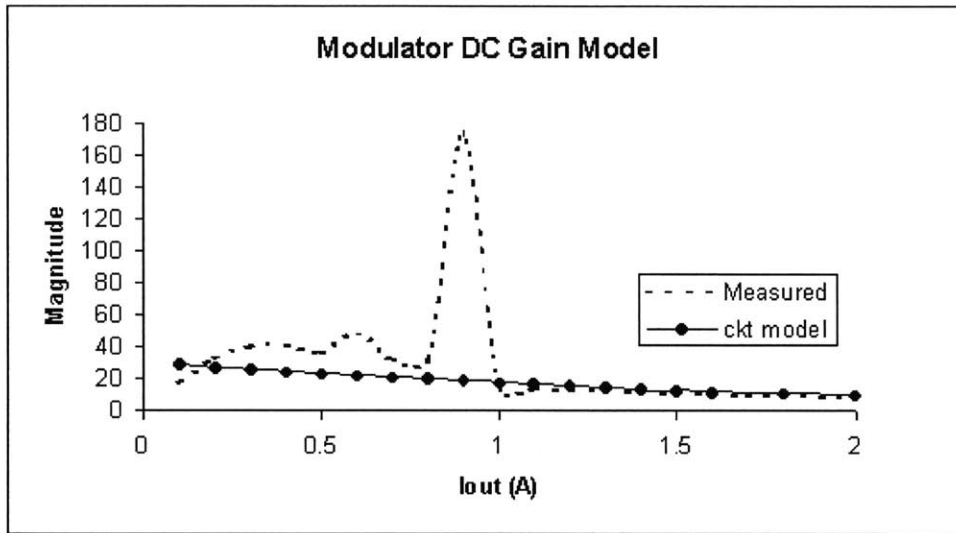
Figure 5-27: Modulator DC gain with the predicted circuit model.

Another way to model the DC gain of the system would be to use the slope information provided by the I_{OUT} versus V_c curves measured along with the measured output impedance. The slope of the I_{OUT} versus V_c curve multiplied by the output impedance results in the DC gain of the system. Figure 5-28 below shows this method and its result against the measured DC gain.
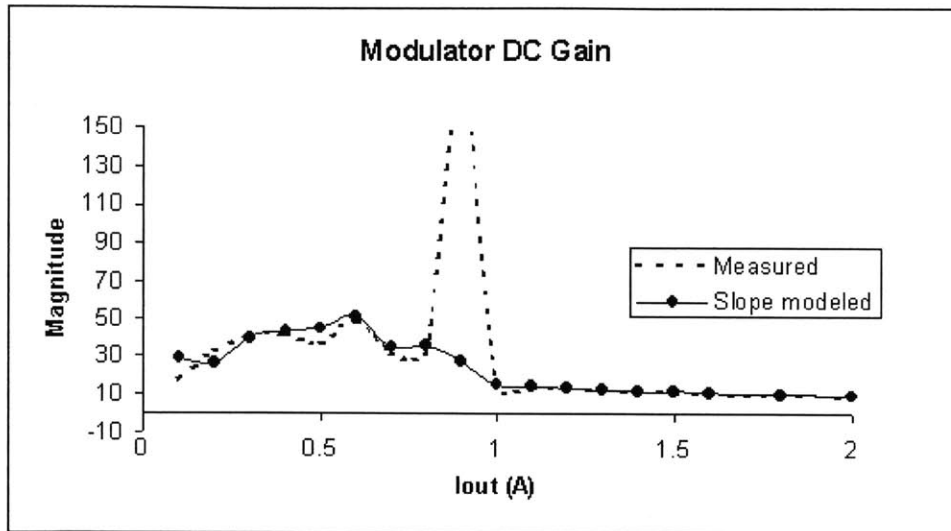
Figure 5-28: Modulator DC gain with slope model.

The slope model shown in the graph above predicts the DC gain fairly closely with the output impedance. It does not predict the sharp spike in DC gain that occurs at the transition. The slope used was the average slope and not the actual slope of the V_c versus I_{OUT} curve. In any case, it provides a good model of the DC gain measured across both BCM and DCM operation. In addition, it supports the importance of the I_{OUT} versus V_c curve.

5.4.2.4 Transient Response

The final measurement of dynamic performance was the transient response. The transient response was taken using a half amp step in current on the output and measuring the output voltage response. The transient response is shown in the photo below in figure 5-29. The top curve is the output voltage on a 100mV/div scale, while the bottom curve is the step in output current with a 0.5A/div scale.
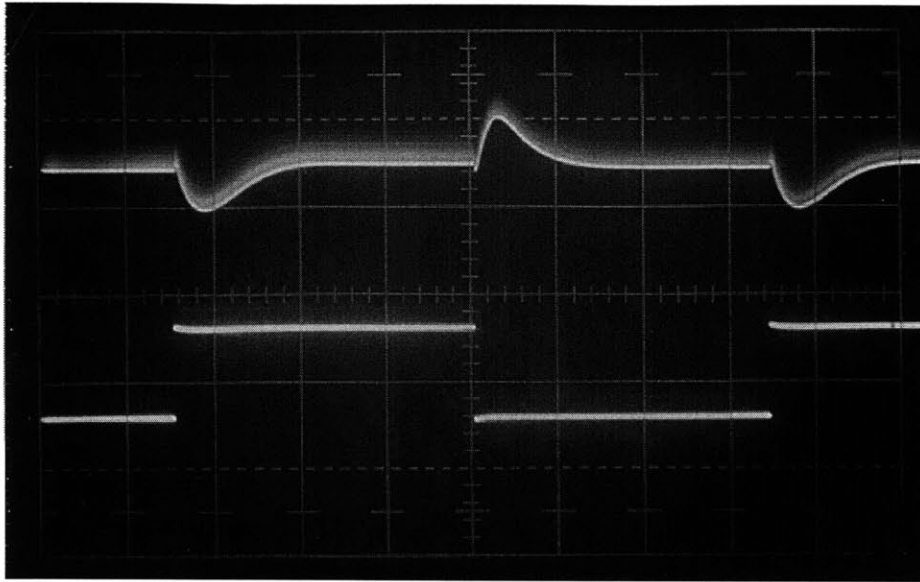
98

Figure 5-29: Output transient response to a 0.5A step from 0.5A to 1A.

The transient response shows a first-order response on both step edges. The response data fits with the phase margin measured data that was above 45°. In addition, the large output capacitance prevents the output voltage from falling too far out of regulation at the edge of the step.

5.4.2.4 Dynamic Characteristics Conclusion

In conclusion, the dynamic performance measurements look good. The various measurements show peaking and stability issues introduced at the transition between BCM and DCM operation. The DC gain picture along with the output impedance does not show smooth behavior, but peaky characteristics in the DCM region. The models introduced do, however, provide a good representation for what was measured and provide clues on how to improve dynamic behavior using both circuit models and dc behavior. The models support the idea that a quadratic form of slope delay may improve both the frequency behavior along with DC gain as shown in section 4.3.2.

5.4.3 Overall Performance Measurements

The final measurements measured overall efficiency of the board along with output regulation over line and load.

5.4.3.1 Efficiency

Efficiency measurements were taken over both load and line to get a sense of the overall efficiency of the flyback solution. Three power supplies powered the proof-of-concept board. One supply powered the application circuit which operated from 36 to 72V in. The other two supplies powered the various logic blocks, op-amps, comparators, and switch driver at 10V and 5V. The total efficiency of the system across both line and load including all three supplies is presented below in figure 5-30.
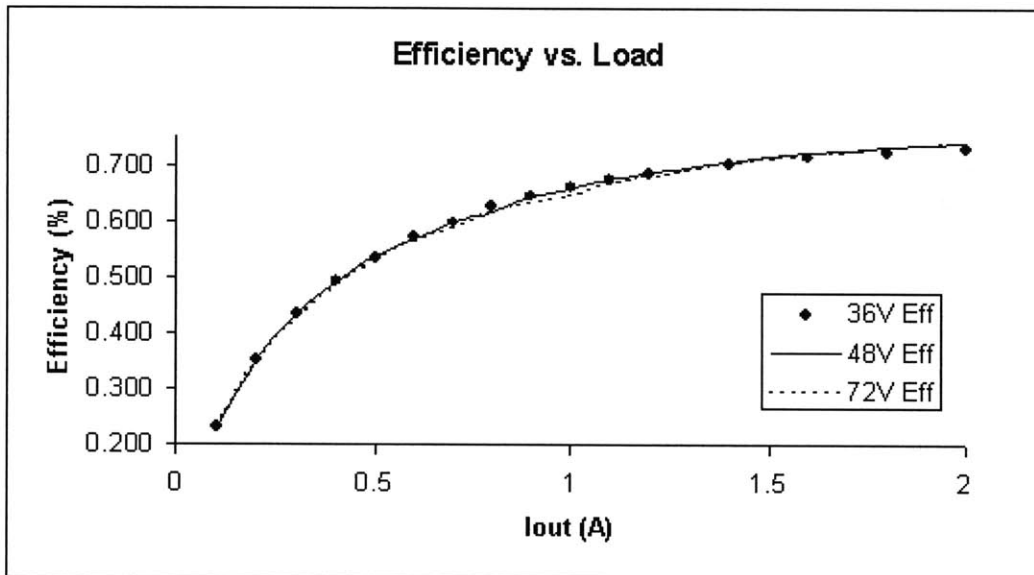
Figure 5-30: Total efficiency over line and load.

The efficiency curve falls off steeply at light loads. The efficiency curve includes all the quiescent currents for each of the op-amps, comparators, and logic blocks. Another curve that provides a good comparison is the efficiency of the converter if only the application circuit power supply is used. Figure 5-31 shows the efficiency over line and load for just the 36V to 72V power supply.
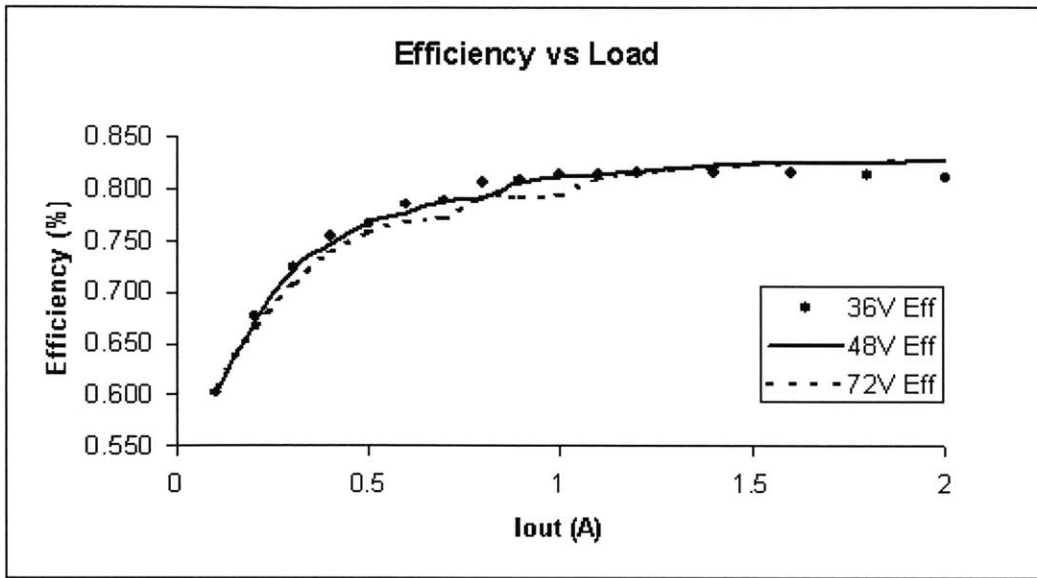
Figure 5-31: Efficiency over line and load of using only the 36-72V power supply.

The efficiency curve presented above shows the application circuit efficiency without the power lost to the control circuitry and the MOSFET driver. It provides a nice comparison to what is lost to the application circuit when using a flyback topology versus what additionally is lost to the controller.

5.4.3.2 Output Regulation

The final performance measurement taken was regulation over both line and load. Figure 5-32 shows the output regulation data at 5Vout.

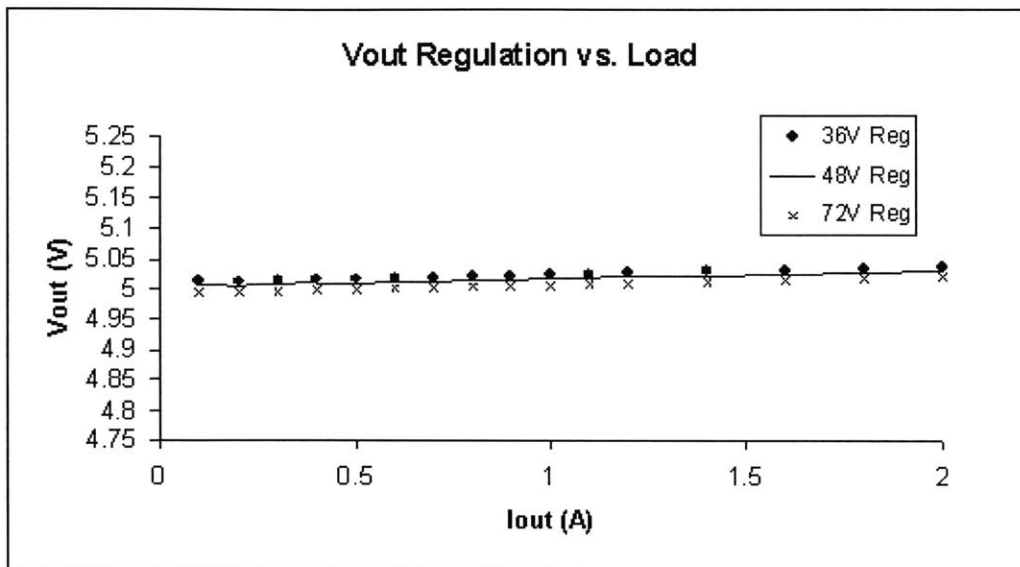Figure 5-32: Output voltage regulation measured over both line and load.

The output regulation data over both line and load was below 1%! Three curves are shown in the graph representing different input voltages measured across the load range from .1A to 2A.

6 Conclusion

The thesis focused on the marriage of magnetic-flux-sensing feedback and boundary-mode operation in a flyback converter to create a simple, small, low-cost, isolated, and tightly regulated power supply. The proof-of-concept board along with the collected data achieved the goals initially outlined for the thesis. The following section details each of the goals and expands on how each goal was met.

6.1 Simple, Small and Low-Cost

The built flyback converter solution was aimed at achieving a simple and small solution to the problem of creating an isolated power supply. The schematics and data shown in section five show the simplicity of the circuit level solution. Many of the discrete pieces serve simple op-amp functions such as addition and gain. Many of the blocks can be easily integrated into simple transistor circuits because of this lack in complexity. Even the more complicated pieces like the track and hold circuit were built with the help of a few 2N3904s and 2N3906s.

The power of the simplicity in the circuit design is evident from the block-level diagrams presented in section 5.1. In addition, the overall data suggest that the simple converter solution works quite effectively. The overall size of the finished solution is quite large because of the use of off-the-shelf op-amps and logic circuits. The board solution serves as a proof-of-concept solution that allows easy, quick modifications to any part of the converter for testing. The IC solution will take the circuits developed in the board design and integrate them all into a small six-pin SOT-23 solution. Figure 6-1 provides a good comparison of the board-level solution built and the SOT-23 solution.

103

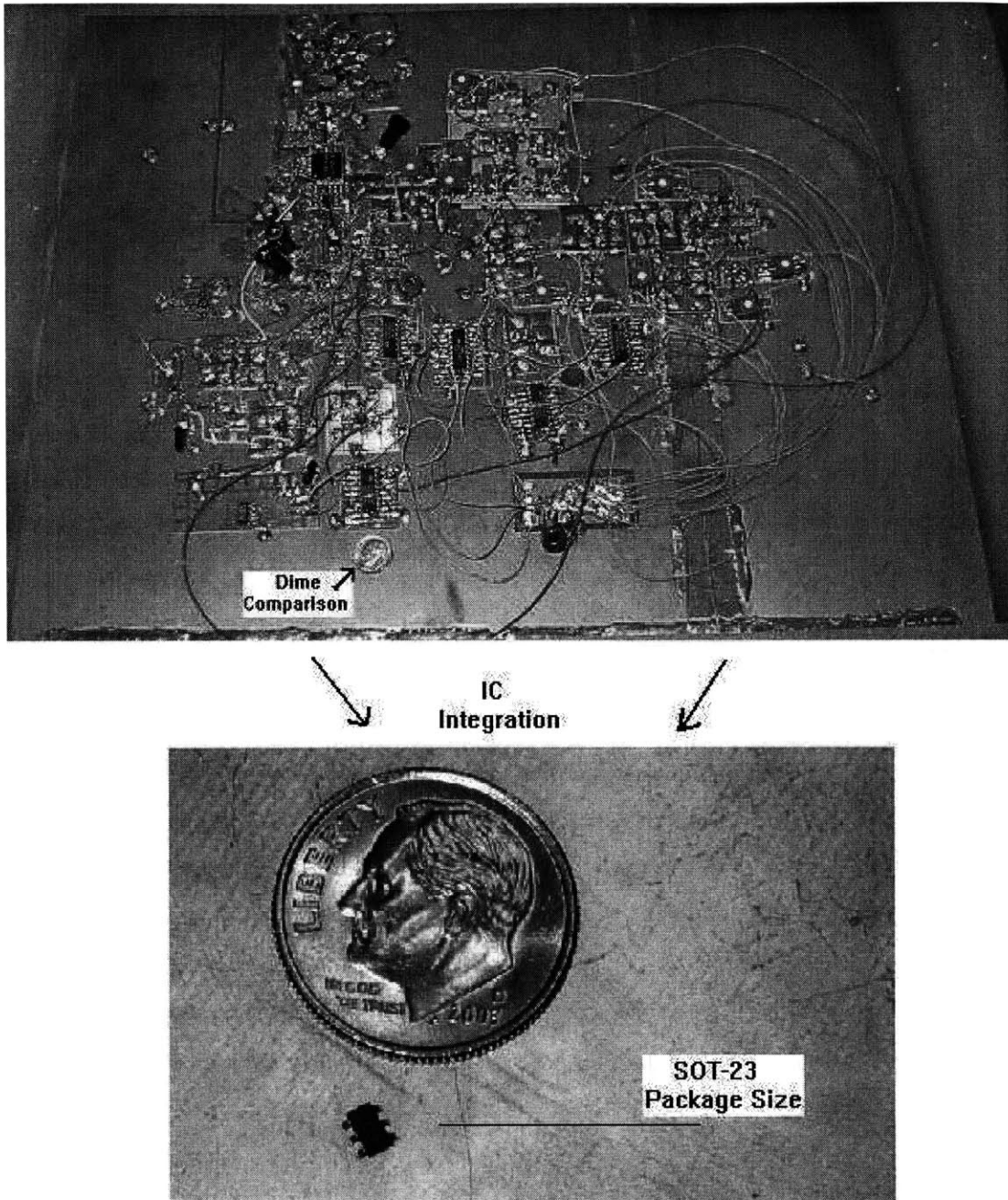Figure 6-1: Proof-of-concept solution and its eventual SOT-23 IC form

In addition to small IC integration, the isolated power supply will significantly simplify and reduce the total application circuit. A typical opto-isolated flyback solution is shown below in figure 6-2. The flyback solution uses the LT3803 controller with an opto-coupler. The circuit requires a secondary circuit to drive the opto-coupler.
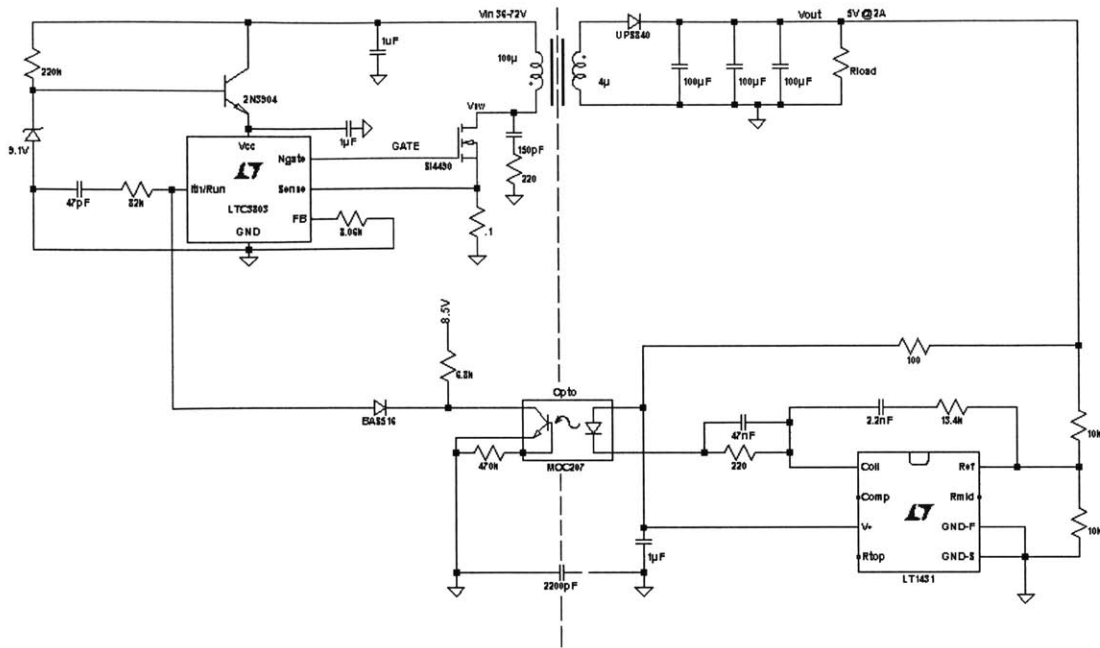
Figure 6-2: Opto-isolated flyback implementation using the LTC3803.

The opto-isolated solution shown above is a telecom solution that converts input voltages from 36 to 72V and regulates to 5V at 2A. The opto-isolated solution requires secondary circuitry to drive the opto-coupler and close the feedback loop. On the other hand, the typical isolated magnetic-flux sensing solution is shown below in figure 6-3.

Figure 6-3: Typical magnetic-flux sensing flyback solution using BCM operation.

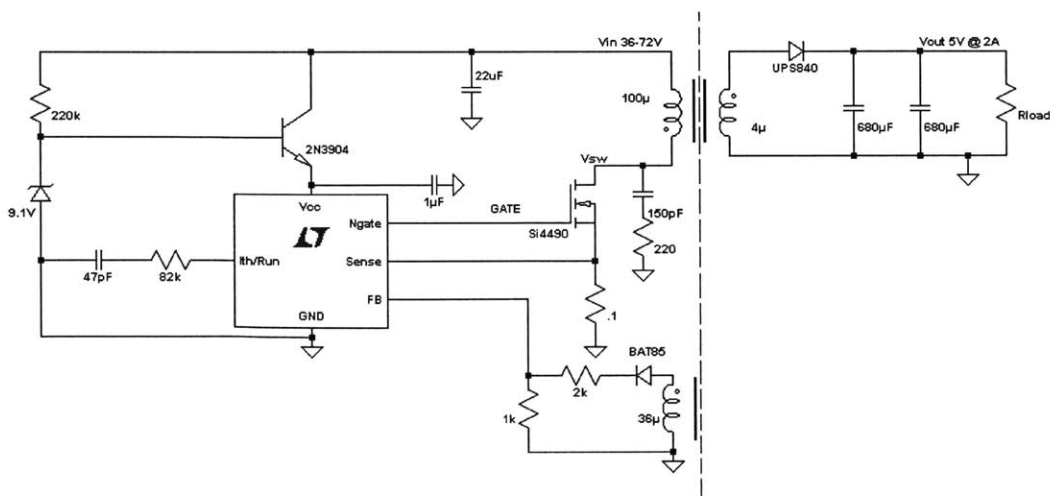The two application solutions provide the same function for telecom taking 36-72V in and converting it down to 5V at 2A. The two solutions can be compared in three distinct ways of cost, complexity, and board space. For example, the two solutions are shown with the typical arrangement of external components. The magnetic-flux sensing solution does not use an opto-coupler or require circuitry to drive the opto. Other than that, the two flyback solutions are the same. The transformer in the magnetic-flux sensing solution does need a third winding, but the relative cost of that additional winding is small in comparison to the other components. The opto-coupled solution requires extra cost related to the opto-coupler and its driver circuitry.

In terms of complexity, the application circuit for the opto-coupled solution requires more external components and must regulate with two additional components in the feedback path. The dynamics through the driver and the opto-coupler must be understood and integrated with the rest of the flyback dynamics. The dynamic performance of the opto-coupled solution may allow better dynamic performance because it does not have the additional sampling delay introduced by magnetic flux sensing feedback. The sampling delay imposes a limit on achievable bandwidth that can be a fourth of the sampling frequency lower than that of the opto-coupled solution.

The third important point of comparison is the relative board space required for both solutions. If we ignore the main controller IC, the opto-coupled flyback solution will require more board space to lay out the additional opto-coupler and support circuitry. The extra winding in the magnetic-flux sensing case can be integrated into the transformer without taking up that much more space. In addition to more components, the opto-coupled solution requires even more space. The requirement for additional space comes from the fact that the primary and secondary side circuitry must be separated both electrically and physically. The dotted line in the two figures represents the physical separation. The opto-isolated solution requires both the transformer and the opto-coupler to reside along the boundary between the two sides. This requirement places a restriction on board layout and does not allow a tighter layout.

6.2 Isolated and Tight Output Regulation

In addition to achieving the goals of simple, small, and low cost, the proof-of-concept board developed an isolated and tight regulated supply. The data introduced in figure 5.32 showed that the magnetic-flux sensing solution achieved less than 1% regulation across both line and load! In addition, the output regulation achieved was with the output physically and electrically isolated.

The proof-of-concept board achieved all the goals initially outlined for the project. In addition, it created an excellent medium for testing out ideas related to light load operation in a quick, efficient manner. The board and the solution described provide and excellent starting point for integration into integrated circuit form. The board also will allow any future design ideas to be tested before being integrated into an IC solution.

6.3 Acknowledgements

First & foremost, I would like to thank the Linear Technology Corporation and its staff for giving me the opportunity to apply the knowledge I have learned over my four years at the Massachusetts Institute of Technology. My experience at Linear has given me a unique opportunity to connect the theory from a variety of classes with the practical design of a power converter. In addition, the staff at Linear Technology has provided a great deal of insight and knowledge that has made it possible for me to complete this thesis.

I would also like to thank my supervisor Tony Bonte for spending considerable time and energy teaching me the fundamentals of engineering and power electronics. In addition, I would like to thank Ron Roscoe from MIT for introducing me to analog circuit design and then encouraging me to look closer at analog circuit design as a rewarding career.

Finally, I would like to thank my parents for providing their unending support through out my life. Their constant encouragement and advice has allowed me to achieve great success academically and in every other aspect of my life.

7 References

[1] Bonte, Anthony, *Conversations on flyback converters*, Milpitas, CA: LTC Design
Engineer, 2003.

[2] Bonte, Anthony and Vinsant Ron, "Offline Switching Regulators Achieve ±1%
Regulation in a Flux-Sensed Converter." Conference. Seventh Annual Applied
Power Electronics Conference, IEEE-7803-0485-392, p 513-516, 1992.

[3] Erickson, Robert and Maksimovic, Dragan, Fundamentals of Power Electronics,
Norwell, MA: Kluwer Academic Publishers, 2001.

[4] Gould, Markey, Roberge, Trumper. Control Systems. Cambridge: Massachusetts
Institute of Technology, 1997. 131.

[5] Huffman, Brian. "Efficiency and Power Characteristics of Switching Regulator
Circuits," Linear Technology Corporation, Application Note 46.

[6] J. Kassakian, M. Schlecht, and G. Verghese, Principles of Power Electronics,
Reading, MA: Addison-Wesley, 1991.

[7] Mammano, Robert, "Isolating the Control Loop." Unitrode Design Seminar, Topic 2,
1990.

[8] Matthews, Kurk, *Conversations on determining transformer losses*, Milpitas, CA:
LTC Applications Engineer, 2003.

[9] Nelson, C., "LT1070 Design Manual," Linear Technology Corporation, Application
Note 19.

[10] Nelson, C., "LT1074/LT1076 Design Manual," Linear Technology Corporation, Application Note 44.

[11] Shannon, John, Conversations on BCM flyback operation, Milpitas, CA: LTC Application Engineer, 2003.

[12] Wu, Albert, *Conversations on dealing with light load operation*, Milpitas, CA: LTC Design Engineer, 2003.

[13] Jieli Li, T. Abdallah, and C. R. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms", in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting*, 2001, pp.2203-2210.

[14] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters", *8th IEEE Workshop on Computers in Power Electronics*, Compel 2002.

[15] D. J. Perreault and G. Verghese, "Time-varying effects in models for current-mode control", *Power Electronics Specialists Conference*, 1995.