Ultra-Thin Moisture Barrier Coatings for Passive Components

by

Robert A. Jensen

B.A., B.E. Dartmouth College (2002)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

Massachusetts Institute of Technology

June 2004

Author_____

Department of Electrical Engineering and Computer Science
May 7, 2004

Certified by_____

Prof. David J. Perreault
Carl Richard Soderberg Assistant Professor of Power Engineering
Thesis Supervisor

Certified by_____

Prof. Charles R. Sullivan
Associate Professor, Dartmouth College
Thesis Supervisor

Accepted by_____

Arthur C. Smith
Chairman, Department Committee on Graduate Students

Ultra-Thin Moisture Barrier Coatings for Passive Components

by

Robert A. Jensen

Submitted to the Department of Electrical Engineering and Computer Science
on May 7, 2004, in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering and Computer Science

Abstract

Polymer Multi-Layer (PML) capacitors have demonstrated excellent performance for numerous power electronics applications, particularly where high temperature stability is required. These capacitors are sensitive to high humidity, and if they are not protected from moisture exposure their performance degrades rapidly due to electrochemical corrosion. Conventional protective coatings, such as epoxies and polyurethanes, are extremely thick - usually over 1 mm. Previous work has shown that a thick coating leads to a large equivalent series inductance (ESL) of the capacitor, and negatively affects the capacitor performance. An ultra-thin moisture barrier coating is desirable to improve both electrical performance and capacitance density. This thesis focuses on developing coatings which are thinner than 200 μm and which adequately protect PML capacitors from humidity. Novel moisture barrier designs have been fabricated and tested.

Thesis Supervisor: Prof. David J. Perreault
Title: Carl Richard Soderberg Assistant Professor of Power Engineering

Thesis Supervisor: Prof. Charles R. Sullivan
Title: Associate Professor, Dartmouth College

Acknowledgements

I would first like to thank Rubycon Corporation for their generosity in making this work possible. Many thanks also to my advisors David Perreault at MIT, and Charles Sullivan of Dartmouth for giving me the opportunity to work on such an interesting problem, and for keeping me busy with lots of ideas.

I would particularly like to thank the students, faculty, and staff of the LEES Laboratory.

Thanks also to Kurt Broderick for countless hours of help in EML. I would also like to thank John Kymissis and Annie Wang of Prof. Akinwande's group for helping me to use their parylene deposition system.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Polymer Multi-Layer (PML) capacitors have excellent electrical performance characteristics across a broad frequency range. The combination of low equivalent series resistance (ESR), high temperature capability, power density, and small size make PML capacitors an excellent choice for many power electronics applications [1, 2, 3]. Moisture resistance is a significant issue, and can be obtained through proper packaging of the capacitor. Traditional methods include application of a thick coating of epoxy resin or encapsulation in a plastic case [3]. These methods are disadvantageous because they can significantly increase packaged capacitor size, thus preventing miniaturization [4]. Furthermore, as described in [5] and illustrated in Figure 1.1, thick coating layers can greatly increase the equivalent series inductance of the packaged capacitor, thereby reducing high-frequency electrical performance.

Previous work has demonstrated that thick layers of packaging can lead to a large parasitic series inductance [4]. Fig. 1.2 demonstrates the effect on capacitor voltage when a current step is applied. For the capacitor with a thick coating, there is a large voltage spike due to the parasitic inductance. When this coating is removed, the capacitor lies closer to the ground plane, thus decreasing parasitic inductance. Fig. 1.2 shows that this voltage spike is eliminated simply by removing the coating on the capacitor.

Improved packaging methods for PML capacitors that overcome these limitations are therefore desirable [5]. This thesis presents an investigation into new packaging methods for polymer multi-layer (PML) capacitors that overcome the limitations of existing approaches. The study focuses on new packaging methods that provide the necessary level of moisture re-

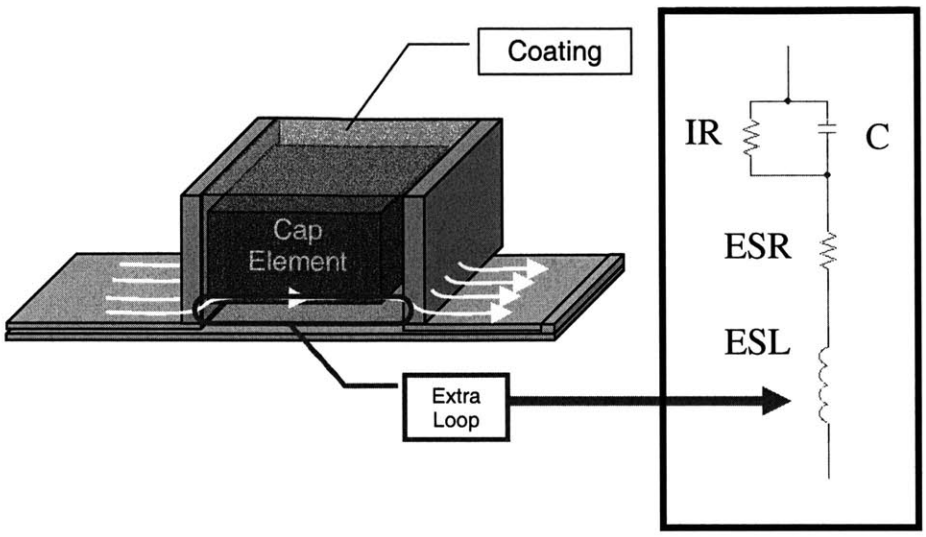

Figure 1.1: Illustration of the current loop area imposed by the packaging layer of a capacitor. The additional inductance associated with this current loop area can have a significant impact on the high-frequency performance of the capacitor.

sistance without incurring large size penalties in packaged devices. For a more detailed background on the science of environmental protection and packaging, please see Ch. 2.

A primary specification will be to use packaging techniques that do not increase the size of the capacitor over its unpackaged size by more than 200 μm in any dimension. To maintain the high-temperature advantages of PML capacitors, packaging methods also must be compatible with operating temperatures of up to 125 °C. Emphasis has also been placed on methods that enhance electrical performance, have the potential for good manufacturability at low cost, and have good reliability.

In addition to exploring, developing, and experimentally demonstrating these new methods, emphasis is placed on quantitative evaluation, and on establishing practical recommendations for their application and further development [4].

To achieve coating thicknesses under 200 μm, and to allow the coating process to be scalable down to even smaller thicknesses, this project focuses on thin film deposition techniques. These include fabrication technologies that have been optimized for the IC industry such

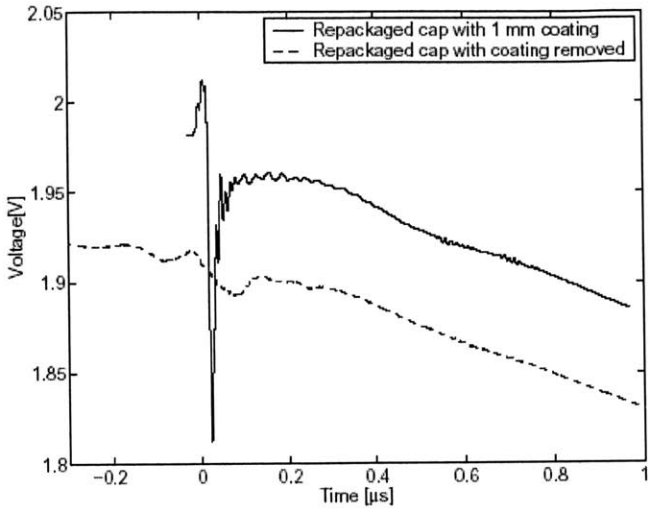

Figure 1.2: Current step response of SMT capacitor. Voltage spike caused by parasitic inductance of packaging. Reprinted from [4] with permission of author.

as sputtering, evaporation, and photolithography. These methods are particularly effective for depositing high quality thin films and patterning them. These techniques are typically used for planar substrates. This presents a practical problem for packaging, as a surface mount capacitor is a three dimensional device with sharp edges. A more detailed discussion of these considerations is presented in Ch. 4.

A key element of this investigation will be the evaluation of coated capacitors. One common method used in industry is to place the capacitors in an environmental chamber. The capacitance and ESR of the capacitors are measured at regular intervals. This method has been used to evaluate coating performance, and is discussed in Ch. 5.

This project focuses on four key methods of encapsulating capacitors.

1. Single-layer Coating
2. Labyrinth Seal
3. Half-Labyrinth

4. buffered-ceramic

The single-layer coating method is to apply a single coating of one material. The advantage of this approach is that it is very simple, and avoids time consuming processing steps. The disadvantage is that it is hard to find a material which is appropriate. The material would need to be extremely moisture resistant, have high electrical resistivity (to avoid shorting out the capacitor), and to have mechanical properties that are well matched to the capacitor itself. For example, the material cannot be too brittle for the coating will crack and break when exposed to high temperature.

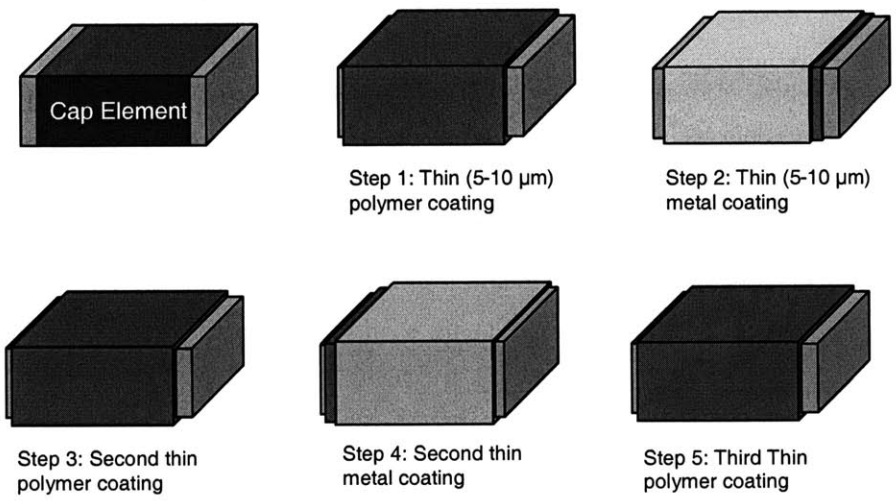

Figure 1.3: Fabrication steps for a capacitor package implemented with the "Labyrinth Seal Method".

The second packaging approach is called the "Labyrinth Seal Method". This approach, proposed by C.R. Sullivan [6] and illustrated in Fig. 1.3, combines multiple layers of thin polymer film (or other insulating coatings) with thin metal coating layers. As illustrated in Fig. 1.4, this approach may provide a large improvement in humidity resistance by forcing moisture penetration through a long and narrow path [5]. Potential advantages of this approach include relaxed material requirements, inexpensive processes that are compatible with existing manufacturing steps, and reduction of both high-frequency inductance and electromagnetic interference due to the conductive shield formed by the package. The

third packaging approach is an extension of the labyrinth seal method which is simpler to fabricate, yet leads to less moisture resistance.

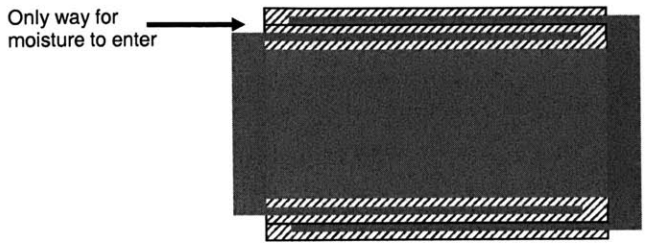

Figure 1.4: Cross Section of a capacitor package with a "Labyrinth Seal".

The fourth coating method is to use a thin ceramic material as a coating. Layers of polymer are used to protect the ceramic material from cracking due to mechanical stresses. This method will be called the "buffered-ceramic" method.

A full description of these methods is presented in Ch. 3. These coatings have been applied to capacitors and tested using and tested in an environmental chamber, as discussed in Ch. 5. Results of this testing are discussed in Ch. 6.

Environmental chamber testing indicates that both the labyrinth and buffered-ceramic methods offer superior moisture protection over organic layers. The buffered-ceramic method is particularly attractive because it is simple to deposit, and can provide as little or as much moisture protection as needed. We have succeeded in achieving greatly improved moisture protection with barrier coating as thin as 30 μm. More work is needed to verify that this protection is adequate to prevent loss of capacitance for 500 hours with 25 V applied. Conclusions from this investigation and suggestions for future work are presented in Ch. 7.

Chapter 2

Background

This purpose of this chapter is to give a background and motivation for the need to have capacitor coatings which are both thin and highly moisture resistant. Section 2.1 presents a basic background on PML capacitors, and discusses how packaging volume limits capacitance density. Section 2.2 details the fundamental physics of moisture ingress into packages and the resulting problem of corrosion.

2.1 Polymer Multi-Layer Capacitors

This thesis focuses on the packaging of surface mount PML capacitors. These capacitors have a number of excellent qualities, particularly with acrylate dielectrics.

1. High Temperature Performance (up to 125 °C)
2. High Capacitance Density
3. Low ESR
4. Non-shorting failure mode

State of the art PML capacitors are made by stacking thousands of layers of aluminum electrodes and dielectric. These newest capacitors are advantageous over conventional PML capacitors because of the use of an acrylate dielectric. The deposition process for this

material creates sub-micron films that are pinhole free and can be deposited very rapidly. This dielectric also has low loss and is stable at high temperatures [2, 3]. Conventional PML capacitors are made using a polypropylene dielectric which is only useful at thickness greater than a micron. This new polyacrylate technology is attractive to the circuit designer particularly for its high capacitance density, low ESR, and stable performance at elevated temperatures.

The performance of these capacitors can become degraded rapidly in a high humidity environment. As moisture enters the capacitor, corrosion of the Al electrodes occurs if the capacitor has a voltage applied. This corrosion results in a dramatic drop in capacitance, as the aluminum electrodes are converted to Al_2O_3 [7]. This problem is particularly pronounced if the dielectric material is hydrophilic, because water will readily adsorb on the dielectric surface, allowing the moisture to diffuse into the capacitor. Unfortunately, this particular polyacrylate dielectric is hydrophilic. It is believed that the amount of moisture ingress into the capacitor could be dramatically reduced if the dielectric were hydrophobic. This is not a trivial problem, as dielectrics with high dielectric constant are polar and tend to be hydroscopic [8]. Altering the chemistry of the dielectric material is beyond the scope of this project. A more detailed discussion of these complex capacitor aging problems can be found in the work of Reed and Cichanowski [7], and Taylor [9].

This investigation focuses on the PML capacitor and the development of a coating such that very little moisture can enter the capacitor. The goal is to prevent loss of capacitance for 500 hours in an 85 °C, 85 % relative humidity environment with 25 Vdc applied. An additional specification is that the coating must be thinner than 200 μm.

Currently, the most common method of packaging capacitors is a thick coating of epoxy. This coating is commonly applied by dipping or box potting [2]. A thicker coating is a better barrier to moisture, but organic coatings in general are very poor barriers compared to metals or ceramics. Thus, the coating must be very thick (on the order of a millimeter) to have any effect. As the coating thickness is increased, the capacitance density begins to

decrease rapidly. This occurs because the volume of the coating is now significant compared to the volume of the capacitor itself.

Assume a capacitor of length l, height h, width w, and coating thickness t.

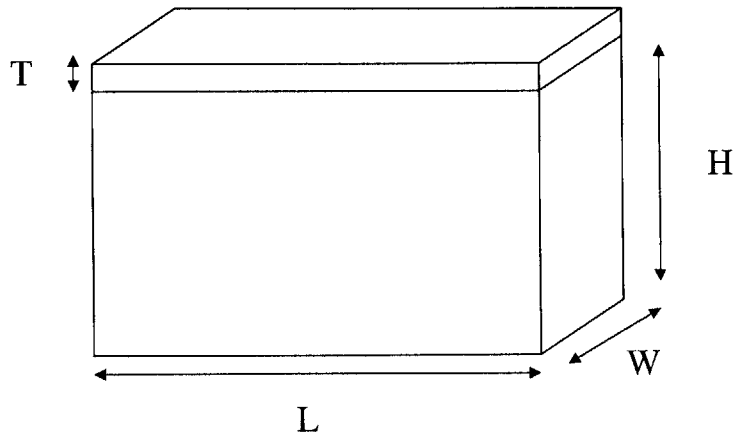

Figure 2.1: Capacitor Dimensions

$$V_{tot} = l(w + 2t)(h + 2t) \tag{2.1}$$

$$C_{density} = \frac{wh}{wh + 2tw + 2th + 4t^2} \tag{2.2}$$

This model assumes that the terminations are an adequate barrier to moisture, and are not coated. At zero coating thickness we have 100% utilization of the available volume. As the coating thickness increases to the order of magnitude of the capacitor, the capacitance density becomes very poor. A quick calculation reveals that for an example PML capacitor (l = 5 mm, w = 3 mm, h = 2 mm), a 1 mm coating would lead to a capacitance density of 30%. This is clearly unacceptable. Furthermore, this would be a relatively large capacitor by the standards of surface mount capacitors, and smaller capacitors would have even lower capacitance density. If the coating thickness could be decreased to 25 μm, then the capacitance density could be increased to 96%.

There are clearly many challenges associated with decreasing the coating thickness. In Section 2.2, I present the basic problem of moisture ingress into packages.

2.2 Moisture Ingress into Packages

Water has long been a reliability problem for electronics. Moisture is ubiquitous in the environment, and is readily absorbed into many organic materials used as protective barriers. To compound the problem, electronic devices typically operate at temperatures much higher than room temperature, thus increasing the rate of moisture diffusion [10].

Water causes numerous problems. As one example, moisture aids in the transport of harmful ionic contaminants (e.g. Cl ions) into packages. Aluminum is frequently used as a material in electronic assemblies, and the Cl ions rapidly attack the aluminum and cause it to break down into alumina or hydrogenated alumina. If even one of these connections become degraded, the circuit can fail.

This example is particularly interesting for capacitor packaging because the metallized layers of the PML capacitor are extremely thin (30 nm) layers of evaporated aluminum. If moisture is allowed to come in contact with these aluminum layers, then this thin metal layer may be corroded away, leading to a dramatic drop in capacitance. In fact, this phenomenon has been seen on PML capacitors, and a near total loss of capacitance results if the capacitor is left unprotected.

Ambient moisture levels are quantified by two types of humidity - absolute humidity (AH) and relative humidity (RH). Absolute humidity is defined as the concentration by weight of water molecules in a mixture of water and another substance. Relative humidity is defined as the amount of water present in a given mixture normalized to the amount of water present when the mixture is saturated with water. RH is typically expressed as a percentage [11].

When moisture is present in the air surrounding a component, it comes into contact with the

surface of that component. The amount of moisture that adsorbs onto the surface depends on the surface energy. If the surface energy is high, then water molecules will "wet" the surface to a high degree, and such a material is called hydrophilic (also hydroscopic). If the surface energy is low, then very few water molecules will bind to the surface. This kind of material is termed hydrophobic. The presence of ionic impurities can facilitate the adsorption of water at lower RH than typically would be required [11].

While adsorption is an effect dominated by relative humidity, the movement of moisture through materials is due to the absolute humidity.

Several studies have shown that water permeation through organic compounds shows Fickian behavior in general, with some deviations due to damage in the polymer matrix [12, 13]. This means that moisture diffuses in response to a concentration gradient. In one dimension, Fick's second law is as shown in Eq. 2.3.

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \tag{2.3}$$

A PML capacitor is clearly a three dimensional structure. In addition, it has a layer structure at a very fine scale. Modeling this complicated structure would be a very involved effort. We can gain more insight into the problem using a lumped element model. Such a model is derived in [11]. Consider a sealed cavity of volume V, surface area A, and wall thickness L. If one assumes a linear distribution of moisture in the wall, and a uniform concentration of moisture inside the cavity, then we can write a differential equation governing the moisture inside the cavity Eq. 2.4 [11].

$$\frac{dc_i}{dt} = \frac{AP}{VL + V_{wall}LK/2}(c_a - c_i) \tag{2.4}$$

In this equation, c_i is concentration of moisture inside the cavity and c_a is the ambient concentration of moisture, and K is the solubility partition coefficient. If the initial con-

centration of moisture inside the cavity is zero, then the solution to Eq. 2.4 is Eq. 2.5, the familiar solution to a 1st order linear ordinary differential equation [11].

$$c_i = c_a[1 - \exp(-t/\tau)] \tag{2.5}$$

Using the relationship $V_{wall} = AL$ and the definition $P = KD$ where P is the permeability and D is the diffusion coefficient, we can a general expression for the time constant τ [11].

$$\tau = \frac{VL}{AP} + \frac{L^2}{2D} \tag{2.6}$$

If the walls are extremely thin and absorb little moisture, then $\tau \simeq VL/AP$. In the case that the walls are very think and absorbing, and in the limit $V \rightarrow 0$ then $\tau \simeq L^2/2D$ [11].

This system can also be modeled by a lumped element circuit. In this model, voltage corresponds to concentration of moisture, and current represents the flow of moisture. A simple RC circuit gives some insight into the problem. We treat the system as having two nodes, or areas of lumped relative humidity. These are the ambient moisture level, and the moisture level inside the capacitor.

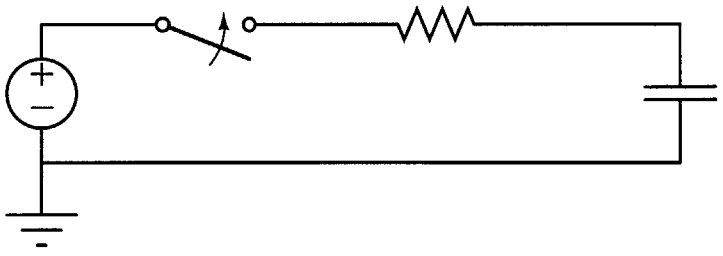

Figure 2.2: Lumped element model for moisture ingress

We see from the transient response (Eq. 2.5) that the relative humidity inside the capacitor will eventually reach the ambient RH level. This increase of humidity inside the capacitor

can only be slowed, not prevented entirely. The speed of this process can be decreased by making τ as big as possible. In the circuit model $\tau = RC$ where R is the moisture resistance and C is the moisture capacity. C could be increased by changing the dielectric material so that it does not absorb much moisture. The humidity resistance R can be increased greatly by encasing the capacitor in coating that slows the permeation of water.

Diffusion is an Arrhenius process, which means that the kinetics are dominated by surmounting local energy barriers. Increasing the temperature speeds up this process, as individual water molecules will have greater thermal motion and it will be easier for them to achieve the necessary activation energy.

$$\ln D \propto \frac{1}{T} \tag{2.7}$$

This is important because the ambient temperature in electronic assemblies is typically much higher than room temperature.

There are several ways that this moisture uptake can be measured, of which the most popular are weighing and capacitance measurement. I have chosen to use capacitance as a measure of moisture content, for this is easily measured and is an established means of measuring moisture in packages.

For a parallel place capacitor, the capacitance is given in Eq. 2.8.

$$C = \frac{K\epsilon_0 A}{d} \tag{2.8}$$

Since these acrylate dielectrics have a K_D of approximately $3-6$, and water has $K_W \simeq 80$, moisture ingress into the capacitor should produce a rise in capacitance. Since these two dielectric constants are more than an order of magnitude apart it should be easy to detect small quantities of water.

To determine the amount of water inside the capacitor, we make several assumptions. The first is that the capacitance of this multi-layer capacitor can be approximated by a simple single-layer capacitor as in Eq. 2.8. Second, it is assumed that K is approximately a linearly weighted combination of K_D and K_W, based on the relative volume that they occupy in the capacitor V_D and V_W. This linear weighting to obtain a mixed dielectric constant is presented in [14]. Other methods exist that use logarithmic weighing such as the Brasher-Kingsbury equation. The linear method seems to correspond better with gravimetric data [14].

$$K = K_D V_D + K_W V_W \tag{2.9}$$

Certainly there is no loss of dielectric material when water is absorbed into the capacitor, so we can approximate $V_D \simeq 1$. Possible swelling of the polymer due to water uptake is ignored in this analysis. If we take Eq. dielectric and then divide by the initial condition (no water uptake), then we have Eq. 2.10.

$$\frac{K}{K_0} = \frac{K_D + K_W V_W}{K_D} \tag{2.10}$$

Rearranging, and using the fact that capacitance is proportional to K, we obtain

$$V_W = \frac{\frac{C}{C_0} - 1}{\frac{K_W}{K_D} - 1} \tag{2.11}$$

where V_W is the volume fraction of water in the capacitor (unitless).

During exposure to humidity, the capacitance has been found to increase 18 % in an 85 % RH environment. Assuming $K_D = 5$, from Eq. 2.11 the volume fraction of water is derived to be 1.2 % , or 248 nL. This amount of water would weigh 0.248 mg, a weight that would be

difficult to measure with accuracy on typical laboratory scales. A protective coating should slow the rate of moisture ingress into the capacitor. Given infinite time in a high humidity environment, diffusion will eventually cause the moisture content of the capacitor to reach this value. A protective coating should ideally make this time constant much longer.

Capacitive sensing is a well established method of measuring moisture concentration in situ for various applications [14]. Since the device in question is a capacitor, this technique seems to be a natural means of monitoring the moisture content. The goal has been to find a material coating which prevents moisture ingress, which will be demonstrated by a slower increase in capacitance under the above test conditions. This test seeks to measure simply the moisture ingress into the capacitor, with the understanding that this will cause corrosion problems in any real application. Thus, we have a simple measurement of the moisture content of the capacitor, and can use the above model to evaluate different packaging techniques directly by their characteristic time constants.

Chapter 3

Coating Techniques

This chapter presents the coating techniques that were developed, fabricated, and tested during this investigation.

The first method to consider is the single-layer coating method, which is the simplest of all the methods considered. It consists of a single-layer of material applied to the capacitor. The biggest advantage is that it is the easiest to deposit, and thus is the least expensive method. This method is commonly used in industry to protect capacitors from moisture. Typically, a thick coating of epoxy is applied by dipping or box potting. Unfortunately, a thick layer takes up quite a lot of space, as discussed in Ch. 2. Decreasing the thickness of the epoxy leads to an inadequate barrier to moisture. Metals cannot be used, because this will lead to the capacitor being shorted out. Ceramics might be considered, but there are two problems with making them work as a single-layer coating.

The first problem with ceramic coatings is the coefficient of thermal expansion mismatch between the ceramic and the capacitor. One could compensate for this problem by making the ceramic very thin and making the film less brittle. There is also the problem that the capacitor is not a flat surface. Surface damage is caused by the dicing saw used to cut the capacitors. These rough edges are very difficult to coat with a thin coating without leaving holes (or leaving the potential for holes to be created by the expansion and contraction of the sharp edges under temperature cycling).

Because of these problems, the single-layer coating method is effectively limited to organic coatings. Several materials have been tested for this method. Our experiments indicate

that the moisture resistance of organic coatings is very limited, particularly if they are made very thin. Several different organic materials have been tested, and these results are discussed in Ch. 6.

The second method under consideration is the labyrinth seal method proposed by C.R. Sullivan [6]. Fig. 3.1 shows the processing steps of making a moisture barrier via this method. The basic principle is to use the low moisture transmission of metals, but to avoid shorting out the capacitor by placing insulating polymer between the metal sections. By using the steps described, one can create a package such as that shown in Fig. 3.2. The only way that moisture can enter this package is by taking a long and narrow path through the labyrinth.

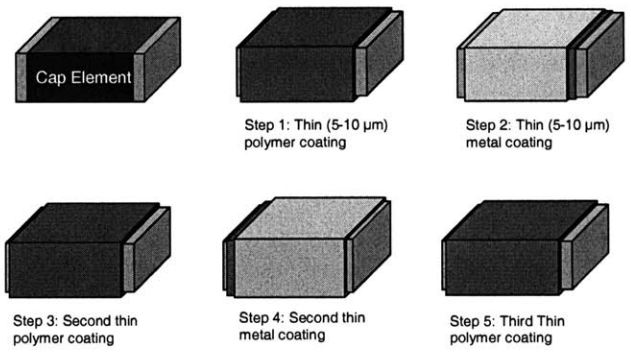

Figure 3.1: Fabrication steps for a capacitor package implemented with the "Labyrinth Seal Method".

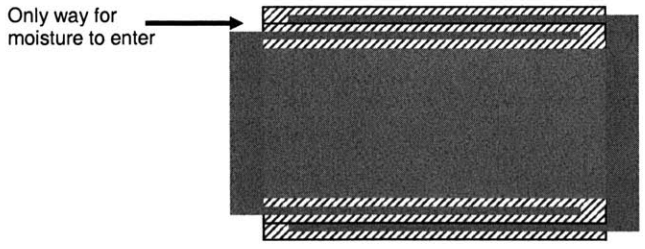

Figure 3.2: Cross Section of a capacitor package with a "Labyrinth Seal".

This method requires more processing steps than the single-layer coating method. There is great potential for improved moisture resistance, because moisture must take a very long

path (the length of the device, which is on the order of a few millimeters) to get to the inside of the capacitor. This channel is also only a few microns in height, which leads to greater moisture resistance. This means that the dielectric layer of the labyrinth can have relaxed moisture resistance properties. The dielectric material must also be able to withstand the voltage applied across the capacitor, as can be seen from the geometry in Fig. 3.2. Ideally, the materials used to make the labyrinth would be inexpensive.

The primary difficulty with this method is that the materials must be precisely patterned in order to prevent shorting of the capacitor. This may be accomplished by a using a photoimageable organic layer, or by using a physical mask to select which areas will be coated. The metal may also be selectively deposited by using a mask.

In this investigation, labyrinth packages were fabricated using parylene-c as the organic layer, and aluminum as the metal layer.

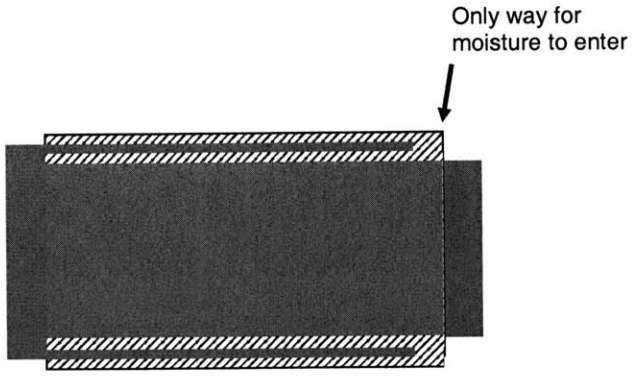

Figure 3.3: Cross Section of a capacitor package with a "Half-Labyrinth Seal".

The third method under consideration is called the Half-Labyrinth Method. This technique is a lower cost alternative to the Labyrinth Seal Method. The processing steps are the same as the first three steps in the Labyrinth Method. This method does not force moisture to take a long path go get into the capacitor, but it does reduce the area of polymer that is exposed to the environment (see Fig. 3.3). Ideally, this would slow the rate of moisture ingress into the capacitor.

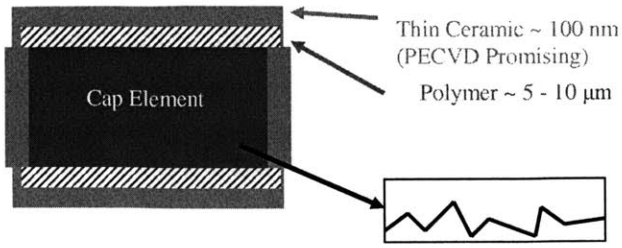

Figure 3.4: Cross Section of a capacitor package with buffered-ceramic Barrier.

The fourth method under consideration is called the buffered-ceramic Method. Fig. 3.4 shows a cross section of this technique, which consists of a layer of polymer and then a layer of ceramic. The polymer serves as a buffer layer to smooth out the peaks and valleys of the capacitor surface. It also separates the ceramic material and capacitor which may prevent CTE mismatch from leading to cracking. This method is attractive because it is relatively simple to apply. It is also scalable, so that is more moisture protection is necessary this technique can be repeated in a stack of several layers. Similar methods have been used for the protection of OLEDs [15], and this type of technique has demonstrated excellent moisture protection. Another benefit over the labyrinth method is that it does not use metal, and so we avoid any concerns about shorting out the capacitor.

These four methods have been fabricated using the materials discussed in Ch. 4. Testing techniques and results of these tests are presented in Ch. 5 and Ch. 6. The buffered-ceramic method is the most promising technique, and has been tested extensively. The results of this testing are discussed in Ch. 6.

Chapter 4

Materials and Deposition Methods

This chapter will present an overview of the materials one might consider for this application and their key characteristics. In addition, we will outline the available deposition methods and considerations for coating PML capacitors.

4.1 Materials

There are many types of materials that one might consider for electronic packaging. For integrated circuit packaging there exist two general types of packages - hermetic and non-hermetic packages. In fact, no material system can ever form a perfect seal against the environment. The term hermetic has been used to describe metal or glass packages which have a helium leak rate of less than 1×10^{-8} $atm \cdot cc/s$ [16]. Hermetic packages are frequently used in military and space applications for which the electronics must have very high reliability. For consumer electronics, packages used to be made of metal or glass. Prohibitively high costs have driven industry to use plastic packages in recent years. Unfortunately, plastic packages must be relatively thick to provide adequate moisture protection.

Figure 4.1 shows the time it would take for moisture to permeate through a given thickness of various materials at room temperature. Glasses and metals have the lowest moisture permeabilities, but there are several difficulties with these materials that limit their use in typical applications. Glasses, for example, have a brittle failure mechanism when the material is stressed. They are also very stiff, due to a high elastic modulus, and have a low

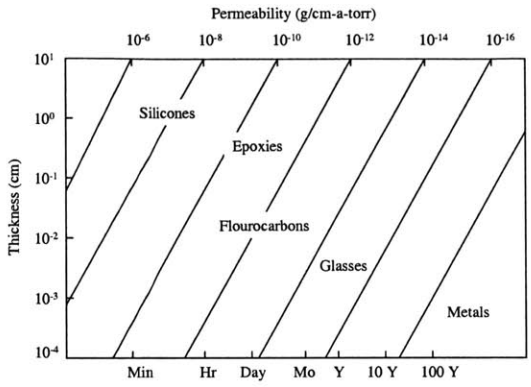

Figure 4.1: Materials Permeability to Moisture. Lower axis shows the time it takes for the inside of a package to reach 50 % of ambient RH level. Adapted from Madou [17].

coefficient of thermal expansion. This high elastic modulus means that even a small strain can cause a very high stress, and stress leads to brittle failure. One source of strain occurs as the capacitor is heated and cooled - any mismatch between the thermal expansion coefficient of the capacitor and that of a glass coating will lead to stress, and possibly cracking. The formation of cracks is a big concern in the design of a barrier coating, as any crack or hole in the package will allow moisture ingress.

Metals tend to be more forgiving than glasses, and can often absorb a stress through deformation rather than brittle failure. A metal coating is difficult to apply to a capacitor because of the danger of creating a low resistance path between the terminals. Even if a metal coating is applied without shorting out the capacitor, there exists the possibility that some of the metal will migrate with time and create a short at some time in the future.

Polymers are difficult to discuss as a group, because they can have many different properties. They can be brittle or plastic, conductive or insulating. There are many plastics which are both sufficiently pliant and also insulating. The difficulty is that polymers are much more permeable to moisture than glass or metal. For some polymers, one can try to improve this property by making a polymer denser. To do this, the polymer is heated or exposed to UV light in order to increase the crosslink density. One potential problem is that increasing

Table 4.1: Summary of material advantages and disadvantages.

Material Class	Advantages	Disadvantages
Polymers	Can be insulating. Good toughness and flexibility	Poor moisture barrier.
Ceramics	Good moisture barrier, can be insulating.	Cracking.
Metals	Excellent moisture barrier	Conductive, can corrode.

the crosslink density also can make the polymer more brittle, and even with an extremely dense polymer the moisture permeability is still poor.

Some very general advantages and disadvantages of the different material classes are summarized in Table 4.1.

The first type of coating to be tested was a 1 μm coating of SiO_2. SiO_2 was chosen because it is a material that is very commonly used in the semiconductor industry. It is readily available, inexpensive, and there are several technologies available for depositing the material. It would be extremely cost effective if a single-layer coating could adequately protect the capacitor from moisture. The only feasible material for achieving this goal is a ceramic.

Capacitors were directly coated with a 1 μm thick coating of SiO_2 using electron beam evaporation. This coating was examined under a microscope, and did not appear to have a large number of cracks; however, when these capacitors were subjected to environmental stress (125 °C, 100 % RH) the film appeared to crack.

This method of protecting the capacitor did not succeed. The SiO_2 coated capacitors failed to show an improvement in moisture resistance. These results are discussed in greater detail in Chapter 6. This failure occurred because the SiO_2 coating cracked due to thermal stress. We believe that this cracking was due to the coefficient of thermal expansion (CTE) mismatch between the capacitors and the coating. These capacitors have electrodes which are made of aluminum, a material with high CTE (Table 4.2). The CTE of SiO_2 is about 10 times smaller in magnitude. As a consequence, the aluminum expanded more than the

Figure 4.2: Left: Uncoated capacitor. Right: Silicon dioxide coated capacitor exhibits cracking at high temperature.

SiO_2 coating during our pressure cooker tests, causing the film to crack. This cracking might be avoided if one were to use a ceramic material that is less brittle, and has a CTE closer to that of aluminum. Unfortunately most ceramics that are currently applied using microfabrication techniques have a CTE which is very low.

Table 4.2: Comparison of Material Properties [10, 18, 19, 17, 20, 21, 22]

Material	Moisture Resistance	Thermal Expansion Coefficient 10^{-6}/ °C	Young's Modulus (GPA)
SiO_2	Moderate	2.3	70
Si_3N_4	Excellent	1.6	270
SiC	Excellent	3.5-4.6	?
AlN	Excellent	4.3-4.7	?
Al	Excellent	25	70

For very thin ceramic films the typical material properties do not apply. When the coating is less than a few hundred angstroms it can endure more stress without cracking. In fact, these very thin films can be so durable that they have been used as flexible packaging materials for displays [15]. It has also been reported that a thicker film is not necessarily a better moisture barrier. Once the film becomes thicker than the size of individual grain sizes, increasing thickness is not beneficial [15]. These observations provide a motivation for the use of very thin ceramic coatings.

Table 4.3: Materials Combinations Considered. Materials that have been tested are shown in bold.

Coating Technique	Organic	Ceramics	Metals
single-layer Coating	**Parylene**, SU8	SiO_2	
Labyrinth Methods	**Parylene**, SU8		**Al**, Ni, Ti, **Cu**
buffered-ceramic	**Parylene**, **SU8**, **Acrylate**	SiO_2,Si_3N_4,Al_2O_3	

Table 4.3 details the materials that were considered for the coating techniques discussed in Ch. 3.

Polymers are generally more permeable to moisture than ceramics or metals. One polymer that has a particularly low permeability to moisture is parylene. This material was originally developed to protect circuit boards. Parylene has excellent properties for capacitor coatings, in particular:

1. High resistivity
2. High breakdown voltage
3. Excellent conformal coating
4. Excellent humidity barrier properties

There are several types of commercially available parylene, of which parylene-c has the highest resistance to moisture diffusion.

Another possible organic material to consider is an epoxy. SU8 (Microchem Corp., Newton, MA) is a photoimageable epoxy that was first developed by IBM in the 1990s [23, 24, 25]. The advantage of SU8 is that it is a liquid which can be applied to the capacitor by dipping. The use of a liquid allows for the filling of areas of surface roughness on the capacitor. In addition, SU8 can be patterned by standard photolithography techniques. This could allow for easier fabrication of the more complex packages discussed in Ch. 3.

Another potentially useful organic material is an acrylate polymer [26]. The capacitor is first coated in liquid acrylate monomer by dipping. The film can then be cured by either an electron beam, or by the addition of photoinitiators and the use of UV light to initiate polymerization. There are several advantages to such an approach. The primary advantage for manufacturing is that the acrylate and photoinitiators are inexpensive. Acrylate is also advantageous because it cures with very low surface roughness. One major drawback to acrylate is that it is hydroscopic and absorbs water readily, but when used with layers of ceramic (buffered-ceramic method) it may be possible to achieve sufficient moisture protection. This method has been tested, and is discussed in Ch. 6.

4.2 Deposition Methods

This section discusses the deposition methods that are potentially useful for moisture barrier coatings of passive components. Regardless of the class of material being deposited, there are several key characteristics for a deposition method used for moisture barrier packaging.

1. Must yield a thin and uniform coating
2. Substrate temperature during deposition must remain below 175 °C
3. Low defect density
4. Scalable for mass production
5. Inexpensive

For metals and ceramics there exist numerous deposition methods which have been optimized for use in the semiconductor industry. Dry deposition methods include sputtering, electron beam evaporation, thermal evaporation, and many others.

Sputtering is the process of using a plasma to bombard a target and transfer a film of material onto a substrate (component to be coated). An electric field (AC or DC) is

Figure 4.3: Step Coverage

applied, and Ar ions are accelerated towards the target. When the Ar ion strikes the target its kinetic energy is transferred to the target material, and particles are ejected. One disadvantage of this method is that the Ar ions strike the target as well as the substrate. This can be beneficial for adhesion, but can also lead to excessive substrate heating. Another disadvantage of sputtering is that the deposition rate can be very low for many materials (less than 1 $\AA$/s).

Evaporation is another process used to deposit metals and ceramics. The principle is that a piece of material is placed in a crucible, and then heated so that the metal evaporates and then condenses on the substrate. Common methods include thermal evaporation (resistive heating) and electron beam evaporation. In electron beam evaporation, an electron beam is directed at the crucible to induce evaporation. This method allows the center of the crucible to be targeted and helps prevent the evaporation of impurities.

Electron beam evaporation provides very high quality metal films, and does not lead to excessive heating of the capacitor. One major concern is that the technique is highly directional, and leads to poor step coverage. This is illustrated in Fig. 4.3.

Evaporation tends to have poor step coverage, and sputtering tends to have very good step coverage. The reason is that sputtering is done at relatively high pressure, which makes the mean free path between molecules shorter. This means that the material encounters more collisions on its way to the substrate, thus causing particles to impinge on the substrate from many angles. Step coverage is important because it affects the number of processing

steps needed to coat a three dimensional device such as a capacitor.

Sputtering and evaporation are known as physical vapor deposition (PVD) methods. An alternative to PVD is chemical vapor deposition (CVD). CVD processes are characterized by the reaction of gases on the surface of a substrate to produce a solid thin film. There are several different types of CVD, including low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD). LPCVD is a very high temperature process used to deposit high quality oxides, nitrides, and polysilicon primarily for integrated circuits. LPCVD is such a high temperature process that it will not be considered further. PECVD is typically used to deposit silicon oxides and nitrides for passivation on integrated circuits. While these films are typically not as high quality as films produced by LPCVD, the deposition temperatures are typically 300 °C. PECVD can even be done at very low temperatures (60 - 100 °C); however, the resulting films have lower density and more defects. PECVD oxides and nitrides are also used in the food packaging industry to seal packages from moisture and oxygen. One disadvantage of PECVD for depositing SiO_2 is that it requires poisonous and explosive silane gas (SiH_4) for depositing SiO_2. The use of silane could make it difficult to scale this process up for mass production.

An alternative method is to use reactive sputtering. This is similar to sputtering, except that a small quantity of O_2 is put into the chamber along with Ar. By adjusting the amount of O_2 a stoichiometric oxide can be achieved. In practice I have seen that stoichiometric films for both sputtering and PECVD are achievable, as evidenced by dielectric constant measurements.

There are also wet methods for depositing metals. These include electroplating and electroless plating. Both are heavily used in the manufacturing of printed circuit boards. They can be used to deposit thick metal films of high quality. Electroplating is used to deposit metal on top of a metal, while electroless plating can deposit metal on top of an insulator. Much thicker films are possible with these methods than evaporation or sputtering. One major drawback is that they are both done in an aqueous environment. Since the capac-

itor is particularly sensitive to moisture absorption, we might expect the acids to become absorbed into the capacitor during deposition.

Electroless plating (Cu) was attempted for use in the labyrinth method. The resulting film was of very poor quality, had poor adhesion, and did not completely cover the area we wished to coat. It is believed that the electroless plating reaction was spoiled by the Al termination of the capacitor. A detailed study was not conducted.

Depositing thin and uniform polymer films is much more difficult than depositing metals or ceramics. In the microelectronics industry this uniformity has been achieved for photoresist materials by spin coating them. Spinning the wafer at high speeds (thousands of RPM) creates a force which pushes the polymer to the outside of the wafer. If the viscosity is low enough, the resulting film will be very uniform. This technique is used commercially in the production of integrated circuits. Spin coating is not feasible for a three dimensional object such as a capacitor.

Spray coating is another option. I have used an airbrush to spray photoresist, but uniformity is difficult to achieve. A low-viscosity polymer is essential for the droplets to spray. This method is very messy, and wastes a lot of material. These two concerns could lead to lower reliability and increased costs in a production setting.

Dipping is simpler than either of these methods. When a material is dipped into a liquid, the thickness of the resulting film is dependent on the viscosity of the liquid, the speed at which the material is removed, and the quality of adhesion. Because of its simplicity and effectiveness, this has been the method of choice for depositing SU8 and acrylate films. Detailed steps for dip coating are given in Appendix B.

Another option is to use an entirely different class of polymer. Parylene-c is interesting for this application, because it is hydrophobic and has a very low permeability to moisture [27]. It is also interesting because it has a unique deposition method. Parylene-c begins in the form of a dimer. The dimer is vaporized at 150 °C, and goes into a much hotter chamber,

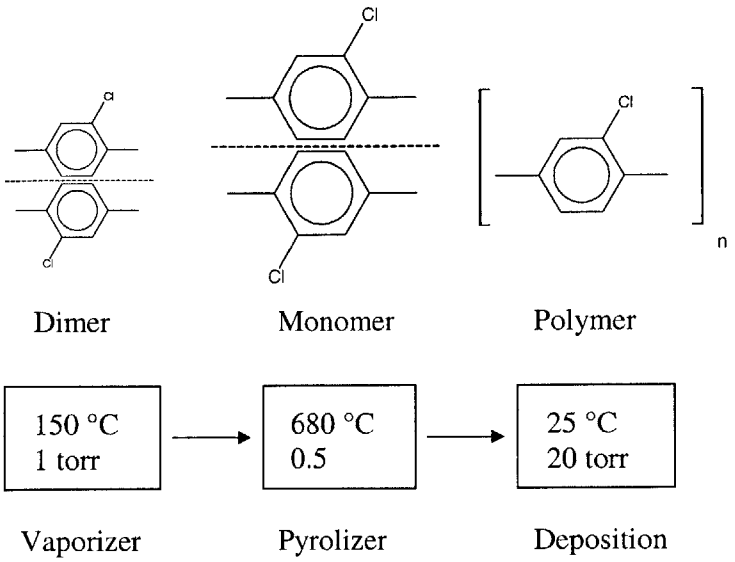

Figure 4.4: Process Flow for Parylene Deposition [27]

where the polymer undergoes pyrolysis. This is known as "cracking" the dimer into its monomer constituents. During this time, the chamber with the substrate (capacitors) stays at room temperature. When these monomers enter the chamber in gas form they polymerize on the (relatively) cool surface of the chamber walls and substrate. The result that the capacitor is coated on every exposed surface with parylene. This vapor deposition process results in a uniform and pinhole free film, and the capacitor never rises more than a few degrees above room temperature. This process is shown in Fig. 4.4.

Unfortunately, parylene-c is not meant to undergo temperatures above 100 °C for an extended period of time. This would most likely prevent it from being used as a packaging material for PML capacitors, which are used in applications up to 175 °C. Another difficulty is that the deposition process is rather slow - for parylene-c the deposition rate is just 1-2 μm per hour. High temperature versions of parylene are currently under development (Cookson Electronics).

Despite these problems for using parylene in a production setting, it is useful for making prototype packages for capacitors. Parylene has been used to make packages based on each of the coating methods proposed (single-layer, labyrinth, and buffered-ceramic). Evaluation of these coating strategies is discussed in Ch. 6.

For each class of materials there are several materials and deposition methods to consider. This chapter has provided an overview of the materials considered in this investigation, and the reasons for choosing them. There are surely many other materials (particularly organic materials) which may be considered for this application.

Chapter 5

Testing Methods

There are many methods available for testing electronics in elevated temperature and high humidity environments. The tests most widely used in industry typically require a humidity chamber. In the first part of this investigation, we attempted to use simplified and less expensive testing procedures. These include the saturated pressure cooker test, the ambient humidity test, and the oven humidity test. These tests were found to be unreliable. We found that a commercial environmental chamber was well worth the cost, as this helps decrease experimental variables. These tests are discussed below.

5.1 Saturated Pressure Cooker Test

As a first test of humidity resistance we used a programmable pressure cooker (Figure 5.1 and 5.2). Capacitors were placed in a steam bath at 125 °C, and 100% RH, and an air valve was left open to keep the pressure at 1 ATM. At this high temperature and high humidity level moisture diffuses into the capacitor at an accelerated rate.

Capacitors are placed in the pressure cooker for 30 minute intervals. After 30 minutes, the capacitors are allowed to cool for 10 minutes at room temperature. The ESR and capacitance are measured, and then they are placed back into the pressure cooker. The total time spent in this high-humidity environment is 2 hours. This experiment has been carried out for bare capacitors, and it has been found that the capacitance of bare PML capacitors increases by about 6% in 2 hours under these conditions. This increase in capacitance

Figure 5.1: Pressure Cooker

is caused by the dielectric properties of water. Water has a very high dielectric constant (80) at the frequency of measurement (100 kHz). Further discussion of theory is presented in Ch.2. This capacitance change is used as a measure of the moisture resistance of the capacitor coating.

Numerous pressure cooker experiments have been carried out to attempt to correlate coating performance. Conditions in the pressure cooker are very harsh. Many standard humidity tests are conducted at 85 °C and 85% RH. By contrast, the pressure cooker test is 125°C and is far greater than 85% RH. One of the most difficult aspects of this test is keeping moisture droplets from condensing or dripping onto the capacitors. These difficulties have also been reported by others [28]. In addition, the atmosphere is very turbulent inside the chamber, as evidenced by the high rate of air escaping. When the chamber is opened one can observe the vibration caused by boiling water. This vibration could be improved by a better experimental setup, but this would not solve the problem of the very high heat and moisture conditions.

We attempted to use the pressure test to differentiate between the effectiveness of different coatings. This test was often not repeatable for capacitors which had the same coating. A better test was needed.

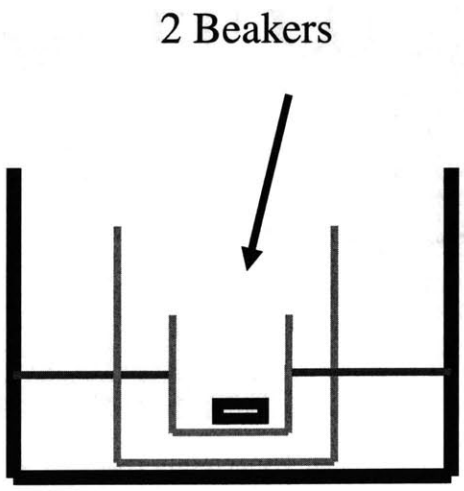

Figure 5.2: Pressure cooker test setup.

5.2 Room Temperature Humidity Test

The room temperature humidity test is the most simple of all the tests attempted. It consists of two vessels. The outer vessel contains water, and the inner vessel contains the capacitors. This allows the two chambers to share the same ambient humidity level. This apparatus can be seen in Fig. 5.3. To begin the test, the outer chamber is sealed. Soon, the air inside reaches an ambient humidity of greater than 90% (the limit of our measuring equipment).

The advantage of this test is that it is very simple, and avoids most of the problems of the pressure cooker test. The disadvantage is that it is a very slow test due to the low temperature (see Ch. 2 for a discussion of the temperature dependence of moisture diffusion).

This test was used to compare the moisture resistance of parylene-c and aluminum films. First, leads were attached to the capacitors, and then the films were deposited. The capacitors were then placed in the test chamber. Fig. A.1 shows the capacitance change over time. An 8 μm film of parylene helps to slow moisture diffusion into the capacitor. In addition, it is clear that a thin layer of Al (0.5 microns) also has a significant improvement on moisture

Figure 5.3: Room Temperature Humidity Test Setup

protection. The implications of this result are discussed further in Appendix A.

5.3 Oven Humidity Test

This purpose of this test is to obtain conditions of 85 °C and over 90% RH, much like standard humidity tests. The setup is similar to that of the room temperature humidity test, but glassware is used instead of plastic containers. The apparatus for this test is shown in Fig. 5.4.

This test was not successful because it was difficult to control the RH inside the chamber. It is believed that this was caused by the unreliability of the glass-to-glass seal. Vacuum grease was used to improve this seal, but it did not solve the problem. It may be possible to achieve the desired conditions with a rubber seal.

After attempting to use these three simple tests as a substitute for a humidity chamber, we abandoned them due to concerns about repeatability. With further work they could each be improved. We decided to use a commercial precision controlled environmental chamber to reduce the number of questionable experimental variables.

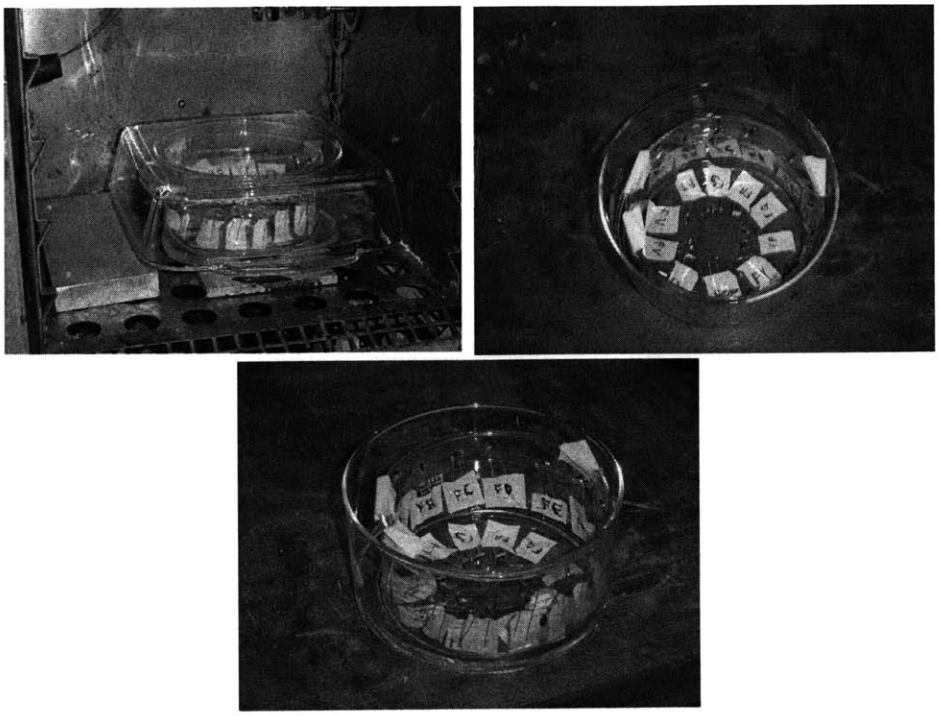

Figure 5.4: Oven Test Setup

5.4 Environmental Chamber Test

An Espec temperature and humidity chamber (Espec model LHU-113, Espec Corp., Hudsonville, MI) was used as the primary testing method in this investigation to measure humidity resistance. The chamber was set to 85 °C and 85% RH. For testing without an applied voltage, capacitors were laid in a glass container which was open to the air. Some tests were conducted with an applied voltage of 25 Vdc. This was accomplished by using a DC power supply and running wires into the chamber. Capacitors were then wired in parallel. This environmental chamber test was found to be a reliable accelerated life test. Results from this testing are discussed in Ch.6.

Chapter 6

Results

This chapter presents the experimental results of the humidity tests introduced in Ch. 5.

6.1 Results of PCT Testing

The first set of testing was done using the pressure cooker test. Parylene-c was investigated as a single-layer coating material. First, leads were attached to the capacitors. Then parylene was deposited using the parylene coating process described in Ch. 4. The results of this test are shown in Fig. 6.1. In these plots, each line represents one capacitor. To make a measurement, the capacitors were taken out of the pressure cooker and allowed to cool for 10 minutes. Capacitance was then measured using an HP impedance analyzer. All capacitance measurements in this investigation were made at a frequency of 100 kHz.

These first results tests were encouraging, and suggest that the parylene-c slows moisture ingress into the capacitor. Capacitors that were coated have a far slower capacitance rise than uncoated capacitors.

When sent to Rubycon Corporation (Nagano, Japan) for testing in an 85 °C and 85 % RH environment this single-layer coating proved to be inadequate. In that test (which is far slower than the PCT and less harsh) capacitors coated with 25 μm of parylene-c did not show a substantial improvement in moisture resistance over bare capacitors. A loss of capacitance was prevented for 50 hours in this environment with an applied voltage. Unfortunately, the goal of this investigation is to prevent capacitance loss for 500 hours.

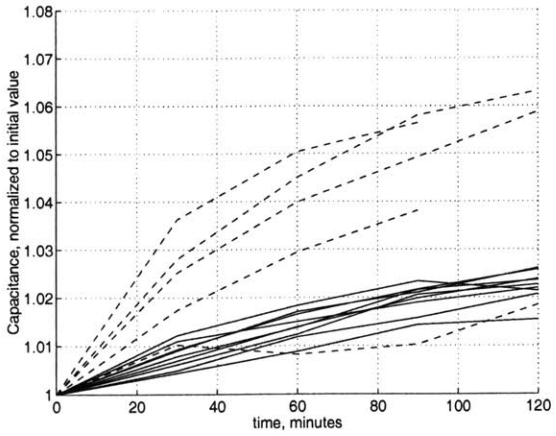

Figure 6.1: Test of parylene-c coated capacitors in PCT. Coated (solid) and bare capacitors (dashed) are shown.

From these tests we can conclude that a single-layer of parylene is not enough protection. In addition, we have learned that it is difficult to correlate the PCT results with the test results at 85 °C and 85 % RH.

To achieve improved moisture protection, several labyrinth and half-labyrinth method prototypes were fabricated and tested. Parylene-c was used as the insulating layer for these packages. To achieve parylene deposition on the sides of the capacitor, but not on the terminations, a novel "lift-off" type process was used (Fig. 6.2). First, capacitors were cleaned in oxygen plasma as discussed in Appendix A. Then, a drop of peelable latex solder mask was placed on the capacitor terminations, and allowed 15 minutes to solidify. Capacitors were then placed on a piece of polypropylene tape, with one termination making contact to the tape. Next, parylene was deposited. To finish the process, a pare of tweezers is used to remove the drop of solder mask. The resulting capacitor has a coating of parylene on the sides but not on the terminations. One disadvantage of this procedure is that the removal of the solder mask can cause the parylene to rip. As a result, I observed that this process works better for thinner coatings (smaller than 10 *mum*).

The materials used and the results of PCT testing are shown in Fig. 6.3. Packages a) (half-

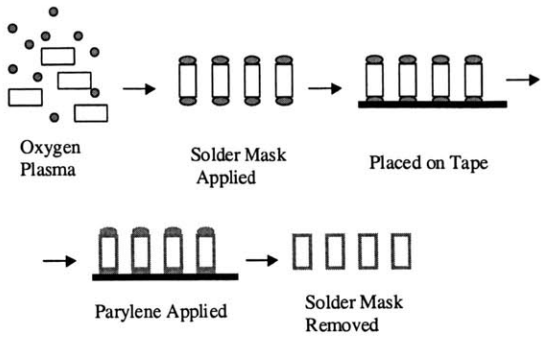

Figure 6.2: Parylene Liftoff Process

labyrinth) were fabricated using a 1 μm layer of parylene-c, and then 0.5 μm of evaporated Al. The Al coating required 4 depositions - one on each corner of the capacitor. Packages b) (half-labyrinth) were made using 8 μm of parylene and 0.3 μm of sputtered Cu. Two depositions were required for the Cu layer (less depositions are required for sputtering since it has good step coverage). Packages c) (full labyrinth) were fabricated using 8 μm parylene and 0.5 μm sputtered Cu. After fabricating the packages I attached leads to the capacitors for the purpose of testing.

Despite the use of metal as a barrier layer, these packages did not show a significant improvement in moisture resistance. In addition, there is a lot of variability within each type of package. Repeatability was difficult to achieve. For these reasons, and due to the difficulty of correlating the PCT test results with the 85 °C and 85 % RH testing, a new test was needed. The reliability of the pressure test was cause for concern for several reasons. It is a very harsh test, with a higher temperature and humidity level than desired. We noticed that often water would condense on the bottom of the pressure lid, and drip onto the capacitors. This problem could not be alleviated by placing a covering over the capacitors, because then water would just condense and drip from this covering instead. An environmental chamber test would greatly reduce the number of experimental variables and allow us to draw some useful conclusions about these coating methods.

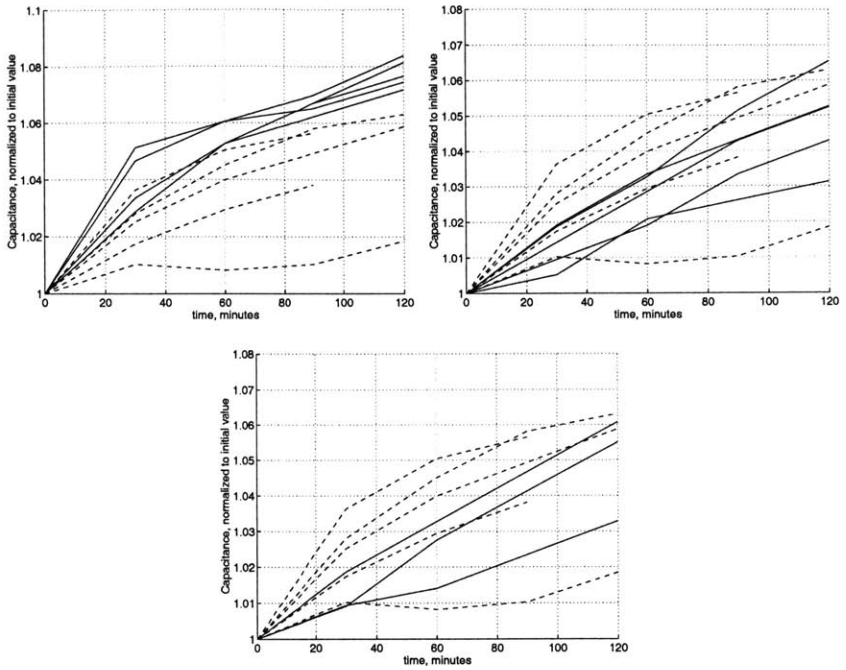

Figure 6.3: a) (top left) Capacitors with half-labyrinth of 1 μm parylene and 0.5 μm evaporated Al, b) (top right) Capacitors with half-labyrinth of 8 μm parylene and 0.3 μm sputtered Cu, c) (bottom) capacitors with full labyrinth of 8 μm parylene and 0.5 μm sputtered Cu.

6.2 Results of Environmental Chamber Testing

After having reliability concerns with the pressure cooker test, we decided to use a humidity chamber to improve the test. This environmental chamber (Espec LHU-113) controls the temperature and humidity to 85 °C and 85 % RH very reliably.

For the first test, capacitors with several different types of coatings were included, in addition to bare capacitors as a control. The results of this test (no applied voltage) is shown in Fig. 6.4. Capacitors with a coating of parylene-c were made by a single-layer deposition of 8 μm of parylene-c (without leads) and then attaching leads. The labyrinth coating was made by a sequence of 8 μm parylene-c (using lift off process discussed above), 4 depositions of E-beam evaporated Al applied with a different corner facing the source each time, 8 μm parylene-c, 4 depositions of Al, and then a final 8 μm parylene-c. Leads were attached

after deposition. A diagram of the geometry of the final product can be seen in Ch. 3. For the third coating technique (buffered-ceramic), 8 μm parylene-c was applied, leads were attached and then 0.17 μm PECVD SiO_2 was deposited. The last coating technique was also the buffered-ceramic method, but with SU8 2010 instead of parylene (see table B.2). Detailed deposition parameters for each of these steps can be found in Appendix B.

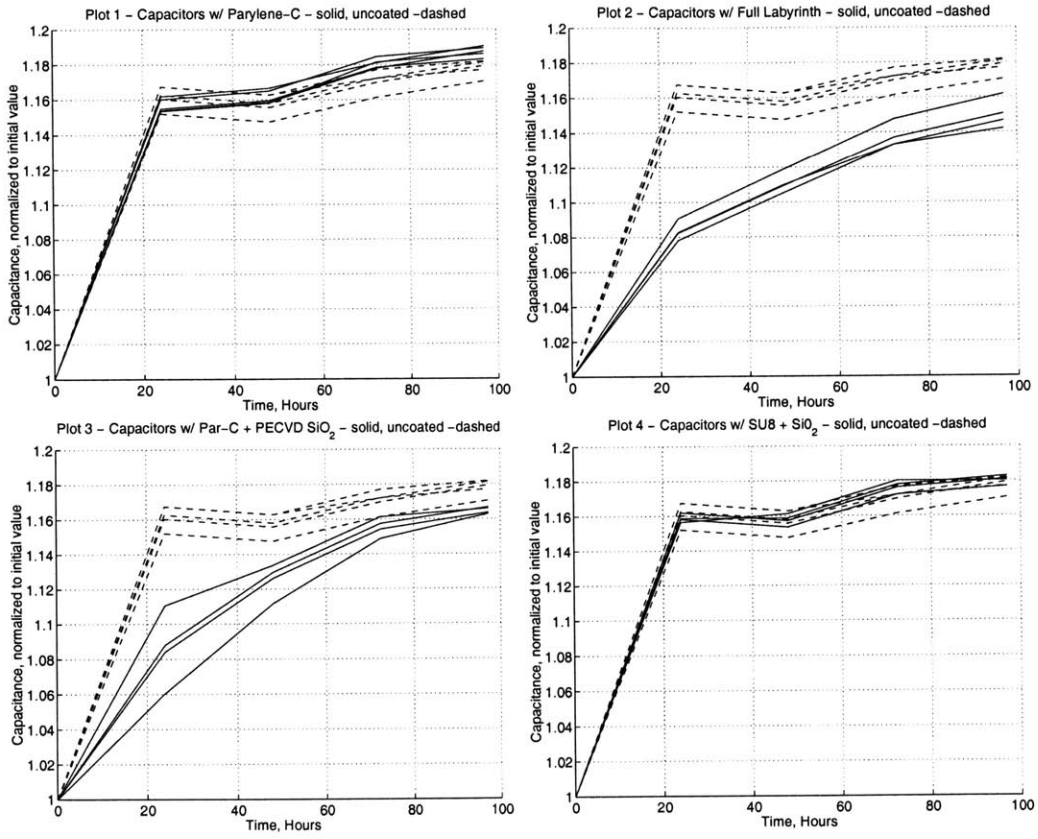

Figure 6.4: Humidity Testing Capacitance Results (without voltage)

This first plot (Fig. 6.4) shows that capacitors with 8 μm of parylene-c applied show the same performance as that of bare capacitors. The last plot shows similar for capacitors coated with SU8 2010 and 0.17 μm PECVD SiO_2. Clearly, these two packaging methods were not successful. In the second plot, we see the results of the labyrinth method. It is clear from this second plot that moisture is taking much longer to enter the capacitor than it does for the bare capacitors. This indicates that the labyrinth method shows promise

as a barrier to moisture. In plot 3 we see the results of 8 μm of parylene-c with 0.17 μm PECVD SiO_2. This technique also protected the capacitor from moisture, but not as well as the labyrinth method.

It is particularly interesting to compare plots 1 and 3, as the only difference between those two packaging methods is the 0.17 μm of PECVD SiO_2. This is strong evidence that the very thin layer of SiO_2 is acting as a very effective moisture barrier. This is a very interesting result, as the thickness of this oxide coating is negligible compared to that of parylene. In plot 4 we see that the SiO_2 did not have as much of an impact when it was applied on top of SU8. In fact, this particular combination is very poor barrier to moisture, at least as indicated by these initial tests. At a first glance this is puzzling, because we saw before that 0.17 μm of PECVD SiO_2 made an enormous difference when applied on top of parylene.

Parylene and SU8 have very different deposition methods, as discussed in Ch. 4. The parylene deposition process is conformal, and ensures that the entire capacitor surface is coated. SU8 deposition is more complex. The capacitor is first dipped in SU8, then baked to remove solvent. The coating is next exposed to UV light, which crosslinks the SU8. Finally, the film undergoes a "post exposure bake" and is then "hardbaked" to solidify and further crosslink the film. A detailed recipe for SU8 deposition is presented in Appendix B. It is likely that some part of this process did not work as expected, and as a result there were places on the capacitor where it was not fully coated. It is essential to leave no holes in the film, or else the very thin SiO_2 layer will not have an acceptably flat surface on which to be deposited. Another possibility is that the SU8 layer cracked. It is well known that SU8 tends to have high intrinsic stress, and can crack even if the film has been baked with care.

This test without an applied voltage has provided some information about the moisture barrier properties of these coatings. The true test of capacitor reliability is to also apply a voltage. Corrosion will eventually cause a loss of capacitance, and this must be prevented for at least 500 hours in this environment.

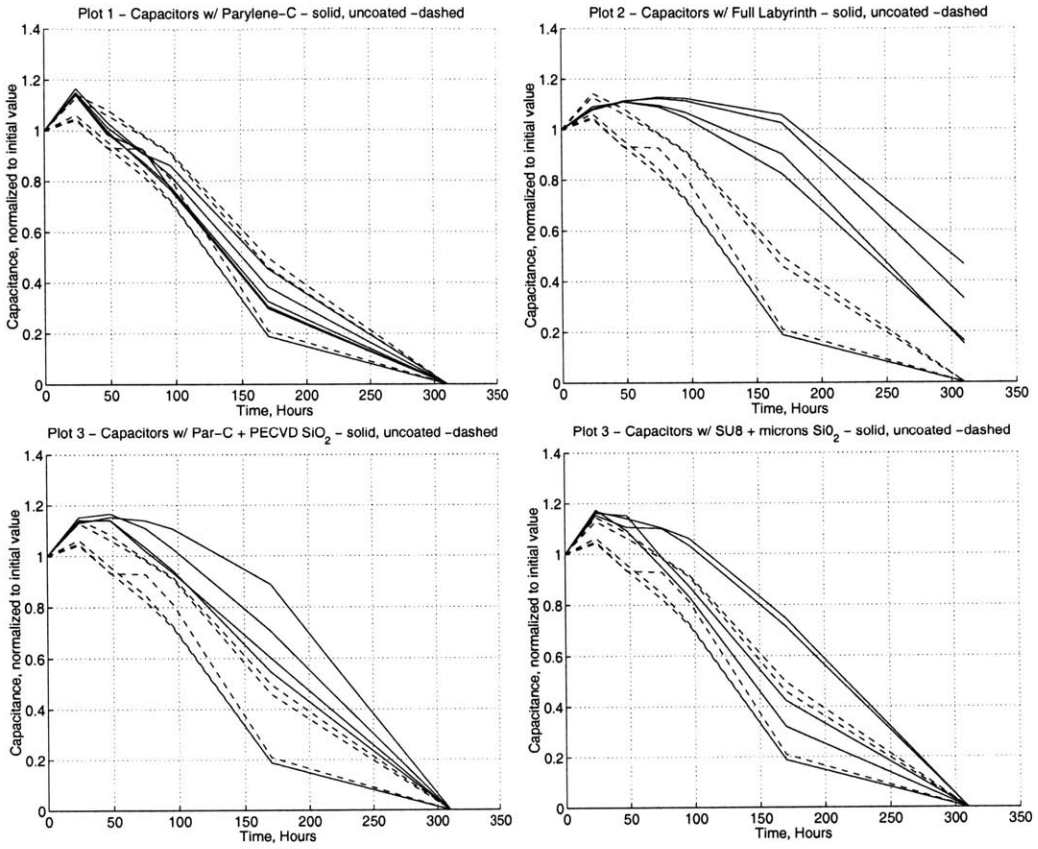

Figure 6.5: Humidity Testing Capacitance Results (25 Vdc)

Fig. 6.5 shows the results of placing the capacitors in the same high humidity and temperature environment while also applying 25 V. Uncoated capacitors first see a loss of capacitance at about 50 hours. The labyrinth method slows moisture ingress enough to delay this loss of capacitance out to approximately 150 hours. The buffered-ceramic method also helps quite a bit, and prevents capacitance loss out to 100 hours. When comparing these results to the test conducted without voltage, we see that the packaging methods which prevent moisture ingress are also those which delay the onset of corrosion.

These results demonstrate a marked improvement in capacitor reliability using either the labyrinth method or the buffered-ceramic method. To achieve this 500 hours of moisture protection we can extend the methods we have already used. We could either make a

labyrinth package that forces moisture to take a longer path, or we could extend the buffered-ceramic method to several layers. Extending the labyrinth method in this fashion would be quite difficult, as the pattern will get quite intricate. The buffered-ceramic method is quite simple, and we should be able to achieve superior moisture protection through the use of several organic and polymer layers.

6.3 Buffered-ceramic Method Testing and Development

We have decided that the buffered-ceramic method would be the best choice due to its simplicity and the ability to scale it to achieve the desired moisture protection. Now the key questions are which materials to use for this method, and which deposition methods. For the ceramic layer we have chosen PECVD because of its higher deposition rates the ability to control substrate temperature. PECVD oxides and nitrides are frequently used as moisture barriers in the integrated circuit and food packaging industries. In the PECVD system at MIT, we can either deposit Si_3N_4 or SiO_2. To decide which would be a better moisture barrier, we deposited 1000 Å of each material at 100 °C on bare silicon. From examining these films under an optical microscope (Fig. 6.6), we can see that SiO_2 has the lower defect density, and is therefore likely to be a better moisture barrier.

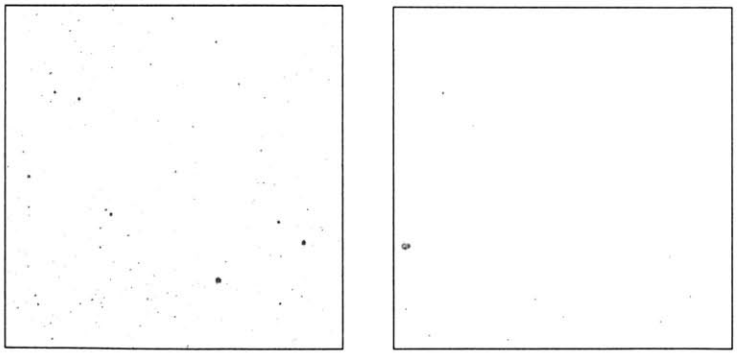

Figure 6.6: Silicon Nitride (Left) and Silicon Dioxide (Right) defects. Magnification is 50x.

We must also choose an appropriate organic material to serve as the buffer layer for these SiO_2 coatings. There are many appropriate materials, as discussed in Ch. 4. The first material that was tried was parylene-c. These coatings were made by using three layers of parylene-c (8 μm each) and two layers of SiO_2 (1000 Å each), as shown in Fig. 6.7. The SiO_2 layers were deposited by PECVD in one set and sputtering in another.

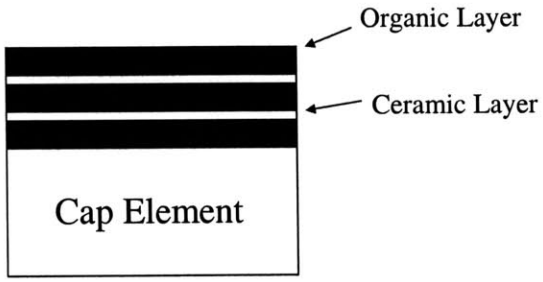

Figure 6.7: Implementation of buffered-ceramic Method

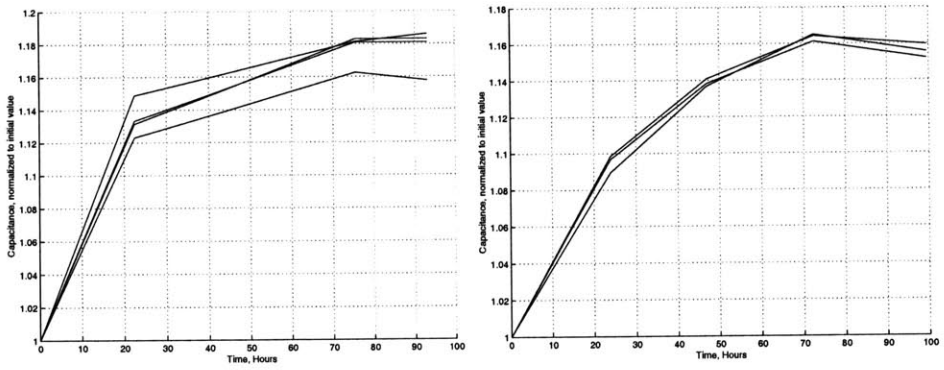

Figure 6.8: Capacitance change of buffered-ceramic coated capacitor w/ Sputtered SiO_2 on parylene (left) and PECVD SiO_2 (right), no voltage applied.

A microscope photograph (Fig. 6.9) of the PECVD version clearly shows the three distinct organic layers. This sample was prepared by using a knife to cut a cross section of the capacitor. The coating has been damaged by the knife, leaving one layer attached to the capacitor and two detached. The capacitor stack is also clearly visible on the left.

Unfortunately, this implementation of the buffered-ceramic method did not succeed (see Fig. 6.8). In fact, this method was not improved by either adding more layers or attaching leads to the capacitors before deposition. Upon investigation, it was discovered that the

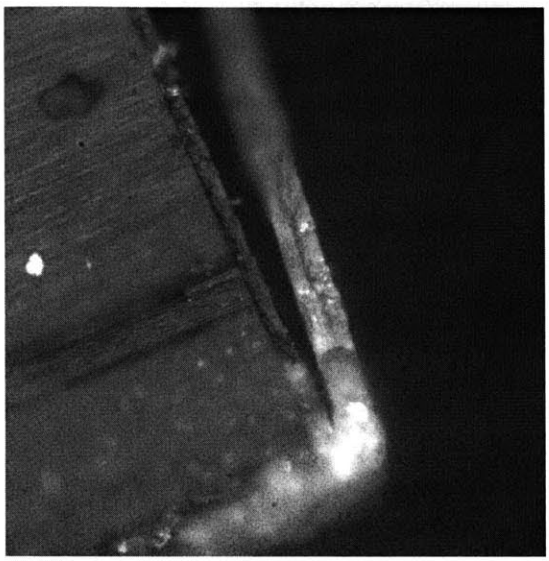

Figure 6.9: Photograph of buffered-ceramic method with parylene

parylene appeared to de-laminate from the surface of the capacitor after being exposed to moisture. It is uncertain whether this problem can be corrected, or whether there are other problems with this technique. It may be possible to improve adhesion of the parylene to the capacitor (or the parylene to the SiO_2) by using an adhesion promoter.

One possible reason why parylene was unsuccessful is because it is a very conformal coating. The parylene layer may be replicating some of the surface roughness of the capacitor, and this roughness may be larger than the thickness of the oxide coating that must be deposited on top of it. Another possible problem lies in the kinetics of parylene film polymerization. Zhao [29] found that thicker parylene films tend to exhibit larger surface roughness than thin films, and found that this roughness can approach 100 Å. Future work could include using an atomic force microscope (AFM) to determine what the actual surface roughness was with our 8 μm films.

Acrylate is another possible organic layer that may be used in the buffered-ceramic method. Acrylate monomers are liquids which are typically cured by electron beam or UV radiation. In this investigation, we elected to use UV radiation to polymerize 1,6 Hexanedioldiacry-

late (HDODA). This was accomplished through the use of 1% weight Benzophenone (BP) photoinitiator, and 1% N Methyl,N Diethanolamine, which acts as a hydrogen donor. This formulation was obtained from Cavitt [30]. Curing of the acrylate occurs by UV induced free radical polymerization, as shown in Fig. 6.10.

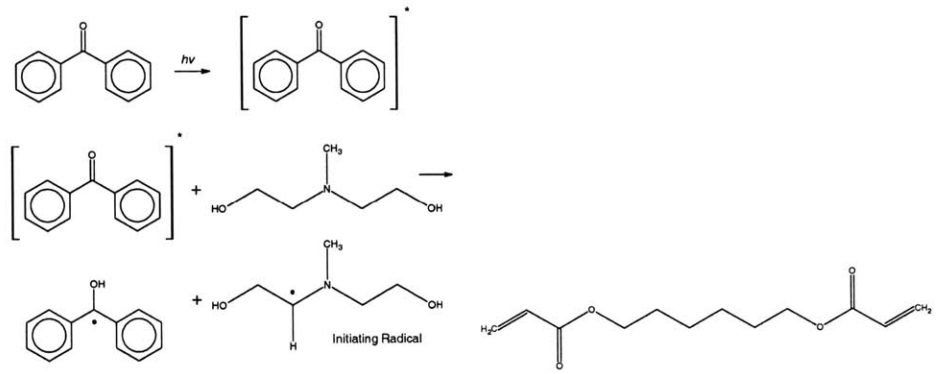

Figure 6.10: UV initiated free radical polymerization (left), 1,6 Hexanedioldiacrylate (right)

After leads were attached, capacitors were dipped in this mixture, and then exposed to UV light. The coating was applied in the same way as in previous buffered-ceramic coatings (Fig. 6.7). Results of humidity testing under 25 V are shown in Fig. 6.11. Despite several attempts, this material system was not successful in protecting the capacitor from moisture ingress. Fig. 6.11 shows that the coating was unable to prevent a loss of capacitance for more than 100 hours in the best case.

Upon curing, the acrylate was found to be rather brittle, and to have poor adhesion to the capacitor. When subjected to moisture, the coating appeared to exhibit yellowing and the acrylate would flake off the capacitor during handling. This would be a significant problem in a real application, and is most likely not something that can be solved by changing the curing parameters. A more flexible polymer material is needed which can stand up to a mechanical stress without breaking. Another problem is the surface of the cured acrylate. Fig. 6.12 shows that the surface of the acrylate is not smooth when cured. Instead, an intricate pattern is created on the surface. This may be causing difficulties for the SiO_2 which must be deposited on a flat surface.

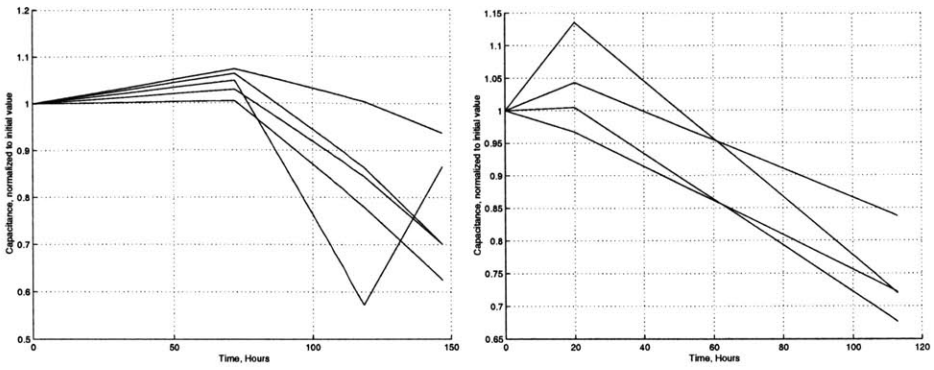

Figure 6.11: Capacitance change of buffered-ceramic coated capacitor w/ acrylate and PECVD SiO_2, 25 V applied. Made with one dip per layer and black light curing (left) and two dips per layer with broadband UV exposure system (right)

Another potential material to use in the buffered-ceramic method is SU8. I fabricated capacitors in the same design as in Fig. 6.7. SU8 2000.1 from Microchem was used (see recipe in table B.3), and an organic layer of approximately 10 μm was built up by three successive dips, followed by baking. A detailed recipe can be found in Appendix B. PECVD SiO_2 was again used for the ceramic layer. Environmental chamber testing results are shown in Fig. 6.13.

First, these capacitors were placed in an environmental chamber without an applied voltage. The results of this test are excellent (Fig. 6.13). The capacitance increased extremely slowly during this test, demonstrating far superior moisture barrier properties than any other barrier coating tested during this investigation. To see the effect of applying a voltage, these capacitors were subsequently baked to remove moisture, and then placed back in the environmental chamber, this time with 25 V applied. This time, the results were extremely disappointing. While a loss of capacitance was prevented for 165 hours, much better performance was expected. It is interesting to note that the capacitance initially rose very quickly in this test - much faster than one would expect based on the test without an applied voltage. This suggests that something happened to the capacitors in between the two tests which ruined their moisture resistance.

Figure 6.12: Acrylate surface morphology, 10x magnification

To determine the cause of this failure, one capacitor from this test was cut open and the cross section viewed under a microscope (Fig. 6.14c). This photograph shows that the coating is extremely thin or even nonexistent at the corners. This was likely caused by the low viscosity of the SU8 used. One possible explanation is that the protective film flexed during the process of baking moisture out of the capacitor, and that these corners were a weak point which cracked and allowed moisture to enter. This problem could be solved by slightly beveling the corners of the capacitor to reduce the contact angle which the SU8 must cover.

Another possible explanation is that the SU8 was not properly cured. This could be caused by either an insufficient UV dose, or an insufficiently long post exposure bake (PEB). If there is residual solvent left in the SU8 layer after curing, then the SiO_2 layer will seal this moisture inside the coating. The SU8 layer could then be softer than expected, which could lead to wrinkles in the SU8 film and destruction of the SiO_2 layer. This problem is currently under investigation. Once this problem is solved we believe that it will be possible to achieve the 500 hour goal for preventing loss of capacitance.

Once this problem is solved, we believe that the buffered-ceramic method using SU8 and PECVD SiO_2 will be a viable means of protecting PML capacitors from moisture. Total

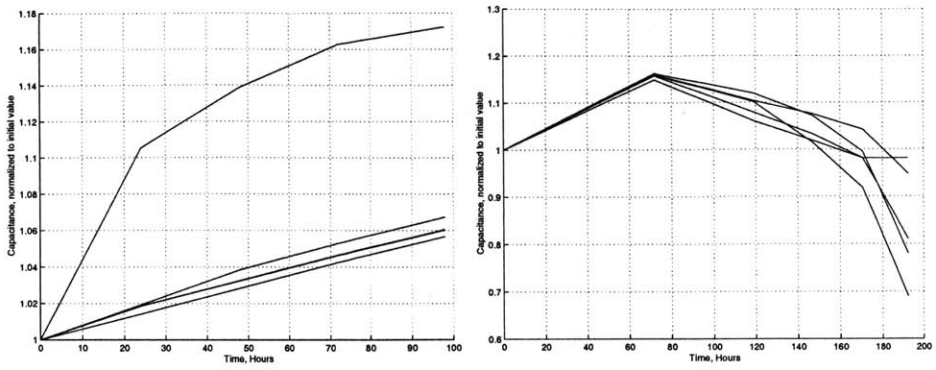

Figure 6.13: Capacitance change of buffered-ceramic coated capacitor w/ SU8 and PECVD SiO_2, without voltage applied (left) 25 V applied (right) and with improved SU8 deposition process.

coating thickness is under 30 μm, as can be see from an SEM image in Fig. 6.14b. The 170 nm oxide layer is also shown expanded in Fig. 6.14a. These SEM images reveal that the oxide layer is adhering to the SU8 layer, and that the package has been constructed as expected.

While this method has not yet been perfected, Fig. 6.15 gives an idea of the protection that could be achieved. In this test, three of the protected capacitors only achieved corrosion prevention for 125 hours. One capacitor behaved as one would expect from the performance of the capacitors without a voltage applied (Fig. 6.13). This capacitor was protected well enough to prevent loss of capacitance for over 250 hours. Upon investigation, it was discovered that the three capacitors that failed in 125 hours exhibited wrinkling of one of the SU8 layers, while the one capacitor that was successful did not exhibit much wrinkling. This suggests that the SU8 buffered-ceramic method could be made more reliable by optimizing the baking times for the SU8, and by achieving a sufficient UV dose. We are currently pursuing improved baking times as a means of making the SU8 buffered-ceramic method more reliable (see Appendix B).

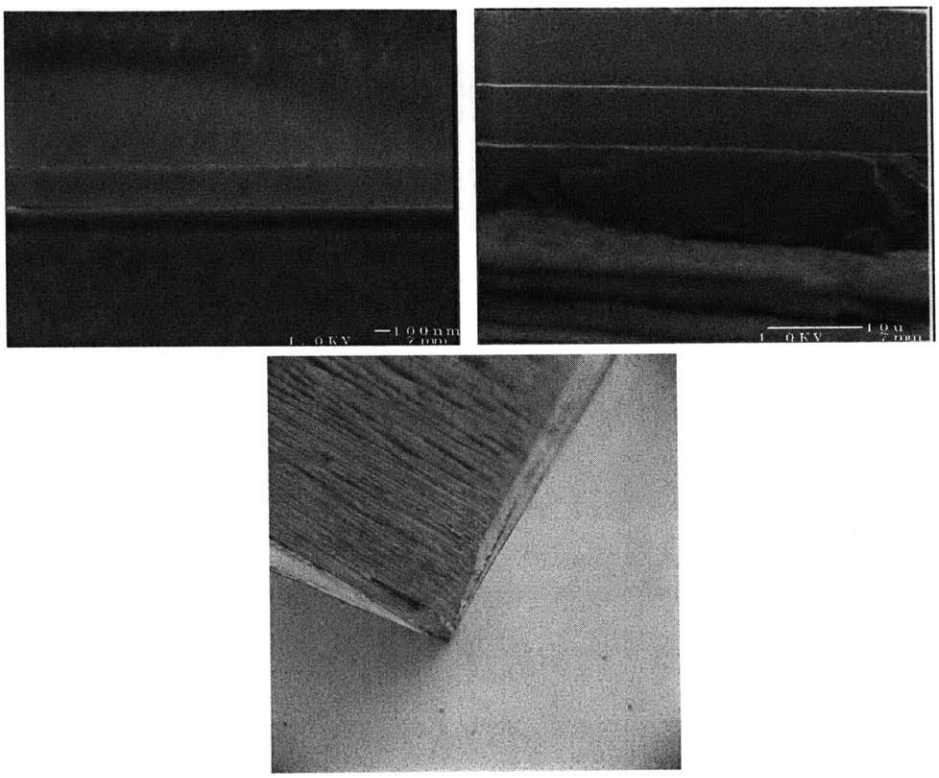

Figure 6.14: a) (top left) SiO_2 layer between SU8 layers. b) (top right) Three layer stack of SU8 alternating with two layers of SiO_2 on top of a capacitor. The top layer ends at the very top of the picture. c) (bottom) Buffered-ceramic w/ SU8 cross section reveals poor corner coverage

.

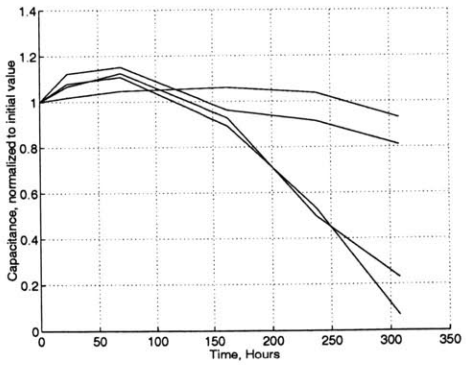

Figure 6.15: Results of Buffered Ceramic method with SU8 (25 V)

Chapter 7

Conclusions

7.1 Introduction

This purpose of this thesis has been to investigate the use of ultra-thin moisture resistant capacitor coatings for passive components. Several novel coatings techniques have been designed, and the resulting packages have been fabricated and tested. These coating techniques have proven successful in improving the moisture resistance of capacitors and enhancing their usable life. This moisture resistance has been achieved while keeping the coating thickness smaller than 30 μm, which is substantially smaller than the specification of 200 μm.

After evaluating several coating materials, deposition techniques, and coating strategies we found that the best performance was achieved by the buffered-ceramic method with SU8 as an organic layer and PECVD SiO_2 as the ceramic layer. With a few modifications, this technique could be feasible for industrial production as a moisture barrier on capacitors. More work on this method is needed to demonstrate that this technique can prevent capacitance loss for 500 hours in accelerated life testing. This specification is very close to being achieved.

7.2 Evaluation of Thesis Objectives and Contributions

The objective of this thesis is to present superior moisture barrier coatings for passive components. As discussed in Ch. 2, ultra-thin coatings are necessary to achieve high capacitance density in SMT capacitors and to limit their parasitic inductance. This investigation has succeeded in developing coatings of less than 30 μm which greatly reduce the rate of moisture ingress. The materials used in these coatings are commercially available, and the deposition process can be theoretically scaled up for mass production.

These coatings have also been tested with an applied voltage to determine if they provide adequate moisture protection to prolong the life of the device. These tests show that a loss of capacitance can be prevented for 200 hours in an environmental chamber test using the full labyrinth method, and that over 250 hours is possible with the buffered-ceramic method. The buffered-ceramic method using SU8 and PECVD SiO_2 has demonstrated superior moisture resistance to the labyrinth method and greater simplicity. We have not yet been able to meet the specification of 500 hours (to prevent loss of capacitance in an 85 °C and 85 % RH environment). Meeting this specification and improving the repeatability of the buffered-ceramic method will be the subject of future work.

7.3 Future Work

Further investigation will focus on increasing the moisture resistance of the buffered-ceramic method with SU8 and PECVD SiO_2. This effort will be directed at increasing the repeatability of this method, in addition to extending the moisture protection by either optimizing the quality of deposited layers or adding more layers. This method must then be developed for coating capacitors which do not have leads attached. Finally, we will explore means for manufacturing this process in a PML capacitor production line.

Appendix A

Coating Preparation

Moisture protection of electronic devices can not be successful without proper preparation. The most important part of preparing the capacitors is to make sure that all of the moisture has been removed from the capacitor prior to coating. If proper precautions are not taken, then residual moisture inside the capacitor will be present for corrosion. Any coating applied will then trap this moisture. Fig. A.1 shows that ambient humidity in a laboratory can cause a substantial amount of moisture to enter a PML capacitor. After baking capacitors to remove moisture, we left them out in the lab in ambient humidity. From capacitance measurements we can see that bare capacitors can soak up moisture from the ambient relatively quickly, and that a protective coating can slow this process. This experiment shows that it is important to store these capacitors in a low humidity environment prior to applying a protective coating, because it does not take long for moisture to get in. To be sure that no moisture is present, bare capacitors should be baked at 90 °C for 12 hours prior to coating.

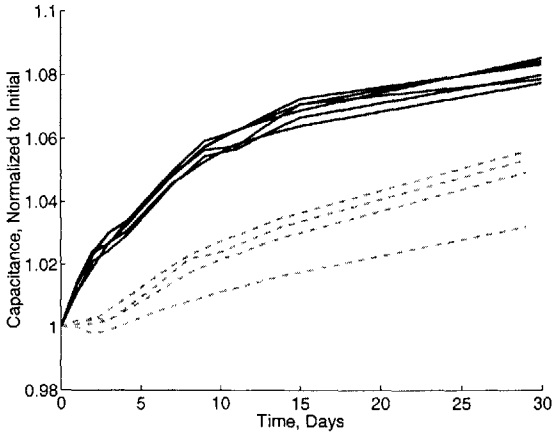

Figure A.1: Effect of Ambient Humidity of 50% on Capacitance. Bare Capacitors - solid lines, and capacitors with Labyrinth - dashed lines

One particularly pernicious effect of trapped moisture is sometimes referred to as the "popcorn effect." This phenomenon occurs when trapped moisture is raised beyond its boiling point. This trapped moisture goes from the liquid to the vapor phase, and the resulting pressure can be great enough to rupture the moisture resistant package. An illustration of

this can be seen in Fig. A.2.

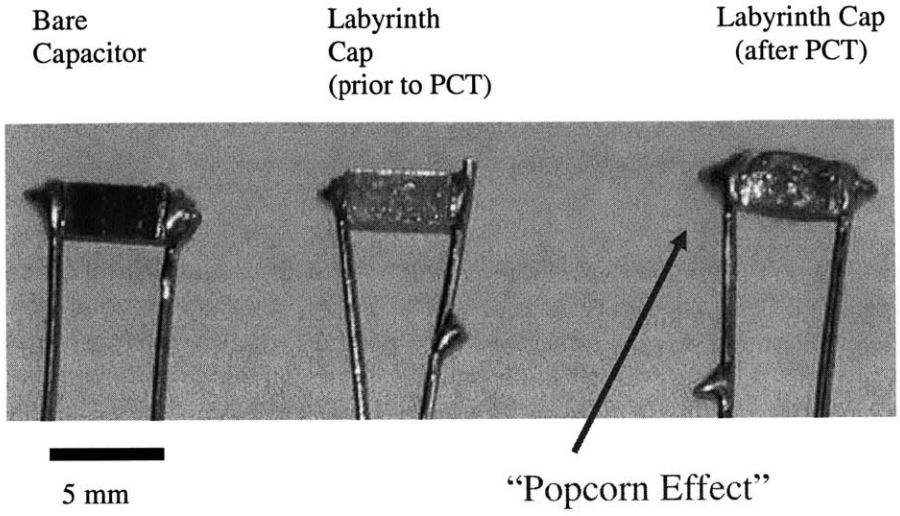

Figure A.2: Illustration of Popcorn Effect

This popcorn effect was caused by the capacitors being left in ambient humidity prior to coating. During the summer months, it was found that this ambient humidity was often greater than 50%. When capacitors were exposed to this environment for several days their capacitance rose significantly.

This problem was solved by baking the capacitors overnight at 90 °C prior to coating, and also by storing the capacitors in a low humidity environment (desiccator). We also investigated using vacuum as a means of extracting the moisture, but baking proved to be much faster.

Another important consideration for coating capacitors is adhesion. For a coating to have good adhesion to the capacitor, it is very important to have a clean surface. In addition, it is helpful to functionalize the surface (i.e. promote the formation of reactive surface groups). Surface functionalization can be accomplished by flame or plasma treatment. We have chosen oxygen plasma treatment because this method bombards the surface with oxygen ions, and aids in removing aluminum pieces that are left by the dicing saw. We found that this method was effective. Surface energy was measured by commercially available dyne pens. Only 1-5 minutes in oxygen plasma was required to increase the surface energy. A much longer time was needed to remove pieces of aluminum (1-2 hours). Plasma power was 50 W. After this long plasma ashing, it is necessary to remove the aluminum particles from the surface. This is done by placing the capacitors in an ultrasonic water bath for 60 seconds. After being placed in this bath the capacitors must be baked several hours to remove this moisture.

Appendix B

Coating Recipes

This appendix presents the detailed deposition parameters for the materials used in this investigation.

Parylene was deposited in PDS 2010 Labcoter 2 (Specialty Coating Systems, Indianapolis, IN). The parameters for this deposition are shown in table B.1.

Table B.1: Parylene-c Deposition

Parameter	Value
Deposition Time	Hours
Dimer Mass	6.5 g
Base Pressure	5 torr
Substrate Temperature	30 °C
Thickness	7.5 μm

SU8 was deposited by dip coating. First, leads were attached to the capacitors. Then they were functionalized in oxygen plasma for 15 minutes. Next, they were dipped in SU8, prebaked at 90 °C, and this process was repeated to build up coating thickness. Then, the capacitors were exposed with broadband UV light. After this, they undergo a post exposure bake (PEB), and possibly a hardbake. Many different temperatures and lengths of time were used for these different steps. The first process that was tried is shown in table B.2. There were several problems with this recipe. For example, a PEB must be done at 90 °C before going to 130 °C. In addition, we found that better coverage of the capacitor was achieved by dipping more than once. The most successful process thus far is shown in table B.3, and was used to make the capacitors for which the results are shown in Fig. 6.15.

Table B.2: SU8 Dip Process with SU8 2010

Step	Temperature (°C)	Time(min)	Misc.
Type			SU8 2010
Prebake	90	5	
Number of Dips			1
Further Prebake			none
Expose	25	1	once
PEB	130	20	
Hardbake			

These layers did show some cracking and wrinkles, and I believe they could be improved. I believe a superior recipe to be that of table B.4. The most important elements are that

Table B.3: SU8 Dip Process 1 (SU8 2000.1)

Step	Temperature (°C)	Time(min)	Misc.
Type			SU8 2000.1
Prebake	90	5	
Number of Dips			3
Further Prebake	90	20	
Expose	25	1.6	once
PEB	90	5	
Hardbake	130	180	

the capacitors receive sufficient UV dose, and that the PEB is long enough to remove all solvents and gases from the SU8.

Table B.4: SU8 Dip Process 2 (SU8 2000.1)

Step	Temperature (°C)	Time(min)	Misc.
Type			SU8 2000.1
Prebake	90	2	
Number of Dips			3
Further Prebake	90	3	
Expose	25	1	4 times - once each side
PEB and Hardbake	Slow ramp from 25 to 130	60	No fast temp. steps

The process for acrylate film dipping and crosslinking is discussed in Ch. 6.

Table B.5: PECVD SiO_2 Deposition

Parameter	Value
Deposition Time	3 minutes
Gas Flow	350 sccm SiH_4, 250 sccm NO_2
RF Power	25 W
Substrate Temperature	100 °C
Pressure	500 mtorr
Thickness	1050 Å
Refractive Index	1.43

Metals were deposited for use in the labyrinth method. Sputtering was generally too hot for the organic layer upon which the sputtered material was deposited. Sputtered copper deposition parameters are detailed in table B.8. Evaporated aluminum parameters are as shown in table B.9.

Table B.6: PECVD Si_3N_4 Deposition

Parameter	Value
Deposition Time	15 minutes
Gas Flow	260 sccm SiH_4, 500 sccm He, 36 Sccm NH_4
RF Power	25 W
Substrate Temperature	100 °C
Pressure	500 mtorr
Thickness	1200 Å
Refractive Index	1.95

Table B.7: Sputtered SiO_2 Deposition

Parameter	Value
Deposition Time	60 minutes
Gas Flow	50 sccm Ar, 10 sccm O_2
RF Power	200 W
Substrate Temperature	unknown, water cooled
Thickness	950 Å
Refractive Index	1.43

Table B.8: Sputtered Cu Deposition

Parameter	Value
Deposition Time	20 minutes
Gas Flow	60 sccm Ar
RF Power	300 W
Substrate Temperature	unknown, water cooled
Thickness	$\simeq$300 nm

Table B.9: Evaporated Al Deposition

Parameter	Value
Deposition Rate	5 Å/s
Current	0.28 A
Substrate Temperature	unknown, above room temp
Thickness	0.5 μm

Bibliography

[1] Ian W. Clelland and Rick A. Price, "High voltage multilayer polymer capacitors fill technology gap", in *IEEE Industry Applications Society Annual Meeting*, Oct. 1997.

[2] V. Gordiyenko S. Pirzada A. Yializis, H. Russel, "High temperature polymer multilayer capacitors", in *Capacitor and Resistor Technology Symposium*, Mar. 2000.

[3] David G. Shaw Angelo Yializis, Gary L. Powers, "A new high temperature multilayer capacitor with acrylate dielectrics", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 12, no. 4, Dec. 1990.

[4] A.M. Kern C.R. Sullivan, Y. Sun, "Improved distributed model for capacitors in high-performance packages", in *IEEE Industry Applications Society Annual Meeting*, Oct. 2002.

[5] C.R. Sullivan and D.J. Perreault, "Investigation of advanced packaging techniques for PML capacitors".

[6] C.R.Sullivan and D.J. Perreault, "Study of advanced packaging for PML capacitors".

[7] C. W. Reed and S. W. Cichanowski, "The fundamentals of aging in HV polymer-film capacitors", *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 1, no. 5, pp. 904–922, Oct. 1994.

[8] James Licari, *Plastic Coatings for Electronics*, McGraw- Hill, 1970.

[9] D. F. Taylor, "On the mechanism of aluminum corrosion in metallized film AC capacitors", *IEEE Transactions on Electrical Insulation*, vol. 19, no. 4, pp. 288–293, Aug. 1984.

[10] Michael Pecht, *Handbook of Electronic Package Design*, Marcel Dekker.

[11] Michal Tencer, "Moisture ingress into nonhermetic enclosures and packages. A quasi-steady state model for diffusion and attenuation of ambient humidity variations", in *Electronic Components and Technology Conference*, Mar. 1994.

[12] Haleh Ardebili et al, "A comparison of the theory of moisture diffusion in plastic encapsulated microelectronics with moisture sensor ship and weight-gain measurements", *IEEE Transactions on Components and Packaging Technologies*, vol. 25, no. 1, Mar. 2002.

[13] E.H. Wong et al, "Non-fickian moisture properties characterisation and diffusion modeling for electronic packages", in *Electronic Components and Technology Conference*, 1999.

[14] A. M. Simoes A. S. Castela, "Assessment of water uptake in coil coatings by capacitance measurements", *Progress in Organic Coatings*, vol. 46, pp. 55–61, 2003.

[15] Burrows et al, "Ultra barrier flexible substrates for flat panel displays", *Displays*, vol. 22, no. 2, pp. 65.

[16] Hal Greenhouse, *Hermeticity of Electronic Packages*, Noyes Publications, 2000.

[17] Marc Madou, *Fundamentals of Microfabrication*, CRC Press, 1997.

[18] Stanley Wolf and Richard Tauber, *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press, 1986.

[19] Stanley Wolf, *Silicon Processing for the VLSI Era*, vol. 2, Lattice Press, 1990.

[20] Winnie Tong and Anette Teng, "Moisture diffusion monitoring in globtop encapsulant with microdielectric sensors", in *IEEE International Symposium on Electronic Materials and Packaging*, Nov. 2000.

[21] Mehmet R. Dokmeci Babak Ziaie, Jeffery A. Von Arx and Khalil Najafi, "A hermetic glass-silicon micropackage with high density on-chip feedthroughs for sensors and actuators", *Journal of Microelectromechanical Systems*, vol. 5, no. 3, pp. 166–179, Sept. 1996.

[22] Michael Pecht et al, *Electronic Packaging Materials and their Properties*, CRC Press, 1999.

[23] J.M. Shaw et al, "Negative photoresists for optical lithography", *IBM J. Res. Develop.*, vol. 41, no. 1, Jan. 1997.

[24] M. Despont et al, "High-aspect-ratio, ultrathick, negative-tone near-UV photoresist for MEMS applications", in *The Tenth Annual International Workshop on Microelectromechanical Systems*, 1997.

[25] Ru Feng and Richard J Farris, "Influence of processing conditions on the thermal and mechanical properties of SU8 negative photoresist coatings", *Journal of Micromechanics and Microengineering*, vol. 13.

[26] Michael Lucey, "UV curable coatings for electronic components", *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 17, no. 2, pp. 326–333, 1994.

[27] Cookson Electronics, *Parylene Conformal Coating Specifications and Properties*, Web site of Cookson Electronics, May 2004.

[28] Pal Nemeth, "Accelerated life time test methods for new package technologies", in *24th International Spring Seminar on Electronics Technology*, May 2001.

[29] Y.P. Zhao et al, "Kinetic roughening in polymer film growth by vapor deposition", *Physical Review Letters*, vol. 85, no. 15, pp. 3229, Oct. 2000.

[30] T. Brian Cavitt et al., "Initiation of 1,6-hexanedioldiacrylate polymerization by three component photoinitiators incorporating 2,3-dimethylmaleic anhydride", *Polymer*, vol. 45, pp. 1119, 2004.