Design and Fabrication of an Addressable MEMS-Based Dielectrophoretic Microparticle Array

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in Partial Fulfillment of the Requirements for the Degree of Master of Science

ABSTRACT

At present, no widespread tool or technology is available to enable active screening of complex cellular phenotypes. Such desired screens mandate sorting of subsets of cells within an overarching population based upon concerns such as morphological characteristics and/or dynamic processes witnessed in localized regions of individual cells over specified time courses. This thesis presents a sequence of design, simulation, fabrication, and testing routines exercised in demonstrating a first-round, proof-of-concept cytometer offering new avenues for addressing the investigation of such screening processes. The methods and tools outlined in this report employ Microelectromechanical Systems (MEMS) technologies to produce electrode structures sized in accordance with single-cell dimensions that afford viable sorting of individual cells through a novel row/column addressability scheme. This addressing scheme and its associated electrode configurations avoids dependencies upon active on-chip transistor-based devices. Implementing such a "simplified" design reliant upon voltage differences between different sets of activation electrodes framed the problem in the context of an approachable academic research endeavor. This report presents two distinct bioMEMS device implementations incorporating negative and positive dielectrophoretic forces for single-cell capture and manipulation. Offered here is the first-known demonstration of the scalability of dielectrophoretic cell trapping technologies where the interconnect requirements grow proportional to $\sqrt{n}$ in nxn trapping grids. This reduction in electrical ties to off-chip circuitry renders an operative tool for biological screening assays with the potential for demonstrating sorting operations on populations sizeable enough to conduct functional genetic surveys.

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List of Symbols
(provided in order of appearance in the text)

Symbol	Definition
F_{DEP}	Dielectrophoretic force
ε_{media}	Complex electrical permittivity of the medium surrounding a particle
R	Radius of a given spherical particle
Re	Notation for the real component of a complex number
CM	Clausius-Mossotti factor
ω	Angular frequency of the driving electrodes
ε_{body}	Complex electrical permittivity of the particle in suspension
E	Electric field
$\tilde{\varepsilon}$	Electrical permittivity
$\tilde{\sigma}$	Electrical conductivity
$\varepsilon_{body,eff}$	Effective complex electrical permittivity of a shelled structure
C_{mem}	Complex membrane capacitance
$\tilde{C}_{mem}$	Membrane capacitance
$\tilde{G}_{mem}$	Membrane conductance
ε_{mem}	Membrane permittivity
Δ	Membrane thickness
σ_{mem}	Membrane conductivity
$\overset{\overset{-}{\vdots}}{\overset{=}{p}}{}^{(n)}$	Multipolar induced moment tensor
F_i	Force in the i direction
E_m, E_i^*, E_n	Electric field in the m, i, and n directions
ε_o	Permittivity of free space
ρ	Charge density
J	Current density
μ_o	Permeability of free space
Φ	Scalar electric potential
Q	Injected thermal energy, heat
σ	Electrical conductivity
$R_{t,cond}$	Conductive thermal resistance
L_i	Heat flow path length
k_i	Thermal conductivity
h_{eff}	Effective heat transfer coefficient
q_x''	Heat flux
$T_{s,i}$	Temperature at a given surface
J_i	Current density on side i of a surface
V_o	Applied nominal peak-to-peak voltage amplitude
σ_{media}	Conductivity of the media
V_{tm}	Transmembrane voltage
G_{mem}	Complex membrane conductance
σ_{cyto}	Electrical conductivity of the cytoplasm
ε_{cyto}	Electrical permittivity of the cytoplasm
τ	Time constant
ρ_{cyto}	Electrical resistivity of the cytoplasm
ρ_{media}	Electrical resistivity of the cell culture media
E_{tm}	Transmembrane electric field
$normE$	Normalized magnitude of the electric field
Ex, Ey, Ez	Electric field in the x, y, and z directions
C_{dox}	Capacitance of a deposited oxide layer
V_{IN}	Drive voltage
V_{OUT}	Voltage "felt" by a microparticle in the media
R_{med}	Electrical Resistance of the media
C_{tox}	Electrical capacitance of the thermal oxide layer
R_{Si}	Electrical resistance of the silicon substrate

Chapter 1: Introduction, Background, and Project Focus

Introduction

This thesis provides a description of the underlying theory, design and fabrication techniques needed to develop a novel, addressable array of electrodes for manipulating micron-scale particles. In this first chapter I set the stage for the remainder of the document by providing an overarching perspective of project goals as well as background context to help the reader understand the project's application space and the approach I adopted to build upon earlier work done in the field of dielectrophoretic particle sorting.

1.1. Genetic Screening and Complex Phenotypes

Investigating and noting distinctions in specific characteristics expressed by individual cells, viruses, microorganisms and the like within given populations is known as screening. Attempts to link observable physical or biochemical characteristics of an organism (phenotypes) to the underlying genetic sequences causing their expression are surveys called genetic screens [1]. Such screens have helped biologists understand various aspects of cell function. Details related to cell-cycle analysis, apoptosis, senescence, embryonic patterning, and the secretory pathway have all been monitored using a host of different genetic screening techniques [1, 2].

All genetic screens (dominant gain-of-function, recessive loss-of-function, complementation and otherwise [1]) incorporate three fundamental components. First, the genetic program within the cell is modified in some manner – either by using a library of induced mutations linking a suite of genes to specific phenotypic behaviors (forward screen) or by taking a known, altered gene and reintroducing it to the cell to test its effects (reverse screen). Next, the cells expressing the phenotypes of interest for a given assay are located (often tracked using molecular probes and/or tags engineered to fluoresce in conjunction with specific biochemical processes) within the overall cell population. Lastly, those cells expressing the phenotype of interest are sorted and separated from the background population of cells such that the alterations in their genetic code responsible for the expressed phenotype can be pinpointed.

Biological cells are the most fundamental living units demonstrating autonomous replication. This miniaturized "system-in-a-box" perspective offers a powerful platform for conducting genetic research. The cell thus serves as a tool for gaining insight regarding broader concerns such as developing models for human diseases and responses to drug treatments.

In the aftermath of the Human Genome Project, researchers in industry and academia face the challenge of managing an overabundance of genetic sequencing information and simultaneously pairing it with an understanding of how specific genes function in the human body. Making this connection will slowly unveil many of the mysteries and complexities governing biological processes that affect our lives both acutely and long-term from cradle to grave. With new technologies such as RNA-interference [3] the door is open for the realization of systematic genome-wide functional screens that target only the genes tied to specific cellular behaviors. Most current screening techniques only provide information on which sets of genes serve as potential players in a given cellular process. In this new era of genomics and systems biology, developing novel screening technologies that provide parallelized information processing and high through-put data collection will prove essential for assigning gene functions.

The work I outline in the remainder of this thesis offers one approach to expand the capabilities afforded by traditional screening methods by enabling the investigation of complex phenotypes. Complex phenotypes include cell characteristics and behaviors that demonstrate both temporal and spatial variations within the cell [1, 3, 4]. They can also encompass details tied to discrimination and sorting based upon whole-cell characteristics related to such items as morphology and intracellular organization. Understanding where, when, and for how long specific behaviors occur within individual cells can provide unparalleled insight regarding the dynamic nature of certain cell processes. Sorting on the basis of complex phenotypes requires a means for better extraction and utilization of information provided by the suite of fluorescents tags and reporter gene technologies developed in recent years. These markers, which activate in coordination with the appearance of distinct phenotypes and monitor various intracellular functions [5, 6], offer a host of new avenues for conducting genetic screens if optical microscopy methods are modified and augmented to help identify and sort in a complementary fashion. Largely parallel, real-time imaging of gene expression and specific cellular events in individual cells and it's subsequent use as a trigger for making screening decisions is a possibility not out of question. My thesis is a first-round, proof-of-concept model for demonstrating this overarching goal.

1.2. Approaches for Conducting Genetic Screens

In general, two separate paths have been explored for conducting optically-based genetic screens. One approach has involved flow cytometry [7]. This method pushes cells through a narrow channel in single file where they pass a discrete optical detection and interrogation sensor. The sensor signals a sorting device downstream to push specific cells into various output channels. The other approach has been the use of microscopy techniques. In other words, attributes that can be observed visually through direct inspection or image capture and analysis are used to classify cell types and/or behaviors.

Flow cytometry has been effective for sorting cells tagged with whole-cell fluorescent markers and in providing high-throughput data collection. Some of the newer flow cytometry machines on the market, including the Vantage SE (BD Biosciences), the Altra (Epics), and the MoFlo (Cytomation, Inc.) report dead-times associated with measurement acquisition on the order of 5-10μs thus enabling sorting rates on the order of 25,000 to 60,000 cells/s [7]. This method despite offering advantages in the form of rapid data collection, requires high system pressures that pose deleterious effects on cell viability and ultimately constrain which types of cells can be surveyed with the technology. It further offers no avenue for imaging the cells under investigation and therefore sorting based upon morphological and intracellular distinctions in a cell population is prevented using flow cytometry. This approach offers no mechanism for trapping individual cells before or after sorting which thereby prohibits the examination of the same cell at different points in time. Screening for complex phenotypes is not easily afforded when considering this technique.

Microscopy methods alternatively afford the interrogation of both spatially and temporally variant cell characteristics yet they lack the ability to viably separate cells from the bulk population after imaging. Isolating distinct cell subpopulations is often essential for extracting genetic content. More recently developed microscopy techniques, such as laser capture microdissection, have proven useful for separating and analyzing fixed cells [8]. At present, viable isolation has been seen with Bio-Rad's Clonis tool [9], but no automated strategies for this operation are readily available. This type of separation is desirable in many cases as it preserves the cell line and permits continued growth in further investigative assays.

1.3. Project Purpose, Focus, and Application Space

The work detailed in this thesis combines some of the benefits and advantages of flow cytometry with those characteristic of microscopy techniques to create a new tool to image and also viably isolate single cells. In the remainder of this report I present a novel first-generation hardware design implementation which, upon expansion in subsequent developmental iterations, could screen large numbers of cells in a timely fashion. My device serves as a platform for trapping, imaging, and viably sorting individual cells located within an electrically-addressable row/column-mapped trap site matrix. I present a new technology for analyzing complex phenotypes expressed by single cells screened from a larger population.

My screening cytometer offers capabilities in many application spaces. As one example, fluorescent probes incorporating fluorescence resonant energy transfer (FRET) techniques show shifts in emission wavelengths upon activation [6]. Monitoring the changes in wavelength mandates screening techniques that can investigate the same cell at separate points in time. Additionally, a useful investigation of the response of fluorescent reporters tied to functions localized to specific organelles within the cell could involve the study of the secretory pathway through the use of vesicular stomatitis virus G strains tagged with green fluorescent protein markers (VSVG-GFP).

1.4. General Approach

A global perspective of my screening cytometer design is outlined in Figure 1-1. The system implements a series of row and column electrodes linking to individual sites in a microparticle trapping grid. Stock solutions are channeled across this array by way of an overriding microfluidic flow chamber. These solutions introduce cells or other small spheroid bodies into the device where they are trapped by non-uniform electric fields at the row and column electrode intersections. These trap sites are organized in a tightly packed and easily viewable (via microscope) two-dimensional area. After trapping items in the grid, an optical survey is conducted to locate sites containing objects for release and downstream capture. These objects can take the form of live mammalian cells demonstrating mutant responses to prescribed input stimuli or simple polystyrene beads stained with a particular dye. The chosen microparticles are then individually released from the trapping grid by grounding their associated row and column electrodes. This deactivation routine squelches the electric field at the necessary capture sites thus eliminating the localized holding capabilities for the selected items.

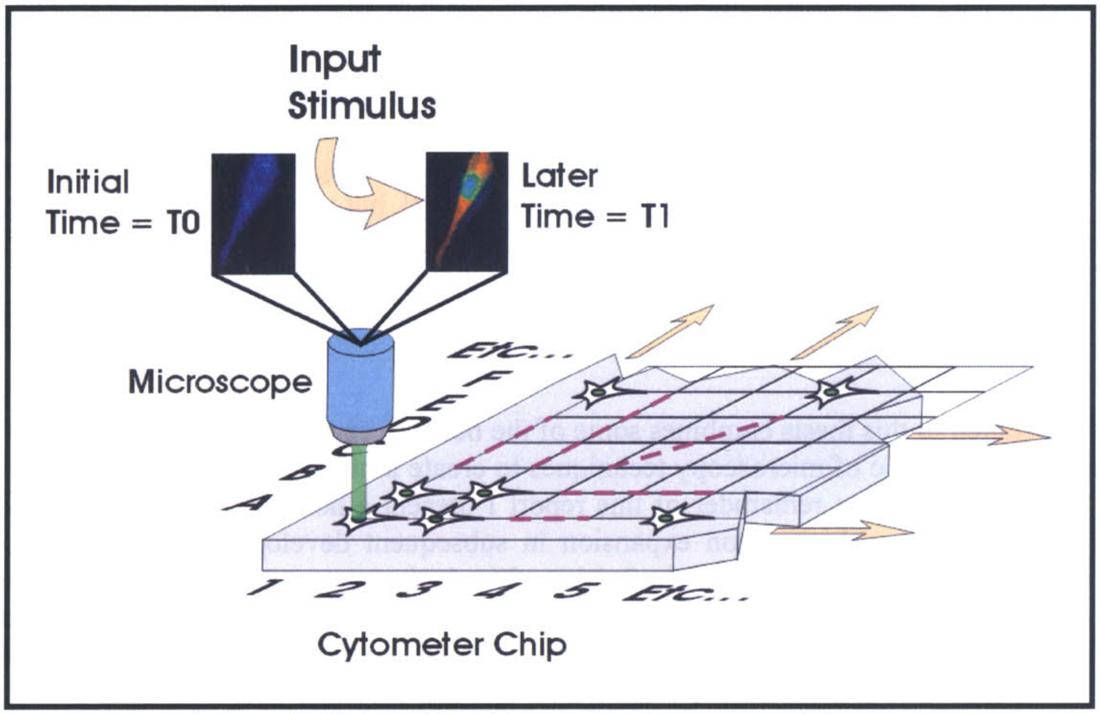


Figure 1-1: This image provides a bird's eye perspective of the DEP chip in operation highlighting the addressable grid layout. To select individual cells within the trap array a given row (ex. E) and column (ex. 3) pair of electrodes are grounded. All cells located on the same row and column are held in place with "half-strength" traps while the remaining sites in the field are maintained at "full-strength".

1.5. Components of an Ideal Design

A chief concern for this project was the issue of scalability. Avoiding the use of control lines that are unique to each site in the array was essential for approaching this design goal. An inability to sidestep such a situation creates cumbersome interconnect requirements for the large trap matrices needed for genetic screens. Interconnect requirements should thus scale in a manner that increases less aggressively than the linearly proportional dependency that would occur when specific unique control lines are mapped to individual trap sites. In an ideal design, each trap, regardless of how it is electrically connected to the outside world, operates without disrupting the holding characteristics of surrounding traps. Such being the case, limitations may easily arise when considering trap density issues in planning trapping footprints. The ideal design would balance out the concern for trapping many cells in a small area with the tendency for individual trap sites to assert negative operational effects on their neighbors.

Any design chosen for the capturing, imaging, and sorting device should use traps that afford reliable single-cell capture. If more than one cell is held in a given location within the trap matrix, activating or deactivating individual trap sites will not offer the selectivity or resolution tolerance needed for effective genetic screens. In the case of clumped cells an ideal design offers a mechanism for either preventing their entrance into the trap matrix all together, an avenue for dissociating them prior to their interaction with trap sites, or a specialized trap design with a potential energy holding well tuned to somehow exclusively trap lone cells while seeming transparent to larger groups of cells. This last feature essentially amounts to the integration of a high-pass filtering mechanism.

Trapping in a two-dimensional, grid-based array requires a layout where the individual trap geometries permit loading of all sites in the matrix. In other words, the first set of traps exposed to cells fed into the device should not promote device clogging or prevent subsequent traps further downstream from filling properly.

The design should provide the most accommodating artificial cellular environment possible, and should not induce dramatic alterations of "normal" cell behavior or function. Also, because many cells require surface attachment for normal function, the cell holding scheme must permit surface/membrane interactions after particle capture.

A truly ideal design would explore the full breadth of available microfabrication technologies available on the market and would not face limitations tied to cost or machine contamination issues. For the sake of pragmatism I designed my process to conform to the set of constraints imposed by utilizing the selection of machines and their associated cross-contamination constraints available within the confines of the Massachusetts Institute of Technology (MIT) Microsystems Technology Laboratory (MTL). This approach provided access to a wide variety of different manufacturing technologies which afforded an adequate amount of design flexibility while simultaneously ensuring that the project aims were reasonably practical and that the initiative fell within the sphere of plausible academic research endeavors.

1.6. Single-cell Control and Manipulation

Technologies capable of probing the length scales characteristic of individual mammalian cells are essential for single-cell manipulation in my screening cytometer. Possible approaches for positioning and holding cells could incorporate optical, physical, or electrical forces either in isolation or in some appropriate combination [10]. Optical tweezing technologies, where focused laser beams subject micron-scale objects to forces on the order of picoNewtons (pN) have been used by numerous research groups to perform studies ranging from the analysis of mechanically induced growth mechanisms in individual single bone and cartilage cells [11] to the establishment of optical lattices capable of separating distinct cell populations based upon size considerations [12].

A plethora of microwell structures incorporating fabrication methods as diverse as silicon bulk micromachining [13] and selective wet etching of the cores of bundled, extruded fiber optic cables [14] have employed physical means to position cells in prescribed locations. Further mechanical manipulations are manifested in a surfeit of innovative patch clamping devices that rely upon the use of carefully controlled pressure differences on separated sides of physical barriers with linking through-holes smaller in size than the target capture cells [15, 16]. Electroporation, transfection, bioprocess monitoring, and even controlled cell-fusion studies have relied upon these sorts of approaches for positioning individual cells. Even micro-bubble generation [17] through controlled, localized fluid boiling has offered means for single cell operations. Despite the large suite of benefits afforded by the methodologies noted above, scaling these techniques to form larger addressable arrays with sorting and isolation functions remains an unsolved problem.

In general, electrically-based forces take the form of either Coulombic interactions exerted on charged molecules present on cell membranes [18] or dielectrophoretic (DEP) forces that interact with induced dipoles [19, 20]. Isoelectric focusing and capillary electrophoresis [4], which separate heterogeneous mixtures of different species, as well as, electro-osmotic flows [16], where bulk fluid movement is generated using an applied electric field, are all demonstrations of interactions that rely upon the presence of charged bodies. These specific techniques are constrained to use direct current (DC) fields to maintain a constant force polarity. This limitation often results in the onset of electrochemical reactions at the electrodes used to generate the fields, which can present negative effects on objects migrating to or present in the vicinity of the electrodes.

In the case of my screening device, DEP forces are most attractive for single cell manipulations. They permit scaling, while offering the ability to avoid electrochemical reactions at the electrodes due to an ability to use alternating current (AC) fields. As is discussed more rigorously in subsequent sections, DEP forces maintain their polarities despite being generated using sinusoidal voltage drives. DEP-techniques additionally offer the potential for implementing stable non-contact traps. Additional to these benefits is the fact that DEP forces can be activated individually through the addressing scheme later outlined in this report. This characteristic proved to be a major deciding factor for choosing to use a dielectrophoretic approach in the design work I performed for my thesis.

1.7. Dielectrophoresis

As mentioned in the preceding section, my thesis employs dielectrophoretic forces for single cell control. Such forces rely upon the existence of spatially non-uniform electric fields that generate asymmetric pushes and pulls on the induced dipoles of beads, cells, and other discrete polarizable bodies. The specific properties of the media, particle, and electric field dictate whether the particle will migrate toward sites of maximum field intensity (positive DEP or p-DEP) or toward sites of minimum field intensity (negative DEP or n-DEP) [19].

Advantages and disadvantages are associated with the two different types of DEP forces. For biological screening purposes, highly conducting solutions, such as DMEM-based media, permit only n-DEP manipulations. This condition endorses cytometer designs that rely upon n-DEP-based trap arrays. In contrast, p-DEP traps mandate the use of low-conductivity buffers. Suspending cells in such solutions may create unsuitable environmental conditions for investigating cell function. Additionally, for a given electric-field gradient, a p-DEP force can be up to twice as strong as an n-DEP force. This condition suggests, and has been supported by some of the simulation work I ran for this project, that it may be fundamentally more difficult to create a stable n-DEP trap geometry with holding characteristics comparable to a p-DEP design. Lacking a best option for the type of DEP forces to incorporate, I worked to develop two discrete designs for the cytometer have each of which incorporated one of the two distinct approaches for cell capture and containment.

To best understand many of the specifics underlying DEP force mechanisms, it is instructional to survey the presiding physics involved and their associated mathematical descriptions. Figure 1-2 (left side) shows an image of two parallel plate electrodes [21]. A charged body and an electrically neutral body are positioned inside of the uniform electric field generated between the two plates. The negatively charged particle experiences a net Coulombic force resulting from a repulsion from the negative upper electrode and an attraction to the positively charged lower electrode. On the other hand, the neutral body experiences no net force since its induced dipole is perfectly symmetric. The upper electrode attracts positive charges to the top of the particle which are exactly balanced out by the negative charges induced by the lower electrode on the bottom side of the particle. This balance prevents the particle from experiencing any net force and therefore maintains its position inside of the electric field.

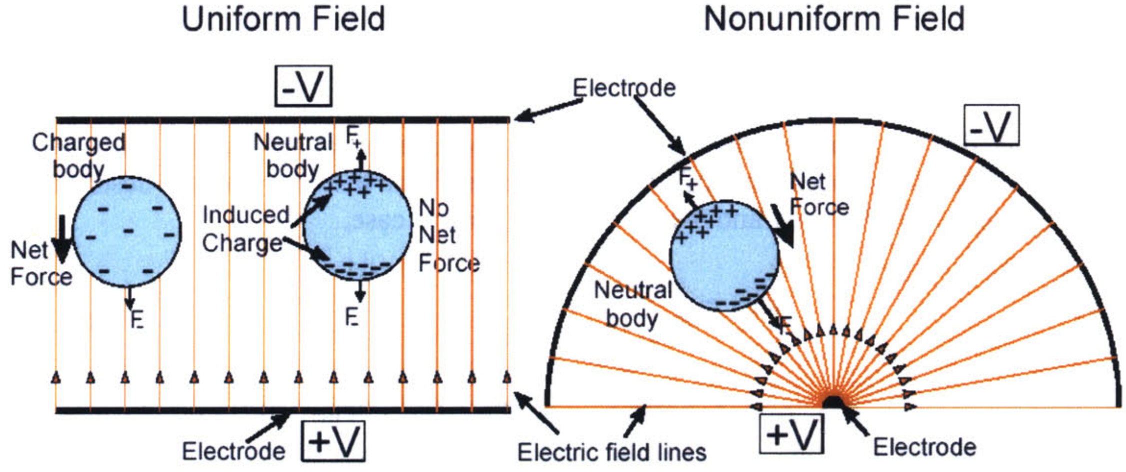


Figure 1-2: Neutral bodies experience no net force in the presence of uniform electric fields due to the generation of spatially symmetric dipoles. In non-uniform field environments neutral bodies experience induced charges which are unbalanced and result in a net force.

The right side of Figure 1-2shows a contrasting situation wherein an electrically neutral particle is located inside of a spatially non-uniform electric field. As was the case for the uniform field condition, a dipole is also induced here. The difference in this situation is that the induced dipole is not in perfect balance across the neutral body. This asymmetry subjects the neutral body to a net force that is either parallel or anti-parallel to the field lines in the neighborhood of the particle.

If the particle inside the non-uniform electric field is assumed to be spherical in shape, and only influenced by the induced dipole the mathematical expression, originally developed by Pohl [22], for the DEP force is as follows [23]:

$$F_{DEP} = 2\pi\varepsilon_{media} R^3 \operatorname{Re}\left\{ CM\left(\omega, \varepsilon_{body}, \varepsilon_{media}\right) \cdot \nabla \left|E\right|^2 \right\} \qquad \textbf{[Eqn. 1-1]}$$

Here ε_{media} is the complex electrical permittivity of the fluid surrounding the particle, R is the radius of the body, CM is a term known as the the Clausius-Mossoti (CM) factor, ε_{body} is the complex electrical permittivity of the body in suspension, and E is the electric field generated between the electrodes. Several interesting features relate to this description for the dielectrophoretic force. First, the force scales with the cube of the particle radius and the square of the gradient of the electric field. These conditions indicate that larger bodies experience greater DEP forces and that a simple doubling of the voltage applied across a set of electrodes in a given set-up results in a fourfold increase in the net DEP force.

The CM factor is the only term in the equation that depends upon the driving frequency of the electrodes in the system. For the case of a spherical body of uniform composition this term is expressed mathematically as [23]:

$$CM = \frac{\varepsilon_{body} - \varepsilon_{media}}{\varepsilon_{body} + 2\varepsilon_{media}} \qquad \textbf{[Eqn. 1-2]}$$

This equation is derived from an evaluation of the Laplace equation for the particle-media system. The frequency dependence of this term stems from the expressions describing the complex permittivities of the body and media. For the general case,

$$\varepsilon = \tilde{\varepsilon} + \frac{\tilde{\sigma}}{j\omega} \qquad \textbf{[Eqn. 1-3]}$$

where $\tilde{\varepsilon}$ denotes permittivity and $\tilde{\sigma}$ indicates conductivity. The j is an indicator of the complex term while the ω marks the frequency dependence. The CM factor can vary between values of -0.5 and 1. Its ability to switch signs is the sole factor determining whether the DEP force is positive or negative.

Biological cells are not homogeneous in nature thereby calling for a more involved description of the CM-factor controlling the associated dielectrophoretic forces. To remedy this challenge the cell can be considered as a structure with a core displaying one set of electrical characteristics and an outer shell maintaining another set. Again applying the Laplace equation to match boundary conditions across the composite body, a single effective permittivity term can describe the nested dielectric structure of the mammalian cell. For a full CM-factor equation describing the mammalian cell, the following expression [23]

$$\varepsilon_{body,eff} = \frac{C_{mem} R \varepsilon_{media}}{C_{mem} R + \varepsilon_{media}} \qquad \textbf{[Eqn. 1-4]}$$

is simply inserted into the position held by the ε_{body} variable in the homogeneous spherical model. Here C_{mem} is the complex membrane capacitance defined as

$$C_{mem} = \tilde{C}_{mem} + \frac{\tilde{G}_{mem}}{j\omega} \qquad \textbf{[Eqn. 1-5]}$$

where $\tilde{C}_{mem}$ and $\tilde{G}_{mem}$ are the cell membrane capacitance and conductance, each described by $\tilde{C}_{mem} = \varepsilon_{mem} / \Delta$ and $\tilde{G}_{mem} = \sigma_{mem} / \Delta$ respectively where ε_{mem} and σ_{mem} are the permittivity and conductivity of the membrane and Δ is the membrane thickness.

Using [Eqn. 1-1] to describe the dielectrophoretic forces acting on a body submerged in a fluid medium may not serve as an adequate descriptor of actual forces experienced in an experimental system setup. Discrepancies between this model and experimental behaviors can often be attributed to the simplified assumption made when deriving [Eqn. 1-1] which solely accounts for the presence of an electrically-induced dipole in the body. In reality a variety of multipoles can be induced in the particle depending upon the shape of and variations in the electric field. When the orientation of the electric field varies spatially over length scales comparable those of the particles being manipulated (often the case for microfabricated electrode structures), the likelihood of inducing mulipoles increases.

Accounting for these higher-order multipole terms is a consideration which was only recently placed into a mathematically rigorous form. Without outlining the specifics of its derivation the tensor notational description of the multipole DEP force is provided here [21].

$$F_{DEP}^{(n)} = \frac{\overset{\overset{-}{\vdots}}{\overset{=}{p}}{}^{(n)}[\cdot]^{n} (\nabla)^{n} E}{n!} \qquad \textbf{[Eqn. 1-6]}$$

In this description n indexes the force terms to their corresponding poles (n=1 for a dipole, n=2 for a quadrapole, etc.) while $\overset{\overset{-}{\vdots}}{\overset{=}{p}}{}^{(n)}$ is a multipolar induced-moment tensor. The specific implementation used in the simulation coding for my thesis (a subset of the code developed by

$$\left\langle F_i^{(1)} \right\rangle = 2\pi\varepsilon_{media} R^3 \operatorname{Re}\left[CM^{(1)} E_m \frac{\partial}{\partial x_m} E_i^* \right] \qquad \textbf{[Eqn. 1-7]}$$

$$\left\langle F_i^{(2)} \right\rangle = \frac{2}{3}\pi\varepsilon_{media} R^5 \operatorname{Re}\left[CM^{(2)} \frac{\partial}{\partial x_m} E_n \frac{\partial^2}{\partial x_n \partial x_m} E_i^* \right] \qquad \textbf{[Eqn. 1-8]}$$

$$\vdots$$

my advisor, Dr. Joel Voldman) relied upon a slightly more readable version of this formulation dependent upon sinusoidal excitations and time averaging and is provided in [Eqn. 1-7] and [Eqn. 1-8] for the sake of completeness [21]. These force terms whose superscripts link to specific higher-order terms are subscripted with "i"s to indicate that they are correlated to the i direction. The functional form of the associated Claussius-Mossoti terms for each of these relations is

$$CM^{(n)} = \frac{\varepsilon_{body} - \varepsilon_{media}}{n\varepsilon_{body} + (n+1)\varepsilon_{media}} \qquad \textbf{[Eqn. 1-9]}$$

Including these higher order terms in the description of the DEP force calculation helps to narrow the gap between prediction and empirical results.

1.8. Prior Work

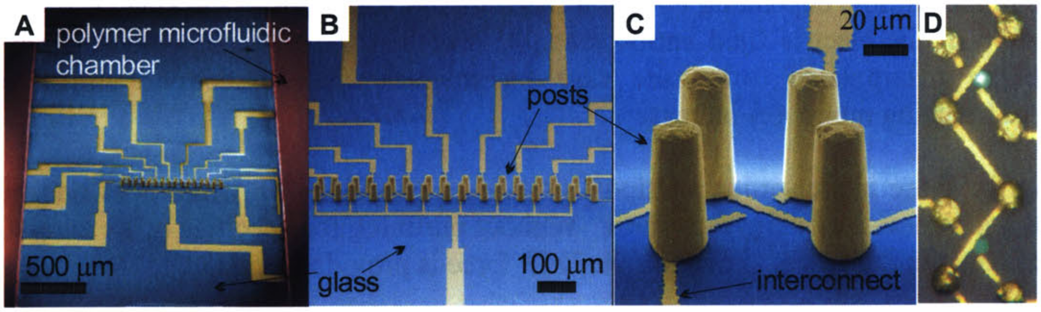


Figure 1-3: (A-C) Pseudo-colored electron micrographs of DEP traps for holding single cells. Each trap (C) consists of four post electrodes made of gold. An array of 8 traps (B) is situated in a microfluidic chamber (A). (D) Top-down view of two viably stained HL-60 cells trapped in the dielectrophoretic traps.

My project is an offshoot from and partial continuation of the work outlined in Dr. Joel Voldman's Ph.D. dissertation. In his work, the dielectrophoretic manipulation of individual non-adherent HL-60 leukocyte cells was demonstrated using micromachined extruded three dimensional trap geometries and n-DEP methodologies [21, 24]. His proof-of-concept layout used a single row of eight cell traps. Each trap could be turned on or off independently via electrical connections to off-chip circuitry. The design, pictured in Figure 1-3, successfully demonstrated the ability to trap, hold, image, and sort individual cells.

My project expands the scope of this earlier work enabling the micromanipulation of adherent cell lines. Dr. Voldman's collaborative efforts with Dr. Christopher Chen at Johns Hopkins University have established a support system for handling cells requiring membrane/substrate interactions. Specifically, through this collaboration, which is largely coordinated with the dissertation work of Darren Gray (a member of Chen's group) [25] designs for p-DEP traps were developed to position adherent cells on substrates within regions of patterned extra-cellular matrix (ECM) proteins. The basic trap design, detailed in Figure 1-4, uses a single electrode plate at the top of the cell flow chamber and a set of point electrodes on the chamber bottom. While a more complete list of this project's specifics are discussed elsewhere [25] its success in enhancing the registration of NIH/3T3 cells and BPAEC endothelial cells to specific sites in a microscale trap network over what is realized without a coupling of dielectrophoretic and surface patterning techniques provided me with some of the tools necessary for considering the feasibility of my project's aims. These prior efforts served as partial templates for the viable development of the cytometer screening technology explored in my work.

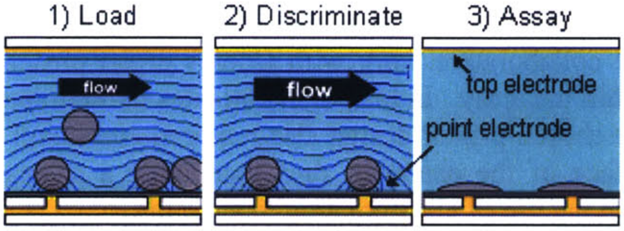


Figure 1-4: p-DEP traps. Side-view schematic of trap operation. Cells are first flowed into the chamber, wherein they are drawn toward the high-field regions near the bottom electrode points (1). Excess cells are flowed away (2), and the traps are turned off, the cells attach and assay proceeds (3).

1.9. Transitioning to the Current Design Approach

The previous work had several limitations for future design scale-up and trap site addressability aims. First, fabrication of the extruded-trap geometry was complex. Furthermore, large arrays of extruded traps would have posed problems during cell loading: the first row of traps would have prevented cells from accessing downstream sites since they would have presented a physical "roadblock". This prior design also required one specific electrical lead for each trap. As mentioned earlier, this would have forced the number of control leads to scale linearly with the number of traps in a given array, limiting its overall size. Finally, the discriminatory capabilities for single cell capture were somewhat limited with this design; it was not uncommon

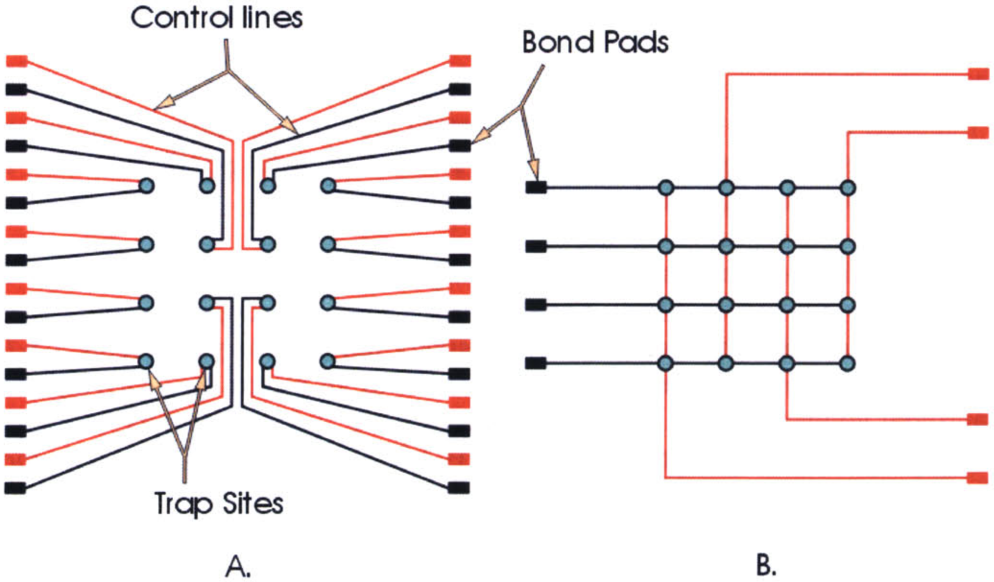


Figure 1-5: Two distinct control line configurations for electrically addressing individual trap sites within a 4x4 grid. In (A.) two unique connections link each site to off-chip circuitry for a total of 32 pad connections. (B) demonstrates the basics of the row/column addressing scheme used in my thesis and its implications on the device scaling. Only 8 connections are needed for this simple 4x4 proof-of-concept network.

to witness two or more cells occupying a single trap site location during experimental assays.

The collaborative work with Chen's group presents no scheme for addressing individual traps within the array. In his project all sites in the trap grid are ON or OFF at a given instant in time. The chosen p-DEP design also required inter-level vias to form the point electrodes on the lower surface of the chamber, thus mandating a substantially involved fabrication sequence reliant upon the use of electroplating techniques.

My work sought to meet several specific design criteria. First, I used planar electrodes to simplify the fabrication process and eliminate the presence of interfering objects in the cell flow path. I also fabricated both n-DEP and p-DEP designs to increase chances for a successful implementation and to better understand the limitations and capabilities associated with the two distinct trapping approaches. In my first-pass, proof-of-concept addressability design I implemented a series of simple four by four (4x4) trap arrays. To minimize interconnect requirements a row/column addressing scheme, based upon voltage differences between control electrodes (instead of active transistor switching devices), was used. With my new addressing method, shown in comparison to individual site control in Figure 1-5, the number of necessary control lines scales proportionally to the square root of the number of traps in a given array ($\sqrt{n}$). For the 4x4 arrays, this leads to a total of eight separate connections to off-chip circuitry (Figure 1-5). In this particular case, this requirement is one quarter the number of connections that would be needed if separate unique pairs of electrical control lines were used for each trap (Figure 1-5). I further sought to improve the single-cell capture capabilities of the design, and was able to do so especially for the n-DEP traps by including the use of confining pit structures sized specifically for the measured dimensions of the target 3T3 murine fibroblast cells.

1.10. Initial Conceptions – How the Implementation Was Originally Envisioned

The initial plans for this project encompassed two distinct cytometer configurations. The first used n-DEP trapping, a series of dielectrically separated crossing electrodes, and pits sized for holding individual cells or beads (see Figure 1-6). The second used p-DEP methods, a similar set of crossing electrodes, and a planar layout (see also Figure 1-6.)

The two envisioned device designs operated in slightly different ways, but both involved sequential load, assay, and sort routines. For the n-DEP case, cell-doped media was to be fed into the device flow chamber where cells would passively fall into the pits (Figure 1-6 (B-1-a)). Continuing the loading step was to involve the activation of all electrodes. Driving the control lines with sinusoidal voltage sources would form electrostatic "lids" on all pits, forcing the cells contained within to remain in place (Figure 1-6 (B-1-b)). Switching to a flush media and increasing the injection flow rate would sweep away excess untrapped cells. With loading completed, the flow would be turned off and all electrodes would be held in the activated state to allow trapped cells to attach to the insides of the pits. With all cells attached, the electrodes were to be turned off and the assaying sequence would begin (Figure 1-6 (B-2)). This process would merit a survey of the trap array and a selection of the specific cells for release and downstream recapture. With the specific traps chosen, the sorting sequence would begin. The row and column electrodes intersecting at release sites would be grounded while all other sites would be set to their nominal +V or –V activated voltage condition (Figure 1-6 (B-3)). To finish sorting, a

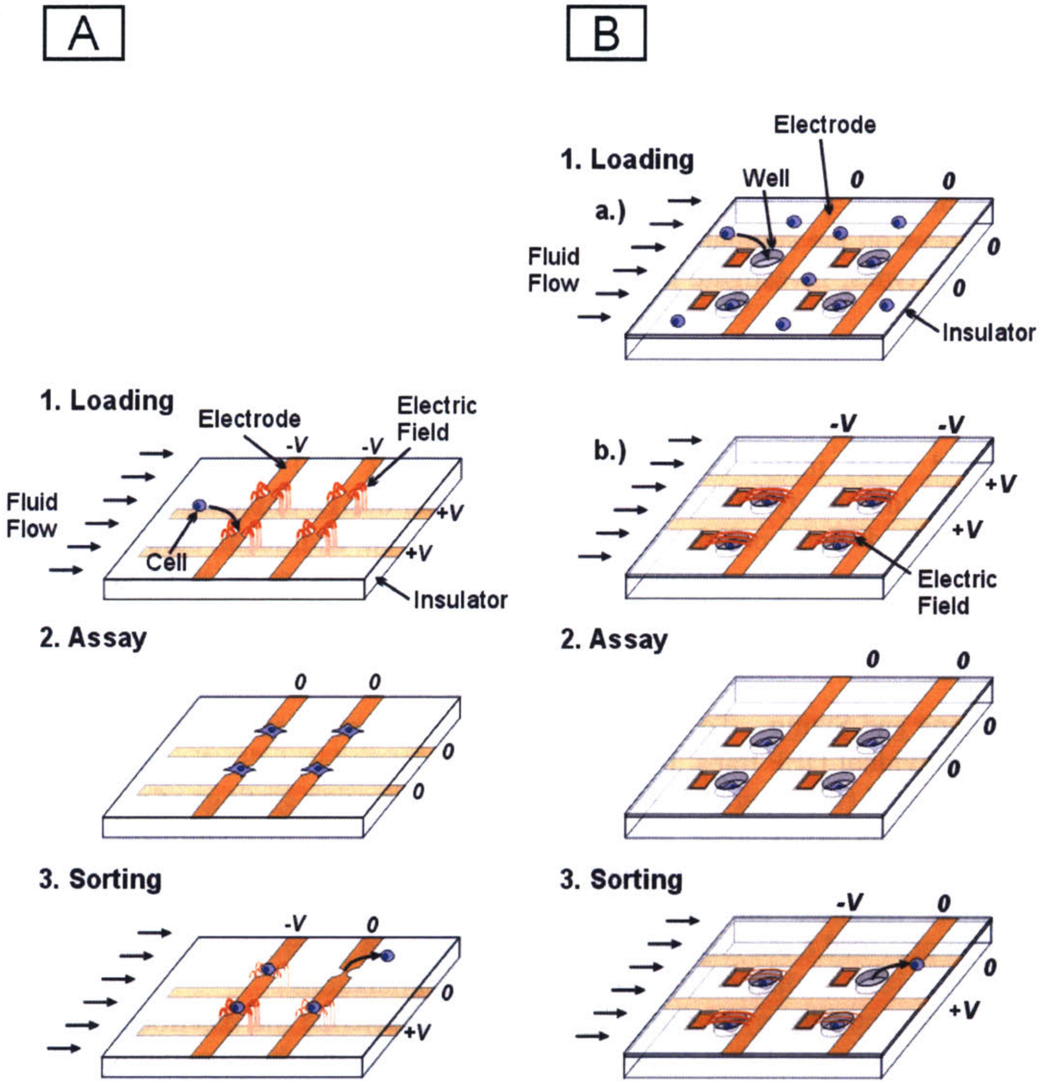

A
B
1. Loading
Electrode
Well
0
0
a.)
Fluid
Flow
0
0
Insulator
1. Loading
Electrode
Electric
Field
-V
-V
Fluid
Flow
+V
Cell
+V
Insulator
b.)
-V
-V
+V
+V
Electric
Field
2. Assay
0
0
0
0
2. Assay
0
0
0
0
3. Sorting
-V
0
0
+V
3. Sorting
-V
0
0
+V

Figure 1-6: Image (A) provides an envisioned p-DEP trapping design, while (B) highlights a potential n-DEP-based layout.

flow rate would be initiated and an enzymatic cleaving agent, such as Trypsin, would be used to dissociate cells from the insides of the pits.

The p-DEP design was imagined to rely upon planar electrode geometries (instead of pits) and thereby eliminate the need for z-directed (perpendicular to the substrate plane) structures in the layout. Operation was to require loading, assaying, and sorting sequences similar to the n-DEP layout, except in the loading step, where the electrodes were to be activated at the onset of fluid flow to *actively* draw cells to the traps (Figure 1-6 (A-1)). With both designs working properly the traps at the intersections of grounded row and column electrodes would afford cell release while all other traps would hold cells in place despite tendencies of the flow to dislodge them from holding sites and force them downstream. The successful operation of this envisioned row/column addressing scheme required trap designs that hold cells in place against fluid flow in both "full-" and "half-strength" activated conditions. A "full-strength" trap would have occurred where the row and column electrodes associated with a trap site were both driven by sinusoidal voltage sources 180° out of phase. A "half strength" trap would occur where either the associated row or column electrode was driven and the other was grounded.

The actual implementation I eventually adopted for my thesis operated using this originally envisioned addressing scheme, though the actual trap geometries were somewhat different from what was first planned. I provide more insight on the specifics of my actual devices in Chapters 2 & 3 which focus on the simulation work conducted to narrow down trap configurations of p-DEP and n-DEP types; investigate the overall system layout; and detail various aspects of the system's fabrication.

1.11. Key Benchmarks for Design Viability

Moving beyond these initial design conceptions to my final layouts required a detailed assessment of a wide variety of concerns tied to physical design implementation. To make this transition, I outlined five specific areas were I believed additional study, simulation, and understanding was necessary. Below I provide a list of those target areas to help the reader understand how I parsed the problem and eventually attacked it in some semblance of an organized and methodical manner.

Dimensioning and Sizing – To understand the range of potential feature sizes needed for the design of individual DEP traps, I was interested in determining the diameters of typical 3T3 cells. I conducted two separate calibration surveys, one using gratings of prescribed spacings and another using polystyrene beads of known diameters, to coordinate pixel counts to physical distances measured for images taken using a Spot CCD (Diagnostic Instruments, Inc.) camera mounted on an inverted Axiovert 200 (Zeiss, Inc.) microscope. This information provided a starting point from which I could generate a suite of initial cell-sized geometries for later evaluation in MATLAB-based simulations.

Fields, Forces, and Flows – I further wanted to characterize the electroquasistatic trapping potential for the designs I was considering for my layout and their operational effects on the surrounding cell environment. I was most interested in investigating concerns related to the range of acceptable drive frequencies for the row/column electrode structures; insurance of x-, y-, and z-directed stability; maintenance of low transmembrane voltages; and balancing trap strength for both half- and full-strength traps against drag forces intrinsic to the fluid flow.

Thermal Considerations – I sought to minimize excessive temperature gradients or temperature excursions caused by electrode activation. By managing both of these concerns I eliminated the need to consider the effects of electro-hydrodynamic flow forces and insured that DEP forces served as the dominant electrically controlled cell manipulation method. I also ensured that my device could be operated under a set of voltage conditions that would minimize the likelihood of adverse cellular effects [26, 27].

Attachment and Release Characteristics – Familiarity with the times required for cells entering the device to attach to and later detach from trap surfaces was fundamental. I ran a host of different evaluations to try and better understand whether or not certain factors could promote attachment and later conducted studies to learn more about the mechanics and chemistry of induced cell release from coverslip surfaces. These experiments helped me to begin assessing the feasibility of the planned load and sort device operations.

Materials, Fabrication, and Packaging – Choosing a suite of materials compatible with the machines and processes in MTL was important. While transparent materials such as Pyrex, quartz, and SU-8 appeared attractive for developing devices capable of being imaged using both standard upright and inverted scopes, I found that concerns related to cost, heat capacities, auto-fluorescence, and the etch capabilities [28] of various materials played an important role in helping me to decide precisely how I would construct my device.

Chapter 2: Trap Design and Simulation

Introduction

Proceeding from initial project plans to the final design implemented for the dielectrophoretic traps used in my thesis was not a serial undertaking. Throughout the process I was continually forced to consider how individual design decisions could create restrictions and pose implications for other components of the overall system layout. This interdependence of concerns impacted my approach to simulation, plans for developing fabrication sequences, and even issues as far downstream as choices for acceptable packaging technologies. As a result of these challenges, the reader may find it useful to flip to the cross-references listed in this chapter to better understand the iterations I pursued to narrow in on my final designs.

2.1. Cell Sizing

Before beginning any simulation routines or process considerations for fabricating my devices, I started from the basics by outlining a ballpark for the dimensional sizes requisite when designing DEP electrodes for 3T3 murine fibroblast manipulations. Despite the historical abundance of research conducted using this particular connective tissue cell line, different groups have reported differing values for the mean cell diameter [possibly try and cite]. Some of this debate may be a function of the wide variety of distinct 3T3 cell lines used throughout the biological research community. Other factors that could explain these inhomogeneities could include differences in culture techniques that might affect cell growth and overall health, as well as, differences in the techniques used for measuring cell size. Regardless of its origin, this situation presented incentives to design a series of calibration studies to evaluate the specific 3T3 cell line used in our lab (obtained from Dr. Phillip Leder, Harvard Medical School, Cambridge, MA).

2.1.1. Methods and Procedures

To approach this problem, I began by culturing 3T3 murine fibroblasts in 100 mm dishes (Corning, Corning, NY) using a media solution comprised of 87% Dulbecco's Modified Eagle Medium (Gibco, Carlsbad, CA), 10% fetal calf serum (VWR, West Chester, PA), 2% L-glutamine (200mM, 100x – supplied at 29.2 mg/mL in 0.85% NaCl) (Gibco, Carlsbad, CA), and 1% penstrep (10,000 units/mL penicillin G sodium, 10,000 μg/mL of streptomycin sulphate) (Gibco, Carlsbad, CA). These cells were incubated at 37°C in a 5% CO_2 atmosphere using a Steri-Cycle CO_2 incubator (ThermoForma, Marietta, OH). When cultures reached densities of approxiamately 10^6 cells/mL, I initiated a passaging regimen using a five minute incubated exposure to Trypsin-EDTA (1x 0.25% Trypsin with EDTA-4Na, prepared with 2.5 g Trypsin 1:250 and 0.38 g EDTA-4Na/L in HBSS without Ca++ and Mg++) (Gibco, Carlsbad, CA). With the cells stripped from their culture substrates, I quenched the Trypsin using the 3T3 media described above. I then triturated the cells and injected them into fresh 100 mm dishes. Prior to placing the new dishes into the incubator I photographed the cells using a Spot RT Color camera (Diagnostic Instruments, Sterling Heights, MI) set to record phase-contrast grayscale images (see Figure 2-1). I viewed all fields through a 10x/0,30 Plan Neofluar objective (Zeiss, Thornwood, NY) mounted on an Axiovert 200 inverted microscope (Zeiss, Thornwood, NY). Choosing to image the cells at the onset of a culture cycle, prior to the inception of surface attachment, afforded the opportunity to capture them in their most spherical forms; a condition similar to what was originally anticipated for the load step of device operation. With the images in digital form I used the Photoshop software suite (Adobe Systems, San Jose, CA) to extract average diameter values, in pixel counts, for a host of different cells in the images acquired. I then determined a rough estimate of the physical length associated with pixel counts using two separate metrics.

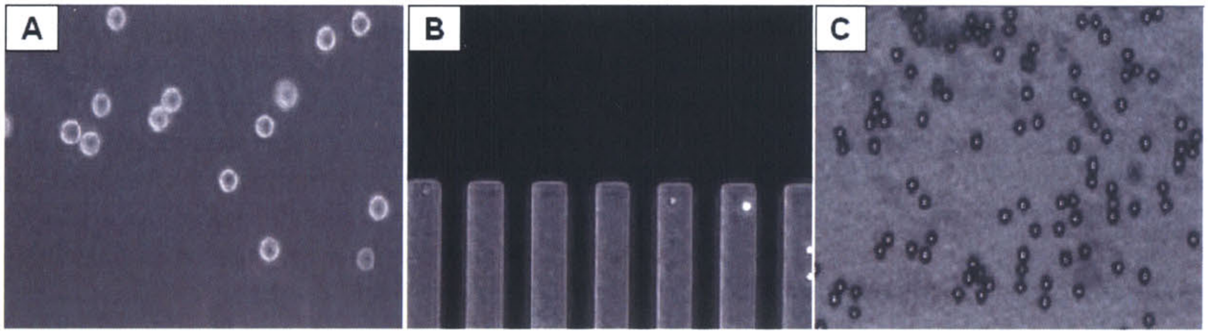


Figure 2-1: (A) An example image of unattached 3T3 murine fibroblasts shown alongside a (B) calibration grating displaying a feature density of 20 lines per mm and a collection of (C) polystyrene beads with prescribed diameters of 9.7 μm.

This step involved imaging both a micromachined grating (Edmund Industrial Optics, Barrington, NJ) with sets of chrome lines patterned in densities varying between 10 and 55 lines per millimeter (stepped in increments of 5 lines per millimeter) and a set of polystyrene beads (Bangs Laboratories, Fishers, IN) with engineered diameters of 9.7, 14.15, and 19.5 microns (see Figure 2-1). Using the grating measurement tool I obtained an average pixel to micron ratio of 3.2 across the entire range of line densities listed above (one measurement taken for each density). For each of the polystyrene bead sizes I took three separate measurements of pixel counts associated with bead diameters. These measurements resulted in a pixel to micron ratio of 3.4. Averaging the ratios from the two different calibration approaches provided a method for converting cell diameters as measured in pixels to corresponding physical distances.

2.1.2. General Results

Across a data set comprised of 54 cell diameter measurements I determined that the unattached 3T3 cells used in our lab manifest an average diameter of 23.5 microns. For illustrative purposes, Figure 2-1 displays three images characteristic of those used in this sizing study. With more insight regarding the specific spatial dimensions associated with my device's target cell line, I became better equipped to assign meaning to the performance characteristics of subsequent DEP trap designs. This sizing information defined the scale and narrowed the focus of my design space. As a result, I began a dedicated focus to experiment with different electrode configurations in pursuit of layouts equipped to capture spherical bodies roughly 20 microns in diameter. In the following section I present details covering many specifics associated with the simulation strategies and tools used in the resulting design process.

2.2. The Simulation Environment

To evaluate different electrode footprints and their associated DEP trapping potentials, I conducted numerical simulations using two separate software packages. I first constructed three dimensional renderings of the trap electrodes and neighboring materials using either the Femlab 2.3 or 3.0 (Comsol, Burlington, MA) multi-physics plug-in for Matlab (The MathWorks, Natick, MA). With the geometries established, I then assigned material properties (electrical and thermal) to the individual components in designs. I set up boundary conditions for all surfaces in the layout and then sequentially initiated electroquasistatic and heat flow solvers to generate electric field data and temperature profiles for each configuration tested. I then exported the electric field data for each design to a Matlab workspace and pushed it through modified versions of a "home-brewed" (developed by Dr. Joel Voldman as a part of his Ph.D. dissertation) assortment of simulation files [21] to render DEP force fields. The temperature profiles, in conjunction with the Matlab simulation work, outlined the performance characteristics of the evaluated designs. With this collection of information on hand for each architecture, I then made plots of various stability parameters and field induced cellular effects and decided which trap designs best met the requirements for safely capturing 3T3s.

2.2.1. Computing the Electric Field

In general, determining the electric field associated with a given electrical system is done through careful application of Maxwell's equations. Oftentimes these formulations are overly descriptive and are therefore simplified in ways that reduce the requisite mathematical overhead and simultaneously provide reasonably accurate depictions of the electromagnetics associated with a given set up. When I designed the simulations for the work done in my thesis I implemented what is known as the electroquasistatic approximation. This simplification of Maxwell's equations (see Table 2-1) modifies Faraday's differential law to neglect the influence of magnetic induction in the system. The approximation was appropriate for the simulation of all of the designs tested in my thesis as it applies to situations where the electric field is the primary field in the system and wave phenomena associated with the lag between voltage sources and their corresponding electric fields is negligible.

Name	Full Form	Electroquasistatic Form
Gauss' Law	$\nabla \cdot \varepsilon_o E = \rho$	$\nabla \cdot \varepsilon_o E = \rho$
Ampere's Law	$\nabla \times H = J + \frac{\partial \varepsilon_o E}{\partial t}$	$\nabla \times H = J + \frac{\partial \varepsilon_o E}{\partial t}$
Faraday's Law	$\nabla \times E = -\frac{\partial \mu_o H}{\partial t}$	$\nabla \times E = -\frac{\partial \mu_o H}{\partial t} \simeq 0$
Magnetic Flux Continuity	$\nabla \cdot \mu_o H = 0$	$\nabla \cdot \mu_o H = 0$

Table 2-1: Outline of Maxwell's equations and the corresponding electroquasistatic reduction

For irrotational field systems described by the electroquasistatic approximation it can be shown [29] that

$$E = -\nabla\Phi \qquad \textbf{[Eqn. 2-1]}$$

where Φ is the potential. Inserting this equation back into Gauss' law provides the Poisson relation

$$\nabla^2\Phi = -\frac{\rho}{\varepsilon_o} \qquad \textbf{[Eqn. 2-2]}$$

where ρ is the charge density and ε_0 is the permittivity of free space. This expression simplifies to the Laplace relation (see [Eqn. 2-3) for cases, such as those in my simulated trap geometries, where there are no free charges.

$$\nabla^2\Phi = 0 \qquad \textbf{[Eqn. 2-3]}$$

By applying the appropriate system boundary conditions one can then evaluate the electric potential everywhere in the system and then back out the corresponding electric fields using the relation listed in [Eqn. 2-1. Unfortunately analytical solutions are possible for only very basic layouts. For more complicated geometries such as those tested in my thesis, computationally-intensive, computer-based, numerical simulations prove essential.

2.2.2. Available Numerical Methods

In general, packaged solvers rely upon one of several techniques to determine field data [30]. Boundary Element Analysis (BEA) is especially apt for modeling constructs where the surface effects of different materials are the dominant features governing the behavior of a system. Finite Element Analysis (FEA) is better suited for applications where the system is largely inhomogeneous in composition. Finite Volume (FV) methods splice a given geometry into smaller regions and perform energy balances and the like over the subvolume elements without consideration for the details of what is located within those smaller components. Finite Difference (FD) methods, on the other hand, place points within a volume and then try to fit algebraic equations to them in a manner which approximates the overarching differential equations governing the system. In general, FD methods have received less research attention in recent years and are considered a less elegant approach when compared to some of these other noted strategies.

In my design space, a BEA-based approach would have provided an especially appropriate method for parsing various electrode geometries. Surface meshes could have been used to describe the voltages on their surfaces (electric fields inside of perfect conductors are zero), thus bypassing the FEA requirement to discretize these high aspect ratio features and thereby reduce computational memory requirements. Unfortunately the available choices of BEA systems were either prohibitively expensive or especially demanding from a learning curve vantage point. The relative accessibility of FEA solvers forced the decision from both cost and usability perspectives. It is likely that a finite volume method could have worked just as well, but again I had no readily available resource for a solver implementing this evaluation strategy and therefore opted for the use of an FEA-based package.

2.2.3. Resolving Temperature Profiles

$$Q = \frac{1}{\sigma}\left|J\right|^2 = \frac{1}{\sigma}\left|\sigma E\right|^2 = \sigma\left|\nabla V\right|^2 \qquad \textbf{[Eqn. 2-4]}$$

With the electric field data numerically determined for each model, I then examined the corresponding volume heat generation in the media by rerunning the Femlab models in a thermal simulation mode. The electric fields served as the source for inducing temperature rises in the liquid surrounding the electrodes through a Joule heating effect. The injected heat on a per volume basis Q is described by the [Eqn. 2-4] [31, 32] where σ is the electrical conductivity and J is the current density. Incorporating this equation into the subdomain description for the reservoir of media sitting atop the trap electrodes rendered the temperature profiles for each design examined by translating field data into an associated thermal response.

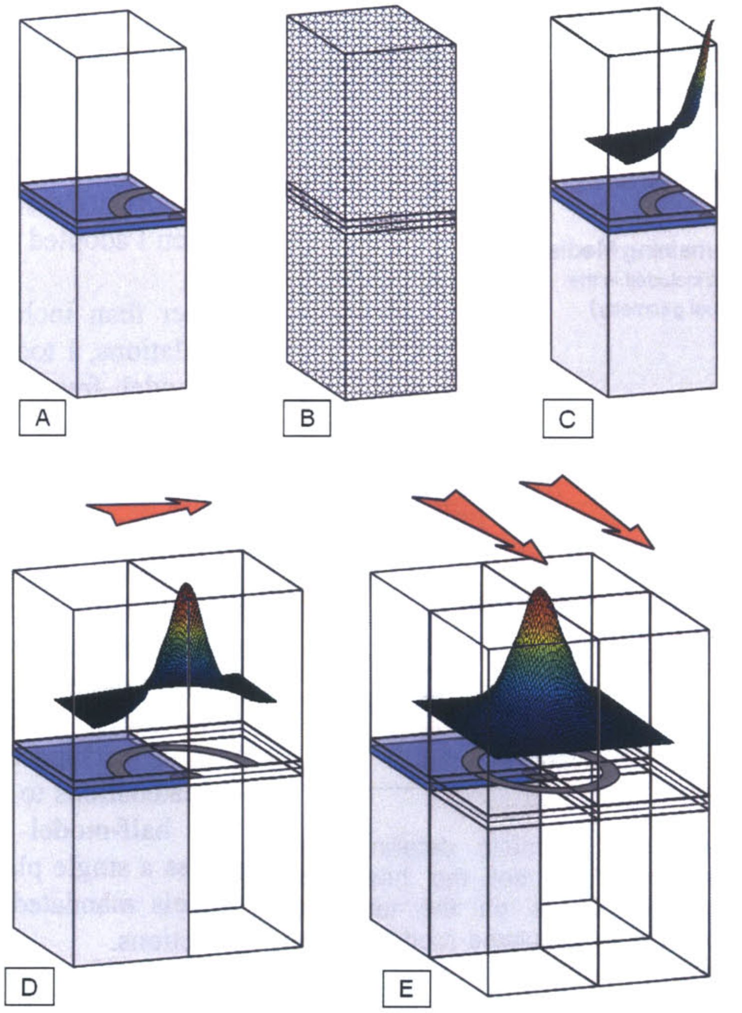


Figure 2-2: Images (A)-(C) outline the sequence of steps performed in the Femlab simulation environment for an example trap design possessing two degrees of symmetry. (A) shows a ¼ model of the geometry, while (B) provides its associated finite element mesh and (C) offers the normalized electric field solution. Pictures (D) and (E) present visuals of the Matlab matrix manipulations necessary for generating a full electric field solution for the trap. (D) shows the reflection in the x-direction, and (E) gives the reflection in y-direction.

This information was essential for defining the allowable drive voltages for individual designs. At issue was the need to avoid large temperature rises above the 37°C value set by the surrounding incubation environmental control chamber. I rejected all designs where temperatures could easily exceed 39°C with increased voltage applications. I thereby avoided negative cellular effects resulting from induced heat shock proteins [26, 27] and sidestepped the need to include considerations for electrohydrodynamic flows caused by large temperature gradients [32-35]. Carefully restricting the temperature allowances simplified the design process and ensured that DEP forces were the dominant field-promoted system response.

2.2.4. Managing a Memory Budget

As one might expect, manipulating the large amounts of data needed to produce the electric and thermal responses of the designs tested in my thesis demanded a significant amount of computing power. Despite running simulations on a Dimension 8200 (Dell, Round Rock, TX) desktop computer equipped with a 2.53 GHz Pentium 4 (Intel, Santa Clara, CA) processor and 1 GB of RAM it was easily possible to overtax the system when simulating the more complicated layouts. As an effort to sidestep some of the computational burden I adopted three specific measures.

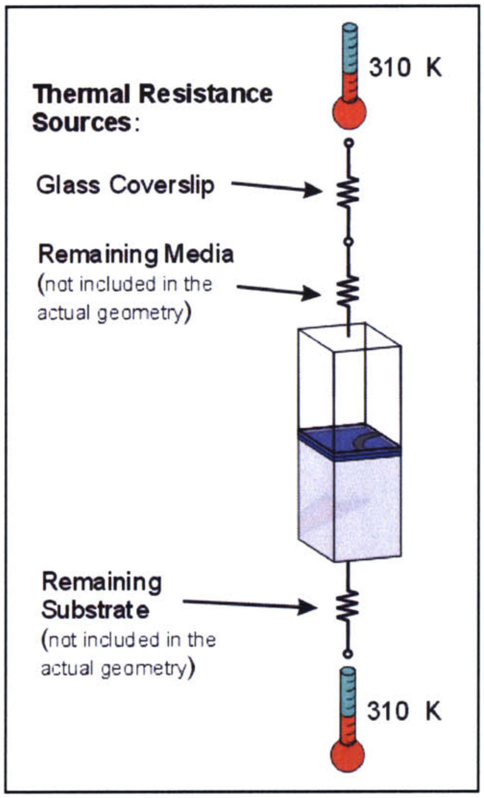

310 K
Thermal Resistance Sources:
Glass Coverslip
Remaining Media
(not included in the actual geometry)
Remaining Substrate
(not included in the actual geometry)
310 K

Figure 2-3: Schematic detailing the approach used to set the heat flux boundary conditions on the top and bottom faces of simulated models. The boundary conditions assume conduction is the primary thermal energy dissipation pathway.

Rather than including the entire trap geometry in simulations, I took advantage of layout symmetries to model fractions of the total design whenever possible. Figure 2-2 provides a general summary of this approach for a sample ring-dot configuration. Using this technique I could build a portion of the model, densely parse it with a finite element mesh, and then produce an electric field solution demonstrating greater refinement and accuracy per unit volume than would have been possible for a full trap simulation. With the quarter- or half-model simulated, I ported the associated field data to a Matlab workspace and performed a series of matrix concatenations to construct a full model description. The half-model layouts required one reflection across a single plane of symmetry while the quarter models mandated reflections in both the x and y directions.

Secondly, instead of creating geometries to exactly mimic the processes needed to fabricate the devices, I adopted a simplified approach to carefully examine the most important features of a given layout and discard minor nuances. Through this approach I modeled the electrodes as flat two-dimensional structures. By neglecting the inclusion of electrode thicknesses, the solver meshed the electrodes as boundary features instead of forcing small tetrahedral elements into geometries with high aspect ratios. This meant that the number of discrete elements needed to characterize a given architecture was reduced, permitting fewer equations in the system description. Shying away from features with sizeable x- and/or y-directed dimensions and comparatively small z-directed projections further encouraged me to implement layered materials with substantial thicknesses in my designs. As an example, the dielectrics, used to prevent shorts between the two metal levels in all processes considered, were generally modeled in accordance with the thickest value that could be reliably realized by the MTL machines responsible for their deposition.

To further conserve on memory requirements I truncated the heights of the substrate and media subdomains in all geometries using boundary conditions that could describe the remaining thermal conduction path to ambient 37°C temperature regimes. (The eventual plan is to house my designs in a portable environmental container that can maintain conditions closely matching those of an incubator and still permit the viewing of on-chip functions with microscope optics.) Figure 2-3 demonstrates the basic setup used for these boundary conditions. To successfully implement this strategy I took special care to insure that the heights of the substrate and media portions of the models were large enough to permit natural e-field attenuation. (Choosing heights which are too restrictive can constrain the volume where the fields are generated and force them into configurations which fail to reflect the actual system behavior.) I then used the resistive thermal model, described by [Eqn. 2-5] [36], to introduce effective heat transfer coefficients for the top and bottom surfaces to the system solver.

$$R_{t,cond} = \sum_i \frac{L_i}{k_i} = \frac{1}{h_{eff}} \qquad \textbf{[Eqn. 2-5]}$$

Here $R_{t,cond}$ marks the thermal resistance associated with the conductive path. L_i is the distance from the top or bottom boundary to either the next material in the heat flow path or a location where the temperature is set to a specified, known value. k_i is the thermal conductivity of a given material and h_{eff} is the effective heat transfer coefficient. In the case of the top boundary condition the heat flow path traveled through a remaining amount of media, through a coverslip, and finally to the set ambient temperature of 37°C. For the bottom boundary condition the heat traveled through a remaining amount of the system substrate and out to the 37°C temperature ambient. The values for the heat transfer coefficient plugged directly into the heat flow relation of [Eqn. 2-6] [36] and prescribed temperatures for the top and bottom surfaces of the geometry.

$$q_x'' = h_{eff}\left(T_{s,1} - T_{s,2}\right) \qquad \textbf{[Eqn. 2-6]}$$

In this relation q_x'' amounts to the heat flux. $T_{s,2}$ matched the isotherm temperatures that would have been seen at the top and bottom surfaces if the remainder of the media/coverslip and substrate thicknesses had been included in the simulated model. Avoiding a need to mesh materials above and below these top and bottom boundary conditions again reduced the number of equations need for system evaluation. $T_{s,1}$ equalled the external ambient temperature for the system.

2.2.5. A Roadmap for Simulation

Electrical Boundary Conditions			Silicon & SU-8 Processes
Perimeter Surfaces	Electrical Insulation	$n \cdot J = 0$	-
Internal Non-Electrode Surfaces	Electrical Continuity	$n \cdot (J_1 - J_2) = 0$	-
Electrodes	Electric Potential	$V = V_0$	V_{M1}=.5 [V]; V_{M2}=-.5 [V]

Thermal Boundary Conditions			Silicon Process	SU-8 Process
Perimeter Surfaces	Thermal Insulation	$n \cdot (k\nabla T) = 0$	-	-
Top Geometry Surface	Heat Flux	$n \cdot (k\nabla T) = h(T_{s,1} - T_{s,2})$	h=4303 [W/m^{2}K]; $T_{s,1}$=310 [K]	h=4303 [W/m^{2}K]; $T_{s,1}$=310 [K]
Bottom Geometry Surface	Heat Flux	$n \cdot (k\nabla T) = h(T_{s,1} - T_{s,2})$	h=328889 [W/m^{2}K]; $T_{s,1}$=310 [K]	h=1189 [W/m^{2}K]; $T_{s,1}$=310 [K]

Material	Thermal Conductivity (k) [W/mK]	Density (ρ) [kg/m^3]	Heat Capacity (C_p) [J/kgK]	Complex Conductivity (σ)	Relative permittivity (ε_r)
Silicon	148.0	2330	712	$4E-4+j*2\pi*10E-6*\varepsilon_0*11.8$	11.8
Silicon Dioxide	1.4	2200	1000	$1E-18+j*2\pi*10E-6*\varepsilon_0*3.9$	3.9
Phosphate Buffered Saline	.6	1000	4184	$1+j*2\pi*10E-6*\varepsilon_0*80$ (ndep) $.1+ j*2\pi*10E-6*\varepsilon_0*80$ (pdep)	80.0
SU-8	.2	1220	1090	$1E-18+j*2\pi*10E-6*\varepsilon_0*4.0$	4.0
Pyrex	1.2	2230	726	$2.5E-5+j*2\pi*10E-6*\varepsilon_0*4.6$	4.6

Table 2-2: A detailed listing of all material properties and boundary conditions used in my numerical simulations.

For completeness, Table 2-2 lists the set of electrical and thermal boundary conditions as well as general material properties used for all simulations run as a part of my thesis. Because two distinct material systems were evaluated in the beginning stages of my project, those material parameters are included as well.

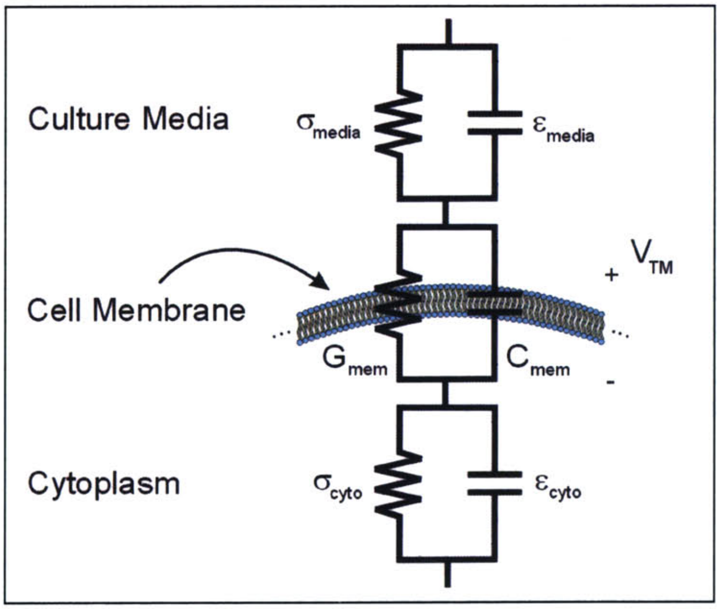


Figure 2-4: Circuit model reduction characterizing the cell/culture media interface. Depending upon the operating frequency of the DEP drive electrodes, the circuit can be either resistance or capacitance dominated. The transmembrane voltage is the key parameter to monitor for preservation of cell health.

After porting the field data to a Matlab workspace, additional performance characteristics for the traps were assessed. Beyond a given design's ability to hold cells in a specified location, it is important to assess and understand the impact that electroquasistatic fields can have on biological cells. Historically much of the research investigating interactions between living systems and electromagnetic fields has been linked to radio-frequency and microwave radiation [37, 38]. These types of studies have stemmed from concerns related to ambient fields associated with broadcasting towers, medical equipment, radar, and other similar commonplace sources. For this project, I wanted to model and simulate the sorts of biological effects that could result from exposure of individual mammalian cells to frequencies beneficial to dielectrophoretic manipulations (typically 10's of kHz to 10's of MHz). Producing this sort of information relied upon the use of a previously developed [24, 39] circuit model describing a mammalian cell stationed within a surrounding fluid. Figure 2-4 provides an illustration of the RC layout used to describe the conduction pathways from an external source through the media and cell membrane and into the cytoplasm of a cell. As the frequency of the driving signal is varied, the relative effects of the resistive and capacitive elements in the circuit define where specific voltage drops occur in the system.

The cell membrane is an anisotropic reaction interface that serves as a site for interactions between species located on its opposing surfaces. It is generally the dominant mechanism through which the cell interacts with external fields in the DEP frequency range. When subjected to external fields the rates of the reactions taking place at this boundary can be altered. Various models including electroconformational coupling (ECC) and descriptions of an oscillatory activation barrier (OAB) [40] have been used when describing these types of reaction modifications. Usually mammalian cell membranes have higher electrical resistivities than the adjacent media and cytoplasm and as a result tend to experience the bulk of the voltage drop at low frequencies. In this operational regime the circuit model reduces to a set of connected series resistances. The magnitude of that drop [41] is provided in [Eqn. 2-7]

$$\left|V_{tm}\right| = \frac{1.5\left|E\right|R}{\sqrt{1+(\omega\tau)^2}} \qquad \textbf{[Eqn. 2-7]}$$

where ω is the angular drive frequency of the signal and τ is the system time constant expressed as

$$\tau = \frac{RC_{mem}\left(\rho_{cyto} + \frac{\rho_{media}}{2}\right)}{1 + RG_{mem}\left(\rho_{cyto} + \frac{\rho_{media}}{2}\right)} \qquad \textbf{[Eqn. 2-8]}$$

In this relation ρ_{cyto} and ρ_{media} represent the electrical resistivity of the cytoplasm and cell culture media respectively. While this analytical description, does offer a mechanism for the attenuation of induced transmembrane voltages above the characteristic frequency ($1/\tau$) it fails to fully describe the system response at higher frequencies. For drives in the 100's of MHz the capacitances in the circuit model dominate and the membrane voltage saturates to a constant value.

The high resistance and small thickness of the cell membrane tend to magnify the effects of external fields, at low frequencies. This field amplification is mathematically described through the following simplification [21].

$$\left|V_{tm}\right| = \frac{1.5\left|E\right|R}{\sqrt{1+\left(\omega\tau\right)^2}} \approx 1.5\left|E\right|R \qquad \textbf{[Eqn. 2-9]}$$

$$E_{tm} = \frac{\left|V_{tm}\right|}{\Delta} = \left(\frac{1.5R}{\Delta}\right)\cdot E \qquad \textbf{[Eqn. 2-10]}$$

Here we see that the field inside of the membrane, E_{tm} is equal to the external field scaled by the 1.5R/Δ ($\approx$1000) ratio. Mapping out the transmembrane voltage as a function of frequency thereby offers a mechanism for monitoring the effective load to which the external field subjects the cell. Because the cell membrane sees the brunt of the induced electromagnetic stress and it is a known site for the transduction of various chemical effects [40] it is important to design traps capable of operating in frequency ranges that induce minimal transmembrane voltages.

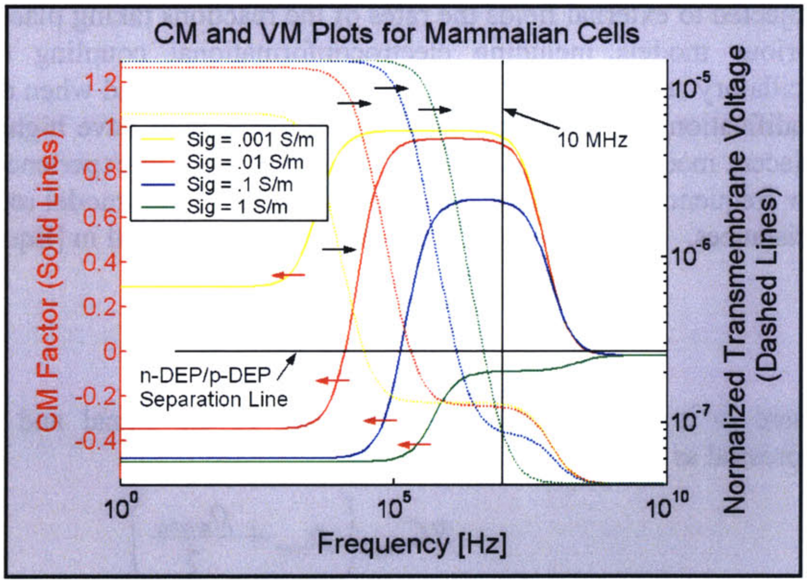


Figure 2-5: The DEP operational roadmap for my device designs. In general, high frequencies reduce the induced transmembrane voltages. Both the magnitude and sign of the CM factor vary over the examined frequency range. Positive CM factors yield p-DEP trapping while negative CM factors mandate n-DEP effects. The 10 MHz line demarks the frequency chosen for all simulation work.

Prior research [42-44] investigating the effects of mammalian cell exposure to DEP frequencies suggests that inducing transmembrane voltages less than 130-150 mV does not negatively impact cell division rates, cell motility, or cell viability. This is not to say that such voltages have no impact on biological function. To the contrary, Archer [45] demonstrated that even for low induced transmembrane voltages upregulation of cfos and the transcription of other unidentified genes was promoted. By checking designs to insure that their corresponding induced transmembrane voltages fell below a loosely defined ceiling of 100mV I created a viable sorting cytometer with a propensity for inducing minimal cellular health effects.

In Figure 2-5 I plot the transmembrane voltage induced by a normalized field of 1V/m as a function of frequency along with overlaying curves to outline the behavior of the real component of the CM factor. This diagram provides the DEP operational roadmap for all of the simulations I ran as a part of this project. Four curves outline the effect that varying conductivities have on the two charted parameters. In general the transmembrane voltages decline with increasing frequency, while the magnitude of the CM factor varies in a non-monotonic fashion and its sign flips throughout the examined range. A 10 MHz line highlights the location of the frequency chosen for all simulation work in my designs. This value was specified unilaterally for all configurations as it is well suited for maximizing the amplitude of DEP force, positive or negative, and it is large enough to minimize transmembrane voltages in trapped cells.

2.3. n-DEP Trap Modeling

Lacking prior experience in designing dielectrophoretic traps resulted in a rather iterative and sometimes circuitous path when moving from initial ideations to final layouts. As I had not decided upon a specific fabrication process or material system in which to implement the designs I was left with a vastly underspecified problem and an overabundance of seemingly plausible approaches. This section of my report details some of the many steps taken to establish the final designs for my n-DEP trap layouts and outlines some of the design lessons learned at various points in the process.

2.3.1. Attempts to Generate Planar Designs

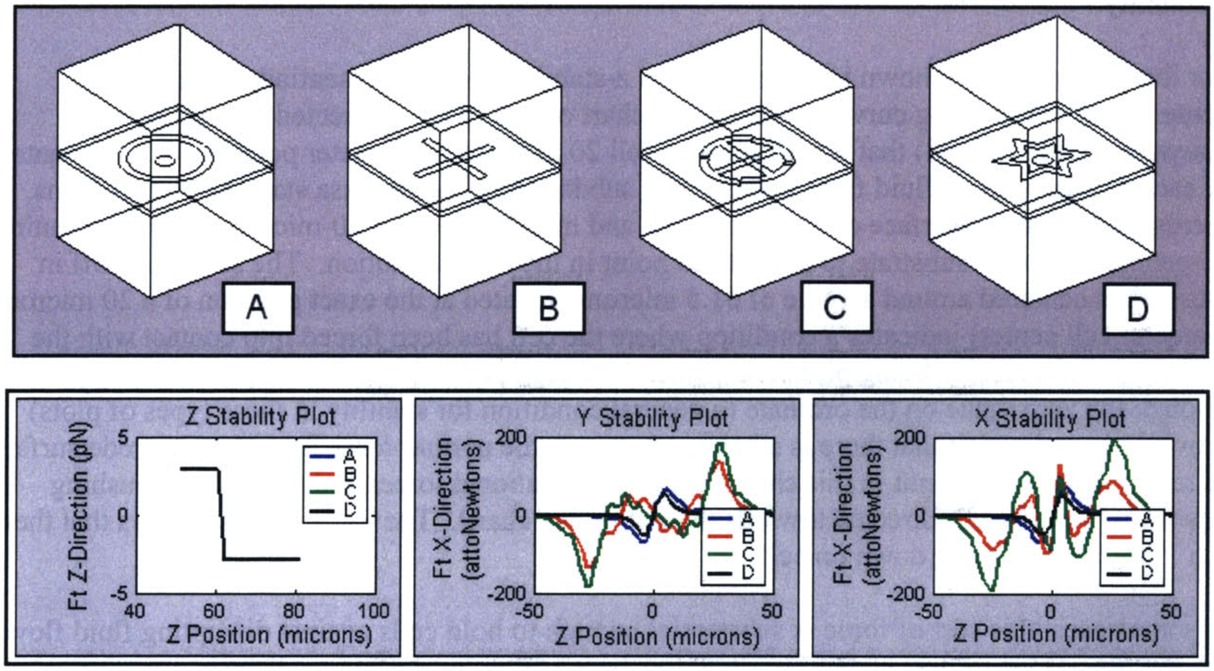


Figure 2-6: A brief overview of several example geometries examined and tested in pursuit of planar n-DEP trap designs. The corresponding stability plots for the four designs shown indicate that despite some level of stability in the Z-direction, X and Y directed holding forces are either unstable or too weak (attoNewton range) to present viable planar traps. [Note: In all of the cases shown in this figure, the geometries were constructed using a silicon substrate; a 3 μm thick silicon dioxide insulating layer with one electrode on its top surface and one electrode imbedded in its center; and a PBS media solution.]

In the early modeling phases of this project, I pushed hard to develop strictly planar n-DEP trap geometries. The advantage of this sort of trap design would have come in the form of a shortened and less complex series of fabrication steps necessary for a physical implementation. I worked hard to avoid the envisioned need for pit structures that would enable confining x- and y-trapping forces as I did not see a clear, established microfabrication process technology that could afford their construction. The measured 23.5 micron diameters of the 3T3 fibroblast cells anticipated for use in the testing phase of this project seemed to mandate the need for wells that would be difficult to construct using surface micromachining technologies [46] and challenging, if not impossible, to create through bulk micromachining strategies in some material systems. In this design stage I was still of the mindset that an ideal setup would produce devices affording optical transparency such that they could be versatile enough for imaging on either inverted or upright microscope platforms.

Admittedly my earliest design attempts were somewhat haphazard in nature. Before running full simulations on any single design, I established a sizeable library of possible electrode configurations, constructed their requisite geometries, and then began pushing them through Femlab and Matlab evaluations. I provide a small set of some of the example electrode architectures examined in this procedure in Figure 2-6. Ring-dot, cross, star, and an assortment of different shapes were tested. Interestingly, most of the designs demonstrated some degree of z-stability.

For the four test cases shown in Figure 2-6 the z-stability plots are essentially identical and demonstrate overlapping curves. These plots chart out all of the z-directed forces (gravity, buoyancy, DEP, normal) that would act on a cell 20 microns in diameter positioned at the center of each design with no fluid flow in the media subdomain. The abscissa starts at 51.5 microns, corresponding to the surface of the electrodes, and marches along a 30-micron-long path running perpendicular to the substrate to an isolated point in the media solution. The sharp dropoff in these plots centered around a value of 61.5 microns (located at the exact position of a 20 micron diameter cell center) indicates a condition where the cell has been forced into contact with the system substrate and is being pinned in place. The negative slope of these curves as they pass through the zero value on the ordinate (a general condition for stability in these types of plots) provides an indication that there is a balance between the normal force from the electrode surface (directed towards the right in this chart) and the gravitational forces and DEP forces pushing downward on the cell (directed towards the left in this chart). The force balance shows that there is a 3 pN force pushing down on cell.

In some cases, this sort of force is substantial enough to hold cells against disrupting fluid flows, yet the associated y- and x-stability plots for these particular designs presents a situation where much is to be desired. (Each of these plots was generated by mapping the total system forces in the x- or y-directions when marching across the electrode design, parallel to the substrate surface, through the 61.5 micron cell center z-position.) Despite the fact that some of these plots display locally stable holding characteristics (negative slopes for ordinate values of zero) they all present holding forces which are far too small to prove useful for DEP-based cell manipulations. In general, forces in the range of picoNewtons are necessary for trapping [21] while those found in these planar geometries were orders of magnitude less, in the attoNewton range.

I simulated a large assortment of different planar-based test electrode geometries and no designs emerged as adequate constructs for trapping 20-micron-diameter cells. In all cases, the x- and y-stability plots showed exceptionally weak holding forces. Such a condition meant that viable single-cell capture could not be realized for any of my layouts when subjected to fluid flow profiles in the media. Although my evaluations do not prove that planar electrodes are incapable of single cell capture, they led me to consider the originally envisioned pit-based approach.

2.3.2. Adopting a Pit-Based Approach

With no viable planar designs in hand, I began simulating different trap geometries exploring the behavior of various well-reliant designs. Not knowing exactly how I might successfully microfabricate structures with 20-micron deep circular pits flanked by surrounding electrodes, I generated a series of designs with identical electrodes implemented in two test material systems. The first, referred to throughout this report as the "silicon-based" system, used a silicon substrate into which the pit formations were carved and on top of which was placed an insulating oxide layer and a host of distinct electrode layouts. The second, earmarked as the "SU-8-based" system, relied upon a pyrex substrate onto which a 20-micron-thick layer of SU-8 photoresist was deposited and pattern in the shape of the necessary cylindrical well features. The electrodes were then designed to sit on top of the SU-8 layer and surround the upper edges of the pit.

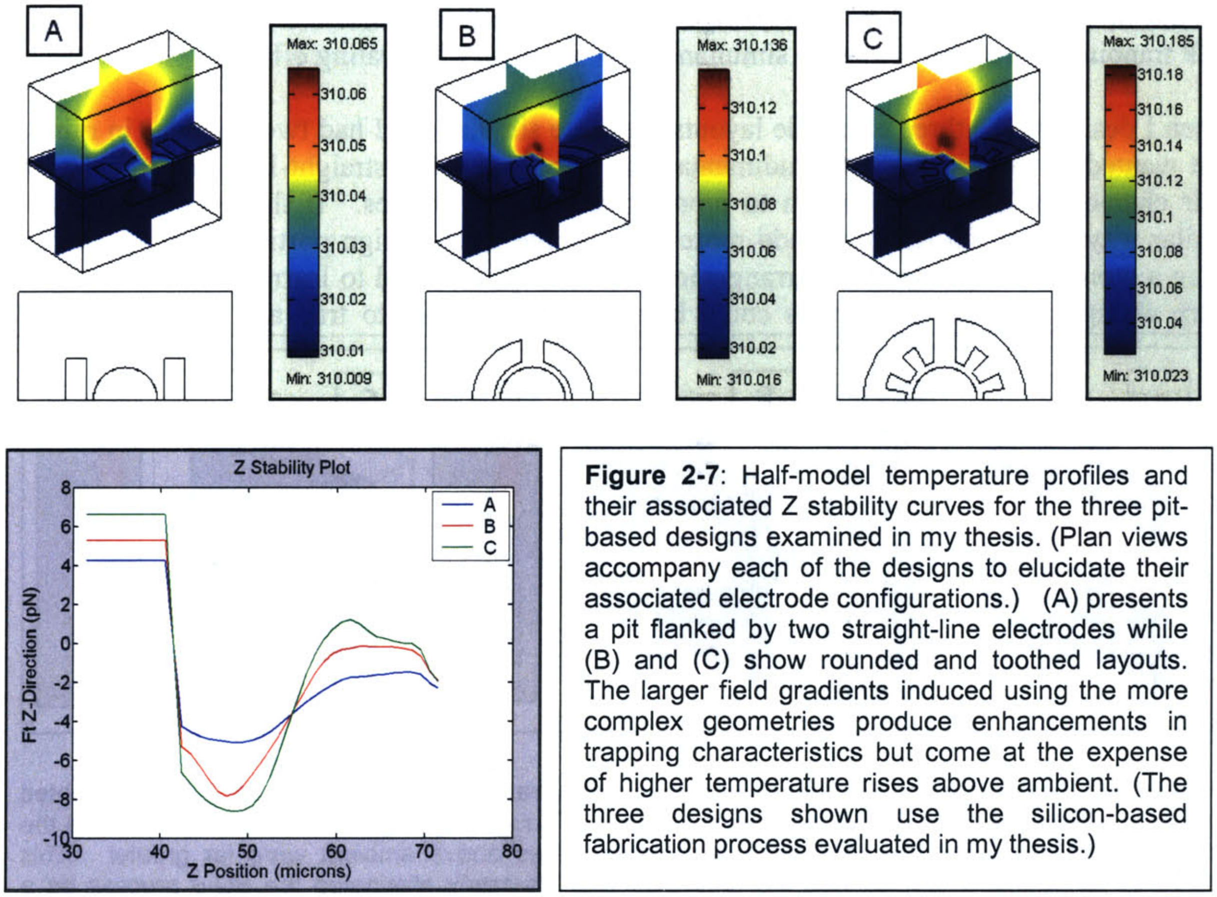


Figure 2-7: Half-model temperature profiles and their associated Z stability curves for the three pit-based designs examined in my thesis. (Plan views accompany each of the designs to elucidate their associated electrode configurations.) (A) presents a pit flanked by two straight-line electrodes while (B) and (C) show rounded and toothed layouts. The larger field gradients induced using the more complex geometries produce enhancements in trapping characteristics but come at the expense of higher temperature rises above ambient. (The three designs shown use the silicon-based fabrication process evaluated in my thesis.)

Again the primary benefit of creating devices employing pit architectures comes from the ability to ensure stable x- and y- holding forces. In these layouts I ran no simulations to generate x- or y-stability curves as these configurations inherently produce "infinite" stability in both of these normally-assessed directions. Any forces pushing the cell laterally within the confines of the pit would eventually be met with a counteracting normal force from the inside wall of the well. Forces that could exceed the opposing normal force would have to be great enough to mechanically fracture the device (an unrealistic possibility). All of these simulations were designed with the assumption that a pit diameter of 30 microns would be size selective for single cells based upon the dimensional studies mentioned at the front-end of this chapter. The electrodes were also all standardized to use 10 micron line widths. This decision cut out one more variable from the suit of choices that I could have made for designing different layouts and it erred on the side of caution from a fabrication ease standpoint.

Figure 2-7 shows three sample half-model designs implemented in the silicon-based material system. In addition to the z-stability plot, I provide planar views of the electrode geometries and images of the corresponding temperature profiles. In all three of the cases displayed, I witnessed stable holding characteristics as indicated by the negative slope of the curves crossing the zero value of the ordinate for all z-positions within the well (the z-position of 31.5 microns marks the bottom of the pit structure while 51.5 microns corresponds to the top of the well) and maximum system temperature rises above ambient that were less than two tenths of a degree Celsius for a 1 volt potential difference applied across the electrodes. With such small temperature rises, a large amount of leeway was left for increasing the voltages applied across the electrodes to enhance DEP trapping characteristics while simultaneously avoiding overheating effects.

When I designed the three electrode layouts for these simulations I had two thoughts in mind. I first wanted to explore the most rudimentary of layouts (i.e. the straight-line setup) and assess their characteristics in comparison to more complex architectures. If they could perform in similar ways I saw no reason to add more work to the mask-design portion of my project, by using a more elaborate electrode arrangement. Secondly, I wanted to learn what sorts of effects sharp changes in local geometries could have on the potential to trap and overheat cells. I surmised that since the DEP forces were proportional to the gradient of the square of the electric-field, including features (i.e. the gear configuration) to promote field non-uniformities over small

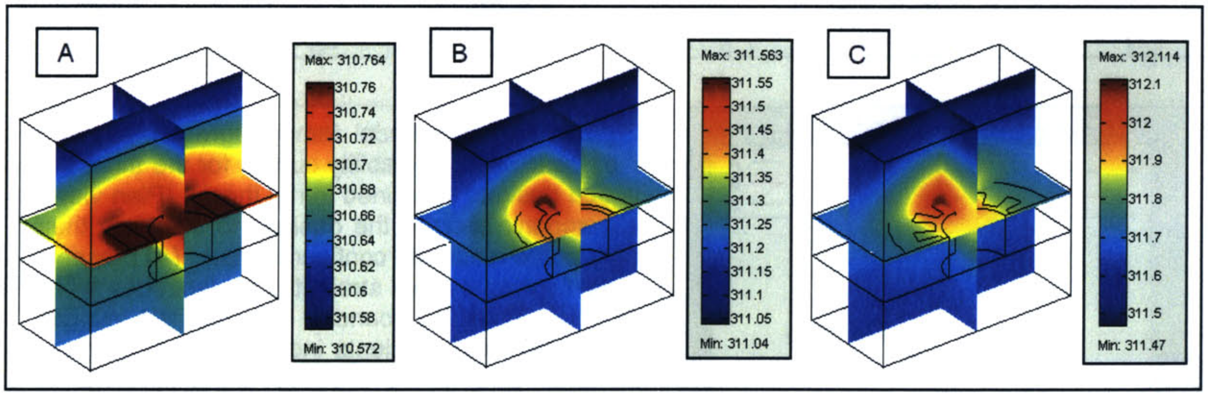


Figure 2-8: Depiction of the same three electrode configurations examined in Figure 2-7 implemented using an alternative SU-8 based fabrication process. Though trapping behaviors were similar to the silicon-based structures the associated temperature rises above ambient were far greater. This series of temperature profiles was the final blow that ultimately eliminated the SU-8 process as a viable choice.

spatial distances could enhance the magnitude of the DEP trapping potential. As Figure 2-7 indicates, the gear layout did in fact render the strongest z-stability trapping forces, but this came at the expense of higher maximum temperature rises in the system and enhanced challenges for translating the setup to an AutoCAD-based (Autodesk, San Rafael, CA) mask design.

When I examined these same electrode structures implemented in the SU-8-based process (see Figure 2-8) I again witnessed essentially the same z-stability trapping characteristics (not shown) but for each case the maximum temperature rise above ambient was substantially larger than the corresponding silicon-based designs. This result, which stems from the fact that the underlying Pyrex substrate possesses a much lower thermal conductivity than silicon, along with further fluorescence issues discussed in Chapter 3, presented an adequate case for nixing the SU-8-based process as a viable option for device implementation. Already for a 1V applied potential across the gear electrodes I saw a temperature rise in excess of the 2 degrees Celsius ceiling permitted for overall system design. This rise is a two degree rise above ambient, which would be permissible if the chamber temperatures were set to values lower than the planned 37 °C setting. For increasing applied voltages however, the ambient chamber temperature would need to be scaled back in an increasingly aggressive manner. For room temperature operation a 14 degree rise would be permissible (23 °C to 37 °C) however, such a situation forces consideration of EHD-based forces and restricts the applied voltages to a 2-3 volt ceiling. I sought to avoid this complication altogether.

2.3.3. The Final n-DEP Design

To move closer to final mask design implementations, I used the exact process flow (described in Chapter 3) for the actual device fabrication to simulate a model for the finalized n-DEP trap geometry that was as accurate as was feasible to test. My final trap layout employed straight-line configurations for the electrodes flanking the pits. Figure 2-9 provides a pictorial view of this final design along with several performance metrics. Maximum system temperature rises were modeled as 0.057°C; the maximum holding force was mapped to 5 picoNewtons for a 1V applied potential; and the maximum induced transmembrane voltage for the same applied potential was well below the 100 mV limit suggested by Fuhr and others [42-44].

Despite measuring the dimensions of the cell line anticipated for use in the testing phase of my thesis and subsequently modeling an effective design for an n-DEP-based trap, I was concerned that the discrepancies between my calculations for cell sizes and those reported in the literature could have stemmed from some sort of error on my end. This fear encouraged me to develop two additional trap designs which were slight variants of the fully tested original design. These variants were made to include pits with 25 micron diameters on the one hand and 35 micron diameters on the other. I imagined that this window would allow for some flexibility in terms of enhancing the potential for single cell capture if my sizing measurements had been incorrect. Pragmatically, building in a safety margin for my first round design seemed to be the only sensible choice.

2.4. p-DEP Trap Modeling

From the beginning, I migrated towards n-DEP design implementations because of a desire to operate my devices using some of the more standard collections of cell culture media and thereby remove added potentials for negatively impacting cell function. Despite this initial urge, I became concerned that there were many opportunities for my pit designs to fail to perform as desired. Top on this list was my concern that even if I could trap cells inside of the pit geometries it might be difficult to extricate them using injected enzymatic cleaving agents and pressure driven flows. Without a fully developed model to explain the flow effects associated with a deformable, polarizable spheroid body quasistatically held inside of a cylindrical structure extruded perpendicularly to an overriding Poiseuille fluid flow field [47], I lacked a complete picture of all mechanics operating in this design. I therefore decided to consider p-DEP models to bolster my arsenal of trap designs potentially capable of demonstrating single-cell capture.

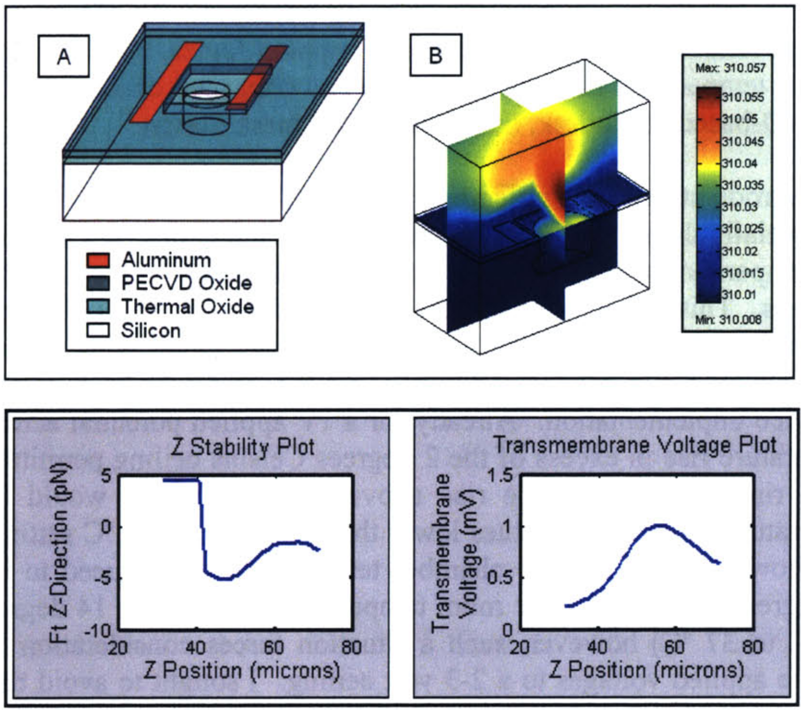

A
Aluminum
PECVD Oxide
Thermal Oxide
Silicon
B
Max: 310.057
310.055
310.05
310.045
310.04
310.035
310.03
310.025
310.02
310.015
310.01
Min: 310.008
Z Stability Plot
Ft Z-Direction (pN)
5
0
-5
-10
20
40
60
80
Z Position (microns)
Transmembrane Voltage Plot
Transmembrane Voltage (mV)
1.5
1
0.5
0
20
40
60
80
Z Position (microns)

Figure 2-9: Final n-DEP trap design (pit diameter = 30 μm). Image (A) provides a three-dimensional cartoon outlining the different layered materials requisite for fabrication. (B) indicates that a 1V potential applied across the trap electrodes produces only a 0.057°C temperature rise above ambient. The performance plots shown below the layouts outline stable holding characteristics and induced transmembrane voltages well below values known to negatively impact cell health.

2.4.1. p-DEP Design Evolution

As was the case for my n-DEP designs, I took a series of iterative steps before arriving at the eventual p-DEP layouts. The design evolution was more straightforward and tactical in this case largely because of the experience and understanding gained in the preceding work. To begin, I first examined the behavior of a simple intersecting cross geometry designed using the actual process flow chosen for the n-DEP designs. This geometry, shown in both pictorial format as well as planar view in Figure 2-10 demonstrated a somewhat unexpected trapping behavior. While I originally supposed that the configuration would produce a single localized capture site, due to the presence of the high field region established between the electrodes, it instead yielded four spatially separated traps. Plotting the associated normE^2 surface for this design created a visual of this response as the normE^2 quantity is directly related to the spatial distribution and relative strength of the DEP forces (see [Eqn. 1-1]) associated with a given layout. For all iterations leading up to the final p-DEP design, I used this same mapping technique to quickly interpret electrode behaviors.

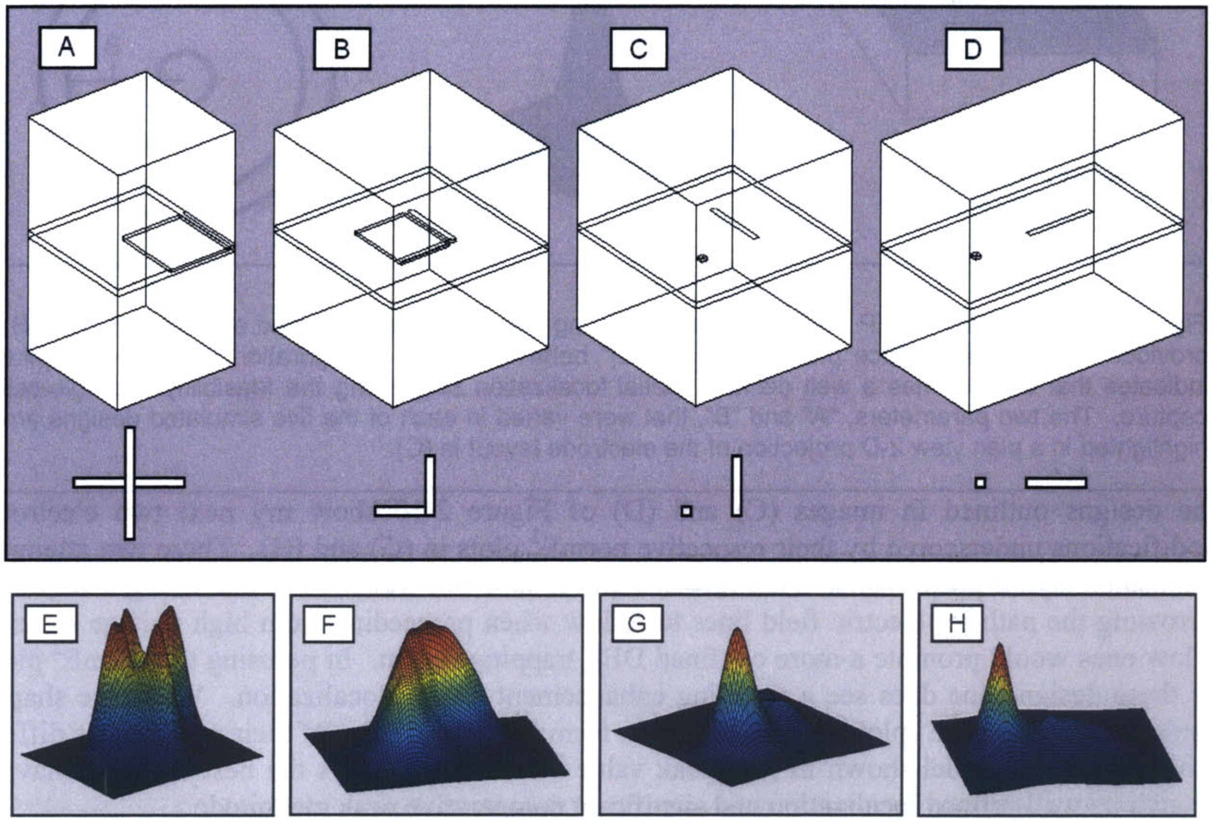


Figure 2-10: A set of four designs (A – D) outline the evolutionary steps taken to zero in on the final p-DEP trap configurations. The corresponding normE^2 (where normE = $\sqrt{(Ex^2+Ey^2+Ez^2)}$) plots (E – H) are provided below each design in this sequence. (The normE^2 behavior of the traps is directly related to the magnitude and spatial localization of the DEP trapping force.) (A) shows a quarter model of a cross electrode design. This first attempt renders four closely bunched traps (E) which present problems for single cell traping. Hoping to establish one peak in the normE^2 plot, a fourth of the original cross geometry was tested (B). This layout rendered a single trap that was widely dispersed spatially (F), again posing challenges to single cell capture. Two line-dot setups were tested (C and D), producing enhanced spatial trapping resolution (G and H). The non-collinear layout (C) rendered a larger peak value in its corresponding normE^2 plot, thus suggesting a move to the final p-DEP ring-dot geometries.

Obviously a trap displaying four spatially separated capture locations could not insure single-cell selectivity. I therefore took a next step and reduced the cross-layout to an L-configuration that could simulate one quarter of the symmetry associated with the cross structure (see Figure 2-10 (b)). This approach did render a single trap site, unfortunately with the disadvantage that it was largely spatially dispersed. Such being the case, this design also posed problems for realizing single-cell capture.

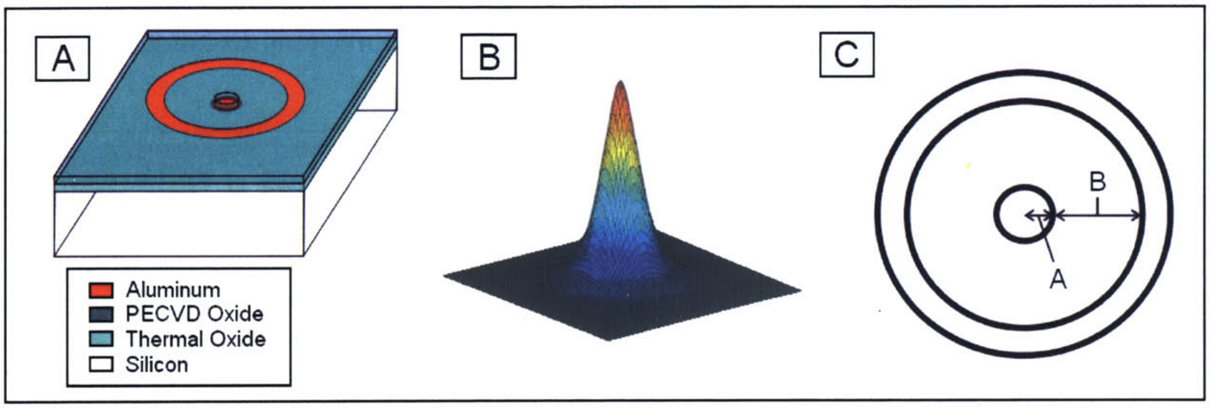


Figure 2-11: The final p-DEP designs consisted of ring-dot structures fabricated as shown in (A). (B) provides an example surface plot of the $|\text{normE}|^2$ behavior of this configuration. The sharp spike indicates that the trap has a well defined spatial localization suggesting the feasibility of single-cell capture. The two parameters, "A" and "B", that were varied in each of the five simulated designs are highlighted in a plan view 2-D projection of the electrode layout in (C).

The designs outlined in images (C) and (D) of Figure 2-10 show my next two electrode modifications underscored by their respective normE^2 plots in (G) and (H). These two attempts to enhance layout performance used further-reduced line-dot footprints. The thought was that narrowing the path for electric field lines to follow when proceeding from high voltage settings to low ones would promote a more confined DEP trapping region. In perusing the normE^2 plots for these designs one does see a resulting enhancement of trap localization. While the shapes displayed in the normE^2 plots appear similar in form, the magnitudes of their peak values differs quite a bit. The model shown in (C) (peak value not listed) displays the best overall behavior through its well-refined localization and significant comparative peak magnitude.

2.4.2. The Final p-DEP design

The basic footprint in image (C) of Figure 2-10 was reliant upon two features, a single isolated spot electrode and an offset extended electrode oriented tangentially to the shortest interconnecting distance. I was curious to know if this geometry could be further accentuated to amplify the associated characteristics responsible for its dominance over prior designs. The next leap then became the construction of a series of ring-dot structures. This next iteration set took the single spot electrode and accompanied it with an offset outer electrode that was tangent to all of the "shortest" interconnecting paths. This extension of the line-dot geometry eventually proved to be even more spatially localized than any of the preceding designs with a stronger relative normE^2 peak magnitude. Figure 2-11 provides a descriptive layout of this final p-DEP design type along with an example of the associated sharply pointed normE^2 plots and a planar view of their overhead architectures.

In the plan view of Figure 2-11 (C) two parameters "A" and "B" are outlined. To assess the relative influence of fluctuations of these two dimensions on the trapping performance of a generalized ring-dot geometry, I chose three easily manufacturable (from a microfab linewidth perspective) dimensions for each then paired them to form a collection of five distinct trap geometries and ran full Matlab simulations to assess the z-directed holding characteristics, the trap strengths, transmembrane voltages, maximum associated temperature rises and fluid flow rates against which they could hold cells in position. The collection of data generated as a part of this investigation is provided in Table 2-3.

A (μm)	B (μm)	Q (μL/min)	max|normE|^2 (V^2/m^2)	Ft-z (pN)	Trap Strength (pN)	V_{TM} (mV)	Max. Temp. Rise (°C)
3	27	3.0/3.1	1.7406E10	103.0965	43.3436	11.6241	0.017
3	20	2.7/2.8	1.5305E10	96.7396	39.3091	10.8999	0.017
3	34	2.6/2.7	1.5382E10	91.9449	37.0796	10.9273	0.016
2	27	0.9/1.0	9.0663E9	33.6884	13.8285	8.3892	0.015
5	27	6.1/6.2	1.4168E10	247.0430	86.8339	10.4874	0.002

A (μm)	B (μm)	Q (μL/min)	V required (V)	max|normE| (V/m)	V_{TM} (mV)	Max. Temp. Rise (°C)
3	27	2.7/2.8	0.95	1.2534E5	11.0429	0.015
3	20	2.7/2.8	1.00	1.2371E5	10.8999	0.017
3	34	2.7/2.8	1.01	1.2526E5	11.0366	0.017
2	27	2.7/2.8	1.67	1.5901E5	14.0100	0.041
5	27	2.7/2.8	0.67	7.9751E4	7.0265	0.007

Table 2-3: The top table displays the performance characteristics of the five final p-DEP trap designs for the case where the applied potential across the electrodes is 1V. The bottom table shows the same five traps examined when the voltages applied to the electrodes is varied until the hold/release flow rate meets a 2.7/2.8 μL/min value.

The top table lists the model responses for cases where a 1V potential difference is applied across the electrodes. The Q values in this chart are denoted as fractions where the value in the numerator provides the maximum flow rate against which the system can hold a cell in the trap and the denominator is the smallest flow rate needed for dislodging cells from activated electrodes. These flow rate calculations assume that the flow within the media is purely x-directed and amounts to a laminar Poiseuille flow profile through a chamber with a height of 100 μm and a width of 2 mm (I provide further description of how these flow rates were determined later in this section.) The Ft-z and trap strength values list the peak amplitudes in the z-stability and x-stability curves respectively for a no flow condition. Transmembrane voltages for the given designs are determined for worst case scenarios where the maximum normE field values in the entirety of the simulated geometries are the driving force for the potential drop.

The lower chart in Table 2-3 reverses the situation presented in the upper table by specifying a hold/release flow rate for each design and then backing out a corresponding and requisite electrode voltage necessary for matching the prescribed flow rate behavior. Again transmembrane voltages are calculated for worse case scenarios and maximum temperature rises are read directly from the output of the Femlab temperature simulations. These examinations each normalized in accordance with a distinct parameter helped me to try and distinguish relative differences in the trap behaviors.

For the most part, all five of the traps demonstrated sets of similar performance characteristics. When compared to the n-DEP designs these layouts present much larger trapping forces. In general, variations in the "A" parameter produced larger swings in the flow rate and corresponding required electrode voltage behaviors than did modifications in the "B" variable. The three final designs chosen for use in the mask layout (see Chapter 3) exhibited variations for both of these criteria (final designs were mapped to A/B pairs of: 3-27, 3-20, and 5-27). Again, I decided to fabricate a host of different p-DEP designs to expand the window for realizing viable implementations.

As I demonstrated in the performance data provided for the p-DEP trap architectures, I determined the flow rate response of each model. This additional information was readily rendered for the p-DEP geometries as they were implemented using planar structures. Such layouts permitted the application of standard fluid dynamic modeling without a need for considering the complexities associated with extruded or out-of-plane structures. I established the flow field by prescribing constant volumetric flow rates in Voldman's previously developed evaluation code [21]. With the flow field in place, I then ran scripts to follow the streamlines associated with cells trapped at the electrodes. Figure 2-12 (B) shows a case (as indicated by the single red dot suspended above the ground plane) where the flow rate is not strong enough to push a cell out of a given p-DEP trap. Figure 2-12 (C) on the other hand, displays an instance where the fluid flow rate is large enough to dislodge a cell originally held at the trap center (see the red streak indicating cell movement downstream from the trap site). Successive models of this sort of scripting routine helped me to iteratively pinpoint which specific flow rates defined the hold/release boundaries for all test cases.

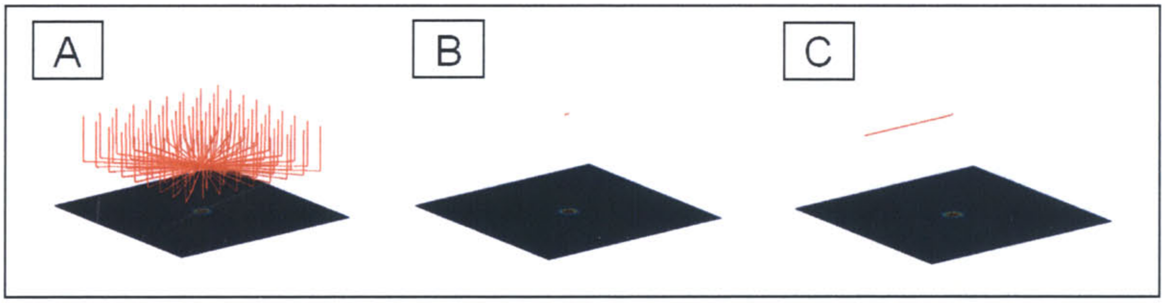


Figure 2-12: Outline of the flowrate evaluations performed to assess the performance of the final p-DEP designs. (A) indicates that for a Q=0 condition cells positioned 10 microns above the trap fall to the substrate and then migrate to the trap center. Image (B) shows a trapped cell held in place against a flow field while (C) shows a situation where the flow is large enough to dislodge a once-trapped cell. The dividing line between images (B) and (C) defined the hold/release flowrate for each trap.

Charting the data listed in Table 2-3 finalized my p-DEP trap designs and readied me for the mask design phase of the project. Heading into this next stage, I was equipped with three effective and modeled trap designs of each DEP type.

Chapter 3: Chip Design and Fabrication

Introduction

In this chapter I provide an overview of the design considerations and final decisions made in translating the simulated trap architectures discussed in Chapter 2 to their actual physical implementations. As I stated at the onset of the preceding chapter, the design evolution tied to my thesis work was a highly iterative and circuitous endeavor. I hope to here fill in some of the pieces that may have been missing for any reader approaching this text in a strictly sequential fashion. In this segment of my report I detail specifics of materials selection, photolithographic mask layout, and the series of process steps used for device fabrication.

3.1. Process Development

3.1.1. Narrowing the Field of Options

When I first began evaluating different approaches for device construction, I adopted an open-armed mentality and attempted to consider a large set of distinct material systems. Over time, I narrowed my search by developing and refining a series of specific process flow ideals. Admittedly my survey was not comprehensive nor even on par with some of the methodic selection strategies suggested in the literature [48, 49], but in the end, it proved sufficient to realize a viable design.

The outer limits of this search were first defined by a host of material compatibility concerns prescribed by the microfabrication equipment available for use in the MIT Microsystems Technology Laboratory (MTL). For all seemingly functional fabrication routines, I was required to demonstrate that the materials involved ran no risk of contaminating cleanroom equipment or adversely interfering with the work conducted by other users. Without this sort of consideration, submitting a process depending upon an incompatible substance would have been immediately rejected by the Process Technology Committee (PTC) (the group overseeing all work conducted in the on-campus microfab environment) and an alternative approach would have been mandated. Ideally I hoped to find a set of materials that were compatible with the MTL equipment list and also demonstrated optical transparency and non-fluorescence; presented high thermal conductivity and substantial mechanical strength; and enabled micropatterning through mask and etch sequences.

I pushed for optical transparency such that my devices could be imaged from either their top or bottom sides using upright or inverted microscopes respectively. With such a design ideal, I sought to enhance the system flexibility by avoiding a mandate to depend upon a specific type of viewing equipment. Projecting well beyond the scope of my thesis to considerations for a possible commercial venture, I envisioned such an affordance as a potential marketing edge for selling microarray devices to a host of different labs with different in-house microscopy tools. I further wanted to avoid materials with auto-florescent properties (especially in the wavelength ranges associated with the suite of standard Cy3, FITC, and DAPI filters used in fluorescence microscopy) to increase the signal to noise ratio when imaging fluorescently stained cells. If my design incorporated materials demonstrating large degrees of auto-fluorescence, screening for specific cellular responses could have become more difficult as the light emitted from the device itself would have overwhelmed that emitted from individual cells.

I hoped for high thermal conductivities in my material selection such that I could ensure avenues for removing heat generated in the media as a result of electric field excitations. As mentioned in the preceding chapter, temperature rises above 2 °C, during device operation, were considered unacceptable for the preservation of cell health. Substantial mechanical strength meant that the chosen materials would have to stand up to the handling requirements associated with a real-world fabrication sequence. Included in this requirement was the need for compatible thermal expansion coefficients among all materials chosen for a process. If too large a mismatch was seen in this parameter for adjacent materials in a layered stack, the likelihood of introducing thin-film stresses and witnessing delamination or even fracture became an increasing risk.

The ability to pattern a given material system with some sort of standard or available mask and etch routine is paramount for shaping layered systems into desirable and functional forms. Even if a given material offered capabilities compatible with the list of criteria discussed thus far, if it could not be engineered to render electrode structures of the requisite shapes, or pit geometries for housing individual cells as the case may have been, it became useless as a viable option.

In the end, after considering options as unique as Pyralux (Dupont, Wilmington DE), Kapton (Dupont, Wilmington, DE), PMMA, and host of polyimides and spin-on-glasses, I narrowed serious consideration to two distinct material systems. Figure 3-1 displays a set of simplified n-DEP trap cross-sections detailing these final two picks. One approach held true to the aim for transparency by utilizing a Pyrex (Corning, Midland, MI) substrate, a 20 μm thick pit layer for cell enclosure, and a series of top-level metal electrodes. With this design idea I built the well structures above the underlying substrate, as I found no viable in-house option for anisotropically etching Pyrex. The use of SU-8 photoresist (Microchem, Newton, MA), which is considered gold contaminated by the PTC, would have permitted the use of gold electrode structures and liftoff-procedures. In the second option I loosened my design requirements by abandoning hopes for optical transparency. This approach utilized a silicon substrate and adopted a combination of

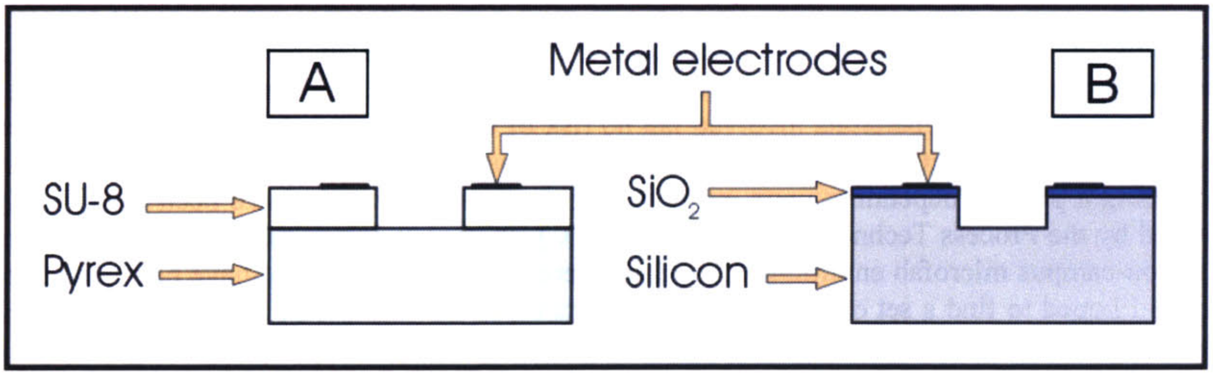


Figure 3-1: Simplified cross-sections of the n-DEP layout implemented in the final two distinct material systems considered and evaluated as part of this project. (A) presents an entirely transparent device capable of being imaged from either the top or bottom sides. Image (B) offers a silicon-based process with top-side viewing capabilities.

both surface and bulk micromachining techniques [50] to produce pit structures flanked by metal electrodes around their upper perimeters. Combinations of thermal and PECVD silicon oxides were used to prevent shorts between the two separate metal levels (M1 = first level of metal; M2 = second level of metal) and to isolate them from the underlying silicon substrate. I envisioned using a deep reactive ion etching technique for formation of the bulk of the pit structures.

3.1.2. Choosing the Final Fabrication Technology

As I showed earlier when comparing Figure 2-7 to Figure 2-8, the lower effective thermal conductivity of Pyrex in comparison to silicon served as a motivator for ousting the SU-8-based process as a viable option. In the end, the silicon-based process was adopted, but not until additional empirical evidence supported such a maneuver. When investigating the behavior of SU-8 photoresist, I produced a substantial experimental argument to suggest that SU-8 2050 photoresist auto-fluoresces despite claims by the manufacturer that it does not [51]. Figure 3-2 offers a summary of the data produced in my survey. In this figure I show three separate images of an SU-8 L-shaped feature 100 microns in thickness atop a Pyrex substrate. These features were produced as components of some of the devices fabricated by Dr. Voldman as a part of his Ph.D. work in accordance with the set of outlined spincoating speeds, baking procedures, and exposure times provided with the material protocol sheet on the manufacturer's website (www.microchem.com). If the SU-8 material was inherently non-fluorescent, then the L-shaped feature would not have been visible in any of the images taken as a part of this investigation.

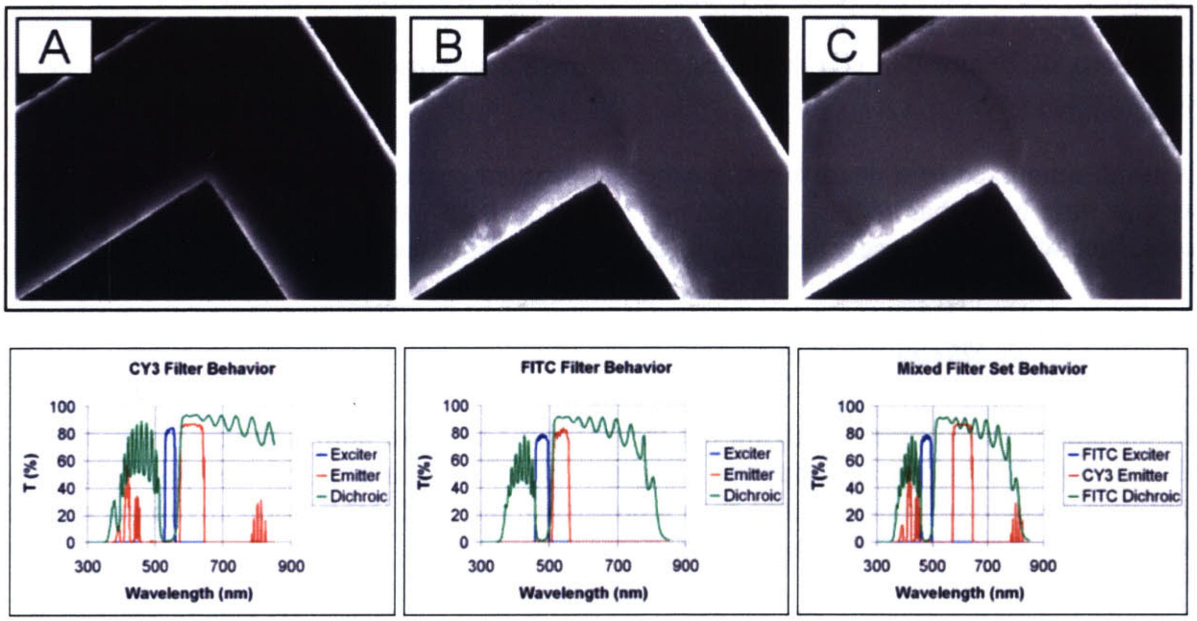


Figure 3-2: Images of a 100 μm high SU-8 dam layer viewed through standard Cy3 (A) and FITC (B) filter sets along with a third image (C) rendered using a combination of the exciter, emitter, and dichroic lenses from the Cy3 and FITC filter sets. The ability to view the dam in image (C) is a strong indicator that Rahman scattering is not a cause for the fluorescent behavior seen in image B and that the SU-8 material is auto-flourescent in at least the shorter-wavelength end of the visible light spectrum.

The structrure was clearly seen in the standard Cy3 and FITC (Chroma, Rockingham, VT) filtered images.

After discussing such behavior with a collaborator (Sam Thomas) in the MIT Chemistry Department, he and I examined the chemical structure of the compound [52]. Its large number of functional epoxy side groups serves as a cross-linking agent when exposed to UV radiation. Mr. Thomas supposed that these same groups were likely the cause of the witnessed fluorescent behavior. Testing for this possibility involved the elimination of what is known as a possible "physical" effect associated with the fluorescence imaging. In some instances undesirable leakage through the dichroic filter (designed to separate the exciting light source from the emitted light source [53]) in a fluorescence light cube can result in a "reflection" of source light back through the optical path in the microscope. Such a condition, which depends upon the inelastic dispersion of light through in effect known as Raman scattering [53], can present the possibility to "image" items that are in fact non-fluorescent. Through a careful combination of the different filters available in the Cy3 and FITC sets I created a unique fluorescent cube with the wavelength dependencies outlined in the plot below Figure 3-2 (C). In this configuration the pass-band of the emitter filter was pushed further away from both the bandwidth window associated with the exciter and the edge of the pass-band associated with the dichroic filter. I designed this layout to eliminate any potential "overspill" from the exciter and to assess whether or not the SU-8 feature luminesced of its own volition. The fact that the L-shaped feature is clearly seen in Figure 3-2 (C) indicates that Raman scattering is unlikely the cause for the fluorescent response.

This result amounted to a death blow for the SU-8-based process. Mr. Thomas suggested that there was little hope that adding "quenching" components to the SU-8 resin could eliminate the fluorescence without adversely affecting its ability to crosslink as a photopatternable material.

3.1.3. Testing the Silicon-based Process

With the silicon-based process edging out the SU-8 model from both a thermal perspective as well as a non-fluorescence standpoint, I began a robust examination of the specific machine capabilities needed for implementing such a process in the MTL fabrication environment. This cascaded into the beginning stages of a final process flow design.

The true test of all the design work done thus far was to then find a specific way to navigate from one machine to another and progress throughout a fabrication sequence without running into machine cross-contamination issues. One of the largest limitations imposed on this work was my need to push wafers through an STS etch sequence as one of the last steps in my fabrication procedure. This requirement forced me to obey all of the restrictions associated with the use of the STS machines [54]. The biggest impact resulting from this STS dependency was the need to avoid gold contamination until after the DRIE silicon etch.

Overcrowding in the Technology Research Laboratory (TRL) portion of MTL encouraged me to organize my processing work such that a large portion of the design employed machines in the Integrated Circuits Laboratory (ICL) section of MTL. This "cleaner" environment specifically catered to CMOS processes presented even more challenges for process design. With my decision to process mainly in ICL I elected to implement aluminum for all electrode structures in my layout. This decision was somewhat forced by the previously mentioned gold restrictions and further encouraged by my desire to utilize a standard CMOS metal that was well understood and readily accepted as a safe material within the confines of ICL. Admittedly, opting for aluminum metal layers was in some ways a suboptimal route as its associated effects on cell health and concerns of biocompatibility were somewhat suspect [55, 56]. Its links to diseases such as Alzheimer's and its supposed promotion of death for certain cell lines suggested that my decision would likely only afford a viable fabrication sequence for a proof-of-concept design.

While a standard lift-off procedure might have worked for patterning the metal layers in my devices, ICL presents a strict ban on all such sequences. This restriction forced me to examine plasma etch options for forming my electrode geometries. The only machine available in the whole of MTL capable of plasma etching aluminum layers without causing gold contamination is the Rainbow (Lam Research, Fremont, CA). This machine further limited my process, by requiring the use of 6" diameter silicon wafers.

As I had learned when organizing geometries for the simulation models described in Chapter 2, thermal and PECVD oxide layers 1.5 μm in thickness were realizable using MTL's wet oxidation furnaces and Concept One (Novellus Systems, San Jose, CA) deposition tools. Discussions with MTL staff and equipment operators indicated that such thicknesses could easily be achieved without a need for excessive concerns related to residual film stresses, wafer warpage, or pinhole effects.

Despite the standardization of multilevel metal processes in industrial CMOS microfabrication facilities, patterning two metal layers and subsequently etching the intermetal dielectric was considered a somewhat challenging process for the academic setting of MTL. Complicating my specific implementation of this sequence was a need to etch the intermetal silicon dioxide layer in a manner that would expose certain portions of the lower M1 metal layer, without damaging it or the machine used to etch the dielectric. The AME 5000 (Applied Materials, Santa Clara, CA) seemed to present a possible option for conducting an anisotropic dry etch of the silicon dioxide, but it bans the use of wafers where metal levels are exposed. While the front end of my etch would not present any exposed metal features, its desired end-point condition would have posed problems. This circumstance obliged me to consider wet etchants, capable of eroding oxides demonstrating high selectivities against aluminum. I was left in a position requiring the introduction of a new material to the MTL microfab environment. While this situation was highly undesirable, my advisor and I saw no apparent alternatives. I eventually proposed a process relying upon a product known as Silox Vapox III (Transene, Danvers, MA).

My fears of possible negative interactions between the aluminum electrodes and mammalian cells motivated me to consider the impact of intentionally depositing a thin insulating oxide layer covering all aluminum surfaces in my devices. The circuit model I provide in Figure 3-3 outlines the modeling used to investigate this curiosity. The drive voltages set for the electrodes in the geometry are given two paths for conduction. They can close a circuit through the overlying media environment or through the underlying silicon substrate. The resistances and capacitances associated with these two distinct paths are outlined and labeled in the upper left hand corner of Figure 3-3. My primary interest was to gain insight concerning the amount of input voltage "seen" across the R_{med} element in the model as a function of the input drive frequency. By establishing the transfer function to map out this response, I could use Matlab simulations to determine whether or not a sizeable fraction of the input voltage was generating electric fields to enable sufficient DEP holding forces. I suspected that thicker PECVD oxide layers might attenuate electric fields to an extent large enough to prevent effective DEP trapping. The Bode plots to the right of the schematic in Figure 3-3 support this suspicion. For the case shown at the upper right where only a double-layer capacitance associated with a Debye layer in the media is modeled [57], no significant field attenuations are seen above 100 kHz. In contrast, the plot in the lower right-hand corner indicates that large field attenuations result when protective oxides (C_{dox}) even as thin as 0.1 μm are used. This 0.1 μm layer was set as the lower limit for protective oxide thicknesses as it was reported to me by the MTL staff that this value approached the lower bound for reliable uniform PECVD deposited coatings. (For all simulations I assumed the presence of an overlying PBS media with an electrical conductivity of 1 S/m.)

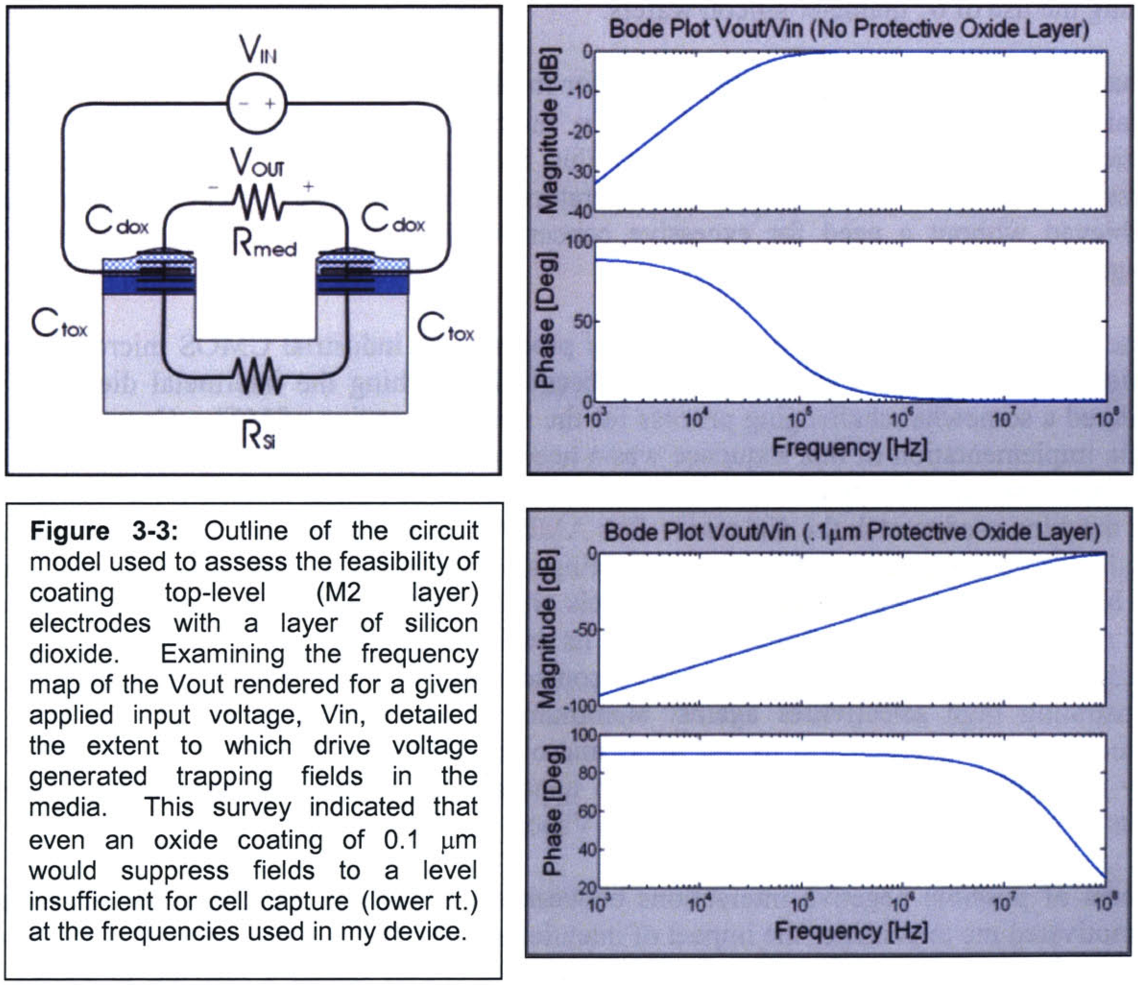


Figure 3-3: Outline of the circuit model used to assess the feasibility of coating top-level (M2 layer) electrodes with a layer of silicon dioxide. Examining the frequency map of the Vout rendered for a given applied input voltage, Vin, detailed the extent to which drive voltage generated trapping fields in the media. This survey indicated that even an oxide coating of 0.1 μm would suppress fields to a level insufficient for cell capture (lower rt.) at the frequencies used in my device.

These results emphasized the importance of implementing a successful strategy for exposing the M1 metal layer in regions where field lines need to bridge paths between high and low voltage electrodes at individual trap sites. Without an effective removal of the PECVD oxide in such regions trap strengths would be compromised.

Although it mattered less than some other concerns, this modeling procedure offered some incentive for trying to use lowly-doped silicon substrates with low conductivities. The actual wafers used in my thesis were prime grade, phosphorus-doped, n-type wafers, with 100 orientations and resistivities between 7 and 20 Ω cm. They were formed using the CZ method and purchased from Wafernet, Inc. (San Jose, CA).

All of these concerns defined the ultimate form of my final process flow. Appendices I and II list the specific steps involved, along with pictorial illustrations and the machines required for each component in the overall procedure. In its most basic form the general sequence for fabrication involved the following key steps:

- Growth of a wet 1.5 μm thick SiO_2 layer on a silicon substrate
- Deposition and patterning of a 0.5 μm thick M1 aluminum layer
- Deposition of a 1.5 μm thick PECVD SiO_2 layer
- Deposition and patterning of a second 0.5μm thick M2 aluminum layer
- Patterning of the PECVD SiO_2 layer
- Patterning of the thermally-grown SiO_2 layer
- Etching of the silicon substrate
- And finally, packaging (to be discussed in Chapter 4)

3.2. Mask Design and Chip Layout

3.2.1. Functional Elements in All Chip Designs

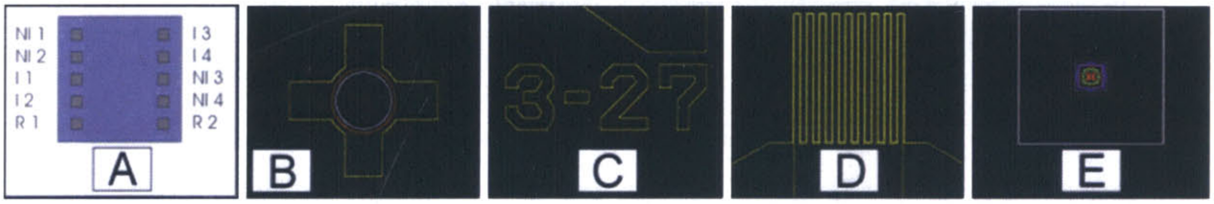


Figure 3-4: Outline of the standard suite of features included on all chips designed in this project. Image (A) indicates that there is a standard pin layout for all chips regardless of type. All of the inverting and non-inverting pads, as well as links to the on-chip resistor are in the same location in every design. (B) shows a cross-shaped pattern large enough for macroscopic visualization that serves as a target for drilling the through holes needed for fluidic port connections. All chips are labeled (C) with graphics large enough to avoid a need for inspection under a scope when sorting them. Each is also equipped with a large resistor (D) offering an avenue for on-chip temperature detection and two separate alignment marks for proper positioning of sequential mask layers.

With the final process in a functional form I began work to design the necessary mask layers for my thesis. Before beginning any actual layout, I defined a set of desirable features to incorporate in each chip on the wafer. Figure 3-4 displays these distinct items. Early on, I chose a 13mm x

13mm chip footprint to render die large enough for ease in handling while at the same time providing flexibility for placing multiple instances of the twenty-odd distinct chip designs on a 6" wafer map. For all chips, I established a single uniform set of pad orientations that later enabled me to use a single packaging design to mount any of the chips fabricated in my process. I labeled all chips with macroscopically visible tags to enable quick sorting and ease in positioning the drill holes necessary for fluidic port connections. I placed resistors with target resistances of 100 Ω on each of the chips to provide an avenue for measuring on chip-temperatures. While I never actually incorporated this function in any of the evaluations I ran during my chip testing phase, one of our lab's undergraduate researchers (UROP) planned to monitor temperature profiles by checking for thermally induced changes in the on-chip resistance using an external balanced Wheatstone bridge circuit. Finally, rather than relying upon global alignment marks, I incorporated alignment patterns in both the upper right and lower left hand corners of each chip. Through this approach I sought to minimize some of the searching involved with locating alignment marks during wafer exposure steps.

3.2.2. The Final Suite of Chip Layouts

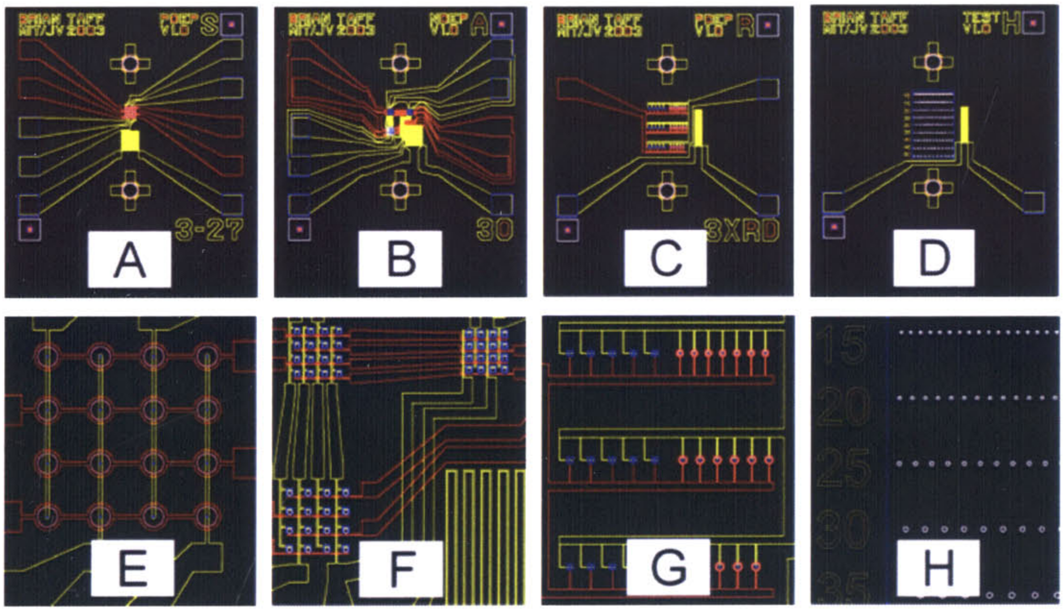


Figure 3-5: Images of the four distinct chip types used in my mask designs. Images (A) and (E) show a layout employing a single 4x4 trap array in full-scale and close-up forms. (B) and (F) present matrix chips which use three separate 4x4 grids for examining the effect of trap spacing on capture potential. Pictures (C) and (G) offer row-chips which are strictly for use as tools to empirically measure trap strength. (D) and (H) outline a specific chip design with an assortment of holes of various diameters. This chip is not activated with any electrodes and works only as a platform for measuring cell diameters and finding the best choice for pit sizes in subsequent designs.

Overall my mask layout incorporated four different types of chips implemented using 24 discrete chip architectures. I used this design breath to explore a multitude of options for testing the designs in my thesis in a robust manner. Samples of these distinct chip "flavors" are provided in

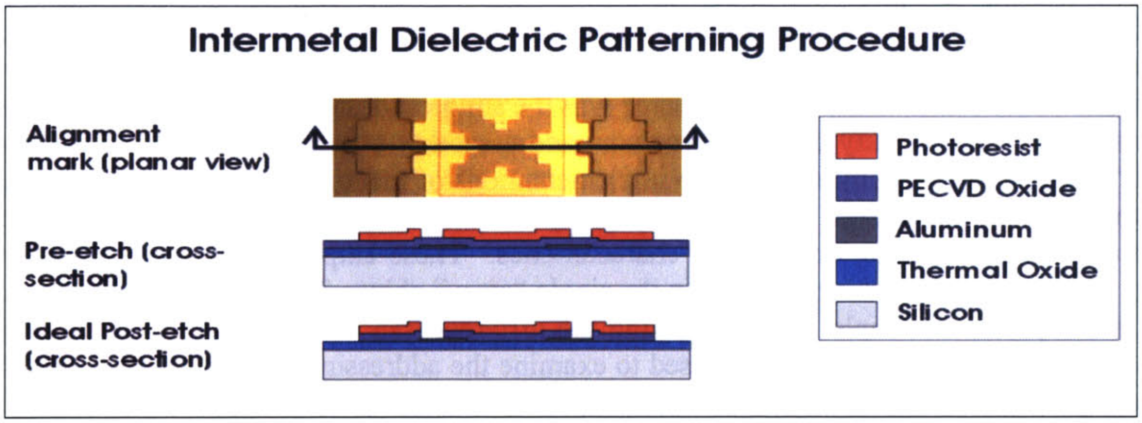
Figure 3-5. My designs were fairly evenly divided between devices incorporating n-DEP trapping techniques and p-DEP trapping techniques. Of primary interest were the designs known as simple "array" chips. These layouts were demonstrations of individual 4 x 4 matrices positioned at the center of the die. This setup was the simplest design rendered for implementing and testing the functionality of my row/column addressability scheme. Secondly I developed a set of "matrix" chips incorporating three implementations of the 4 x 4 grid structures associated with the single "array" chips. I designed this group to assess both addressability and examine the effect of inter-trap spacing on trapping characteristics. These chips use a novel layout pattern which requires no more control lines than the single "array" chips. The third group of chips uses layouts comprised of simple rows containing the different trap designs chosen for the project. While these "row" designs can not be used to examine the addressing scheme they are useful for validating the simulation work discussed in Chapter 2. With these chips, concerns related to trap holding characteristics can be checked experimentally. The final chip type is useful for determining cell size considerations for future layouts. It incorporates a series of distinct STS-etched well structures of various diameters. These wells have no associated control electrodes and simply serve as a platform for evaluating which well diameters are best suited for cell capture and containment. Not shown in Figure 3-5 were an additional ancillary series of layouts developed for the sake of demonstration purposes only. Those chips which again incorporated both n-DEP and p-DEP methodologies served to capture large groups of cells and then release certain sets of them to spell out the words M-I-T. I created this set of chips such that I could later make interesting movies detailing DEP trapping behavior.

All of the layout was performed using five separate mask layers. I used different patterns for each of the two metal levels, one for the intermetal dielectric, another for the thermal oxide and STS etches, and a final mask for the SU-8 dam layout. All masks with the exception of the SU-8 layer design (created through a transfer process from an overhead transparency to a photopaternable chrome plate) were purchased from Advanced Reproductions (North Andover, MA) and laser etched into chrome coated glass plates.

3.3. Miniprocess Validation

Despite developing what appeared to be a viable full process flow (see Appendices I and II), after submitting my design to the PTC, I was asked to run a demonstration of the intermetal dielectric patterning procedure before gaining a full process approval. This sequence, employing the Silox Vapox III product, required the PTC to consider incorporation of a new fabrication etchant in the MTL clean room environment. I therefore ran a "miniprocess" to evaluate the etchant's behavior and demonstrate its functionality.

For this study I took a single silicon wafer and pushed it through the process steps associated with thermal oxidation, M1 patterning, and the subsequent PECVD oxide deposition (see steps 1-10 in the full process flow provided in Appendix I). Then, rather than depositing and patterning the M2 level as I would in the full process flow, I patterned photoresist using the PECVD oxide mask. After cleaving the wafer, using a hand scribe, I immersed samples into beakers filled with Silox Vapox III for varying percentages of the manufacturer's suggested etch time for the Nanospec-measured (Nanometrics, Sunnyvale, CA) PECVD oxide thickness of 15351Å. I took Dektak (Veeco, Woodbury, NY) profilometer readings to measure the etch


Intermetal Dielectric Patterning Procedure
Alignment mark (planar view)
Pre-etch (cross-section)
Ideal Post-etch (cross-section)
Photoresist
PECVD Oxide
Aluminum
Thermal Oxide
Silicon

Percent Etch time	80%	100%	120%	150%	200%	300%	500%	1000%
Etch depth (μm)	.55	.64	.72	.90	1.16	1.59	1.86	2.87

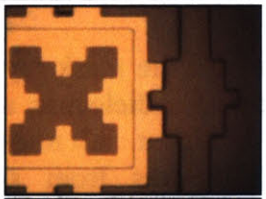
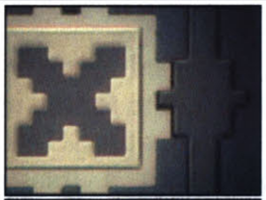
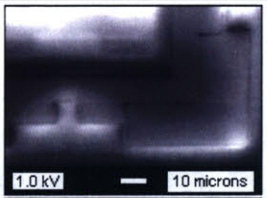
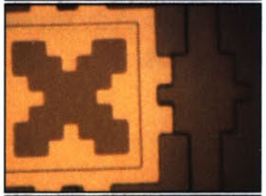
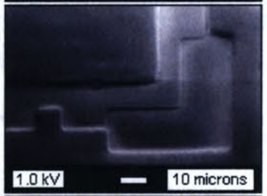
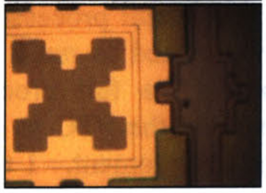
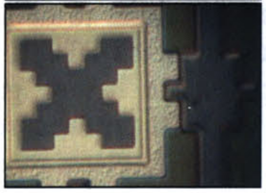
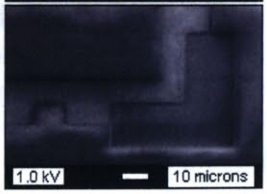
% Sugg. Etch Time (1.5 μm PECVD SiO_2)	**10x BF Optics**	**20x BF Optics**	**20x DIC Optics**	**SEM**
100%				 1.0 kV 10 microns
150%				 1.0 kV 10 microns
1000%				 1.0 kV 10 microns

Figure 3-6: Brief synopsis of the "mini-process" used to evaluate the Silox Vapox intermetal silicon dioxide etch step proposed in my full fabrication process. The top portion of the chart displays the alignment mark and a pair of cross sections detailing the behavior of an ideal etch sequence. The bottom table outlines the effect of exposure to the etchant for a range of times measured as a percentage of the time recommended for a 1.5 μm thick deposited PECVD SiO_2 layer. For the 100% and 150% cases no adverse effects are seen on the quality of the exposed metal surface. Even at 1000% the undercutting of the photoresist and the pocking of the metal surface are not great enough to destroy the aluminum layer. The middle table shows the actual measured etch depths for all examined data points.

depth associated with each of the exposure times and to try to calibrate and measure the actual etch rate associated with the Silox Vapox III etchant. In all instances I examined the alignment marks on exposed wafer samples as they were present on all chips regardless of type.

Figure 3-6 presents a visual summary of some of the key results obtained in this study. Cross-sections of the various materials comprising the alignment mark are outlined along with listings of the various measured etch depths as a function of exposure times. The photo gallery provides an assortment of various alignment mark surface features seen throughout the course of the study. In general, the etchant removed PECVD SiO_2 less aggressively than expected when compared to the manufacturer's suggested rate. Even in cases where the etch proceeded long enough demonstrate excessive undercutting (see the 1000% etch case) and eroded all of the overlying SiO_2, the exposed M1 metal remained intact despite some level of surface pocking. The overall performance of this study indicated that the Silox Vapox III product could potentially serve as a viable intermetal dielectric etch capable of preserving the integrity of exposed metal layers. I presented these results to the PTC and was granted approval for proceeding with my full process. In the remainder of this chapter I outline the specifics of the key steps involved in the full process flow.

3.4. Full Process Assessment

For all of the processes I describe in this section I provide brief overviews of the specifics related to each step and encourage the reader to reference the Appendices at the back of this report for further machine related recipe considerations.

3.4.1. Progressing to the M1 Level

The growth of thermal oxide layers on silicon is a process which requires increasingly lengthy amounts of time for given linear increases in oxide thickness [58]. This behavior results because new oxide growth is only realized at the oxide/silicon interface. As thermal oxides become thicker and thicker oxygen species in the surrounding heated atmosphere must diffuse over greater distances through the already-grown oxide to the underlying silicon. As my process targeted a substantially thick oxide of 1.5 μm, I opted for a wet oxidation process to minimize the required furnace time and thus reduce the expense of this particular fabrication step. Rather than performing this step myself, MTL staff ran this process in the Thermco 10K 5C-ThickOx tube over the course of approximately 10 hours to produce thermal oxides with an average thickness of 15220Å.

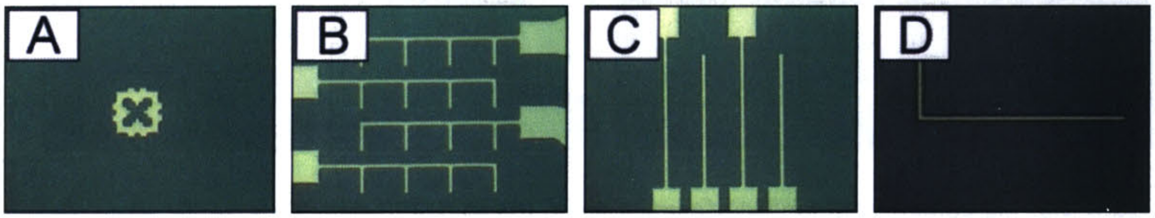


Figure 3-7: Process pictures displaying (A) the alignment mark, (B) an n-DEP grid, (C) a p-DEP grid, and (D) a 3μm -wide line after patterning the first level of aluminum.

I then sputter coated the oxidized wafers using the Endura (Applied Materials, Santa Clara, CA) aluminum deposition recipe set for a 5000Å target thickness (see Appendix V). The resulting metal film was very uniform and highly reflective. After coating the wafers with SPR 700-1.2 photoresist (Shipley) using the standard T1HMDS recipe (see Appendix III) on the ICL Coater6 (Semiconductor Systems), I exposed the M1 layer using a 2.5 second exposure on the EV1 (Electronic Visions, Phoenix, AZ) and then developed my wafers using the standard DEV6 recipe (see again Appendix III) on Coater6. With the wafers thus prepped I proceeded to the Rainbow plasma etching tool where I developed and used a personalized recipe (see Appendix IV) for patterning the M1 layer. Figure 3-7 details four specific features of this patterning sequence. In all case I witnessed minimal undercutting and straight edge features. This etch, which required a great deal of process refinement, enabled effective patterning of features even as small as 3 μm linewidths.

3.4.2. Moving to the M2 Sequence

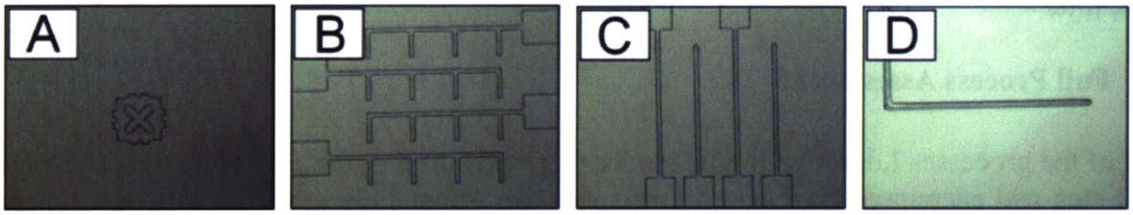


Figure 3-8: Images of the same four features displayed in Figure 3-7 with overlying PECVD oxide and aluminum layers. This set of images indicates that the underlying feature patterned in the MI layer are clearly visible at this stage, thus enabling effective M2 pattern alignment.

After depositing a 1.5 μm thick oxide using the Concept One PECVD silicon dioxide recipe (see Appendix V), I coated my wafers again with a second level of metal in the Endura sputtering system. Because aluminum layers, even as thin as 5000 Å are not transparent in the visible spectrum, I was concerned that I would have trouble aligning the M2 aluminum patterning mask to the underlying M1 layer. As Figure 3-8 indicates I could easily locate the necessary alignment patterns, despite their coverage by an oxide layer and a metal layer.

Using the same coat, expose, and develop routines on the Coater6 and EV1 machines as I had

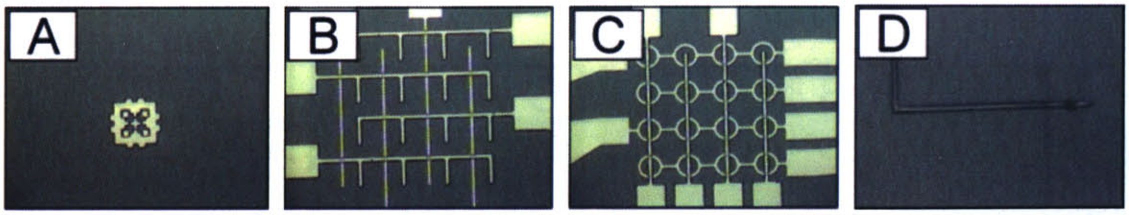


Figure 3-9: M2 patterning of the (A) alignment mark, (B) an n-DEP grid, (C) a p-DEP array, and (D) a 3μm-wide line. All features show up nicely and well aligned except for the 3μm-wide line which was overetched on the specific wafer photographed. Revisions in the M2 etch recipe reduced this effect in subsequent wafers.

used in the M1 sequence, I established the M2 photoresist pattern and subsequently etched it into the M2 layer using my developed process recipe in Rainbow. Figure 3-9 displays the finalized M2 patterning stage and again indicates the presence of nice, straight edge features and very tight alignment between the two metal layers. Figure 3-9 (D) indicates that the 3 μm wide line running vertically in the image was unintentionally sacrificed at this stage; subsequent Rainbow process modifications eliminated this effect for future wafers.

3.4.3. The Intermetal Dielectric Etch

Despite the apparent success of the miniprocess used for evaluating the intermetal dielectric etch, my first attempt to conduct such a procedure on a full process wafer amounted to a dismal disaster. Figure 3-10 portrays the same set of features examined in the preceding full process picture sequences. Here the alignment mark appears fairly well intact, but the n-DEP, p-DEP and 3 μm wide line features all highlight severe damage to the intermetal oxide layers and in some cases the metal lines. Rather than inching up on the final etch time in the conservative fashion adopted in the mini-process, I assumed that the etch rate for the Silox Vapox III product was better described by my mini-process study than the manufacturer's recommendation. In my first etch exposure with a full process prime wafer I therefore submersed the wafer for 80% of the time required for etching the nominal 1.5 μm PECVD oxide layer with an estimated etch rate of 1500 Å/minute. Despite indications from the miniprocess evaluation seemingly highlighting the safety of overetching in this step, my full wafer adaptation of the process proved otherwise. Possible reasons for the difference between the two processes could have involved differences in ambient temperatures in the clean room environment on the separate occasions resulting in unique and different etch rates; distinct humiditiy conditions for each process which could have rendered poor adhesion between layers in the stacked material system and subsequent leaching of the etchant into undesired regions on the prime wafer; or loading effects wherein the size of a given feature governs its etch rate. The last of these three suggestions could explain why the alignment mark shown in Figure 3-10 remains fairly well intact as compared to the other smaller examined items. Perhaps monitoring the alignment mark was a poor choice for understanding the etch behavior in my miniprocess and when translated to the full process proved painfully inadequate.

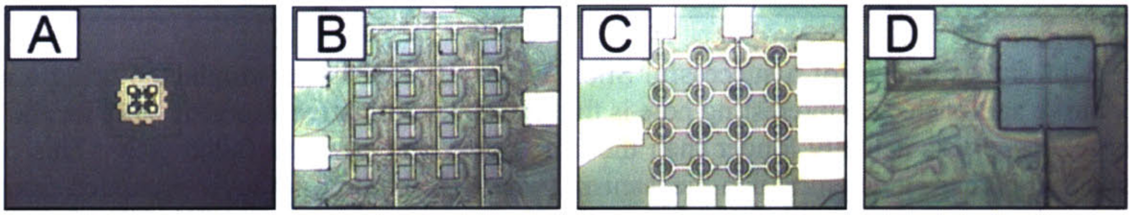


Figure 3-10: Images of the same features seen in the preceding process figures for a failed intermetal SiO_2 etch. Despite the appearance of the alignment mark all of the other examined features display dramatic overetching and apparent leaching of the Silox Vapox III product between process layers.

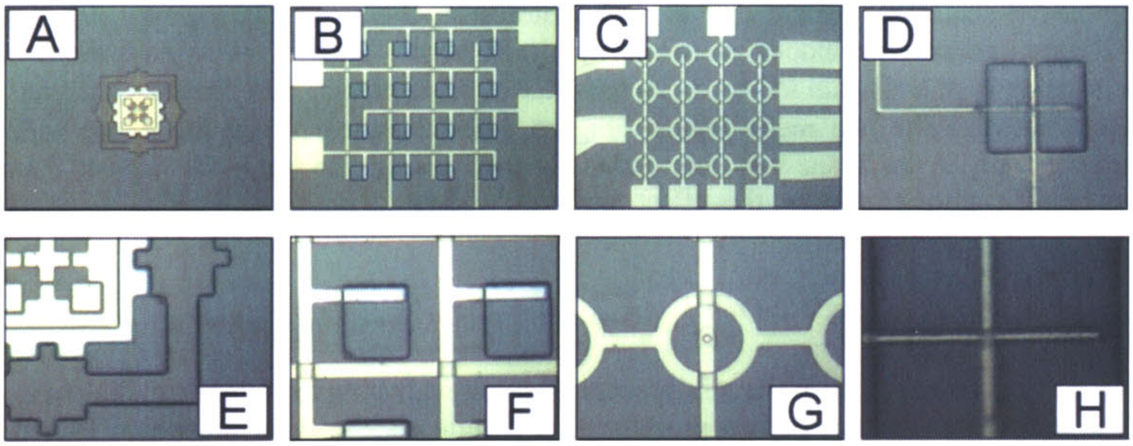


Figure 3-11: Images of a successful intermetalic oxide etch. (A)-(D) display the same four images seen in earlier process photos, while (E)-(H) present zoomed in perspectives.

Figure 3-11 shows images of a successful Silox Vapox III etch I later conducted using a more conservative approach. An interesting note is that the total cumulative exposure time for the etch in this sequence was actually longer than the time associated with the failed etch. This result suggests that perhaps a delamination mechanism (where the photoresist layer separated from the underlying layers) caused the failure outlined in Figure 3-10 rather than a modification of the etch rate with temperature. If this estimation is the case, then ample support is offered for diligently checking the relative humidity levels, which can cause resist swelling and hence delamination, on days when photoresist sequences are to be carried out.

The biggest challenge associated with successfully running an intermetal dielectric etch of this sort is that there is no etch stop material involved with the process and no easy method for detecting when the PECVD oxide has been cleared from underlying M1 structures. To evaluate etch depths, I exposed the wafer to Silox Vapox III for incremental amounts of time, ran spin dry operations and then conducted a series of Dektak profilometer measurements to read step-height changes in the exposed regions. When the Dektak step heights stopped changing for scans across the M1 layer I assumed that the aluminum had been reached. For further support I visually examined the wafers under an optical microscope and searched for evidence of surface roughening on exposed metal features. In most cases, I witnessed slight necking of the metal regions exposed to the etchant and considered this sufficient evidence to suggest that the etch had run to completion. Ensuring cross-wafer etch completion meant that some exposed areas actually ended up being a bit overetched while others were just sufficiently etched.

3.4.4. Thermal Oxide Patterning and the STS Etch

The second to last mask layer, served to pattern both the thermal oxide and STS pit layouts in my device designs. With one application of a defined photoresist pattern two sequential etches were thus run without the standard intermediary stripping process generally seen. My first attempt to run this sequential etch resulted in disastrous effects (see Figure 3-12) from the get go. In a fashion similar to that seen for the failed intermetal oxide etch, I witnessed a large degree of what appeared to be etchant leaching between layers in the stacked material system. In this first failed attempt I used a wet Buffered Oxide Etch (BOE) to try and run what is generally considered a "standard" processing etch step. Unexpectedly, regions that I had hoped to preserve were exposed to the hydrofluoric acid-based etch and many of my drive electrodes were destroyed or damaged beyond usability.

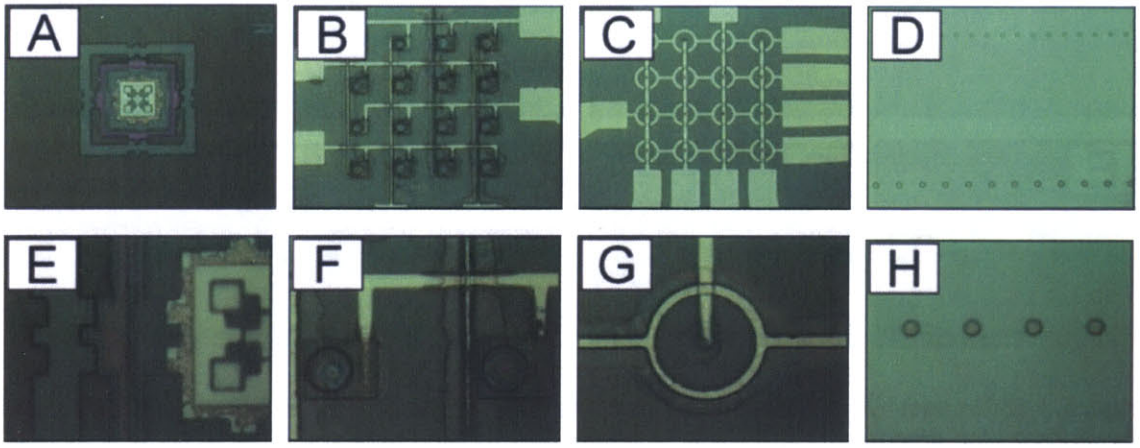


Figure 3-12: Images of an unsuccessful BOE etch used to target the thermal oxide layer. (A)-(C) and (E)-(G) examine the alignment mark, n-DEP traps, and p-DEP traps at two levels of magnification. (D) and (H) show a set of holes used in the cell-sizing chip. In all images but (D) and (H) there is significant undercutting and etching of undesired locations. As this behavior is not seen in (D) and (H), which are inherently less complicated structures, there is a suggestion that the failure of this etch is dependent upon either poor adhesion between prior process layers, or an insufficient photoresist thickness resulting in exposed sidewalls.

I did not expect this behavior and it ended up being quite a setback for realizing final design implementations. Two possible explanations come to mind for describing this behavior. Perhaps humidity in the clean room environment was sufficient enough to hinder adhesion between the photoresist and underlying materials thus enabled lateral etching outside of the prescribed regions. It is also possible to image that the previously-patterned metal and PECVD oxide layers presented step heights substantial enough to reduce the effective sidewall coverage in certain regions around the traps. Lacking sufficient sidewall coverage could have presented new avenues for the BOE to etch in undesirable ways. The failure of the BOE wet etch in Figure 3-12 prevented any subsequent aims for running an STS etch.

On the chance that improper sidewall coverage was the failure mechanism, I revamped the set of preceding photoresist coating procedures by running the TAFFC and TAFFD (See Appendix III) programs on Coater6 while boosting EV1 exposure times from 2.5 seconds to 6.5 seconds. This alternative coating routine presented a slower wafer spin speed and produced a thicker photoresist layer (on the order of 2.7 μm). On the chance that delamination was a cause for the etch failure, I spoke with the PTC and modified my process design to utilize the anisotropic oxide etching capabilities of the AME 5000. The use of a thicker photoresist coating further helped to ensuring that the desired etch pattern would be preserved throughout the two sequential anisotropic etch procedures (thermal oxide and silicon etches). While I am still uncertain about the specific cause for the response shown in Figure 3-12, increasing the photoresist thickness and opting for the plasma etch (I used the cyclic Oxide Pegasus recipe, see Appendix IV), rendered a successful patterning of the thermal oxide layer as shown in the top half of Figure 3-13.

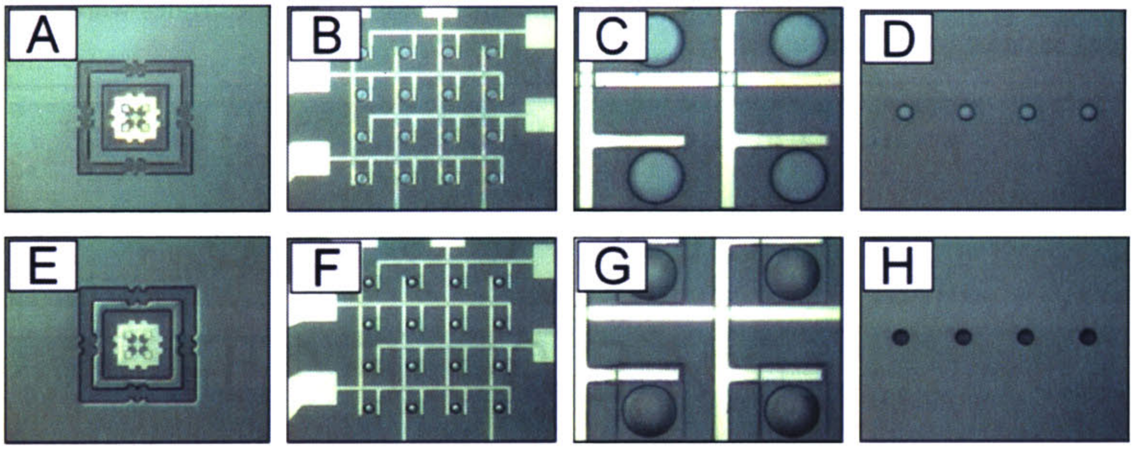


Figure 3-13: Images (A)-(D) display the same features shown in Figure 3-? after a switch to a dry plasma etch process in AME 5000. Minimal undercutting appears. (E)-(H) show again the same images after the STS step. Aside from building the fluid dam and a few subsequent packaging steps, these images present the chips in their final functional form.

The success of the thermal oxide etch allowed me to move onward to the STS reactive ion etch sequence. A host of images outlining a successful STS etch are shown in the lower half of Figure 3-13. To target a 20 μm depth for this step, I used the STSHAL-A (see Appendix IV) recipe on STS2 and incrementally measured the pit depths using the WYKO Optical Profilometer (Veeco, Woodbury, NY). I provide an outline of the sequence of information obtained for the final etch depth in Figure 3-14. The measured pit depths are on the order of 22 μm, which ultimately produced actual pit depths of 20 μm once a 2 μm layer of photoresist was stripped from the wafer's top surface.

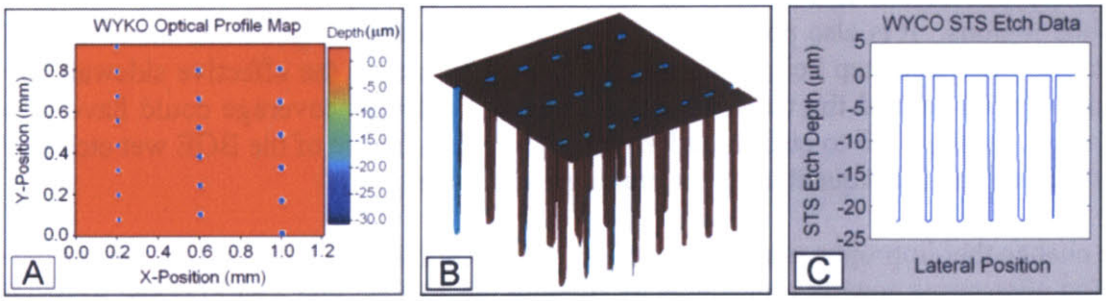


Figure 3-14: Images of the data used to calibrate the STS etch step in the process. (A) shows a planar view of the optical profile rendered for the final etch depth. Picture (B) is a Matlab graphic of the 3-D data extracted from (A). For ease of depth measurement, I also show a plot along one of the rows of etched holes (C). Subtracting out a 2 μm height for the photoresist layer, the 20 μm target depth was easily reached.

3.4.5. *An Exit Strategy for MTL*

Completing the STS etch opened the door for the use of gold-contaminated processes. In some cases I continued to process my wafers in MTL to render 100 μm thick SU-8 fluidic dam layers (see Appendix III for the specific protocol). Such a procedure required the bulk of a day as the SU-8 bake times are exceptionally lengthy and the sticky nature of the negative photoresist makes alignment in EV1 a complicated endeavor. Oftentimes the wafer would adhere to the SU-8 mask layer and pose great difficulties for using X, Y, and θ alignment adjustment. Even when I managed to align and pattern a substantially uniform SU-8 layer on a wafer I often witnessed adhesion difficulties between the SU-8 and the substrate which resulted in a tendency for the dams to pop off from the surface of the wafer.

As a design alternative, in some cases, I skipped the SU-8 sequence and went straight to the die saw. Afterwards I would place a PDMS gasket on the surface of the wafer and thus render a fluidic dam without the hassle of SU-8 processing. These alternative chamber types presented larger volumes than those associated with the SU-8 dams, which meant that I could inject cells into the chambers at lower volumetric concentrations and still witness substantial cell counts for DEP capture.

I present the remaining fabrication steps associated with the packaging sequence in Chapter 4 as a precursor for the description of the experimental set up used when testing my designs. In the end my designed process, despite being lengthy and challenging, proved successful and I managed to push an entire wafer (rendering 80 chips) through a full fabrication cycle.

Chapter 4: Design Evaluation

Introduction

In this chapter I begin by discussing the "back-end" portion of my process flow and detail specifics involved with chip packaging. This survey should aid the reader in understanding how the DEP devices are linked to peripheral electronic and fluidic equipment and cascade into an examination of the general experimental set up used for design testing. A pandect of the routines used to conduct design evaluations to date is also offered, specifically calling attention to preliminary experiments run to assess cell/substrate interactions and unexpected challenges associated device operation.

4.1. Chip Packaging

4.1.1. Final Process Steps

As a final preparation in the push towards packaging, I coated individual wafers with thick blankets of OCG 825 positive photoresist (Rohm and Haas, Philadelphia, PA) and then baked them for half an hour at 90 °C. This application served as a temporary protective layer for minimizing the impact that diesaw slurry could have on the endpoint functionality of my devices. (In general cluttering the surface of a chip with silicon residue could disrupt DEP trapping capabilities by undesirably masking the electrodes.) With the protective layer in place, I pushed wafers through a dicing routine using the 2060 blade (cuts streets 220 μm wide) on the DAD-2H/6T diesaw (Disco, Santa Clara, CA) available in ICL. The agitation accompanying the waterjet used to cool the cutting blade unfortunately also served to separate individual die from the backside adhesive mounting layer. Separated chips were then whisked down stream where they often landed facedown on the diesaw table and were subjected to more contamination and handling than necessary. I also observed additional separations between SU-8-based dam layers and die surfaces as a result of waterjet bombardment. Challenges aside sets of 13mm x 13mm chips eventually came off the line and were ready for mounting on printed circuit boards. A single PCB layout was used for packaging all chip designs (regardless of type) and establishing a platform for electrical and fluidic ties to the "outside world." The general configuration of the chip package is shown in Figure 4-1 in an exploded diagram format along with an actual photograph of an experimental assembly.

4.1.2. The General Layout

In this design, I affix a 9mm x 9mm Bellco coverslip (Electron Microscopy Sciences, Ft. Washington, PA) to a dam layer (either SU-8- or PDMS-based as discussed in the final portion of Chapter 3) using high performance fiberglass-reinforced epoxy (Loctite). The chip/flow chamber assembly is bonded to the underlying PCB (ExpressPCB, Santa Barbara, CA) using a stack of several layers of double-sided tape. This tape bond has a pair of holes cut in it which align to a set of vias in the underlying PCB and a matching pair of through holes hand-drilled

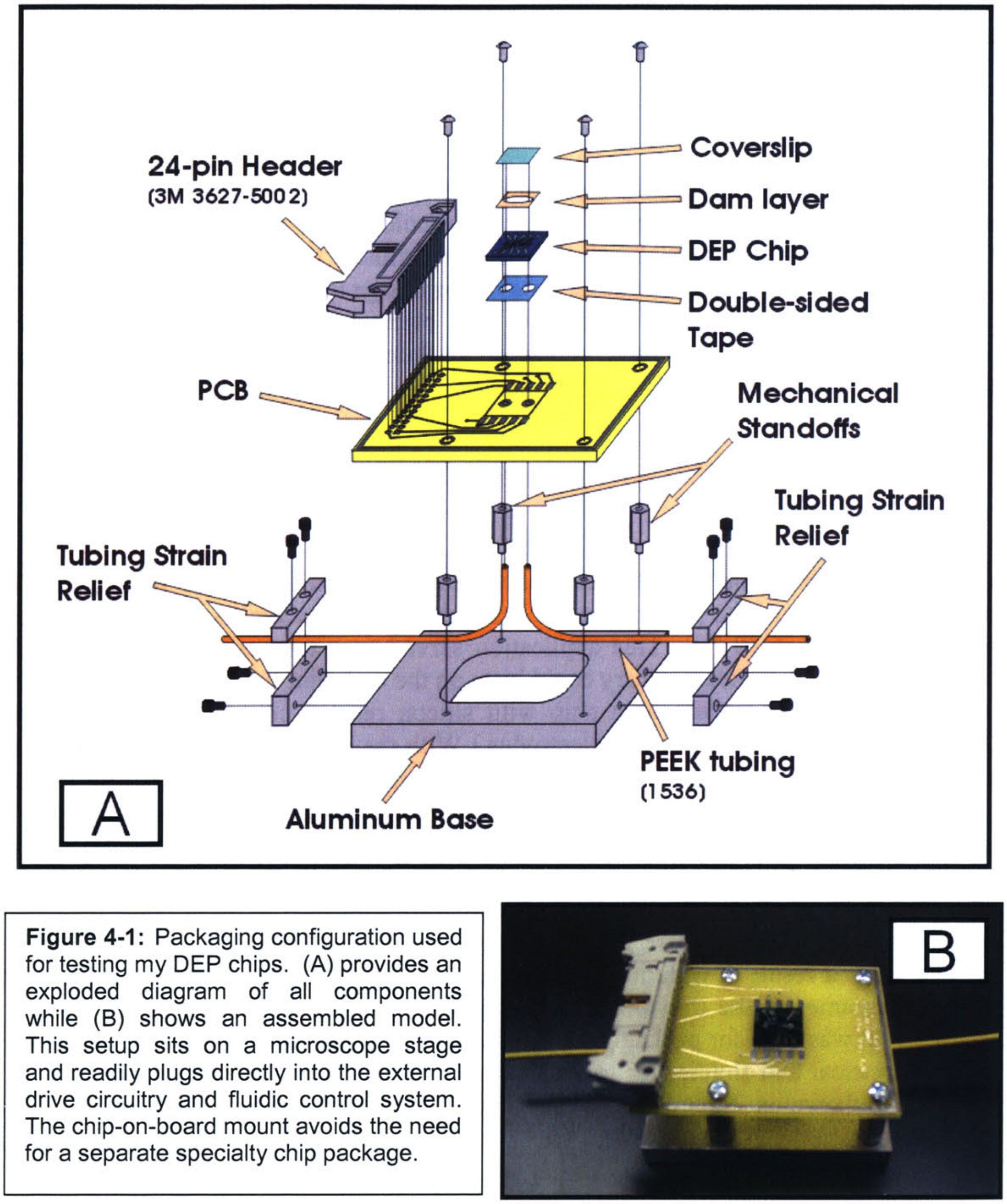

24-pin Header
(3M 3627-5002)
Coverslip
Dam layer
DEP Chip
Double-sided Tape
PCB
Mechanical Standoffs
Tubing Strain Relief
Tubing Strain Relief
PEEK tubing
(1536)
A
Aluminum Base
B

Figure 4-1: Packaging configuration used for testing my DEP chips. (A) provides an exploded diagram of all components while (B) shows an assembled model. This setup sits on a microscope stage and readily plugs directly into the external drive circuitry and fluidic control system. The chip-on-board mount avoids the need for a separate specialty chip package.

using a Triple Ripple .75 mm diameter diamond drillbit from C.R. Laurence Co (Los Angeles, CA) powered using a Dremel (Mount Prospect, IL) model 380-6 variable speed Moto-tool. (Regardless of dam type, all through holes were drilled prior to mounting the top glass coverslip. This approach ensured that most of the debris associated with the drilling procedure could be removed from the chips before enclosing the final flow chambers. It was after this drilling sequence that I removed the final protective layer of photoresist using sequential baths of acetone, methanol, and isopropanol.) For electrical connections between the PCB and the DEP chips I used a Kulicke and Soffa model 4123 (Willow Grove, PA) wirebonding tool. The on-board electrical traces were then run to a 3M (Maplewood, MN) 3627-5002 pin connector where a link was made to the external control circuitry using a ribbon cable. The general packaging architecture also includes a set of four mechanical standoffs which affix the PCB/chip structure to an underlying aluminum support plate. This machined plate provides a solid base which easily rests on the stage of an upright microscope while allowing tubing connections on the underside of the printed circuit board. To link the tubing to the DEP chip I specifically designed the vias in the PCB such that 1/16" outer diameter 1536 PEEK tubing (Upchurch Scientific, Oak Harbor, WA) could be wedged snuggly inside. I then applied the same high-performance epoxy used when sealing the dam layer to caulk around the back-side connections. As an added safety feature I machined a pair of mechanical strain reliefs as a part of the overall package design. These items amounted to a set of clamps capable of grabbing the package tubing and thus minimizing the possibility of accidentally ripping one or both of the fluidic port connections from the underside of the chip.

4.1.3. Benefits and Challenges

Overall this package design functioned quite well. It afforded simple connections to off-chip electronics as well as the fluidic control system. The package also easily mounted on an upright microscope stage and thus provided simple top-side device imaging. The design is also readily portable and it demonstrates a substantial level of mechanical robustness.

Establishing the electrical contacts between DEP chips and the underlying PCB backbone was undoubtedly the most challenging component of the packaging sequence. Oftentimes it was difficult to form wirebonds on the PCB bond pads. I saw slight improvements in this operation after cleaning the board-based pads using a cotton swap dipped in isopropanol. Roughing the surface of such pads using a razor blade seemed to have little to no effect on the potential for bonding. Maxing out the force, time, and power settings on the wirebonder was most beneficial. In general a ball bond (the first bond made when installing a wirebond) is a stronger, more easily formed bond than a wedge bond (the second bond made in a wirebond connection).

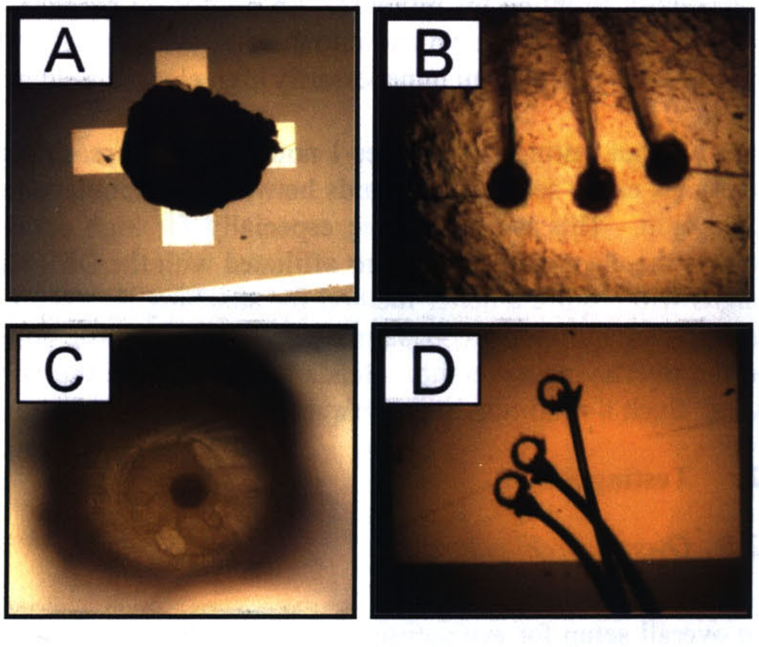


Figure 4-2: Key features for establishing the fluidic and electrical connections between DEP chips and the packaging setup. Image (A) shows the "cross" feature on each layout used to position the manually-drilled through holes which mate to the backside PEEK tubing. (C) provides a close-up of the hole demonstrating proper alignment with the bore of the tubing. (B) and (D) illustrate successful ball and wedge wire bonds respectively.

Using ball bonds on the PCB pads unsurprisingly served to create more successful connections than when placing them on the chip pads. Images (B) and (D) in Figure 4-2 provide pictures of successful ball and wedge bonds made in a sample packaging setup. As is seen, redundant wirebonds were established for each chip to board connection to provide system failsafes.

Despite the crude hand-drilling technique used for establishing through holes in the silicon substrates, alignment with the PEEK tubing connections on the back-side of the PCB proved to be quite impressive. Images (A) and (C) in Figure 4-2 demonstrate this alignment by examining the cross-shaped drill target using two different levels of magnification. In Image (C), which peers down into the drill hole, the center bore of the back side PEEK tubing appears. This alignment is better than what is necessary for proper fluid delivery. It should be noted here that special care was taken when bonding the backside PEEK tubing to the underbelly of the PCB so as to avoid clogging the tube end with epoxy. Such a clog would prevent fluid delivery and render the entire package useless for experimental evaluations.

As discussed later in this chapter, time constraints and fabrication process failures only permitted an assessment of p-DEP chip behavior during the testing phase of this project. As a result assessing whether or not n-DEP structures were negatively affected by the protective photoresist layer applied just prior to diesaw operations was not afforded. I hold extra concern for the effect that this "safety" protocol may have on n-DEP structures because they incorporate 20 μm deep holes that could seemingly serve as sites where residual photoresist would accumulate and require extra attention for removal. An n-DEP pit clogged with photoresist would not permit a cell to fall completely down and into the designed cavity which could pose problems for trapping while exposing cells to an unnecessarily high electric field environment.

Once I began testing my devices I noticed that increasing the pressure in the fluid system did sometimes cause seepage of liquids between the double-sided tape bond layers on the back side of the chip. This is problematic especially for high conductivity buffers if the leaking fluid contacts the electrical connections affiliated with the DEP chip causing unwanted shorts. Future designs will require a better method for attaching the chip to the circuit board. Additionally, in the chips reliant upon SU-8 dam layers there was little adhesion between the top SU-8 surface and the overlaying coverslip. Beads and cells were therefore often trapped between these two layers. Such a condition begs the question of how clean the chambers can be on subsequent uses.

4.2. Testing Setup

4.2.1. Overall Architecture

The overall setup for evaluating DEP chips fabbed in this thesis is shown in Figure 4-3. For the fluidic connections four separate solutions and three different valves are necessary. The first valve en route downstream to the chamber selects between two pump-driven 5 mL syringes (Hamilton, Reno, NV) containing in one case 10X Trypsin-EDTA (Gibco, Carlsbad, CA) and in another a cell- or bead-free stock media solution (see the list below for an outline of the different solutions used in different applications). The second valve selects between either a pump-driven fluid or a 70% ethyl alcohol (ETOH) flush solution. At the onset of each experiment the syringe pump is left deactivated while this second selection valve is turn to permit an initial injection of ethyl alcohol. In addition to cleaning the inside of the chamber, this fluid tends to wet the inside surface better than water-based solutions. The alcohol therefore reduces the likelihood of trapping bubbles inside the flow chamber thereby avoiding a possible mechanism for interfering with DEP trapping forces in the system. Because this initial flush is done prior to cell or bead injection it is not crucial that the flow rate is well controlled. The ETOH solution is therefore manually driven rather than being powered by a syringe pump. The final valve in the series of three is an Upchurch Scientific 6-port injection valve. This device connects to a sample loop of variable length (and therefore volume) that is supplied by a concentrated cell or bead and media solution. This solution is the same as that found in the media syringe powered by the syringe pump with the exception that it also contains microparticles of a prescribed type. The injection valve places a plug of cell- or bead-containing media in the flow path to the chamber. The benefit of such a device is that it can reduce the total number of cells needed for establishing a given density inside of the chamber and it can introduce cells in controlled numbers at specified times.

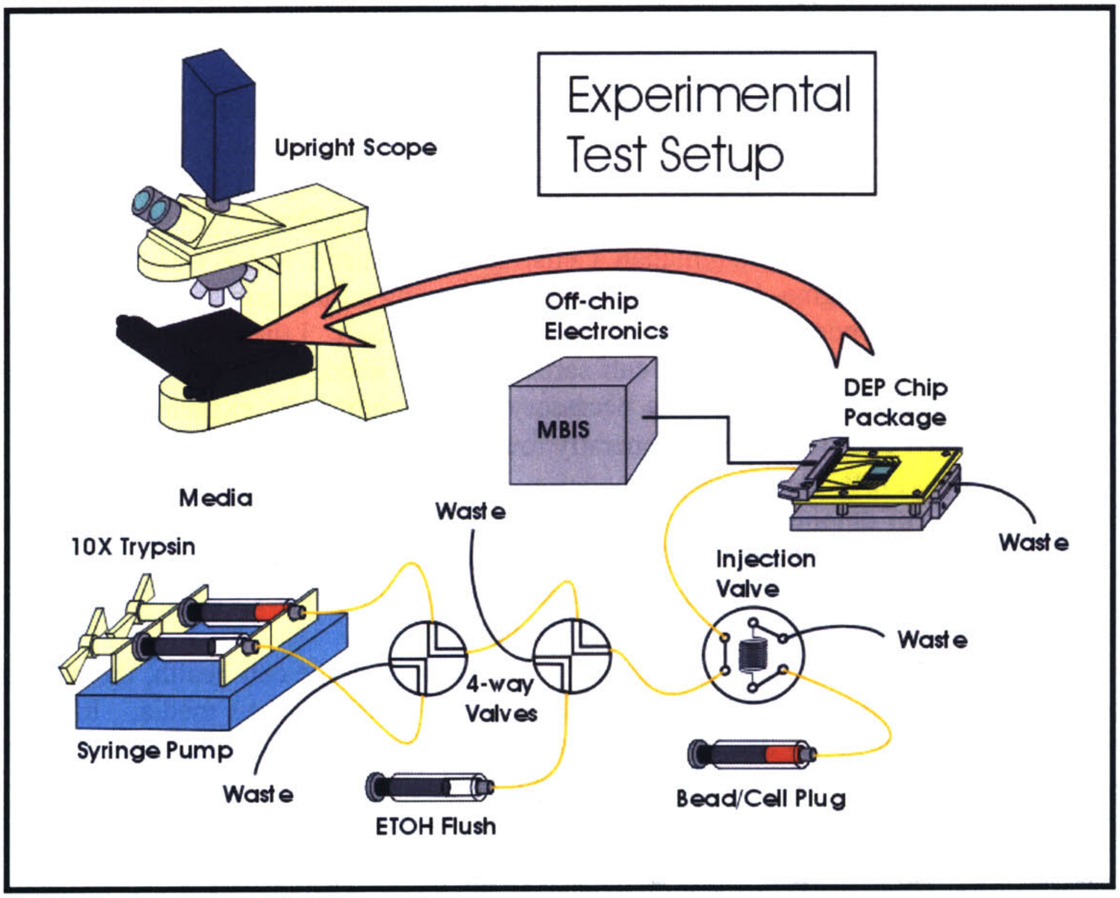

Experimental Test Setup
Upright Scope
Off-chip Electronics
MBIS
DEP Chip Package
Media
10X Trypsin
Waste
Injection Valve
Waste
Waste
4-way Valves
Syringe Pump
Waste
ETOH Flush
Bead/Cell Plug

Figure 4-3: Overview of the test setup for evaluating DEP trap behavior.

The off-chip electronics reduce to a simplified "black-box" description in Figure 4-3 labeled as the matrix buffer inverter switch or MBIS for short. This external control circuitry amounts to a series of low-noise op-amp stages that preserve or invert the signal produced by an Agilent (Palo Alto, CA) 33250A waveform generator. This external circuitry is controlled using a Matlab-generated graphical user interface (GUI) on an accompanying desktop PC. Through the GUI individual rows and columns in the arrays present on my DEP chips can be activated or deactivated with the click of a mouse.

4.2.2. Solution Compositions

Depending upon whether cells or beads are being examined in an experiment presents certain flexibilities for the make-up of the stock solutions used. The bulleted list shown in this section, provides a comprehensive outline of the different options chosen for chip tests as well as descriptions of solutions envisioned for future n-DEP studies. I used 20 μm diameter Polybeads (Polysciences, Warrington, PA) for all bead-based investigations. To minimize any potential effect imposed by their native suspension solution, I ran five repeated wash cycles with the stock solution used in a given experiment prior to injecting them into the system. These wash cycles involved suspension of the beads in the requisite media, vortexing, centrifugation (5 minutes at 1000 rpm), and aspiration of the supernatant. For all bead/cell plug solutions, densities were set to approximately 5×10^6 microparticles/mL using centrifuge-based concentration.

- p-DEP Operation Using Polystyrene Beads: This stock solution was comprised of deionized water containing Triton X-100 (Sigma-Aldrich, St. Louis, MO) detergent at a 0.05% (by volume) concentration to minimize cell clumping. This solution generally demonstrated a measured conductivity of approximately 3 μS/cm.
- p-DEP Operation With Mammalian Cells: First deionized water was combined with granular sucrose (Sigma-Aldrich, St. Louis, MO) using a magnetic stir bar on a hot plate set to 120 °C to render a 50% w/v saturated sugar solution. I then combined 20.5 mL of this solution with 1 mL of bovine calf serum (BCS) (Gibco, Carlsbad, CA) and 78.5 mL of deionized water to produce the necessary stock solution for experimental operation. The associated conductivity was generally found to be roughly 126.5 μS/cm.
- Envisioned n-DEP Bead-based Operation: Stock solutions will be comprised of combinations of deionized water and phosphate buffered saline (PBS) (Gibco, Carlsbad, CA). The PBS salt solution will boost the conductivity of the media above that of the beads by introducing ionic charge carriers. Varying amounts of PBS may be necessary for adequate demonstrations of n-DEP behavior.
- Envisioned n-DEP Cell-based Operation: To better preserve cell health, these solutions will likely incorporate DMEM or RPMI (Gibco, Carlsbad, CA) media. In any case serum-starved solutions (those containing 0% fetal bovine serum (FBS) or BCS) would likely minimize the tendency for cells to randomly adhere to undesirable locations on the chip. For the case of 3T3-based assays one possible solution might include a 97% DMEM, 2% L-glutamine, and 1% Penstrep mixture.
- CellTracker Green CMFDA and Orange CMTMR Dyes (Molecular Probes, Eugene OR): To stain cells for fluorescence studies I generated stock 10mM dye solutions by dissolving the sold lyophilized products in DMSO (Sigma-Aldrich, St. Louis, MO). I then took these stock solutions and further diluted them using serum-free media to final 5 μM working solutions. To dye the cells I incubated each desired cell type in the necessary working solution at 37 °C for 45 minute time-spans. The cells were then resuspended in their usual media until just prior to on-chip operations. A 41001 model FITC filter set (Chroma, Rockingham, VT) was used for the green dye and a 31000

model Cy3 filter set (Chroma, Rockingham, VT) was used for imaging the orange dye during fluorescent studies.

4.3. Attach and Release Studies

4.3.1. Overview

The microfabrication sequence detailed in Chapter 3 amounted to a very lengthy time investment. Upwards of four months were spent pushing wafers from start to finish. Anticipating the large commitment involved with full wafer fabrication, I sought other avenues for gaining preliminary empirical information regarding chip operation. Of chief concern was a desire to understand various details of cell/substrate interactions. Specifically I hoped to understand what sort of time window might be required for allowing trapped cells to adhere to the substrate and what sorts of flowrates and enzymatic cleaving agents would be necessary for promoting cell detachment when running sorting operations. The first bit of information would offer insight regarding the amount of time that cells would mandate exposure to external electric fields and the second would test the overall viability of anticipated addressability sorting operations.

4.3.2. Cell Attachment

For each of the preliminary attachment assays conducted, six separate 35mm diameter plates were filled with media solutions containing approximately $0.6\text{x}10^6$ 3T3 fibroblasts. Immediately after introducing the media/cell mixtures all six plates were placed into a ThermoForma (Marietta, OH) 370 Steri-cycle hepa-filtered CO_2 incubator. Every fifteen minutes for the span of an hour and a half one of the original six plates was removed from the incubator and then examined and photographed at 10X magnification using a Spot RT Color camera (Diagnostic Instruments, Sterling Heights, MI) and an inverted Axiovert 200 (Zeiss, Thornwood, NY) scope.

To assess cell attachment, five photographs were taken of random regions in the dishes immediately after removing them from the incubator. Following gentle flushs of the dishes with PBS, five random regions were again chosen and photographed. Using Matlab code, I analyzed each of the images generated from the assays and produced quantitative plots showing the percentage of cells that had attached to the bottom surface of the dish at each of the six times surveyed.

This front-end assessment unfortunately offered relatively little insight for defining a cell attachment time window. Wide variations appeared in the times required for cell attachment when comparing repetitions of the same experimental procedures. Utilizing dish surface treatments such as fibronectin and 3T3 media precoating unexpectedly offered little enhancement of cell attachment characteristics. Because the same random regions were not investigated before and after the PBS flush step it was common to count a higher number of cells in the post-flush state than in the pre-flush state. This result meant that systematic errors in the experimental design introduced attachment percentages which often exceeded 100%. Using five random fields wasn't a large enough data set to iron out this complication. I did not manage to develop and run a more involved experiment to better define realistic attachment times prior to the completion of the actual cytometer devices. With the real devices in hand, it now makes less sense to try and run a separate investigation on surface binding using a "dumbed down" evaluation platform. To date I have not yet run additional specific attachment surveys with real devices and attachment times are still open an open question.

4.3.3. Cell Detachment

Investigating cell substrate separations involved the use of PDMS flow chambers. These devices were comprised of 5-7 mm thick PDMS layers patterned with bottom side 30 mm x 3 mm x 100μm cavities. These layers were plasma bonded to 22 mm x 50 mm glass coverslips, Nanostrip-cleaned (Cyantek, Fremont, CA) beforehand for 10 minutes, to form the bottom enclosing surfaces of the cavities. Figure 4-4 depicts this design. Connections to external syringe pumps and waste containment devices were made using PEEK tubing fluidic ports embedded in to the top surface of the PDMS layer. Such a setup offered a controlled environment for cell incubation and a platform for imaging a specified field of cells as it was subjected to fluid flows and different stock solutions.

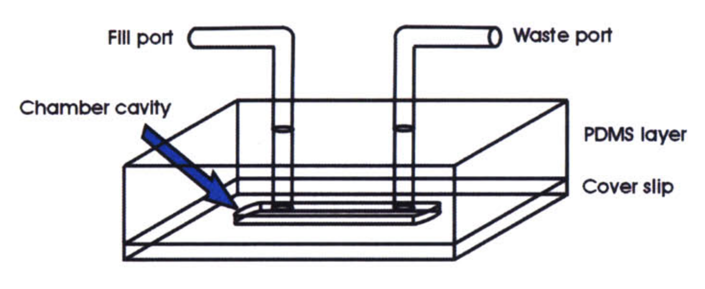


Figure 4-4: Detachment flow chamber assembly

The experimental set up for this evaluation involved the sequential injection of ETOH as a wetting agent, cell-free media as a flush solution and, finally the working solution of 3T3 media, containing approximately 1.8×10^7 cells/mL into the flow chambers. This injection procedure was then followed by an overnight incubation for the chambers at 37 °C in a 5% CO_2 atmosphere. After 12-15 hours of incubation the cells were fully attached to the bottom coverslip surface in the device. The chambers were then placed upon a specially machined microscope mount and attached to peripheral waste and fill tubes. The fill tube was controlled by a KD Scientific 210 C (Holliston, MA) syringe pump and used to introduce either 3T3 media or 10X Trypsin depending upon the assay. The attachment study progressed as follows: first I imaged the chamber prior to any flow injection to establish an experimental starting point; next, flow (either media or Trypsin) was injected into the chamber at a rate of 24 μL/min for a time span of 1.5 minutes. I then halted the flow and imaged the chamber once again as I began a 5 minute soak cycle. Images were recorded one minute into the soak routine as well as at its end. Finally, I reinitiated the flow at a rate of 12 μL/min and imaged the chamber every other minute for the next 27 minutes. In total, I completed seven separate assays in succession as a part of this study. Three of the assays used Trypsin while four were controls run with 3T3 media

I adopted this final routine after gaining some insight regarding the complexities of substrate/membrane interactions witnessed through a series of prior experimental failures. The Nanostrip process used to clean the coverslip surfaces prior to sealing the flow chamber cavities in a plasma bonder emerged as a necessary step for minimizing dramatic fluctuations in cell binding behaviors. I found empirical support suggesting that residual organics present on the coverslip surface could promote cell detachment in uncontrollable ways. Originally I had also supposed that PBS could serve as an adequate control solution for running my assays. After running several assays with this sort of buffer, I unexpectedly witnessed a repeatable cell detachment behavior. Hoping to understand this response I discovered that the lack of magnesium chloride ($MgCl_2$) and calcium chloride ($CaCl_2$) salts in the standard PBS solutions used in our lab could actually serve as a motivator for detachment [59]. I also opted to use a soak time rather than continual fluid flow in my experiments after cultivating some data suggesting that soak times could allow the chemistry involved with detachment promotion to override some of the same effects associated with continual fluid bombardment. Soak times seemed to offer better detachment discrimination when comparing assays run with a control media verses those conducted using enzymatic cleaving agents.

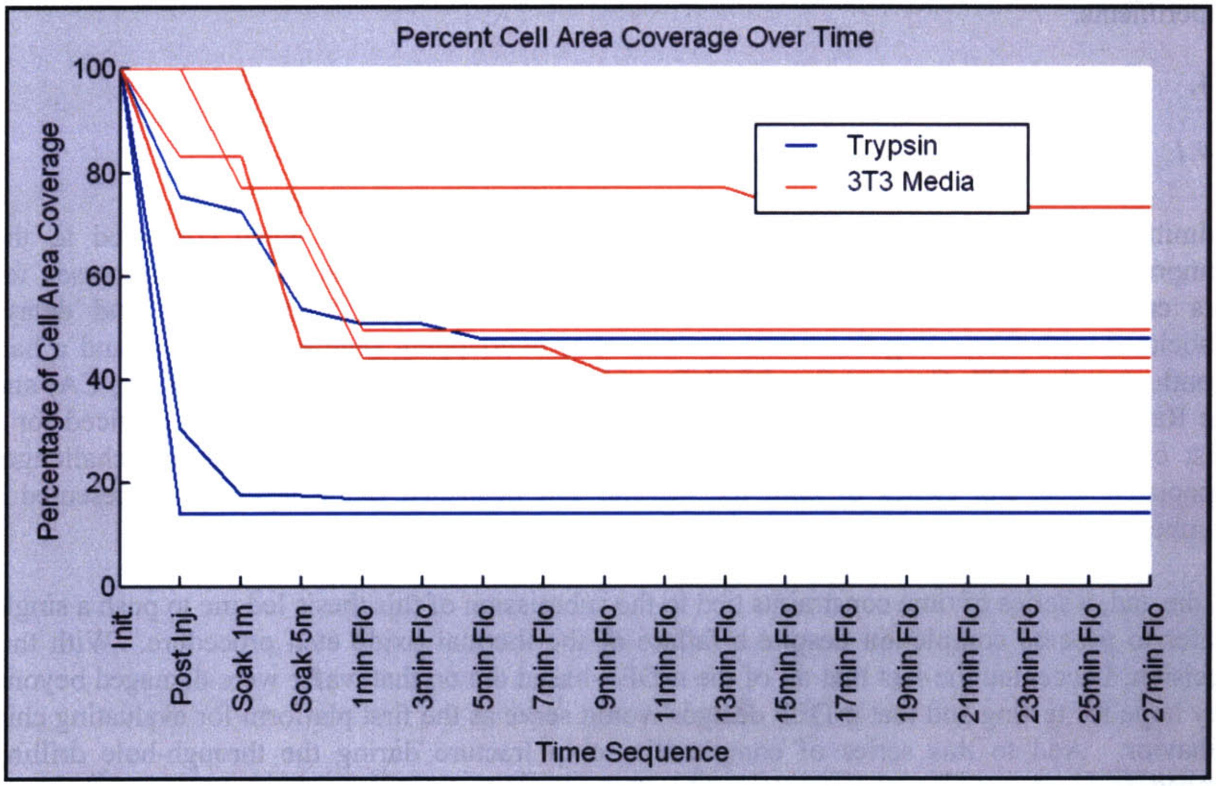


Figure 4-5: Cell detachment investigation. The key feature to note in this plot is the qualitative difference in behavior seen when comparing cells subjected to flow with 10X Trypsin vs. those with 3T3 Media alone. There is a general bifurcation in the data set suggesting that Trypsin is a viable option for promoting cell/surface detachment.

Figure 4-5 highlights the general bifurcated cell detachment response to the media and trypsin solutions. I generated this plot after running Matlab-based image analysis code to automatically extract cell counts from the photos taken during this series of assays and weight them as percentages of detached cells as compared to the initial starting point cell counts. In general, as expected, less detachment was seen when media was used and more cell/substrate separation resulted when trypsin was injected. This plot offered preliminary evidence highlighting the feasibility for removing attached cells from the chip surface during operation of the actual cytometer devices. I ran a statistical t-test on the averaged end-point values for the two solution types presented in Figure 4-5 and produced a p-value of 0.125 for a two-tailed examination assuming that each data set displayed unequal variances. This result indicates that the there is a twelve and a half percent chance that the data from one solution type could have produced the behavioral response seen by the other. This high p-value suggests that the data presented in Figure 4-5 is not terribly robust (in general a benchmark value of 0.05 is a strong indicator of two distinct responses). In all likelihood, this result stems from the single Trypsin run which cuts through the region of the plot dominated by 3T3 media release curves. Better understanding of this response would require a survey of the specific data taken for that Trypsin curve. It is possible that the software used to count cells from the images taken during the experiment failed to properly count the cells located on the surface for this run. I did not specifically examine this data set manually after the fact but will need to do so before proceeding with any further similar experiments.

4.4. Preliminary Chip Tests

4.4.1. Overview

Admittedly the testing phase of this project is somewhat lacking when compared to the comprehensive approach demonstrated in other sections of this report. The primary reason for this condition stems from a seemingly overabundant series of complications and delays associated with fabricating functional devices. For overlapping segments of a two and a half month span the MTL Concept One PECVD oxide deposition tool (Novellus, San Jose, CA) and the Rainbow metal etcher (Lam Research, Fremont, CA) were offline and being serviced for a host of different maintenance operations. As noted in the details of Chapter 3 challenges associated with wet etches of both the thermal and deposited oxide layers also presented a number of setbacks.

In the end, a series of time constraints tied to the submission of this thesis led me to push a single wafer to process completion despite a failure of the thermal oxide etch procedure. With this decision, I accepted the fact that all of the n-DEP-based die on that wafer were damaged beyond any hope for testing and that p-DEP designs would serve as the first platform for evaluating chip behavior. Add to this series of complexities chip fracture during the through-hole drilling procedure and die surface damage caused by improper coverslip bonding and it is understandable that only a very small set of the original 80 chips on the final wafer survived the entire fabrication sequence. In the following portions of this chip testing section I will detail the host of different preliminary evaluations conducted using the surviving p-DEP chips and offer discussion on the implications of those tests for functional characterization.

A special section in Chapter 5 will detail a list of proposed experiments I will run as a part of my planned future involvement with this project.

4.4.2. Electrode Activation in Bead-based Studies

In a very rudimentary attempt to understand my designs, I first entertained the most basic of curiosities by simply injecting a dionized-water-based solution containing polystyrene beads (see section 4.2.2 for specifics) into the chamber, turning off all system fluid flow to allow settling on the surface, and then activating the on-chip electrodes. Through this simple procedure I sought to understand whether or not I had successfully manufactured designs capable of subjecting 20 μm diameter microspheres to dielectrophoretic forces and in turn whether or not those forces could promote the sort of grid-based trapping desired during device operation. I ran this first assay using polystyrene beads to avoid the need for worries about impacting cell health and to sidestep requirements for the more complex stock solutions associated with cell-based assays.

Figure 4-6 highlights this "turn-on" operation. Here, image (A) presents a well-dispersed collection of beads covering the substrate surface. In (B) we witness a complete reorganization of the microparticles. After activation large groups of beads conglomerated in regions between and on top of the control electrodes (regions highlighted by red ellipses). Additionally, eight of the 16 sites in the array yielded bead capture of either single beads or collections of two to three. The site-specific trapping behavior was an encouraging response lending support to the idea that the fabricated devices could operate as planned. The clustering of beads on top of peripheral control electrodes and in the regions between suggested that the witnessed behavior may have included some undesirable n-DEP effects. If the device had been functioning in a strictly positive dielectrophoretic regime a bias toward bead collection around the perimeter of these electrodes (where electric fields are highest) would have been anticipated. The challenges associated with minimizing the conductivity of the stock solution as compared to that of the polystyrene beads eventually motivated the 3T3 cell-based assays discussed later in this Chapter.

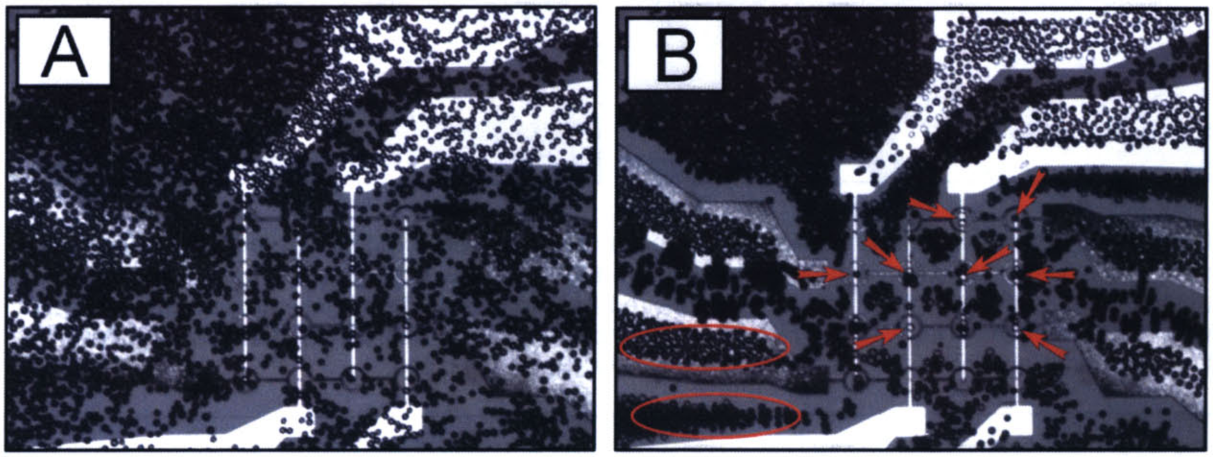


Figure 4-6: Image (A) shows a p-DEP trap array in a deactivated state with polystyrene beads resting on the chip surface. Image (B) highlights this same trap after turning on all control electrodes. The red arrows highlight cells or groups of 2-3 beads that have been capture in this activated state. The red ellipses show a preference for beads to migrate to areas between and on top of (rather than on the edges) electrode structures. This result suggests that an undesirable n-DEP behavior may be taking place.

As a general note the drive voltages used in all chip-base experiments discussed in Chapter 4 were set to 5V peak to peak values using the Matlab-based control software and cycled at 10 MHz. This voltage may have been too substantial for cell-based operations but also may have helped to enable the p-DEP trapping behavior witnessed in the "turn-on" evaluation. As I did not measure the specific output voltage by tapping electrical traces on the PCB chip package it is possible that additional voltage drops across the ribbon cable linking to the MBIS box caused further signal attenuation. Add to this complication any potential drops associated with wirebonded connections and it is feasible that the actual voltage delivered to the chip was far less than that output by the drive circuitry. Future chip evaluation studies may require a full impedance analysis of the packaged system as well as voltage taps on the PCB traces. It is conceivable to imagine a setup where the path from the drive circuitry to the chip electrodes involves so many loses that the original input signal needs amping beyond the 10V peak to peak swing permitted using the current setup. Such a scenario would mandate the use of op-amps demonstrating large slew rates capable of delivering high voltages at high frequencies. This demand is an inherently challenging prospect.

4.4.3. First-pass Attempt at Addressability

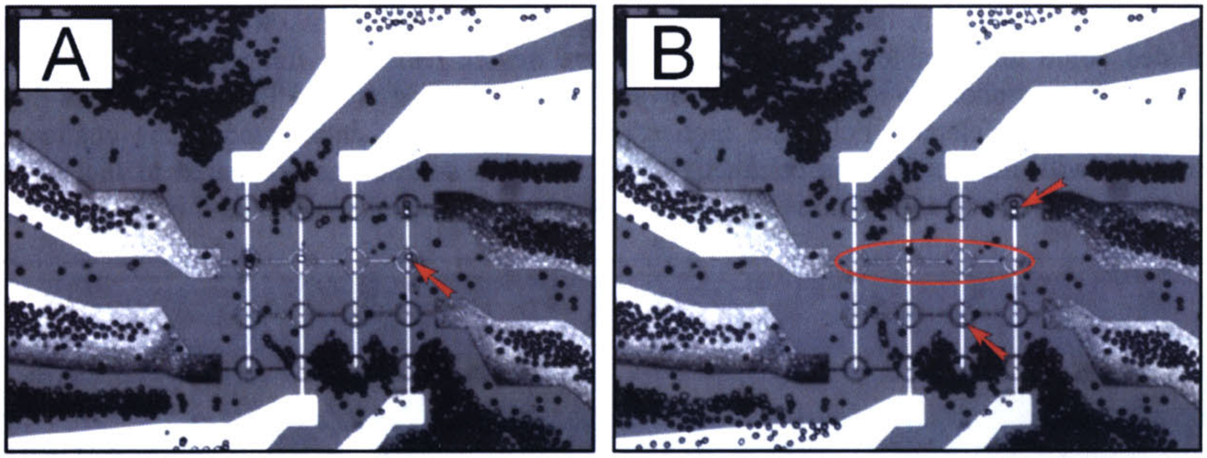


Figure 4-7: Image sequence showing a first-pass attempt to demonstrate the addressability feature using polystyrene beads on a p-DEP chip. In (A) the red arrow highlights the bead to be released. (B) indicates that rather that releasing the desired bead alone, all beads on the same row escaped with this operation. The two red arrows in (B) show that some degree of addressability may have been demonstrated as two other beads in the array remained in place.

In the second round of p-DEP chip testing I tried to assess the ability for my devices to demonstrate row/column addressing through the selective release of individual trapped beads. In this examination I again injected a plug of 20 μm diameter microspheres into the chamber, turned off all fluid flow to permit bead settling, and then activated all of the control electrodes. After witnessing the same sort of site specific trapping seen in the preceding "turn-on" evaluation I selected a specific trapped bead in the array and attempted release by grounding the associated row and column electrodes and initiating a hand-driven fluid flow.

The photo set shown in Figure 4-7 (A) shows three individual beads held in the second row from the top of the grid. I attempted to release the bead located furthest to the right in this row (highlighted with the red arrow). I selected this specific bead because of the three trapped in the second row it was the only one also having a neighboring cell held in its associated column.

Image (B) highlights the results of this attempt and shows that the fluid flow (progressing from the bottom of the picture to the top) did dislodge the desired bead. Unfortunately the other two beads in the row were also freed during this operation (highlighted by the blue oval displaying an empty second row). Of note is the fact that the two beads trapped elsewhere in the grid (highlighted by red arrows in image (B)) remained trapped and in place. The one at the upper rightmost corner of the grid was interestingly enough on the same column as that of the freed cell. In a videoclip made to follow this addressing operation, the desired bead was seen leaving its trap center prior to the other two in the second row.

While this evaluation was indeed preliminary and admittedly crude, it did provide the first inkling of empirical evidence to suggest the feasibility of an addressing scheme during actual device operation. Knowing that a greater difference in relative conductivities between cells and sucrose stock solutions could enhance the p-DEP force strength through modifications of the Clausius-Mossotti factor, I moved to examine device operation with 3T3 fibroblasts. The results of that switch are discussed in the following section.

4.4.4. Cell-based Testing

To initiate cell-based evaluations I first attempted to simply repeat the same tests run in the bead studies. The switch to live-cell tests proved more difficult than hoped. As is outlined in Figure 4-8 when I injected 3T3 cells into the device they tended to quickly adhere wherever they came into contact with the surface of the chip. This behavior occurred seemingly regardless of the cell density in the chamber. The swift and prevalent surface adhesion seen for most cells in the device created challenges for determining which cells were trapped using DEP forces and which were held in place by non-field-based mechanisms. It was likewise difficult to attempt any of the planned array loading procedures since cells resting on the surface of the device outside of the 4 x 4 grid held in place against the drag forces of introduced fluid flows. Despite several attempts, I never centered in on an effective balance between injection flow rates and applied voltages that could serve to capture cells from an overriding flow and hold them in place while enabling a flushing operation for the remainder of the chamber surface.

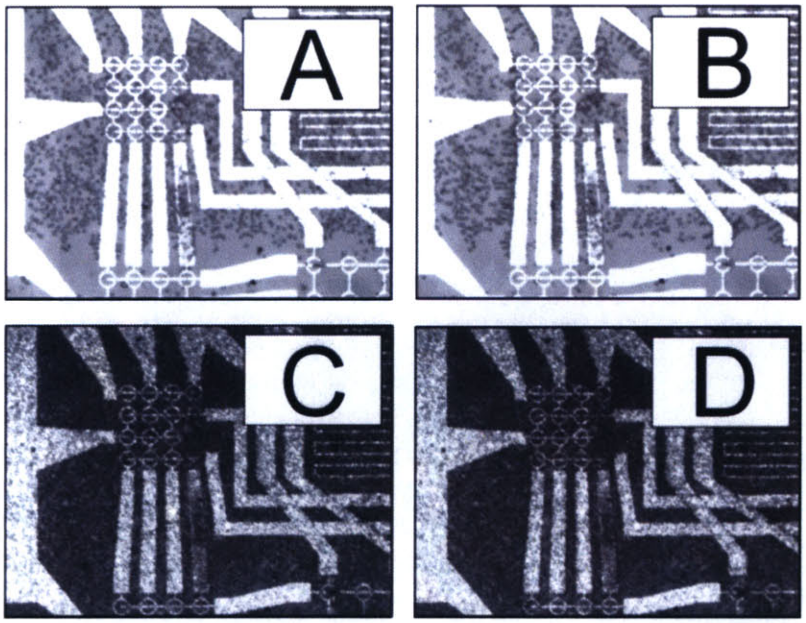


Figure 4-8: A series of images highlighting the adhesion behavior seen in tests run with 3T3 fibroblasts. (A) and (B) provide pictures before and after electrode activation for a sparse injected cell population. Images (C) and (D) again show the general lack of response to the onset of voltage drives in before and after photographs for a high surface cell density.

In Figure 4-8 I present a series of photographs advertising cell positions inside of the chamber before (images (A) and (C)) and after (images (B) and (D)) electrode activation. These before and after images are essentially identical in form. A vast majority of the cells remain in the same locations despite being subjected to field-induced ponderomotive DEP forces. This situation indicates that the cell surface binding forces overwhelm the effects of the multipolar electroquasistatic forces. While some cell movement was witnessed upon application of the driving voltages, none of the typical n-DEP (cells clumping between the electrodes where field strengths are lowest) or p-DEP(cells amassed around electrode perimeters where fields are highest) cell grouping behaviors were seen. I ran a set of similar tests later with an added step to include the injection of bovine serum albumin fraction V (BSA) (Roche Diagnostics, Indianapolis, IN) as a surface blocking agent in hopes of reducing the observed binding and saw no appreciable difference in the cell/substrate interactions. Such results encourage consideration of studies using non adherent cell lines (HL60 leukemia cells may be an adequate substitute) and searches for better surface blocking agents. Modifying the sucrose solution such that it is serum-free also presents another avenue for minimizing adhesion.

Despite the noted complexities associated with cell-based operations, I ran one additional follow-up study to assess the ability to simultaneously place two uniquely-dyed 3T3 cell populations on a device surface. Admittedly this examination was a necessary but cursory step along the path toward full-device characterization. Figure 4-9 provides a sample composite image generated by overlaying the separate fluorescent responses seen for orange and green Celltracker (Molecular Probes, Eugene, OR) dyes outlining the feasibility of a two-color imaging process. For future demonstrative purposes I could conceivably perform a sorting operation to remove all trapped cells of a particular dye-type from the trap array.

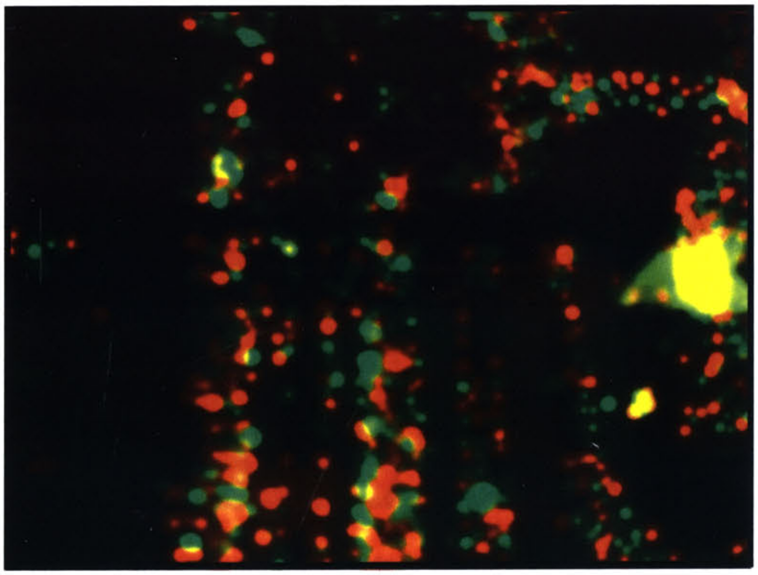


Figure 4-9: Demonstration of the imaging platform for use in conducting addressability studies indicating a successful dye of two separate cell populations.

4.4.5. An Unanticipated Challenge

As mentioned in Chapter 3, I hesitated to implement a fabrication process reliant upon aluminum metal layers. Initial hesitations were largely based upon concerns for potential negative interactions with cell health. As an unanticipated adjunct to this initial qualm I unfortunately discovered that with extended use my aluminum electrodes demonstrated pronounced levels of deterioration. Figure 4-10 highlights this response by examining the drive electrodes on a chip subjected to three days of experimental evaluations. In both the wide-field and close-up perspectives, the corrosion response is seen for the exposed M2 layer. Such behavior, I later found [60], is possibly the result of aluminum break-down through exposure to DI water-based solutions. While this effect may seem counterintuitive at first, when one considers that deionized water is a sink for ions and aluminum is a viable ion source, it is understandable that DI water could serve as an aluminum solvent.

Over time, the M2 electrode features on the test chips were so badly damaged that they failed to connect to the external control circuitry and thus rendered the devices ineffective for cell trapping. Subsequent aluminum-based test chips seemed to display a reduced corrosion response after incorporating an N_2 injection routine for blow-drying the insides surfaces of the flow chamber between uses.

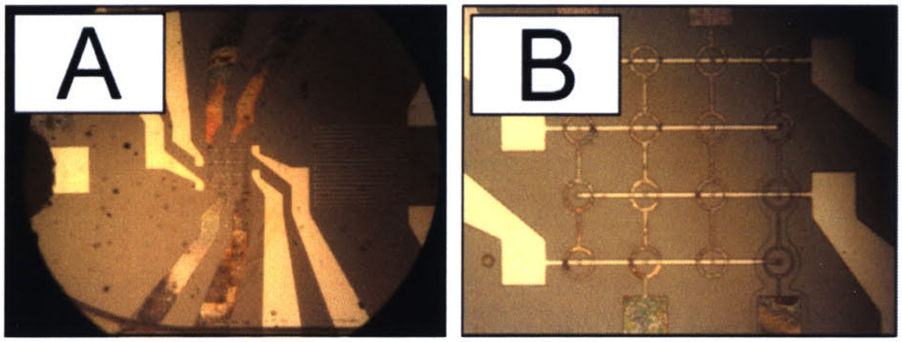


Figure 4-10: Photographs of the unanticipated corrosion behavior seen on the M2 level after several days of chip testing. (A) provides an overall perspective while (B) is an enlarged image of the array shown at the center of (A).

While it is conceivable that these observed electrode deteriorations resulted from voltage-induced electrochemical reactions, the same sort of behavior was seen on a series of alternative test chips subjected to DI water exposure without any application of external drive voltages. A follow-up experiment, conducted by one of our lab's UROPs, where unmounted chips were left submerged in DI water for upwards of three day time spans demonstrated a less dramatic corrosion response. The complete underlying cause for the disintegration of the M2 layer is not known at present. I do however suspect that deionized water exposure is the primary culprit. Further testing with my chips will likely help to sort out this detail.

Chapter 5: Conclusions and Future Work

Introduction

In this final chapter I tie together several loose ends by reviewing the key accomplishments of my work and then discussing details of what remains to be done in follow-up studies. I provide both an explanation of my design's shortcomings and a detailed plan for future experimental assays aimed at helping later stages of the project to come full circle. I then take some license and project well beyond the current state of my research progress to mention ideations for future improved cytometer designs extracting from lessons learned while developing this first proof-of-concept architecture.

5.1. A Survey of Project Accomplishments

Over the course of the past 18-20 months this cytometer project evolved from a set of preliminary ideations developed as an offshoot of prior work in the field [21, 25] to a state where actual physical device implementations were rendered and subjected to a round of simple evaluative tests. My work demonstrates, for the first time, a plausible approach to designing scalable, site-addressable dielectrophoretic traps where the electrical interconnect requirements grow proportionally with the $\sqrt{n}$, where n is the number of trap sites in a given array. I further present an outline for the feasibility of live-cell sorting using optical techniques. My current 4 x 4 cytometer chips create the first-known viable cell sorting platform for conducting genetic screens based upon complex phenotypes. Sorting individual cells based upon characteristics as elaborate as morphological expressions and dynamic intracellular processes is now conceivably approachable through future generations of this technology. The chosen geometries for each of the three n-DEP and p-DEP trap designs fabricated for this project presented architectures unlike any of the previously known, layouts discussed in related literature [61-63]. These new planar-based geometries may further encourage others to explore alternative approaches for trap designs. Increasing the suite of known functional trap layouts would likely prove beneficial for future studies in the DEP field. The incorporation of numerical-based temperature simulations in my studies, in addition to the evaluation of transmembrane voltages provided a method for assessing the biological impact of device operation from the onset. This situation promoted quicker iterations in the design cycle than could be realized through a fab and test routine alone. Despite avoiding the complexities required to implement on-chip transistor elements for the control of individual traps, my eventual two-level metal process flow was involved enough to help expand the fabrication capabilities available in the MIT Microsystems Technology Laboratory. By validating the use of Transene's Silox Vapox III product I created a crude but viable mechanism for the in-house patterning of deposited silicon dioxide layers positioned between underlying and overlying patterned aluminum layers. Overall this project ran a very involved course to progress through design, simulation, fabrication and test procedures to validate the initial goal of introducing a new tool to the biological research community.

5.2. Design Limitations

Despite hitting many of the benchmarks of the project's mission, my efforts certainly had their shortcomings and there is still ample room for design improvement in subsequent implementations. The most outstanding feature falling short of an encompassing design progression came in the form of needed simulation tools. For the n-DEP well-based trap geometries I was ill-equipped for predicting the behavior of cells or beads positioned inside of the wells subject to a host of complex fluid phenomena. This scenario presents particularly challenging problems as cells located within the pit structures are capable of translation, rotation, and deformation responses. Coupled to the localized pit environment is the potential for the overriding fluid flow to induce vortices, low-pressure Bernoulli lift forces, and cell shearing. The presence of the cell alone modifies the volume occupied by the fluid inside of the well and likewise there is an associated impact on flow dynamics. As an added complication, the quasistatic lid formed by the electrodes flanking the upper rims of each well presents a dielectrophoretic force field which may not be subject to analysis through superposition principles. Fully simulating this environment alone is likely a task complex enough to demand a majority of the work for a doctoral dissertation. Through discussions with collaborators in Dr. Jacob White's research group considerations are being made by others for the development of such an accompanying investigation.

Another key trouble spot resulted from the need to pattern the PECVD oxide layer in my devices. The Transene wet etch process was inherently isotrotic in nature. This characteristic meant that the dimensions of all exposed aluminum layers were often compromised. Linewidths tended to be reduced, and in cases of smaller geometries, full wafer development resulted in dramatic overetching to the point where some connections were corroded beyond use. Endpoint detection was particularly challenging. My designs lacked an etch stop layer which forced me to periodically stop etch cycles and inspect the response using microscopy and profilometry tools.

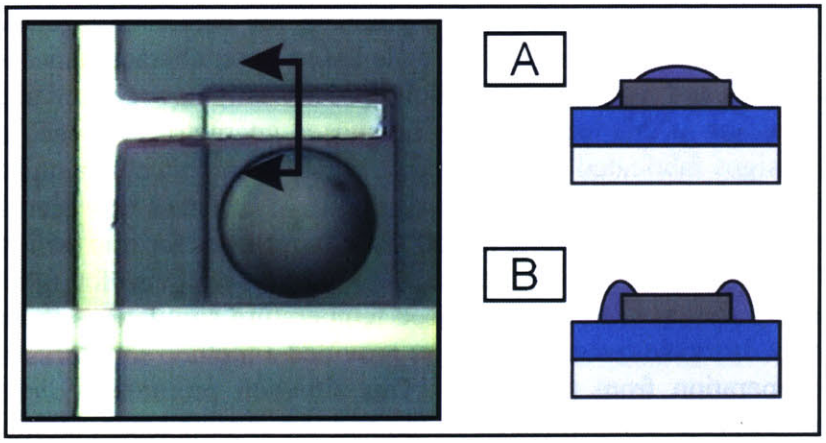


Figure 5-1: Fully fabbed n-DEP trap and a pair of accompanying cartoons offering two possible material cross-sections to explain the band-like feature bordering the edges of the M1 level at the "end-point" of the Silox Vapox III process step. Option (A) suggests that only the edges have been etched and that a residual layer of PECVD oxide covers the bulk of the metal layer. (B) speculates that the edges of the metal are locations where the deposited oxide is attacked less aggressively. Option (B) is a highly preferable cross section as it is less likely to truncate e-fields in the surrounding media during chip operation.

Despite monitoring step height changes and looking for slight necking and corrosion on the M1 layer it was often challenging to interpret measured and visual cues. Figure 5-1 highlights this sort of complexity. In the image provided a photograph displays an individual finalized n-DEP trap. (A) and (B) suggest two possible cross-sections to explaining the observed line-like features along the edges of the exposed M1 layer. In (A) only the edges of the underlying aluminum layer have been exposed and residual amounts of oxide are present over the top surface of the electrode and along its edges. In (B) there is a bias for remnant oxide to cling to the outer perimeter of the metal. It was hoped that the edge-feature observed during the Silox Vapox III etch could be explained by the supposition in case (B). This explanation of the observed effect would have meant that a majority of the electrode would have been exposed, rendering it capable of forming the electric fields necessary for DEP trapping.

It is possible however to imagine that the cross-section in (A) is a more adequate descriptor. Thinner conformal coatings of the PECVD oxide layer around the sharp edges of the underlying M1 layer could have meant that there was a preferential edge etch bias and that the apparent necking behavior of the metal was simply an artifact of localized oxide consumption. Unfortunately my testing efforts have not allowed time to evaluate the behavior of fabbed n-DEP devices. If during those upcoming tests I find that my n-DEP traps struggle to capture microparticles it may be the result of an overlying oxide layer on the M1 electrode serving as a field attenuation source. In that case, subsequent SEM images of the features may prove useful. Overall exposing the M1 layer without imposing excessive damage was a challenging prospect. Future process flows should seek to avoid this complication.

Despite the particular challenges of the Transene step, all etch processes involved in my fabrication sequence failed to benefit from end-point detection mechanisms. This condition was true for aluminum etches in the Rainbow, thermal oxide etches in the AME 5000, and silicon etches in the STS. This dilemma, which mandates more of a hands-on approach to etch procedures slows fabrication cycles, but is likely a circumstance that will remain unchanged for future designs as upgrading the necessary equipment in MTL for closed-loop control is prohibitively expensive [64].

5.3. Future Testing and Design Validation Work

As I advertised in Chapter 4, the test routines run on my devices prior to the thesis submission deadline were lacking in terms of what is needed for full-cycle characterization and design validation. Here I offer an outline of a strategic series of tests necessary for addressing this deficit.

Figure 5-2 provides an updated and enlarged version of the chip operation cycles originally proposed in Figure 1-6. This revised sequence of procedures presents the specific trap geometries developed through the simulations of Chapter 2. Additional details related to the injected fluid types and process layers used for fabrication are included.

Fully characterizing the behavior of my designs will require several unique experiments. Those proposed in this second-round testing phase are not necessarily suggested as sequential investigations but should be considered instead as a comprehensive list of all strategies needed for completely assessing the functionality and trapping capabilities of the n-DEP and p-DEP-based designs.

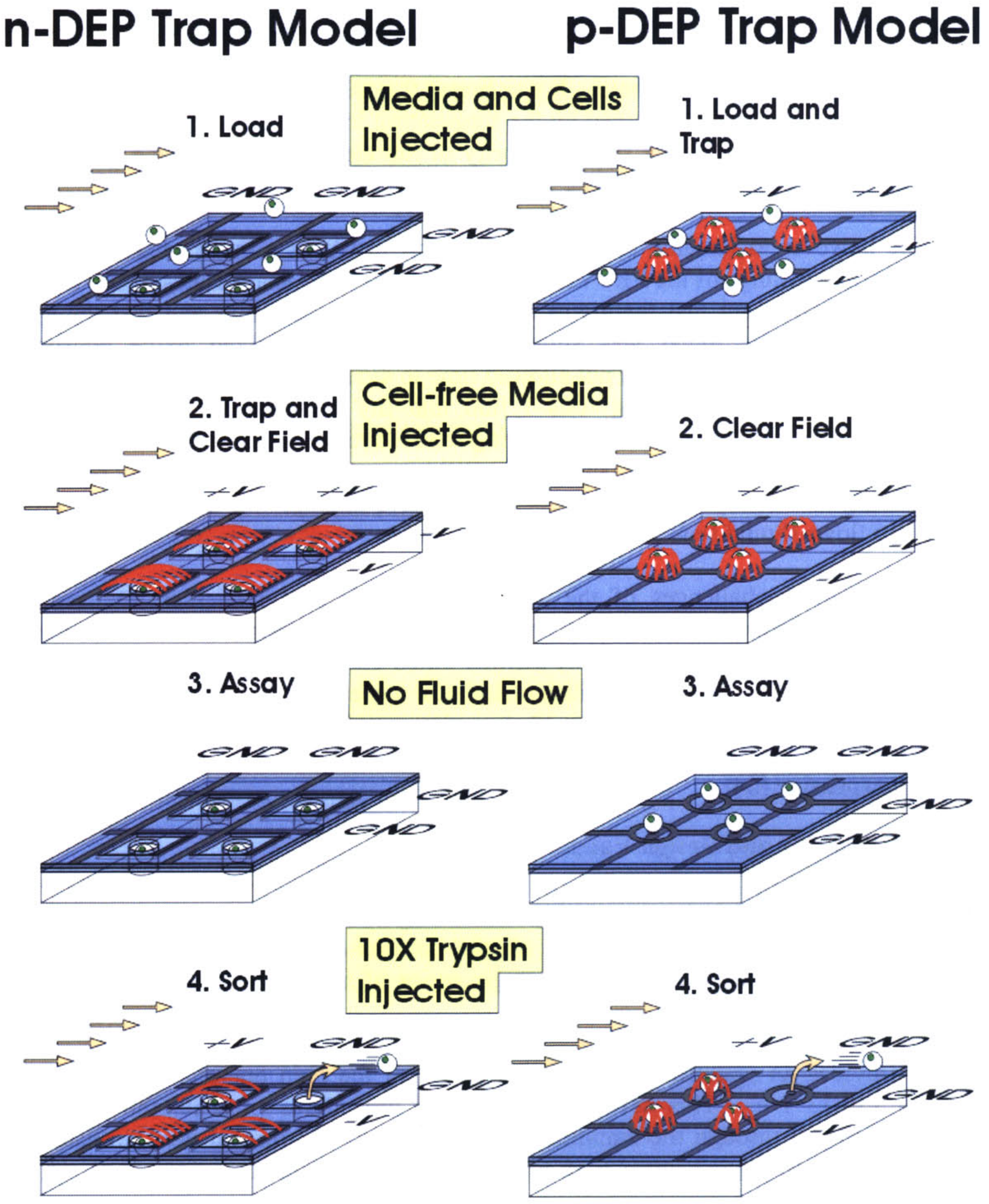

n-DEP Trap Model
p-DEP Trap Model
1. Load
Media and Cells Injected
1. Load and Trap
GND
GND
GND
GND
+V
+V
-V
-V
2. Trap and Clear Field
Cell-free Media Injected
2. Clear Field
+V
+V
-V
-V
+V
+V
-V
-V
3. Assay
No Fluid Flow
3. Assay
GND
GND
GND
GND
GND
GND
GND
GND
4. Sort
10X Trypsin Injected
4. Sort
+V
GND
GND
-V
+V
GND
GND
-V

Figure 5-2: Outline of the four step operational sequence involved with demonstrating row/column site addressability. Both the n-DEP and p-DEP approaches are hightlighted. In contrast to all previous schematics, the silicon substrate is not colored here as an attempt to offer added visual clarity.

Assessing the selectivity offered by variations in pit dimensions associated with the n-DEP structures will be an initial step in understanding n-DEP trap behavior. The passive row chip, with no control electrodes, incorporating pit features ranging from 10 to 50 microns (in 5 micron intervals) in diameter, is designed for this purpose. A PBS solution heavily saturated with polystyrene beads, 20 microns in diameter (comparable to 3T3 cell sizes) will be fed into this chip at a moderate flow rate (tens of microliters/minute). After stalling the flow rate, I will survey the traps using a microscope and take images to asses which pit diameters are appropriately sized for single cell capture. The pits must be large enough to permit the beads to fall into the chambers yet small enough to avoid having more than one in a single pit. I will repeat this experiment with 3T3s and extend the permitted residence time in the well structures to survey the ability for cells to attach to the inner walls of the pits and then release after being subjected to a 10X Trypsin injection at a moderate flow rate. Bead and/or cell clumping would complicate these assessments. Triton will be used in the bead solution to discourage this behavior and surface blocking agents will be incorporated into the cell-based assays.

I will use the "row" chips incorporating electrode components to better understand n-DEP trap holding characteristics for a host of different fluid flow rates. In these assays I will inject a plug of beads into the flow chamber to initiate a loading sequence. After watching the beads settle on the chip surface and fall into the pit features, I will activate all of the control electrodes using a 1V peak-to-peak source driven at 10 MHz. I will then begin assessing the trap holding characteristics by initiating flow of a bead-free stock solution at a rate of .5 μL/min. This flow rate will be ramped until release is witnessed. Empirically measuring the flow rate needed for release at the specified voltage of 1 V will provide a means for comparing simulation results to actual device function for the n-DEP geometries. This study will serve as an active feedback loop for future design implementations. Again this experiment will need to be repeated with fibroblasts in DMEM-based stock solutions.

Testing the p-DEP trap holding characteristics may prove simpler as the selectivity for single-cell capture will be assessed in conjunction with the trap holding strength. Using the requisite DI-based stock solution I will port polystyrene beads into a row chip design that incorporates the three distinct fabricated p-DEP ring-dot trap architectures. I will initiate loading by setting the electrodes to a 1V peak-to-peak potential difference and starting a moderate injection flow rate. I will slowly decrease the injection flow rate while monitoring the trapping characteristics of each of the three designs on the chip. I will then compare the experimental values for the hold/release flow rates to those found during simulation for design validation purposes. To provide insight on the trapping behavior that might be witnessed for a real assay, I will repeat the sequence will live mammalian cells. To ensure cell attachment is feasible at trap sites, the study will be run long enough to allow cell/substrate binding. Switching the media to 10X Trypsin deactivating the electrodes, and increasing the flow rate to a moderate level should demonstrate the ability to detach cells from the actual device structure.

The final test of p-DEP holding characteristics will require row chips with both intersection and ring-dot geometries. I will load these chips in the same fashion as was used in the preceding set of p-DEP tests and image them to compare the holding behaviors of the two different trap configurations. I expect that the intersection geometries will hold beads and cells less well than the ring-dot structures. I further anticipate that the intersection geometries will display poorer selectivity for single cell capture. The intersection traps are not designed to function very adequately, they would only be used to compare the two design types and to serve as a check for my front-end simulation work.

Testing the designed row/column addressability scheme is a more complex endeavor. The single-array-based chips are well suited for this purpose. As discussed earlier in Chapter 3 six different designs fall under this chip heading. Three implement n-DEP layouts of varying pit diameters and three incorporate the p-DEP designs with variations in the "A" and "B" parameters detailed in Figure 2-11. Testing and witnessing the addressability of at least one n-DEP design or one p-DEP design would serve to validate the proposed implementation scheme.

To test the n-DEP arrays, I will use the same loading sequence outlined earlier for the n-DEP row chip tests. I will inject the stock solution at a rate below the release rate determined from the preceding n-DEP tests. A single specified trapped object in the array will then be selected and its corresponding row and column electrodes will be grounded. As I did for the tests of this sort in Chapter 4, I will monitor the array for the expected release behavior. Again, the half-strength traps along the grounded control lines will be of special interest as they are more likely to release trapped microparticles than the full-strength traps. If it proves difficult to hold objects in place with the half-strength traps I will increase the voltage applied between the control electrodes and adjust the flow rates as necessary. Subsequent assays will involve selections of multiple objects for release within the trap grid. These studies will provide some insight regarding the ability to conduct the large-scale releases that would be needed in real genetic screens. For evaluations with cells, two distinct fluorescent tags will be used to mark separate cell populations. After combining such marked cells and subsequently injecting them into the flow chambers all of the cells of a given color will be selected for removal from the trap array. Although these studies may not take place over time courses long enough to promote cell attachment, 10X Trypsin will be used as a solution in the sorting step to squelch adherence to the inner walls of the pit structures.

I plan for similar tests of the p-DEP single-array-based chips again using both polystyrene beads and cells. In contrast to the n-DEP arrays which I will load with grounded electrodes, the p-DEP designs will require activated control lines set to the trapping drive voltages found in preceding studies. These active electrodes will center beads and cells over individual trap sites by extracting them from the passing fluid flow. Again, during operation I may need to adjust the applied voltages and balancing flow rates if half and full strength traps. are to demonstrate the desired holding characteristics. The "holy grail" for these addressability studies will be the production of before and after images displaying multicolored dyed cells that have been trapped and released as shown in Figure 5-3.

Running tests with the multiple-array chips will show the extent that spacing between traps affects the ability to hold cells or beads in individual discrete sites. Loading the n-DEP traps will take the same passive form that they have in all preceding assays. To induce release responses, I will gradually ramp the flow rates with all electrodes activated. I will continually monitor the three arrays on this chip platform throughout the process. It will be interesting to learn whether or not any of the arrays release cells sooner than others. Loading the p-DEP traps will require the activation of the control electrodes paired with fluid flow rates below the empirically-found release values. With all or most of the sites loaded, I will ramp the flow rate and image all three

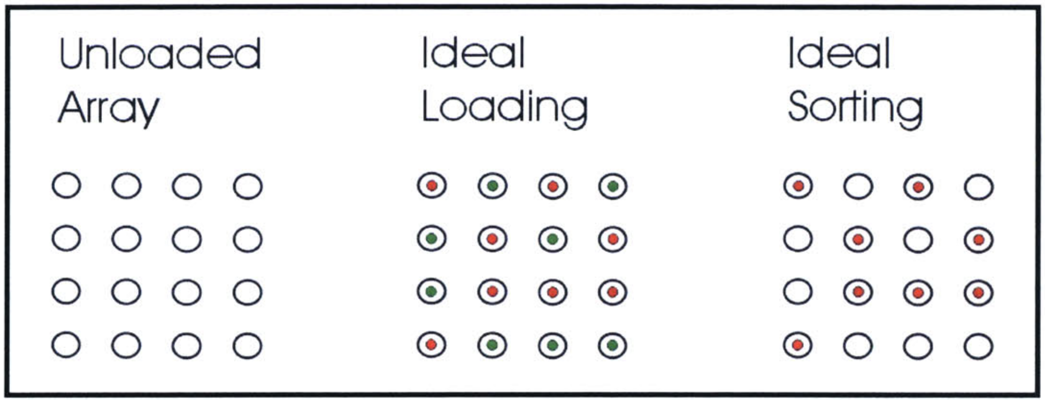


Figure 5-3: This image highlights what amounts to the gold standard for demonstrating row/column addressability with my specific 4 x 4 matrix chips. Two uniquely-dyed populations are combined and trapped in a single array and then one of the two cell types is released. Producing actual fluorescence photographs of my chips progressing through this sorting sequence will be a milestone in helping my future work come full circle.

on-chip arrays. Again it will be important to note whether or not release from any one array precedes another. These studies will offer insight regarding optimal trap densities for use in larger arrays. Ideal spacings would be both dense and provide robust trapping for flow rates on the order of tens of microliters per minute.

I will run a final set of assays using the chips that include MIT-array-based designs. With these chips, I will demonstrate in an easily visualized manner, the ability for the technology developed in this project to be scaled for the manipulation of large groups of particles. I will use the same loading and release strategies outlined for the single-array chips. Because these specific assays mainly serve demonstration purposes I will only run them with beads.

5.4. Future Design Improvements

Looking ahead to possible second-generation cytometer designs will require a serious reconsideration of the microfabrication process used for device implementation. Of primary interest will be the determination of a sequence of manufacturing steps affording a two-level metal process with the ability to pattern an intermetal dielectric layer. Ideally the actual metal chosen will possess biocompatibility characteristics supreme to those known for aluminum, will not prohibit subsequent processing in any potential STS etch processes, and will provide increased resilience to corrosion from deionized water. I have more recently learned [25] that silicon dioxide depositions with thicknesses on the order of 100 Å and less are not only possible but are thin enough to cause minimal electric field attenuation for covered electrode structures. If aluminum still amounts to the best choice for electrode implementations in future designs from the standpoint of process compatibility, depositing a thin overlaying silicon dioxide layer could offer a route for avoiding direct cell/electrode contact and also insulate the material from water-based corrosion. Of chief concern will be the incorporation of an etch stop layer for the chosen dielectric material. A demonstration of high degrees of etch selectivity against the M1 material will also be of outstanding importance. Perhaps a dry plasma-based dielectric etch could be used to remove a brunt of the material from regions covering electrodes and the final drive to completion could incorporate a short wet etch procedure with an etchant posing minor threats the electrode material type. Ruminations have been made to consider opening one of the STS silicon etching machines to gold-contaminated processes. If such a decision was made by MTL administrators an entire new suite of opportunities would emerge for process development. If I can effectively address these metal and dielectric material concerns I will make significant improvements over the current design.

At present the pit formation routine, dependent upon an STS etch, comes very late in the overall process sequence. This lineup greatly constrains the options available for preceding process steps. There might be a way that I could organize a protocol permitting the generation of these features before patterning electrode geometries. Such a plan would pave the way for incorporating potentially less difficult fabrication strategies thereafter. If alternative substrate materials were considered it might also be conceivable to produce the pit geometries using some sort of hot embossing technique [65]. Alternative substrate materials would still face the need to demonstrate the high thermal conductivities prescribed by the thermal simulations discussed in Chapter 2.

While the planned testing routine for future evaluations will bear it out, I am very much concerned that the pit-structures incorporated in all n-DEP designs will create severe challenges for extricating trapped cells. After adhering to the inside surfaces of the wells it seems very plausible that cells thus trapped might not present large enough surface areas to injected Trypsin treatments for effective disruption of surface binding deep within the well. In effect, these pit structures may amount to swift and shallow graves for individual cells. Future trap configurations might need to incorporate a backside pressure source for "popping" cells out of the wells. Admittedly such a requirement would add great complexity to the fabrication cycle as silicon on insulator (SOI) wafers or wafer bonding may be prove essential. This sort of demand for n-DEP designs would also likely pose problems for fabricating p-DEP layouts on the same wafer. This result could mean that separate mask sets would be needed for the two distinct trapping techniques. One project in effect becomes two at that point.

Additionally I am concerned that the small size of the n-DEP pit geometries may prevent fluid filling during operation as a result of surface tension effects. This hypothesized situation would mean that microparticles suspended in injected fluid flows would never have the opportunity to settle into trap sites during loading operations. Without effective loading the devices would prove useless for conducting screens. If such surface tension behavior proved characteristic of these architectures it is conceivable that injections of surfactants demonstrating enhanced wetting capabilities might present a work around. The worry then becomes whether or not such solutions would actually be fully flushed from the wells upon follow-up injections of different fluid types. If residual amounts of a surfactant remained resident within the wells then the microenvironment of the cell could be largely different from expectation. Such a scenario might promote negative effects on cell health or adversely modify the inducible localized DEP force fields.

From a mask design perspective I failed to consider the possibility for accidentally matching an alignment mark from the top of a chip on one mask level with one on the bottom of a chip from another level. After making this sort of unexpected misalignment error on one of the wafers used in the early stages of my processing work, I adopted added safety measures to prevent mistakes in future photopatterning procedures. These added checks were both time consuming and could have been avoided through the use of a modified mask design approach. Figure 5-4 delineates a simple suggestion for next generation alignment marks. In this figure alignment marks located at the top of a given chip layout would incorporate the letter "T" while those found at the bottom of a chip design would display the letter "B". For any possible future SU-8 mask levels I would also shoot for improvements by sizing the outer edges of dam features such that they would not encroach on the inner chamber edges at any point. In the designs used in my current implementation narrow bands of the SU-8 dams bounding regions surrounding through-hole locations often proved excessively fragile and ripped during drilling operations. Such a result posed challenges for effectively sealing the fluid flow chambers.

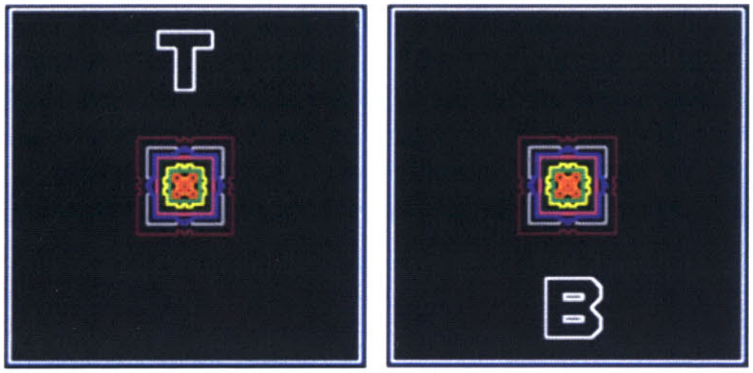


Figure 5-4: Proposed modifications for alignment marks in future mask designs. Because the marks at the top and bottom of each chip on all mask layers used in my thesis were identical, it was possible to accidentally offset photopatterning procedures by overlaying the top alignment mark of one layer with the bottom mark of another or visa versa. Distinguishing the two registers will help avoid this issue in subsequent designs.

The many challenges associated with SU-8 dam fabrication motivated experimentation with PDMS-based replacements. As mentioned in Chapter 3, I formed alternative dam structures by pouring thin layers of PDMS, at a 10:1 base to hardener ratio, into cell culture dishes and cutting them into the required shapes after two hour 65 °C oven cures. This approach, which depended upon hand-manipulations of a razor blade, allowed for a less complex implementation, yet produced a rather crude solution. Future designs should explore options for purchasing PDMS films of uniform thicknesses and implementing "cookie-cutter" strategies for shaping chamber cavities in a more professional manner. Figure 5-5 illustrates this plausible design evolution. The technique proposed for these next-generation dam layers would require a precision milled metal stamp that could be pressed into the PDMS film and used to pluck out the central cavity region. This sort of dam-shaping tool could be made using a small cutting head and a computer numerical control (CNC) driven milling machine.

The planned testing phases of this project could likewise stand some improvement. Rather than struggling with the challenges of creating p-DEP stock solutions demonstrating low electrical conductivities, metal-coated polystyrene beads could be used to boost the bead conductivity in comparison to the surrounding fluid. At present all known vendors retailing such specialized beads have been unwilling to sell their products to academic research laboratories due to worries pertaining to industrial secrets regarding their use in IC chip packaging technologies or they have been priced well-beyond (ie. minimum purchases on the order of $20,000) what could be considered reasonable academic research investments. I have plans to attempt to manufacture such items myself, in-house, either through the use of e-beam depositions and/or by following published protocols involving chemical surface activation and seeding [66, 67].

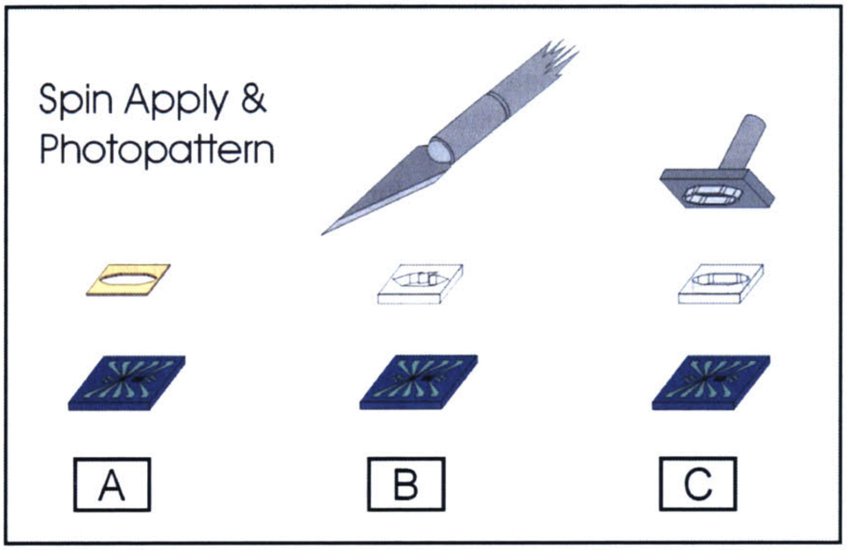


Figure 5-5: Illustration of the fluidic dam evolution. (A) indicates the original process where an SU-8 layer was applied using a host of microfabrication techniques. Damage to significant numbers of the SU-8 dams and chronic separation from the substrate led to a revised PDMS-based approach (B). This technique involved pouring and curing a thin layer of PDMS and then cutting out a dam feature using a razor blade. The inherent challenges associated with making straight lines or uniform dam features suggests a move to a "cookie cutter" stamping process as shown in (C).

The struggles I faced related to 3T3 adhesion to chip surfaces may well be reduced through the application of better surface blocking agents such as Pluronics F127 (BASF, Ludwigshafen, Germany), or through a switch to experimentation using a non-adherent HL60 human leukemia cell line. Such a switch would help demonstrate the functionality of the chip, but I would fail to address the original goal of the project for registering adherent cell lines requiring surface interactions.

To fully characterize my devices, future studies will mandate a robust impedance analysis of the entire electrical control system. This sort of study will provide information for understanding where voltage drops and losses occur in the path progressing from the signal generator to the individual DEP traps. Knowing such information may help to improve system performance.

New designs may well benefit from different packaging structures where fluidic ports connect from the sides of the chip rather than by way of through-holes in the underlying substrate. Such designs, while unessential, would potentially render more sleek and compact packages capable of canceling out the risks of chip fracture presented during the hand drilling sequence currently in use.

Introducing a spring-loaded mechanism for establishing electrical connections between PCB traces and chip pads would help to avoid the patience necessary for hand wire-bonding individual chips. Such structures could conceivably be more robust than the wirebonding approach and thereby reduce the risk of damaging the electrical connections while handling and testing the chip.

The literature mentions use of impedance techniques for detecting the presence of cells in DEP traps [68]. Future designs might possibly implement such methods to enhance the overall system capabilities and better automate screening routines.

Despite this broad summary of possible improvements, the work I present in this report successfully charts an initial course for a full demonstration of this novel cytometry technology. The experience I gained by progressing through planning, design, simulation, fabrication, and testing cycles has prepared me for tackling future challenges associated with my continued involvement in the project.

Appendix I: Microfabrication Process Flow

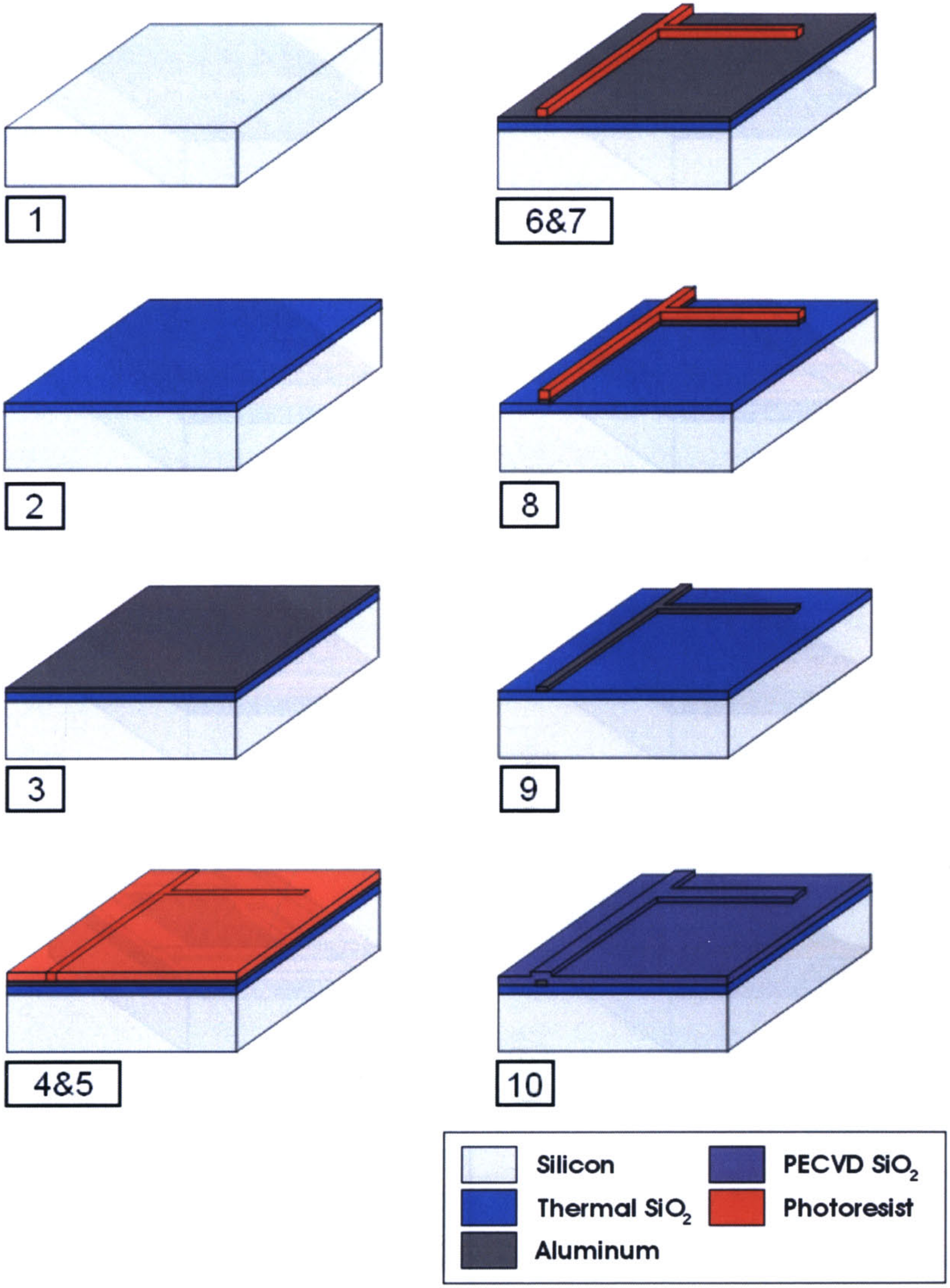
Process flow for 4X4 cell trapping array:

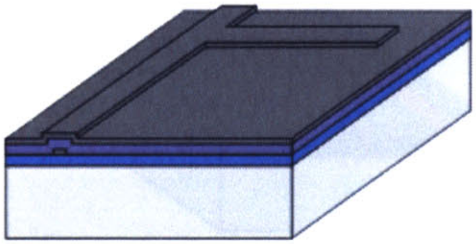
1) RCA clean 6” silicon wafers (rcaICL [ICL])
2) Grow wet thermal oxide - 1.5 microns thick (5D-FieldOx [ICL] or 5C-ThickOx [ICL])
3) Sputter on 5000Å aluminum (endura [ICL])
4) Spin on standard positive photoresist – 1 micron thick (coater6 – track1 [ICL])
5) Mask aligner/expose photoresist (EV1 – green chuck [TRL])
6) Photoresist development (coater6 – track2 [ICL])
7) Descum to remove photoresist from areas where not desired (asherTRL [TRL])
8) Plasma etch aluminum – use either Cl_2 or BCl_3 – include dump rinse step (rainbow [ICL])
9) Ash to remove remaining photoresist prior to SiO_2 deposition (asher-ICL [ICL])
10) PECVD deposition of blanket SiO_2 film -1.5 microns thick (concept1 [ICL])
11) Sputter on 5000Å aluminum (endura [ICL])
12) Spin on standard positive photoresist – 1 micron thick (coater6 – track 1 [ICL])
13) Mask aligner/expose photoresist (EV-1 – green chuck [TRL])
14) Photoresist development (coater6 – track2 [ICL])
15) Descum to remove photoresist from areas where not desired (asherTRL [TRL])
16) Plasma etch aluminum – use either Cl_2 or BCl_3 – include dump rinse step (rainbow [ICL])
17) Ash to remove remaining photoresist (asher-ICL [ICL])
18) Spin on standard positive photoresist – 1 micron thick (coater6 – track1 [ICL])
19) Mask aligner/expose photoresist (EV-1 – green chuck [TRL])
20) Photoresist development (coater6 – track2 [ICL])
21) Descum to remove photoresist from areas where not desired (asherTRL [TRL])
22) Wet etch of secondary oxide in Transene’s Silox Vapox III – timed (acid-hood [TRL])
23) Ash to remove remaining photoresist (asher-ICL [ICL])
24) Spin on standard positive photoresist – 1 micron should be enough but may elect to go thicker (coater6 – track1 [ICL])
25) Mask aligner/expose photoresist (EV-1 – green chuck [TRL])
26) Photoresist development (coater6 – track2 [ICL])
27) Descum to remove photoresist from areas where not desired (asherTRL [TRL])
28) Wet etch of primary oxide in BOE or Transene’s Silox Vapox III (acid-hood [TRL])
29) Silicon deep trench etch – 20 micron depth etch (sts2 [TRL])
30) Ash to remove remaining photoresist (asher-ICL [ICL])
31) Spin on SU-8 photoresist (SU8spinner [TRL])
32) Mask/aligner expose photoresist (EV-1 – red chuck [TRL])
33) Solvent wet station for photoresist development (SU8spinner [TRL])
34) Descum to remove photoresist from areas where not desired (asherTRL [TRL])
35) Coat wafer with OCG 825 photoresist (coater [TRL])
36) Cut wafer into individual die (diesaw [ICL])
37) Wirebond chips to packages (Alwire [ICL])

Items enclosed in [] *shown in list above indicate the locations of specific machines.*

Steps 1-30 are non-gold contaminated.
Step 31 is the first instance of gold contamination.
All bakes for the SU-8 steps will be done in SU8 specific ovens.

Appendix II: Pictorial Sequence of Full-Process Microfabrication Steps


1
6&7
2
8
3
9
4&5
10
Silicon
PECVD SiO_2
Thermal SiO_2
Photoresist
Aluminum



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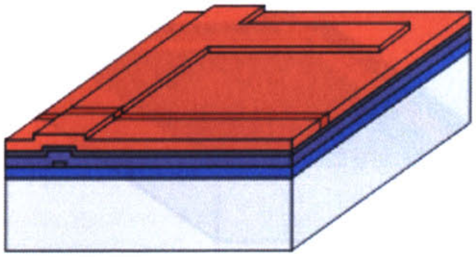
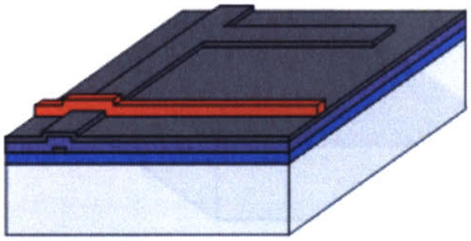
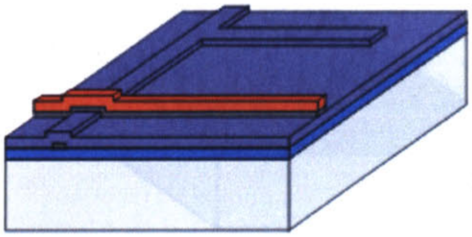


12&13



14&15



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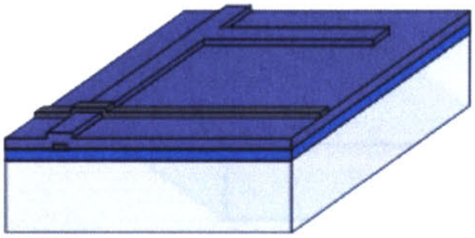

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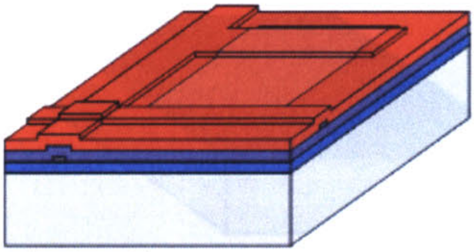
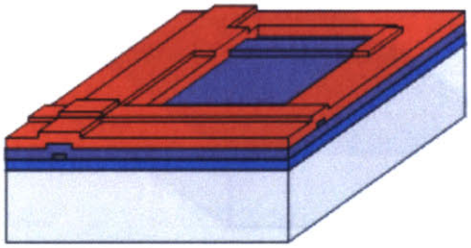


18&19



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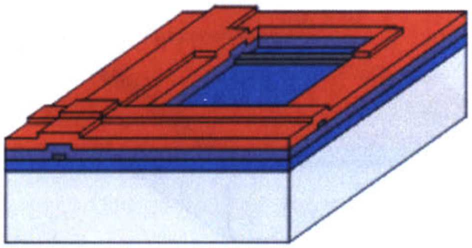
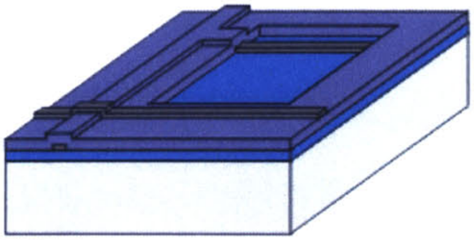
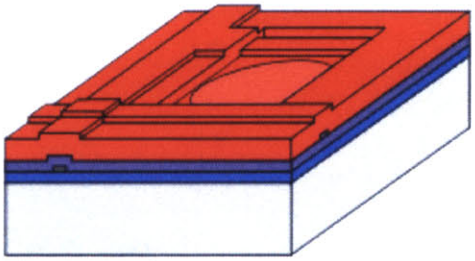


22

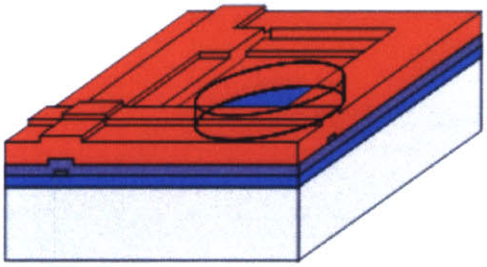
⬜	Silicon	🟪	PECVD SiO_2
🟦	Thermal SiO_2	🟥	Photoresist
⬛	Aluminum		



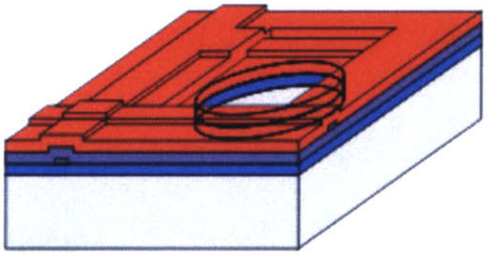
23



24&25



26&27



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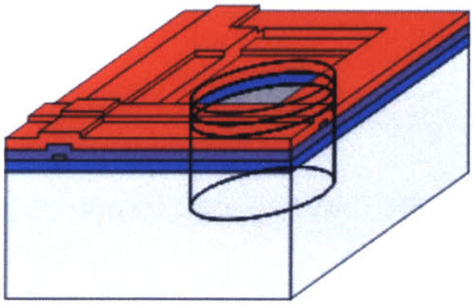

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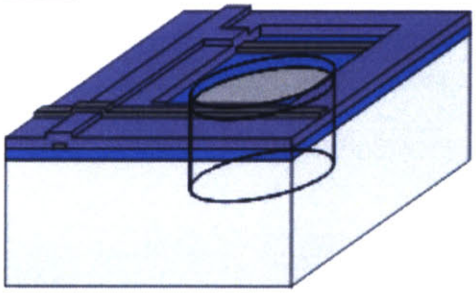

30

Remaining steps are not shown in pictorial format.

⬜ **Silicon**

🟪 **PECVD SiO_2**

🟦 **Thermal SiO_2**

🟥 **Photoresist**

⬛ **Aluminum**

Appendix III: Photopatterning Recipes

Coater6 “T1HMDS” Standard Photoresist Coating Recipe				
Stage1	Stage 2	Stage 3	Stage 4	Stage 5
130 °C	130 °C	95 °C	500 RPM	3000 RPM
30 sec	60 sec	60 sec	8 sec	30 sec

Coater6 “TAFFC” Modified Photoresist Coating Recipe				
Stage1	Stage 2	Stage 3	Stage 4	Stage 5
130 °C	130 °C	95 °C	500 RPM	700 RPM
30 sec	60 sec	60 sec	8 sec	30 sec

Coater6 “DEV6” Standard Photoresist Development Recipe				
Stage1	Stage 2	Stage 3	Stage 4	Stage 5
115 °C	130 °C	25 °C	400 RPM	3500 RPM
60 sec	60 sec	60 sec	25 sec	30 sec

Coater6 “TAFFD” Modified Photoresist Development Recipe				
Stage1	Stage 2	Stage 3	Stage 4	Stage 5
115 °C	130 °C	25 °C	400 RPM	3500 RPM
60 sec	60 sec	60 sec	42 sec	30 sec

SU-8 2100 Protocol (100 μm target thickness)					
Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
Dehydrate	Coat	Softbake	EV1 Exposure	Post-exposure bake	Develop
15 min @ 95 °C on a	Pour on excessive amounts; Spread speed = 500 RPM (15 sec), Spin speed = 1700 RPM (35 sec)	4 min @ 65 °C, ramp to 95 °C and hold at 95 °C for 20 min	Interval exposure mode; 13 seconds on, 45 sec off, repeat 4 times	1 min @ 65 °C, ramp to 95 °C and hold at 95 °C for 10 minutes	≈10 min in PM Acetate

Appendix IV: Etching Recipes

Rainbow Etch Protocol

Step No.	1	2	3	4
Pressure	13	13	10	20
Top Coil	0	375	375	0
Bottom Coil	0	120	120	0
Gap	3	3	3	6
BCl_3	40	40	40	0
Cl_2	60	60	40	0
N_2	10	10	5	0
Ar	0	0	0	120
He	10	10	10	0
Time	10	8000Å/min	20% over etch 6000 Å/min	15

AME 5000 Etch Protocol

“Oxide Pegasus” Cycled Etch for Thermal SiO_2				
Step 1	Step 2	Step 3	Step 4	Step 5
Stabilization	Descum	Stabilization	Etch	Stabilization
20 sec	20 sec	30 sec	180 sec	150 sec
200 mTorr	200 mTorr	200 mTorr	200 mTorr	200 mTorr
O_2 10 scc	O_2 10 scc	CF_4 8 scc CHF_3 6 scc	CF_4 8 scc CHF_3 6 scc	CF_4 8 scc CHF_3 6 scc
RF =0W	RF =100W	RF =0W	RF =350W	RF =0W
50.0 Gauss	50.0 Gauss	50.0 Gauss	50.0 Gauss	50.0 Gauss
			Cycle steps 4 and 5 through 10 etch cycles	

STS Etch Protocol

STS “STSHAL-A”		
General	Power	Gases
Pressure = 30.0 mTorr	APC Mode = Automatic	C_4F_8 = 80 sccm
APC Mode = Auto	Platen Generator Power = 10.0 W	SF_6 = 40 sccm
Base press. = 5.0 mTorr	Coil Generator Power = 600 W	
Press. Trip = 45.0 mTorr		

Appendix V: Deposition Recipes

Concept One PECVD Oxide (1.5 μm Target Thickness)

A1 N_2	1.500
B1 N_2	0.000
A2 SiH_4	0.300
B2 N_2O	9.500
HF Power	1.10 kW
LF Power	0.00 kW
Pressure	2.40 T
Temperature	400 °C
Time	34.60 sec
Deposition Rate	5250 Å/min
Etch Rate	6690 Å/min
Precoat	60 sec
PreA Delay	0.5 sec
PostA Delay	0.5 sec
Temp Soak	10.0 sec
X Value	0.00 sec
Y Value	3.00 sec

Endura 5000 Å Aluminum Deposition

Step No.	1	2	3	4
Step Name	Gas Stabilization	Strike	Deposition	Purge
Step End Control	By Time	By Time	By Time	By Time
Max. Step Time	10.0 sec	3.0 sec	25.0 sec	75.0 sec
Process Positive Pressure Control	None	None	None	None
Gate Pressure	Full	Full	Full	Full
Process Pressure	0.00 mTorr	0.00 mTorr	0.00 mTorr	0.00 mTorr
Wafer Gas Pressure	5000 mTorr	5000 mTorr	5000 mTorr	0 mTorr
DC Power	0 W	750 W	9000 W	0 W
DC Power Ramp Rate	0 W/sec	750 W/sec	4500 W/sec	0 W/sec
Pressure Servo Gass	AR-1: 45 scc	AR-1: 45 scc	AR-1: 45 scc	AR-1: 0 scc
Gas Names and Flows	ARH-1:14 scc	ARH-1:14 scc	ARH-1:14 scc	N/A

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