Doubled-Gated Field Emission Arrays

By

Liang-Yu Chen

B.S. Electrical Engineering and Computer Science
University of Hawaii, Manoa, 2001

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

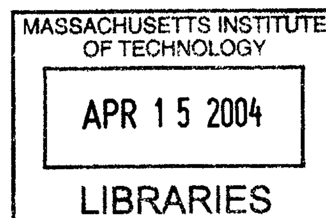
Master of Science

at the

Massachusetts Institute of Technology

February 2004

©2004 Massachusetts Institute of Technology
All rights reserved



Signature of Author___
Department of Electrical Engineering and Computer Science
December 24, 2003

Certified by________
Akintunde Ibitayo (Tayo) Akinwande
Professor of Electrical Engineering
Thesis Supervisor

Accepted by________________
Arthur C. Smith
Chairman, Department Committee on Graduate Students

BARKER

Doubled-Gated Field Emission Arrays

By

Liang-Yu Chen

Submitted to the Department of Electrical Engineering and Computer Science
On January 30, 2003 in Partial Fulfillment of the
Requirements For the Degree of Master of Science in
Electrical Engineering and Computer Science

Abstract

There is a need for massively parallel, individually addressed and focused electron sources for applications such as flat panel displays, mass storage and multi-beam electron beam lithography. This project fabricates and characterizes double-gated field emission devices with high aspect ratio. One of the gates extracts the electrons while the second gate focuses the electrons into small spots. High aspect ratio silicon field emitters were defined by reactive ion etching of silicon followed by multiple depositions of polycrystalline oxide insulators and silicon gates. The layers were defined by a combination of lithography, chemical mechanical polishing and micromachining. We obtained devices with gate and focus apertures of 0.4μm and 1.2μm diameter. The anode current has very little dependence on the focus voltage and the ratio of the focus field factor to the gate field factor β_F / β_G is 0.015. Scanning electron micrographs of the devices, numerical simulation and spot size measurements on a phosphor screen confirmed these results. An e-beam resist, PMMA, was successfully exposed using the FEA device as an electron source.

Thesis Supervisor: Akintunde Ibitayo (Tayo) Akinwande
Title: Professor of Electrical Engineering

Acknowledgements

There are many people I want to thank.

First, I would like to thank my advisor Professor Tayo Akinwande for his guidance, encouragement, and support, which enabled me to complete the project. His high scientific standards taught me how to be a good scientist.

I would like to thank Leonard Dvorson. This work is based on his Ph. D thesis. His thesis provided a good foundation for me to extend this project.

I am fortunate to work with the members in my research group —: Dr. Ching-Yin Hong, Dr. John Kymissis, Guobin Sha, Annie Wang, Jeremy Walker, and Dr. Yong-Woo Choi. They were a constant source of knowledge, advice and support. Especially, I want to thank Dr. Ching-Yin Hong and Dr. John Kymissis for all the valuable discussions and help with experimental work presented here. I also want to thank Goubin Sha for his advice and help with numerical simulation.

I would like to thank the staff of the MIT Microsystems Technology Laboratories. It would have been impossible to finish this thesis work without them. Especially, I want to thank Mr. Robert Bicchieri, Mr. Paul Tierney, Mr. Bernard Alamariu, and Mr. Joe Walsh. I appreciate your training and help with the equipment.

I would also like to thank my family for their encouragement and support.

Mostly I would like to thank my wonderful boyfriend, Huankiat Seh, for his support. He always gave me support when I struggled.

I would like to thank Dr. Cha-Mei Tang, the President of Creatv Micro Tech, Inc. for technical and moral support of the project.

Finally, I would also like to acknowledge the financial support that made this project possible. Creatv Micro Tech supported by NIH Phase II SBIR Grant 2R44RR12265-02A1 and 5R44RR12265-03 funded this work.

Table of Contents

1. **Introduction**
    1.1 Applications

2. **Background**
    2.1 Statement of the Problem
        Divergence of the Electron Beam Produced by Field Emission from Sharp Tips
        Objective and Technical Approach
    2.2 Field Emission models of Field Emission
    2.3 Thesis Organization

3. **Device Design and Fabrication**
    3.1 Device design
        Geometry of the focus electrode in IFE-FEA – device structure selection
        Device structure and operation
        Device Dimension Goal for better performance

    3.2 Formation of sharp 3μm tall Silicon Field Emitters
        Photoresist Dot and Oxide Dot definition
        Isotropic Silicon Etch
        Anisotropic Silicon Etch
        Oxidation sharpening
        Deposition, planarization and Etch back of the Gate Insulator
        Formation of the Gate Electrode
        Formation of the Focus Electrode
        Pattern contact electrodes for both gate and focus
        Annealing and Final BOE Etch
        Completed Device
    3.3 Chapter summary

4. **IV Characterization of Double-Gated FEAs**
    4.1 Measurement Setup
    4.2 Device Description
    4.3 Three-terminal Measurements
    4.4 Four-terminal Measurements
    4.5 Chapter Summary

5. **Optical Characterization of IFE-FEA**
    5.1 Measurement setup for Image Acquisition
    5.2 Collimation of the electron beam at different values of focus voltage
    5.3 Chapter Summary

6. **Photoresist Characterization of IFE-FEA**
    6.1 Measurement setup for photoresist exposure

6.2 Materials selections
6.3 Photoresist exposure result
6.4 Chapter Summary

7. Thesis Summary and Suggestions Future Work
7.1 Thesis Summary
7.2 Suggestions Future Work

Appendix A. Process Flow of the Fabrication of Silicon Double-gated Silicon FEA
Appendix B. FN coefficients of array 20x20 and array 50x50
Appendix C. Matlab code to compute the β_F and β_G
Appendix D. Field Factors for Double-Gated FEA

References

1. Introduction

1.1 Application

Several applications use arrays of electron sources that are based on the extraction of electrons by an electrostatic field. Examples of such applications include field emission displays [1.1, 1.2. 1.3. 1.4], multiple electron beam lithography [1.5, 1.6, 1.7], power switches [1.8], field emission mass storage [1.9] and RF power amplifiers [1.10, 1.11, 1.12, 1.13]. For some of these applications, there is a growing need for arrays of collimated or focused electron sources because of the requirement for smaller beam spot size to improve resolution and brightness.

The first example is the field emission display (FED). The predominant application for field emission arrays (FEAs) is the FED. FEDs promise the best of display worlds - performance and portability [1.14, 1.15, 1.16, 1.17, 1.18]. The bulky cathode ray tube (CRT) is commonly used in televisions and computer monitors. However, the strong demand of space saving, for instance, flat panel TVs, and portable applications such as laptop computers has triggered the development of thin and light screens. While the cathode of a CRT uses a point electron source that is raster scanned across the screen, an FED uses a 2D array of surface electron sources. Each pixel comprises of several thousands sub-micrometer tips from which electrons are emitted when an electrostatic field is applied. In an FED, electrons are extracted from the cathode and are accelerated through vacuum to a fluorescent anode where the energetic electrons create a multitude of hole-electron pairs, which recombine to emit light. A collimated or focused electron source would improve the resolution and brightness of FEDs.

Another example is massively parallel e-beam lithography. The massively parallel e-beam lithography is one of the best solutions for obtaining high resolution when optical lithography reaches its resolution limit. With a resolution of 70nm and below, e-beam

lithography technology is suitable for maskmaking and direct-write applications [1.19, 1.20, 1.21, 1.22, 1.23, 1.24, 1.25]. However, it has not been suitable for the IC production environment because of the low throughput of direct writing of resist. The throughput of e-beam lithography could be improved through massive parallelism of the direct write operation. The e-beam writing head for massively parallel e-beam lithography has a similar concept to the FEDs described earlier. The e-beam writing head consists of an array of microguns independently driven by an active circuit. Each microgun is a field-emission microcathode comprised of an extraction gate and an emitter, whose mutual alignment is critical in order to achieve highly focused electron beams [1.26].

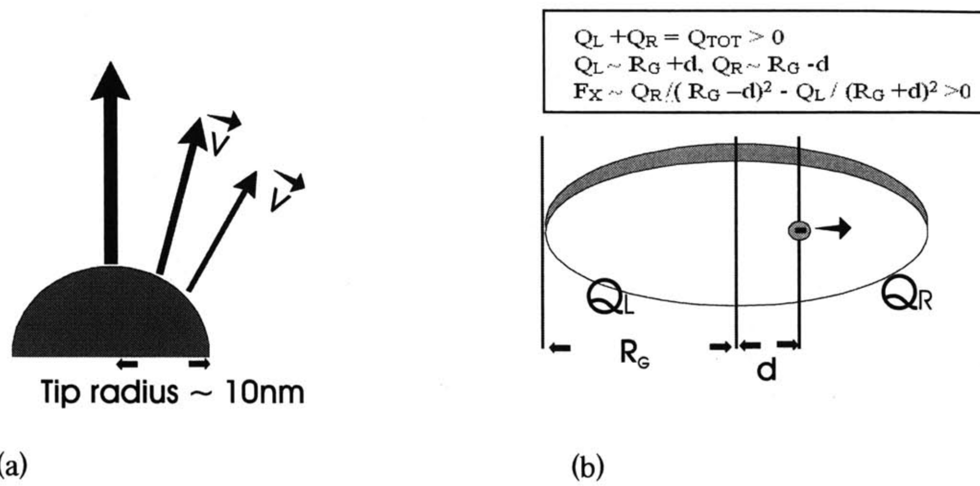
2. Background

2.1 Statement of the Problem

The type of field emitter examined in this work consists of a sharp cone centered in an annular opening of the gate conductor (Figure 2-1 [2.1]). Electrons in a room temperature material do not normally have enough energy to leave the material; an energy barrier, which blocks electron emission, exists. There are two methods to emit electrons. One approach is to give electrons sufficient energy to exceed the potential barrier, which depends on the work function. The other approach is to reduce the width of the potential barrier at the surface by applying a high enough field to allow electrons to tunnel into vacuum at room temperature. The second process is known as the Fowler-Nordheim tunneling [2.2, 2.3, 2.4]. The objective of this thesis is to fabricate a field emission device, which can produce the collimated electron source after the electrons are extracted into the vacuum.

Divergence of the Electron Beam Produced by Field Emission from Sharp Tips

There are two major reasons for the divergence of the electron beam [2.5]. Electrostatics indicates that the electric field is maximized at the apex of the tip and the field decreases away from the apex. Moreover, the field is strong enough to make the points around the tip field emit leading to an angular distribution of emitted electrons. Emitted electrons are accelerated by the local electric field, which is normal to the tip within a few tip radii of the tip. Thus, the electrons that are not emitted from the apex of the tip carry a horizontal velocity component, which introduces an angular spread into the field emission beam. In Figure 2-3 (a), the electrons can be emitted from points that are 10, 20, and 30 degree from vertical with different emission current density. Non-zero emission from points other than the apex introduces an inherent angular spread in to the field emission beam.



(a) (b)

Figure 2-3. Angular spread of the field emission beam from the origin. (a) Emission current density at different point on the tip. Non-zero emission from points other than the apex introduces an inherent angular spread into the field emission beam because electrons emitted at non-zero angles acquire horizontal velocity from the tip field. (b) An electron in the plane of the positively charged gate opening experiences a horizontal force directed away from the center, which further amplifies its horizontal velocity [2.5].

The second reason is that after electrons move more than a few tip radii away from the emitter, the gate electrode further amplifies electrons' horizontal velocity. In Figure 2-3 (b), Q_{TOT} is the charge on the rim of the gate. It is positive because the gate is biased above the cathode. Q_L is the charge to the left, which attracts the electron toward the axis and Q_R is the charge to the right, which pulls it away from the axis. While Q_L is greater than Q_R, the difference between the two is linear in the distance between the electron and the center of the opening, designated d in the figure. However, the forces exerted on the electron vary as the inverse square of electron's distance from the center. Thus, the net horizontal force on the electron is directed away from the z-axis.

Objective and Technical Approach

From above, it is obvious that we cannot prevent the beam spreading but we can attempt to re collimate the beam. The objective of this thesis is to fabricate a field emission device, which can produce a collimated electron source. By having a collimated electron source, we can improve the resolution of field emission displays and e-beam lithography. Next, we are going to propose an approach to attain this goal.

For most FEA applications, larger cathode-anode spacing is always desired. For instance, for a higher efficiency and higher brightness field emission display (FED), we want to use higher anode voltage (~keV), which then requires a large cathode-anode spacing (1-2mm) to avoid dielectric breakdown of the spacers between the cathode and anode plates. However, electrons emitted from sharp points do not all travel directly to the anode but have a significant lateral divergence and furthermore in the opening of a positively charged gate electrode, electrons experience an outward horizontal force. Thus, larger cathode-anode separation leads to increased pixel-to-pixel cross talk, which reduces the display resolution. If the electrons' horizontal velocity can be reduced or eliminated, then the cathode-anode distance can be increased without incurring pixel-to-pixel crosstalk and the resultant loss of resolution. In addition, increased cathode-anode separation would allow FEDs operate at higher voltages. In other words, collimation of the field emission beam would allow FEDs to employ high voltage phosphors and achieve higher luminous efficiency, brightness, and longer screen lifetime without sacrificing resolution.

To achieve our goal, we can add the second gate stacked on top of the first gate, called focus gate, as shown in Figure 2-4. The structure shown in Figure 2-4 has been shown to be the most effective in beam collimation [2.6]. To make the focus electrode accumulate negative charge, one simply biases it sufficiently below the gate voltage. However, strictly speaking, it does not focus the electron beam into a single point. Instead, when the focus bias is lowered, the electron beam is collimated and a dim, large spot is reduced to a much brighter and smaller spot.

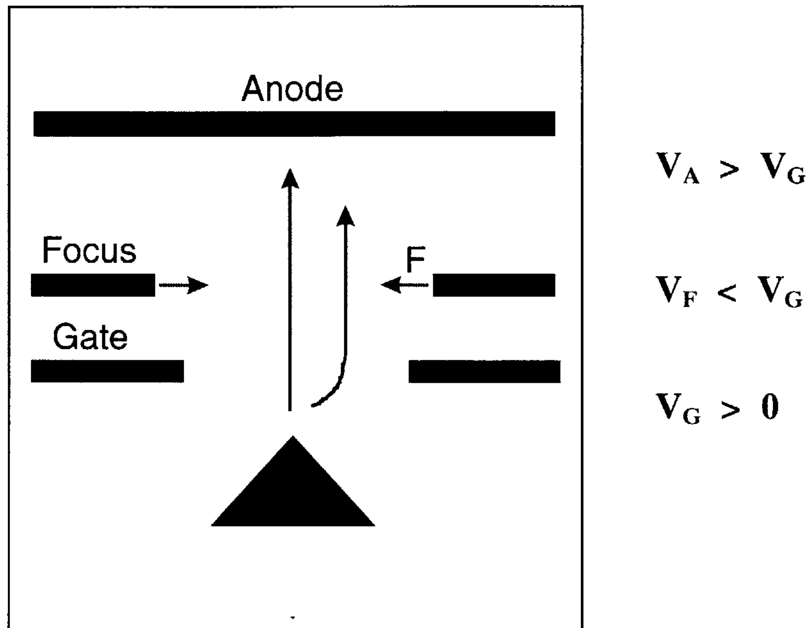


Figure 2-4. Negative charge on the rim of the focus electrode exerts a horizontal force, F. of the electron that is directed toward the z-axis. This has the effect of collimating the electron beam.

2.2 Field Emission Models

A critical component that will advance FED technology is the development of models to predict FEA behavior. Modeling of FEAs is extremely useful because (1) it identifies the parameters that determine FEA performance and thus serves as a valuable design tool; (2) given device parameters, modeling can predict device performance and operating conditions and expose potential failure modes; and (3) modeling provides a physical insight into device operation and thus helps to interpret the data.

Field Emission Phenomena

R. Fowler and L. Nordheim published the seminal paper in 1928 about the theory of field emission in metal [2.2, 2.4, 2.7]. In order to eject the electrons which are confined by a potential barrier from a metal surface into the vacuum, either the energy of the electrons could be increased to overcome the potential barrier as in photoemission and thermionic emission, or the width of the potential barrier at the surface reduced by applying an electric field so that electrons can tunnel through the barrier as in field emission. These two methods of ejecting electron from inside a metal to vacuum are depicted in Figure 2-5 [2.1]. Here, the focus is on electron field emission.

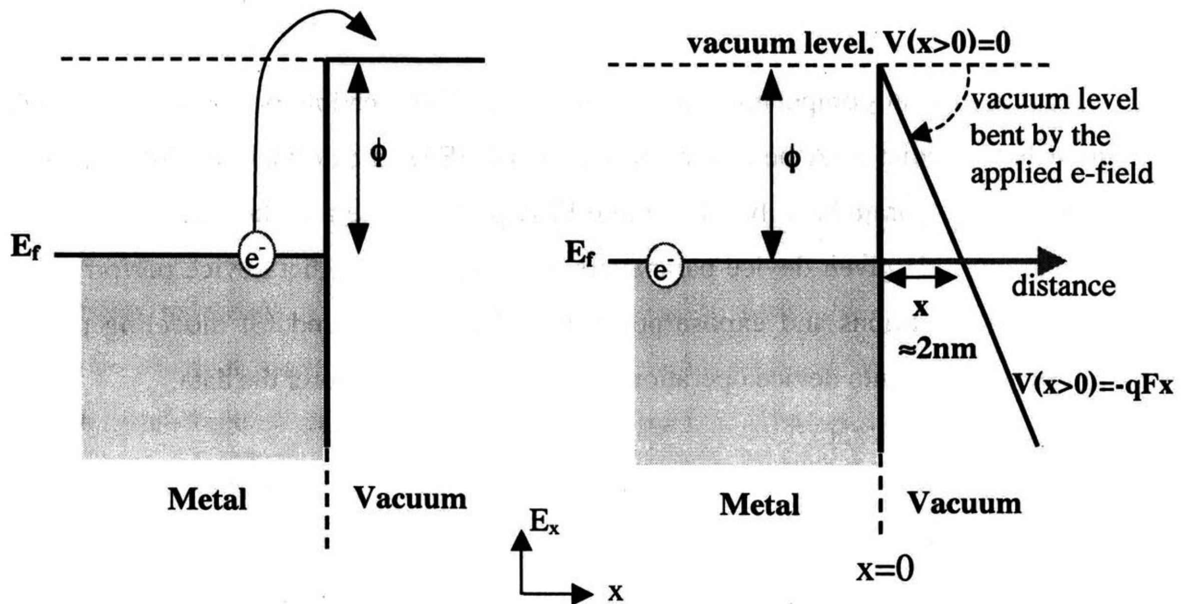


Figure 2-5. Two ways of electron ejection: (1) thermionic emission or photoemission and (b) field emission. ϕ is the work function.

Similar to metals, electron field emission from silicon occurs by reducing the width of the potential barrier at the surface with an applied electric field. Electrons in silicon are considered to be in a square potential well in relation to the surrounding vacuum, as shown in Figure 2-5 (b). If the vacuum is taken to be at zero energy, electrons near the Fermi level have the highest energy $-\phi$ (in eV) where ϕ is the workfunction of silicon. In an n-type poly-silicon, the workfunction, ϕ, is $\approx$4.05eV. The vacuum level will bend when a strong electric field (F) is applied assuming a triangular shape as depicted in Figure 2-5, for distances close to the silicon surface. This reduces the barrier width for the most energetic electrons allowing these electrons to tunnel through the barrier. Using arguments for an evanescent wave, we can estimate the threshold electrostatic field for electron emission. Significant transmission of electrons

through the barrier will only occur when the width of the barrier is of the order of 3X (or less) the electron wavelength in the barrier region. This occurs when the barrier width is of the order of 2 nm implying the threshold field for field emission is of the order of 2 V/nm (2 x 10^7 Vcm^{-1}). The number of electrons that tunnel through the barrier per unit time, per unit area (the field emission current density) is defined by the equation below:

$$J(F,E_x) = e\int_0^{\infty} D(F,E_x)N(E_x)dE_x \quad (\text{A/cm}^2) \tag{2.1}$$

$$D_{WKB}(F,E_x) \cong e^{-2\int k(x)dx}, \tag{2.2}$$

and $$k(x) = \sqrt{\frac{2m}{\hbar^2}(V(x,F) - E_x)}\,, \tag{2.3}$$

$$\begin{aligned} V(x,F) &= -(E_F + \phi) && \text{for } x < 0 \\ V(x,F) &= -qFx && \text{for } x > 0 \end{aligned} \tag{2.4}$$

where D(F, E_x) is the transmission probability through the barrier. F is the electrostatic field, E_x is the x-directed electron kinetic energy and V is the electrostatic potential energy. x is the width between the interface (x = 0) and the bent vacuum level. N(E_x) is the supply function comprised of the available electron states and the occupation of the states as determined by the Fermi function and it is given by

$$N(E_x) = \frac{4\pi m k_b T}{h^3}\ln\left(1 + e^{\frac{E_F - E_x}{k_b T}}\right) \tag{2.5}$$

where E_F is the Fermi-level, k_b is the Boltzman factor, m is the electron mass, T is the absolute temperature and h is Plank's constant. The emission current density equation can then be reconstructed as:

$$J = \frac{AF^2}{\phi t^2(y)}\exp\left[-B\frac{\phi^{3/2}}{F}v(y)\right] \tag{2.6}$$

where $A=1.54*10^{-6}$, $B=6.87*10^{-7}$ and $y=3.79*10^{-4}F^{1/2}/\phi$. $V(y)$ and $t^2(y)$ are the Nordheim elliptical functions added to account for image charge effects [2.2, 2.8]

Field Factor β and the tip radius r

As the applied field on the solid surface increases, the vacuum level would bend and the width of the energy barrier decreases. The narrower the width of the energy barrier, the more electrons tunnel through the barrier. Hence, the emission current increases. With several approximations ($t^2=1.1$ and $v(y)=0.95-y^2$), substituting $J=I/\alpha$ and $F=\beta V$, where α is the emitting area, the equation (2.5) can be simplified as follow:

$$I = a_{FN} V_g^2 \exp\left(\frac{-b_{FN}}{V_g}\right) \tag{2.7}$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B(1.44\times10^{-7})}{\phi^{1/2}}\right] \tag{2.8}$$

$$b_{FN} = \frac{0.95B\phi^{3/2}}{\beta} \tag{2.9}$$

where $\phi=4.05V$ in silicon. This is the well-known Fowler-Nordheim (FN) equation [2.2, 2.8]. The field emission current equations in Equations (2.7) to (2.9) relate the field F to the applied voltage V through the field factor β. A high value of β implies electron emission at low gate voltages. We explore the relationship between the field factor β and tip radius r below.

A typical field emission microstructure has a small tip radius located within a conducting gate electrode containing an annular aperture. When a high voltage, relative to the emitter, is biased on the extraction gate, a high electric field appears at the tip apex and nearby, which reduces the surface barrier width and increases the electron emission probability. It takes around 1-2 V/nm of the electric field to reduce the barrier width to 2nm for electrons to tunnel through to obtain reasonable emission current.

A good model for describing geometry effects in a field emitter cone structure is the "ball- in a sphere" model [2.5, 2.9, 2.10, 2.11, 2.12, 2.13, 2.14]. The schematic of this model is shown in Figure 2-6 [2.15]. The apex of the emitter cone is not strictly speaking a spherical ball. However, the smallest radius circle that could be drawn best represents the curvature of the tip apex. In Figure 2-6, the interior ball is analogous to the cone tip and the outer sphere is the gate. The ball in sphere can be solved analytically in spherical coordinates. A solution to Laplace's equation in spherical coordinates gives the electric field at the tip surface to be

$$F = \frac{V}{r}\left[\frac{d}{d+r}\right] \tag{2.10}$$

where d is the distance between tip center and the gate, and r is the radius of curvature of the tip. To the first order, where d >> r, $F \approx \frac{V}{r}$. In other words, $\beta \approx \frac{1}{r}$. To deduce a more accurate tip radius, a device model was built in Matlab by M. Ding, which uses a finite element method. The simulation result indicates that the field factor β varies with tip radius r as $\beta = \frac{22.73\times10^{5}}{r^{0.693}}$ (r in nm) [2.15]. This shows that the electric field is inversely proportional to the radius of the emitter tip. This means the smaller the tip radius is and the greater the electric field is to extract the electrons, and hence higher current. According to the Fowler-Nordheim equation, the emission current is exponentially dependent on the tip radius. A small change in the tip radius will result in a huge change in emission current. In addition, to obtain an emission current at lower operation gate voltage, a smaller radius is better [2.16, 2.17, 2.18].

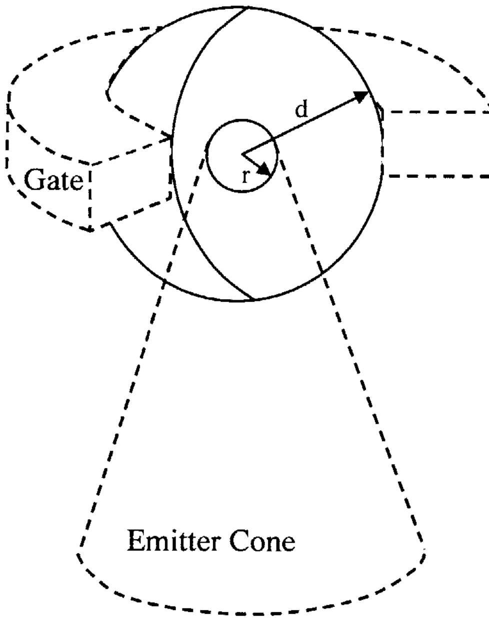


Figure 2-6. Ball-in-a-sphere model [2.15].

Bowling Pin Model of Conical Field Emitters

Next, we will show a result of an analytical model applicable to a conical field emitter with single or multiple gates. The model is based on using the orthonormal basis of Legendre functions to expand the potential of charged ring(s) in the presence of a grounded "bowling pin", i.e. a cone with a sphere centered on its apex. The Bowling Pin Model enabled us to prove the validity of the empirical IV equation for field emitters [2.5, 2.9, 2.10, 2.11, 2.12, 2.13]:

$$\ln\left[\frac{I}{V^2}\right] = a_{FN} + \frac{b_{FN}}{V} \qquad (2.11)$$

and the coefficients a_{FN} and b_{FN} that depend only on the geometric parameters of the device – the tip radius of curvature and the gate radius:

$$a_{FN} = -8.5 + Log\left[\alpha' C_G'^2\right] + 2V_0 Log\left[\frac{R_T}{R_G}\right] + 2Log\left[\frac{\upsilon_0 + (1+\upsilon_0)\gamma^{1+2\upsilon_0}}{1-\delta}\right] \qquad (2.12)$$

$$b_{FN} = -59\frac{R_G^{\upsilon_0} R_T^{1-\upsilon_0}}{C_G'\left(\upsilon_0 + (1+\upsilon_0)\gamma^{1+2\upsilon_0}\right)}(1-\delta) \qquad (2.13)$$

R_T is tip radius of curvature (ROC) in nm; R_G is the gate radius in nm, measured as the distance from the tip to the gate [2.2, 2.4, 2.5, 2.8, 2.19, 2.20]. Since the gate is co-planar with the tip is the most common, the equations above have been confined to this case {See L. Dvorson's thesis for details}.

$0.2 < \upsilon_0 < 0.4$ ($\upsilon_0 = 0.2$ will be used in fitting data)

$0.4 < \gamma < 0.6$

$$\delta \approx 0.92C_G'\left(\frac{R_T}{R_G}\right)^{\upsilon_0}\left(1-\gamma^{1+2\upsilon_0}\right)$$

$$Log(\alpha') \approx -2$$

C_G' is an adjustable parameter of order 1. It is independent of R_G and R_T.

The equations for a_{FN} and b_{FN} can be recast into other useful forms, for instance, the expression for the total emission current, I, in terms of the emission current density at the apex, J_A.

$$I = 2\pi R_{TIP}^2 \alpha' J_A = 0.14 \times 2\pi R_{TIP}^2 \times J_A \qquad (2.14)$$

and the expression for the gate field factor, β, which relates the electric field at the apex to gate voltage.

$$\beta \equiv \frac{E_A}{V_G} \approx 0.9C_G' \frac{1}{R_T}\left(\frac{R_T}{R_G}\right)^{\upsilon_0} \frac{\left(\upsilon_0 + (1+\upsilon_0)\gamma^{1+2\upsilon_0}\right)}{1-\delta} \qquad (2.15)$$

The field factor, which effectively sets the operating voltage of the device, is seen to be strongly dependent on the tip radius of curvature.

In addition, the BPM

- captures the true geometry of a circular gate around a conical field emitter and describes the dependence of the field factor on gate radius
- explains the effect of the vertical position of the gate with respect to the tip through gate-to-cone capacitance
- demonstrates the importance of tip eccentricity through the γ parameter.

Extension of the BPM to double-gated emitters produced expressions for the gate and focus field factors in terms of four capacitance coefficients.

$$E_A = \beta_G V_G + \beta_F V_F \tag{2.16}$$

$$\beta_G = \left[\frac{A_0 P_{0.2}(\mu_G)(R_T/R_G)^{0.2} 0.2(1+6\gamma^{1.4})}{R_T}\right]\left(C_{11}^{'} + \omega^{0.2} C_{12}^{'}\right) \tag{2.17}$$

$$\beta_F = \left[\frac{A_0 P_{0.2}(\mu_G)(R_T/R_G)^{0.2} 0.2(1+6\gamma^{1.4})}{R_T}\right]\left(\frac{P_{0.2}(\mu_F)}{P_{0.2}(\mu_G)}\right)\left(C_{21}^{'} + \omega^{0.2} C_{22}^{'}\right) \tag{2.18}$$

where β_G is the gate field factor, V_G is the gate voltage, β_F is the focus field factor, V_F is the focus voltage, and R_G is the radius of the gate aperture.

A way to compute the capacitance coefficients for a given device geometry has been presented making it possible to predict the relative effects of the gate and focus electrodes on the apex electric field and hence on the emission current [2.19, 2.20]. All of the preceding constitutes original contributions by the L. Dvorson [2.5].

2.3 Thesis Organization

The outline of this thesis is as follows:

In chapter 3, we discuss the design and the fabrication process of the FEA with an integrated focus electrode. Our process is based on L. Dvorson's Ph. D. thesis; however, we will make some improvement to obtain devices with better structure.

Chapter 4 and 5, the electrical and optical data and analysis are presented. Chapter 4 includes IV characteristic with three-terminal and four-terminal measurements. Chapter 5 examines the spot size of the FEA as a function of the focus voltage.

Chapter 6 presents the procedure and the result of the exposure of PMMA resist using field emission arrays.

Chapter 7 presents the summary of this thesis and suggestions for future work.

3. Device Design and Fabrication

3.1 Device design

Device Structure Selection— Geometry of the focus electrode in IFE-FEA

There are different ways to integrate the focus electrode into the FEA triode. They can be classified into four groups, according to focus position. In Figure 3-1, the global vs. local focus electrode informs us if each tip has its own focus (local scheme), or if a single focus is used to collimate emission beams from several tips (global scheme). In-plane vs. out-of-plane describes if the focus electrode is coplanar with the gate electrode or stacked above the gate electrode [3.1].

Figure 3-1. Classification of IFE-FEA according to device geometry [3.1].

In 1990, W. B. Hermannsfeldt confirmed that for focusing purpose the most effective device geometry is local-out-of-plane (L/OP) by detailed numerical modeling [3.2, 3.3, 3.4, 3.5, 3.6]. The L/OP configuration has the smallest radius of the focusing aperture, and the distance between the tip and the focus is minimized. Minimizing the tip to focus separation can improve beam collimation by observing the path of the electron.

Once the electron is emitted from the tip, it goes from the divergent region, which is dominated by the strong gate field to the focus region, which is dominated by collimating focus field. Obviously, the beam is collimated well when electrons pass from the gate region to the focus region sooner. This suggests that for optimal focusing the vertical distance between the gate and the focus should be minimized. However, there is a downside. When the focus electrode is too close to the field emitter, its negative charge will reduce the field at the tip and hence decrease emission current. Since our goal is to optimize the focusing, and the gate is closer to the tip than focus, we expect to be able to compensate for field reduction due to the focus by a relatively small increase in gate voltage L/OP IFE-FEA is hence our chosen.

Device Structure Dimensions

Our objective is to produce collimated electron beams to improve the resolution of high voltage field emission displays (FEDs). In order to achieve our goal, we need to choose the device dimensions to obtain the desired performance.

After choosing the L/OP IFE-FEA device structure for producing collimated electron beams, we also need to ensure that the current density is sufficient. This implies that the device would require higher extraction voltages (and lower focus voltages), which points to some inherent structural limitation for the L/OP IFE-FEA. One such limitation is the need for the structural support by insulators for both the gate and focus electrodes. The insulator is typically silicon dioxide. There is a limit to the maximum voltage or field the insulators can withstand. The breakdown field of silicon dioxide is $\approx 10^7$ Vcm^{-1}, however, a more reasonable design value that accommodates surface asperities is $\approx 10^6$ Vcm^{-1}. In order to sustain voltages of about 100 V, an oxide thickness of 1 μm is required between the emitter ground plane and between the gate electrode and the gate and focus electrodes. This thickness is increased to 1.25 μm to be on the safe side. Assuming the thickness of the gate and focus electrodes is each 0.25 μm, this implies that the emitter tips should be 3 μm tall. Furthermore, they should have a "cone-on-tower" structure to

minimize the gate-to-tip distance, which is critical for high field factor. The gate-to-tip distance of our device is 0.3 μm. The insulator for our device is low temperature oxide (LTO) deposited by low-pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). The breakdown voltage of LTO after densification at high temperature is similar to thermal oxide [3.7].

In order to have a low turn on voltage and increase the maximum current density, small tip radius is required. We also want to make the gate aperture as small as possible. See equations (2.16) and (2.17). The smaller the gate aperture is the stronger the electric field at the apex of the tip to extract more current.

$$E_A = \beta_G V_G + \beta_F V_F \tag{2.16}$$

$$\beta_G = \left[\frac{A_0 P_{0.2}(\mu_G)(R_T/R_G)^{0.2} 0.2(1+6\gamma^{1.4})}{R_T} \right] \left(C_{11}' + \omega^{0.2} C_{12}' \right) \tag{2.17}$$

To make the focus gate effective, we want to minimize the distance between the top of the gate opening and the bottom of the focus gate. By decreasing this distance, the electrons can pass through the extraction zone faster and are collimated by focus gate before the electrons spread further outwards. However, the gate and focus should have sufficient separation to prevent electrical short between them. We chose a gate-to-tip of 0.3μm for our device design. We also want the focus opening as small as possible to be more effective on focusing the electrons as in equation (2.16) and (2.18).

$$\beta_F = \left[\frac{A_0 P_{0.2}(\mu_G)(R_T/R_G)^{0.2} 0.2(1+6\gamma^{1.4})}{R_T} \right] \left(\frac{P_{0.2}(\mu_F)}{P_{0.2}(\mu_G)} \right) \left(C_{21}' + \omega^{0.2} C_{22}' \right) \tag{2.18}$$

Poly-silicon was chosen as the gate material for both gate and focus electrodes. The thickness of the poly-silicon layer is not critical but must be continuous and conductive. To make the poly-silicon electrodes conductive, the poly-silicon layer was later implanted with phosphorus. Due to depositions of thick oxides (≈4μm), we choose

the spacing between the tips to be 10μm, to prevent the interference between tips during the fabrication.

3.2 Formation of Sharp 3μm Tall Silicon Field Emitters

As indicated above, a small tip radius is desired in order to obtain emission current at a reasonable operating extraction gate voltage. The process flow for the fabrication of sharp and uniform silicon emitters is summarized in Figure 3-2. The fabrication starts with growing a 0.6μm thick thermal oxide on the n-type (100) 6-inch silicon wafers. The emitter arrays have different sizes: 1x1, 5x5, 10x10, 25x25, 50x50, and 100x100. The pitch of the emitter tip-to-tip distance is 10μm.

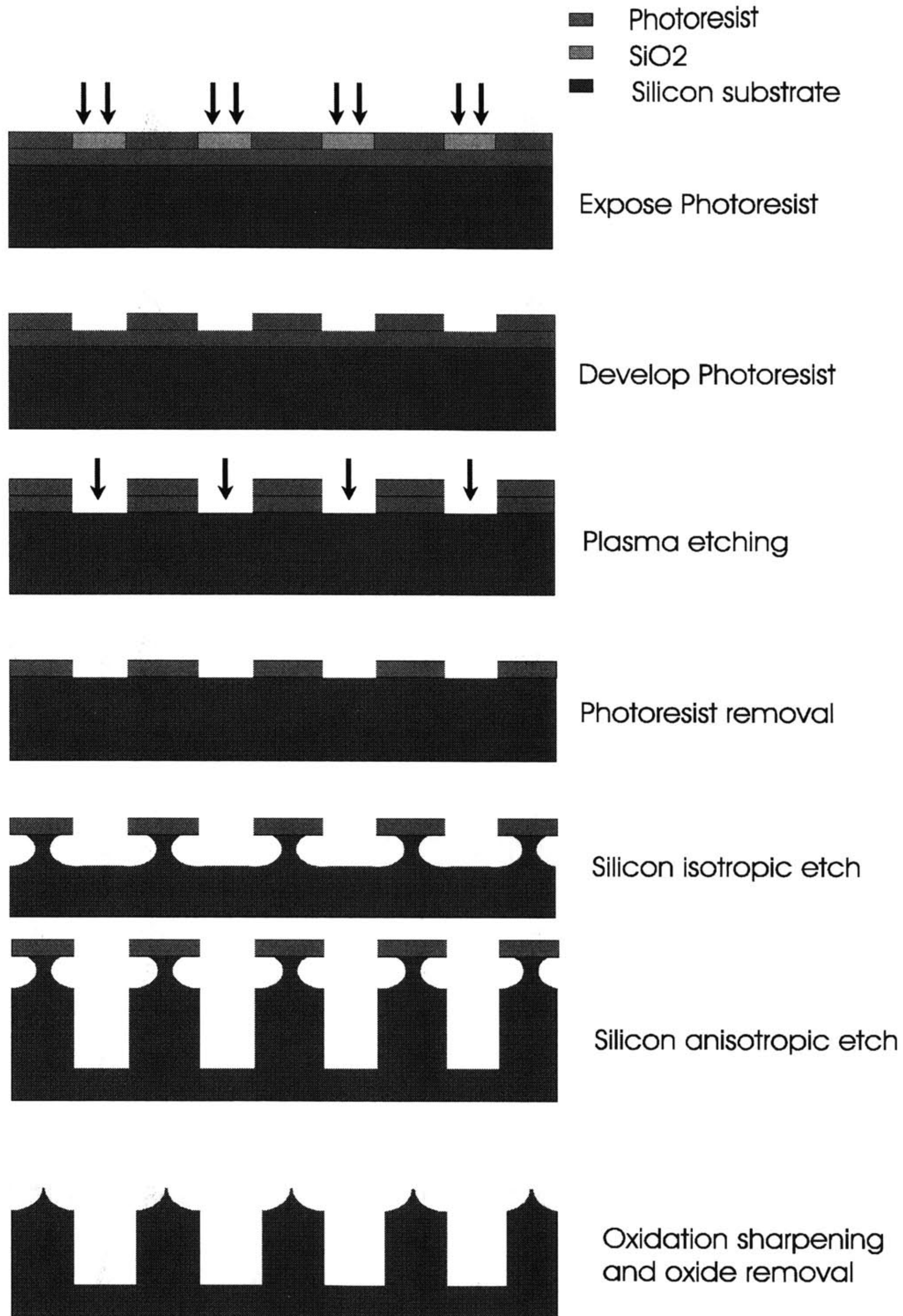


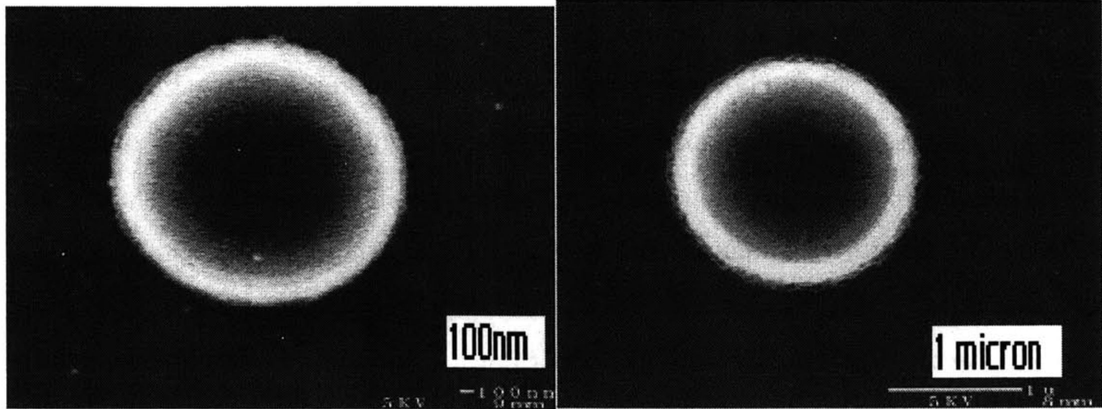
Figure 3-2. The process flow for the fabrication of sharp and uniform silicon emitters

Photoresist Dot and Oxide Dot definition

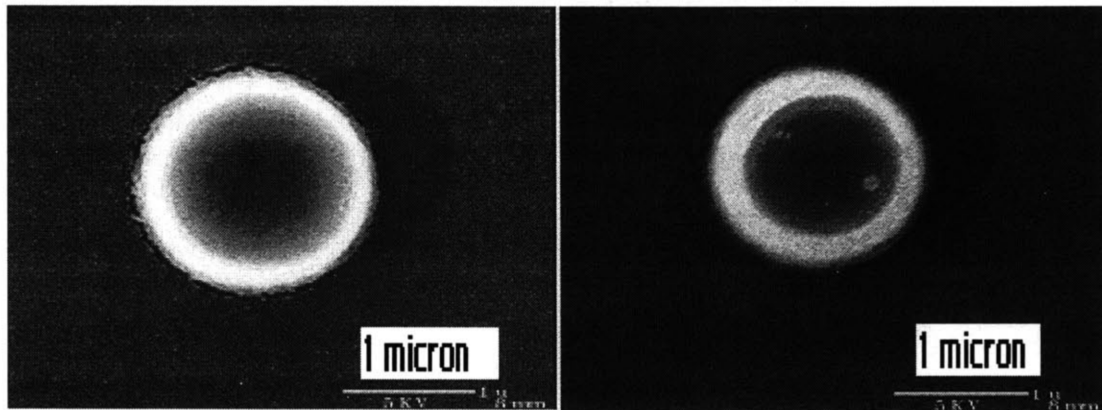
The first step of the fabricating sharp silicon emitter is to define masking-dots on the silicon. Here, thermal oxide will be the hard mask and photoresist (PR) is used to define the oxide disk. The thickness of the oxide disk is crucial. Silicon isotropic etch and anisotropic etch steps followed right after the oxide disk is made. Both steps use dry etch method, which does not have as good selectivity between silicon dioxide and silicon as wet etch. A 500 nm oxide disk is needed based on the silicon / oxide etch rate selectivity of about 6:1. To make it safer, 650nm oxide disk thickness was chosen. The wafers were oxidized with steam at 1000°C for 126 minutes to obtain an oxide layer with thickness of 660nm, followed by a coat of 1μm thick of photoresist.

There are three dimensions of the photoresist dot we need to pay attention to in order to complete the oxide disk etch step successfully later. First is the diameter of the photoresist dot. Initially, we started with the 1μm dot size on the mask. However, the diameter of the dot was reduced to less than 0.5μm because a longer exposure time is required to obtain uniform dot size. Overexposure of the photoresist leads to more uniform feature size across the wafer. Thus, we increased the diameter of the dot size on the mask to 1.7μm, based on several preliminary trial and error experiments. In order to obtain the best result, PR was exposed with different exposure time, 120ms, 140ms, 160ms, 180ms and 200ms and we examined the feature size and the cross section with a scanning electron microscope (SEM). Specifically, the photolithography step was as follows: Hexamethyldisilazane (HMDS) vapor phase application – photoresist spin-coating – soft bake (115 °C) – expose – post exposure bake (100 °C) – develop – hard bake (130 °C). Several wafers exposed at different exposure times were examined in an SEM at 5 keV. The samples were coated with a thin layer of Au/Pd to avoid charging in SEM. In Figure 3-3, we can see the slightly different sizes of the PR dot diameter with different exposure times from 120ms up to 200ms. The diameters of the PR dots vary from 1.7μm to 1.5μm.

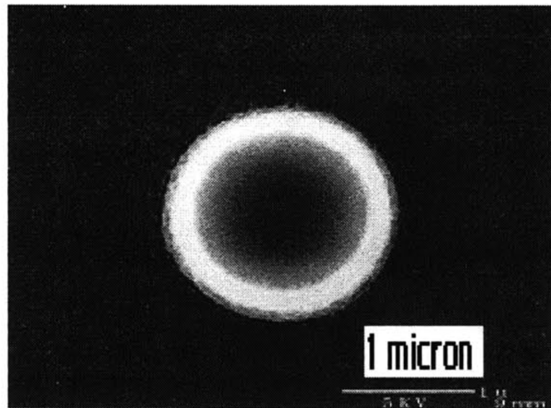
Second is the curvature of the photoresist dot's sidewall. A straight sidewall is desired instead of bell shape photoresist dot. A sloped photoresist sidewall results in a sloped oxide disk sidewall. If the photoresist is severely attacked during the oxide etch step, especially the edge of the photoresist dot, which is thinner, the oxide disk will turn out to be smaller than the original photoresist dot and have a non-uniform circular shape. The irregular oxide dot will lead to an inability to fabricate sharp 3μm tall emitters later. After looking at the top view of the photoresist dot to examine the diameter of the dot with SEM, we titled the sample 90 degree to see the sidewall of the dot. We saw straight sidewall for different exposure times. In Figure 3-4, we can see the cross section of the PR dots with 120ms and 160ms exposure time are straight, which gave us the oxide disk with the exact PR size when the oxide was etched later.



(a) (b)

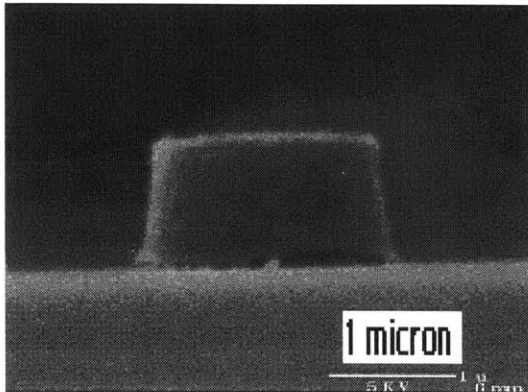


(c) (d)

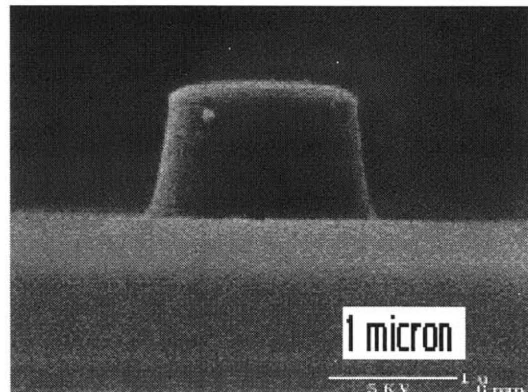


(e)

Figure 3-3. Various exposure times from 120ms up to 200ms (a) 120ms (b) 140ms (c) 160ms (d) 180ms (e) 200ms.



(a)



(b)

Figure 3-4. The cross section of the PR dots with 120ms and 160ms exposure time are fairly straight (a) 120ms (b) 160ms

The last dimension we need to pay attention to is the thickness of the photoresist dot. There is 0.66μm layer of oxide underneath the photoresist dot, which we need to etch away using the plasma. The etch selectivity between photoresist and oxide is about 1 to 6 or higher. According to this selectivity, 1μm of photoresist thickness is more than adequate to etch 0.66μm oxide layer allowing for 10% of over-etch. An over-etch process is necessary to clean the residual and native oxide on the silicon surface. Once all three dimensions of photoresist dot meet the required conditions, the photoresist dots were defined and they served as etching masks for the silicon dioxide layer. The anisotropic etch conditions were 25 sccm of C_2F_6 at a pressure of 3 mTorr. After the oxide disk was formed, the photoresist was removed in an O_2 plasma. Figure 3-5 is a photomicrograph of the oxide disk after reactive ion etch.

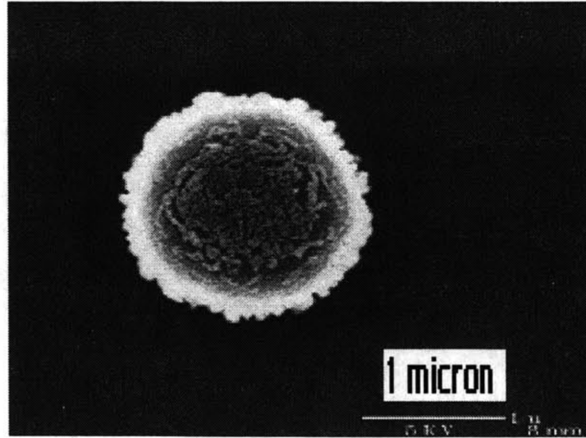


Figure 3-5. The oxide disk is formed after the reactive ion etch (RIE) .

Isotropic Silicon Etch

After obtaining uniform 1μm diameter oxide disk, this oxide disk was used as hard mask to etch its underlying silicon isotropically to form emitter cones. This closely followed the work of Dr. Han Kim who developed a process for making uniform arrays of silicon tips by isotropic plasma etch and oxidation sharpening in our laboratory [3.8]. SF_6 plasma was used for silicon isotropic etch. Several etching conditions were explored (19 sccm, 10 sccm, and 5 sccm of O_2) to obtain the best silicon cone profile, which would lead to a taller emitter cone before anisotropic etch. By changing the O_2 parameter, the horizontal etch rate changes without changing the vertical height. Finally, we used the recipe with 300 mTorr, 130 Watt, 190 sccm of SF_6 and 10 sccm of O_2 to etch silicon isotropically with Lam490B. The horizontal etch rate was 10nm/sec, the vertical etch rate was 13 nm/sec and the silicon surface remained smooth after etching. The ratio of horizontal to vertical length is approximately 2:3. The target thickness for the neck of the silicon cone is about 100 nm to 130 nm. Further isotropic silicon etching would cause the oxide caps fall off and destroy the neck region, which would harm the following step – anisotropic etch. Figure 3-6 shows the silicon cone with oxide cap after silicon isotropic etch.

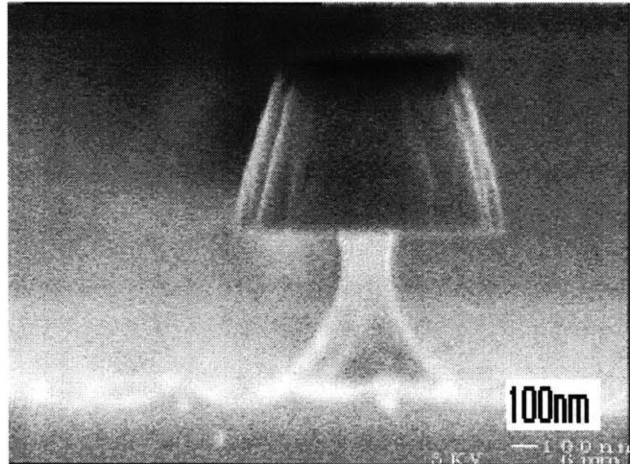


Figure 3-6. The silicon cone with oxide cap after silicon isotropic etch.

Anisotropic Silicon Etch

In Dr. Kim's process, the tip would now be sharpened via dry thermal oxidation. However, in order to avoid the large emitter gate leakage and early insulator breakdown, the tip height of 0.5-1 micron was insufficient. Anisotropic silicon etch was needed to increase the aspect ratio of the silicon emitter. Thus, we increased the tip height by using silicon reactive ion etch. In the Lam 490B, we used the recipe with 400 mtorr, 200 Watt, 134 sccm of H_2 and 96 sccm of Cl_2 to etch silicon anisotropically for 5mins in order to etch 2.5 microns deep. Now, the tip is about 3 microns tall, is shown in Figure 3-7.

Figure 3-7. The 3-micron-tall sharp silicon tip with oxide cap.

Oxidation Sharpening

Silicon oxidation is a sensitive reaction process. Silicon dioxide is grown when the dry oxygen or water vapor is introduced to the silicon wafers at elevated temperature. Dry oxidation was chosen due to its more severe retardation of curved silicon surface oxidation than wet oxidation. The key factors of oxidation are the oxidation temperatures and time durations. Based on process simulation, the recipe we used is 100 % dry O_2 at 950 °C for 15 hours in tube 5C in ICL. Figure 3-8 shows the silicon tip after oxidation sharpening.

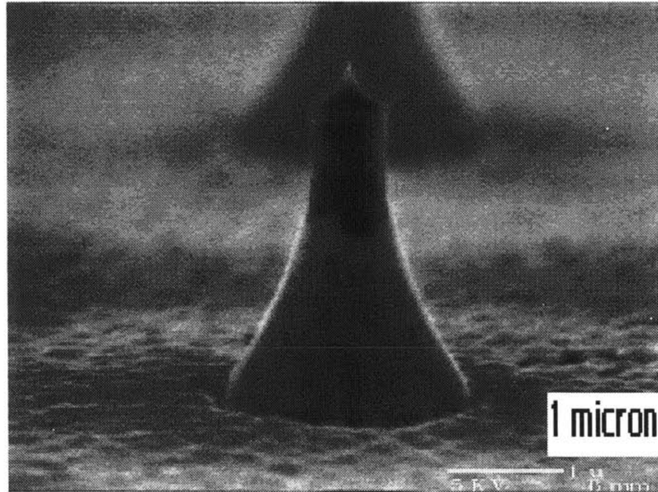


Figure 3-8. The silicon tip after oxidation sharpening step and removal of the oxide cap.

Deposition, planarization and Etch back of the Gate Insulator

The next two steps, shown in Figure 3-9, illustrate a novel technique, developed by L. Dvorson and used several times in the process. Using, LPCVD, we deposit a low temperature oxide (LTO) layer that is thick enough to submerge the tip. In our case, we should deposit 4μm thick of LTO to cover the 3μm tips, which is thicker than the tip height so the tips would not be destroyed at the next step – chemical mechanical polishing (CMP). The thick LTO layer is meant to protect the silicon tip from damage, while CMP planarizes the oxide surface. We used the 6C tube in ICL to deposit about 1μm LTO at a time and repeated it three to four times. In the end, we obtained 4.3μm thick oxide. A blunt bump was formed above every single emitter as shown in Figure 3-10 [3.9, 3.10, 3.11].

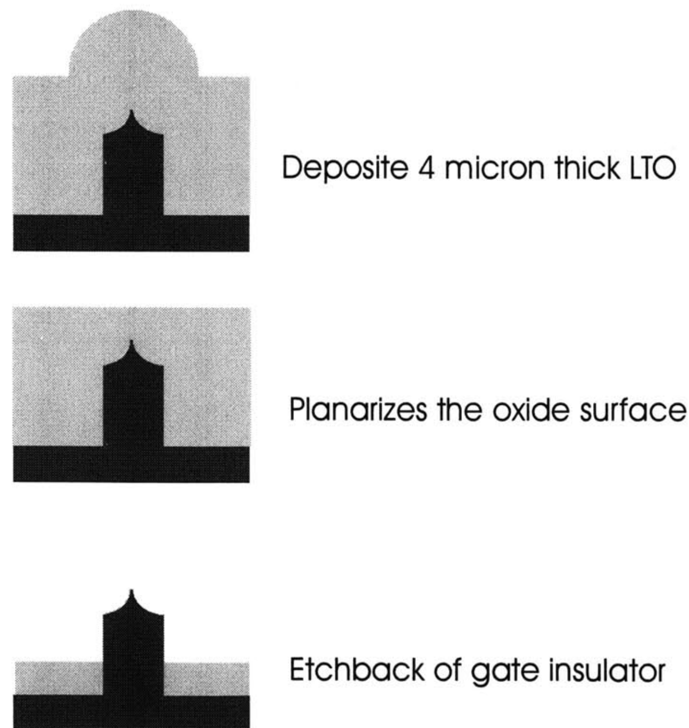


Figure 3-9. Illustration of a novel technique, which is used several times in the process. Deposition, planarization and etch back of gate insulator.

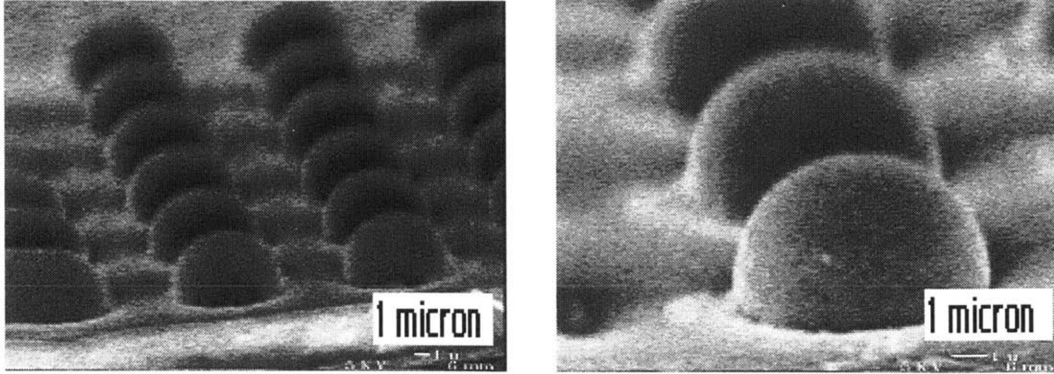


Figure 3-10. A blunt bump was formed above every single emitter.

Several CMP recipes were tried to insure the planarization is uniform. In Figure 3-11 are micrographs of planarization using different polishing times. We can see that the surface became flatter with longer polishing time. We polished the wafer until it was flat. Then we used BOE to etch back the oxide until 2μm oxide left. The 2μm oxide would be the insulator between the gate and the substrate. Then the oxide was densified in O_2 to increase the breakdown voltage. Afterward, a 0.3μm layer of LTO oxide was deposited to separate the tip and the poly-silicon layer, which next be deposited.

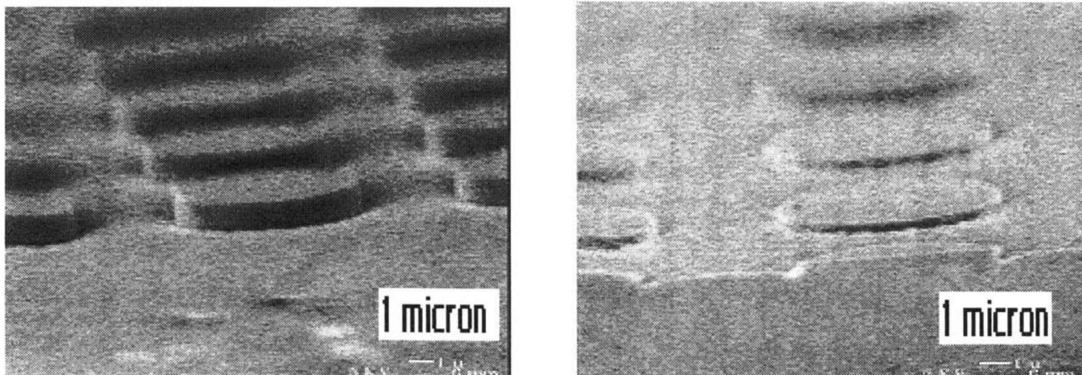


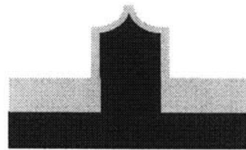
Figure 3-11. The oxide disk with different polishing times.

Formation of the Gate Electrode

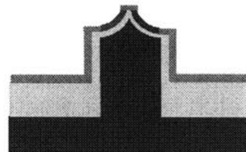
On top of the 0.3μm LTO oxide, 0.3μm of amorphous silicon was deposited. This amorphous silicon layer is the gate electrode. In order to make it conductive, the silicon layer was doped by ion implant with 2E15 cm^{-2} of phosphorus at 100keV [3.12]. For phosphorous implants at 100keV, the implant-projected range is 0.13μm and the standard deviation is 0.045μm. Note that the high-temperature drive-in was not done until later to keep amorphous silicon from the developing a grain structure. Now, the sequence of 'LTO deposition – CMP – BOE etch back' will be used to open gate aperture. Figure 3-12 shows the process of forming the gate electrode.

Next, another 2μm of oxide was deposited by using PECVD (Plasma Enhanced Chemical Vapor Deposition) system in ICL. The thickness of the deposited oxide was chosen again to exceed the height of the emitter, which allowed us to use the CMP to planarize the oxide surface. In single-gate devices, gate aperture can be revealed by CMP and careful SEM monitoring was required. Over-polishing in CMP would damage the silicon tip. On the other hand, under-polishing would form an emitter structure with silo-gate structure and silicon emitter tip would be below the extraction gate. However, we opened the gate using a different approach. After planarizing the oxide layer, we etched back the flat oxide layer by using BOE until the poly gate protruded 0.2-0.3μm above the oxide. Then an anisotropic silicon etch in the LAM490B was used to remove the protruded silicon material. The formed extraction gate has an aperture of only about 0.3μm.

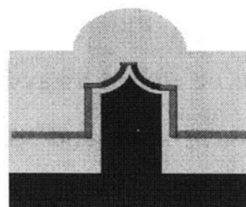
Amorphous silicon
Insulator
Silicon



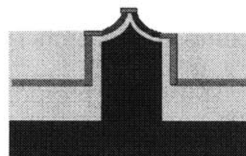
Deposit 0.3 micron of insulator



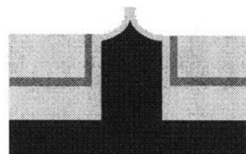
Deposit 0.3 micron of amorphous silicon



Deposit 2 micron of insulator



Planarizes the oxide surface
and etch back of the insulator

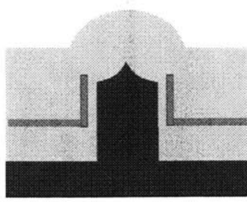


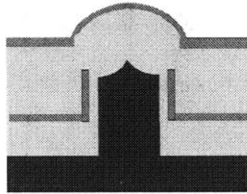
Etch the protrude amorphous silicon
to open the gate

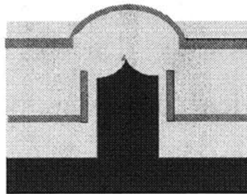
Figure 3-12. The gate electrode formation process.

Formation of the Focus Electrode

Our next step is to form the focus gate. First, we deposited 0.3μm of oxide by PECVD to form the insulator layer between extraction gate and the focus gate. Now, the top surface of the oxide is approximately level with the tip. Then another 0.3μm of the poly-silicon was deposited as the focus gate. In order to make it conductive, the silicon layer was doped by ion implant with 3E15 cm^{-2} of phosphorus at 100keV [3.12]. The focus aperture was opened in the same way as the gate aperture – Oxide deposition, planarization, oxide etch back, and anistotropic silicon etch. We deposited 2μm of oxide by PECVD followed by CMP to planarize the oxide surface. BOE was used to etch oxide until the poly bump protruded. However, at this point, the oxide layer is very thin (≈0.1μm or less) and a 0.3μm of poly-silicon needed to be etched away in the next step. This means that a recipe with a high selectivity between oxide and silicon is needed. There is an existing recipe, which was characterized recently, in AME 5000 in ICL that has a main silicon / oxide etch rate selectivity ~13:1 (pressure of 200 mTorr and Cl_2 of 20 sccm and HBR of 20 sccm) and an over etch silicon / oxide etch rate selectivity ~ 1000:1 (pressure of 100 mTorr and HBr of 40 sccm). With this recipe, we formed the focus gate successfully. The schematic flow of forming the focus electrode is shown in Figure 3-13.







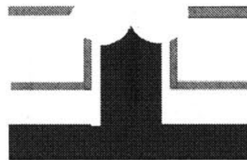


Figure 3-13. The schematic flow for forming the focus electrode.

Pattern contact electrodes for both gate and focus

In order to characterize our device, we need to have the contact pads for both gate electrode and the focus electrode. First, we coated our wafer with standard photolithography procedure and patterned Mask #2 on the photoresist. We used photoresist as mask and transferred the pattern onto the top silicon layer (focus electrode layer) by using anisotropic etch in AME 5000. The oxide layer beneath the top silicon layer with the electrode patterns is etched away with BOE. Then we repeated the same procedure – etch the second silicon layer (gate electrode) with AME 5000 and the oxide underneath the gate electrode with BOE. By doing these steps, the pads, which contact to focus gate was formed. Later, we used Mask #3 to make the contact with the extraction gate with the same procedure as we made the contact with the focus gate. There is a slight difference in the diameter of focusing apertures of different devices, depending on the extent to which the corresponding oxide masks were etched back (Figure 3-14). Now, both electrodes for gate and focus have been fabricated.

Annealing and Tip exposure

After contact patterning, the wafer was annealed in tube B3 in TRL at 900° C for 30 minutes with N_2. After the high-temperature drive-in, the gate and focus electrodes are conductive. The last step of our process is to "release" the structure with a BOE etch. This step would remove the oxide between the focus electrode, gate electrode and the field emitter. Now, Gate electrode is able to extract the electrons from the field emitter when voltage is applied and focus electrode is able to apply a negative horizontal force to collimate the electrons.

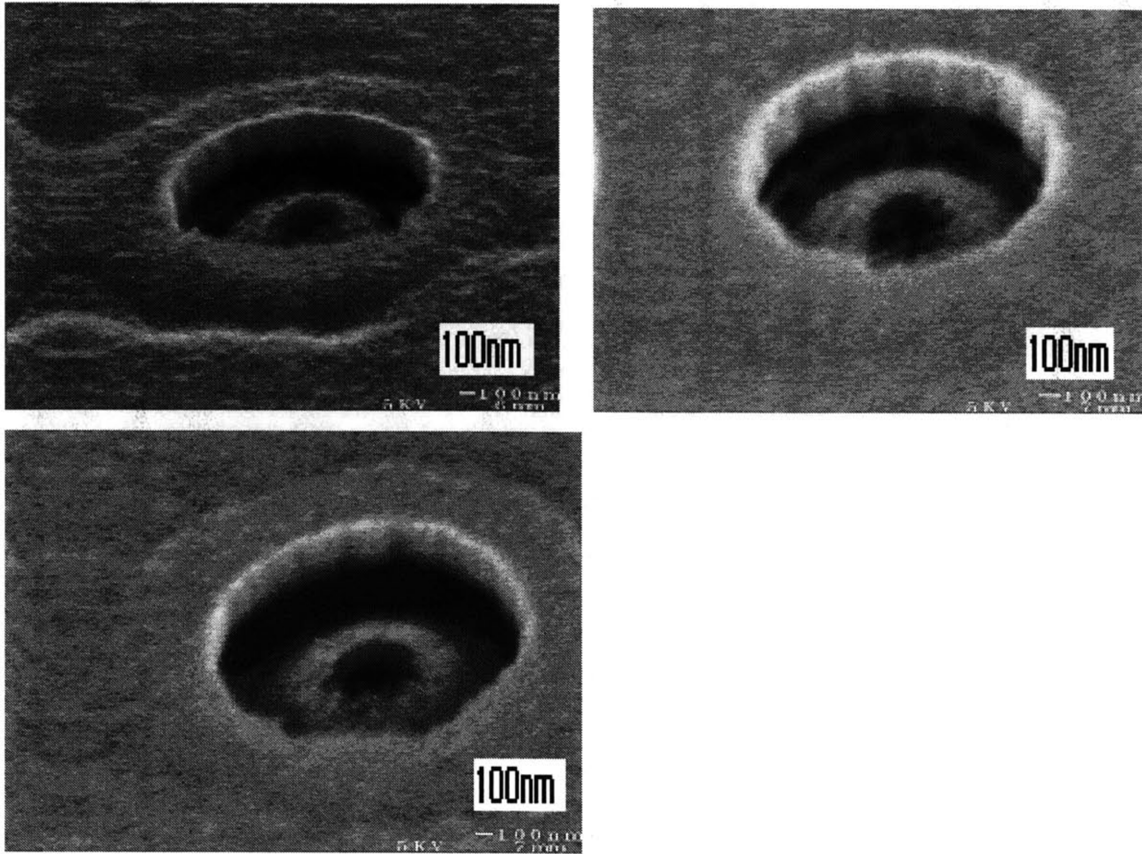
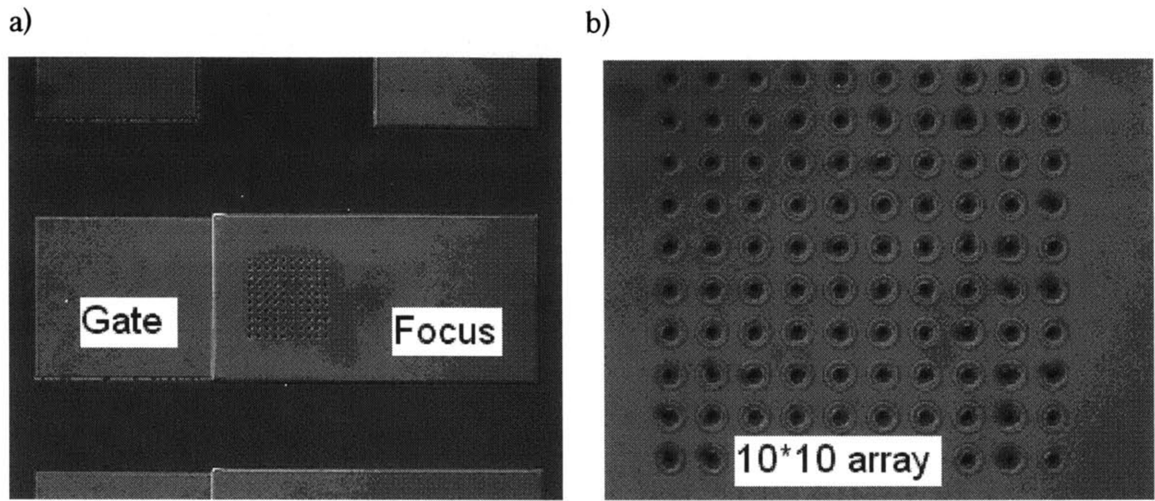


Figure 3-14. The 30º tilt SEM micrographs of the focus aperture and gate aperture.

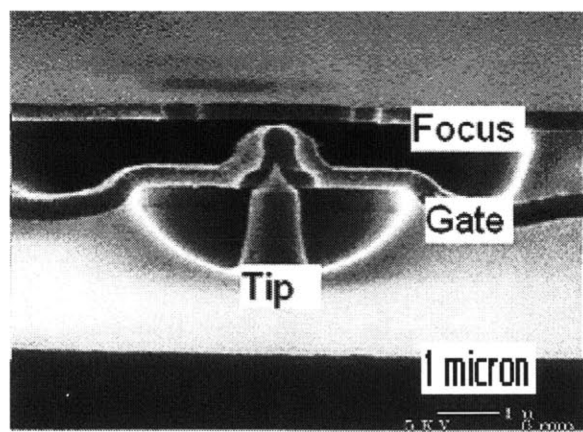
Completed Device

Figures 3-15 (a)-(c) show the optical micrographs and the SEMs of the completed device. In Figure 3-15 (a), the FEA with 10 X 10 array emitters with gate electrode and focus electrode is shown. The gate electrode extends to the left side of the emitters while the focus electrode is at the right side. Figure 3-15 (b) is a close look of the emitters. Figure 3-15 (c) is the SEM of the cross section of the device. We can clearly see the gaps between focus, gate and emitter and the relative position of the three electrodes

a) b)



(a) (b)



(c)

Figure 3-15 (a)-(c) shows the optical microscope photos and the SEM pictures of the completed device.

3.3 Chapter Summary

This chapter presented a modified version of L. Dvorson's process for fabrication of IFE-FEA. However, it is still not perfect. Here are the suggestions for improving the process. First, the tips could be made taller by about 1μm to allow thicker insulators between the electrodes. In addition, the spacing between the electrodes should be equal, for example, 2μm each. Second, the oxide between the gate and focus electrode could be densified to increase the oxide breakdown voltage. Finally, the CMP tends to damage the periphery of the die, most likely due to different polish rate. A strategy of using dummy fills around the die periphery and in the field regions to equalize the pattern densities should solve this problem.

In this chapter, we introduced a double-gated field emission device. We presented the design of the double-gated FEA and the fabrication process flow documented with SEM pictures. The process is capable of achieving gate and focus radii of 0.3μm and 0.6μm.

4. IV Characterization of Double-Gated FEAs

4.1 Measurement Setup

Electrical characterization of the FEA devices was conducted in an ultra-high vacuum (UHV) chamber at a pressure of about 2×10^{-9} Torr or lower without bake-out, field forming, or conditioning. Figure 4-1 is the photograph of the test station. The chamber on the right is the loadlock chamber and on the left is the main test chamber. On top of the chamber, a high-resolution camera magnifies the image of the wafer surface. The device was probed with very sharp tungsten probes and the backside of the wafer was contacted directly through the metallic stage, which is always grounded. To eliminate vibration that would break the probe contacts, the UHV chamber is mounted on a floating optical table. Triaxial cables were used for all signals to minimize noise and interference. Instrumentation included 5 source-measure units (Keithley 237), capable of simultaneously sourcing voltage and measuring current; and Labview, a computer interface program, provided remote control of the instrument and collected the data over the GPIB.

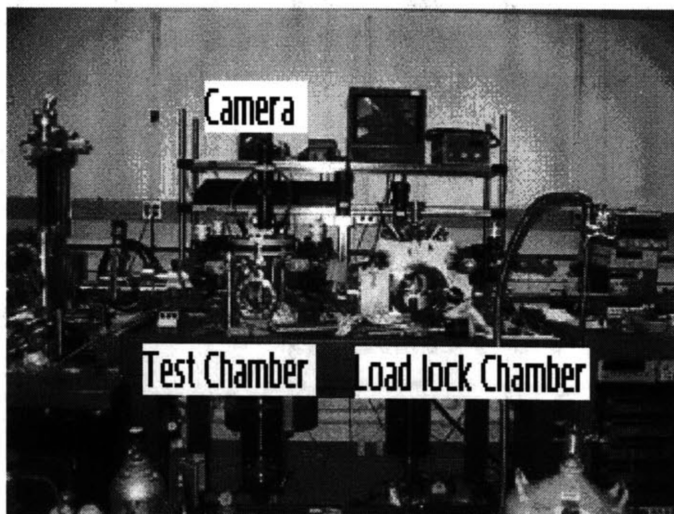


Figure 4-1. The photograph of the test station.

4.2 Device Description

From the SEM picture shown in Figure 4-2, we can clearly see the device structure - a high-aspect-ratio field emitter is formed with an extraction gate slightly above the tip and a focus gate that is about 300nm above the top plane of the gate opening. Gate and focus diameters are 358nm and 686nm respectively. However, we can see there are some oxide strips connecting the extraction gate and focus gate, which potentially could cause the short circuit between these two gates. Later, the author ran some four- terminal test measurements – first probe is on the extraction gate, second probe is on the focus gate and the third terminal is connected to the emitters (the backside of the wafer) to ground, which is attached with the metallic stage directly. These test measurement results agreed with the SEM pictures – the extraction gate and the focus gate are shorted in some devices. We can see the gate and focus currents have the same values but different signs. Amazingly, comparing the array sizes (1x1, 5x5, 10x10, 20x20, and 50x50), the 1x1 array has the highest yield of all different array sizes i.e. no shorts between gates. This is a good sign for us since we are more interested in the smaller arrays. In comparison to L. Dvorson's process, he had no 1x1 array working for four terminal measurements.

L. Dvorson's Ph. D thesis measurements focused on 5x5 arrays and 10x10 arrays; we took measurements on 1x1 arrays, 5x5 arrays, and 10x10 arrays for four-terminal measurements with more focus on 1x1 array measurements [4.1]. For three-terminal measurements, we took measurements on different array sizes (1x1, 5x5, 10x10, 20x20, and 50x50) to extract the Fowler-Nordheim coefficients.

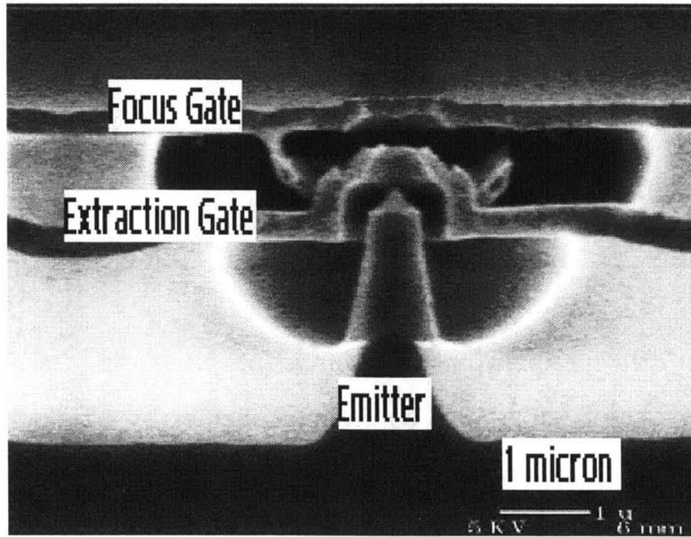


Figure 4-2. The SEM picture of the device. A high aspect ratio of field emitter is formed with an extraction gate slightly above the tip and a focus gate is about 300nm above the top plane of the gate opening. Gate and focus diameter are seen to be 358nm and 686nm respectively.

4.3 Three-terminal Measurements

Measurement and Analysis of Fowler-Nordheim coefficients

In order to perform three-terminal measurements to extract the FN coefficients, the focus gate and extraction gate were connected together by tri-axial cables to one Keithley 237. By doing this, we can make sure that there is no voltage difference between these two gates. The devices were probed on-wafer and the emitter current I_E, anode current I_A and gate current I_G were monitored. The diagram of the three-terminal setup is shown in Figure 4-3.

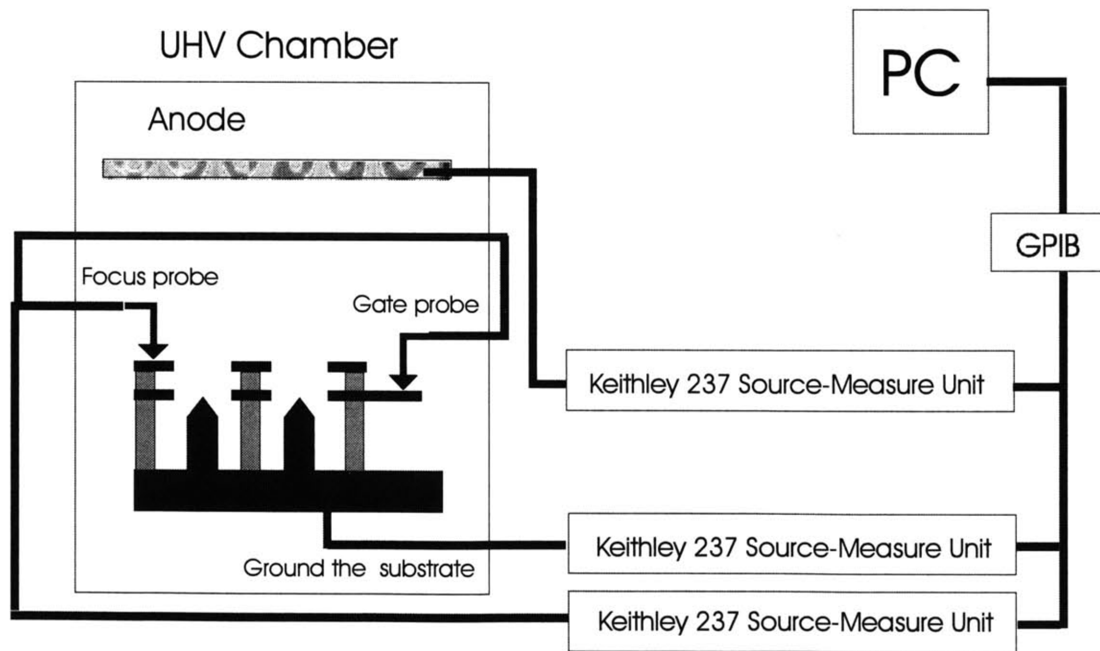


Figure 4-3. The diagram of the three-terminal measurement setup.

Obtaining a careful measurement of the FN coefficients requires more than a simple IV sweep. Our goal here is to ensure that the data we take to extract FN coefficients is not a one-time-only data. 21 up-down IV sweep measurements were done in sequence for all the arrays, 1x1, 5x5, 10x10, 20x20, and 50x50. Less fluctuation is expected from the larger arrays due to the averaging. The first ten and last ten sweeps recorded single measurement of the currents for each gate/focus voltage, while the eleventh sweep averages 20 current data points at each gate/focus voltage. The gate/focus voltages were swept up and down between 0V and 60V.

The data for 1x1, 5x5, 10x10, 20x20, and 50x50 arrays are shown in Figure 4-4 through Figure 4-8. Besides providing a careful measurement of the FN coefficients, the peak data is interesting in its own right. We note that the peak current is fluctuating between 20-60nA for 1x1 array. According to the measurement results, 5x5 array and 10x10 array have about the same current per tip. At the same time, 20x20 array and 50x50 array have much less current per tip. This is due to the non-uniformity of the tip radii in the larger arrays and the domination of the IV characteristics by the smallest tip radii, which are at the tail end of the distribution.

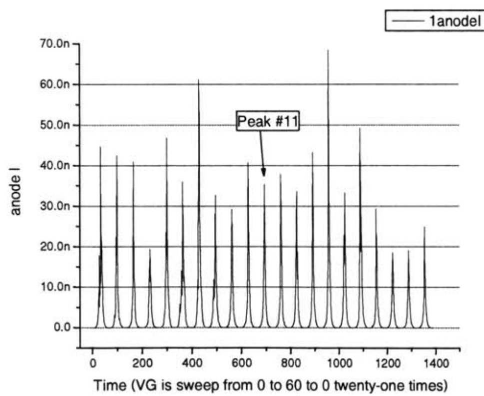


Figure 4-4. IV sweeps for a 1x1 array

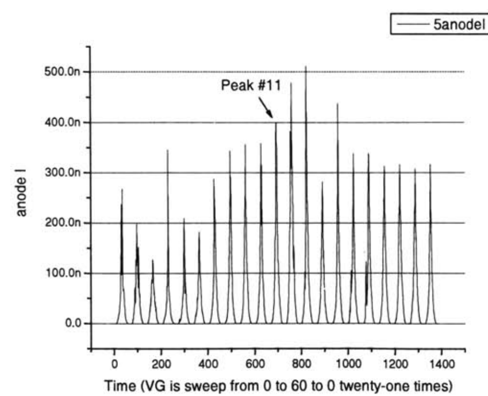


Figure 4-5. IV sweeps for a 5x5 array

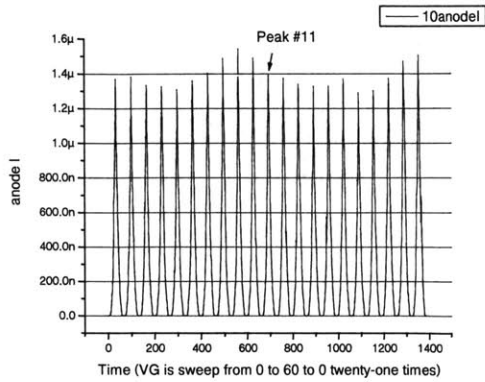


Figure 4-6. IV sweeps for a 10x10 array

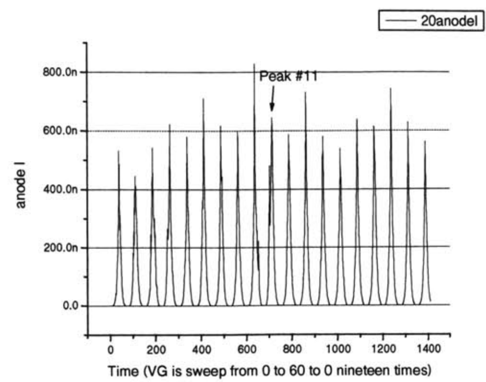


Figure 4-7. IV sweeps for a 20x20 array

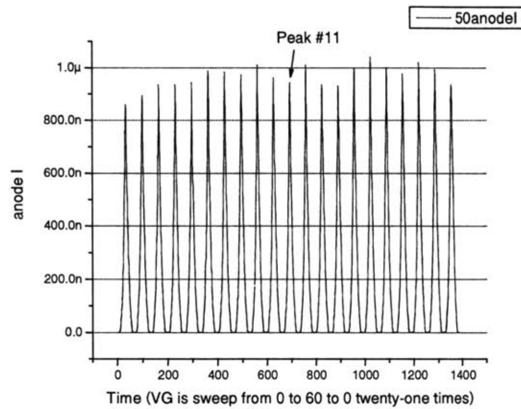


Figure 4-8. IV sweeps for a 50x50 array

Figure 4-9 through Figure 4-13 illustrate the fluctuations in the total emission current for all sizes of arrays through a plot of all 21 up-down current vs. gate voltage as opposed to time. From the plots, we observe that the 10x10 array and the 50x50 array have smaller fluctuations than other arrays while 1x1 has the most fluctuation.

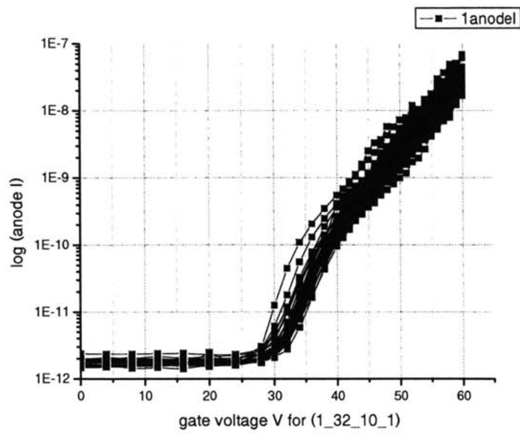


Figure 4-9. Repeatability of current reading for a 1x1 array (same data as in Figure 4-5).

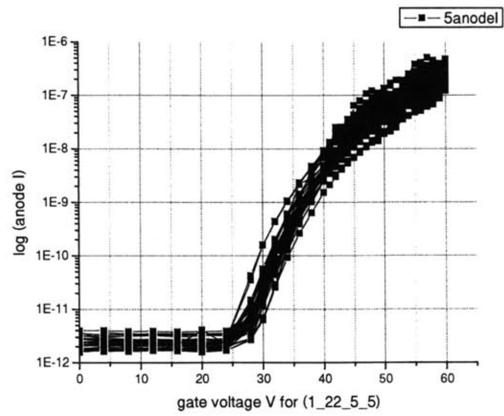


Figure 4-10. Repeatability of current reading for a 5x5 array (same data as in Figure 4-6).

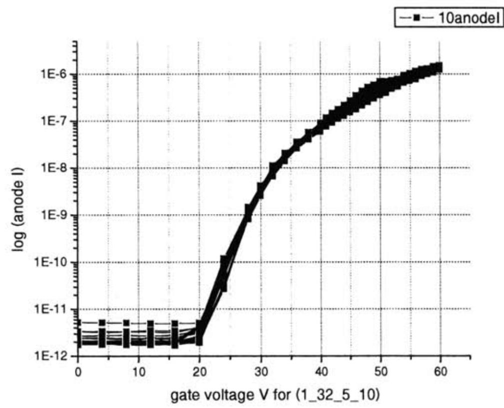


Figure 4-11. Repeatability of current reading for a 10x10 array (same data as in Figure 4-7).

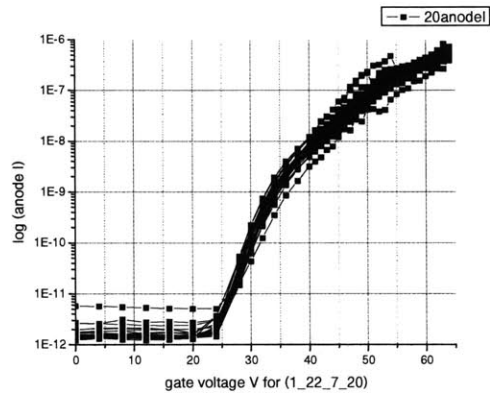


Figure 4-12. Repeatability of current reading for a 20x20 array (same data as in Figure 4-8).

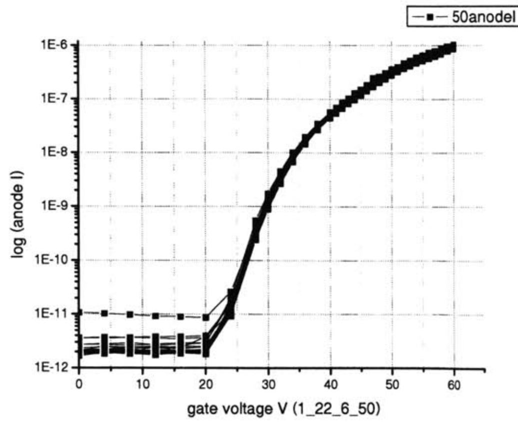


Figure 4-13. Repeatability of current reading for a 50x50 array (same data as in Figure 4-9).

Now, we can extract the FN coefficients. From the previous graphs, we observed that not all the tips are working in the larger arrays; however, we are more interested in the smaller arrays for the future applications, such as e-beam applications. We extracted the FN coefficients from the smaller arrays, 1x1, 5x5, and 10x10 arrays.

Using the Fowler-Nordheim (FN) equations (2.7), (2.8) and (2.9) in section 2.3, which is the current-voltage relationship of the field emission device, shown below, we extracted the Parameters: a_{FN} and b_{FN}:

$$I = a_{FN}\, V_g^2 \exp\left(\frac{-b_{FN}}{V_g}\right) \tag{2.7}$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B(1.44*10^{-7})}{\phi^{1/2}}\right] \tag{2.8}$$

$$b_{FN} = \frac{0.95 B \phi^{3/2}}{\beta} \tag{2.9}$$

where $A=1.54\text{x}10^{-6}$, $B=6.87\text{x}10^{7}$. I is the emission current, β is the local field factor at the emitting surface ($F = \beta \text{ x } V$), and V_g is the voltage applied to the extraction gate. α is

the effective emitter area. The barrier height in the FN equations is replaced by the electron affinity of silicon, χ, which is 4.05V in silicon.

In the extraction the FN coefficients, a source of concern is the variation of FN parameters with time. So for each array, we have three different plots for its FN coefficients. One plot is for the 11th sweep, which is the only one (up & down) sweep that averaged 20 data points at each voltage step, another plot is the up-sweep (left) half of the rest of the 20 peaks (no 11th peak), and the third plot is the down-sweep (right) half of the rest of the 20 peaks. Figure 4-14 (a) (b) (c) through Figure 4-16 (a) (b) (c) show the results of the FN coefficients with the error and standard deviation for 1x1, 5x5, and 10x10 arrays.

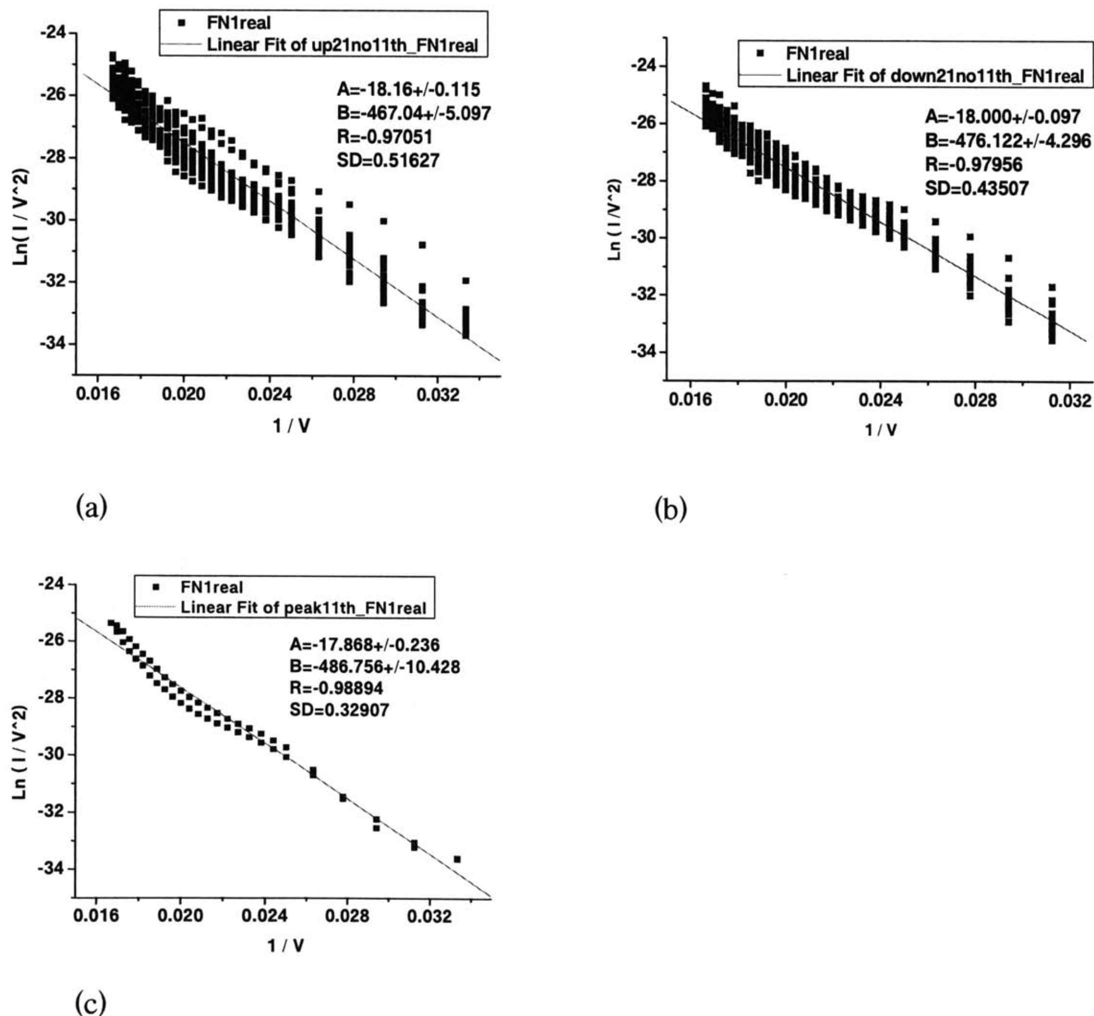
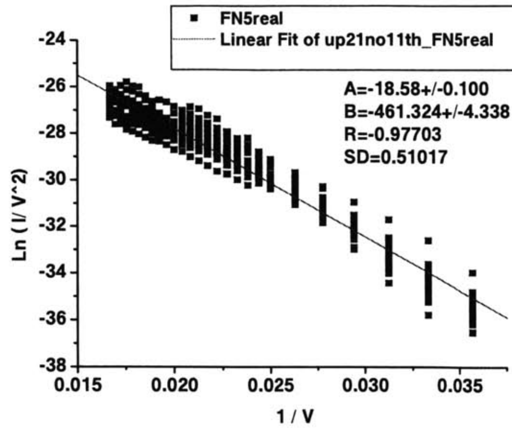
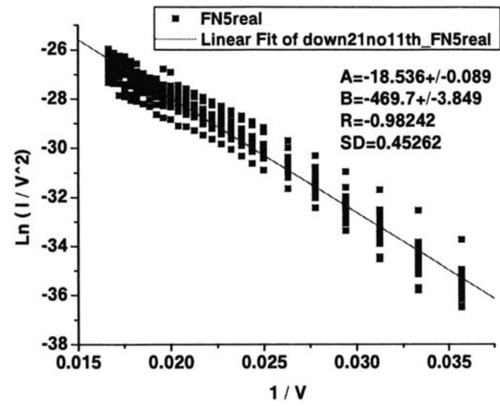


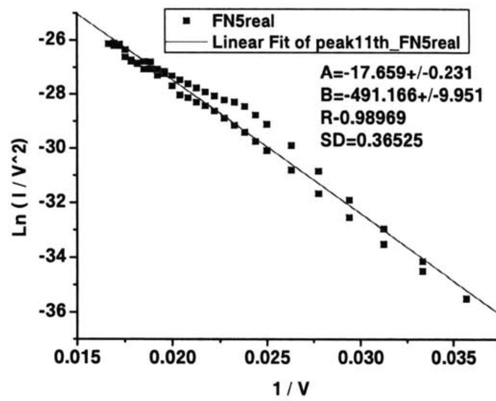
Figure 4-14. FN coefficients of array 1x1. (a)up sweep (b)down sweep (c) #11 peak sweep



(a)



(b)



(c)

Figure 4-15. FN coefficients of array 5x5. (a)up sweep (b)down sweep (c) #11 peak sweep

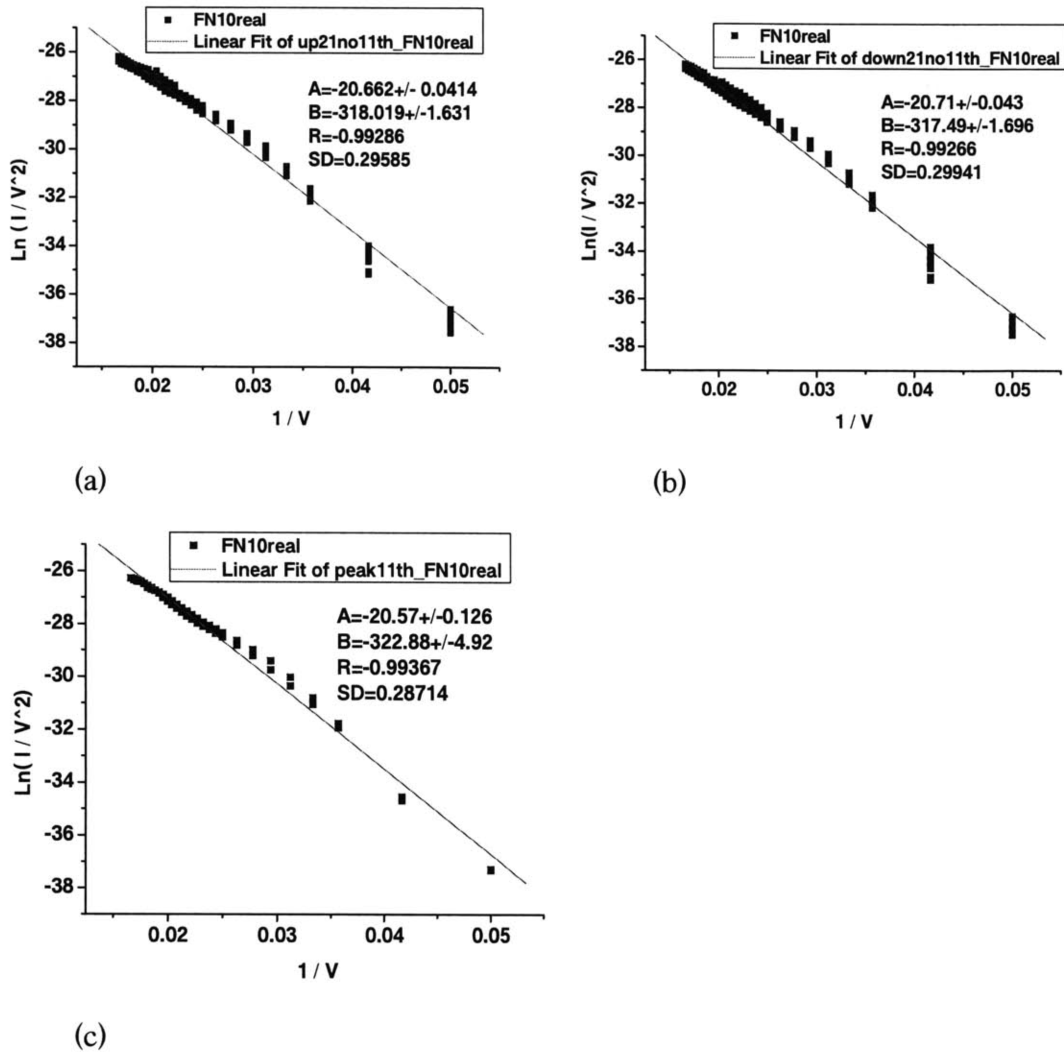


Figure 4-16. FN coefficients of array 10x10. (a)up sweep (b)down sweep (c) #11 peak sweep

The correlation coefficient, R, and the standard deviation, SD, are provided in each graph. These two numbers can help us to study the stability and the uniformity of the tips. R is a measure of the degree of linearity between two variables, say x and y. A value of R near +1 or -1 indicates a high degree of correlation between x and y, whereas a value near 0 indicates a lack of such correlation. A negative value of R indicates that y tends to decrease when x increases [4.2]. As for the standard deviation, it is a parameter that tells us how tightly all the data are clustered around the mean in a set of data. When the data are pretty tightly bunched together, the standard deviation is small.

It can be seen from the FN plots that all the values of R in our graphs are close to -1 and the standard deviations are relative small. Also, the FN coefficients show only little variation between up sweep, down sweep, and 11th peak, even for the 1x1 array. This indicates that the FN coefficients we obtained from three different types of sweep are consistent in time. We also observed that 11th peak is quite representative for the device behavior. 1x1 array has similar FN coefficients as 5x5 array (b_{FN}~480+/-10 and a_{FN}~18+/-0.5) while the b_{FN} of 10x10 array is less than other 2 arrays. Table 4-1 summarized the FN coefficients of three arrays. This indicates that the tips with smaller radius dominate in the larger array. Note: The FN coefficients of the 20x20 and 50x50 arrays are included in the Appendix B. The Fowler-Nordheim equation is an exponential in voltage and a variation of 2-3% is small for an exponential process. This suggests that the tip-to-tip uniformity is good.

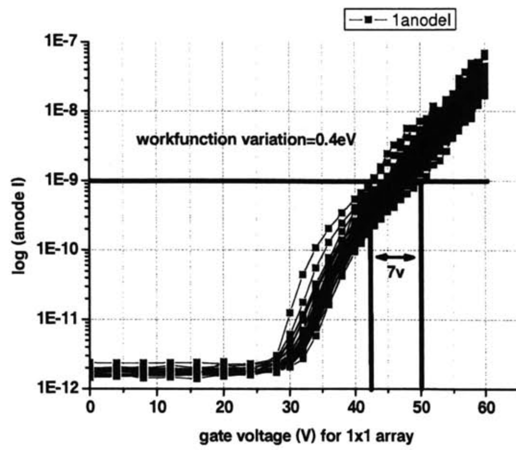
We constructed a finite element model in Matlab for the double-gated FEA using an approach similar to M. Ding [4.3]. Our results indicate that the effective field factor is given by $\beta = \frac{38.3\times10^5}{r^{0.753}}$ [V/cm] when V_F=V_G. (See Appendix D for details). We extracted tip radii of about 4.9-5.3nm for the 1x1 and 5x5 arrays while the corresponding tip radius for the 10x10 array is 3nm. The tip radii were extracted from the slope for the FN plots (b_{FN}) under the assumption that the workfunction of n-type silicon is its electron affinity χ=4.05eV.

	Up sweep			Down sweep			11th peak		
	b_{FN}	a_{FN}	SD	b_{FN}	a_{FN}	SD	b_{FN}	a_{FN}	SD
1x1	-467.0 ±5.0	-18.16 ±0.1	0.516	-476.1 ±4.3	-18 ±0.09	0.435	-486.8 ±10.4	-20.7 ±0.2	0.329
5x5	-461.3 ±4.3	-18.58 ±0.1	0.510	-469.7 ±3.8	-18.5 ±0.08	0.453	-491.1 ±9.95	-17.7 ±0.23	0.365
10x10	-318.0 ±1.63	-20.7 ±0.04	0.296	-317.5 ±1.7	-20.7 ±0.04	0.299	-322.9 ±4.9	-20.6 ±0.13	0.287

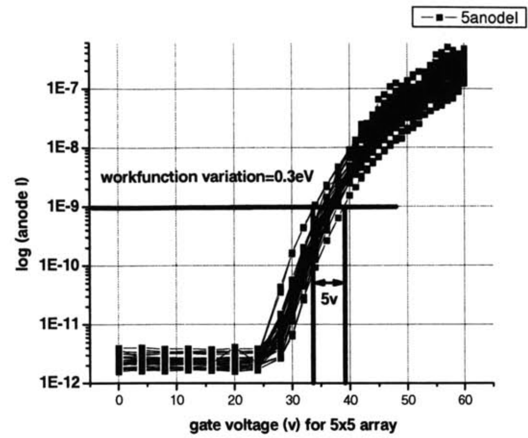
Table 4-1. Summary of FN coefficients.

Temporal Stability

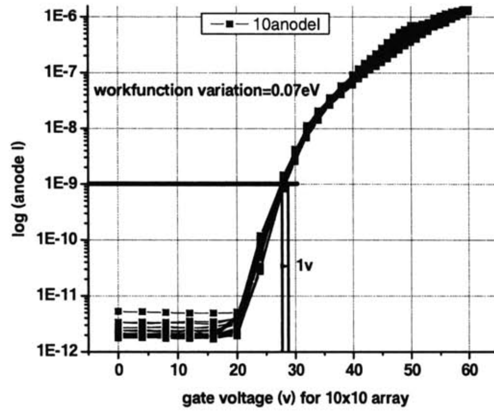
The principle sources of random variation of the emission current are the adsorption and desorption of foreign molecules on the emitter tip surface, which leads to variation in the electron transmission probability through fluctuations of the local work function (barrier height) or the local field factor (barrier width). Since the emission current is exponentially dependent on either barrier height or local field factor, a small change is work function lead to large changes in emission current. The 21 up-down I-V sweeps were done for each array to assess emission current fluctuations. The results are shown in Figure4-14 (a) (b) (c) through Figure 4-16 (a) (b) (c). To study the temporal stability and the array size relationship, we examined 1x1, 5x5 and 10x10, 20x20 and 50x50 arrays. In Figure 4-17 (a), the thick horizontal line shows that the voltages range over which a constant current of 1nA for 1x1 array could be obtained is ~7V (43V to 50V). This means to maintain a constant emission current of 1nA, the gate voltage variation of ~7V is required. The work function difference corresponding to this voltage range could be obtained by solving the FN equation, which was described earlier in this section. In order to calculate the work function variation, we set the work function equal to 4.05eV first to get the values of β and α. Assuming $\beta=1/r$ (r in cm) for simplicity, for array 1x1 r = 11.17nm, $\alpha = 2.58\times10^{-16}\ cm^2$, and the work function difference is 0.4eV. As for the other arrays, 5x5, 10x10, 20x20, and 50x50 arrays, we used the same method to obtain the work function variation at 1nA. From the graphs, we can see that the larger arrays have less variation in the work function. Table 4-2 summarized all the work function variation values for all the arrays.



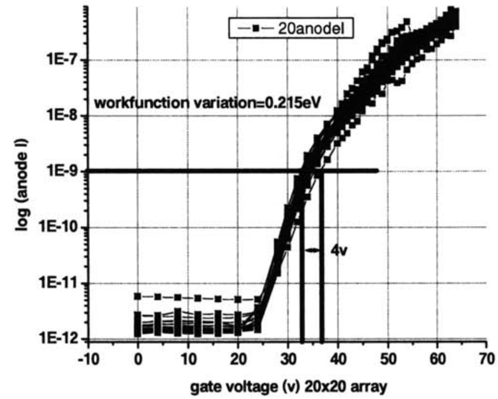
(a)



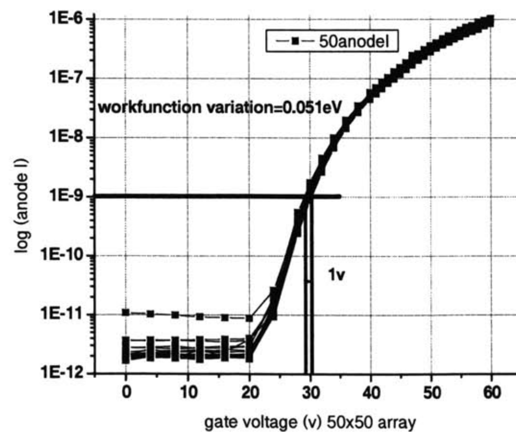
(b)



(c)



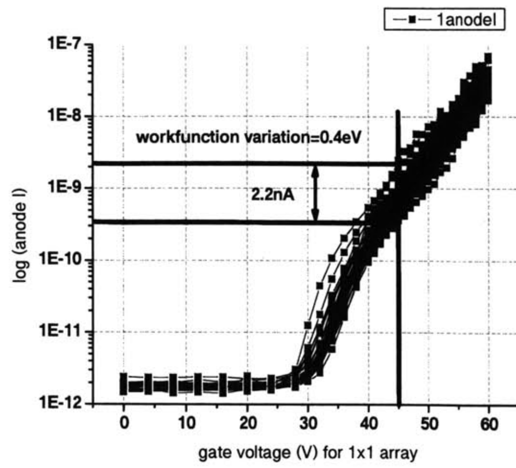
(d)



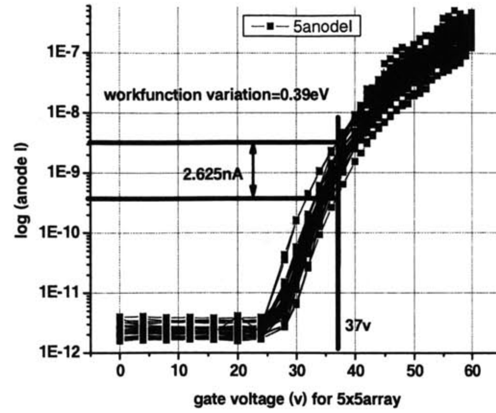
(e)

Figure 4-17 (a) (b) (c) (d) (e). I-V characteristics of 1x1, 5x5, 10x10, 20x20 and 50x50 FEA. The voltage range over a constant current of 1nA is to see the work function variations.

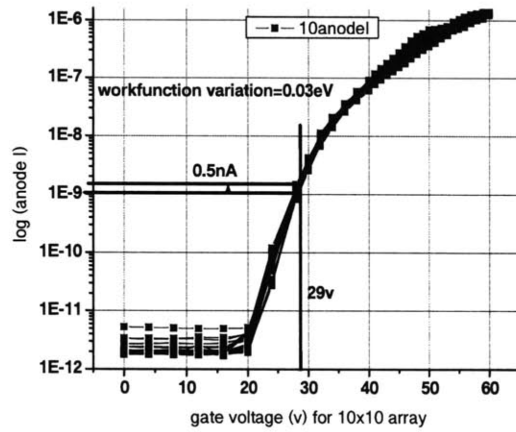
The vertical thick line in Figure 4-18 (a) shows that the current range over which a constant voltage of 45 V could be obtained is from 0.35nA to 2.59nA ($\Delta I \sim 2.24nA$). This means the field emission device is operated at the extraction gate voltage of 45 V, the current variation could be at the range of 2.24nA over the operation time. This current range corresponds to a work function difference of 0.4eV. We obtained this number by using the same method stated earlier. The variation for the 5x5, 10x10, 20x20, and 50x50 arrays were also calculated below. From the graphs, we can see that the larger arrays have less variation in the work function. Table 4-2 summarized the work function variation for each array. In order to see the relationship between the array size and the current fluctuation at specific gate voltage, we also calculated the anode current standard deviation for all the arrays at V_G=35V. In Table 4-3, we can clearly see that the value of $\Delta I / I_{AVG}$ becomes smaller as the array size gets larger. This means the current is more stable for larger array.



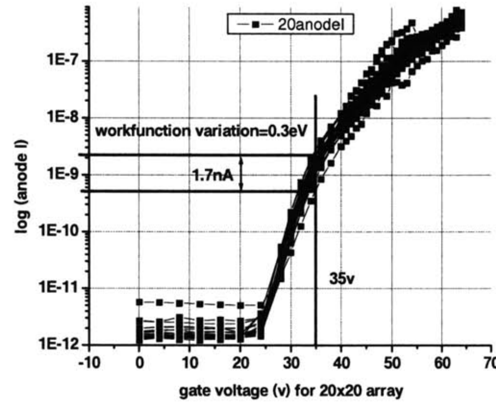
(a)



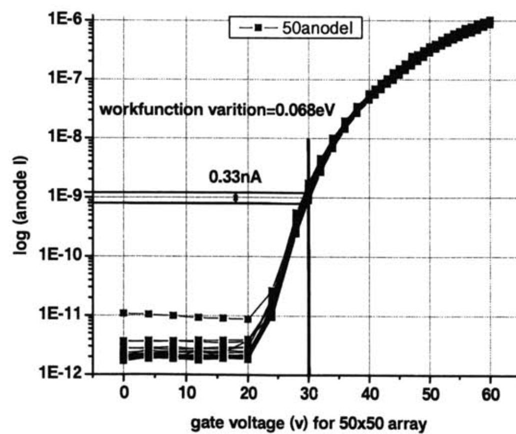
(b)



(c)



(d)



(e)

Figure 4-18 (a) (b) (c) (d) (e). I-V characteristics of 1x1, 5x5, 10x10, 20x20, and 50x50 FEA. The current range over a constant voltage value is to see the work function variations.

	1x1	5x5	10x10	20x20	50x50
The work function variation when I=1nA	0.4eV	0.3eV	0.07eV	0.215eV	0.051eV
The work function variation of a fixed gate voltage	0.4ev	0.39eV	0.03eV	0.3eV	0.068eV

Table 4-2. The summary of the work function variation of different arrays respect to fixed current or fixed voltage.

	1x1	5x5	10x10	20x20	50x50
Average current at V_G=35 (I_{AVG})	4.42×10^{-11}	9.35×10^{-10}	3.03×10^{-8}	2.36×10^{-9}	1.75×10^{-8}
Standard Deviation (SD or ΔI)	3.30×10^{-11}	4.63×10^{-10}	2.40×10^{-9}	6.16×10^{-10}	1.32×10^{-9}
SD/ I_{AVG}	0.745	0.495	0.0795	0.261	0.0756

Table 4-3. The summary of average current at V_G=35, standard deviation, and the ratio of SD/ I_{AVG} for all the arrays.

4.4 Four-terminal Measurements

The four-terminal measurement is similar to the three-terminal measurement. The difference is the focus is biased at a lower voltage than the extraction gate to collimate the beam. The diagram of the measurement setup is in Figure 4-19.

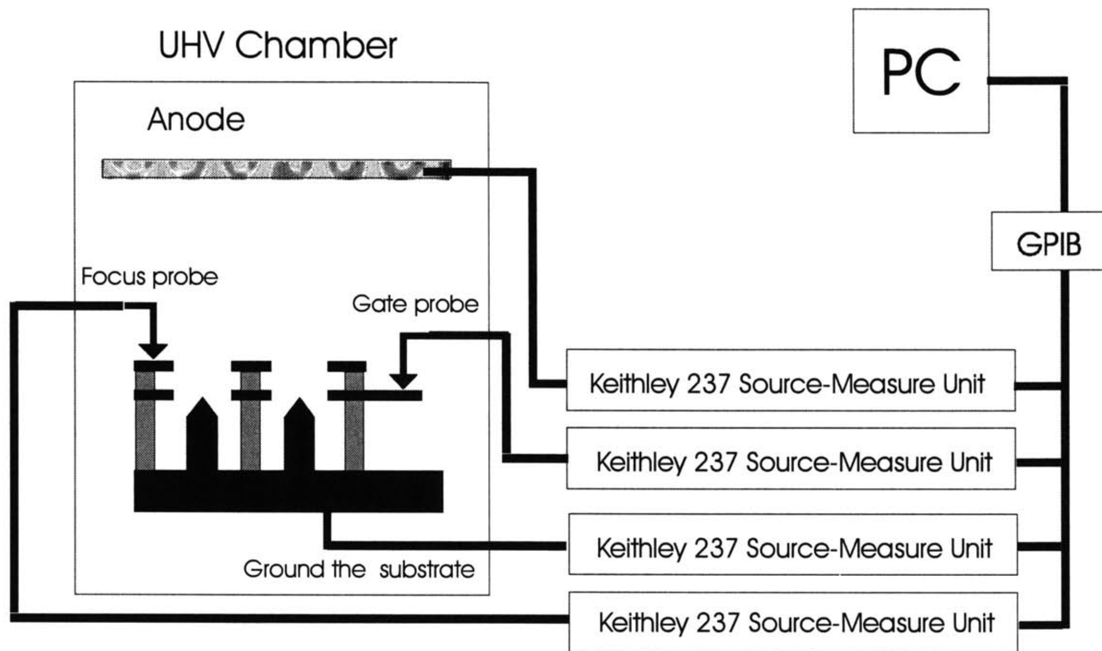


Figure 4-19. The diagram of the measurement setup

In section 2.3, the general IV equation for an IFE-FEA is given by:

$$I(V_{G,}V_{G}) = \alpha \times (4.27 \times 10^{-5}) \times (\beta_G V_G \times \beta_F V_F)^2 \exp\left[\frac{-55}{\beta_G V_G \times \beta_F V_F}\right] \quad (4.1)$$

β_G and β_F are in nm^{-1}.

From this equation, we know the influence of the gate and focus electrodes on the emission current are quantified by the gate and focus field factors, β_G and β_F. Our goal in this section will be to extract their values from the four-terminal IV data.

In the four-terminal measurement, one of the electrodes is fixed while the other is swept through the operation range. Figure 4-20 through Figure 4-22 are the measurement results for 1x1 array, 5x5 array and 10x10 array. The left hand side of each figure shows the gate transfer characteristics in which the focus voltage is fixed and the gate voltage swept from 0-70V. The right hand side of each figure shows the focus transfer characteristics in which the gate voltage is fixed and the focus voltage swept from 0-56V.

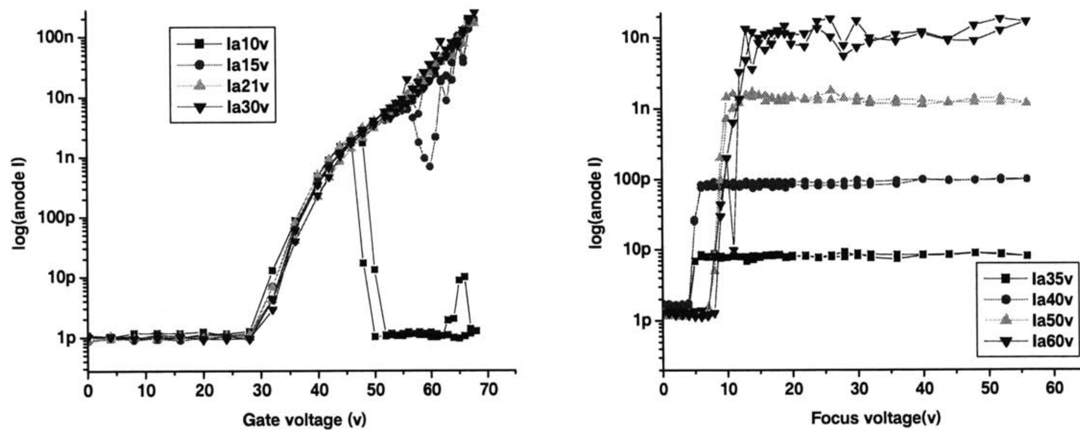


Figure 4-20. Four-terminal measurement IV data for a 1x1 IFE-FEA. Left: I_A vs. V_G at fixed V_F; Right: I_A vs. V_F at fixed V_G.

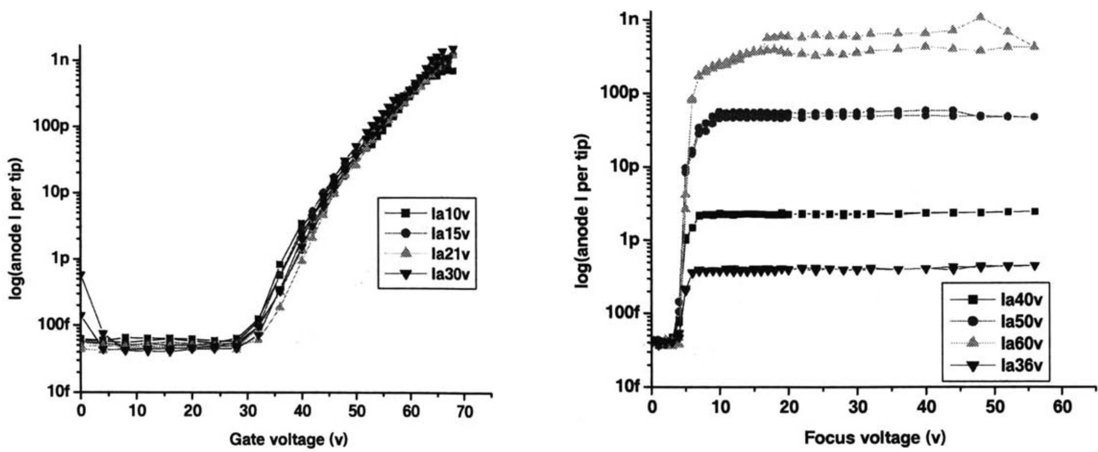


Figure 4-21. Four-terminal measurement IV data for a 5x5 IFE-FEA. Left: I_A vs. V_G at fixed V_F; Right: I_A vs. V_F at fixed V_G.

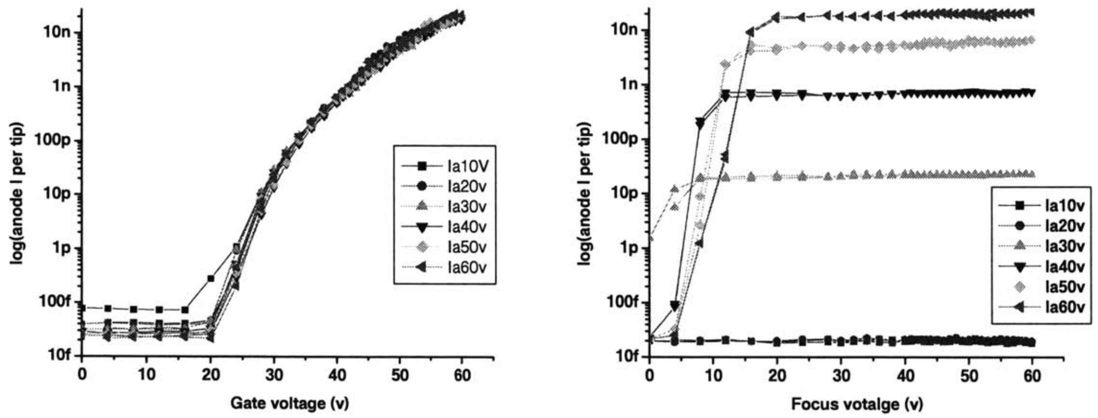
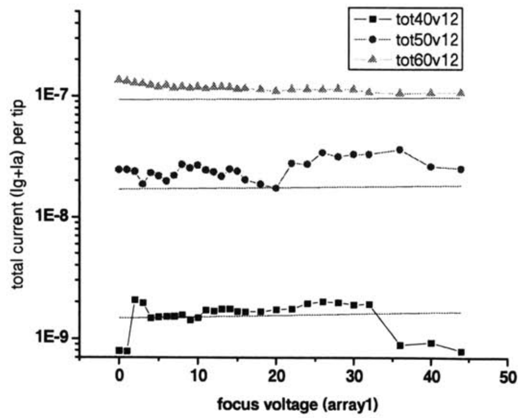


Figure 4-22. Four-terminal measurement IV data for a 10x10 IFE-FEA. Left: I_A vs. V_G at fixed V_F; Right: I_A vs. V_F at fixed V_G.

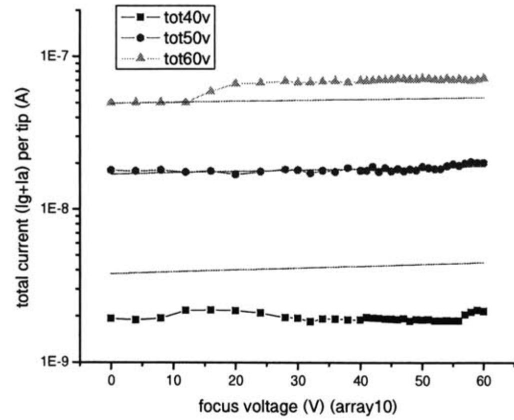
Looking at the right side of the graph, the anode currents are constant for focus voltage greater than ~15 V, which means that the anode currents are weakly dependent on focus voltages. Before fitting the data, we can predict that the magnitude of β_G is much larger than β_F for all devices, $\beta_G >> \beta_F$. To quantify this effect, we compute the total emission current by adding anode current and gate currents, and fit the data to equation (4.1). Since the focus current here is about 100 times smaller than the anode current and the gate current, we did not need to add the focus current into the total current. The results are shown in Figure 4-23. We observe that the fit for all arrays (10x10 array, 5x5 array and 1x1 array) are quite good, though not perfect fit. In the previous section, we saw how much current fluctuation is exhibited due to the change in workfunction, ϕ. Considering that temporal stability may have had an effect on the fit, we can rewrite equation (4.1), which is directly derived from fundamental electrostatics, into a generalized form for total emission current:

$$I(V_G, V_F) = a_J(\phi[t]) \times (\beta_G V_G \times \beta_F V_F)^2 \exp\left[\frac{b_J(\phi[t])}{\beta_G V_G + \beta_F V_F}\right] \quad (4.2)$$

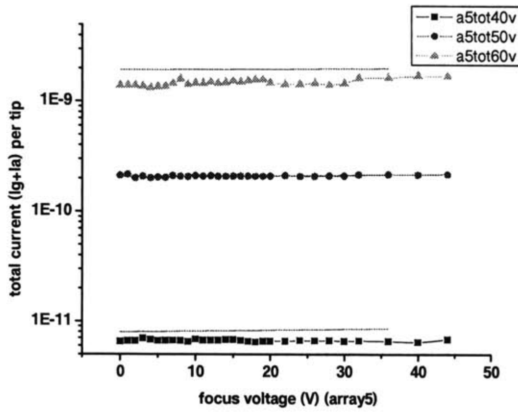
where the value of the work function ϕ fluctuates randomly with time. Thus, the currents fit to equation (4.1) are in fact produced by different values of the work function and should be fit to equation (4.2). In the previous section, we show how much the work function varies and we cannot predict the exact the work function at any one moment. We also used the value of area factor, α, from the previous section (three-terminal measurement) to fit in four-terminal measurement fitting equation as a rough estimate value. Also, due to the non-uniformity in the process, the structure dimensions varied across the wafer, especially the gate and focus apertures. From those effects described above, we should have significant variation of the values for β_F and β_G for each array. However, this should not affect the ratio of β_F / β_G. After using the equation (4.1) to fit the data, the values of β_G are about 100 times bigger than the values of β_F in three cases, which agreed with our prediction $\beta_F > \beta_G$. Table 4-4 summarizes these parameter estimates.



(a)



(b)



(c)

Figure 4-23. Emission current vs. Focus voltage at fixed gate voltage based on equation 4.1. (a) 1x1 array (b) 10x10 array (c) 5x5 array

Matlab Simulation

In L. Dvorson's Ph. D thesis [4.1], we know that the ratio of the gate and focus field factors correlated with the relative position of the tip and the gate. There are three different types of the relative positions of the top and the gate. One position is that tips are above their gate openings and in fact closer to the focus electrode. In this case, the focus field factor than the gate field factor ($\beta_F > \beta_G$). Another position is that tips are in the same plane of the gate opening. In this case, the field factor for the focus is about the same as the field factor of the gate ($\beta_F \sim \beta_G$). The third position is that tips end up below their gate openings and shielded from the effect of the focus. In this case, the focus has a smaller field factor than the gate ($\beta_F << \beta_G$). A member of our group, Guobin Sha, built models of these geometries in Matlab to quantify this effect [4.1].

Here, we wanted to double check if we would obtain similar simulation results for the tip above, in plane, and below the gate opening, for our structure. To quantify this effect, we built models of our device geometries in Matlab (courtesy of Goubin Sha), using the SEM pictures of our devices in Figure 4-24 (b) and (c) for guidance. Later, we used the same structure dimensions but vary the tip heights, relative to the top of the gate opening to see the change of the ratio of β_F / β_G. In Figure 4-24 (a), we chose the focus aperture to be 1.2μm and the gate aperture to be 0.4μm, according to the SEM picture in Figure 4-25 (b). Also, from Figure 4-24 (c), we know that the tip is 0.4μm below the gate opening, the bottom of the focus gate is 0.2μm above the top of the gate opening, and the gate protruded 0.4μm above its flat area in the tip area. These important dimensions described above are all drawn in Figure 4-24 (a).

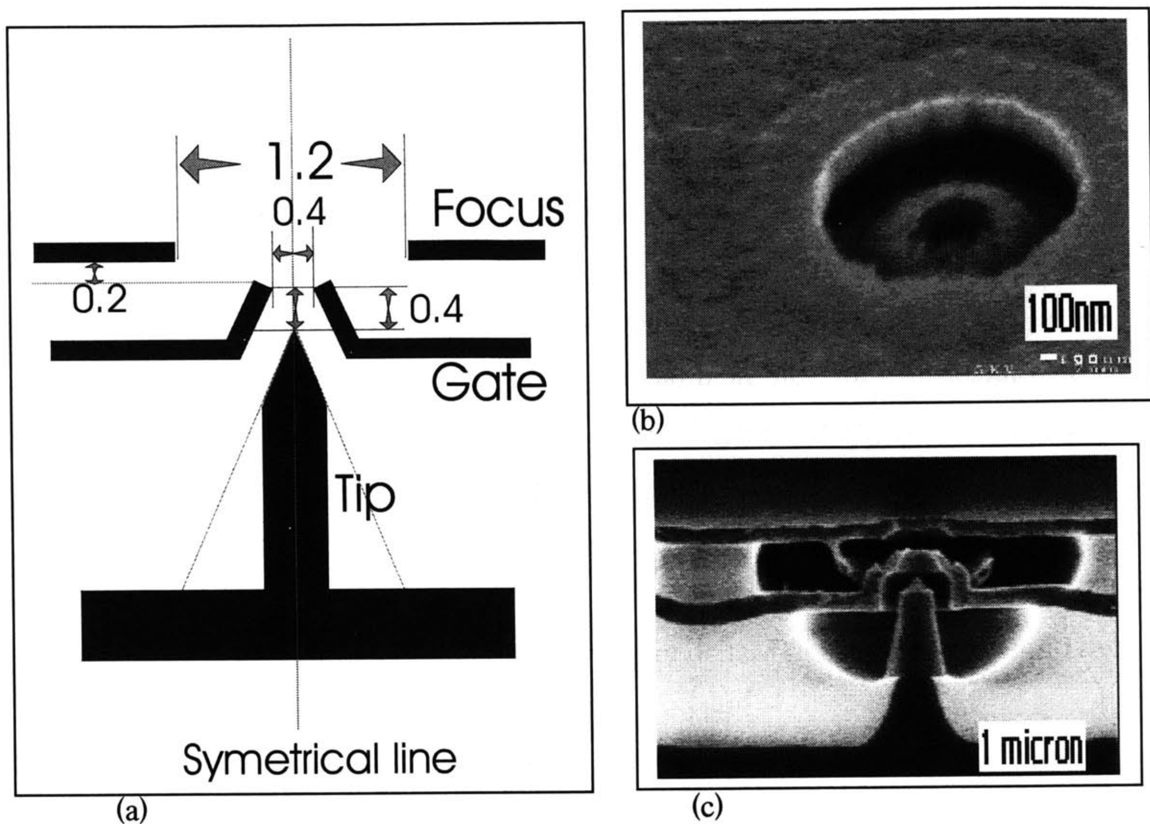


Figure 4-24. (a)The schematic diagram of the structure is shown in (a) following dimensions obtained from the SEM pictures in (b) and (a). (b) The dimensions of gate aperture (0.4μm) and focus aperture (1.2μm) were selected based on this SEM picture. (c) The relative positions of gate electrode, focus electrode and the tip are shown in this SEM picture.

For simplicity, the device structure simulated assumed the conical structure shown in Figure 4-25 (a). Furthermore, since the structure is axially symmetrical, only half of the device structure was needed, as shown in Figure 4-25 (a). The real Matlab picture is shown in Figure 4-25 (b)

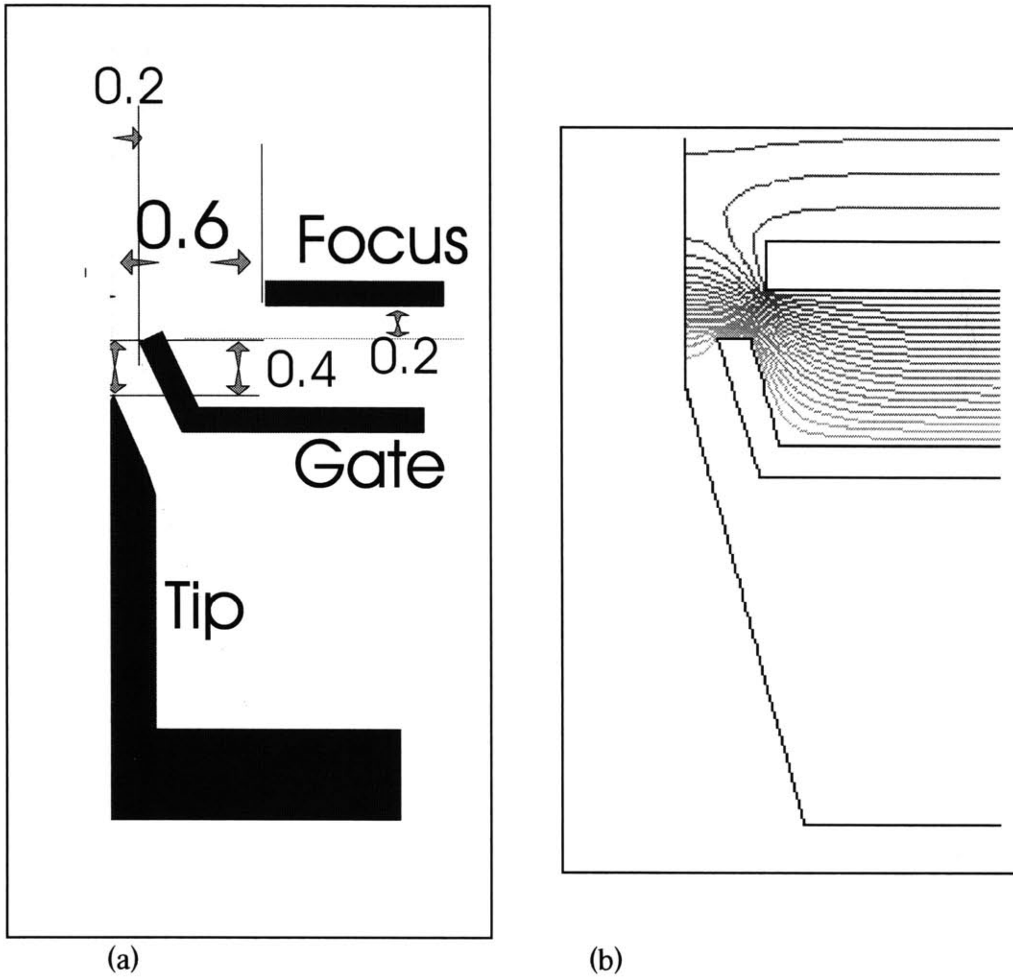


Figure 4-25. (a) The half of the schematic drawing of the structure. (Unit: micron) (b) Output drawing from Matlab.

Using the device dimensions shown in Figure 4-25 (a), the ratio of β_F / β_G we obtained from the Matlab simulation is 0.0119 ($\beta_F << \beta_G$), which is close to what we obtained from the fit. The ratio of β_F / β_G obtained from the data fit is 0.0097 for 1x1 array and 0.0156 for 10x10 array. This means that the gates shield the tips and the focus electrode has very little effect on the electron trajectories. Since the structures are not exactly the same for all the arrays, the results of the ratio of β_F / β_G vary but fairly stable. The details are included in Table 4-4.

	β_G (nm^{-1})	β_F (nm^{-1})	β_F/β_G
1x1 array	0.13716	0.00133	0.0097
5x5 array	0.09797	0.00052	0.0053
10x10 array	0.2601	0.00408	0.0156
Matlab simulation	0.06692	0.000797	0.0119

Table 4-4. Matlab simulation results and the fitting results for 1x1 array and 10x10 array.

Next, we used the same structure but varied the tip height, relative to the top of gate opening. The variations are (i) the tip is in plane of the gate and (ii) the tip is 100nm above of the gate. We examined the changes in the ratio of the β_F / β_G with the variation in tip height. Figure 4-26 shows these two relative positions. Note: the original tip height in Figure 4-25 (a) is 400nm below the top of the gate opening. The results indicate that the ratio of β_F / β_G is larger as the tip move from (1) below the gate aperture to (ii) being in the same plane as the gate aperture to (iii) finally being above the gate aperture. As the tip gets higher and closer to the focus electrode, the focus electrode has more effect on the device performance. Another result is that β_G decreases as the tip moves while β_F increases. Both results are consistent with the focus being closer to the tip and the gate further from the tip. Table 4-5 summarized the β_F and β_G for the three different tip positions in the device.

Tip and gate are in plane — Tip is 100nm above gate

(a) (b)

Figure 4-26. (a) The tip is in plane with the gate opening in the left diagram. (b) The tip is 100nm above the gate opening in the right diagram.

	β_G [nm^{-1}]	β_F [nm^{-1}]	β_F / β_G
400nm below the gate	0.0669	0.000797	0.01191
In plane with the gate	0.0427	0.02697	0.632
100nm above the gate	0.0273	0.03863	1.415

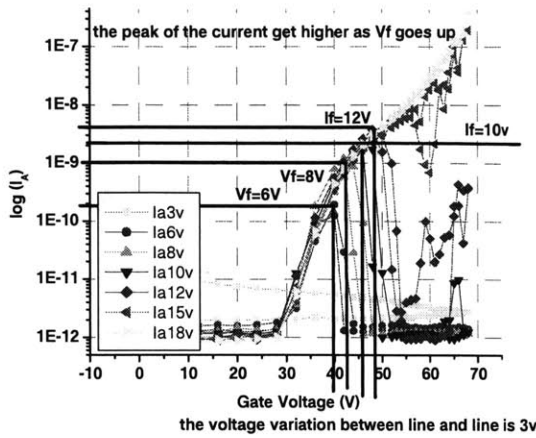
Table 4-5. Matlab simulation results for the tip (i) 400nm below the gate (ii) in plane with the gate (iii) 100nm above the gate.

Investigation of Space Charge at Focus below 15V

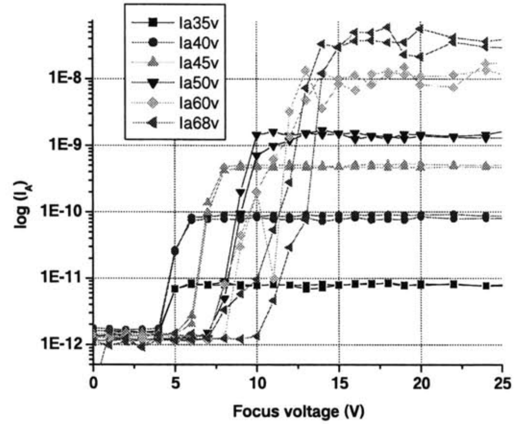
For all four-terminal measurements, we noticed an abrupt drop in the anode current when V_F is below ~15V. This effect results from lowering the focus bias only. There is a discrepancy between model and data in the range $V_F < 15V$, which means that we are observing a phenomenon that is not described by the generalized FN IV equation 4.1. Dr. J. Itoh, who first observed this effect in his devices, wrote [4.4]:

"In the region V_F <10V, on the other hand, I_A shows a quite different V_F dependence and abruptly decreases down to a few nanoamperes. In such conditions, electrons are not repelled as shown in Fig. 2C [i.e. back to the tip or back to the gate-LD] because V_F is still positive. A possible explanation is space charge effect caused by the retardation effect of the upper gate. In order to clarify the cause of the present I_A behavior, however, it is necessary to measure all the currents (I_E, I_G, and I_A) carefully as a function of V_F. Especially, the dependence of I_A and V_A is essentially important for consideration of space-charge effect."

L. Dvorson also saw the same result as Dr. J. Itoh [4.1]. In order to see what is going on when V_F is small, we varied gate voltages from 0V to 70V, with the focus voltage fixed between 3V and 18 V. Surprisingly, at a fixed small focus voltage (see Figure 4-27 (a) of the gate transfer characteristics) the anode current initially increased with gate voltage and then peaked. Further increase in gate voltage leads to a decrease in the anode current as the gate voltage increases (negative resistance region). This negative resistance region has not been reported in the literature before and this negative resistance region was duplicated for both upward and downward sweeps of gate voltage. This eliminates any suggestion of time dependence. In most instances the current then reaches a minimum at higher gate voltage and stays at minimum even at gate voltages as high as 70V. At focus voltages higher or equal to 10-12V, there is a minima and anode current increases with gate voltage beyond this current minima (second positive resistance region).



(a)



(b)

Figure 4-27.Four-terminal IV data for a 1x1 array. (a) I_A vs. I_G at fixed V_F (b) I_A vs. V_F at fixed V_G.

From the Figure 4-27 (a), we can see the higher the focus voltage, the higher the anode current peak. Also the peak of the anode current shifted to a higher gate voltage. For example, the peak of the anode current occurred at V_G=40V when the fixed V_F=6V, while the peak of the anode current occurred at V_G=49V, when the fixed V_F=12V. In Figure 4-27 (a), we could see the peak-shifting pattern. After breaking the threshold focus voltage (the threshold focus voltage to observe any anode currents is 6 V), we took measurements for every 2V change in V_F. The peak of the anode current shifted about 3V in V_G. Once focus voltage hit another threshold voltage, i.e. V_F > 15V, the anode current would increase with the gate voltage without a negative resistance region.

Figure 4-27 (b) shows the focus transfer characteristics of the same device. Here the gate voltage was fixed while the focus voltage was swept from 0 to 25V. Regardless what the gate voltage was, there was no anode current for focus voltage below 4V. This

is consistent with notion that all emitted electrons would be reflected back to the emitter for focus voltage less than the workfunction of the focus (in this case $\approx$ 4.05eV for poly-silicon).

One of Dr. J. Itoh's papers [4.4] reported electron trajectories with fixed gate voltage at 100V and with 5V, 0V, and -5V for the focus voltage, shown in Figure 4-28. He indicated that the focusing effect becomes stronger as the focus bias decreases toward the tip potential. At negative focus bias, almost all electrons are repelled by the focus electrode and finally return to the lower gate. We observed a similar result, the electrons were repelled by the focus electrode, but not exactly as he described. Our experimental results showed that the focus electrode repelled the electrons when the voltage difference between the gate voltage and the focus voltage is large enough not only when the focus voltage is biased negative as Dr. Itoh's simulation result suggests. So in Figure 4-27 (a), we can see that when the focus voltage is fixed, as long as the voltage difference between the focus and the gate has not reached a limit, the current would increase as the gate voltage increases. However, once the voltage difference between focus and the gate voltage reaches this limit (i.e. the voltage difference is too large enough), the force created by the focus electric field not only collimates electrons but also push electrons downward to either gate electrode or the tip. When electrons do not have enough kinetic energy to cancel this downward force, the electrons would be repelled and absorbed by the gates and the emitter. They do not reach the anode. This is the mechanism by which electrons are repelled by the focus voltage when the voltage difference between the gates is large enough.

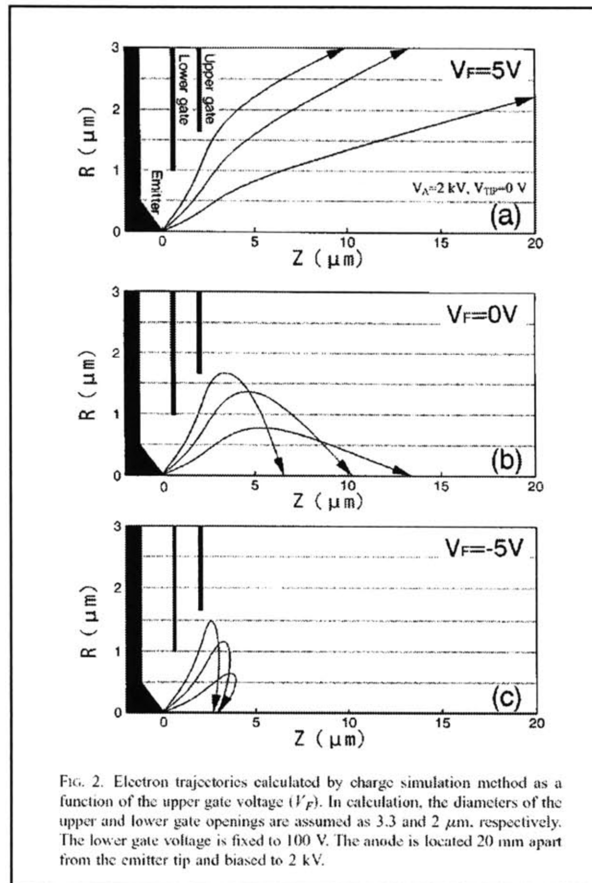


Figure 4-28. Dr. J. Itoh's simulation result in JVST B 13(5), 1995. [4.4]

Our explanation for this result is thus: the electric field generated by the gate electrode is large enough to cause field emission. However, the kinetic energy acquired by the electron in region of the gate field is not enough to surmount the region of the focus field and be collected by the anode. The electrons lose their velocities and are then decelerated by the focus field and reflected back to the cathode effectively retracing its trajectory but with a slight shift towards the gate. Thus, the electrons end up oscillating between the focus and the cathode and are gradually absorbed by both gates. Figure 4-28 presents an example of such oscillating trajectory.

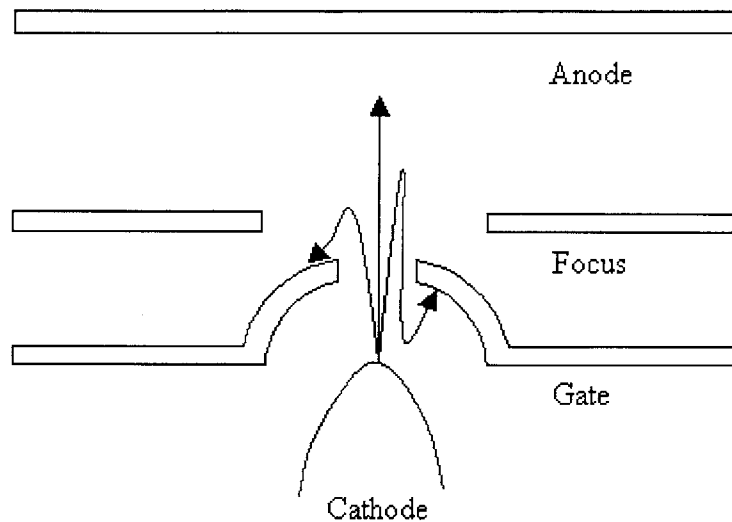
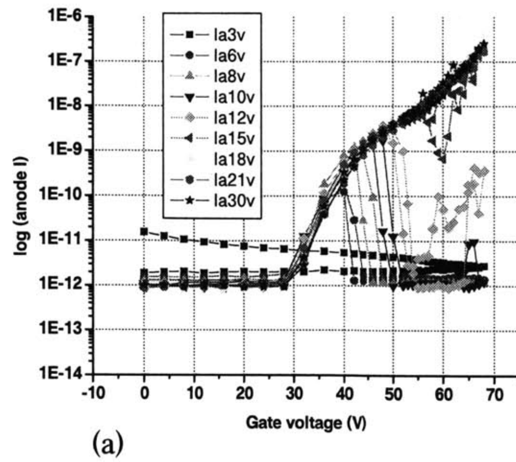


Figure 4-28. An example of oscillating trajectory.

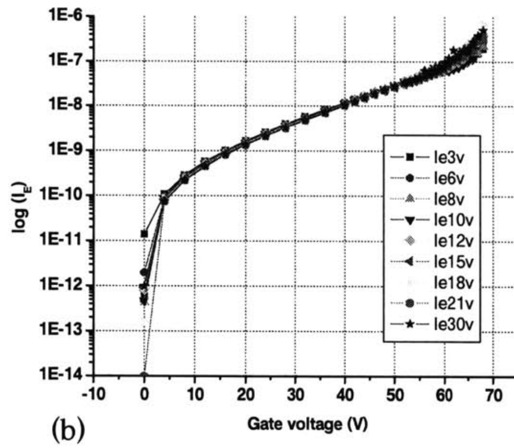
The data we took for I_G, I_F, I_E and I_A agree with this explanation. The current data were taken at the same time are shown in Figure 4-29. Figure 4-29 (a) shows all the anode currents with fixed focus voltage at 3V, 6V, 8V, 10V, 12V, 15V, 18V, 21V, and 30V. The anode currents overlap when the focus voltage is 18V or above. The emitter current also called the total emission current, increases as the gate voltage increases, shown in Figure 4-29 (b). The gate current is shown in Figure 4-29 (c). Note that all the plots for anode current, emitter current, and the gate current are in log scale and have almost the same magnitude (10^{-7}A) while the plots for the focus current is on a linear scale and the magnitude is much smaller than other currents. The focus currents are negative when the fixed focus voltage less than 18V, shown in Figure 4-29 (d) while the focus currents become positive when fixed focus voltage at 18 or above, shown in Figure 4-29 (e).

The focus currents are negative when the focus voltage is less than 15V and the negative focus current occurs in the "negative differential resistance" region of the anode current. . The focus currents become positive when the focus voltage is 15V or larger and the maximum values of the focus peak current are almost the same. This indicates

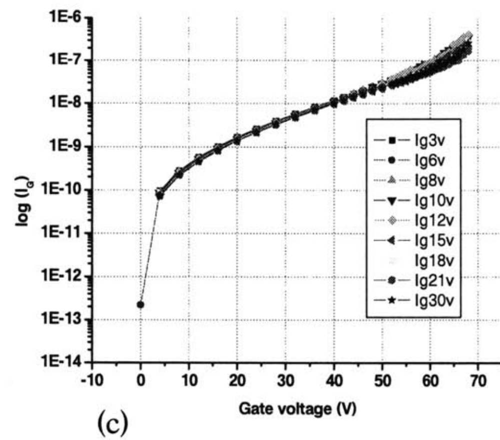
that when the voltage difference between focus and gate electrode is large and V_F is not large enough ($V_F < 15V$), the electrons from the emitter would be suppressed by the focus voltage and cannot reach the anode. The focus current observed could be attributed to leakage on the surface of the oxide. We also considered the possibility that the focus may be emitting electrons that are collected by that gate. The rather low values of the focus currents particularly in the voltage range over which negative differential resistance occurs do not support this assertion. When the gate voltage is larger enough and the fixed focus voltage is larger than 15V, the focus currents become positive. This indicates that the electrons are extracted from the tip and collected by the gate, focus, or anode depends on its spreading angle and the kinetic energy it has.



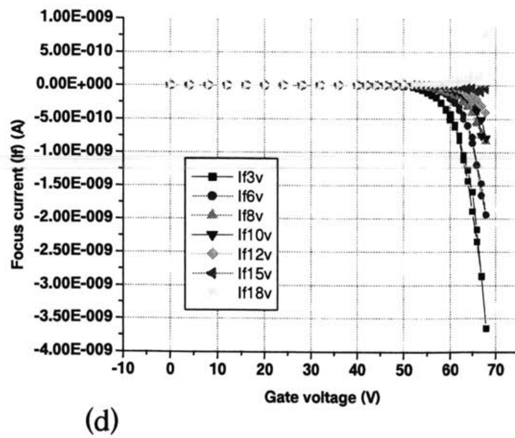
(a)



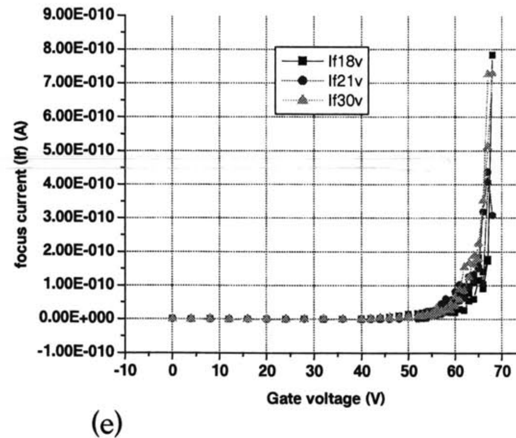
(b)



(c)



(d)



(e)

Figure 4-29. (a) Anode current (b) Emitter current (c) Gate current (d) Focus current with $V_F \leq 18V$ (e) Focus current with $V_F \geq 18V$ as a function of gate voltage for different values of focus voltage for 1x1 array.

4.5 Chapter Summary

This chapter discussed the IV characteristics of IFE-FEA for both three-terminal measurements and four-terminal measurements.

After describing the measurement setup, three-terminal measurements were taken to extract the FN coefficients. 1x1, 5x5, 10x10, 20x20, and 50x50 arrays were examined. To insure the accuracy measurements, IV sweeps on each array were repeated 21 times confirming the hypothesis that random fluctuations in emission current are due to adsorption and desorption of foreign particles on emitting surfaces. Multiple sweeps also insured the accuracy of the extraction of the FN parameters. The FN coefficients showed only little variation between up sweep, down sweep, and peak 11th for all the arrays. We also presented the temporal emission fluctuation and calculated the workfunction distribution that leads to the current fluctuation.

For four-terminal measurements, we saw the variation of the anode current with the gate voltage while the focus voltage is fixed, vice versa. Next, we extracted the value of β_G and β_F by using the FN IV equation generalized for the case of IFE-FEA equation (4.1):

$$I(V_{G,}V_G) = \alpha \times (4.27\times10^{-5}) \times (\beta_G V_G \times \beta_F V_F)^2 \exp\left[\frac{-55}{\beta_G V_G \times \beta_F V_F}\right] \quad (4.1)$$

β_G, β_F in nm^{-1}.

After fitting the data, the values of β_G are much larger than the values of β_F, which implies that the tips are below the gate and the focus has no effect on the electrons near the tip. Because of this structure, the anode current is independent on the focus electrode. The β_F / β_G ratio was verified by Matlab simulation. The analysis of four-terminal measurements agreed with the simulation results and the dimensions were selected based on SEMs. We also demonstrated in Matlab that ratio β_F/β_G is determined by whether the tip is in the plane of the gate opening, below the plane, or above the plane.

Finally, the anomalous reduction in emission current at low focus bias ($V_F < 15V$) was studied. This phenomenon has been reported in the literature but not adequately

explained. Following a critique of the existing hypothesis, we presented an alternative mechanism that we believe is responsible for this effect.

5. Optical Characterization of IFE-FEAs

5.1 Measurement setup for Image Acquisition

Figure 5-1 shows a schematic of the experimental setup. The setup is similar to the previous setup for IV characterization of IFE-FEA except for the addition of an image intensifier and a scientific digital camera.

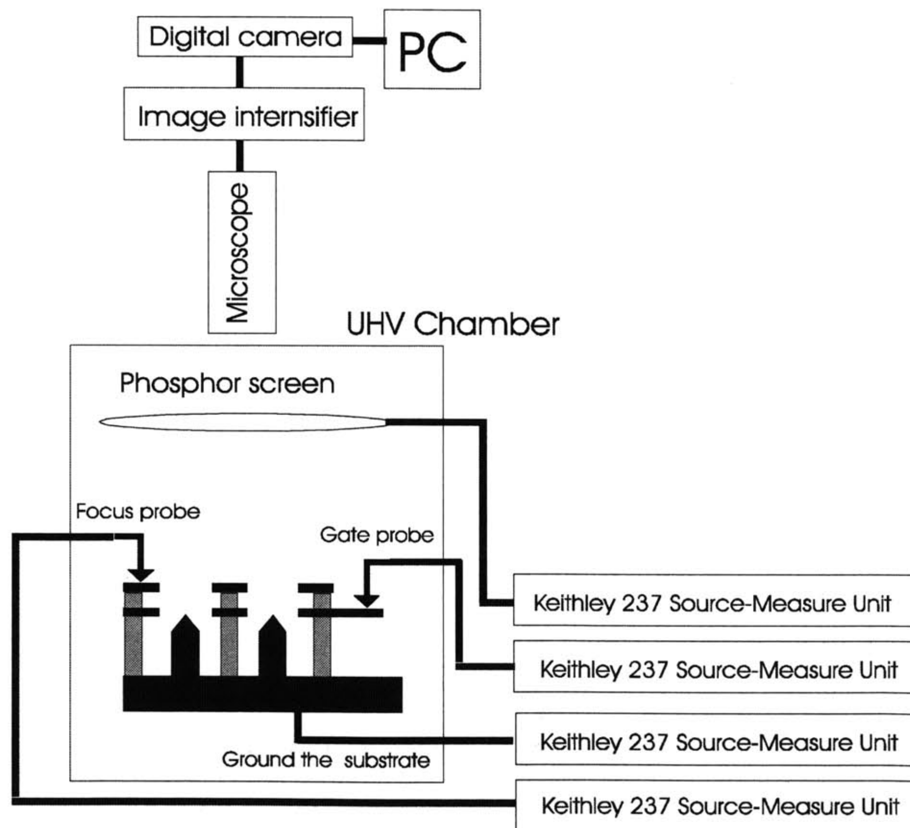


Figure 5-1. Schematic of the experimental setup.

This chapter will examine the most important aspect of IFE-FEA performance — reduction of spot size as a function of focus bias. In spot size measurements, instrumentation plays an important role. A simple high-sensitivity monochrome CCTV (closed-captioned TV) is not enough here since the spot produced on the phosphor anode by the electron beam is very dim and the anode is far away from the camera. Therefore, we added another two elements into our setup to help us capture better images. One is a scientific digital camera capable of timed exposure. It proved to be an excellent tool for spot size measurements. The other is an image intensifier (II) [Litton model M942], which produced very bright and clear images. However, the image intensifier measurement method posed several problems. One is that it saturated the camera at a wide range of light intensities making it impossible to distinguish a large and bright uniform spot from a small and bright spot, surrounded by dim halo.

This effect will be problematic when measuring the spot size. As focus bias is lowered, the emission current is lower and will not saturate the camera except in the immediate vicinity of the center of the spot. Since image intensifier is a night vision tool rather than a precise scientific instrument, it creates another problem with image intensifier measurement. The intensifier does not amplify the signals with the same factor for different pixels. In summary, the images captured by intensifier are good to determine the trends and general dependencies, but not extract quantitative results.

Our measurements used the scientific digital camera or both the scientific digital camera and the intensifier depending on the difficulty of the image capture. Most of the time, we used both instruments first to find the spot then switched to only the scientific digital camera if the situation allowed. The difficulty of the measurement here was that we needed to turn the gate voltage very high (about 70 V) to have enough emission current to activate the phosphor screen. However, some emitters broke down at very high gate voltage before we switched to the scientific digital camera only.

5.2 Collimation of the electron beam at different values of focus voltage

In this thesis, our objective is to observe how the smaller arrays behave hence we focused on the 1x1 array and the 5x5 array during the optical measurements. In this section, we examine the variation of spot size by varying focus voltage while the gate voltage is fixed. Theoretically, if we start with the same focus and gate voltages ($V_F=V_G$) and then lower the focus voltage while keeping the gate voltage fixed, we expect to observe a smaller spot size as the focus voltage is lowered. The reason is that there will be a negative charge included on the focus electrode, which will exert an electrostatic force on the electrons that pulls the electrons towards the cone axis thereby collimate the spreading electrons. Trajectory calculations are detailed in section 3.3.4 of L. Dvorson's Ph. D thesis [5.1].

Figure 5-2 shows the images of a 5x5 array taken with both the scientific digital camera and the image intensifier. The gate voltage is fixed at 70V while varying the focus voltage. We enlarged the original images 400 times. It may be argued that at V_F=0V, V_F=5V, and V_F=10V we started seeing the beginnings of focusing as the focus voltage is reduced; however, this also corresponds to the regime where there is a steep drop in anode current which is expected to have an effect on the brightness. The expected trend of the reduction of the spot size as the focus voltage is lowered was not observed. The diameter of the spot is between 40 to 50μm, which is about the same size as a 5x5 array. Note that the pitch of the emitter tip-to-tip distance is 10μm. Figure 5-3 shows the images of a 1x1 array taken with only the scientific digital camera when gate voltage is at 66V. Enlarging the images 1600 times is obviously beyond the camera resolution. We can clearly see that a number of pixels were activated by the current. However, it was not possible to observe any changes in the spot size with focus voltage. This agrees with the IV characteristics where we saw that $\beta_G >> \beta_F$. This means that the effect of the focus electrode is much lower than the effect of the gate electrode. The diameter of the spot size is about 9μm or less.

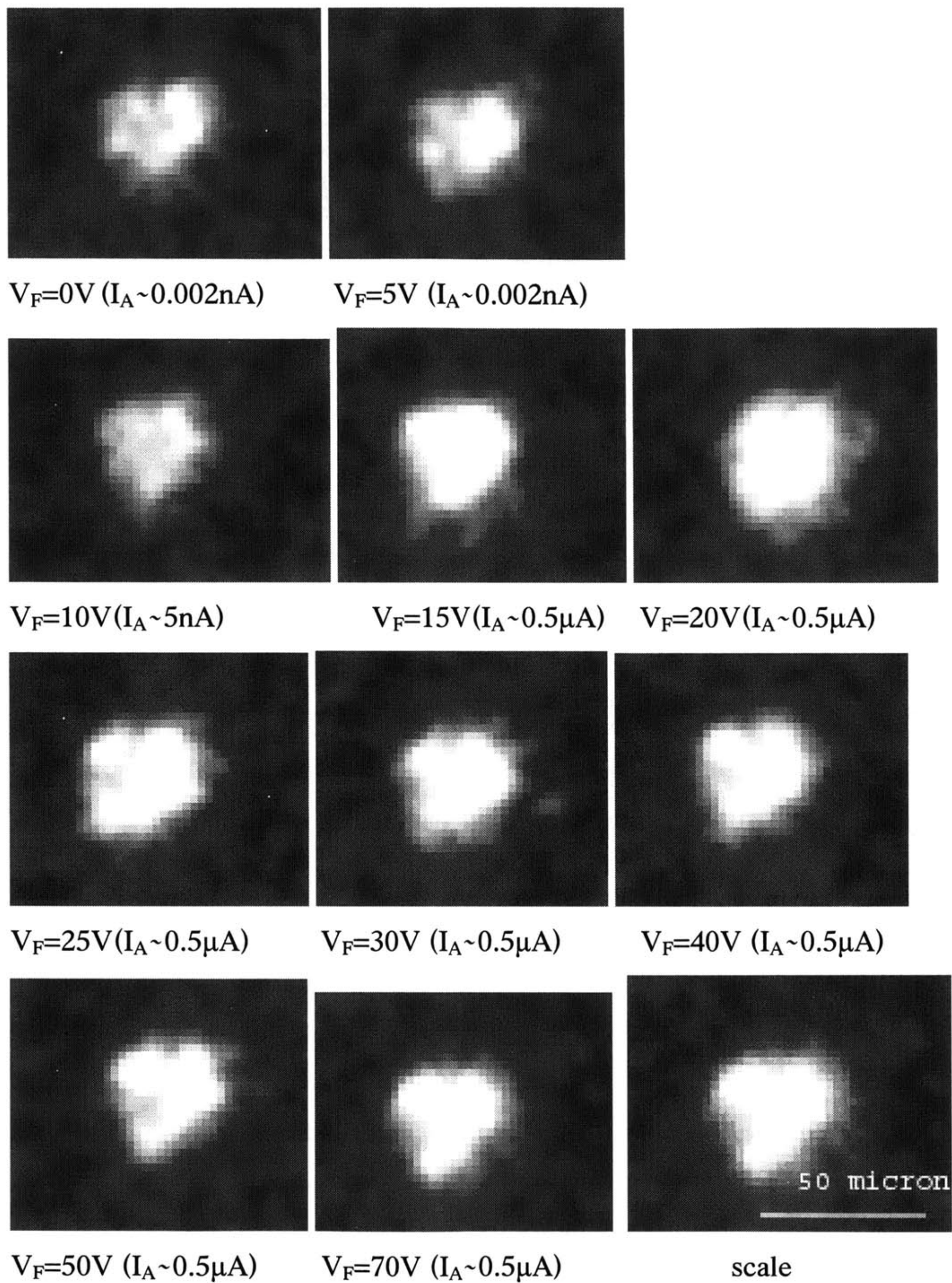
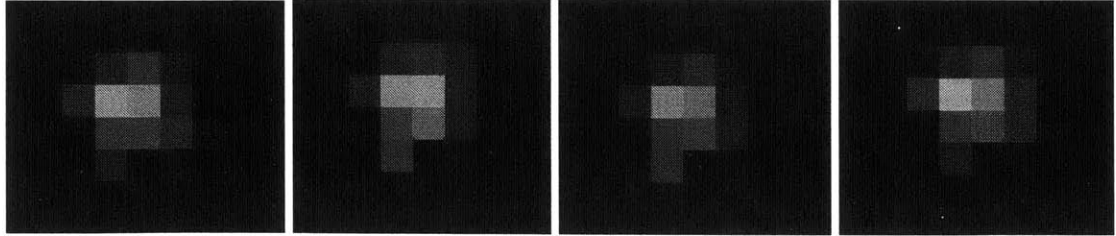
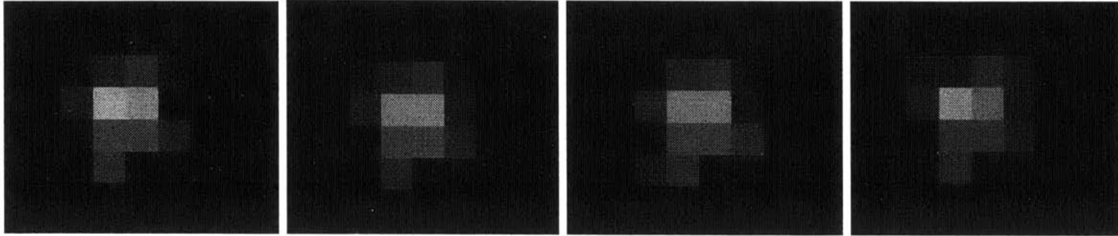


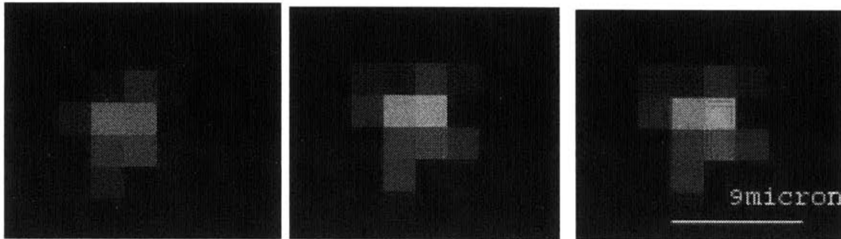
Figure 5-2. Variation of spot size with focus voltage at V_G=70v for 5x5 array. The photos were taken with both the scientific digital camera and the image intensifier.



V_F=0v (I_A~0.002nA) V_F=3v (I_A~0.002nA) V_F=10v (I_A~0.1nA) V_F=15v (I_A~0.2nA)



V_F=20v (I_A~0.4μA) V_F=25v (I_A~0.4μA) V_F=30v (I_A~0. 4μA) V_F=40v (I_A~0. 4μA)



V_F=50v (I_A~0. 4μA) V_F=66v (I_A~0. 4μA) scale

Figure 5-3. Variation of spot size with focus voltage at V_G=70v for 1x1 array. The photos were taken using only the scientific digital camera.

To analyze why the spots size did not change with focus voltage, we need to examine the relative positions of the tip, gate and focus electrode, and the gate and focus apertures. First, let us consider the relative position of tip and gate electrode. From the SEM, we know that tips are about 350-500 nm below the gate electrode. As we discussed in Chapter 2, when an electron is emitted at a nonzero angle, it acquires a certain horizontal velocity due to the roughly spherical field at the field emitter tip. The

electrons with emitted a large angle with respect to the cone axis would hit the gate electrode especially the tips that are much lower than the gate aperture. Since the gate aperture is much smaller than the focus aperture, the gate electrode would capture most of the electrons emitted at large angles with respect to the axis of the cone tip. The remaining electrons, which go through the gate aperture, are those that were emitted at a very narrow angle with respect to the cone axis. This is the reason why we obtained rather small spot sizes for both 5x5 array and 1x1 array. The mechanism described above is depicted in Figure 5-4. This result is consistent with the high gate current and low focus currents. The gate current is higher than the anode current while the focus current is negligible. The combined effect of the small aperture and a device structure with the tip below the aperture leads to significant interception of emitted electrons by the gate. The attractive force for electrons emitted at narrow angles with respect to the cone axis, from a positively biased gate, magnifies the interception of electrons by the gate further.

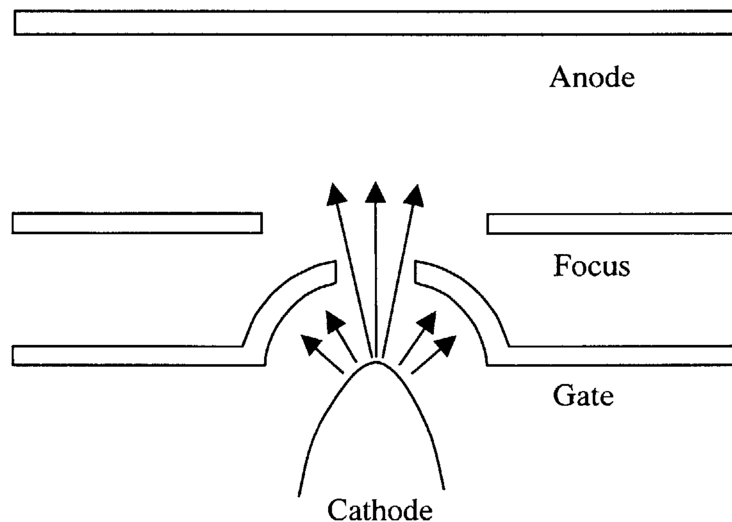


Figure 5-4. The electrons emitted at large angles with respect to the cone axis are captured by the gate leading to small spot size and high gate currents.

This result is consistent with both our IV characterization and the simulation results. The device structure in which tips are below the gate electrode would have much smaller value of focus field factor than the value of gate field factor ($\beta_F << \beta_G$). When $\beta_F << \beta_G$, the focus electrode would have less effect on the electrons. Analysis by L. Dvorson and experimental results for G/IP FEAs reported by Tang et al indicate that much lower voltages on the gates are required if tips are screened by the gate [5.1, 5.2, 5.3, 5.4]. This is also consistent with notion that the focus field effect has to be experienced by the tips very close to the gate aperture in order to have an effect on the trajectory.

5.3 Chapter Summary

In this chapter, we tried to demonstrate how lowering the focus bias reduces the diameter of the light spot produced on the phosphor screen by the electron beam. However, we did not observe any reduction in the spot size as the focus voltage was reduced. This result agrees with the IV characterization in Chapter 4 of this thesis in which $\beta_G >> \beta_F$. While the focus had little effect on the electron trajectory, the spot size was small and comparable to fully collimated electron beams. The device structure in which the tip is below the gate explains the results. Only electrons emitted at very shallow angles with respect to the cone axis are able to reach the anode. In contrast L. Dvorson's optical results, found a strong evidence of beam collimation by the focus electrode. He examined beam collimation at different values of gate voltage and observed that spot size changes only slowly until the focus voltage is reduced significantly below the gate voltage. The optimal focusing voltage was about ¼ of the gate voltage. His results were obtained for devices with different β_F / β_G ratio of 0.15. This may suggest that β_F / β_G cannot be lower than this in order to be able to focus. However, it cannot be much larger 0.5 if we want to maintain near constant current as focus voltage is varied.

6. Photoresist Exposure by IFE-FEAs

6.1 Measurement setup for photoresist exposure

The setup for phtotresist measurement is the same as IV characterization except we replaced the phosphor screen with a piece of the silicon wafer coated with photoresist. This chapter will exam the final goal of this project — use IFE-FEA to expose the photoresist. This experiment was motivated by e-beam lithography. Here, IFE-FEA will be the electron source and direct write of patterns on silicon wafers [6.1,6.2, 6.3, 6.4, 6.5].

6.2 Materials selections

Resist

PMMA positive resist is suitable for our photoresist experiment since PMMA positive resists are based on special grades of polymethyl methacrylate designed to provide high contrast, high resolution for e-beam and other lithographic process. Also it has excellent adhesion to most substrates. Standard products from MicroChem include 495,000 and 950,000 molecular weights (MW) in a wide range of film thicknesses formulated in chlorobenzene, or a safer solvent anisole.

In general, the higher the molecular weight, the slower it will dissolve in a solvent developer. After exposure (molecular chain scission), the develop contrast between the exposed and unexposed regions of the film becomes higher as MW increases. This is the reason 950 PMMA with 4% anisole was chosen, which has 950,000 molecular weights (MW) instead of 495 PMMA, which has 495,000 molecular weights. Also, in most of the cases PMMA formulated in anisole and chlorobenzene will have virtually identical

performance characteristics. In our case, it will not make any difference and for the environmental concerns, anisole would be better.

Developer

The developer formulations from MicroChem are blends of MIBK (Methyl Isobutyl Ketone) and IPA. MIBK is the solvent and active ingredient, which controls the solubility and swelling of the resist, while IPA is the alcohol. Formulations containing higher amounts of solvent (MIBK) are more aggressive and offer higher throughput, while formulations containing higher amounts of non-solvent (IPA) are less aggressive and designed for higher resolution applications. The developer we used consists of MIBK and IPA, in the ratio of 1:1, which would give us high resolution and high throughput, according to the chart provided by MicroChem [6.6].

6.3 Photoresist exposure result

Coating procedure

The coating process for PMMA is similar to the regular photoresist. The steps are: spin, pre-bake, exposure, develop and postbake. First, we spun the PMMA at 3000 rpm for 45 seconds and then we pre baked the wafer at 170 ºC for 30 minutes in convection oven. A 0.2µm thick of PMMA layer was deposited and examined by a profilometer as shown in Figure 6-1.

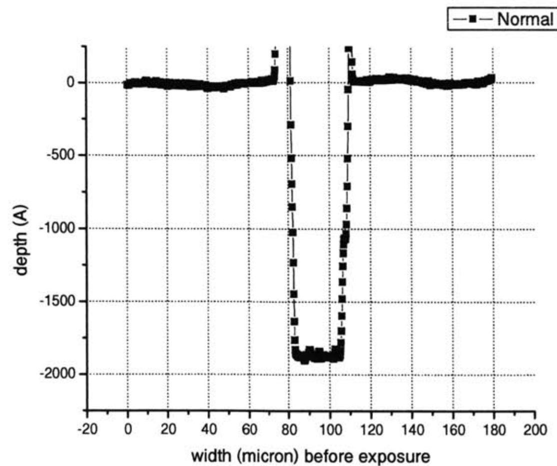


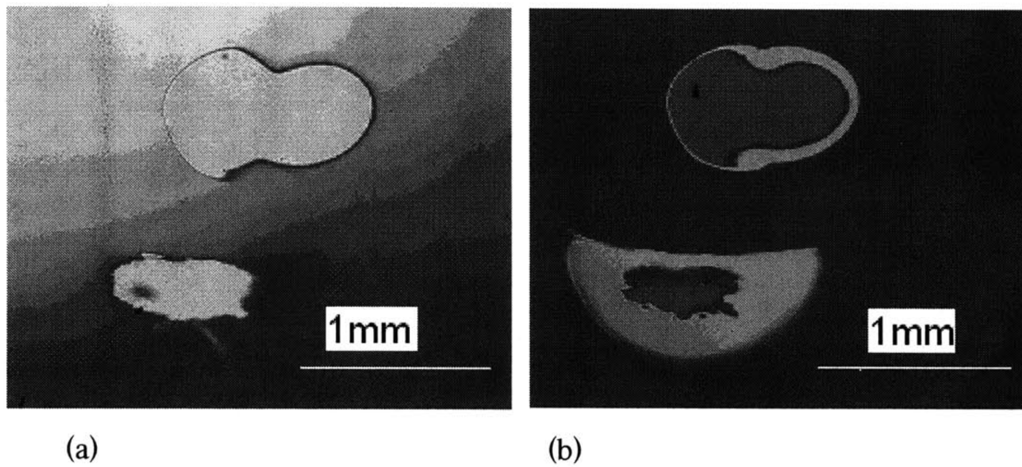
Figure 6-1. A 0.2μm thick PMMA profile.

Exposure and Results

PMMA can be exposed with an e-beam at a dose 50~500 $\mu C/cm^2$ depending on radiation source/equipment and developer used. J. Itoh's group used 5kV anode voltage to exposed 1μm thick of the PMMA with an exposure dose of 50nC (5nA for 10s) [6.7, 6.8]. However, this would not penetrate through to the bottom of the resist. After converting the units, a does of 0.01μAs was needed for an area of $100\mu m^2$. An array of 5x5 would give us 0.01~0.08 μA when both gate e and focus voltages are around 45V and about 0.1~0.6 μA with both gate and focus voltages are around 55V. The anode voltage was set to be 3kV or 4.5kV to provide enough energy for electrons to penetrate the 0.2μm thick of PMMA layer [6.9].

We exposed the PMMA with different doses. We first used 3kV for anode voltage and exposed the PMMA with V_G=V_F=45V and V_G=V_F=55V for approximately for 1 second. Later, the anode voltage was set at 4.5kV and the PMMA was exposed with V_G=V_F=45V and V_G=V_F=55V for approximately for 1 second. The resist was developed by a mixture of MIBK and IPA (1:1). Figures 6-2 (a) & (b) show the area (two dots in each figure) exposed by the 5x5 array. These two dots indicate that not all the tips were

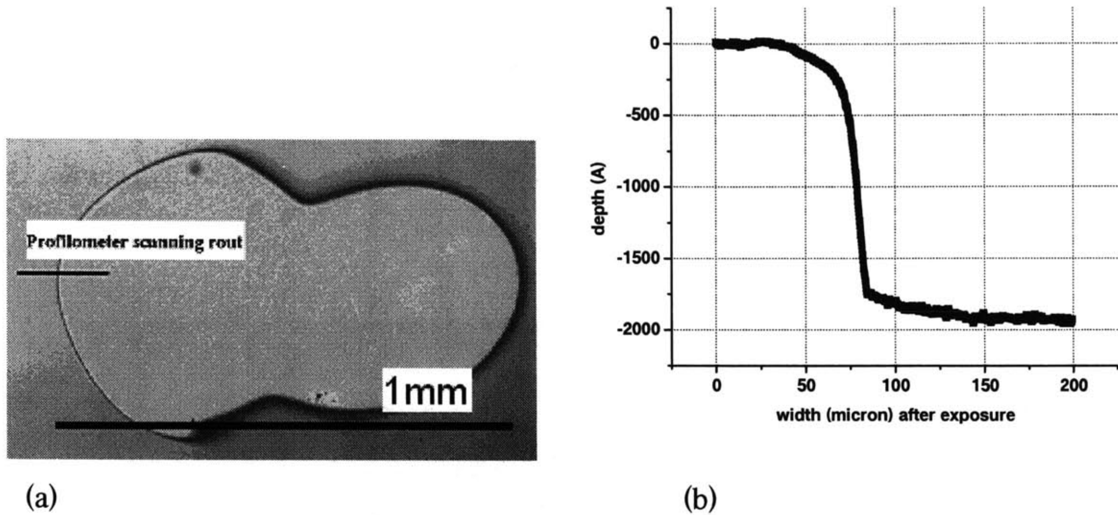
working in this particular 5x5 array. Only 2 areas in this 5x5 array were working. (Note: these two dots in each Figure were generated at the same time using the same array). Due to the different doses used, we obtained different results. When the PMMA was exposed with $V_G=V_F=45V$ and the anode voltage was 3kV, the resist had gave a better result, shown in Figure 6-2 (a). In comparison to when the PMMA was exposed with $V_G=V_F=55V$ and with the anode voltage equal to 4.5kV, the resist was overexposed. The center of the two dots were polymerized and could not be developed away, shown in Figure 6-2 (b).



(a) (b)

Figure 6-2. (a) The exposure of PMMA with $V_G=V_F=45V$ and the anode voltage was 3kV. (b) The exposure of PMMA with $V_G=V_F=55V$ and the anode voltage was 4.5kV.

We used the profilometer to study the profile of the edge of the dot, which was exposed with anode voltage at 3kV and had gate and focus voltages set at 45V. Figure 6-2 (a) shows the dot under the microscope with the indication of where we scanned the profile. Figure 6-2 (b) shows the profile of the resist across of the edge of the dot. We can see that the PMMA region, which was exposed to the electrons, was completely removed as indicated by the depth of the resist, which is 0.2μm.



(a) (b)

Figure 6-2. (a) The exposed dot area. (b) The depth profile of the edge of the dot.

6.4 Chapter Summary

In this chapter, we introduced the FEA as an e-beam source to expose the positive PMMA resist. We reported how the materials were selected and calculated the expected dose range. We showed the exposure results for different exposure doses. The resist polymerizes if the dose is too high. A clear dot area where the resist fully developed away was presented and confirmed with a profilometer.

7. Thesis Summary and Suggestions for Future Work

7.1 Thesis Summary

This thesis used a stacked double-gated field emitter arrays to produce collimated electron beams to improve the resolution of high voltage field emission displays and other related application. A novel process for fabricating a stacked double-gated field emitter arrays was presented and the device performance was characterized electrically, optically and with PMMA.

A completed fabrication process of the double-gated FEA was described. The process is self-aligned and relies on deposition, planarization via chemical-mechanical polishing (CMP), and etchback of oxide layers. The final dimension of the gate aperture radius was 0.3μm and the focus aperture diameter was 0.6μm. These apertures are smaller than any that has been reported before.

In the three terminal measurements, per tip emission currents were about 40nA at 60V. After extracting the FN coefficients, we obtained b_{FN} is about 480+/-10 from the slope and a_{FN} is about 18+/-0.5 from the intercept of the y-axis, which suggests there is a high degree of tip-to-tip uniformity. The value of the tip radius of curvature (ROC) is calculated with Ball-in-a-sphere model (BPM), which turned out to be around 8.3~8.9nm.

In the four terminal measurements, the emission currents were largely independent of the focus voltage, which is most desirable. The gate field factor β_G and the focus field factor β_F were extracted. β_G is much larger than β_F. Matlab simulations using device dimensions provided by SEM pictures were performed. The simulations agree with the fit (i.e. $\beta_F \ll \beta_G$). We also simulated two other cases using the same

dimension except the relative height of the tip with respect to the gate opening was varied: the tip is in-plane with the gate opening and the tip is above the gate opening. The simulations showed that the tips that are below the gate aperture are shielded by the gate and have lower focus field factor.

Images were taken with the gate voltage fixed while the focus voltage was varied. While the spot size was very small, the focus had very little effect on the spot size confirming that the gate shielded the tip from the focus.

The most significant result of this work is the exposure the PMMA positive resist by electrons extracted from a 5 x 5 field emitter array. When the dose is too high, the PMMA resist polymerizes. With the optimal dose, the PMMA resist is fully exposed and developed. The result was confirmed by an edge profilometer.

7.2 Suggestions Future work

The first suggestion is to increase the breakdown voltage between the gate layer and the focus layer. The tip could be made taller by about 1μm to allow thicker insulators (2μm of oxide in each insulating layer would be excellent).

An extension of the PMMA exposure work is to study the size of the exposed area as a function of focus voltage (with fixed gate voltage). Another experiment is the exposure of PMMA using the 1x1 array.

The emitter is potentially an electron source for some sensors or e-beam lithography. A much better control of the electron emission is needed. Therefore, combining a double-gated FEA with MOSFET is a good method to control the electron emission.

Appendix A. Process Flow of the Fabrication of Silicon Double-gated Silicon FEA

Starting Wafers: 6" n-type Silicon prime wafers, 1-10 Ωcm resistivity, <100> orientation

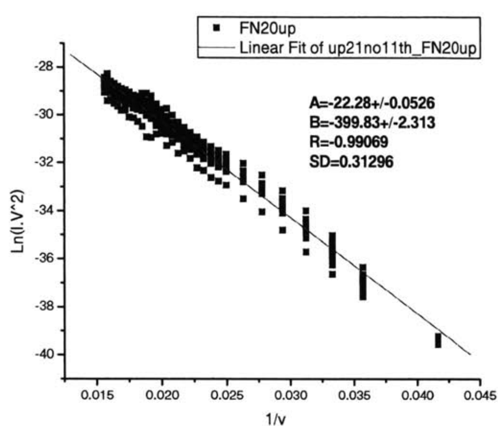
Process flow:

Step#	Lab	Machine	Recipe	Description
1	ICL	RCA	Standard RCA	
2	ICL	Tube5C	1000ºC, 126 min	Grow 250nm of SiO_2 on the Si substrate
3	ICL	Coater	1um	Coat 1um positive PR
4	ICL	Coater	90ºC, 60sec	Pre bake
5	ICL	i-stepper	140ms	Exposure, Mask #1: Pit pattern
6	ICL	developer	~15 s	Develop, rinse + dry
7	ICL	coater	30sec	Post bake
8	ICL	Asher	Descum	Remove residual resist
9	ICL	Centura	C_2F_6: 25sccm pressure: 3mtorr	Etch SiO_2 for 0.66μm
10	ICL	Lam490	300 mtorr, 130 watt, 190 sccm of SF_6 and 10 sccm of O_2	Isotropic etch Si to form 1μm tips
11	ICL	Lam490	400 mtorr, 200 watt, 134 sccm of H_2 and 96 sccm of Cl_2	Anisotropic etch Si for 4μm for the extension
12	ICL	Asher	Descum	Strip PR/clean
13	ICL	oxide	7:1 BOE	Etch the oxide cap in BOE
14	ICL	RCA	Standard RCA	
15	ICL	Tube5C	950ºC, 15hrs, 100% dry O_2	Dry Si oxidation for 0.2μm to sharpen the tip
16	ICL	Tube6C (LTO)	450ºC, 20min	Deposit 2μm SiO_2
17	ICL	Tube6C (LTO)	450ºC, 20min	Deposit 2μm SiO_2
18	ICL	CMP	Table speed 15 rpm, quill speed 15 rpm, down force 5 psi, slurry 150 ml/min, back pressure 4 psi, polish time 564s	To polish the SiO_2 bump
19	ICL	Post CMP clean		
20	ICL	RCA	Standard RCA	

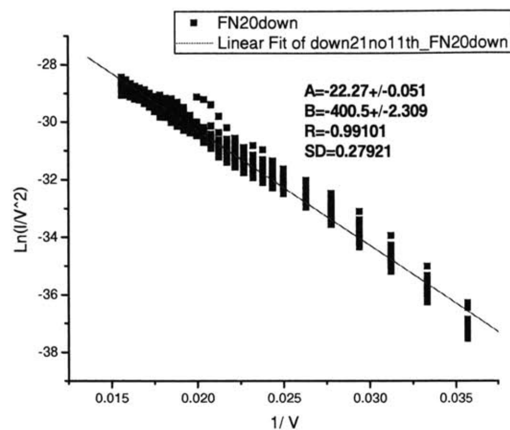
21	ICL	Tub5C	O_2	Densify the SiO_2 by O_2 to increase the breakdown voltage
22	ICL	Oxide	7:1 BOE	Etch SiO2 2μm
23	ICL	RCA	Standard RCA	
24	ICL	Tube6C (LTO)	450ºC, 6min	Dry Si oxidation for 0.25μm to form the gap between tips and gates
25	ICL	Tub6A		Deposit poly-Si for 0.3μm to form gates
26	ICL	Implant	P+ 3E15 at 100keV	Doped phosphorous on Si
27	ICL	Post Implant clean		
28	ICL	Lam490B	400 mtorr, 200 watt, 134 sccm of H_2 and 96 sccm of Cl_2	Etch poly Si, which protrudes the flat oxide surface, to open the second gate
29	ICL	Concept1		Deposit (0.285um) SiO2 to separate the first and second gate
30	TRL	RCA	Standard RCA	
31	TRL	TubB4		Deposit (0.35um) poly-Si to make the second gate
32	ICL	Implant	P+ 3E15 at 100keV	Doped phosphorous on Si
33	ICL	Post implant clean		
34	ICL	Concept1		Deposit (1.5um) SiO2 for submerge the tips
35	ICL	CMP	Table speed 15 rpm, quill speed 15 rpm, down force 5 psi, slurry 150 ml/min, back pressure 4 psi, polish time 280s	Planarize the oxide surface
	ICL	Post CMP clean		
36	ICL	Oxide	7:1 BOE	Etch the oxide until see the bumps of the second gate
37	ICL	LAM490B	400 mtorr, 200 watt, 134 sccm of H_2 and 96 sccm of Cl_2	Etch poly Si, which protrudes the flat oxide surface, to open the second gate
38	ICL	Coater track 1	Re bake 95ºC, 60sec	Coat 1um positive P.R
39	ICL	i-stepper	Soft bake 115ºC, 60sec	Expose Mask #2 for contact patterning for first and second gate (with two contact pads)
40	ICL	Coater track 2	Post bake 130ºC, 60sec	
41	ICL	Lam490B	400 mtorr, 200 watt, 134 sccm of H_2 and 96 sccm of Cl_2	Etch poly Si of the second gate (with two contact pads)
42	ICL	AME500	Main etch: pressure of 200mtorr and Cl_2	Etch the oxide between the first and second gate

			of 20sccm and HBR of 20sccm Overetch: pressure of 100mtoor and HBr of 40sccm	
43	ICL	Lam490B	400 mtorr, 200 watt, 134 sccm of H_2 and 96 sccm of Cl_2	Etch poly Si of the first gate (with two contact pads)
44	ICL	Asher		Take off remaining P.R.
45	ICL	Coater track 1	Re bake 95ºC, 60sec	Coat 1um positive P.R
46	ICL	i-stepper	Soft bake 115ºC, 60sec	Expose Mask #3 for contact patterning to etch away one of the contact pads on the second gate
47	ICL	Coater track 1	Post bake 130ºC, 60sec	
48	ICL	AME500	Main etch: pressure of 200mtorr and Cl_2 of 20sccm and HBR of 20sccm Overetch: pressure of 100mtoor and HBr of 40sccm	Etch away one of the poly Si contact pads of the second gate
49	ICL	Oxide	7:1 BOE	Etch the oxide between the first and second gate so one of the poly Si contact pads of the first gate can be seen.
50	TRL	RCA	Standard RCA	
51	TRL	Tube B3	900° C for 30 minutes with N_2	Anneal (RTA)
52	ICL	oxide	7:1 BOE	Extensive SiO2 etch to etch the oxide all the way down to the substrate

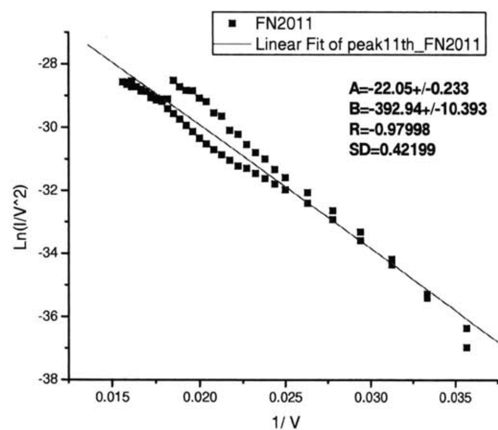
Appendix B. FN coefficients of array 20x20 and array 50x50



(a)

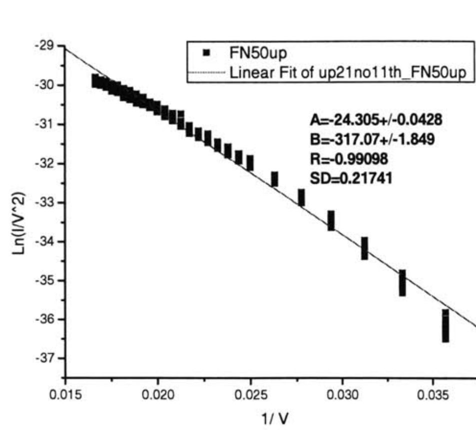


(b)

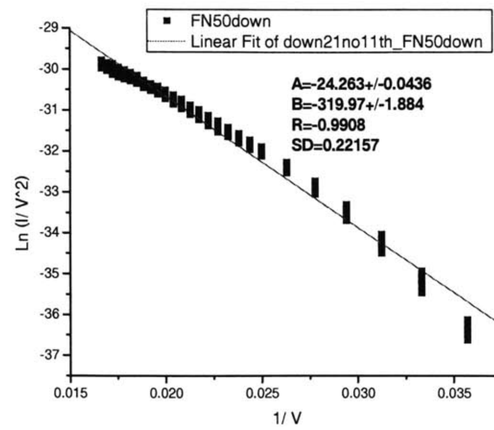


(c)

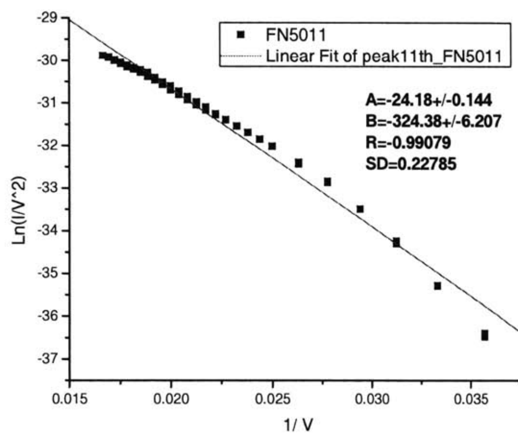
Figure B-1. FN coefficients of 20x20 tip array. (a)up sweep (b)down sweep (c)#11 peak sweep



(a)



(b)



(c)

Figure B-1. FN coefficients of 50x50 tip array. (a)up sweep (b)down sweep (c)#11 peak sweep

Appendix C. Matlab code to compute the β_F and β_G.

```
% Field Emitter Tip Simulation
% Guobin Sha
% modified from David Pflug
clear
% all in units of nm
apr=200;      % gate aperture outside tip nm
aprfocus=600; %aperture of focus gate
roc=10;       % tip radius of curvature
hei=2117;      % gate height , i.e. oxide thickness
hei2=647;     % height of verical gate
gap=400;          % difference of tip height and the top of vertical gate. postive if tip is
below, negative if tip is above.
gap2=600; % difference of tip height and bottom of focus gate.
thi=300;      % focus gate thickness
thi2=200;     % vertical gate thickness, can be changed, don't have to be same as focus
gate thickness anymore
the=75;       % cone base angle in degrees

%the resuling beta are in voltage/cm
% the resulting graph is beta vs. angel of the tip.

% don't change anything below, don't change anything in coneleo2model
htip=hei+thi+hei2; % tip height
apr2=(htip -hei)/tan(the * pi/180.0)+apr;
apr3=(htip-thi-hei) /tan(the *pi/180.0)+apr;
htip=htip-gap;
mr=2;         % mesh refinement, 0-3, 0 means coarse, 3 means very fine

wf=4.05;
Va=0;
Vg=1;
[p,e,t,ua,pg,eg,tg,ug]= coneleo2model(aprfocus, gap2,
apr3,apr2,apr,roc,hei2,hei,thi2,thi,the,htip,mr);
u=ug;

[ux,uy]=pdegrad(p,t,u);
uxn=pdeprtni(p,t,ux);
uyn=pdeprtni(p,t,uy);

sc=8; %segment of circle
theta=0:the*pi/(180*sc):the*pi/180;
x0=sin(theta)*roc;  %starting point of trajectory
y0=cos(theta)*roc+(htip-roc);
for i=1:size(uxn)
```

```
uen(i)=sqrt(uxn(i)*uxn(i)+uyn(i)*uyn(i));
end

for i=1:size(theta')
   %pnt=[x0(i),y0(i)];
   %[Ex(i),Ey(i)]=eatpt(pnt,p,t,ux,uy);
   Ecircle(i)=tri2grid(p,t,uen,x0(i),y0(i));
end
plot(theta,Ecircle);

sprintf('beta gate=%f', Ecircle(1)*10^7)

va=1; vg=0;
u=ua;

[ux,uy]=pdegrad(p,t,u);
uxn=pdeprtni(p,t,ux);
uyn=pdeprtni(p,t,uy);

sc=8; %segment of circle
theta=0:the*pi/(180*sc):the*pi/180;
x0=sin(theta)*roc;  %starting point of trajectory
y0=cos(theta)*roc+(htip-roc);
for i=1:size(uxn)
uen(i)=sqrt(uxn(i)*uxn(i)+uyn(i)*uyn(i));
end
for i=1:size(theta')
   %pnt=[x0(i),y0(i)];
   %[Ex(i),Ey(i)]=eatpt(pnt,p,t,ux,uy);
   Ecircle2(i)=tri2grid(p,t,uen,x0(i),y0(i));

end
plot(theta,Ecircle2);
sprintf('beta focusing gate=%f', Ecircle2(1)*10^7)
end
end
```

Appendix D. Field Factors for Double-Gated FEA

We constructed a finite element model (FEM) of the double-gated FEA in Matlab to determine the gate field factor and the focus field factors as a function of tip radius. Our approach is similar to the one used by M. Ding in [4.3] with the difference that our device has an additional electrode — the focus. Figure D.1 and D.2 are plots of β_G and β_F as a function of the tip radius indicating that $\beta_G >> \beta_F$ expected for our device geometry. For the extraction of FN coefficient from three-terminal IV characteristics in the double-gated FEA, the focus voltage was made equal to the gate voltage. The effective field factor β_{eff} for this situation is given by

$$\beta_{eff} V_G = \beta_G V_G + \beta_F V_G = (\beta_F + \beta_G) V_G$$
$$\beta_{eff} = \beta_G + \beta_F$$

Figure D.3 plots the field factor for different models that could potentially be used for tip radius extraction. The simplest model is the ball-in-a-sphere model while the Ding model assumes a three terminal device with a gate aperture of 1μm and our model assumes a four terminal device in which the focus and gate voltages are equal. Our model uses device dimensions extracted from SEMs. We used the plot of the effective field factor, $\beta_{eff} = \beta_G + \beta_F$, to extract the tip radius in Chapter 4.

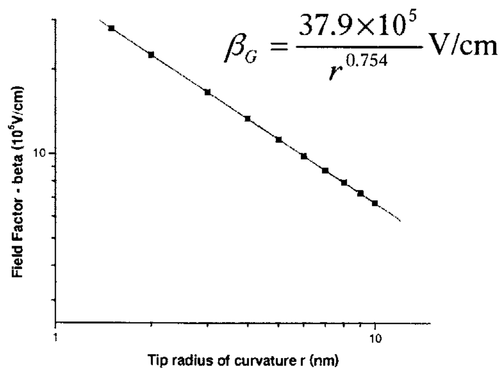


Figure D.1. β_G as a function of tip radius.

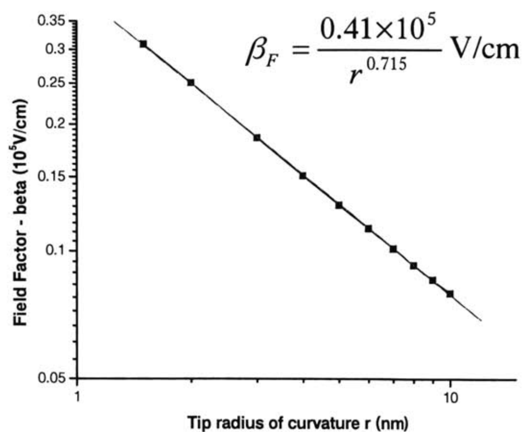


Figure D.2. β_F as a function of tip radius.

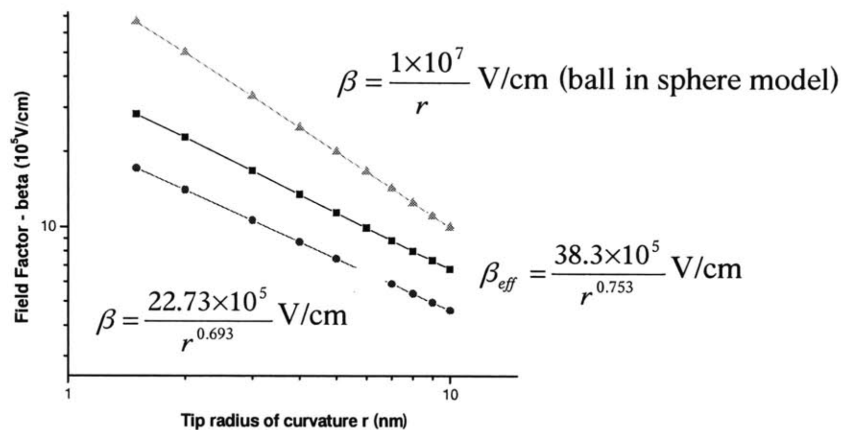


Figure D.3. The field factor as a function of tip radius for three different models. (i) $\beta = \frac{1\times10^7}{r}$ V/cm is ball in sphere model (ii) $\beta_{eff} = \frac{38.3\times10^5}{r^{0.753}}$ V/cm is based on our four-terminal model while V_G=V_F (iii) $\beta = \frac{22.73\times10^5}{r^{0.693}}$ is based on M. Ding's three-terminal model.

References

Chapter 1

[1.1] C.A. Spindt, C.E. Holland, I. Brodie, J.B. Mooney, and E.R. Westerberg, "Field-emitter Arrays Applied to Vacuum Florescent Display," IEEE Transactions on Electron Devices, January, 1989, v. 36, no. 1, p.225-227

[1.2] P. Vandaine, R. Meyer, "Microtips Fluorescent Display," IEEE IEDM, 1991, p8.1.1-8.14

[1.3] W.B. Choi, D.S. Chung, J.H. Kang, H.Y. Kim, Y.W. Jin, I.T. Han, Y.H. Lee, J.E. Jung, N.S. Lee, G.S. Park, and J.M. Kim, "Fully sealed, high-brightness carbon-nanotube field-emission display," Applied Physics Letters, v. 75, no. 20, p3129-3131

[1.4] W.B. Choi, Y.W. jin, H.Y. Kim, S.J. Lee, M.J. Yun, J.H. Kang, Y.S. Choi, N.S. Park, N.S. Lee, and J.M. Kim, "Electrophoresis deposition of carbon nanotubes for triode-type field emission display," Applied Physics Letters, v. 78, no. 11, p1547-1459

[1.5] H. Schafer, P. Schaffer, S. Kleindiek, K.H. Herrmann, "Advances in the electron optical design of a multi e-beam comb probe printer," Microelectronic Engineering, v 11, n 1-4, April 1990, p 355-8

[1.6] M.J. Paulus, C.E. Thomas, M.L. Simpson, J.A. Moore, L.R. Baylor, D.H. Lowndes, D.B. Geohegan, G.E. Jr. Jeellison, V.I. Merkulov, A.A. Puretzky, E. Voelkl, J. Walter, F.W. Barber, "Addressable amorphous diamond field emission array for E-beam lithography," Annual Device Research Conference Digest, 1998, p 122-123

[1.7] A.H.V. Van Vee, B.J. Kampherbeek, M.J. Wieland, P. Kruit, "Field emission photocathode array for high throughput lithography," IVMC 2001. Proceedings of the 14th International, 12-16 Aug. 2001, p127 – 128

[1.8] N.L. Rupesinghe, M. Chhowalla, K.B.K. Teo, G.A.J. Amaratunga, "Field emission vacuum power switch using vertically aligned carbon nanotubes," IVMC 2001. Proceedings of the 14th International Vacuum Microelectronics Conference, 2001, p 3-4

[1.9] S. T. Lam, "Field emission information storage technology," IVMC 2001. Proceedings of the 14th International Vacuum Microelectronics Conference, 2001, p 135-6

[1.10] C.A. Spindt, C.E. Holland, A. Rosengreen, , I. Brodie, "Field Emitter Array Development for Gigahertz Operation," IEDM,1992, p 14.1.1-14.1.3

[1.11] C.A. Spindt, C.E. Holland, A. Rosengreen, , I. Brodie, "Field-emitter-array development for microwave applications," IEDM,1995, p 16.1.1-16.1.4

[1.12] C.A. Spindt, C.E. Holland, P.R. Schwoebel, I. Brodie, "Maximizing field-emitter-array transconductance for microwave applications," IVMC '95. Eighth International Vacuum Microelectronics Conference. Technical Digest, 1995, p 137

[1.13] P. Vincent, L. Gangloff, E. Minoux, G. Pirio, J.P. Schnell, D. Pribat, P. Legagneux, K.B.K. Teo, R. Lacerda, M. Chhowalla, D.G. Hasko, H. Ahmen, G.A.J. Amaratunga, O. Groening, V. Semet, V.T. Binh, W.H. Bruenger, J. Eichholz, H. Hanssen, D. Friedrich, M. Castignolles, A. Loiscau, "Carbon nanotubes/nanofibers for microwave amplifiers and parallel e-beam lithography," Vacuum Microelectronics Conference, 2003. Technical Digest of the 16th International, July 7-11, 2003 P73 - 74

[1.14] D. Temple, "Recent Progress in Field Emitter Array Development for High performance Applications," Material Science and Engineering, Vol. R24, pp.185-239, 1999

[1.15] H. F. Gray, "state-of-the-art of field emission displays," Int. Soc. Opt. Eng. Proceedings of SPIE, vol. 3057, pp. 214-224, 1997

[1.16] C. Curtin, "The field emission display: a new flat panel technology," Conference Record of the 1991 International Display Research Conference. IEEE. 1991, pp.12-15. New York, NY, USA

[1.17] L. Pellizzari, "From Vacuum fluorescent display to field emission display," Elettronica Oggi, no. 281, 15 Oct. 1999, pp.139-41. Publisher: Gruppo Editoriale
Jackson, Italy

[1.18] AA. Talin, B. Chalamala, BF. Coll, JE. Jaskie, R. Petersen, L. Dworsky, "Development of field emission flat panel displays at Motorola," Flat-Panel Display Materials-1998. Symposium Mater. Res. Soc. 1998, pp.175-7. Warrendale, PA, USA.

[1.19] M.A. Guillorn, J.H. Whealton, L.R. Baylor, A.V. Melechko, V.I. Merkulov, D.K. Hensley, M.D. Hale, R.J. Kasica, D.H. Lowndes and M.L. Simpson, "Electron Sources for Massively Parallel Electron Beam Lithography System using Single Vertically Aligned Carbon Nanofiber Cathodes," Technical procedding of the 2003 Nanotechnology conference and trade show 2003 Vol. 3.

[1.20] Vito Dai, Avideh Zakhor, "Lossless Compression Techniques for Maskless Lithography Data" in Emerging Lithographic Technologies VI, Proceedings of SPE Vol. 4688, 2002.

[1.21] G. X. Guo, K. Tokunaga, E. Yin, F. C. Tsai, A. D. Brodie, and N. W. Parker, " Use of microfabricated cold field emitters in sub-100 nm maskless lithography," J. Vac. Sci. Tech. B 19, 2001, 862

[1.22] T. H. P. Chang, L. P. Muray, U. Staufer, and D. P. Kern, "Arrayed miniature electron beam columns," J. Microelectronic Engineering, v 21, n 1-4, Apr, 1993, p 129-140

[1.23] E. Yin, A.D. Brodie, F. C. Tsai, G.X. Guo, N.W. Parker, "Electron optical column for a multicolumn, multibeam direct-write electron beam lithography system" J. of Vac. Sci. & Technol. B, v 18, n 6, Nov, 2000, p 3126-3131

[1.24] L.P. Muray, K.Y. Lee, J.P. Spallas, M. Mankos, Y. Hsu, M.R. Gmur, H.S. Gross, C. B. Stebler, T.H.P. Chang, "Experimental evaluation of arrayed microcolumn lithography," Microelectronic Engineering, v 53, n 1-4, June 2000, p 271-7

[1.25] T. H. P. Chang, M. Mankos, K.Y. Lee, and L. P. Muray,"Multiple electron-beam lithography" Microelectronic Engineering, v 57-58, Sept., 2001, p 117-135

[1.26] R.E. Fontana, J. Katine, M. Rooks, R. Viswanathan, J. Lille, S. MacDonald, E. Kratschmer, C. Tsang, S. Nguyen, N. Robertson, P. Kasiraj, "E-beam writing: A next-generation lithography approach for thin-film head critical features," IEEE Transactions on Magnetics, v 38, n 1 I, January, 2002, p 95-100

Chapter 2

[2.1] C.-Y. Hong, "Intelligent Field Emission Arrays," Ph. D. Thesis, Department of Material Science and Engineering, MIT, Cambridge, 2003.

[2.2] R. H. Fowler and L. Nordeim, "electron Emission in Intense Electric Fields," Proceedings of the Royal Society of London, Ser. A 119, pp.173-181, Mar. 1928

[2.3] W. Zhu, Vacuum Microelectronics, Wiley, New York, 2001

[2.4] R. H Good and E. W. Muller, "Field Emission," Handbook of Physics, vol. XXXI, Springer, 1956

[2.5] L. Dvorson, "Micromachining and Modeling of Focused Field Emitters for Flat Panel Displays," Ph. D. Thesis, Department of Electrical Engineering and

Computer Science, MIT, Cambridge 2001.

[2.6] W. B. Hermannsfeldt, R. Becker, I. Brodie, A. Rosengreen, and C. A. Spindt, Nucl. Intsrum. Methods A 298, 39, 1990

[2.7] P. W. Hawkes and E. Kasper, "Principles of Electron Optics," Vol. 2, Chapter 44, Academic Press, San Diego, 1989.

[2.8] R. Stratton, "Field Emission From Semiconductors," Proc. Phys. Soc., Vol. B68, pp. 746-757, 1995

[2.9] R. N. Hall, "The Application of Non-Integral Functions to Potential Problems," Journal of Applied Physics, vol. 20, pp. 925-931, Oct. 1949.

[2.10] W.P. Dyke, J.K. Trolan, W.W. Dolan, and G. Barnes, "The field emitter: fabrication, electron microscopy, and electric field calculations," Journal of Applied Physics, vol. 24, pp. 570-576, May 1953

[2.11] D. Nicolaescu, "Physical basis for applying the Fowler-Nordeim J-E relationship to experimental I-V data," J. of Vac. Sci. and Technol. B., vol. 11, pp. 392-395, 1993

[2.12] C. A. Spindt, I. Brodie, L. Humphrey, and E. R. Westerberg, "Physical properties of thin-film field emission cathodes with Molybdenum cones," Journal of Applied Physics, vol. 47, pp. 5248-5263, Dec. 1976

[2.13] K.L. Jensen, E.G. Zaidman, M.A. Kodis, B. Goplen, D.N. Smithe, "Analytical and seminumerical model for gate field emitter arrays. I. Theory," J. of Vac. Sci. and Technol. B 14(3), pp. 1942-1946, May/Jun 1996

[2.14] M. Abramowitz and I. Stegan, Handbook of Special Functions, Dover Publications, Washington, DC. 1970.

[2.15] D.G. Pflug, "Low Voltage Field Emitters Arrays though Aperture Scaling," Ph. D. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge 2000

[2.16] M. Ding, "Field Emission from Silicon," Ph. D Thesis, Department of Physics, MIT, Cambridge, 2001.

[2.17] M. Ding, G. Sha, and A. Akinwande, "Silicon field emission arrays with atomically sharp tips: Turn-on voltage and the effect of tip radius distribution," IEEE-Transactions on Electron Devices. Dec. 2002; 49(12): 2333-42.

[2.18] M. Ding, H. Kim, and A. Akinwande, "Highly uniform and low turn-on voltage Si field emitter arrays fabricated using chemical mechanical polishing," IEEE

Electron device letters, vol. 21, No. 2. Feb. 2000

[2.19] L. Dvorson, M. Ding, and A. Akinwande, "Analytical electrostatic model of silicon conical field emitters - Part I," IEEE-Transactions on Electron Devices. Jan. 2001; 48(1): 134-43

[2.20] L. Dvorson, M. Ding, and A. Akinwande, "Analytical electrostatic model of silicon conical field emitters - Part II: extension to devices with focusing electrode," IEEE-Transactions on Electron Device. Jan. 2001; 48(1): 144-8

Chapter 3

[3.1] L. Dvorson, "Micromachining and Modeling of Focused Field Emitters for Flat Panel Displays," Ph. D. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge 2001.

[3.2] W. B. Hermannsfeldt, R. Becker, I. Brodie, A. Rosengreen, and C. A. Spindt, Nucl. Intsrum. Methods A 298, 39, 1990

[3.3] J. Itoh, Y. Tohma, K. Morikawa, S. Kanemaru, K. Shimizu, "Fabrication of double-gated Si field emitter arrays for focused electron beam generation," J. of Vac. Sci. and Technol. B 13(5), Sept/Oct 1995

[3.4] Y. Toma, S. Kanemaru,and Y. Itoh, "Electron-beam characteristics of double-gated Si field emitter arrays," J. of Vac. Sci. & Technol. B v 14, n 3, May-June 1996, p 1902-5

[3.5] C. Py, J. Itoh, T. Hirano, S. Kanemaru, "Beam focusing characteristics of silicon microtips with an in-plane lens," IEEE Transactions on Electron Devices, vol. 44, no 3, March 1997, pp. 498-502

[3.6] C.M. Tang, T.A. Swyden, "Beam collimation from field-emitter arrays with linear planar lens," IEEE International Conference on Plasma Science, 1996, p. 243

[3.7] M. Ding, "Field Emission from Silicon," Ph. D Thesis, Department of Physics, MIT, Cambridge, 2001.

[3.8] M. Ding, H. Kim, and A. Akinwande, "Highly uniform and low turn-on voltage Si field emitter arrays fabricated using chemical mechanical polishing," IEEE Electron device letters, vol. 21, No. 2. Feb. 2000

[3.9] L. Dvorson, I. Kymissis, and A. I. Akinwande, "Novel CMP-based process for

fabricating arrays of double-gated silicon field emitters," J. of Vac. Sci. & Technol. B Microelectronics and Nanometer Structures Jan/Feb. 2001; 139-40

[3.10] L. Dvorson, and A. I. Akinwande, "Double-gated Spindt emitters with stacked focusing electrode," J.of Vac. Sci. & Technol. B Microelectronics and Nanometer Structures Jan. 2002; 20(1); 53-9

[3.11] L. Dvorson, I. Kymissis, and A. I. Akinwande, "Double-gated silicon field emitters," J. of Vac. Sci. & Technol. B Microelectronics and Nanometer Structures Jan/Feb. 2003; 21(1)

[3.12] J. D. Plummer, M. D. Deal, P. B. Griffin, Siliconm VLSI Technology, Prentice Hall, New Jersey, 2000

Chapter 4

[4.1] L. Dvorson, "Micromachining and Modeling of Focused Field Emitters for Flat Panel Displays," Ph. D. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge 2001

[4.2] S. Ross, A First Course in Probability, Prentice Hall, New Jersey, 2002

[4.3] M. Ding, "Field Emission from Silicon," Ph. D Thesis, Department of Physics, MIT, Cambridge, 2001.

[4.4] J. Itoh, Y. Tohma, K. Morikawa, S. Kanemaru, K. Shimizu, "Fabrication of double-gated Si field emitter arrays for focused electron beam generation," J. of Vac. Sci. and Technol. B 13(5), Sept/Oct 1995

Chapter 5

[5.1] L. Dvorson, "Micromachining and Modeling of Focused Field Emitters for Flat Panel Displays," Ph. D. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge 2001

[5.2] J. Itoh, Y. Tohma, K. Morikawa, S. Kanemaru, K. Shimizu, "Fabrication of double-gated Si field emitter arrays for focused electron beam generation," J. of Vac. Sci. and Technol. B 13(5), Sept/Oct 1995

[5.3] C. Py, J. Itoh, T. Hirano, S. Kanemaru, "Beam Focusing Characteristics of

Silicon Microstips with an In-Plane Lens," IEEE Transaction on Electron Devices, March, 1997, v. 44, No. 3, p498-502

[5.4] C. M. Tang, T. A. Swyden, "Beam Collimation from Field-Emitter Arrays with Linear Planar Lenses," SID 1997 Digest. V.28, P.115

Chapter 6

[6.1] G. X. Guo, K. Tokunaga, E. Yin, F. C. Tsai, A. D. Brodie, and N. W. Parker, " Use of microfabricated cold field emitters in sub-100 nm maskless lithography," J. Vac. Sci. Tech. B 19, 2001, 862

[6.2] E. Yin, A.D. Brodie, F. C. Tsai, G.X. Guo, N.W. Parker, "Electron optical column for a multicolumn, multibeam direct-write electron beam lithography system" J. of Vac. Sci. & Technol. B, v 18, n 6, Nov, 2000, p 3126-3131

[6.3] L.P. Muray, K.Y. Lee, J.P. Spallas, M. Mankos, Y. Hsu, M.R. Gmur, H.S. Gross, C. B. Stebler, T.H.P. Chang, "Experimental evaluation of arrayed microcolumn lithography," Microelectronic Engineering, v 53, n 1-4, June 2000, p 271-7

[6.4] T. H. P. Chang, M. Mankos, K.Y. Lee, and L. P. Muray,"Multiple electron-beam lithography" Microelectronic Engineering, v 57-58, Sept., 2001, p 117-135

[6.5] R.E. Fontana, J. Katine, M. Rooks, R. Viswanathan, J. Lille, S. MacDonald, E. Kratschmer, C. Tsang, S. Nguyen, N. Robertson, P. Kasiraj, "E-beam writing: A next-generation lithography approach for thin-film head critical features," IEEE Transactions on Magnetics, v 38, n 1 I, January, 2002, p 95-100

[6.6] http://www.microchem.com/products/pdf/PMMA_Data_Sheet.pdf

[6.7] J. Itoh, Y. Tohma, K. Morikawa, S. Kanemaru, K. Shimizu, "Fabrication of double-gated Si field emitter arrays for focused electron beam generation," J. of Vac. Sci. and Technol. B 13(5), Sept/Oct 1995

[6.8] Y. Toma, S. Kanemaru,and Y. Itoh, Proceedings of the IEEE International vacuum Microelectronics Conference, IVMC, 1995, p 9-13

[6.9] J. F. Gibbons, Projected range statistics: semiconductors and related materials, Halsted Press, New York, 1975