Magellan Instant Camera Testbed

by

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Abstract

The Magellan Instant Camera (MagIC) is an optical CCD camera that was built at MIT and is currently used at Las Campanas Observatory (LCO) in La Serena, Chile. It is designed to be both simple and efficient with minimal optics between the telescope port and the detector, a high quantum efficiency and throughput detector, a CryoTiger® self-contained, cooling system that cleanly and cost-effectively maintains observing temperatures as low as 70K, and a modular user interface that allows the observer to control all elements of an exposure. The goal of this thesis project is to create a testbed for MagIC at MIT. The testbed consists of identical camera electronics, software, and hardware to MagIC, but it has an engineering-grade CCD. The system will be used to test electronics and software before installation occurs at LCO and to serve as an additional camera at Wallace Astrophysical Observatory for MIT students and other observatory users. This thesis will serve a documentation source for MagIC as well as a manual for setting up and running the MagIC testbed.

Thesis Supervisor: James L. Elliot
Title: Professor of Physics and Planetary Astronomy

Acknowledgments

Thank you to Professor Elliot for advising me on my thesis and for teaching me the last few years. Thank you Amanda Gulbis for teaching me about Unix and the electronics system and for surviving the frustrations of Sun workstations. Thank you Brian Taylor for being an constant source of information and help.

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Chapter 1

Introduction

1.1 What is MagIC?

1.1.1 History of MagIC

MagIC is short for the **Mag**ellan **I**nstant **C**amera. It is an optical CCD system designed for use on either of the two Magellan telescopes[1] at Las Campanas Observatory (LCO) in La Serena, Chile.[1] See Figure 1-1 for a simplified telescope schematic. MagIC was designed to have high throughput, with a minimum of interfening optics. The only additional optics that MagIC introduces between the telescope and detector are the filter and the clear dewar window. See Figure 1-2 for the optical path of light entering MagIC. The focal plane scale of 0.069 arcsec/pixel gives MagIC the high resolution that is desired for the science programs at LCO.[6, p. 9-10]

Camera construction was headed by Professor James Elliot of MIT with personnel from the MIT Department of Earth, Atmospheric, and Planetary Sciences, MIT Department of Physics, and the MIT Center for Space Research. [5, p. 1] While camera construction was scheduled from September, 1999, to September, 2001, it was mounted on the Baade telescope in March, 2001. Since March, 2001, MagIC has been available for scheduled full-night and shared-night use. Scientists measured its

[1]The telescopes are denoted "Magellan I" or "Baade" and "Magellan II" or "Clay", and both have an altitude-azimuth mount.

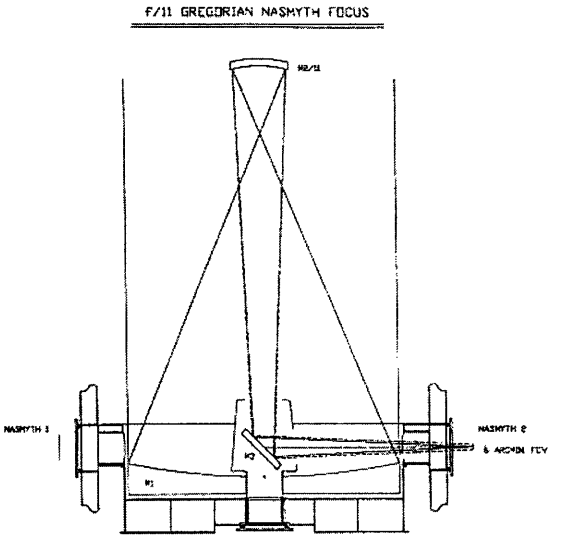


Figure 1-1: **Reflecting Telescope**. The schematic is of a reflecting telescope like the Magellan Telescopes at Las Campanas Observatory. The telescope employs a Gregorian configuration for the f/11 (Nasmyth) focus. On the telescope itself, the Nasmyth foci are located on the axis about which the telescope moves to change altitude. The folded ports, or axilliary ports, are located in the same horizontal plane as the Nasmyth foci, but rotated out of the page of the drawing. These are not located on any special axes. Courtesy of http://www.lco.cl/lco/magellan/telescopes/index.html.

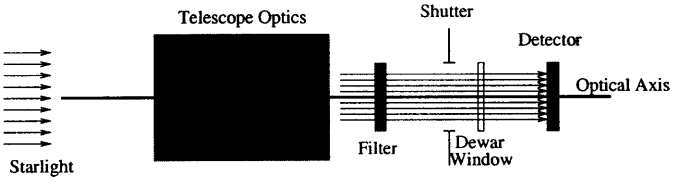


Figure 1-2: **Optical Path of Light Through MagIC**. Starlight is collected by the Magellan telescope. The tertiary mirror (shown in Figure 1-1) directes collimated light towards the instrument. The light passes through a filter that transmits a certain bandwidth. Then, the light passes through the shutter, which is large enough that the detector receives an unvignetted beam of light. [6]

Table 1.1: **MagIC Current Status**. Adapted from http://occult.mit.edu/ instrumentation/magic.

MagIC Current Status	
MagIC Location	Folded Port 3 of the Clay telescope; Available for scheduled full-night and shared-night use
Operating Modes	Quad-amp readout and (unsupported) single-amp readout (binned 1×1 or 2×2) Readout time: 20 seconds (quad amp 1×1) Output files contains serial and parallel overscans for each quadrant for bias calibration
Filter Status	Filters Installed: Johnson-Cousins: B, V, R, I Sloan: u', g', r', i', z' Custom: VR 6 positions for guest filters Filter positions recorded in lookup table
Folded Port Guider	Operational Dual-probe system Shack-Hartman test per min

performance on the telescope: read noise, gain, and saturation levels, while also using it for observational data. In September 2002, the camera was moved from the Baade to a principal Nasmyth port of the Clay telescope. Finally, in October 2002, MagIC was moved to its permanent home at the third folded port on the Clay telescope.[2][11]

MagIC has a quad-amp readout mode (with either 1×1 or 2×2 binning), ten available filters (See Table 1.2 for the filter bandwidths), six slots for custom filters, and an operational guider used exclusively for MagIC. A description of the current status of MagIC is listed in Table 1.1.

[2]Both 6.5 m telescopes have an f/15 focus in the Cassegrain position (although the Cassegrain positions are not implemented), f/11 foci at the two Nasmyth locations, and f/11 foci at the three auxilliary ports, or folded ports. The f/11 foci implement Gregorian configurations. See http://www.lco.cl/lco/magellan/telescopes/index.html

Table 1.2: **Filter Transmission Bandwidth**. Adapted from http://occult.mit.edu /instrumentation/magic.

Filter Transmission Bandwidth		
Filter	**Center Wavelength (nm)**	**FWHM Bandwidth (nm)**
B	425	100
V	525	100
R	650	150
I	830	200
u'	360	50
g'	485	110
r'	625	150
i'	775	140
z'	910	140
VR	625	175

1.1.2 MagIC System Components

The primary components of are a detector, filter system, electronics, and cooling system.. Figures 1-3 and 1-4 illustrate how these components fit together as mounted on folded port 3 of the Clay telescope.

The mounting plate (A) physically supports the entire system and attaches at the telescope port. Attached to plate (A) is the filter-wheel housing (B). This piece weighs approximately 275 pounds, and it holds two filter wheels, each with slots for nine, four-inch filters. Also, the remaining parts of the instrument are attached to the housing. The rest stand fittings (D), located on either side of the filter-wheel housing, support the housing when it is not on the mounting plate. The filter-wheel control box (J) allows the observer to control the filter-wheel motors (H) that move the filters into proper position. The CCD array is located in the lower, central portion of the set-up. The dewar (F) is an octogonal housing and it holds the CCD array in an evacuated chamber. The CCD electronics box (E) allows the observer to control the camera via computer (See Chapter 2 for more detail). The CryoTiger® cold end (G) extends off the back of the dewar and cools the CCD. In the photograph the CryoTiger® cooling system is attached to the cold end via tubes that transport the

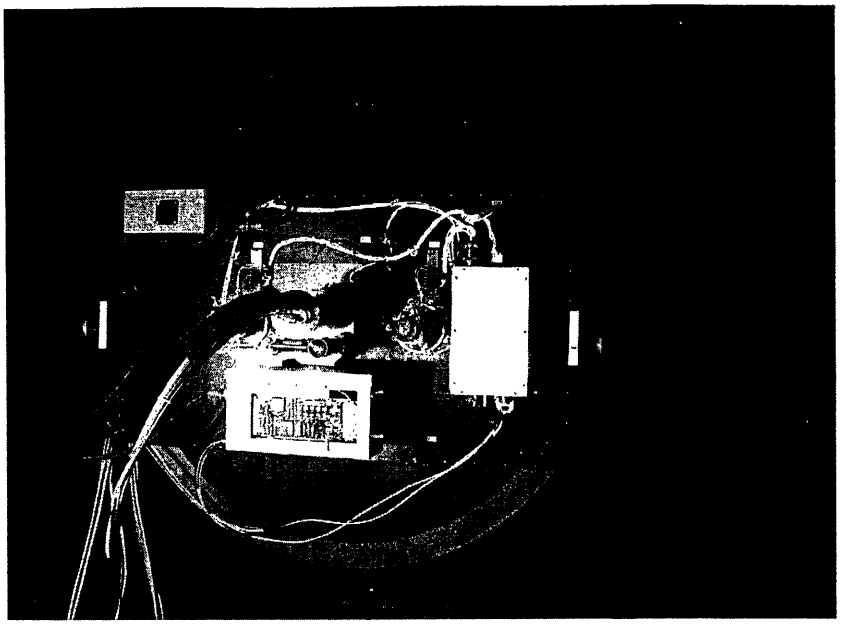
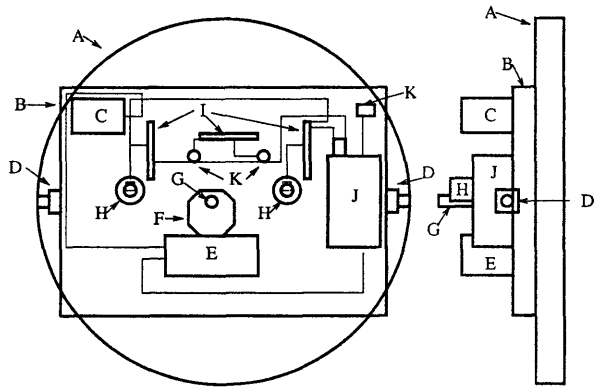


Figure 1-3: **MagIC on a Clay auxilliary port.** MagIC is currently mounted as pictured. The diameter of the anodized mounting plate is about 1.5 m. For a labelled diagram representing this photograph, see Figure 1-4. Courtesy of Susan Kern.

coolant. The camera control box is connected directly to the power supply (C), while the other motors and control boxes are connected to power distribution strips (I).

The instrument rotator and guider are not included in the diagram. Both of the Magellan telescopes have an altitude/azimuth design that leads to a field rotation as the telescope tracks celestial objects. The rotator appropriately rotates the camera to compensate for the field rotation while the telescope is tracking. The guider, specifically built for MagIC, is a dual-probe system that monitors the guiding and performs a Shack-Hartman test once per minute, compensating for any distortions in the primary and secondary mirrors. Both of these components greatly increase the quality of MagIC images. [6, p. 8-9]

The filter-wheel and shutter mechanism also play very important roles in the MagIC sytem. The filter-wheel housing, shown in Figure 1-4, holds two filter wheels that each can accomodate nine, four-inch filters. One filter position in each wheel is left open. The filter wheels overlap each other so that an open spot on one is set when a filter from the other wheel is being used. The filter-wheels rotate by remote



A. Mounting Plate
B. Filter Wheel Housing
C. Power Supply (GL Scientific)
D. Rest Stand Fitting
E. CCD Electronics Box (Leach)
F. Dewar
G. CryoTiger® Cold End
H. Filter Wheel Motor
I. Distribution Strip (Terminal Block)
J. Filter Control Box
K. Electrical Port to Filter Wheel

Figure 1-4: **MagIC System Components**. The mounting plate attaches directly to the telescope, and the filter-wheel housing attaches to the mounting plate. At 275 lbs, the filter-wheel housing comprises the bulk of the mass of MagIC and therefore requires rest stand fittings when unmounted. The filter-wheel housing holds the two filter wheels (which can be rotated via the filter control box and the filter-wheel motor), and all smaller components shown attach directly to it. The GL Scientific power supply provides power for the Leach CCD electronics box. The electronics box is the controlling medium between the observer and the CCD array. The dewar that is attached to the electronics box holds the CCD array, and the CryoTiger® cold end is the junction between the thermo-electric cooling device and the dewar. The electrical ports and distribution strips are used to receive and send power between the various components.

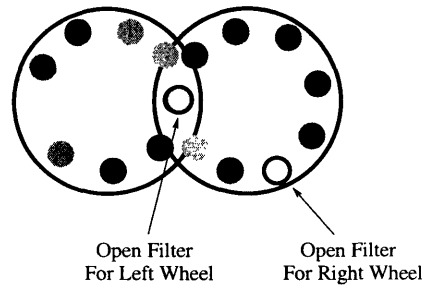


Figure 1-5: **Filter Wheel Diagram.** Each filter wheel has 9 openings. There are 10 installed filters, 6 spaces for observers to add custom filters, and 2 open spots or "Open filters" as noted in the figure. The observer can remotely position the wheels such that the filter on one wheel overlaps with the open filter of the other filter wheel.

command so that the observer has a choice of 16. See Figure 1-5. There are ten permanent filters and two open positions in the MagIC filter wheels (See Table 1.1), leaving six spaces for observers to add custom filters. The shutter (not shown) is mounted between the dewar and the filter-wheel, and it is large enough to provide an unvignetted view of the optical beam. [6, p. 9]

The design goal for the camera and dewar was to achieve the highest efficiency over the widest possible range of optical wavelengths. Hence MagIC contains no optics except for the dewar window. The other camera characteristics that allow for high efficiency are discussed in Chapter 2. [6, p. 9-10]

1.2 MagIC Testbed

In order to provide instrument support for MagIC, the PI (Professor Elliot) has decided to build a testbed at MIT. This will allow testing of operational modes and upgrades to the software before installing them in Chile. Our goals are to have:

- A complete, working replica of the MagIC detector, electronics, and computer that will be used for undergraduate study at MIT's Wallace Astrophysical Observatory (WAO).
- As a result, a backup computer that runs the most recent version of the instrument software and interfaces with the electronics to be the primary control

system for MagIC at LCO (the current control computer at LCO will become a backup).

1.2.1 Motivation

Having a working replica of MagIC at MIT has many benefits. First, we can test software upgrades on the engineering-grade chip before they are installed at LCO. By doing this, we can see how the software might affect the electronics and the chip itself and avoid downtime and problems at the telescope. We can also use this system for students to do research at WAO. The system could be used for both astronomy research and instrumentation. The camera will give MIT students and other observatory users a wider variety of possible projects for observing classes and undergraduate research. Finally, it is cost-effective to have the testbed at MIT because MIT personnel can avoid the travel expenses that would be required to work on-site at LCO.

A spare control computer is desirable for any instrument that is in use for an extended period of time. At LCO, the spare computer will be used as a safe way to test software upgrades or for troubleshooting without damaging the CCD array. Also, by using the current control computer as the backup, we can be confident that the backup will work if it is needed. The benefits of replacing the existing computer now are that the new computer will be able to withstand use for longer and the new operating system will not crash as often as the current operating system does.

1.2.2 Action Plan

We accomplished several tasks towards the goal of completing the testbed. See Chapter 3 for full detail. In the beginning we had a dewar with no CCD, an electronics box, four of the necessary electronics boards, and a Sun Ultra 10 that contained MagIC's software (LOIS-**L**owell **O**bservatory **I**nstrumentation **S**ystem) but was not functional. After our own attempts to update the Ultra 10 failed, we sent the Ultra 10 and all electronics to Lowell Observatory in Flagstaff, Arizona. Here, Brian Taylor, the creator and maintainer of LOIS, worked with Amanda Gulbis, a post-

doctoral researcher working with Professor Elliot to support MagIC, to update the control software and to interface the software with the electronics. They also tested all the electronics boards and returned the viable spares to LCO. Once these tasks were complete and we had the Ultra 10 and the electronics back at MIT, we installed the necessary compilers (SunOne Studio 7) on the Ultra 10 and ran LOIS with the electronics and tested the different running modes. We then bought a Sun Blade 150 and installed the updated operating system (Solaris 9), SunOne Studio 7, and LOIS so that it too would interface with the electronics. Our final step will be to acquire MagIC's engineering CCD chip to mount in our dewar so that the WAO system will be operational.

Chapter two describes the MagIC detector, electronics, and software components in detail. This section is the necessary background for understanding the testbed and the steps taken to create it. Chapter three details our steps in creating the testbed. Chapter four includes my conclusions and recommendations for future work on the testbed.

Chapter 2

Camera and Electronics Components

All design characteristics of MagIC are focused on being a simple but capable camera. The thinned, back-illuminated CCD array from Scientific Imaging Technologies, Inc. has high quantum efficiency and throughput over a wide wavelength range.[1] A CryoTiger® cryo-cooler from IGC-APD Cryogenics allows the CCD array to constantly and cost-effectively maintain observing temperatures as low as 70K while mounted in an evacuated dewar.[2] [6, p. 10] The software interface, LOIS, lets the observer control the type of exposure, the filter used, the length of the exposure, and the data storage, via a specialized electronic control system. This chapter delves into the design specifics of these camera elements and gives the reader necessary information about the camera operation.

Table 2.1: **SITe SI424A CCD Chip Specifications.** The serial number of our CCD chip is S/N 99061AABR02-01, SI424AB4-0. Adapted from http://occult.mit.edu/instrumentation/magic.

SITe SI424a Specifications	
Detector Size	2048 pixels × 2048 pixels
Pixel Size	24 μm
Focal Plane Scale	2.89 arcsec/mm= .069 arcsec/pixel
Field of View	2.35 armin × 2.35 arcmin
Quantum Efficiency	85% – 400nm; 82% – 700nm; 48% – 900nm
Output	4 output device at 50 + Kpix/sec
Readout	4 amp, full frame = 23 sec

2.1 Technical Characteristics of CCD and Focal Plane

Table 2.1 provides information on the characteristics of the CCD. At approximately 2 inches × 2 inches, MagIC's detector is comparable to the single detectors of other astronomical instruments. MagIC's detector is a SI424A, grade 0 (less than 4 column defects, less than 10 cluster defects, and less than 80 pixel defects) chip from SITe.[12] The detector dimensions are 2048 pixels × 2048 pixels, with a pixel size of 24 μm. MagIC is mounted on the Clay telescope at folded port 3 so it has an f/11 focus, and the focal plane scale is .069 arsec/pixel (approximately 1 arcmin/inch). Hence, the field of view is about 2 armin × 2 arcmin (2.35 arcmin × 2.35 arcmin). The modest field of view and large detector size were chosen because the science conducted using MagIC[3] requires high resolution.[6]

A high quantum efficiency is also essential for the science programs at Magellan. For the SI424A CCD, the quantum efficiency is 85% at 400 nm, 81.8% at 700 nm, and

[1]Quantum efficiency is the percent efficiency at which the CCD can produce electronic charge from incident photons. Throughput is the amount of work a system can do in a given time period. We measure throughput in magnitudes for 1 DN/sec (Data Number/second) or electrons/sec for the 20^th magnitude.

[2]The CryoTiger® cryo-cooler is a self-contained system that requires no renewable cryogen.

[3]Science programs include: monitoring gravitationally lensed quasars, stellar occulations of solar system bodies, Kuiper belt objects and Centaurs, and optical follow-up to gamma-ray bursts, among others.

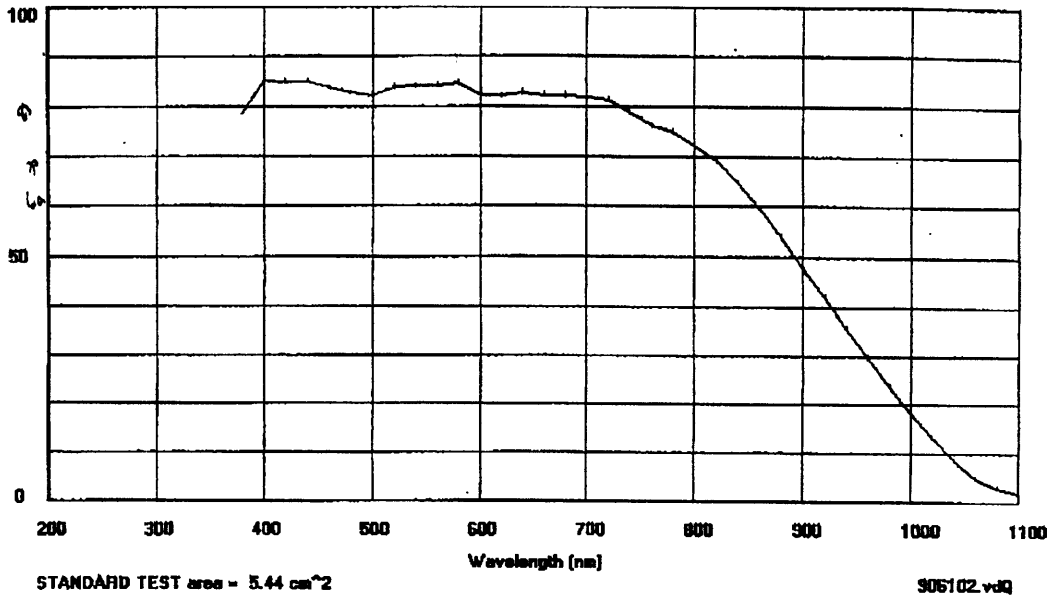


Figure 2-1: **Quantum Efficiency**. The quantum efficiency of our SI424A CCD is 85% at 400 nm, 81.8% at 700 nm, and 47.6% at 900nm. [12]

47.6% at 900 nm. See Figure 2-1 for a plot of quantum efficiency vs. wavelength for the SI424A. MagIC's throughput varies for the different filter bandwidths. Table 2.2 lists the throughput for the filters that are always mounted in MagIC's filter wheel. The visible and red filters give the highest throughput.

We also consider the output and readout of the CCD array. Although mechanically contiguous, the CCD is separated electrically into four, 1024 $\times$ 1024 pixel quadrants. The quadrants are designated I or A for the lower left, II or B for the lower right, III or C for the upper right, and IV or D for the upper left. Each quadrant then has its own output/readout channels. Each of MagIC's four outputs operate at 50 Kilopixels/sec. Therefore, the chip outputs in about 23 seconds. See Table 2.1. The four readout channels allow the simultaneous readout of each 1024 pixel $\times$ 1024 pixel quadrant. [6]

Besides having very good throughput, quantum efficiency, readout, and output, the CCD array has very good performance because it is low-noise. Table 2.3 outlines the original data for the gain, read noise, and saturation levels for each of the amplifiers, and Table 2.4 does the same for the updated data for the gain and read noise.

Table 2.2: **Throughput.** The data was collected during the June 2001 engineering run. Adapted from http://occult.mit.edu/instrumentation/magic.

Filter	Throughput	
	mag for 1 DN/sec	e-/sec for 20 mag
B	25.95	478.41
V	26.30	665.15
R	26.60	874.74
I	25.94	473.54
u'	23.62	55.90
r'	26.76	1016.25
g'	26.44	751.14
i'	26.38	715.68
z'	25.22	244.70

Table 2.3: **Gain, Read Noise, Saturation, and Linearity.** The results are from June 2001 engineering data at the Baade. Adapted from http:// occult.mit.edu/instrumentation/magic.

Camera Mode: Unbinned, 4-amp readout				
Amplifier	Gain (e-/DN)	Read Noise (e-)	Sat. Level (ADU)	Linearity
1	1.94	5.9	65K	linear to sat.
2	1.92	4.6	65K	linear to sat.
3	1.91	5.3	34K?	linear to sat.
4	2.05	5.2	34K?	linear to sat.

The new measurements are more precise than the old measurements, but the new performance data resembles the older performance data.

2.2 Electronics Design

To control the CCD array, we use a low-noise, programmable electronics system developed by Bob Leach of Leach Electronics at San Diego State University. The controller uses 16-bit, A/D (analog to digital) converters that are designed to readout a variety of CCD arrays. The Leach electronics system is designed to operate one or more CCD arrays, each with one or more readout circuits (up to 16 total readouts) runing as fast

Table 2.4: **Updated Gain and Read Noise.** The results are from April 2004 engineering data at the Clay. [8]

Camera Mode: Unbinned, 4-amp readout			
Amplifier	**Measurements**	**Gain (e-/ADU)**	**Read Noise (e-)**
1	36	1.993 ± 0.015	5.529 ± 0.047
2	36	1.994 ± 0.019	6.074 ± 0.052
3	36	1.891 ± 0.018	5.002 ± 0.056
4	36	2.042 ± 0.017	4.824 ± 0.053

as 1 megapixel per second. We previously mentioned that MagIC's detector has 4 readouts that run at 50 kilopixel per second, so these electronics are quite capable of processing data.[7] MagIC's electronics were customized by instrumentation experts at Lowell Observatory, who developed the LOIS operating system to interface the electronics with the host computer.

The mounted CCD array is connected to a header board and amplifiers in the dewar and these amplifiers are wired to the Leach electronics box. For a diagram of the CCD and the pinout, see Figures 2-2 and 2-3. The electronics box is connected to a power supply and the control computer, so the observer can control the camera via computer (See LOIS, section 2.3) by entering commands that are processed by the electronics and then sent to the CCD array.

The Leach electronics box holds several circuit boards that act as media between the control software and the CCD. These boards include the timing board, the clock driver board, the CCD video processor boards, the utility board, the power control board, and the backplane. Exact Diagrams of the clock driver and video processor boards are located in Appendix A.

The basic communication in MagIC is a loop from the observer to the CCD array and back to the observer again. See Figure 2-4 for a schematic. First the observer enters commands into the software interface, LOIS (see Section 2.3) These commands are interpreted by the host computer, which then sends commands to the timing board via a fiber optic link. The fiber optic link plugs directly into the computer by way of a PCI card. See Appdendix B for descriptions of commands sent to the timing

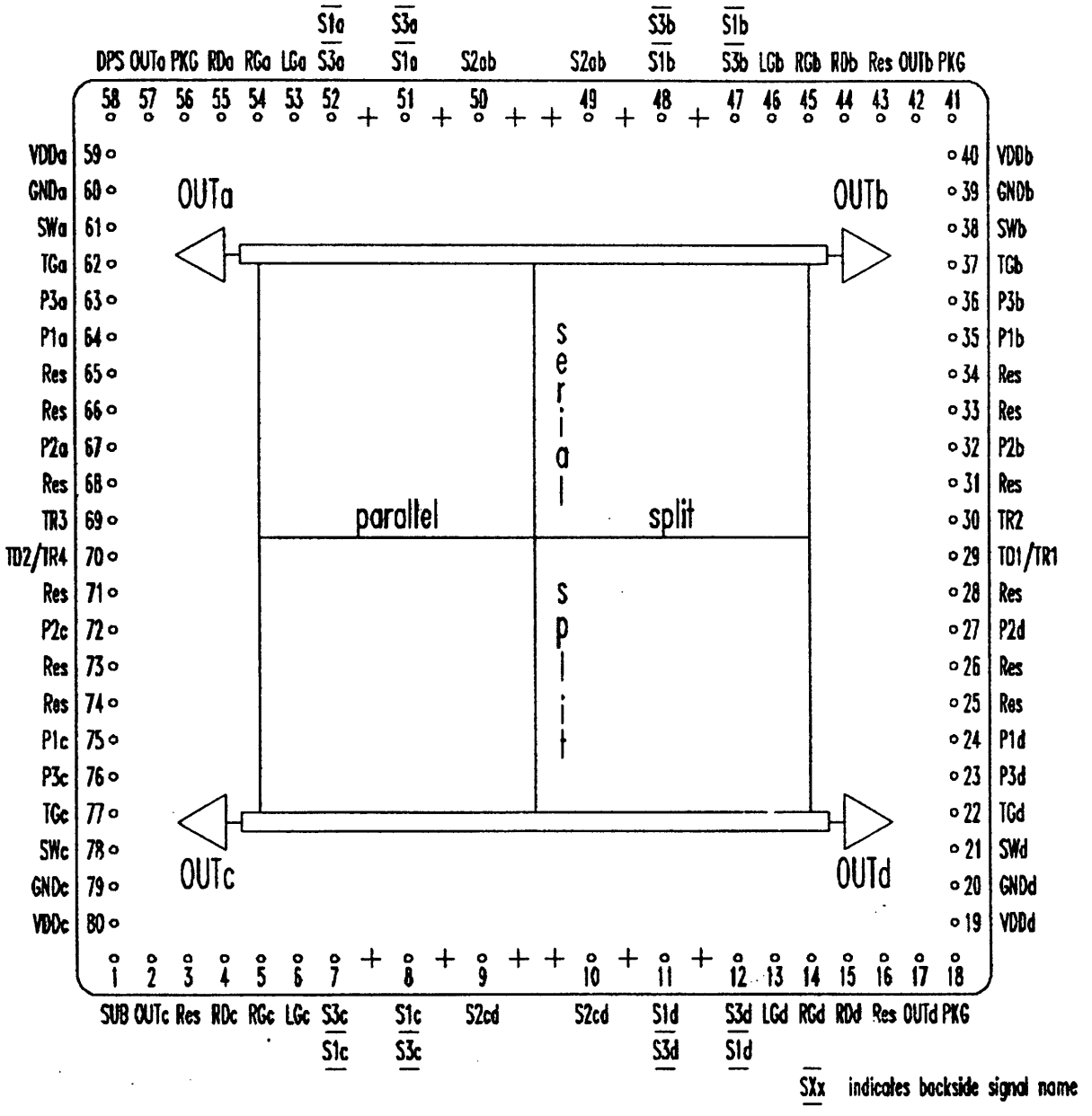


FIGURE 6 SI-424A *pin labels*

Figure 2-2: **SI424A Chip**. The physical layout of the chip is shown here. We can see the four quadrants of the chip as well as the layout of the pinouts shown in Figure 2-3. These pins attach to a header board that mounts the CCD in the dewar. [13]

SI-424A PIN DEFINITION

PIN # (BACK)	FUNCTION	REGISTERS	SYMBOL	PIN # (BACK)	FUNCTION	REGISTERS	SYMBOL
1	Substrate and Package Ground		SUB	41	Substrate and Package Ground		PKG
2	Output transistor source, c output	c register	OUTc	42	Output transistor source, b output	b register	OUTb
3	Reserved	*	Res	43	Reserved	*	Res
4	Reset Drain Supply, c output	c register	RDc	44	Reset transistor drain, b output	b register	RDb
5	Reset Gate, c output	c register	RGc	45	Reset transistor gate, b output	b register	RGb
6	Last gate, c output	c register	LGc	46	Last gate, b output	b register	LGb
7(8)	Serial phase 3, c register	c register	S3c	47(48)	Serial phase 3, b register	b register	S3b
8(7)	Serial phase 1, c register	c register	S1c	48(47)	Serial phase 1, b register	b register	S1b
9	Serial phase 2, common cd register	cd register	S2cd	49	Serial phase 2, common ab register	ab register	S2ab
10	Serial phase 2, common cd register	cd register	S2cd	50	Serial phase 2, common ab register	ab register	S2ab
11(12)	Serial phase 1, d register	d register	S1d	51(52)	Serial phase 1, a register	a register	S1a
12(11)	Serial phase 3, d register	cd register	S3d	52(51)	Serial phase 3, a register	a register	S3a
13	Last gate, d output	d register	LGd	53	Last gate, a output	a register	LGa
14	Reset transistor gate, d output	d register	RGd	54	Reset transistor gate, a output	a register	RGa
15	Reset transistor drain, d output	d register	RDd	55	Reset transistor drain, a output	a register	RDa
16	Reserved	*	Res	56	Substrate and Package Ground		PKG
17	Output transistor source, d output	d register	OUTd	57	Output transistor source, a output	a register	OUTa
18	Substrate and Package Ground		PKG	58	Diode Protection substrate		DPS
19	Output transistor drain, d output	d register	VDDd	59	Output transistor drain, a output	a register	VDDa
20	Output Ground Reference	d register	GNDd	60	Output Ground Reference	a register	GNDa
21	Summing well, d output	d register	SWd	61	Summing well, a output	a register	SWa
22	Transfer gate, lower serial register	cd register	TGd	62	Transfer gate, upper serial register	ab register	TGa
23	Parallel phase 3	lower quadrants	P3d	63	Parallel phase 3	upper quadrants	P3a
24	Parallel phase 1	lower quadrants	P1d	64	Parallel phase 1	upper quadrants	P1a
25	Reserved	*	Res	65	Reserved	*	Res
26	Reserved	*	Res	66	Reserved	*	Res
27	Parallel phase 2	lower quadrants	P2d	67	Parallel phase 2	upper quadrants	P2a
28	Reserved	*	Res	68	Reserved	*	Res
29	Temp. Sense Diode and Resistor		TD1/TR1	69	Temp. Sense Resistor		TR3
30	Temp. Sense Resistor		TR3	70	Temp. Sense Diode and Resistor		TD2/TR4
31	Reserved	*	Res	71	Reserved		Res
32	Parallel phase 2	upper quadrants	P2b	72	Parallel phase 2	lower quadrants	P2c
33	Reserved	*	Res	73	Reserved	*	Res
34	Reserved	*	Res	74	Reserved	*	Res
35	Parallel phase 1	upper quadrants	P1b	75	Parallel phase 1	lower quadrants	P1c
36	Parallel phase 3	upper quadrants	P3b	76	Parallel phase 3	lower quadrants	P3c
37	Transfer gate, upper serial register	ab register	TGb	77	Transfer gate, lower serial register	cd register	TGc
38	Summing well, b output	b register	SWb	78	Summing well, c output	c register	SWc
39	Output Ground Reference	b register	GNDb	79	Output Ground Reference	c register	GNDc
40	Output transistor drain, b output	b register	VDDb	80	Output transistor drain, c output	c register	VDDc

NOTES: The signals applied to pins 7, 8, 11, 12, 47, 48, 51, and 52 are different for front and back-illuminated parts. The amplifier ground references (GNDx) are local substrate connections, intended for signal chain reference. They should not be biased differently than the other substrate or package connections.

* This is a package connection on the current version; future versions may omit this connection.

TABLE 3 SI-424A *pin definitions*

Figure 2-3: **SI424A Pinout.** The SI424A is interfaced with the Leach electronics by the pinout shown here. [13]

board. The timing board then sends digital signals to the clock driver board along the backplane.[4] The clock driver board translates the digital timing signals into controlled voltage levels for driving the array clock lines. These voltages are the signals that directly control the CCD array. Once the exposure is complete, the CCD video processor board amplifies and digitizes the data video signals from the CCD array. These signals are sent back to the host computer and can be stored using LOIS and viewed using an image viewing program such as SAOimage DS9. For more information on these electronics boards see http://mintaka.sdsu.edu/ccdlab/LabMain.html.[5] For more information on DS9, see http://hea-www.harvard.edu/RD/ds9. The timing, clock driver, and video processing boards are described in more detail below. [7]

2.2.1 Timing Board

See Figure 2-5 for a block diagram of the board and Figure 2-6 for a diagram of part placement on the actual board. The two main functions of the timing board are to generate digital timing signals to control the other circuit boards and to serve as a communication hub between the controller and the host computer interface board, via a duplex fiber optic link.

The general theory of operation is that the host computer sends a generic command to the timing board (for a list of commands, see Appendix B). The digital signal processor, or DSP[6], runs the generic commands that can cause the electronics to open the shutter, take an exposure and readout the chip. To carry out the commands, the timing board sends digital signals to the clocking board along the backplane. These signals are called the "switch states" and can be found in the DSP code, MagIC.waveforms.s, which is shown in Appendix C. This DSP code is currently being run at LCO and it will be used as an example. This code is our mechanism for

[4]The backplane has access to each board's pinout and connects all boards to the power supply. The power control board (or "master board") monitors and controls analog power to the backplane.

[5]In the Leach documentation, an SBUS to controller interface board is mentioned; however, we do not seem to have one in our electronics box and we are not clear on how it would fit into our system.

[6]The Motorola DSP56002GC66 digital signal processor (DSP) runs at a clock speed of 50 MHz and executes instructions in 40 ns. This is the limiting time scale that also controls the analog circuit functions.

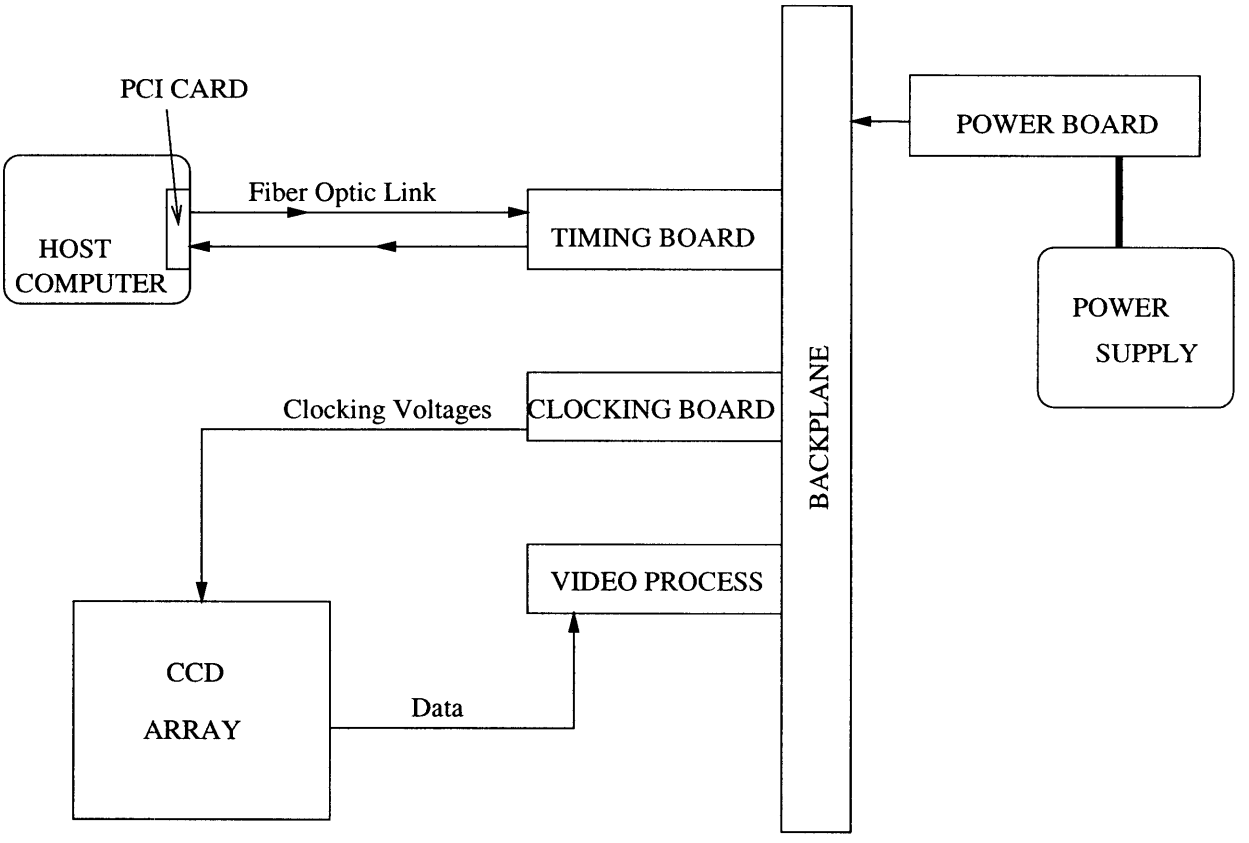


Figure 2-4: **MagIC Communication Loop**. The timing board, clocking board, video processing board, backplane, and power board are all incorporated into the Leach electronics box. The observer enters commands at the host computer command line. The host computer interprets these commands into be a series of generic commands (listed in Appendix B). These commands are sent to the timing board via the fiber optic link. The timing board sends digital signals to the clock driver board along the backplane. The clock driver board then translates the digital signals into a series of voltages that are sent to the CCD array. These voltages are the signals that directly control the CCD array. The CCD array sends data back through the video processing board, which then sends the data to the host computer via the timing board and the fiber optic link. [7]

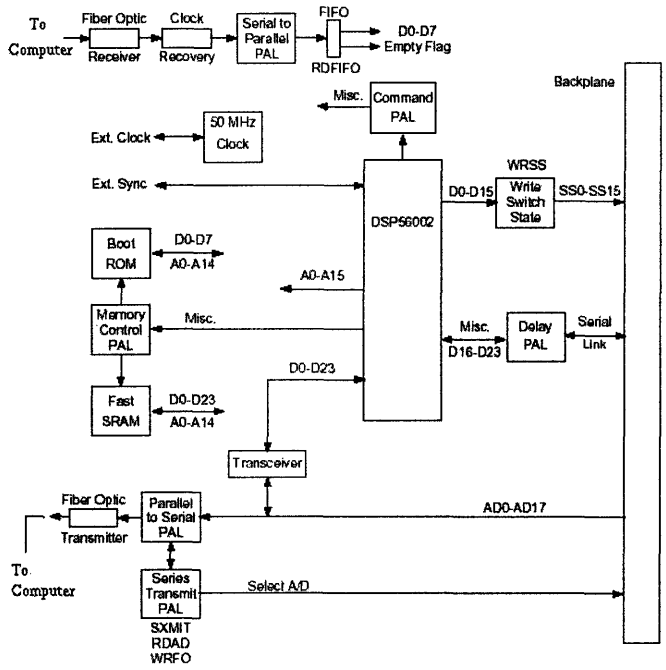


Figure 2-5: **Timing Board Block Diagram.** The signals of the timing board travel between the host computer and the backplane. The DSP is a Motorola DSP56002GC66 and it controls the signal processing in the board.[3]

programming the the Leach electronics to run at prescribed voltages. [3] [14]

2.2.2 Clock Driver Board

See Table 2.5 for the specifications for the clocking board. The clock driver board or "clocking" board translates the digital switch states received from the timing board. The received switch states cause the clocking board to switch from a high voltage DAC (Digital to Analog Converter) to a low voltage DAC. The switch to the low voltage DAC causes the voltage clock to output. See Table 2.6 for the translated timing waveforms for the SITe SI424A. These are the voltages and corresponding commands that the clocking board sends to the CCD array. This list can also be found at the beginning of MagIC.waveforms.s.

The clock driver board has 24 clocks. Only 12 clocks can be addressed at one time, so the board has two sets of clocks deemed the upper and lower clocks. The timing

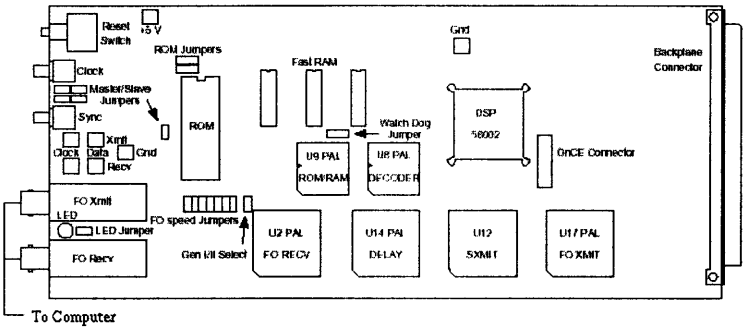


Figure 2-6: **Timing Board Part Placement**. These parts are the pieces that facillitate the signal chains shown in Figure 2-5. This diagram shows the locations of the timing board electronics as seen on the circuit board. [3]

Table 2.5: **Clock Driver Board Specifications**. [3]

Specifications	
Power Dissipation **10 W total**	304 mA at 5 V digital 247 mA at +16.5 V analog 258 mA at -16.5 V analog
Board Size	3.96 × 9.0 in.
Number of Channels	24 output channels avail. 12 outputs changed by single timing board instruction
Voltage Output	± 10 V max. 60 mA current drive capability
Rise and Fall Times	20 ns for a 10V change
Resolution	10 mV
Diagnostic Output	Any two clock driver outputs may be software selected for viewing

Table 2.6: **Timing Waveforms for the SITe SI424a**. These voltages are listed from the MagIC.waveforms.s sample code in Appendix C.

Timing Waveforms for SITe 424a		
CCD Clocking Voltages		
Name	**Abbrev.**	**Voltage**
Reset Gate High	RG_HI	+10.0
Reset Gate Low	RG_LO	0.0
Serial High	S_HI	+4.5
Serial Low	S_LO	-4.5
Summing Well High	SW_HI	+5.0
Summing Well Low	SW_LO	-6.0
Parallel High	P_HI	+1.5
Parallel Low	P_LO	-7.0
Parallel Phase 3 High	P3_HI	+3.0
Parallel Phase 3 Low	P3_LO	-7.0
Transfer Gate High	TG_HI	+1.5
Transfer Gate Low	TG_LO	-7.0
Unused Pins	ZERO	0.0
DC Bias Voltages		
Name	**Abbrev.**	**Voltage**
Output Drain	VOD	+24.30
Reset Drain	VRD	+13.50
Last gate before Summing Well	VLG	-3.5

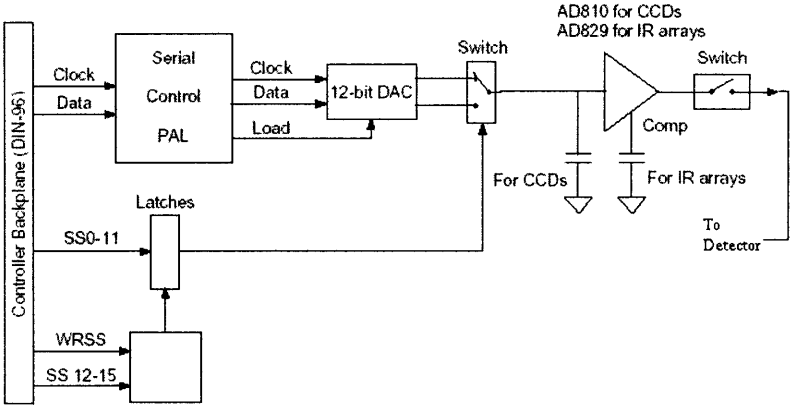


Figure 2-7: **Clock Driver Board Channel Block Diagram.** This signal chain represents 1 of 24 clocks located on the clocking board. 12 of these signals can be read simultaneously.[3]

board preprograms each DAC to have a fixed voltage value. These values are shown in the DAC's section of the DSP code shown in Appendix C. In this section, the first 24 lines refer to the first 12 clocks and the second 24 lines refer to the second 12 clocks. The voltages are designated by the corresponding commands from Table 2.6.

The scanned circuit diagram for the Clocking board is shown in Appendix A. Figure 2-7 shows a block diagram of one of the 24 clock driver channels. Figure 2-8 shows the parts layout for the clocking board.

The analog signals described in Table 2.6 are passed to the CCD array by a 37-pin DB male connector. The pinouts are shown in Table 2.7, and the physical location of these pins can be seen in Figure A-6 in Appendix A. The designations Clk0-Clk23 correspond to the clocks that are programmed with the DAC. To find the clock voltages, see the DAC section of Appendix C. For example, the first 8 lines of DAC DSP code show the DAC outputs for the high and low clocks, 0→3, which correspond to the reset gates for each quadrant of the CCD. The reset gate voltages are defined in Table 2.6, so the voltages can be manually verified to be sure that the clocking board is properly communicating with the CCD array. As discussed in Section 2.2.1, the switch state bit number can also be found in Appendix C. In the section "Define switch state bits for the CCD clocks", we see what switch state bit

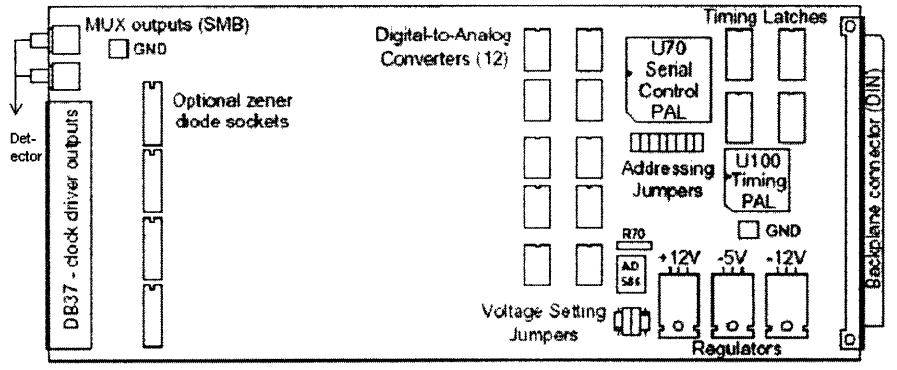


Figure 2-8: **Clock Driver Board Parts Layout**. The diagram is a rough layout of the entire clocking board. It does not show the full detail of each clock, but this detail is shown in appendix A.[3]

numbers correspond to what commands. For example "Reset Gate 0" corresponds to switch state bit number 1. These commands are also seen in the DAC section where CLK0 is labeled as "Reset Gate 0". The DAC address is set by jumpers and the DAC code. This address is necessary for intraboard communication. [3] [14]

2.2.3 CCD Video Processing Board

Once the exposure is taken, the detector sends data back to the host computer via the CCD video processing board, or video board. Two identical video processing circuits (Channels A and B) allow the video board to simultaneously processe and digitize the video output from the CCD array. In addition to these processes, the video board also supplies DC bias voltages to the CCD array. Examples of the DC bias voltage values and names are in Table 2.6.

The electronics box holds two video boards, each with two 16-bit A/D converters[7]. The video board receives analog signals from the CCD array, and the A/D converters output digital signals that are sent to the host computer via the timing board. The digital outputs are multiplexed on the backplane on dedicated A/D data pins. The

[7]These are also DACs. They have voltages, names, and addresses like the clocking DACs. However, these DACs do not appear in the 48-line DAC section of MagIC.waveforms.s. Rather, these voltages are programmed in the later sections of MagIC.waveforms.s, starting with the section labelled "Set gain and integrator speed"

Table 2.7: **Clock Driver Board Pinout**. [3]

Clock Driver Board Pinout							
Lower Bank				**Upper Bank**			
Pin #	**Signal Name**	**Switch State Bit #**	**DAC Addr.**	**Pin #**	**Signal Name**	**Switch State Bit #**	**DAC Addr.**
1	CLK0	1	0 and 1	13	CLK12	1	$18 and $19
2	CLK1	2	2 and 3	14	CLK13	2	$1a and $1b
3	CLK2	4	4 and 5	15	CLK14	4	$1c and $1d
4	CLK3	8	6 and 7	16	CLK15	8	$1e and $1f
5	CLK4	$10	8 and 9	17	CLK16	$10	$20 and $21
6	CLK5	$20	$a and $b	18	CLK17	$20	$22 and $23
7	CLK6	$40	$c and $d	19	CLK18	$40	$24 and $25
8	CLK7	$80	$e and $f	33	CLK19	$80	$26 and $27
9	CLK8	$100	$10 and $11	34	CLK20	$100	$28 and $29
10	CLK9	$200	$12 and $13	35	CLK21	$200	$2a and $2b
11	CLK10	$400	$14 and $15	36	CLK22	$400	$2c and $2d
12	CLK11	$800	$16 and $17	37	CLK23	$800	$2e and $2f
20	+12 volt power supply, regulated, 100 mA current						
21	−12 volt power supply, regulated, 100 mA current						

Table 2.8: **Video Board Pinout and DC Bias Voltage Definition.** [3]

Video Board Pinout and DC Bias Voltages				
Pin #	**Function**	**Voltage Range**	**DAC Addr.**	**Desc.**
	Input-Offset-A		$0c0xxx	Input offset, ch. A
	Output-Offset-A		$0c4xxx	Output offset, ch. A
	Input-Offset-B		$0c8xxx	Input offset, ch. B
	Output-Offset-B		$0ccxxx	Output offset, ch. B
1	VOD-A	+7.5 to +30	$0d0xxx	Output drain, ch. A
2	VOD-B	+7.5 to +30	$0d4xxx	Output Drain, ch. B
3	VRD-A	+5.0 to +20	$0d8xxx	Reset Drain, ch. A
4	VRD-B	+5.0 to +20	$0dcxxx	Reset Drain, ch. B
5		+5.0 to +20	$0e0xxx	not used
6		+5.0 to +20	$0e4xxx	not used
7		+5.0 to +20	$0e8xxx	not used
8		+5.0 to +20	$0ecxxx	notused
9	VLG-A	−5.0 to +5.0	$0f0xxx	Very Last Gate, ch. A
10	VLG-B	−5.0 to +5.0	$0f4xxx	Very Last Gate, ch. B
11	VOG-A	−10 to +10	$0f8xxx	Output Gate, ch. A
12	VOG-B	−10 to +10	$0fcxxx	Output Gate, ch. B
14				+15 V Power
15				−15 V Power
13, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25				Ground

DC bias supply section of the board provides twelve separate, low-noise, digitally programmable voltages with a variety of voltage ranges. These signals are shown in Table 2.8. [3]

A scanned copy of the circuit diagram for the video board, including a close-up of the pinout, is shown in Appendix A. See Figure 2-9 for the block diagram of the video board. See Figure 2-10 for the parts layout as seen on the video board.

2.3 Software – LOIS

LOIS (**L**owell **O**bservatory **I**nstrumentation **S**ystem) is the control system for many astronomical instruments, including MagIC. [4] Because LOIS is used for many instruments and these instruments could be used on a variety of telescopes, the sofware

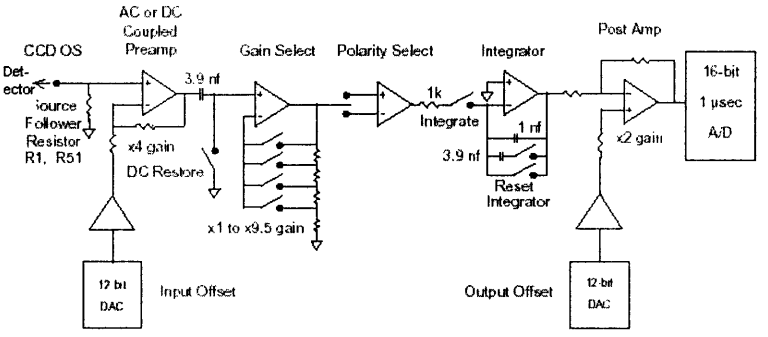


Figure 2-9: **Video Board Block Diagram**. This block diagram shows the signal chain for the data to travel from the CCD array to the host computer via the backplane. In each electronics box, there are two video boards to accomodate all data readout. [3]

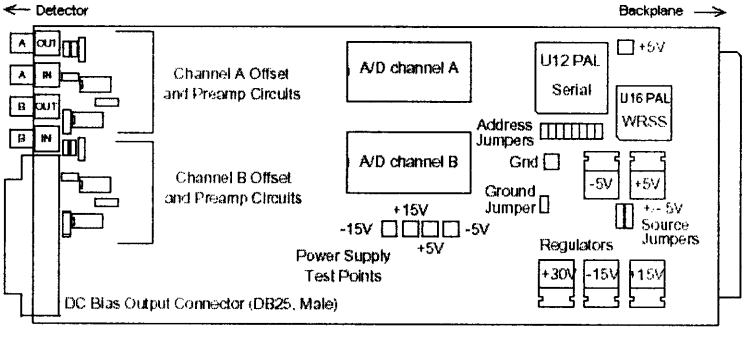


Figure 2-10: **Video Board Parts Diagram**. The diagram is a layout of the electronics on the video processing board. [3]

is designed to view the telescope, detector, and other instrument components as separate entities. Each entity is contained in a separate communication module that is loaded into the running LOIS session during configuration portion of startup. So, when the observer starts LOIS while the computer is connected to MagIC's electronics, the startup configure interface asks what telescope to use (`None`, `MagellanII`, or `Telescope Test`), what camera (`None`, `MagIC`, or `Test Camera`), what instrument interface (`None`, `MagIC Filter Wheel`, or `Test Instrument`), and what display interface (`None`, `SAOimage ds9`, or `Window`). See LOIS Explanatory Supplement for more information on the scripting launguage and the architecture of the system. [9]

The observer can either run LOIS from the host computer or remotely from a second computer that is networked to the host computer with a remote secure shell (`ssh`) connection. At LCO, the observer uses a remote connection but with the testbed we use the host computer. Both MagIC and the testbed use SAOimage DS9 to view the images. LOIS and DS9 provide a variety of functions for the observer. Using LOIS, the observer sets the startup information (telescope, camera, etc), the folder where data files are saved, the detector mode (such as quad- amp), the binning (1x1 or 2x2), the number of exposures, the time of exposures, the frame type, and any notes and comments the observer would like to add. DS9 allows the observer to view the images (inlcuding pan, zoom, rotate, and examine), and to do primary analysis on the images (graphical imaging of pixel values, psf fitting, and judging image quality). [10]

Chapter 3

MagIC Testbed

The MagIC testbed camera will be a working replica of the CCD array, electronics, and software of MagIC. The testbed will run identically to MagIC at LCO but has an engineering grade CCD and no filter wheel or shutter control. It will be used to test software and debug programs at MIT before upgrading the functioning system at LCO. The system will also be used as an additional camera at WAO. This camera will interface with the 24" telescope at WAO so that MIT students and other observatory users can use the testbed camera. As a result of the testbed, we are providing LCO with a spare host computer (or hard drive) for MagIC. This control computer will replace the existing control computer, and it will have an updated operating system that smoothly interfaces with the most current version of LOIS.

3.1 Working Testbed Requirements

Several items are required to setup and use the MagIC testbed. The electronics hardware, detector hardware, and software were discussed as the functioning components of MagIC in Chapter 2. Here we have a summary of these requirements.

- **Computer Hardware**
  - *Host Computer.* Because of LOIS, the host computer must be a Sun workstation with 256 RAM. The computer must also have good communication

on serial lines, disk space for data, and a PCI card slot. The Sun must be an Ulta10 or newer model.[1] The computers we are using for the testbed are a Sun Ultra 10 workstation and a Sun Blade 150.

- *PCI Card.* The PCI card is absolutely necessary for the testbed. It provides for communication between the host computer and the electronics box. The PCI card is installed directly into the computer and has ports for the fiber optic links that run between the electronics timing board and the computer. The PCI card must be programmed from the computer command line.

- **Electronics Hardware**

  - *CCD Control Electronics.* The CCD control electronics box, purchased from Leach electronics, includes all electronics boards described in chapter 2: timing board, clock driver board, two video boards, utility board, and power board.

  - *Power Supply.* The CCD control electronics are powered by GL Scientific power supply.

- **Detector Hardware**

  - *Dewar.* The electronics can run without a CCD and its associated dewar, but for the WAO setup, a dewar is necessary. The dewar is an octogonal housing that holds the CCD array and provides a connection for the cooling system.

  - *CCD.* The CCD directly attaches to a header board that attaches to amplifiers and the electronics box.

  - *CryoTiger® Cryo-cooler.* The CryoTiger®, built by IGC-APD Cryogenics, maintains observing temperatures as low as 70K. The cooling range of

[1]There is still uncertainty about whether an Ultra 5 would interface with the electronics and LOIS, but this computer has not been tested.

the CryoTiger® is -203°C to 20°C (70k to 293K). The CryoTiger® cold end is attached to the back of the dewar.

- **Software**
  - *Solaris Operating System.* Solaris 5.7 (Solaris 5.X systems are commonly referred to as Solaris X) is currently running at LCO, but the new control computer is running Solaris 9. Solaris 9 interfaces with LOIS and the electronics more smoothly than the other Solaris operating systems. Currently Solaris 7 is occasionally crashing at LCO and Solaris 9 will fix this problem.
  - *LOIS.* This program is needed to interface the Sun workstation with the electronics and camera. It can be obtained from Lowell Observatory (http://www.lowell.edu) and it is described in more detail in Section 2.3.
  - *Compilers.* In order to run LOIS on the Sun workstation, we first obtain a source-code copy from Lowell, then must compile it on our computer. SunOne Studio7 is sufficient to compile LOIS but SunOne Studio8C, the more recent compiler, is recommended.

3.2 Setting Up the Testbed

To start, we had a dewar with no CCD, a Leach electronics Generation II controller with all necessary boards but one, and a Sun Ultra 10 workstation (with PCI card) that ran Solaris 8 and contained LOIS. LOIS was not running and the computer was not networked.

Much of the time we spent in lab was dedicated to Sun troubleshooting. Almost every time we tried to work with the Sun workstations, we spent a half day or more figuring out the error message that appeared with each command. The problems involved a variety of tasks, including (but not limited to): logging into a Sun workstation without knowing the password, modifying files that control the workstation's networking, installing a new operating system, installing compilers, ejecting

disks (when the eject button and typing `eject` do not work), adding a new user, and switching shells. These problems are all described in detail in the MagIC lab notebook.

After many attempts to network the computer and to run LOIS, we sent to the computer and electronics to Lowell Observatory in Flagstaff, Arizona. Personnel at LCO also sent their spare electronics boards to Lowell. Here, Brian Taylor and Amanda Gulbis worked to network the computer, to test the electronics boards, and to interface the electronics with the computer. Once the tests were complete, Brian Taylor sent all necessary hardware (the Sun Ultra 10, a GL Scientific Power Supply, and the Leach electronics box with all necessary boards) back to MIT, so we could run LOIS with the electronics and set up another host computer. The remaining testbed electronics and lower noise power supply were returned to LCO as spares.

3.3 Testbed Set Up Procedure

The steps necessary to set up a the MagIC testbed are:

- *Collect the necessary hardware.*

All hardware listed in Section 3.1 is necessary to run a full testbed. However, the dewar and CCD are NOT necessary to run the camera electronics.

- *Install Solaris 9 and Network the computer*

LOIS and the electronics run with Solaris 8, but Solaris 9 will be the updated operating sytem at LCO. If a new computer is already running Solaris 9, these steps are not necessary and you should read ahead to the next paragraph. To install Solaris 9, retrieve the necessary license and obtain the installation disks (we borrowed the disks from the computing help desk at MIT). To start installation, login to the workstation with the older operating system (e.g. Solaris 8) and insert the first disk into the cdrom drive. Then, press the "Stop" button and "a" together. This will bring you to the "ok" prompt. Here, type "boot cdrom" and the computer

should restart, booting from the installation disk. The installation prompts will automatically appear, asking for network information.

To network the computer, a user must have a host name, IP address, a subnet mask, a default router address, a domain name, a search domain, and, if the computer is networked using DNS, a list of DNS servers. If the user is starting with a new Sun workstation or is in the process of installing a new operating sytem, the initial startup will ask for this information and will prepare the necessary files. This will most likely be the case, because computers must upgrade to Solaris 9.

However, if your computer has Solaris 9 and is not networked properly, there is a list of files in the root `/etc/` directory to change. These files are `resolv.conf`, `nsswitch.files`, `defaultrouter`, `nodename`, `netmasks`, `hosts`, and `hostname.hme0`. The content of `defaultrouter`, `netmasks`, and `hostname.hme0` is self-explanatory. `nodename` contains the same information as `hostname.hme0` (the hostname). `hosts` contains the "local host" and the log host. The log host is the host name the IP address. The "local host" is specific to your network. `resolv.conf` has the domain name, the namesever (DNS address), the search domain. Once these files are changed, the computer should be networked properly.

- *Add LOIS to the computer*

To add LOIS to our computer, we used a checkout and installation procedure from Brian Taylor.

First, check to make sure that our CVSROOT env variable is set to: `setenv CVSROOT:pserver:loisbelay.lowell.edu:/belay/mirror/cvsroot` in the `.cshrc` file. Then, download the necessary CVS (**C**oncurrent **V**ersioning **S**ystem) program from www.cvshome.org.[2] Next, log in to the CVS server by typing `cvs login` at the command line while in the t-shell. At this step, the computer asks for the CVS password. After giving the correct password, checkout LOIS by entering `Checkout LOIS` at the command line. Once LOIS finishes checking out, run a series of auto build commands in succession from the command line. These commands are `aclocal`,

[2]There are many files required for installing CVS, but we are currently not sure of which files are necessary and which are not. This paper will be appended once this information is acquired.

`automake -a`, and `autoconf`.[3] After the autoconfigure of the LOIS files, configure them. Type `./configure --help` to see the configuring options. Be sure to make the directory `/opt/LOIS/etc` for installation. To see what modules to install, type `more config.site`. We can also add modules from the command line if necessary. After choosing the configure options, type `./configure` with the options listed after the command. Finally, to start the compilation process, type `make`.

- *Testing Electronics Boards*

By referencing the electronics board diagrams in Appendix A and the pinout tables in Chapter 2, we can test the pinouts of the clock driver board and the video processing board. To do this, use a voltmeter with the proper connectors. When the pinouts were tested at Lowell, the voltages matched what the DSP code and board schematics specified they should be and were within the ranges specified by the Leach documentation. We could also test the pinout of the CCD. The CCD pins, shown in Chapter 2, connect to a header board that is mounted into the dewar and wired to the electronics boards.

- *Using LOIS with Electronics Boards*

To startup, first check to see that the orange fiber optic cables are properly connected between the computer and the electronics box. The cables have blue connectors and red connectors. On the electronics box, looking at the face that has the fiber optic ports when it is upright, the blue connector attaches at the right port. On the Ultra 10, looking at the back of the computer when it is upright, the blue connector attaches at the top port. Next, make sure the GL Scientific power supply is connected to the Leach electronics box and is turned on. Finally, we can start LOIS. To start LOIS, make sure that you are in the LOIS directory, established when compiling LOIS, open a terminal window, and enter the commands:

`hostname% xhost` *hostname*

[3]These are the commands that build the makefiles.

```
hostname% lois &
hostname% ds9 &
```

At this point, a LOIS window and a DS9 window will be open. The DS9 is not important until you take an exposure. In the LOIS window, click on the `Configure` button. Here, you select the telescope, the camera, the instrument interface, and the display interface. When we just test the electronics we choose NONE for the telescope and instrument interface, MagIC for the camera, and SAOimage DS9 for the display interface. If the computer is also connected to the telescope, the telescope module can be loaded during the LOIS configure process and we can select our telescope from the list. The same goes for the instrument interface.

After hitting `OK` in the `Configure` window, the camera control screen appears. From this window, we can specify the exposure type, time, binning, and filter. There is also a button to select the AMP, but the button does not work properly.[4,5] On the primary LOIS window, we can select `Storage` to specify where we would like our data stored. Once the user takes the exposure, the image is displayed in the DS9 window. Here, we can carry out preliminary analyses, like finding position estimates and photon counts. Also, it is important to note that the observer may write LOIS scripts that include the exposure time, type, and filter. These scripts are inputted at and executed from the LOIS command line. Details on the proper structure of the scripts can be found in the LOIS Manual. These scipts can also be aborted mid-session using the button on the LOIS control window.

[4]Currently, LCO only supports a quad amp readout, but we can change the amp in the LOIS command line by typing `set_amplifier amp=[A, B, C, D, or ALL]`.

[5]If we change amplifiers and binning too often in a LOIS session, the LOIS window freezes. If this occurs, type `pkill` at the computer terminal command line. This will shut down LOIS and DS9. When restarting, the computer will think it is on the same exposure as it was when the system froze, so we must go to storage and change the name of the first exposure file to the next name in the sequence. (e.g. if we were on date.006, switch to date.007).

Chapter 4

Conclusions and Future Work

This document gives the background for the electronics, hardware, and software for MagIC and the details on how to begin to setup a testbed. However, there are still steps to take in order to complete the testbed.

First, we must finishing setting up LOIS on the Sun Blade 150. Brian Taylor is in the process of writing documentation on the LOIS checkout process, and once that is complete, we will complete our documentation on the LOIS checkout and installation procedure.

The second major task is to retrieve MagIC's engineering chip from Hawaii. Once we have the chip, we can use the pinout diagram to wire to the chip to the header board.[1] The header board can then be mounted in the dewar.

Once the chip is mounted in the dewar and the chip is properly wired to the electronics, we can start to use MagIC at Wallace and to test the chip and electronics. To interface MagIC with the WAO 24" telescope, we will create a LOIS module for the telescope. When we load this module, LOIS will allow us to select the WAO telescope when in the `Configure` window. At this point, we will be able to test MagIC's engineering chip and start to test the electronics and software with real exposures.

[1] We already received a header board from the Carnegie Institute.

Appendix A

Leach Electronics Board Diagrams

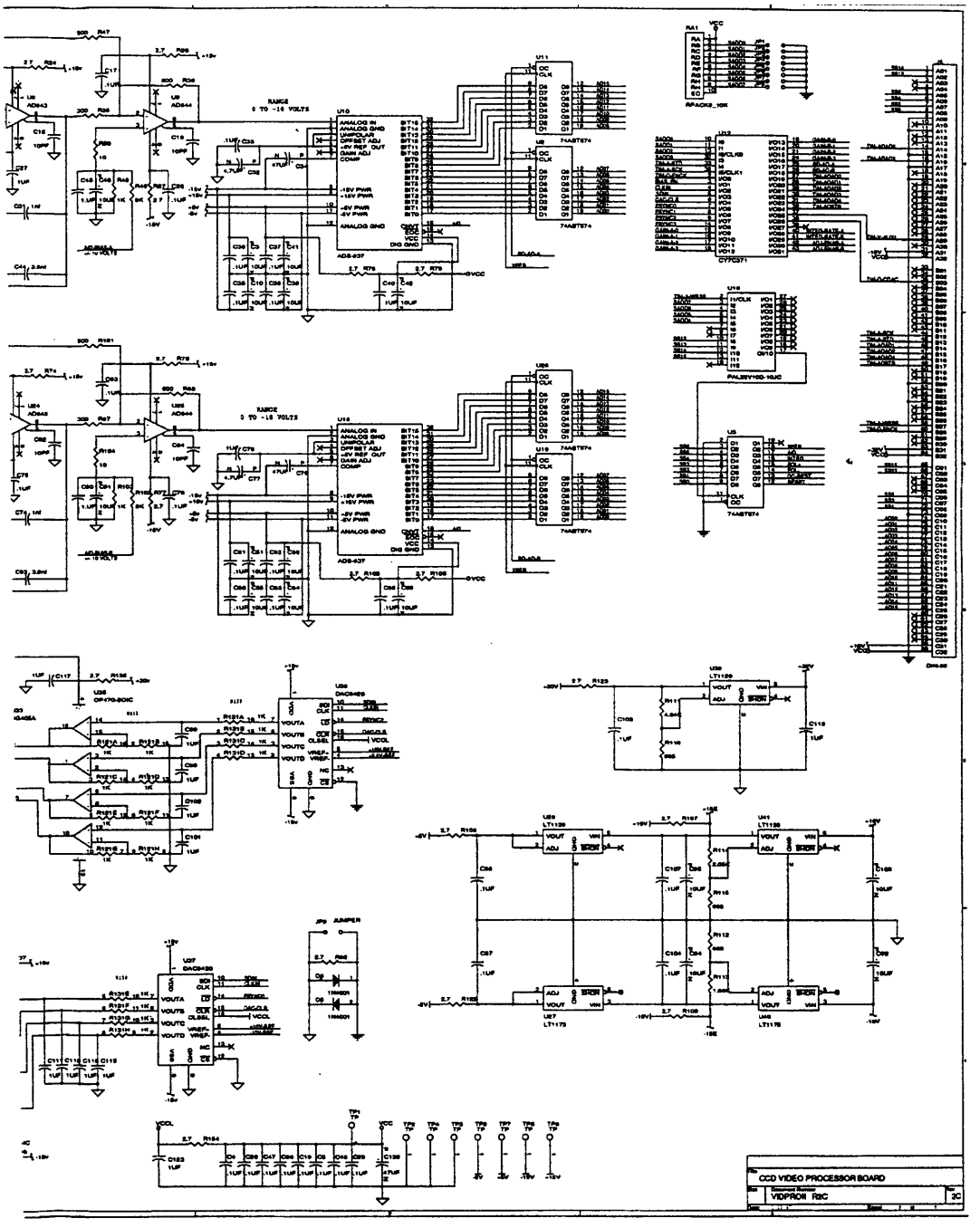


Figure A-1: **Video Processing Board 1.** This is the right half of the video processing board circuit diagram. When compared with the parts diagram in section 2.2.3, we can see how this diagram matches to the large scale part placement. [2]

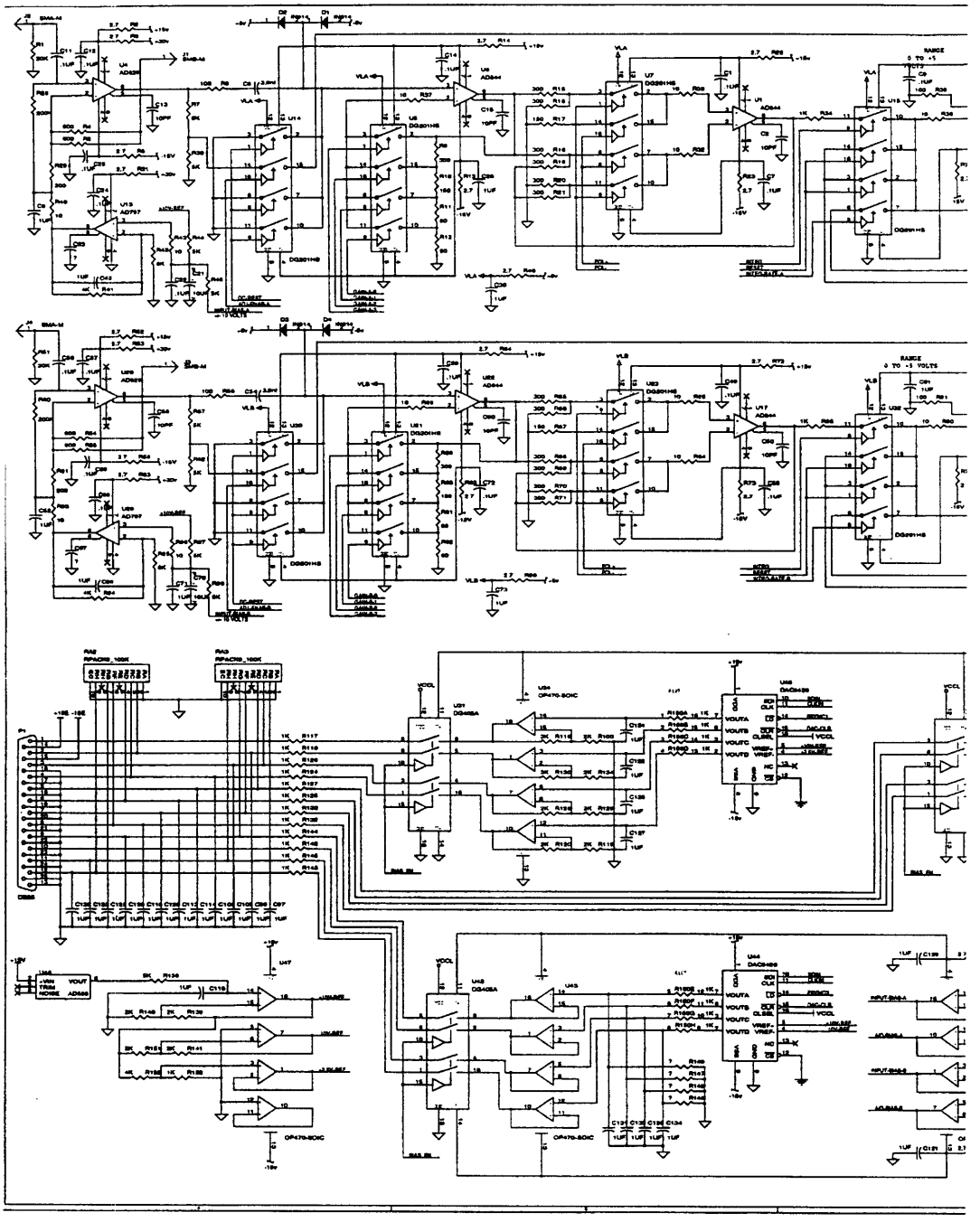


Figure A-2: **Video Processing Board 2.** This is the left half of the video processing board circuit diagram. Again, the diagram can be matched to the more general part placement diagram. On the lower left side, we can see the pinout section of the board. The pinout is shown in closer detail in Figure A-3. [2]

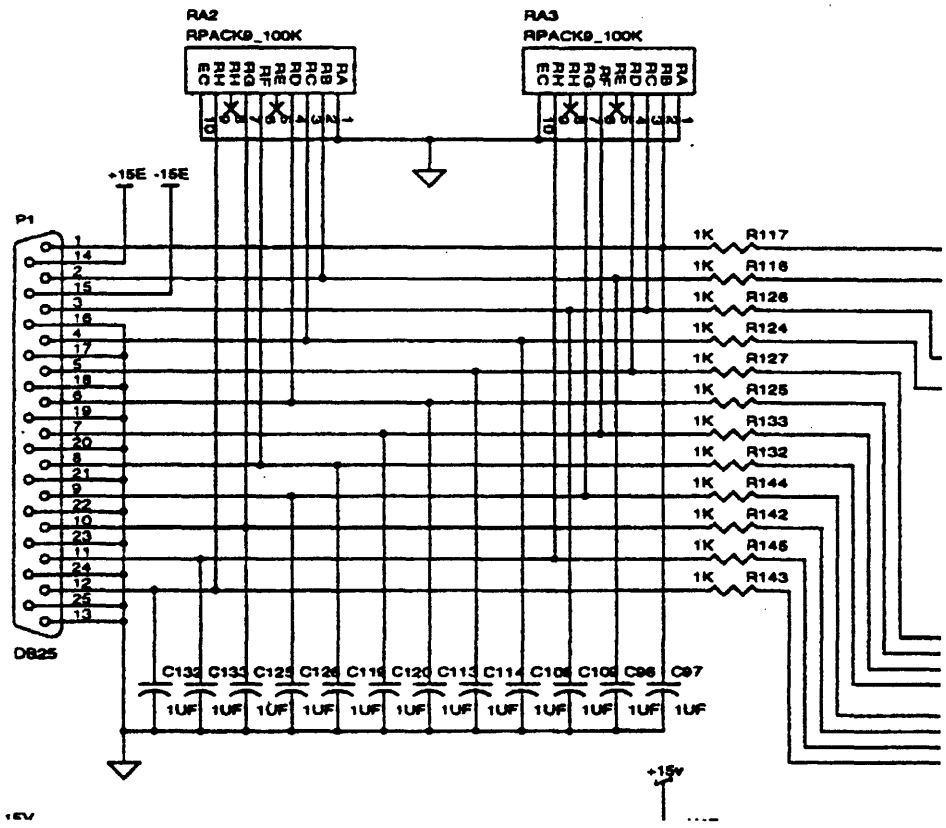


Figure A-3: **Video Processing Board Pinout.** This pinout matches to the pins listed in Table 2.8. [2]

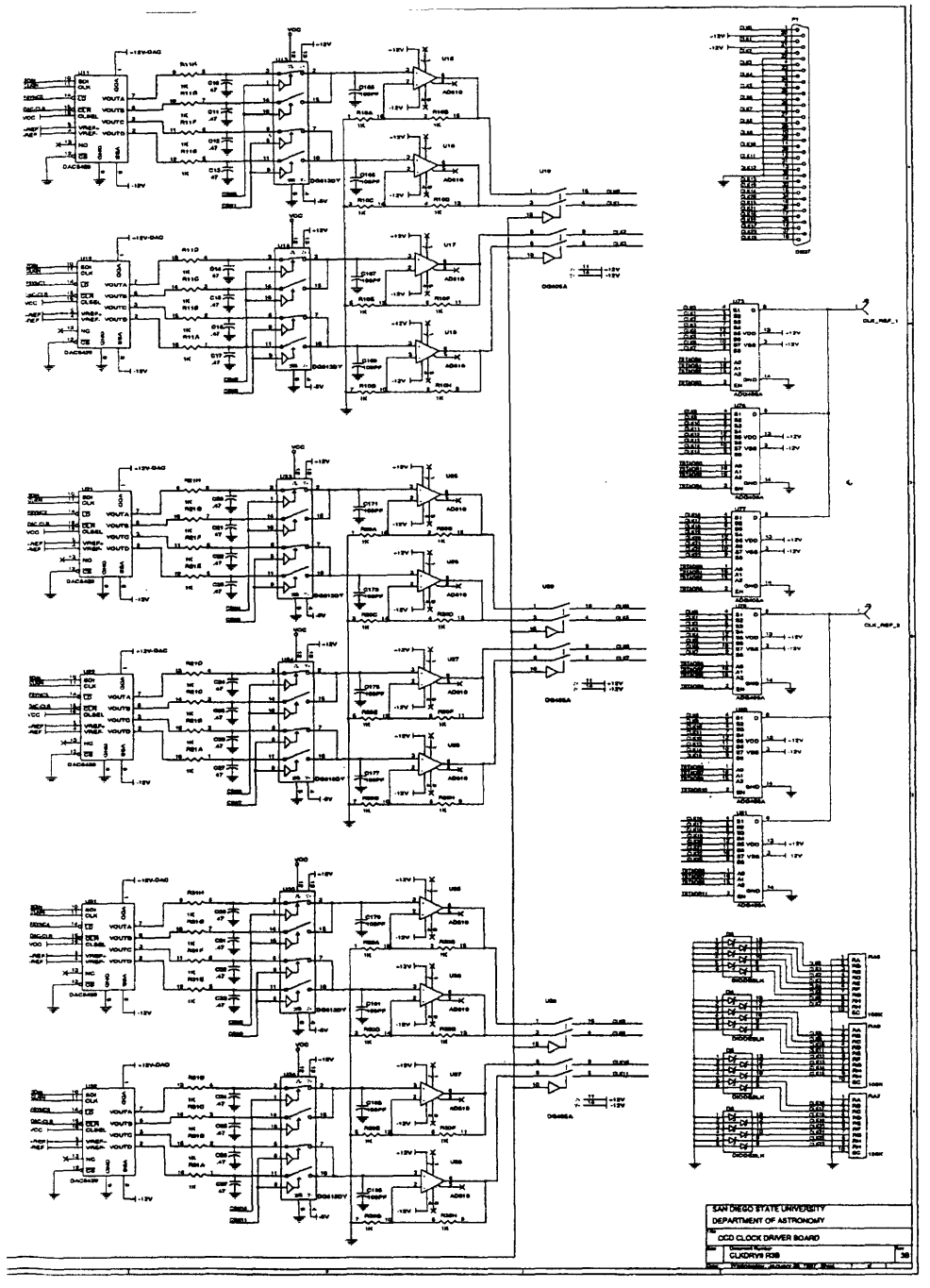


Figure A-4: **Clock Driver Board 1.** This is the right side of the clock driver board circuit diagram. The upper right side shows the pinout for the clock driver board. The pinout is enlarged in Figure A-6. [2]

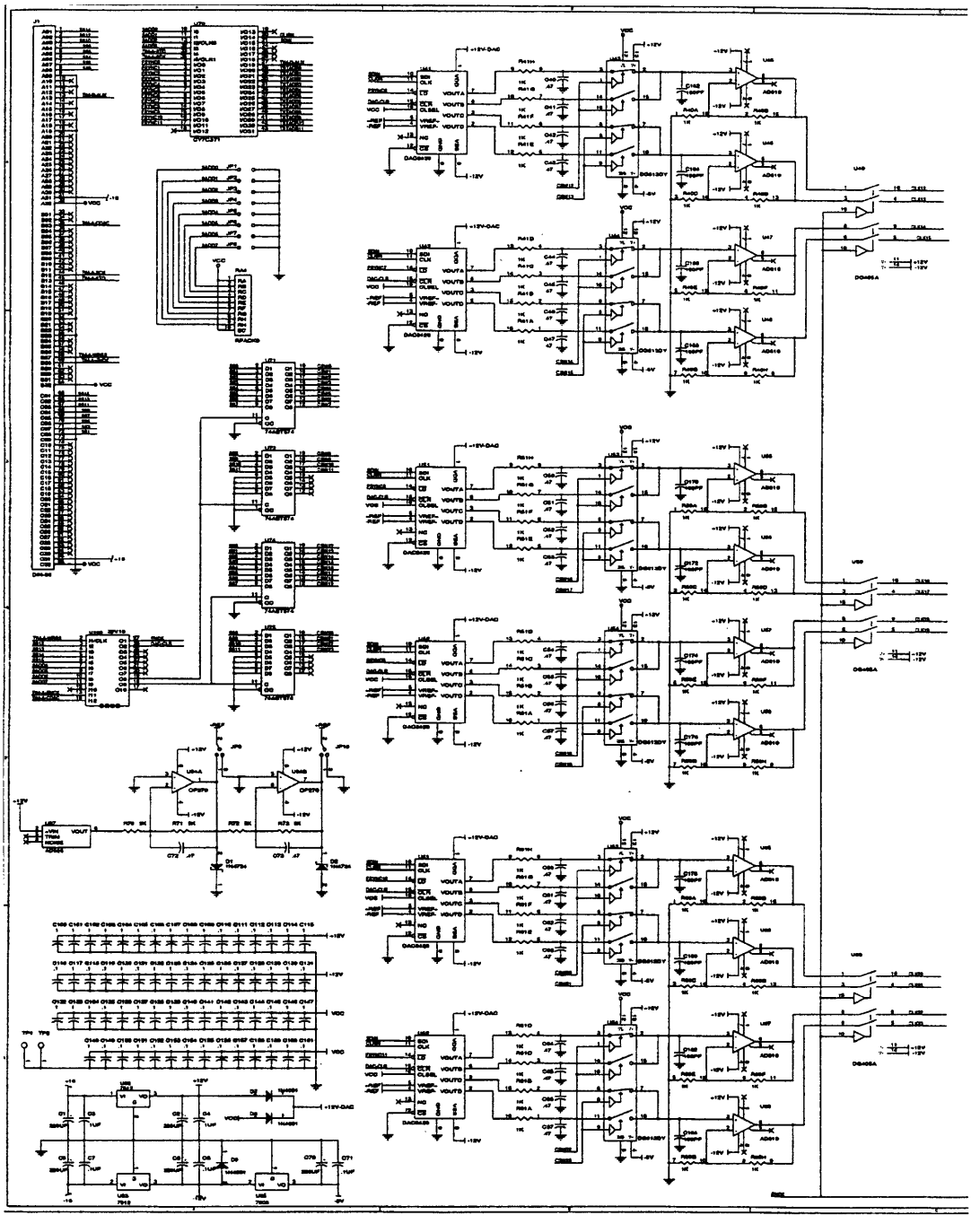


Figure A-5: **Clock Driver Board 2.** This is the left side of the clock driver board circuit diagram. The rows of clocks/DACs is seen along the center of the page. [2]

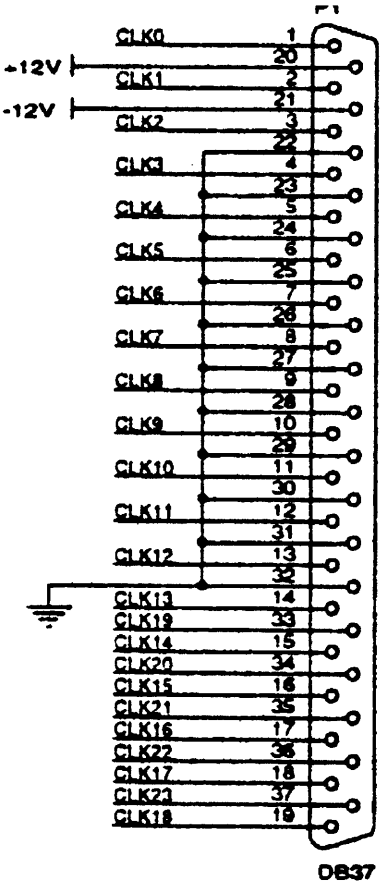


Figure A-6: **Clock Driver Board Pinout.** This pinout corresponds to Table 2.7. [2]

Appendix B

Command Descriptions

These are the generic commands sent from the host computer and executed by the timing board. These commands can be seen in the file tim.asm. The term "controller" refers to the timing board. While running the commands, LOIS will display the controller replies. All successful commands reply with "ASCII DON" and all unsuccessful commands reply with "Err" or "TOUT" (Error or Timeout). [3]

Table B.1: **Timing Board Boot Command Description.** [3]

Timing Board Boot Command Description		
Type	**Symbol**	**Name**
Boot	TDL	Test Data Link
Boot	RDM	Read Memory
Boot	WRM	Write Memory
Boot	LDA	Load Application
Boot	STP	Stop Idling Clocking

Table B.2: **Timing Board Application Command Description.** [3]

Timing Board Application Command Description		
Type	**Symbol**	**Name**
Application	PON	Power On
Application	POF	Power Off
Application	SBV	Set Bias Voltage
Application	IDL	Start Idle Clocking
Application	OSH	Open Shutter
Application	CSH	Close Shutter
Application	RDC	Read CCD
Application	CLR	Clear Array
Application	SET	Set Exposure Time
Application	RET	Read Elapsed Exposure Time
Application	SEX	Start Exposure
Application	PEX	Pause Exposure
Application	REX	Resume Exposure
Application	AEX	Abort Exposure
Application	ABR	Abort Readout
Application	CRD	Continue Readout
Application	SGN	Set Gain
Application	SBN	Set Bias Number
Application	SMX	Set MUX
Application	CSW	Clear Switches
Application	SOS	Select Output Source
Application	SSS	Set Subarray Size
Application	SSP	Set Subarray Position
Application	RCC	Read Controller Configuration

Appendix C

MagIC.waveforms.s DSP Code

The DSP code for MagIC is called MagIC.waveforms.s.

```
This  file contains timing waveforms for the SITe 424 2048 x 2048 pixel CCD

*
PAGE    132     ; Printronix page width - 132 columns

; Definitions of readout variables
SXMIT EQU     $00F060 ; Default is Amplifier C = #0 only
CLK2 EQU $004000 ; Clock driver board lower half
CLK3 EQU $005000 ; Clock driver board upper half
VIDEO EQU $000000 ; Video processor board switches
P_DELAY EQU $FF0000 ;FF Parallel clock delay = maximum FF
S_DELAY EQU $120000 ;12 Serial clock delay 10
INT_TIM EQU $A50000         ; default was A5

; CCD clocking voltages
RG_HI EQU 10.0 ; Reset Gate High
RG_LO EQU  0.0    ;
```

```
S_HI EQU +4.5 ; Serial High +4.5
S_LO EQU -4.5    ; -4.5
SW_HI EQU +5.0 ; Summing Well +5
SW_LO EQU -6.0    ; -6.0

P_HI EQU +1.5 ; Parallel High +1.5
P_LO EQU -7.0    ; -7.0
P3_HI EQU +3.0 ; Parallel Phase 3 High +3.0
P3_LO EQU -7.0    ; -7.0
TG_HI EQU +1.5 ; Transfer Gate High +1.5
TG_LO EQU -7.0    ; -7.0
ZERO EQU  0.0 ; Unused pins

; DC bias voltages
VOD EQU 24.30 ; Output Drain 24.30
VRD EQU 13.50 ; Reset Drain 13.50
VLG EQU -3.5 ; Last gate before the summing well

; Four output video offsets
OFFSET EQU 2250
OFFSET5 EQU     4000
OFFSET0 EQU 3405     ;g1 2301    ;g2 2632 ;g5 3405 ;g10 3493 it93 ;  ll
OFFSET1 EQU 3098     ;g1 2234    ;g2 2503 ;g5 3120 ;g10 3196 it93 ;  lr
OFFSET2 EQU 3341     ;g1 2287    ;g2 2609 ;g5 3349 ;g10 3441 it93 ;  ur
OFFSET3 EQU 3348     ;g1 2297    ;g2 2614 ;g5 3351 ;g10 3393 it93 ;  ul


; Define switch state bits for the CCD clocks - CLK2, which is lower bank
RG0 EQU 1 ; Reset output node #0
RG1 EQU 2 ; Reset output node #1
```

```
RG2 EQU 4 ; Reset output node #2
RG3 EQU 8 ; Reset output node #3

P2L EQU $80 ;10 Parallel shift register phase #1, lower
P2U EQU $40 ;20 Parallel shift register phase #2, upper
P1L EQU $20 ;40 Parallel shift register phase #2, lower
P1U EQU $10 ;80 Parallel shift register phase #1, upper
P3 EQU $100 ; Parallel shift register phase #3, upper and lower

TG EQU $200 ; All transfer gates
S2L EQU $400 ;4 Serial shift register phase #2, lower
S2U EQU $800 ;8 Serial shift register phase #2, upper

; Now for CLK3, which is the upper bank
S10 EQU     1 ;10 Serial shift register phase #1, quadrant #0
S30 EQU 2 ;30 Serial shift register phase #3, quadrant #0
S31 EQU 4 ;31 Serial shift register phase #1, quadrant #1
S11 EQU 8 ;11 Serial shift register phase #3, quadrant #1

S32 EQU $10 ;32 Serial shift register phase #1, quadrant #2
S12 EQU $20 ;12 Serial shift register phase #3, quadrant #2
S13 EQU $40 ;13 Serial shift register phase #1, quadrant #3
S33 EQU $80 ;33 Serial shift register phase #3, quadrant #3

SW0 EQU $100 ; Summing well, quadrant #0
SW1 EQU $200 ; Summing well, quadrant #1
SW3 EQU $400 ; Summing well, quadrant #2
SW2 EQU $800 ; Summing well, quadrant #3

; ****************************************************
```

```
; RG0+RG1+RG2+RG3+P1L+P1U+P2U+P2L+P3+TG+S2L+S2U (CLK2)
; S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3 (CLK3)
; ***************************************************

;  ***  Definitions for Y: memory waveform tables  *****
;  ***  Definitions for Y: memory waveform tables  *****
SERIAL_READ_A
DC SERIAL_READ_B-SERIAL_READ_A-2
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+000+000+000+000
RGH_1 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC VIDEO+$000000+%1110100 ; Change nearly everything
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+SW0+SW1+SW2+SW3
RGL_1 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
SXMIT_A DC SXMIT ; Transmit A/D data to host
DC VIDEO+$000000+%1110111 ; Stop resetting integrator
DC VIDEO+$000000+%1110111 ; Additional settling time
DC VIDEO+INT_TIM+%0000111 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop Integrate
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
DC VIDEO+INT_TIM+%0001011 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop integrate, A/D is sampling

SERIAL_READ_B
```

```
DC SERIAL_SPLIT-SERIAL_READ_B-2
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+000+000+000+000
RGH_2 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+00+000+000
DC VIDEO+$000000+%1110100 ; Change nearly everything
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+SW0+SW1+SW2+SW3
RGL_2 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
SXMIT_B DC SXMIT ; Transmit A/D data to host
DC VIDEO+$000000+%1110111 ; Stop resetting integrator
DC VIDEO+$000000+%1110111 ; Additional settling time
DC VIDEO+INT_TIM+%0000111 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop Integrate
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
DC VIDEO+INT_TIM+%0001011 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop integrate, A/D is sampling

SERIAL_SPLIT
DC SERIAL_IDLE-SERIAL_SPLIT-2
DC CLK3+S_DELAY+S10+000+S12+000+000+S31+000+S33+000+000+000+000
RGH_3 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC VIDEO+$000000+%1110100 ; Change nearly everything
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+S11+000+S13+S30+000+S32+000+SW0+SW1+SW2+SW3
RGL_3 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
```

```
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
SXMIT_AB DC SXMIT ; Transmit A/D data to host
DC VIDEO+$000000+%1110111 ; Stop resetting integrator
DC VIDEO+$000000+%1110111 ; Additional settling time
DC VIDEO+INT_TIM+%0000111 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop Integrate
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
DC VIDEO+INT_TIM+%0001011 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop integrate, A/D is sampling

; Video processor bit definition
;       xfer, A/D, integ, Pol+, Pol-, DCrestore, rst   (1 => switch open)
SERIAL_IDLE DC SERIAL_SKIP_A-SERIAL_IDLE-2
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+000+000+000+000
RGH_4 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC VIDEO+$000000+%1110100 ; Change nearly everything
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+SW0+SW1+SW2+SW3
RGL_4 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
DC VIDEO+$000000+%1110111 ; Stop resetting integrator
DC VIDEO+$000000+%1110111 ; Additional settling time
DC VIDEO+INT_TIM+%0000111 ; Integrate
DC VIDEO+$000000+%0011011 ; Stop Integrate
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000
```

```
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
DC VIDEO+INT_TIM+%0001011 ; Integrate
DC VIDEO+$000000+%0011000 ; Stop integrate, A/D is sampling

; Serial clocking waveform for skipping into amplifier A
SERIAL_SKIP_A
DC SERIAL_SKIP_B-SERIAL_SKIP_A-2
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+000+000+000+000
RGH_5 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+SW0+SW1+SW2+SW3
RGL_5 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000

; Serial clocking waveform for skipping into amplifier B
SERIAL_SKIP_B
DC SERIAL_SKIP_SPLIT-SERIAL_SKIP_B-2
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+000+000+000+000
RGH_6 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+00+000+000
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+SW0+SW1+SW2+SW3
RGL_6 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000
```

```
; Serial clocking waveform for skipping into both amplifiers
SERIAL_SKIP_SPLIT
DC CCD_RESET-SERIAL_SKIP_SPLIT-2
DC CLK3+S_DELAY+S10+000+S12+000+000+S31+000+S33+000+000+000+000
RGH_7 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+S11+000+S13+S30+000+S32+000+SW0+SW1+SW2+SW3
RGL_7 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000

CCD_RESET
DC SERIAL_CLOCK_A-CCD_RESET-2
DC CLK2+$100000+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+00+S2L+S2U
DC CLK2+$100000+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+00+S2L+S2U

SERIAL_CLOCK_A
DC SERIAL_CLOCK_B-SERIAL_CLOCK_A-2
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+SW0+SW1+SW2+SW3
RGH_8 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+SW0+SW1+SW2+SW3
RGL_8 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3

SERIAL_CLOCK_B
DC SERIAL_CLOCK_SPLIT-SERIAL_CLOCK_B-2
DC CLK3+S_DELAY+S10+S11+S12+S13+000+000+000+000+SW0+SW1+SW2+SW3
RGH_9 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
```

```
DC CLK3+S_DELAY+000+000+000+000+S30+S31+S32+S33+SW0+SW1+SW2+SW3
RGL_9 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3

SERIAL_CLOCK_SPLIT
DC VIDEO_PROCESS-SERIAL_CLOCK_SPLIT-2
DC CLK3+S_DELAY+S10+000+S12+000+000+S31+000+S33+000+000+000+000
RGH_10 DC CLK2+S_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+000+000+000+000
DC CLK3+S_DELAY+S10+S11+S12+S13+S30+S31+S32+S33+SW0+SW1+SW2+SW3
DC CLK3+S_DELAY+000+S11+000+S13+S30+000+S32+000+SW0+SW1+SW2+SW3
RGL_10 DC CLK2+S_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+000+000+S2L+S2U
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+SW0+SW1+SW2+SW3

VIDEO_PROCESS
DC END_DSPMEM-VIDEO_PROCESS-2
SXMIT_VIDEO_PROCESS
DC SXMIT ; Transmit A/D data to host
DC VIDEO+$000000+%1110111 ; Stop resetting integrator
DC VIDEO+$000000+%1110111 ; Additional settling time
DC VIDEO+INT_TIM+%0000111 ; Integrate for 1 microsec
DC VIDEO+$000000+%0011011 ; Stop Integrate
DC CLK3+S_DELAY+000+000+000+000+000+000+000+000+000+000+000+000
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
DC VIDEO+$000000+%0011011 ; Delay for signal to settle
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
; DC VIDEO+$000000+%0011011 ; Delay for signal to settle ADDED
DC VIDEO+INT_TIM+%0001011 ; Integrate for another microsec
DC VIDEO+$000000+%0011011 ; Stop integrate, A/D is sampling
DC VIDEO+$000000+%1110100 ; Start A/D, XFER, and more
```

```
END_DSPMEM

DAC_DISP EQU APL_NUM*N_W_APL+APL_LEN+MISC_LEN+COM_LEN+$100

; Put all the following code in SRAM.
IF @SCP("DOWNLOAD","HOST")
ORG Y:$100,Y:$100 ; Download address
ELSE
ORG Y:$100,P:DAC_DISP
ENDIF

PARALLEL_UPPER
DC PARALLEL_LOWER-PARALLEL_UPPER-2
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+P3+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U
DC CLK2+0000000+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U

PARALLEL_LOWER
DC PARALLEL_SPLIT-PARALLEL_LOWER-2
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+P3+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U
```

```
DC CLK2+0000000+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U

PARALLEL_SPLIT
DC PARALLEL_UPPER_MPP-PARALLEL_SPLIT-2
DC CLK2+P_DELAY+000+000+000+000+000+P1U+P2L+000+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+P1U+P2L+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+000+000+P2U+P3+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+000+000+P2U+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U
DC CLK2+0000000+000+000+000+000+P1L+P1U+P2L+P2U+00+00+S2L+S2U

; The following waveforms are for MPP = Multi-Phase-Pinned (low dark current)
PARALLEL_UPPER_MPP
DC PARALLEL_LOWER_MPP-PARALLEL_UPPER_MPP-2
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+P3+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+00+00+S2L+S2U
DC CLK2+0000000+000+000+000+000+000+000+000+000+00+00+S2L+S2U

PARALLEL_LOWER_MPP
DC PARALLEL_SPLIT_MPP-PARALLEL_LOWER_MPP-2
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+P2L+P2U+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+P3+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+P1U+000+000+00+00+S2L+S2U
```

```
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+00+00+S2L+S2U
DC CLK2+0000000+000+000+000+000+000+000+000+000+00+00+S2L+S2U

PARALLEL_SPLIT_MPP
DC PARALLEL_CLEAR-PARALLEL_SPLIT_MPP-2
DC CLK2+P_DELAY+000+000+000+000+000+P1U+P2L+000+00+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+P1U+P2L+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+000+000+P2U+P3+00+S2L+S2U
DC CLK2+P_DELAY+000+000+000+000+P1L+000+000+P2U+00+00+S2L+S2U
DC CLK2+0000000+000+000+000+000+000+000+000+000+00+00+S2L+S2U

PARALLEL_CLEAR
DC DACS-PARALLEL_CLEAR-2
DC CLK2+P_DELAY+RG0+RG1+RG2+RG3+000+P1U+P2L+000+00+00+S2L+S2U
DC CLK2+P_DELAY+RG0+RG1+RG2+RG3+000+P1U+P2L+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+RG0+RG1+RG2+RG3+000+000+000+000+P3+TG+S2L+S2U
DC CLK2+P_DELAY+RG0+RG1+RG2+RG3+P1L+000+000+P2U+P3+00+S2L+S2U
DC CLK2+P_DELAY+RG0+RG1+RG2+RG3+P1L+000+000+P2U+00+00+S2L+S2U
DC CLK2+P_DELAY+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+00+00+S2L+S2U
DC CLK2+0000000+RG0+RG1+RG2+RG3+P1L+P1U+P2L+P2U+00+00+S2L+S2U


; Initialization of clock driver and video processor DACs and switches
DACS DC END_EXTMEM-DACS-1
DC (CLK2<<8)+(0<<14)+@CVI((RG_HI+10.0)/20.0*4095)
; RG #0 High
DC (CLK2<<8)+(1<<14)+@CVI((RG_LO+10.0)/20.0*4095)
; RG #0 Low
DC (CLK2<<8)+(2<<14)+@CVI((RG_HI+10.0)/20.0*4095)
```

```
; RG #1 High
DC (CLK2<<8)+(3<<14)+@CVI((RG_LO+10.0)/20.0*4095)
; RG #1 Low
DC (CLK2<<8)+(4<<14)+@CVI((RG_HI+10.0)/20.0*4095)
; RG #2 High
DC (CLK2<<8)+(5<<14)+@CVI((RG_LO+10.0)/20.0*4095)
; RG #2 Low
DC (CLK2<<8)+(6<<14)+@CVI((RG_HI+10.0)/20.0*4095)
; RG #3 High
DC (CLK2<<8)+(7<<14)+@CVI((RG_LO+10.0)/20.0*4095)
; RG #3 Low

DC (CLK2<<8)+(8<<14)+@CVI((P_HI+10.0)/20.0*4095)
; P1L High
DC (CLK2<<8)+(9<<14)+@CVI((P_LO+10.0)/20.0*4095)
; P1L Low
DC (CLK2<<8)+(10<<14)+@CVI((P_HI+10.0)/20.0*4095)
; P2U High
DC (CLK2<<8)+(11<<14)+@CVI((P_LO+10.0)/20.0*4095)
; P2U Low
DC (CLK2<<8)+(12<<14)+@CVI((P_HI+10.0)/20.0*4095)
; P2L High
DC (CLK2<<8)+(13<<14)+@CVI((P_LO+10.0)/20.0*4095)
; P2L Low
DC (CLK2<<8)+(14<<14)+@CVI((P_HI+10.0)/20.0*4095)
; P1U High
DC (CLK2<<8)+(15<<14)+@CVI((P_LO+10.0)/20.0*4095)
; P1U Low
DC (CLK2<<8)+(16<<14)+@CVI((P3_HI+10.0)/20.0*4095)
; P3 High
```

```
DC (CLK2<<8)+(17<<14)+@CVI((P3_LO+10.0)/20.0*4095)
; P3 Low
DC (CLK2<<8)+(18<<14)+@CVI((TG_HI+10.0)/20.0*4095)
; TG High
DC (CLK2<<8)+(19<<14)+@CVI((TG_LO+10.0)/20.0*4095)
; TG Low

DC (CLK2<<8)+(20<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S2L High
DC (CLK2<<8)+(21<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S2L Low
DC (CLK2<<8)+(22<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S2U High
DC (CLK2<<8)+(23<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S2U Low

DC (CLK2<<8)+(24<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S10 High
DC (CLK2<<8)+(25<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S10 Low
DC (CLK2<<8)+(26<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S30 High
DC (CLK2<<8)+(27<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S30 Low
DC (CLK2<<8)+(28<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S11 High
DC (CLK2<<8)+(29<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S11 Low
DC (CLK2<<8)+(30<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S31 High
```

```
DC (CLK2<<8)+(31<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S31 Low

DC (CLK2<<8)+(32<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S12 High
DC (CLK2<<8)+(33<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S12 Low
DC (CLK2<<8)+(34<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S32 High
DC (CLK2<<8)+(35<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S32 Low
DC (CLK2<<8)+(36<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S13 High
DC (CLK2<<8)+(37<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S13 Low
DC (CLK2<<8)+(38<<14)+@CVI((S_HI+10.0)/20.0*4095)
; S33 High
DC (CLK2<<8)+(39<<14)+@CVI((S_LO+10.0)/20.0*4095)
; S33 Low

DC (CLK2<<8)+(40<<14)+@CVI((SW_HI+10.0)/20.0*4095)
; SW0 High
DC (CLK2<<8)+(41<<14)+@CVI((SW_LO+10.0)/20.0*4095)
; SW0 Low
DC (CLK2<<8)+(42<<14)+@CVI((SW_HI+10.0)/20.0*4095)
; SW1 High
DC (CLK2<<8)+(43<<14)+@CVI((SW_LO+10.0)/20.0*4095)
; SW1 Low
DC (CLK2<<8)+(44<<14)+@CVI((SW_HI+10.0)/20.0*4095)
; SW2 High
```

```
DC (CLK2<<8)+(45<<14)+@CVI((SW_LO+10.0)/20.0*4095)
; SW2 Low
DC (CLK2<<8)+(46<<14)+@CVI((SW_HI+10.0)/20.0*4095)
; SW3 High
DC (CLK2<<8)+(47<<14)+@CVI((SW_LO+10.0)/20.0*4095)
; SW3 Low

; Set gain and integrator speed. (77, bb, dd, ee; low gain to high)
DC $0c3f77 ; Gain, fast integrate, board #0
DC $1c3f77 ; Gain, fast integrate, board #1
; DC $0c3c77 ; x1 Gain, slow integrate, board #0
; DC $1c3c77 ; x1 Gain, slow integrate, board #1

; DC $0c3cbb ; x4.75 Gain, fast integrate, board #0
; DC $1c3cbb ; x4.75 Gain, fast integrate, board #1

; Input offset voltages for DC coupling. Target is U4#6 = 24 volts
DC $0c0800 ; Input offset, ch. A
DC $0c8800 ; Input offset, ch. B
DC $1c0800 ; Input offset, ch. A, bd. #1
DC $1c8800 ; Input offset, ch. B, bd. #1

; Output offset voltages to get about 1000 ADUs on a bias frame
DC $0c4000+OFFSET0 ; Output video offset, Output C
DC $0cc000+OFFSET1 ; Output video offset, Output D
DC $1c4000+OFFSET2 ; Output video offset, Output B
DC $1cc000+OFFSET3 ; Output video offset, Output A


; Output drain DC supply voltages
```

```
DC $0d0000+@CVI((VOD-7.5-0.1)/22.5*4095) ; Vod #0, pin #1, VID0
DC $0d4000+@CVI((VOD-7.5-0.2)/22.5*4095) ; Vod #1, pin #2, VID0
DC $1d0000+@CVI((VOD-7.5-0.4)/22.5*4095) ; Vod #2, pin #1, VID1
DC $1d4000+@CVI((VOD-7.5)/22.5*4095) ; Vod #3, pin #2, VID1

; Reset drain
DC $0d8000+@CVI((VRD-5.0)/15.0*4095) ; Vrd, pin #3, VID0
DC $0dc000+@CVI((VRD-5.0)/15.0*4095) ; Vrd, pin
#4, VID0 added

; Last gates
DC $0f0000+@CVI((VLG+5.0)/10.0*4095) ; Vlg #0 =
-3.5V pin #9, VID0
DC $0f4000+@CVI((VLG+5.0)/10.0*4095) ; Vlg #1 =
-3.5V pin #10, VID0
; DC $1f0000+@CVI((VLG+5.0)/10.0*4095) ; Vlg #0 =
-3.5V pin #9, VID1
; DC $1f4000+@CVI((VLG+5.0)/10.0*4095) ; Vlg #1 =
-3.5V pin #10, VID1


; DPS voltage for entire CCD
         DC      $0f80CC                                    ; VDPS 0CC
=-9.0v pin #11 VID0 added



END_EXTMEM

; Check for overflow in the EEPROM case
```

```
IF @SCP("DOWNLOAD","EEPROM")
IF @CVS(N,@LCV(L))>(APL_NUM+1)*N_W_APL
WARN    'EEPROM overflow!'; Make sure the next application
ENDIF ;  will not be overwritten
ENDIF
```

Appendix D

Documentation URLs and Server Locations

Leach Electronics

http://mintaka.sdsu.edu/ccdlab/LabMain.html

(For the main manual and some board information)

astron:local:projects:active:MagIC:documentation:electronics

(For information on the timing board, clocking board, video processing board, and command descriptions)

SI424A CCD

http://www.site-inc.com/index2.html

SITe manual and quantum efficiency information

(Hard copy documentation)

LOIS

astron:local:projects:active:MagIC:documentation

http://www.lowell.edu/Research/telescopes.html

(For LOIS Manual MagIC 3.1 and LOIS Explanatory Supplement)

SAOimage DS9

http://hea-www.harvard.edu/RD/ds9

(For DS9 background and beta versions)

Lowell Observatory

http://www.lowell.edu

MagIC Homepage

http://occult.mit.edu/instrumentation/magic

LCO Homepage

http://www.lco.cl

CVS

http://www.cvshome.org

Sun http://sunfreeware.com

(For Sun software)

http://www.sun.com

For Sun hardware

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[2] Leach Electronics. Circuit board diagrams. SDSU CCDLab- on file.

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[5] James Elliot. Development of the MIT Auxiliary Nasmyth Instantly Accessible Camera (MANIAC) for the Magellan i 6.5-Meter Telescope Cover Sheet. February 1999.

[6] James Elliot. Development of the MIT Auxiliary Nasmyth Instantly Accessible camera (MANIAC) for the Magellan I 6.5-Meter Telescope Project Summary. February 1999.

[7] Bob Leach and Ken Salvestrini. *Optical and Infrared Camera Electronics User's Manual.* San Diego State Astronomy CCD Lab, San Diego, CA, generation ii edition.

[8] Gabriel Martin. Emails on gain and read-noise. 3 April, 2004.

[9] Lowell Observatory. Lois explanatory supplement.

[10] Lowell Observatory. LOIS Manual for MagIC. Version 3.1.

[11] David Osip. Emails on the status of MagIC. 2 March, 2001 & 16 March, 2001.

[12] Inc. Scientific Imaging Technologies. SI424A S/N 99061AABR02-01, SI424AB4-0 CCD information.

[13] Scientific Imaging Technologies, Inc., Beaverton, OR. *SITe 2048 x 2048 Scientific-Grade CCD.* On file at MIT.

[14] Brian Taylor. Emails describing the leach electronics system. 26 April, 2004 - 29 April, 2004.