Integrated Thin Film Batteries on Silicon

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ABSTRACT

Monolithic integration has been implemented successfully in complementary metal oxide semiconductor (CMOS) technology and led to improved device performance, increased reliability, and overall cost reduction. The next element to be incorporated on the silicon chip is the power unit; possibly as part of the back end process of the very large scale integrated (VLSI) circuits' production. This thesis describes the work done in developing and studying thin film integrated lithium ion batteries compatible with microelectronics with respect to the material system employed, the cells' fabrication methods, and performance.

The project consisted of three stages; first, a material system new to the battery application field was explored and power cells were fabricated and characterized. In the second stage, the fabrication process of the first material system cells was optimized thereby improving their performance. The third stage dealt with a more conventional battery material system, utilizing thin film technology to fabricate and explore power cells. All the cells fabricated in this work were created using microelectronic technology and were characterized by thin film analysis techniques and by measurement equipment commonly used for microelectronic device testing. The cells were fabricated in four sizes of active areas: 5×5 mm^2, 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2.

The first material system consisted of a novel lithium-free electrolyte in the form of an ultra-thin SiO_2 layer, thermally grown from sacrificial polysilicon layer on a doped polysilicon anode. The concept of SiO_2 as an electrolyte is innovative since common solid state lithium and lithium ion batteries consist of 1-2 μm thick lithium-containing electrolytes. The controlled transport of lithium through SiO_2, 9-40 nm thick, was studied for electrolyte application. The fabricated $LiCoO_2/SiO_2$/polysilicon cells were successfully charged and discharged. This stage of the project demonstrated the concept of an ultra-thin lithium free electrolyte layer and introduces SiO_2 as an interesting candidate material.

The second stage of the project focused on improving the $LiCoO_2/SiO_2$/polysilicon cell's performance and optimizing its fabrication process. Chemical mechanical polishing (CMP), a typical planarization method in microelectronics, new to the battery application field, was introduced in order to enhance the cell's properties and performance. $LiCoO_2/SiO_2$/polysilicon cells consisting of SiO_2 layers 7-40 nm thick were studied. Cells with the planarized polysilicon anode were

characterized and the planarization effect was evaluated. This stage demonstrates the importance of interfacial quality in thin film batteries and the advantages incorporation of CMP as a planarization step in the fabrication process.

Finally, the third stage of the project focused on applying the thin film technology knowledge and expertise to a more commonly used material system V_2O_5/LiPON/$LiCoO_2$. With the aim of reducing interfacial roughness, a surface morphology study of V_2O_5 was performed, tailoring different deposition conditions and surface morphology. Implementing the optimized conditions obtained from this analysis, a V_2O_5/LiPON/$LiCoO_2$ rocking-chair battery was studied next. The cells consisted of approximately 100 or 350 nm thick lithium phosphorus oxynitride (LiPON) electrolyte. This stage demonstrated the advantage of thin film technology in reducing film thickness and the performance enhancement achieved.

The work described in this thesis approached the thin film battery subject from the microelectronic perspective, in order to "bring the battery into the clean room".

Thesis Supervisor: Eugene A. Fitzgerald,
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I wish that my dad were alive to witness my graduation. I would like to dedicate this thesis to my family and to the memory of my father.

1 Introduction

1.1 Motivation and Objectives

Silicon complementary metal oxide semiconductor (CMOS) technology has significantly advanced by implementing integration of various electronic circuit elements onto a single chip. Examples of successful integration of novel electronic and optoelectronic components with silicon integrated circuits, as demonstrated by the Fitzgerald group at MIT include germanium p-type metal oxide semiconductor field effect transistors (MOSFETs)[1] silicon germanium on insulator (SGOI) for high speed and low power applications[2], optical links of GaAs PIN light emitting diode (LED) and detector diodes[3], as well as $Al_xGa_{1-x}As/In_xGa_{1-x}As$ LEDs and lasers[4]. It is natural to consider what system-level function may be integrated next onto the silicon CMOS platform. One important remaining integration challenge is to incorporate the energy source, initially as part of the global power supply, onto the silicon chip. This requires the development of a thin-film solid state battery, compatible with silicon IC technology in terms of fabrication methods, materials, and performance. The low power requirements of CMOS-technology-based devices have allowed for new materials to be considered for battery applications, materials that are compatible with microelectronic technology but are rather innovative to the battery industry. The objective of this work was to develop such a thin-film integrateable battery in three stages. The first stage goal was to develop a power cell by introducing a new materials system to this field of applications, and to use microelectronics technology to fabricate it. This integrateable battery consisted of reduced thicknesses compared to the common battery. The second stage of the project focused on characterizing and studying the developed cell as well as optimizing the fabrication process by addressing materials and processing issues. Finally, the third stage concentrated on implementing the developed process and thin films related expertise to a more conventional solid state battery materials system.

1.2 Organization of Thesis

This work focused on developing an integrated thin film battery on silicon, approaching the subject from the microelectronic perspective. This work utilizes materials compatible with silicon integrated circuit (IC) technology and employs processing methods and characterization techniques typical of thin-film and silicon ICs in order to "bring the battery into the clean room". Chapter 2 gives an overview and literature survey on solid-state lithium and lithium-ion batteries. The materials used for the different battery functions are compared with respect to their performance and deposition methods. Chapter 3 details the material systems selected for the different stages of the project and gives a broader background on these materials. Chapter 4 describes some early material characterization results as well as the experimental procedures and the characterization methods used in this research. Chapter 5 presents the $LiCoO_2/SiO_2$/polysilicon cells containing SiO_2 as thin as 9 nm as the electrolyte layer. The charge and discharge behavior of the cells is studied at different active areas and different charging rates. Impedance measurements and a circuit model of the cell are presented, and the appearance of precipitates on the polysilicon surface is discussed. In this chapter, the concept of ultra-thin SiO_2 as a lithium-free electrolyte is presented and results supporting this concept are shown. Chapter 6 reports the application of microelectronics technology to optimize the $LiCoO_2/SiO_2$/polysilicon cells and, in particular, the interfacial roughness of the cells. The application of chemical mechanical polishing (CMP) to planarize the polysilicon anode is described. The planarization step was found to significantly improve the cell's performance and supporting data are shown. Chapter 7 examines the second material system which is the more conventional battery compatible material system. A thin-film V_2O_5/LiPON/$LiCoO_2$ rocking chair battery is fabricated and characterized using microelectronic compatible technology. The cells described in Chapter 7 consist of lithium phosphorus oxynitride (LiPON) electrolyte as thin as 100 nm and the overall thickness of the cell, of the electrodes and the electrolyte, is as thin as 0.55 μm. The potential gain from the electrolyte thickness reduction is demonstrated. A theoretical calculation presented in this chapter shows that a significant weight and thickness reduction, as well as a possible performance enhancement, can be

achieved compared to a commercial lithium-ion battery. In addition, the practical aspect of on-chip power integration is examined. Finally, a summary of the results and conclusions are presented in Chapter 8, along with suggestions for future work and applications.

2 Background and Literature Review

2.1 Batteries

A battery is an electrochemical cell supplying power by converting chemical energy to electrical energy. A battery consists of two electrodes and an electrolyte. The electrodes are referred to as the anode and the cathode and they are primarily electronic conductors. The electrolyte is dominantly an ionic conductor and an electronic insulator. Electric current is produced in a battery when a neutral atom or molecule becomes ionic by transferring an electron, which is released to the outside circuit, through an oxidation reaction, and passes through the electrolyte to the cathode where a reverse electron-transfer occurs via a reduction reaction. The change in charge carrier type between the electrodes and the electrolyte is forcing the electron transfer reactions at the electrode/electrolyte interfaces. This process for a basic electrochemical cell is depicted schematically in Figure 2-1. Obtaining energy through reduction/oxidation reactions is referred to as discharging the cell and the reverse action of investing energy to drive the ions back to the anode is referred to as 'charging.' The driving force for the reduction oxidation reaction is the difference in the chemical potential of the transferred chemical element between the electrodes or in the case of two metal electrodes, the chemical potential difference between those two metals.

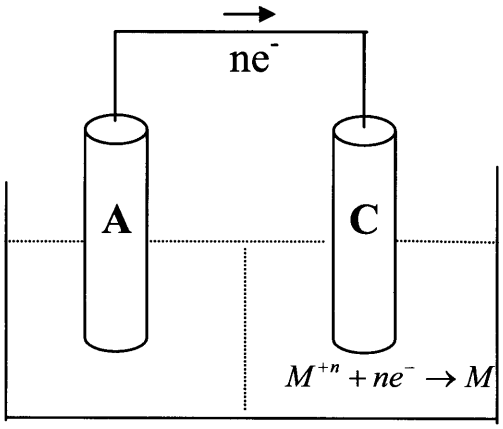


Figure 2-1: Schematic description of a basic electrochemical cell

A distinction should be made between two basic types of cells: the non-rechargeable battery, which supplies energy during one discharge and is referred to as a primary battery, and the rechargeable battery which is a secondary battery.

2.2 Solid-State Batteries

The first electrochemical cell was discovered by Volta in 1800. Since the early days of the lead-acid battery of the end of the 19th century, batteries have come a long way; Ni-Cd, Ni-H and lithium batteries are all nowadays commercially available and used for cars, watches, portable phones and computers, credit cards, cameras, cardiac pacemakers, and more[5].

The battery industry, as part of the general trend to scale down dimensions in various technology applications, is striving towards smaller dimensions with high energy densities. High energy densities can be achieved by reducing the weight of the battery or by increasing the level of energy exchange in the electrochemical cell or both. The application for the power cell dictates the energy density requirements.

The electrolyte is an ionic conductor and an electronic insulator. In commercially available batteries the electrolyte is often an acidic or alkaline solution containing dissolved metal ions or an organic solvent consisting of salts with the relevant ions. Among the merits of a liquid electrolyte are its perfect contact with the electrodes, high ionic conductivity and high electronic resistance. Liquid electrolyte- containing cells suffer from corrosion of their electrodes. In addition, aqueous electrolytes are problematic due to consumption of the water contained in the solvent by electrolysis, a phenomenon which occurs during recharge in the secondary batteries. Due to safety, environmental and stability issues, the liquid electrolyte containing battery requires a hermetic and heavy form of packaging. However, due to gaseous products of corrosion and electrolysis side reactions, the packaging cannot be entirely sealed since that would create a safety hazard. Additionally, this packaging adds weight and reduces the gained energy density of the battery. In addition to the safety issue, in aqueous electrolytes containing cells, the electrolysis process imposes an upper limit on the cell voltage to be approximately 1.23 V[5,6].

A solid-state electrolyte is an electronically insulating solid phase material with high ionic conductivity, i.e. low electronic transfer number, t_e. For a single-ion conductor, t_e is described in Equation 2-1, where σ_e and σ_i are the electronic and ionic conductivities respectively.

$$t_e = \frac{\sigma_e}{\sigma_i + \sigma_e} \qquad \textbf{Equation 2-1}$$

The change in the Gibbs free energy involved in the process of a battery discharge is given by:

$$-\Delta G = nFV_{OC} \qquad \textbf{Equation 2-2}$$

Where n is the number of exchanged electrons that is equal to the valence of the positive ion, F is the Faraday constant = 96487 C/mol (1 mole of charge) and V_{OC} denotes the open circuit voltage (OCV) or the electromotive force, which is given by the potential difference between the two electrodes[5].

The theoretical value of the achievable energy from an electrochemical cell is given by:

$$E_{th} = xnFV_{OC} \qquad \textbf{Equation 2-3}$$

Where x is the number of moles taking part in the reaction[5].

A high-quality solid-state electrolyte, in addition to being a good single-ion conductor, must wet the electrode surfaces to establish good contact and its chemical stability against the electrodes materials should be high. Higher energy densities are potentially obtainable in an all solid-state battery; however, issues such as low electronic transference number of the electrolyte, the quality of its contact with the electrodes, and interfacial quality are still being addressed today[5].

2.3 Lithium and Lithium Ion Batteries

Due to its favorable characteristics, lithium is one of the most common active chemical elements in existing solid-state batteries. In this section, a literature survey of the different lithium and lithium-ion power cell functions, materials, their deposition methods, and properties is presented.

2.3.1 The Anode

The anode is the ion source. It is where oxidation reactions take place and products are released; the ions to the electrolyte and the electrons to the external circuit. The anode is electronically conductive and supplies ions that diffuse rapidly through the electrolyte. Therefore, a desired anode will be made of a light metal or light metal-containing compound with low electronegativity and high electronic conductivity.

Lithium is an excellent choice for the active element in a battery due to its low molecular weight (6.94 g/mole), its small ionic size (1.25 Å covalent radius), and low electronegativity (0.98 Pauling's). Elemental lithium is a common anode material choice in solid-state batteries. In batteries containing a liquid electrolyte, usually a lithium foil is employed[7-17]. In solid state batteries the lithium anode film is often grown by means of thermal evaporation[18-22]. Balkanski *et al.* used molecular beam deposition (MBD) for the lithium anode film[23]. Metallic lithium melts at 180.7°C and is highly reactive and sensitive to nitrogen and moisture, thus using elemental lithium as an anode is a potential safety risk. Consequently, a large volume of research has been done on alternative anode materials to the elemental reactive lithium in batteries.

Commercial batteries employ a graphite anode, sometimes mixed with carbon black, in which lithium is intercalated in the layered structure to form Li_xC_6[24-26]. Contestabile *et al.* dealt with environmental recycling of battery materials testing on a commercial battery with a non-graphitized carbon anode, LiC_x[27].

Extensive work has been done on lithium-metal or lithium-semiconductors alloys as anode materials. Reports of studies done on: Li-Zn, Li-Cd, Li-Pb, Li-Bi, Li-Sb, Li-Al,

Li-Sn, Li-Au, Li-Ag, Li-Cu, Li-Ge, and Li-Si can be found [28-40]. Previous work done on the Li-Si system will be described in more detail in Section 3.1.2.

Anodes made of lithium-metal or semiconductor alloys are usually prepared electrochemically[28,30,31,38] or by melting one or both elements and mixing them[32,33,39,40]. Alloys of lithium with metals or semiconductors offer higher capacity density than the commercially available graphite-lithium intercalation compounds. For example, in the Li-Sn system, $Li_{4.4}Sn$ exhibit specific capacity of 710 mAh/g versus 370 mAh/g for LiC_6[24]. However, the formation and decomposition of metal or semiconductor alloys with lithium involve large volume changes that lead to stresses, cracks, capacity loss, and failure of the electrode.

In search of ways to avoid dealing with these instabilities, other alternative groups of materials for the anode function have been investigated. Among these are carbon with nano-silicon particles prepared by mixing powders,[41] and intermetallic or III-V compounds such as Cu_6Sn_5, AlSb, and InSb, made by ball milling. The latter have been reported to exhibit little volume expansion compared to lithium-metal anodes and showed average reversible specific capacity of 170, 150, and 270 mAh/g respectively[42]. Another studied group of potential anode materials in lithium ion batteries is the silicides. Anodes from $CrSi_2$, Mg_2Si, $CaSi_2$, $CoSi_2$, $FeSi_2$, and $NiSi_2$ were prepared by a reaction with lithium while heated or by mixing the electroactive material with a binder and a dopant followed by coating and annealing[43,44]. Si-V electrode sputtered films were also evaluated by Lee *et al*[45]. Examples of silicides delithiation obtained capacities are 198 mAh/g for $NiSi_2$ and 320 mAh/g for $CaSi_2$[43].

Bates *et al.* explored a couple of nitride anodes, Sn_3N_4 and Zn_3N_2, by sputtering tin and zinc targets respectively in N_2 atmosphere. When testing these anodes electrochemically, they observed capacity loss occurring upon cycling[46]. Silicon-tin oxynitride (SiTON) prepared by sputtering $SnSiO_3$ in an N_2 atmosphere, with a typical composition of $SiSn_{0.87}O_{1.20}N_{1.72}$, was another investigated compound. The SiTON anode suffered from capacity loss upon the first cycle due to the formation of Li_3N and Li_2O by lithium trapping, however, exhibited capacity density of 450 mAh/g[46,47] . Li *et al.* tested SnO prepared by mechanical ball milling as a possible anode material and reported discharge capacity density of 1560 mAh/g that decreased after the first cycle due to

irreversible Li_2O formation[48]. Other metal oxide anodes such as: CoO, CuO, NiO, and FeO were studied by Poizot *et al.* who reported capacities as high as 700 mAh/g[49]. A system composed of a mixed powder of graphite and silicon encapsulated in a Si-O network formed by sol-gel was used by Ng *et al.* They reported discharge capacity density of approximately 500 mAh/g which decreased upon further cycling[50].

Transition metal oxides are traditionally used as cathodes, however, when lithiated, they can serve as anodes as well. In a 'rocking chair' battery, the lithium ions are transferred back and forth between two intercalation compounds, typically two transition metal oxide electrodes. For $Li_xV_2O_5$ against V_2O_5, good cycability was reported[8,51]. Other reported rocking chair systems comprised of: $Li_xFe_xO_3$, Li_xWO_2[52] or $LiMnO_4$[53] as anodes against V_2O_5. Another group of anode materials mentioned in the literature is the spinel structured oxides. Examples for compounds of that group are: $Li_4Ti_5O_{12}$, $Li_4Mn_5O_{12}$, and $Li_2Mn_4O_9$ all prepared by solid state reactions with theoretical capacity densities of 168, 156, and 202 mAh/g, respectively[54,55]. A "lithium free" battery was reported by Bates *et al.* and consisted of a $LiCoO_2$ cathode as the lithium source while the copper current collector was deposited directly on top of the electrolyte layer. Upon cycling, lithium was plated and stripped beneath the copper layer[46].

Table 2-1 compares some of the anode materials presented in this section with respect to their properties and issues involved in their usage:

Anode Material	**Group**	**Capacity [mAh/g]**	**Issues**
$Li_{21}Si_5$	Li-semiconductor	1967	Volume changes
$Li_{22}Sn_5$	Li-metal	710	Volume changes
LiC_6	Li-carbon/graphite	370	Limited obtainable capacity
InSb	Intermetallic and III-V	270	Limited obtainable capacity
$CaSi_2$	Silicides	320	Limited obtainable capacity
$Li_4Ti_5O_{12}$	Transitional metal oxides	168	Limited obtainable capacity
SiTON	Nitrides	450	capacity loss
SnO	Metal oxides	1560	capacity loss

Table 2-1: A comparison of some anode materials with respect to their specific capacity and issues to their utilization

2.3.2 The Cathode

The cathode is the electron exchanger, often referred to as the working electrode. It is where the reduction reaction takes place by electron transfer. The electrons travel in the external circuit and the ions are transported across the electrolyte and are intercalated in the cathode material. In order to enable fast and effective electron exchange, the cathode material merits are high electronic conductivity, high diffusivity of the ionic species, and high insertion capability. Depending on the desired battery voltage and on the anode material, the higher the OCV of the cathode versus a reference point, the higher the obtainable voltage is. For lithium and lithium ions batteries that reference element is often lithium.

Most cathode materials consist of a layered structure; the bonding within a layer is of covalent type and the layers are bonded to each other by weak Van der Waals interactions. The process of intercalation, i.e. reversible insertion of foreign species into a host structure, is enabled due to these weak interactions and is accompanied by a charge transfer reaction between the intercalated guest species and the host material[5,56]:

$$xA^{+} + xe^{-} + H_s \leftrightarrow A_x^{+} H_s^{x-}$$ **Equation 2-4**

Where H_s is the host structure, A^{+} is the alkali ion, and x is the number of electrons participating in the transfer reaction. Although the intercalation process does not affect the chemical and crystallographic stability of the host material, its energy band structure and thereby its electronic properties are affected by that process.

Layered structured compounds are excellent cathodes due to the stability of their structure and the low volume change they exhibit with ion intercalation and electron transfer reactions. Upon removal of the inserted species, the host material ideally retreats to its initial state[57]. Many materials in addition to the open structure layered cathodes were evaluated as cathodes. The most often mentioned group of these materials is the spinel type compounds which will be described at the end of this section.

Of the open structure layered materials, two main sub-groups are discussed in the literature, the transition-metal oxides and transition -metal dichalcogenides. Examples of the dichalcogenides are: TaS_2, MoS_2, and TiS_2. The latter is a popular layered cathode material grown usually by sputtering or vapor deposition with a reported OCV~2.1-2.5 versus lithium and theoretical specific energy of 473 Wh/kg[5,29,58,59]. Subbarao *et al.* compared the performance of TiS_2 with other cathode candidate materials such as MoS_3, $NbSe_3$, and V_6O_{13}. They found that TiS_2 had the best performance out of the compounds they studied in terms of cyclability and specific energy close to the theoretical value[29].

Vanadium oxides are part of the second sub-group materials employed as cathodes are. They are usually employed in the form of orthorhombic or amorphous V_2O_5 although V_6O_{13}, V_3O_8, and VO_x were also mentioned in publications. The vanadium oxides are typically RF sputtered or deposited by Pulsed laser deposition (PLD), plasma enhanced chemical vapor deposition (PECVD), or thermally evaporated[7,9,60-68]. Depending on the growth method and level of crystallinity in the film, V_2O_5 exhibits OCV in the range of 3-3.7 V versus lithium[8,9,64,66]. The calculated theoretical specific energy for intercalation of one lithium ion per one unit cell of V_2O_5 assuming average voltage of ~3 V is 442 Wh/kg. An explanation for calculating the theoretical specific energy is given in Appendix A. Previous work done on vanadium oxide compounds will be described in more detail in Section 3.2.

Another commonly studied oxide material, used also in commercial lithium batteries is $LiCoO_2$ (lithiated Co_3O_4 was also mentioned in the literature[69]). In most cases the deposition method utilized is RF sputtering[10,12,16,25,45,47,70-73]. Sometimes other preparation methods are used for $LiCoO_2$ such as: spray pyrolysis[54], laser direct-write method,[74] solid-state reactions of lithium and cobalt salts,[17,69,75] or PLD[14]. Bouwman *et al.* compared $LiCoO_2$ films deposited by RF sputtering with films deposited by PLD[76]. $LiCoO_2$ was reported to have an OCV~3.6-4.7 V versus lithium depending on the deposition method and conditions[10,11,71,72,74,76,77]. Assuming full intercalation of one lithium ion per CoO_2 unit cell and average voltage of 4 V, its obtainable theoretical energy density is approximately 1000 Wh/kg. This assumption of one lithium ion per CoO_2 unit, however, is not accurate since the structure becomes instable when less than half of the lithium is intercalated[78] and a more practical assumption would be a

theoretical energy density value of ~500 Wh/kg. Previous work done on lithium cobalt oxide will be described in more detail in Section 3.1.

Substituted lithium cobaltites $LiCo_{0.5}M_{0.5}O_2$ with M=Ni, Mg, Mn, and Zn were investigated by Julien *et al.* with respect to structural and electrochemical property changes upon substitution[13]. Benqlilou-Moudden *et al.* prepared and characterized $LiNiO_2$, and $LiNi_{0.7}Co_{0.3}O_2$ as other possible cathode materials[73]. Recent reports presented substituted lithiated transition-metal-oxides such as $LiNi_{0.5}Mn_{0.5}O_2$[79] and $LiNi_{1/3}Co_{1/3}Mn_{1/3}O_2$[80] as other interesting cathode compounds. Other group of layered materials, for instance InSe and $InSe_3$, deposited by MBD, were shown to have OCV of ~2 and ~1.2 V, respectively versus lithium[23].

Out of the spinel structure type of cathode materials, the most common one is $LiMn_2O_4$. The compound is usually prepared by e-beam evaporation[46,63,81,82], PLD[83], solid state reaction,[84] or RF sputtering[46,85-87]. A post-deposition annealing is required to maintain the spinel structure of the $LiMn_2O_4$. The OCV values measured versus lithium vary in different publications between 3-4.5 V[46,63,83,84]. The calculated energy density, assuming 1 lithium per Mn_2O_4 and average voltage of 3 V is ~462 Wh/kg and twice this value for 2 lithium. The downside of $LiMn_2O_4$ as a cathode is its instability expressed in structural and electronic changes occurring upon lithium intercalation with a consequent change in manganese oxidation state. Those are referred to as the Jahn-Teller distortion and are accompanied by a volume change of ~5.6%[84,88]. One approach to stabilizing the $LiMn_2O_4$ structure is to substitute manganese with another element to receive a composition of: $LiZn_{0.025}Mn_{1.95}O_4$[55], $(Na, K, Li)_xMn_{1-y}Co_yO_2$,[89] or $Li_2Co_{0.4}Fe_{0.4}Mn_{3.2}O_8$ [90].

Table 2-2 compares some of the cathode compounds presented in this.

Cathode Material	Theoretical specific energy [Wh/kg]	OCV versus lithium [V]
TiS_2	473	2.1-2.5
V_2O_5	442 (1 Li)	3-3.7
$LiCoO_2$	500 (0.5Li)	3.6-4.7
$LiMn_2O_4$	462 (1Li)	3-4.5

Table 2-2: A comparison of some cathode compounds with respect to their theoretical specific energy and their OCV against lithium

2.3.3 The Electrolyte

The electrolyte is an ionic conductor and an electronic insulator. Among its merits are high ionic conductivity, compared to electronic conductivity, good contact and chemical stability with the electrode surfaces, and materials respectively.

Commercially available batteries usually consist of a liquid electrolyte; a solution containing an acid, a base, or an organic solvent consisting of the relevant ions. Battery experiments done in the 1970's at temperatures of 400-500°C, employed liquid electrolytes prepared from molten lithium salts. The electrolyte mostly used was an eutectic mixture of LiCl-KCl[31-34,40,91] and sometimes other combinations of lithium salts such as LiF-LiCl-KCl or LiF-LiCl-LiBr, which failed to exceed the performance of the eutectic mixture LiCl-KCl[33,34]. More recent publications on batteries utilizing liquid electrolytes at room temperature describe the use of either $LiPF_6$ or $LiClO_4$ typically dissolved in EC-DEC/DMC (ethylene carbonate- diethyl carbonate/dimethoxythane) and PC (propylene carbonate), respectively[7,9-14,17,26,41,44,48,50,55,62,65,76,83,92,93]. These electrolytes are typically stable up to about 5 V and exhibit high ionic conductivities in the order of 10^{-3}-10^{-2} Scm^{-1} [15,29].

Liquid electrolytes have perfect contact with the electrodes, high ionic conductivity, and high electronic resistance; however, batteries comprising of liquid electrolytes often suffer from corrosion of their electrodes and due to safety,

environmental, and stability considerations require closed packaging. The packaging adds to the battery weight reducing the gained energy density. Fueled by these considerations, research activity among the battery community has started drifting more and more in the direction of an all-solid-state-battery. A desired solid-state electrolyte will be insulating electronically and highly ionic conductive. It will have high quality and stable interfaces with the electrodes in terms of wetting, chemical stability, and roughness. The first solid-state electrolyte to be employed in commercially available batteries, powering pacemakers since the beginning of the 1970's, was LiI with ionic conductivity of $\sim 5.5\times10^{-7}$ Scm^{-1} [6]. Some other research activity on solid-state electrolytes in the 1970's included lithium silicates and aluminosilicates[94].

During the late 1980's and early 1990's, the focus of attention among the solid-state battery research community was lithium-containing glassy electrolytes. Glass-type electrolytes are generally composed of three structural components. The first is the network formers, which are covalent compounds such as oxides or chalcogenides of silicon, boron, phosphorus, germanium, and arsenic. The second is the network intermediate modifiers, which cause structural changes in the glass networks like oxides and chalcogenides of alkali, alkaline earth or silver. The third structure component of a glassy electrolyte is the doping salts that are usually additives in the form of halogens sulfates or phosphates with the same cation contained in the network modifier[95]. Examples for glass-type electrolytes are many and only a few will be mentioned here. B_2O_3-xLi_2O-yLi_2SO_4 ($x < 0.6$, $y < 0.3$) amorphous films grown by MBD were reported to have ionic conductivity of $\sigma_i\sim10^{-8}$ Scm^{-1} [23]. Amorphous glass with compositions of xLi_2O:$ySiO_2$:zP_2O_5, or $xLiO_{0.5}$:$ySiO_2$:$(1-y)PO_{2.5}$ were sputtered and exhibited ionic conductivities of $\sigma_i\sim10^{-9}$-10^{-7} Scm^{-1} depending on x, y, and z [96,97]. Another example of a glassy electrolyte is Li_3PO_4-Li_2S-SiS_2 synthesized by heating and quenching, with ionic conductivity as high as 5.2×10^{-4} S/cm^{-1} for a glass composition of $0.61Li_2S$-$0.39SiS_2$[6].

Extensive work done at Oak Ridge National Laboratory on glasses sputtered from various targets such as Li_3PO_4, Li_4SiO_4, Li_2O, SiO_2, and their mixtures, in various ambiance conditions[20,97-100] has led to the development of lithium phosphorus oxynitride (LiPON), one of the most popular solid-state electrolyte materials of today. LiPON is usually sputtered from a Li_3PO_4 target in a nitrogen environment, although sometimes it

is prepared by PLD[101]. LiPON ionic conductivity values in the range of 2×10^{-7}-2×10^{-6} Scm^{-1}, linked to the nitrogen content of the film, were mentioned in the literature and it is known to be stable up to voltage values of 5.5-5.8 V[19,20,25,63,71,72,86,101,102]. Kim *et a.l* investigated the possibility of increasing LiPON conductivity by nitrogen ion implantation and found the impact to be inconsistent[103]. Previous work done on LiPON will be described in more detail in Section 3.2.

Brousse *et al.* presented another type of electrolyte, a lithiated peroversuskite with the composition of $Li_{0.33}La_{0.56}TiO_3$, prepared by powder pressing. They reported a previously measured ionic conductivity of $\sigma_i \sim 10^{-4}$ Scm^{-1} [54].

Table 2-3 summarizes this section with a comparison of the electrolytes.

Electrolyte	**Group**	**Ionic conductivity [Scm^{-1}]**
$LiClO_4$ or $LiPF_6$ in EC-DEC/DMC and PC	Liquid electrolyte	10^{-3}-10^{-2}
LiI	Solid	~5.5×10^{-7}
$Li_{0.33}La_{0.56}TiO_3$	Solid	10^{-4}
B_2O_3-xLi_2O-yLi_2SO_4 ($x<0.6$, $y<0.3$)	Glassy	10^{-8}
xLi_2O:$ySiO_2$:zP_2O_5	Glassy	10^{-9}-10^{-7}
LiPON	Glassy	10^{-7}-10^{-6}

Table 2-3: A comparison of some electrolytes presented in this section with respect to their ionic conductivities.

3 Materials Selection

3.1 $LiCoO_2/SiO_2$/polysilicon cells

The low power requirements of CMOS-technology-based devices have led to the consideration of new materials for battery applications. Materials that are compatible with microelectronic technology can now be incorporated into power cell fabrication processes. The motivation for investigating this material system, and in particular controlled lithium motion in SiO_2, was its potential application as an ultra-thin solid electrolyte in a silicon CMOS compatible power cells. The applications of this study, however, are not limited to batteries and can be used for other novel electronic or optoelectronic devices. In this section, the selected material system is described, along with more detailed background specific to these materials.

3.1.1 SiO_2 as a Solid Electrolyte

One of the most commonly used and well-studied materials in silicon integrated circuits technology, is silicon dioxide. SiO_2 is used as an insulating field material between devices, as an inter-metal dielectric material, and as a transistor-gate-dielectric layer. It is a stable material, with an energy gap of Eg~8 eV which makes it electronically insulating with a bulk resistivity of $\rho \sim 10^{15}\ \Omega cm$[104]. SiO_2 is known to be susceptible to alkali metal ions diffusion. In fact, an interesting aspect of incorporating solid state batteries on semiconductors is that light ion motion in oxides was one of the main barriers to the commercialization of MOSFET devices. The insulating properties, permeability to light ions, and precise level of process control (due to the vast advances in microelectronic device processing) for thin SiO_2 layers provided the motivation to investigate the usage of SiO_2 as a solid-state electrolyte in an integrated thin-film battery.

The idea of using silicon oxide as an electrolyte is unconventional since it is lithium-free. The only study known to present a lithium free electrolyte for a lithium

battery was that of Kushida *et al.*[22] in which they used a porous spin-on glass as the electrolyte with a thickness range of 0.5-1.5 μm. Common solid electrolytes are typically 1-2 μm thick[47,51,63,70,101,105,106] and therefore in order to enable ionic conductivity within them, they consist of a lithium ion network within their structure. The lithium ions conductivity is performed in a continuous manner via that network such as illustrated schematically in Figure 3-1 based on Figure 5 from Bates *et al.* [107].

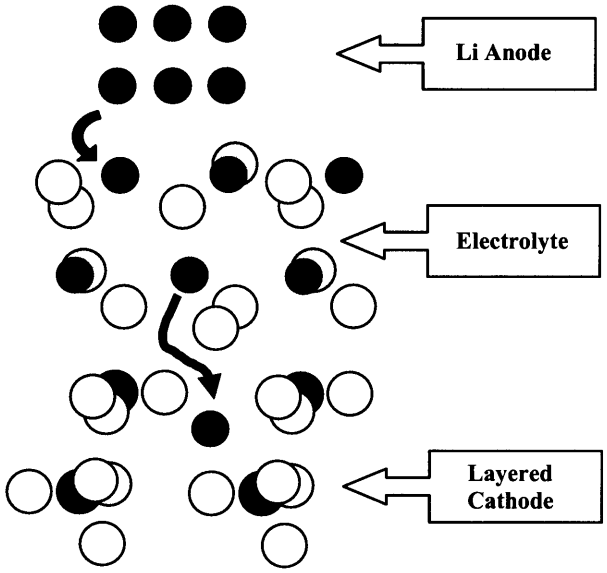


Figure 3-1: A schematic illustration of the lithium ion conduction in conventional solid state electrolytes (based on Figure 5 from Bate *et al.*[107])

As opposed to other common electrolytes, SiO_2 does not contain lithium nor is it doped with a lithium- containing salt. Alkali ions diffuse through SiO_2 rather easily as mobile positive charges and thereby cause instabilities in CMOS devices[108-112]. Sodium, for example, was shown to have a diffusivity of D_0=6.9 cm^2/sec and activation energy of Ea=1.3 eV[113] which yields an overall diffusion coefficient of ~10^{-21} cm^2/sec at room temperature. Lithium ions were shown to be mobile in SiO_2 as well, with a faster mobility compared to sodium ions due to their smaller radii although their mobility was not measured directly[109,110,112]. The diffusion of species in the insulating layer in the form of charged ions is enabled by the columbic capture of their respective electrons. For this to happen, their ionization potential needs to be smaller than the sum of the conduction

band width and the energy gap of the SiO_2, which is equal to the energy distance from the edge of the valence band to the vacuum level as illustrated schematically in Figure 3-2[111].

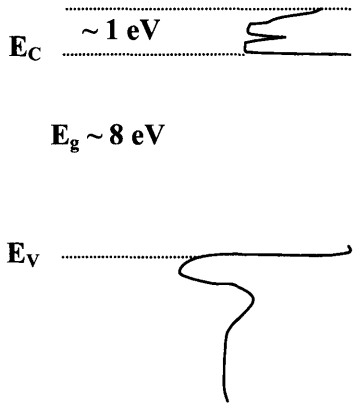


Figure 3-2: A schematic illustration of the energy band structure of SiO_2 (after McCaughan *et al.*[111])

One might expect that an electrolyte that does not contain lithium ions would become positively charged when lithium ions diffuse through it, thereby creating an electric field that would halt the diffusion. The potential created across a bulk oxide layer due to space-charges can be described by the poisson equation:

$$\nabla^2 V = \frac{\rho}{\varepsilon\varepsilon_0} \qquad \textbf{Equation 3-1}$$

$$V = \frac{d}{\varepsilon\varepsilon_0}\int_0^d \frac{x}{d}\rho(x)dx \qquad \textbf{Equation 3-2}$$

Where d is the oxide thickness, ε is the dielectric constant of the oxide, ε_0 is the permittivity of vacuum, and $\rho(x)$ is the charge distribution as function of distance from the electrode/SiO_2 interface. The electric field formed is the derivative of the potential and since $x/d < 1$, it will be maximum at the SiO_2/Si interface. Hino and Yamashita estimated this field to be $E_{max} \sim 2.5 \times 10^6$ V/cm[109].

Snow *et al.* modeled the potential formed across SiO_2 due to space charge distribution of alkali ions in MOS structures[112]. In their model, which was verified

experimentally, they assumed a boundary layer, near the metal/oxide interface, in which diffusion processes, due to concentration gradients, are dominant and space-charge field effects are negligible. Based on experimental results, they estimated this boundary layer thickness to be approximately 14 nm. Therefore, by decreasing the SiO_2 thickness the space charge field effect can be minimized. In this work, cells with thermally grown SiO_2 films of thicknesses of 7-40 nm are studied.

3.1.2 Silicon as an Electrode

The most common and studied CMOS compatible material is silicon itself. Li-Si alloys as anodes were studied intensively in the 1970's and continue to be a research subject, both at room temperature and at higher temperatures (typically ~400°C)[28,32-34,38,43,44,71,92,93,114,115]. When reacted with lithium, silicon forms four compounds: $Li_{12}Si_7$, Li_7Si_3, $Li_{13}Si_4$, and $Li_{22}Si_5$ as can be seen in Figure 3-3.

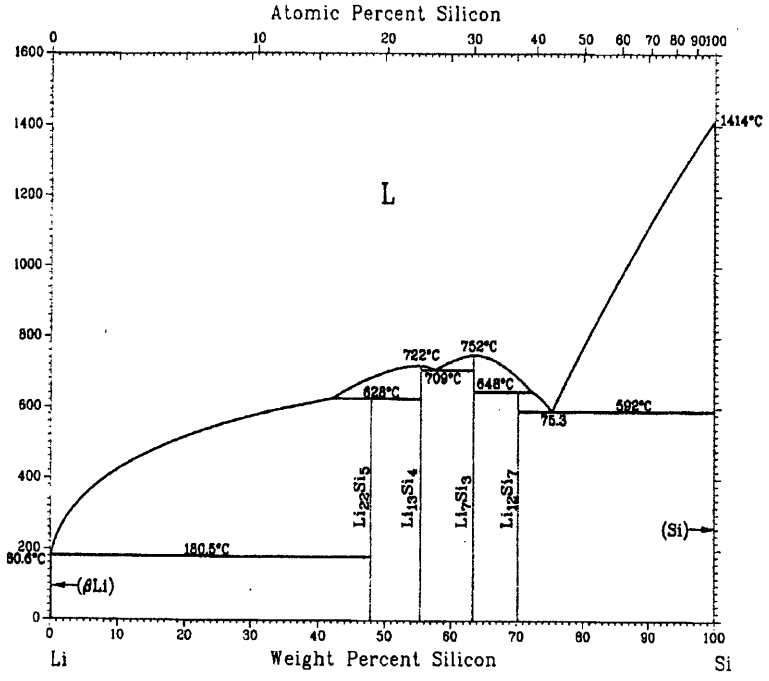


Figure 3-3: The lithium-silicon phase diagram

Li-Si alloys are reported to be capable of reversible specific capacities greater than 1700 mAh/gr[38]; the theoretical capacity density of the most lithium-rich alloy, $Li_{21}Si_5$, is as high as 4020 mAh/gr (4.2 lithium atoms per one silicon atom – see appendix A for calculation). Nesper and Von Schnering wrote about $Li_{21}Si_5$ properties as the most lithium-rich phase in the Li-Si system[39].

Lithium is highly mobile in silicon with a diffusion coefficient of D_{Li}~2-3.5×10^{-14} cm^2/s at room temperature[116]. To illustrate, lithium advances approximately 14 nm in one minute in silicon. Its high permeability to lithium and its high theoretical capacity, in addition to its natural compatibility with CMOS technology, has been the motivation to study silicon as an electrode in the first thin-film integrateable cell of this work.

Often, the electrode/electrolyte interface is a source of problems in batteries. Instabilities and potential failure mechanisms such as chemical reactions and interfacial roughness impose minimum thickness limitation on the electrolyte to prevent shorting the cell. In this work the SiO_2 electrolyte was thermally grown in a clean environment from the silicon electrode film, thus obtaining a high quality and well-understood SiO_2/Si interface never exposed to an atmospheric ambiance.

The major drawback to using silicon as an electrode in a lithium ion battery is the large volume change that accompanies lithium insertion into a silicon electrode which can lead to stresses, cracks, and failure of cells. For example, the formation of the $Li_{12}Si_7$ orthorhombic phase is accompanied by a volume change of 200%:

$$\frac{\frac{8.61\times 19.73\times 14.34}{42} - \frac{5.431^3}{8}}{\frac{5.431^3}{8}} \approx 200\% \qquad \textbf{Equation 3-3}$$

In order to minimize the stresses induced by the volume change in Li-Si reactions, some composite systems have been investigated. The active phase in these systems is silicon embedded in a SnO or TiN matrix designed to alleviate the volume-change-related stresses[40,117]. Some publications described the role of the substrate in the Li-Si reactions,

and suggest using a porous substrate as a way to accommodate volume changes[92], or a passivated nickel foil that adheres well to the expanding and shrinking silicon layer[115].

Silicon morphology and the level of crystallinity also help control the Li-Si system electrochemical properties and the volume change problem. Gao *et al.* studied alloying of lithium with nano-structured silicon and claimed that the reactions' energy barriers were reduced compared to macroscopic silicon made from commercially purchased powder[28]. Hatchard *et al.* studied amorphous silicon as an electrode with homogeneous volume changes compared to crystalline silicon[114].

Thin films consist of higher surface-to-volume ratio and therefore are expected to exhibit less stresses related to the expansion and contraction accompanying lithium insertion and extraction. In this work, a thin layer of highly doped polycrystalline silicon is employed as an electrode in the first material system-based cells.

3.1.3 $LiCoO_2$ as a Cathode

$LiCoO_2$ was reported to have an open circuit voltage (OCV) of ~ 3.6-4.7 V versus lithium depending on the deposition method and conditions[10,11,71,72,74,76,77]. Assuming full intercalation an average voltage of 3.5 V for an intercalation of half of the existing lithium per one unit cell of CoO_2, its obtainable theoretical energy density is approximately 500 Wh/kg (see Appendix A for cathode energy density calculations). $LiCoO_2$ consists of a layered hexagonal structure in which the oxygen anions form a closed packed network with the lithium and cobalt cations on the alternating (111) planes of the cubic rock-salt sub-lattice. Upon lithium extraction, the oxidation state of cobalt changes from Co^{+3} to Co^{+4} and the structure remains stable providing that the lithium extraction does not exceed half of the existing lithium ions[78]. A schematic illustration of the structure with intercalated lithium can be seen in Figure 3-4:

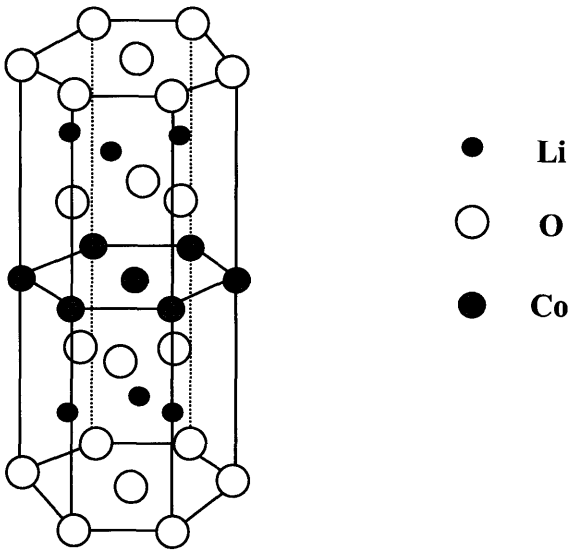


Figure 3-4: Schematic description of the $LiCoO_2$ crystallographic structure

For Li_xCoO_2 an experimental structure density of $\rho \sim 3.7$ g/cm^3 [25] was reported versus the theoretical value of 5.06 g/cm^3 [71]. Semiconducting properties have been detected for a lithium content $x < 1$, and an energy gap of $Eg \sim 2.7$ eV for $x = 1$[118]. Lithium ion mobility in $LiCoO_2$ is highly dependent on the lithium content in the film. Reported diffusion coefficients of lithium in $LiCoO_2$ range between $D_{Li} \sim 10^{-12}$ and $\sim 10^{-9}$ cm^2/s[14,17,71]. In this work, a thin layer of polycrystalline $LiCoO_2$ is employed as an electrode in the first material system based cells. Although it is a common cathode material, $LiCoO_2$ served as the lithium source in this study since the cells are deposited in their discharged state in which there is no lithium in the polysilicon anode.

3.1.4 The Current Collectors (Contacts)

The current collectors are the cell contacts, electronically conductive materials, metals, which do not conduct ions and preferable do not alloy with lithium. Aluminum can react with lithium and titanium is inert and impermeable to lithium. Titanium is a microelectronics compatible element as it is commonly used to form silicides to improve the silicon/metal contact quality. In the cell based on the first material system, a bi-layer of titanium and aluminum is employed both as front (the anode current collector) and back (the cathode current collector) contacts.

3.2 V_2O_5/LiPON/$LiCoO_2$ Cells

The first material system in this work consisted of SiO_2 and the combination of SiO_2/Si, which is compatible with microelectronic technology but is rather new to battery applications. The employed fabrication and characterization methods were compatible with microelectronics processing as well. The second phase of the work involved optimizing the fabrication process and improving the cell properties by utilizing chemical mechanical polishing (CMP), a film planarization method used by microelectronics. In the third part of this research, a conventional electrochemistry-compatible material system was studied by applying the microelectronics thin-film expertise, process, and characterization methods. In this section, the second selected material system is described, along with a more detailed background specific for these materials.

3.2.1 LiPON – Solid-State Electrolyte

Lithium Phosphorus Oxynitride (LiPON) is one of the recent additions to the battery field. It was developed at Oak Ridge National Laboratory as a result of research done on glasses sputtered from various targets such as: Li_3PO_4, Li_4SiO_4, Li_2O, and SiO_2 and their mixtures in various ambient conditions[20,97-100]. The chemical composition of LiPON is of the form: $Li_{3+y}PO_{4-x}N_z$ where $-0.25 < y < 0.6$, $0.1 < x < 1.11$, and $0.17 < z < 0.69$. LiPON is essentially a lithiated phosphoric glass with nitrogen atoms substituting oxygen ones[18,20,99,103]. LiPON is usually sputtered from a Li_3PO_4 target in a nitrogen environment. It can also be prepared by PLD[101]. This amorphous glass density was reported to be 2.4-2.5 g/cm^3, its ionic conductivity values can be as high as 2×10^{-7}-3×10^{-6} S/cm, linked to the nitrogen content of the film, and it is known to be stable up to voltage values of 5.5-5.8 V with a dielectric constant of $\varepsilon = 26.6$[18-20,25,63,71,72,86,101,102,119]. The incorporation of nitrogen in the film is believed to increase its lithium conductivity by modifying the glass structure. Nitrogen replaces bridging oxygen atoms and its incorporation increases the level of cross-linking in the electrolyte as described in Figure 3-5 based on Figure 3 from Rho *et al.*[102].

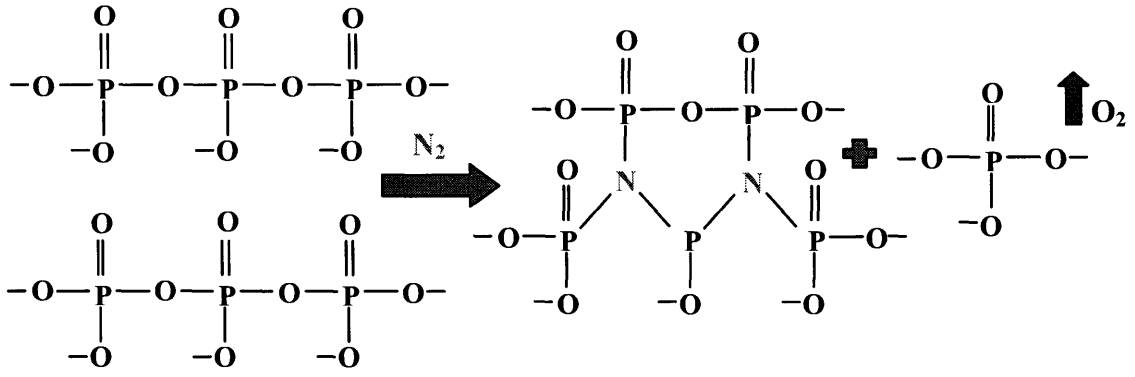


Figure 3-5: Schematic illustration of nitrogen incorporation and structure modification in formation of LiPON[102].

Kim *et al.* investigated the possibility of increasing LiPON conductivity by nitrogen ion implantation and found the impact to be inconsistent[103]. In this work LiPON serves as the electrolyte in the second material system.

3.2.2 V_2O_5 – Anode

A commonly used cathode material is vanadium oxide, usually in the form of orthorhombic or amorphous V_2O_5 although V_6O_{13}, V_3O_8, and VO_x have been reported as well. In the rocking chair battery studied in this work, both electrode compounds are typically used as cathodes and in the fabricated state V_2O_5 serves as the anode. The vanadium oxides can be RF sputtered from a V_2O_5 target or reactive sputtered from a vanadium target in O_2 ambience[8,9,63-68,106]. Vanadium oxides can also be deposited by PLD, PECVD or may be thermally evaporated[7,51,60-62]. Crystalline V_2O_5 consists of an orthorhombic layered structure in which each vanadium atom is positioned in the center of a deformed pyramid of five oxygen atoms and is connected to a sixth one forming an octahedron, as can be seen in Figure 3-6 based on Chiba *et al.*[120]. The octahedrons are connected to each other through their edges and thereby form a layered structure. Lithium can be intercalated between those layers.

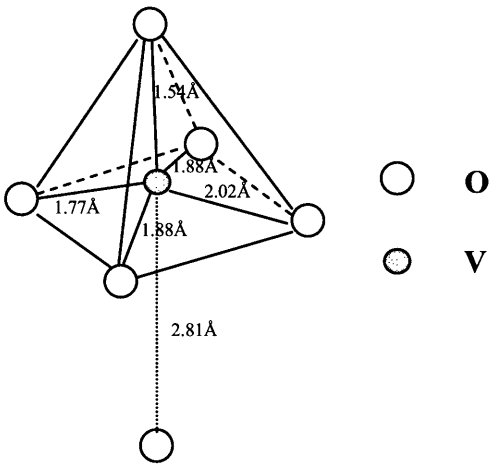


Figure 3-6: Schematic illustration of the deformed pyramid of the V_2O_5 structure (after Chiba *et al.*[120])

Amorphous V_2O_5 is often used as a cathode as well and was suggested to have better electrochemical performance than crystalline V_2O_5[7,66]. Depending on the growth method and level of crystallinity in the film, V_2O_5 exhibits OCV in the range of 3-3.7 V versus lithium[8,9,64,66] with a reported density value of 3-3.36 g/cm^3 [8,63]. The theoretical specific energy for intercalation of 1 lithium ion per one unit cell of V_2O_5 assuming average voltage of ~3 V is 442 Wh/kg (see Appendix A for calculation). The diffusion coefficient of lithium in $Li_xV_2O_5$ at 25-40°C was found to be D_{Li}~10^{-15}-10^{-12} cm^2/s decreasing with an increase in lithium content[8,63] and its band gap Eg~2.15 eV[68]. V_2O_5 was used in an all solid-state rocking-chair battery, in which lithium is transferred back and forth between two intercalation compounds, sometimes against a lithiated V_2O_5 anode[51,106], and sometimes against another lithiated transitional metal oxide such as $LiMn_2O_4$[53]. In this work an amorphous thin-film of V_2O_5 is studied against a $LiCoO_2$ thin electrode forming a rocking chair thin-film battery as well.

3.2.3 $LiCoO_2$ - Cathode

In the second material system explored in this work, a thin polycrystalline film of $LiCoO_2$ was used as cathode against V_2O_5. For background and literature survey on $LiCoO_2$, see Section 3.1.3.

3.2.4 Current Collectors

Platinum is an inert metal, often used as a current collector in electrochemistry. In this material system, the metals for the electrode contacts were picked to be platinum and aluminum. Employing two different metals for the two electrodes is designed to simplify the fabrication process by allowing high selectivity in the wet etch step in the fabrication process, as will be described in Section 4.3. For adhesion enhancement between the platinum layer and the silicon substrate as well as the cell layers, thin layers of titanium were deposited beneath and above the platinum.

4 Cell Design and Materials Characterization

4.1 Films Growth Methods

4.1.1 Chemical Vapor Deposition (CVD)

Chemical vapor deposition is a thin-film growth method that utilizes a chemical reaction in which the reacting materials are gases and at least one of the products is solid. The gaseous reactants diffuse to the substrate surface, get absorbed and react on the surface to create the desired film. The gaseous byproducts are desorbed and exhausted out of the reactor. In this work, Low Pressure CVD (LPCVD) is used to grow the polysilicon layer from silane gas through the reaction:

$$SiH_{4[g]} \rightarrow Si_{[s]} + 2H_{2[g]} \qquad \textbf{Equation 4-1}$$

The doped polysilicon layer was deposited using reaction 4-1 with an added precursor of $PH_{3[g]}$ which decomposes into phosphorous atoms and hydrogen gas, $H_{2[g]}$. In this reaction, the phosphorous atoms reside on silicon lattice sites. The growth temperature was 625°C and the pressure in the tube during deposition was ~250 mTorr. The undoped polysilicon layer was grown at 550°C. The wafers were cleaned, as described in Section 4.2, prior to loading them into the quartz boat which was inserted in the growth tube for undoped polysilicon deposition. In the second phase of the project, amorphous silicon layers meant for oxidation were grown on top of the planarized doped polysilicon films in an ultra high vacuum CVD (UHV-CVD) reactor at 550°C at a pressure of 2-3 mTorr. A cleaning step preceded the amorphous layer deposition as described in Section 4.2. After the cleaning step the wafers were loaded into the reactor, which was pumped down to $\sim 1 \times 10^{-9}$ Torr. Before introducing the precursor gases, the wafers were held at 800°C for 10 minutes to volatilize the native oxide that might have

formed during the wafers' cleaning step. After 10 minutes at 800°C, the wafers were transferred to a different area in the reactor which was kept at 550°C, the amorphous silicon growth temperature.

4.1.2 Silicon Thermal Oxidation

A distinction is made between two types of thermal oxidation of silicon: dry oxidation and wet oxidation. Dry oxidation is performed with $O_{2[g]}$ (Equation 4-2) whereas in wet oxidation the oxidant is water vapor, $H_2O_{[g]}$ (Equation 4-3):

$$Si_{[s]}+O_{2[g]}\rightarrow SiO_{2[s]} \qquad \textbf{Equation 4-2}$$

$$Si_{[s]}+2H_2O_{[g]}\rightarrow SiO_{2[s]}+2H_{2[g]} \qquad \textbf{Equation 4-3}$$

The silicon wafers are cleaned by a standard RCA clean (see Section 4.2.1) which is aimed to get rid of organic and metal contaminations as well as etching the existing native oxide and passivating the surface to prevent the formation of a new native oxide layer. Immediately after cleaning, the wafers are loaded into a quartz boat and inserted into an oxidation tube kept at high temperature.

The silicon oxidation reaction occurs at the Si-SiO_2 interface, initiating with the silicon and ambient interface. The rate of oxidation depends on the diffusion of oxidizing species through the oxide to the Si-SiO2 interface, where they subsequently react with silicon atoms and form SiO_2. Of the two oxidizing agents, $H_2O_{[g]}$ is smaller than $O_{2[g]}$, therefore its diffusion to the SiO_2/Si interface is more rapid, resulting in a much faster oxidation rate for wet oxidation. Hence, dry oxidation is normally used for ultra-thin oxides in slower processes whereas wet oxidation is used when thicker oxides or faster growths processes are required. The higher the oxidation temperature is, the faster the diffusion of the oxidizing species will be, therefore leading to faster growth.

In this work the oxidation process occurred in parallel with a competing phosphorous upwards diffusion, originating from the highly doped polysilicon layer, into

the layer being oxidized. The presence of phosphorous in an oxidizing silicon layer can degrade the oxide quality, damaging its electronic insulation as well as alternating the oxidation rate. Therefore, wet oxidation at 700°C was chosen as the processing condition, to slow P diffusion by oxidizing at a relatively low temperature and using the highly mobile oxidizing species associated with wet oxidation.

4.1.3 RF and DC Sputtering

Plasma is a conductive gas containing charge carriers such as electrons and ions. RF and DC deposition methods utilize plasma as the deposition media. Plasma is formed by applying high DC or AC voltage (1-5 kV) to gas at low pressure (~10^{-3}-10^{-2} Torr). The gas typically used in sputtering is argon, which has a high atomic mass and is relatively inexpensive. A voltage is used to accelerate the molecules and collisions between them generate charge carriers within the gas. Fast electrons are created and as a consequence of collisions with argon atoms, they ionize the latter, releasing new electrons and slow down. The argon atoms ionization reaction is described by:

$$15.76eV + Ar + e^{-}[fast] \rightarrow Ar^{+} + e^{-}[slowed] + e^{-} \quad [121] \qquad \textbf{Equation 4-4}$$

The electrons resulting from the argon ionization are accelerated by the electric field and take part in additional collisions. When the charge carriers number increase, the avalanche of charge carriers, i. e. the gas breakdown, causes an abrupt drop in the required voltage and the glow discharge appears. Recombination of ions and electrons occurs in a slow pace and therefore the plasma is not extinguished [121].

Thin film growth by sputtering occurs when the target acts as an electrode and the plasma collision momentum causes atoms to be sputtered off the target and coat the substrate.

AC sputtering is used to deposit dielectric materials by the application of AC voltage, typically at radio frequency (RF), between two electrodes: one is the target and the other is the chamber with the substrate holding electrode which is grounded. Opposite currents of ions and electrons are generated. Positive ions are accelerated into the

negatively charged target inducing sputtering. By adding a capacitor, connected in series to the RF circuit, the sputtering is controlled to take place on one electrode only[121].

In this work, DC sputtering was used to deposit the cathode contact metals, titanium and aluminum, in the first material system studied, and aluminum in the second material system. RF sputtering was used to deposit $LiCoO_2$ in both material systems and V_2O_5 and LiPON in the second material system using N_2 plasma for the latter. A schematic line drawing of the CMS-18 sputter deposition system used in this work can be seen in Figure 4-1 taken from the Kurt J. Lesker company internet website:

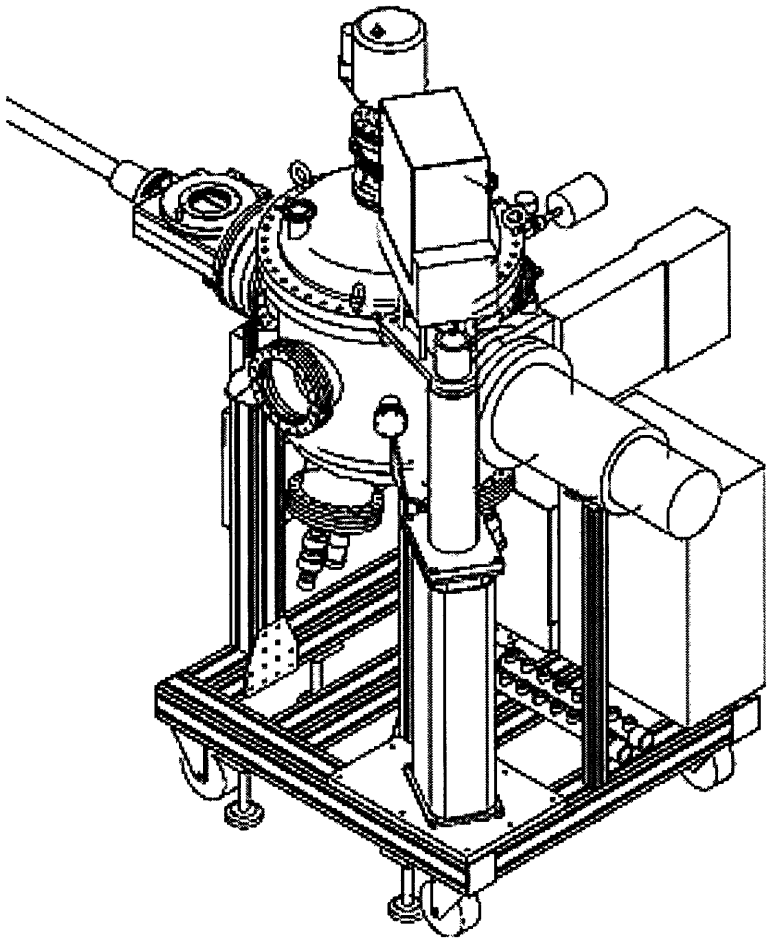


Figure 4-1: The CMS-18 sputtering unit used in this research (taken from the Kurt J. Lesker website).

The sample is inserted into the chamber via the load lock which is pumped down to ~10^{-4} Torr by a roughing dry pump in combination with a turbo pump. The base

pressure in the growth chamber is typically 10^{-7}-10^{-6} Torr, achieved by a cryogenic pump. The gases, Ar, N_2, or Ar/O_2 mixture, are introduced into the chamber and the pressure during deposition is ~10^{-2} Torr. The system consists of two DC and one RF sputtering guns which each hold a sputtering target. The targets used in this work were commercially purchased. Gun power values were in the range of 200-350 W, which corresponds to 4.4-7.7 W/cm^2 power density range for a 3" diameter target. The substrate holder is rotated during deposition for greater film uniformity.

4.1.4 Electron Beam Evaporation

Electron beam evaporation is a technique used to deposit various thin films, normally metals. The substrate is placed in a vacuum chamber which is typically pumped down to ~10^{-6} Torr by a combination of a mechanical pump (up to ~10^{-2} Torr) and a cryogenic pump. The source material is contained in a ceramic crucible and is radiated by an electron beam emitted from an electrically heated tungsten filament. The material in the crucible is heated until it melts and starts evaporating and molecules come to rest on the substrate. The deposition is monitored *in-situ* by a thickness-monitor crystal. In this work, the e-beam evaporator in the exploratory materials laboratory (EML) was used to deposit the back contacts, titanium and aluminum, in the first material system and the e-beam evaporator in the technology research laboratory (TRL) was used to deposit titanium and platinum in the second material system.

4.2 Experimental Procedure of LiCoO2/SiO2/polysilicon cells

4.2.1 Cell Fabrication Process

The $LiCoO_2/SiO_2$/polysilicon cells , up to the electrolyte layer were created in the integrated circuits laboratory (ICL) lab at MIT, a class 10 clean-room. The cells were fabricated upon 1 μm of oxide, grown on a (100) silicon substrate. In principle, the method described in this work could allow the integrated battery to be grown on the back side of the wafer as part of the back-end silicon processing on the chip. The fabrication

process of the cells is illustrated in Figure 4-2. Note that the layers' thicknesses, as depicted in the illustrations, are not to scale.

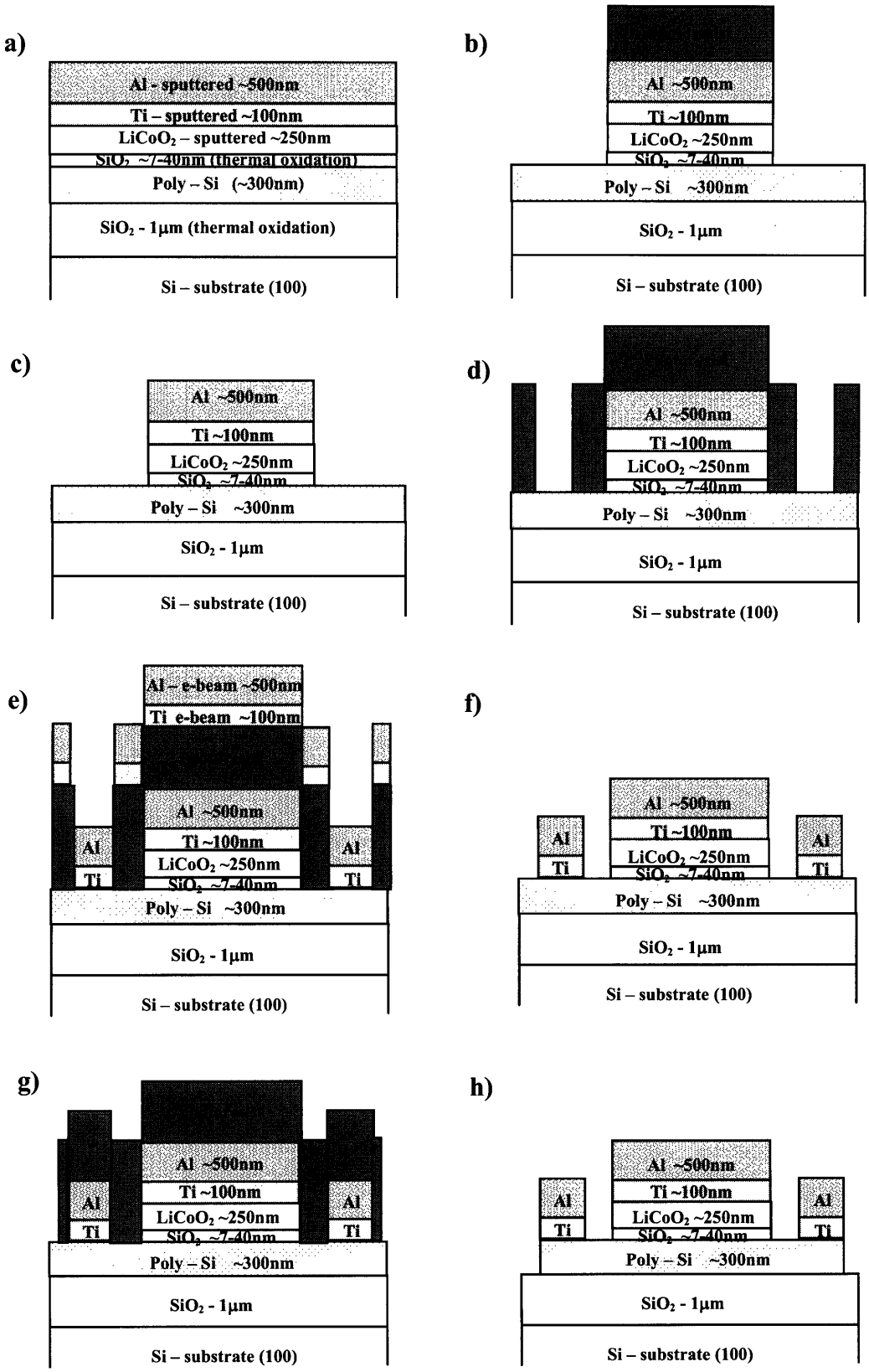


Figure 4-2: An Illustration of the $LiCoO_2/SiO_2$/polysilicon cell fabrication process

A ~300 nm thick polysilicon anode layer was deposited using LPCVD at 625°C from a SiH_4 gas precursor and was highly doped *in-situ* with phosphorus to make the film electronically conductive (n-type) followed by a 12 minutes anneal step at 900°C to activate the dopants. The resistivity of the *in-situ* doped polysilicon layer was measured, post annealing, by a sheet resistance profiling method and was found to be 10^{-3} Ωcm. In order to obtain better quality of SiO_2 and to maintain better control over thickness and uniformity, a thin layer (14-17 nm) of undoped polysilicon layer was deposited at 550°C, using LPCVD, on top of the doped poly. The undoped polysilicon layer was subsequently thermally oxidized, by wet oxidation, at 700°C to create a uniform layer of SiO_2 (7-40 nm).The low temperature of oxidation was chosen in order to minimize phosphorous diffusion into the growing oxide layer. The wafers were cleaned by a standard RCA cleaning process which includes: organic clean – standard clean one (SC1), which is done with a solution of $NH_4OH:H_2O_2:H_2O$ in a 1:1:5 ratio at 80°C for 10 minutes, HF (50:1) dip for 30 seconds (removal of oxide formed by the organic clean stage), and ionic and heavy metals clean - standard clean two (SC2), which is performed with a solution of $HCL:H_2O_2:H_2O$ in a 1:1:6 ratio at 80°C for 15 minutes. The RCA clean ended with a dilute HF (50:1) dip for 30 seconds prior to poly growth or thermal oxidation to etch the grown oxide and to leave the surface terminated with hydrogen.

In the second phase of the project, as will be described in Chapter 6, the doped poly was grown thicker (330 nm) and was planarized by chemical mechanical polishing (CMP) using an NaOH solution type slurry to a final polysilicon thickness of approximately 300 nm. For a detailed description of the CMP method, see Section 4.2.2. After the CMP step, the wafers were cleaned using standard piranha solution ($H_2SO_4:H_2O_2$ 3:1) twice (10 minutes each time) and then by dipping them into a dilute HF (50:1) solution. A thin layer of amorphous silicon was then grown at 550°C from SiH_4 gas at growth pressure of approximately 2-3 mTorr, using UHV-CVD. Prior to loading the wafers into the UHV-CVD reactor, they were cleaned by using an additional Piranha etch for 10 minutes and a dilute HF dip (10:1) for one minute.

RF sputtering in argon ambient was used to deposit the $LiCoO_2$ cathode layer at 200°C from a commercially purchased $LiCoO_2$ target 3" in diameter, using gun power of 200 W. Initial depositions indicated that films with better quality were grown when

slightly heating the substrate as opposed to growing at room temperature. This is demonstrated by the two SEM pictures shown in Figure 4-3, comparing $LiCoO_2$ films deposited at room temperature and at 150°C.

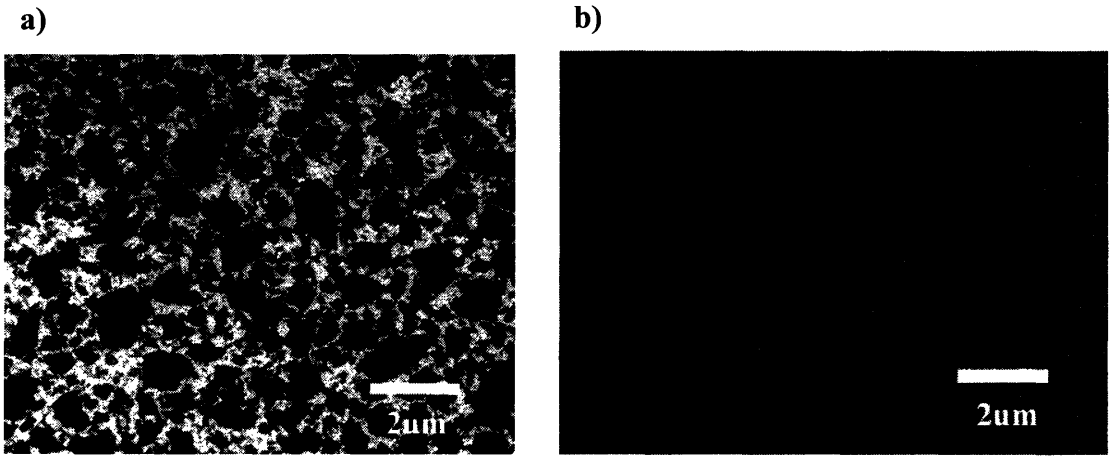


Figure 4-3: SEM micrographs showing initial film characterization depositions of $LiCoO_2$ a) at room temperature and b) at 150°C

The thickness of the deposited $LiCoO_2$ films in the fabricated cells was 250 nm and they were polycrystalline in nature, as verified by transmission electron microscopy (TEM) imaging and electron diffraction (see Figure 4-4). The rings in the $LiCoO_2$ diffraction pattern are an indication of a polycrystalline microstructure. Secondary ion mass spectrometry (SIMS) determined the Li:Co ratio in the as-deposited films to be 0.7. A more detailed description of the characterization methods used in this research can be found in Section 4.4.

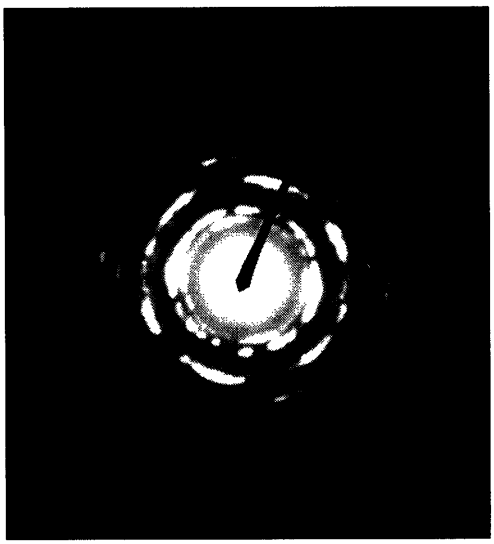


Figure 4-4: An electron diffraction image from RF sputtered $LiCoO_2$ film

The cathode Ti-Al contact bi-layer was deposited by DC sputtering from titanium and aluminum targets respectively in an argon environment. The wafer was then patterned using photolithography with a chromium-coated glass mask and a thick resist, type AZ-4620, followed by a wet chemical etch to create square cells of four different sizes of active areas: 5×5 mm^2, 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2 (parts a, b, and c in Figure 4-2). The aluminum layer was etched at 50°C for two minutes employing a commercial aluminum etching solution - type A, consisting of H_3PO_4:HNO_3:HAc:H_2O at a ratio of 16:1:1:2. The titanium and $LiCoO_2$ etches were performed at room temperature for 90 seconds with a solution of HF:H_2O_2:H_2O at a ratio of 1:1:20. The cells consisted of a 'body type' square ring back contact to minimize resistance and to allow contacting both cathode and anode from the same side of the wafer. The back or anode contact was created by masking the active areas using photolithography, with a dark field mask, cleaning the polysilicon exposed areas, by a dilute HF dip, followed by e-beam evaporation deposition of titanium and aluminum and ending with acetone lift-off. The deposited metal in the areas which were initially covered by photoresist protecting the active area of the cells is 'lifted-off' as a result of the resist dissolving in acetone leaving the square ring metal covered areas (see parts d, e, and f in Figure 4-2).

The fabricated cells were electronically isolated from each other by etching trenches in the polysilicon layer using photolithography followed by a chemical etch. The

wet chemical etch was performed at room temperature for two minutes using HNO_3:H_2O:NH_4F at the ratio of 126:60:5 (see part g and h in Figure 4-2). The deposited and patterned cells were annealed for one hour at 400°C in N_2 in order to improve the quality of the contacts and the $LiCoO_2$ film.

The final cell structure from a side view and top view can be seen in Figure 4-5 as a schematic illustration with an inset of a TEM image showing a cell with a 40 nm thick oxide. Note that the thickness of the layers in the structure illustration is not to scale.

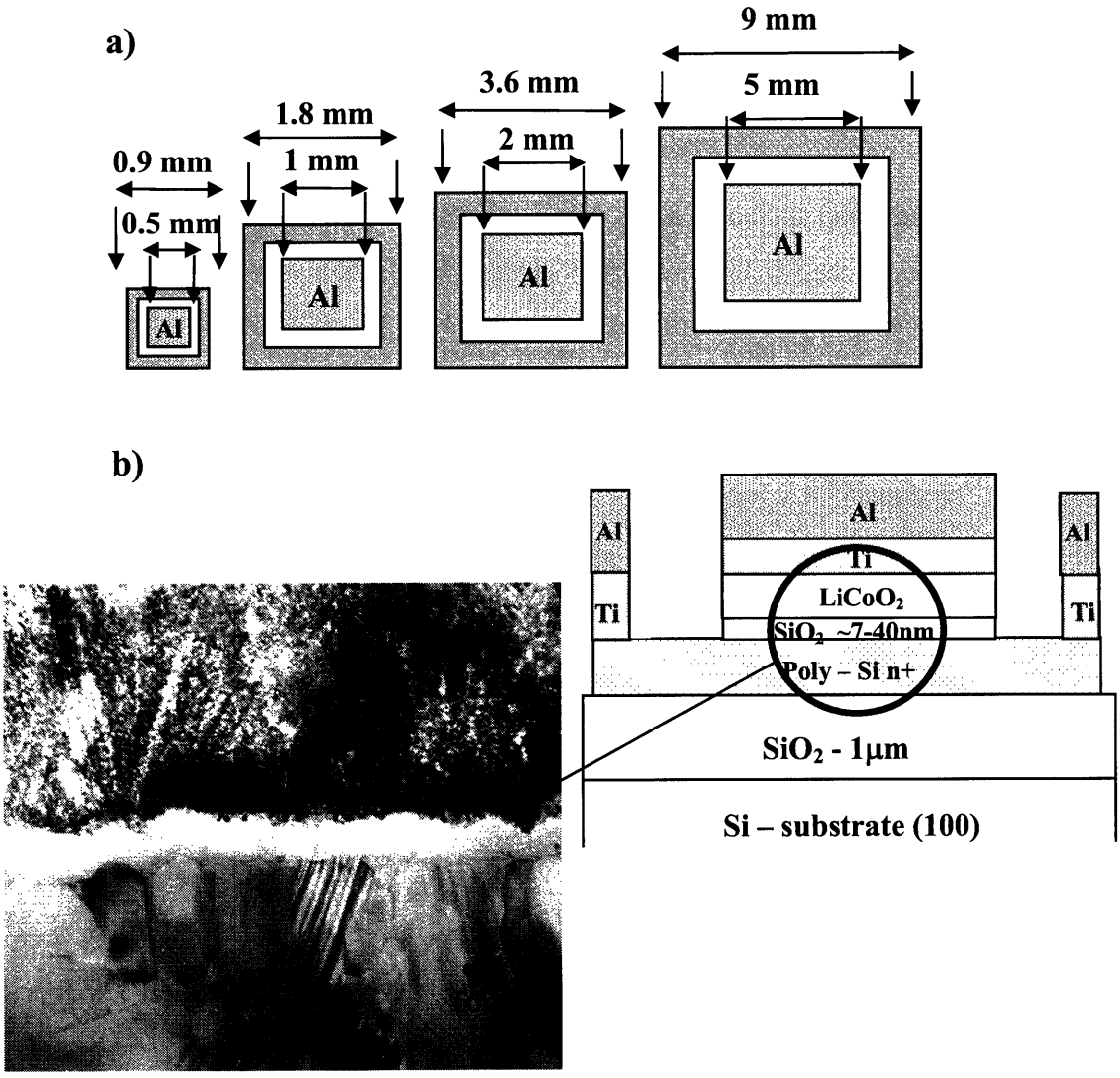


Figure 4-5: a) Top view and b) side view of the fabricated $LiCoO_2$/SiO_2/polysilicon cells with a TEM inset showing a cell with 40 nm thick SiO_2.

4.2.2 Chemical Mechanical Polishing as an Electrode Planarization Method

Chemical mechanical polishing is a known planarization method used by the microelectronics industry for 40 years. CMP is used to polish SiO_2 glass, to facilitate wafer bonding, for planarizing inter-layer dielectrics (ILD) as well as metals, especially copper, the new metal in ICs' interconnects. A CMP system consists of an automated rotating table with an adhered polishing pad and a mechanical wafer holder which can independently rotate the wafer and apply force on it against the table[122]. The pad is continuously wet by polishing slurry that typically contains colloidal silica suspended in a KOH solution which acts as a silicon etchant. For slower removal rates, NaOH solution can be employed.

The CMP process should not be regarded as mechanical abrasion of slurry against the wafer surface, but rather a process consisting of a joint chemical and mechanical mechanism. It involves the formation of hydrogen bonds between the surfaces of the wafer and the slurry, the formation of molecular bonds between the wafer and the slurry and the breaking of the film bonds when the slurry particles move away see Figure 4-6 (based on Sze and Chang[122]). Planarization is achieved since only topographically higher points on the wafer come in contact with the polishing pad.

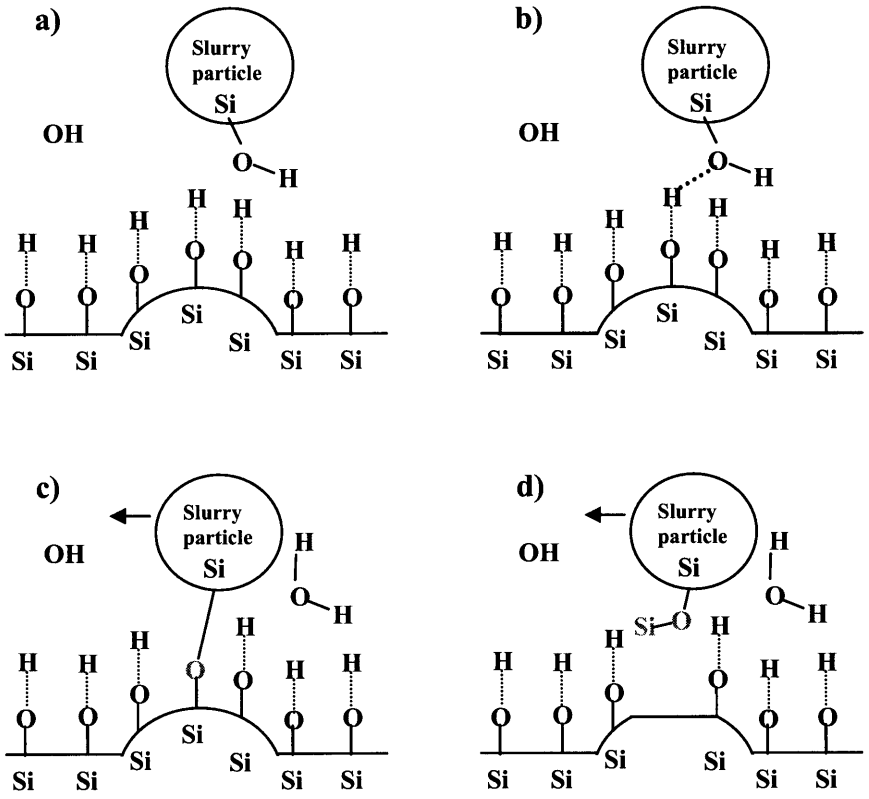


Figure 4-6: An illustration of the CMP mechanism: a) surface oxide forms hydroxyls, b) H bond formation between the slurry and the wafer surface, c) Si-O bond formation and water molecule release, d) Si-Si bond break when particle is moved[122]

Uniformity in removal rate across the wafer and between wafers is not easily achieved due to differences in relative velocities of wafer sections compared to the polishing pad, lack of uniformity in the distribution of the slurry beneath the wafer and pre-existing non-uniformities of the wafer[122].

In spite of its common usage in microelectronics, so far, CMP has not been used as a planarization method in any battery application process. In this work, CMP was used to planarize the doped polysilicon layer in order to improve the quality of the interface with SiO_2 and to reduce the oxide thickness distribution. A slurry solution of NaOH was used to achieve removal rates of approximately 0.86 nm/sec. By removing 30 nm of the polysilicon layer, its root mean squared (RMS) roughness was reduced from 8.069 nm to 0.528 nm for a scanned area of 1 μm × 1μm.

4.3 V_2O_5/LiPON/$LiCoO_2$ Cell Design and Fabrication

4.3.1 Layers Sequence and optimization of deposition conditions

Conventional solid state batteries often consist of rough interfaces which dictate thickness limitations on the electrolyte in order to prevent shorting between the electrodes. In this material system, deposition conditions were tailored in order to achieve higher quality electrode films with minimal roughness. As was shown in Figure 4-3, early depositions of $LiCoO_2$ have indicated the need to slightly heat the substrate during deposition for greater film quality. The surface morphology of a 200 nm thick $LiCoO_2$ film deposited at substrate temperature of ~200°C can be seen in Figure 4-7. The film exhibited a 1 μm × 1 μm RMS roughness of 12.6 nm.

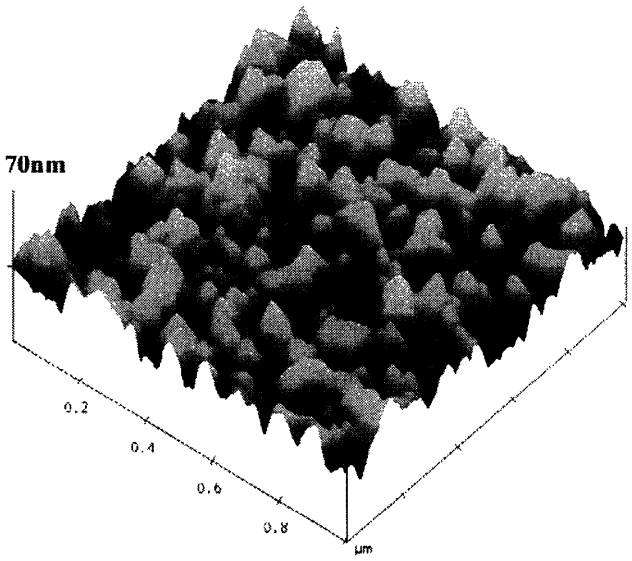


Figure 4-7: An AFM image of a $LiCoO_2$ film

A surface morphology study was performed on 200 nm thick V_2O_5 films deposited on a silicon substrate with varying growth parameters, in order to determine the optimal conditions for V_2O_5. The films were RF sputtered from a commercially purchased V_2O_5 target at a constant oxygen background pressure of 3%, to maintain

film's stochiometry, and various gun power and substrate temperature values. The gun power values are given for a 3" diameter sputtering target and correspond to gun power density values of: 5.48, 6.48, and 7.47 W/cm^2 for 250, 300, and 350W, respectively. Table 4-1 shows 1 μm × 1 μm RMS roughness values as function of growth conditions. From the values shown it is apparent that temperature is a key parameter in achieving smooth films of V_2O_5. Films deposited at room temperature exhibited the lowest RMS roughness values.

Temp / Power	R.T	150°C	250°C
250W	$2V_{11}$ 5.59nm	$2V_{12}$ 9.37nm	$2V_{13}$ 13.90nm
300W	**$2V_{21}$ 3.78nm**	$2V_{22}$ 36.73nm	$2V_{23}$ 72.67nm
350W	$2V_{31}$ 4.80nm	$2V_{32}$ 11.87nm	$2V_{33}$ 25.29nm

Table 4-1: RMS values of 200 nm thick V_2O_5 for different deposition conditions

The surface morphology and film microstructure for different conditions will be described in detail in Chapter 7.

Based on the preferred conditions found for deposition of the two electrode materials, the layers sequence was chosen to begin with $LiCoO_2$ sputtering at 200°C followed by LiPON, and to allow the system to fully cool down prior to V_2O_5 deposition.

Reported works on LiPON, described ionic conductivity values as high as 2×10^{-7}-3×10^{-6} S/cm^{-1}, increasing with nitrogen content in the film[19,20,25,63,71,72,86,101,102]. In this work LiPON films were sputtered from a commercially purchased Li_3PO_4 target in N_2 ambience. In order to find the optimal conditions for LiPON deposition, several films were deposited at different conditions on aluminum foil and on a platinum-covered silicon substrates for ionic conductivity measurements (by impedance measurements, see Section 4.3.9) and nitrogen content analysis (by XPS, see Section 4.3.7) respectively. The ionic conductivities values measured for LiPON films deposited at different conditions with their corresponding nitrogen content can be seen in Table 4-2:

Process parameters: N_2 flow [sccm], T, power [watt]	N content [at%]	Conductivity [Scm^{-1}]
36 , 200°C, 250	0	5×10^{-12}
37 , R.T, 300	0.41	2.6×10^{-10}
40 , R.T 300	0.19	6×10^{-12}
40 , R.T, 350	1.05	1.4×10^{-8}
37 , R.T, 350	0.23	1.3×10^{-10}
43 , R.T, 350	0.40	1.95×10^{-9}

Table 4-2: LiPON conductivities and nitrogen content for various deposition conditions

4.3.2 Cell Processing

The V_2O_5/LiPON/$LiCoO_2$ cells were fabricated on silicon substrates, using a microelectronics compatible process. The fabrication process of the cells is illustrated in Figure 4-8. Note that the layers' thicknesses, as depicted in the illustrations, are not to scale. An inset of a XTEM image showing a 100 nm thick LiPON and its interfaces with the two electrodes can be seen in Figure 4-8. Again, the fabrication method described here can be used to deposit the cell as part of the back end process, possibly on the back of the chip.

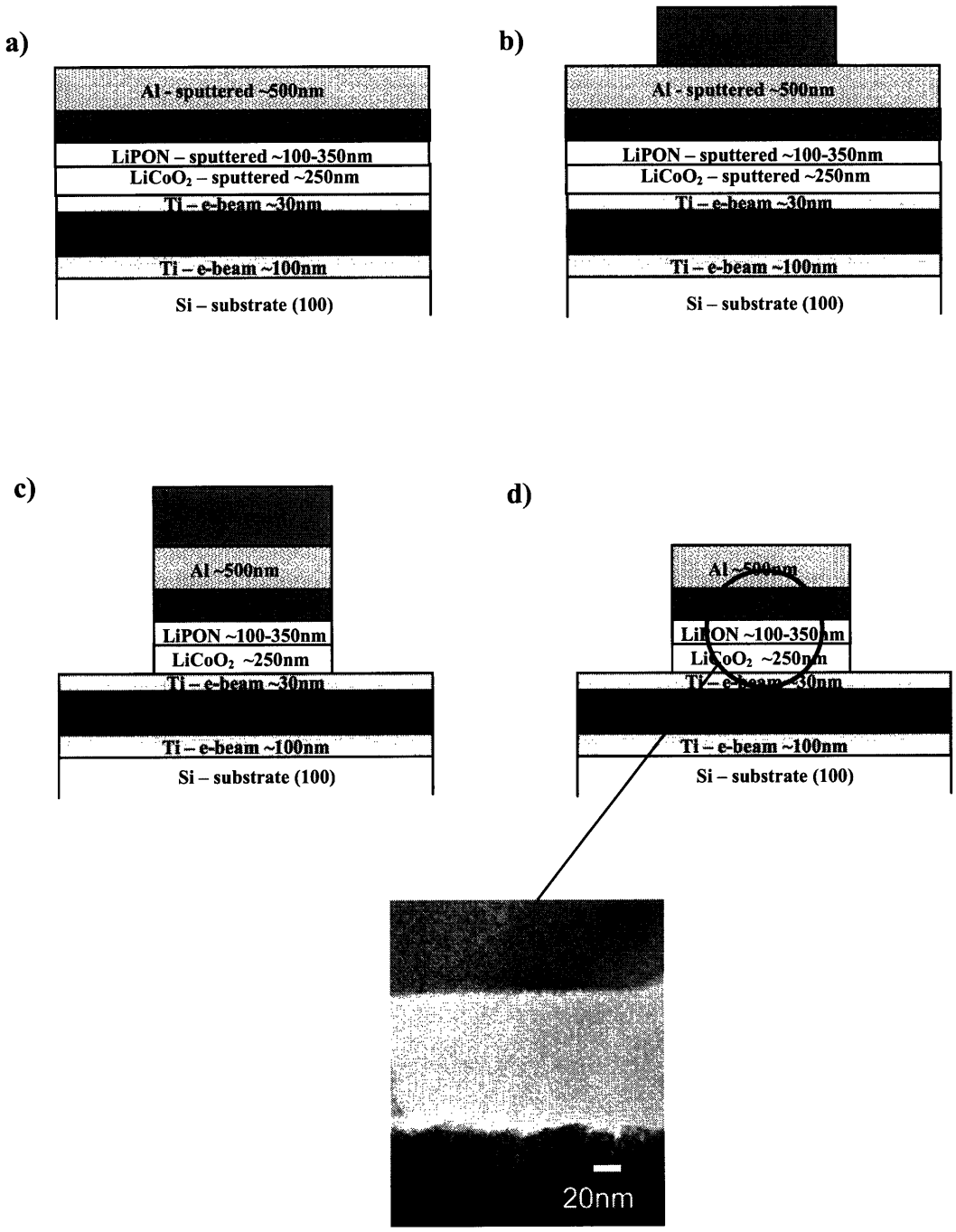


Figure 4-8: A Schematic description of the V_2O_5/LiPON/$LiCoO_2$ cell fabrication process: a) layers deposition, b) photolithography to define the active area, c) wet etch and d) the final structure with a TEM inset of a 100 nm LiPON and its interfaces with the electrodes

In this process, a (100) silicon wafer was cleaned by a standard piranha clean (10 minutes in a solution of H_2SO_4:H_2O_2 in a 3:1 ratio) followed by a quick HF dip (diluted

with water in a 10:1 ratio). A metallization tri-layer consisting of ~100 nm thick titanium layer, a ~500 nm platinum layer, and an adhesion seed layer of 30 nm, was then evaporated on the silicon wafer using the e-beam evaporator in TRL. The wafer was then loaded into the sputtering system for RF sputtering of the cell layers. $LiCoO_2$ was deposited in an argon environment at 200°C using gun power of 250 W and a commercially purchased $LiCoO_2$ target. The thickness of the $LiCoO_2$ electrode film was 250 nm. LiPON was then sputtered from a commercially purchased Li_3PO_4 target at room temperature in a nitrogen environment using gun power of 350W, followed by RF sputtering of V_2O_5 in an argon environment with 3% oxygen background using gun power of 300W. The V_2O_5 film thickness was 200 nm and for the LiPON electrolyte, two thicknesses were studied: 350 nm and 100 nm. The layers deposition was terminated with DC sputtering of the upper contact of aluminum.

The wafer was then patterned using photolithography with a chromium-coated glass mask and a thick resist, type AZ-4620, followed by a wet chemical etch to create square cells of three different sizes of active areas: 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2 (parts b and c in Figure 4-8). The aluminum layer was etched at 50°C for two minutes employing a commercial aluminum etching solution - type A, consisting of H_3PO_4:HNO_3:HAc:H_2O at a ratio of 16:1:1:2. The V_2O_5, LiPON, and $LiCoO_2$ etch was performed at room temperature for 3-5 seconds with a solution of HF:H_2O at a ratio of 1:5. The photoresist was then removed by acetone, creating the final structure seen in Figure 4-8 part d.

4.4 Characterization Methods

4.3.3 Transmission Electron Microscopy (TEM)

TEM is a powerful tool for studying microstructure of thin films with capabilities of high magnifications and atomic resolution. In this microscopy technique, electrons are emitted from a filament, typically LaB6, under high vacuum and are accelerated by a high electric field. The electron beam is controlled by a set of lenses and apertures in the form of electromagnetic coils. An image is created by transmitting the electron beam

through the sample, penetrating through areas of several atomic layers thick, and by the absorbance of the transmitted electrons on a phosphoric screen. The contrast is accomplished by the difference in the number of diffracted electrons from various features of the film microstructure. An image of the reciprocal space can be projected on the screen in the form of a diffraction pattern. The electron wavelength is extremely short as a result of its low mass and the high acceleration voltage used which is typically 200 kV. Therefore the diffraction image is, in effect, an image of the reciprocal lattice of the layer from which it was taken.

Cross-section TEM (XTEM) specimens were prepared by manually polishing face-to-face glued pieces of wafer to thickness of approximately 10 μm using SiC paper flowed by gluing the polished foil onto a 3 mm in diameter copper grid. Final thinning was achieved using a precise ion polishing system (PIPS) by Ar^+ ion milling at 5 V with an incidence angle of 5°.

TEM analysis was performed using both a JEOL 2000FX TEM and a JEOL 2010F TEM operating at 200 kV and 110-120 mA. The technique was used to study the microstructure of the films, quality of interfaces and thickness measurements.

4.3.4 Environmental Scanning Electron Microscope (ESEM)

In SEM, an electron beam is formed in a similar manner to that of a TEM. By scanning the electron beam across a specimen surface, secondary electrons are emitted from it and are detected and translated into an image. SEM has a large depth of field, which allows one to obtain high resolution images at either very low or very high magnifications. A FEI/Philips XL30 FEG ESEM, with a resolution of 3.5 nm at 30 kV, was used to study the films' surfaces.

4.3.5 Atomic Force Microscope (AFM)

In tapping-mode AFM, precise surface topologies are imaged by a silicon cantilever with a sharp tip that oscillates above the sample surface and taps on it in a raster pattern. The surface topography is translated into an image by a piezoelectric crystal from the forces caused by the deflection of the tip. Those are coupled with a HeNe

laser which is reflected of the tip edge allowing the measurement of the tip bending. A Digital Instrument Nanoscope III AFM, in tapping mode, was used to study surface morphology and roughness over 1 μm×1 μm scanned areas.

4.3.6 Secondary Ion Mass Spectroscopy (SIMS)

SIMS is a highly sensitive technique for obtaining materials composition and a composition depth profile of samples. Typically, a Cs^+ or O_2^+ ion beam is used to bombard a specimen surface, simultaneously with detection of the secondary ions that were emitted from the surface. The emitted ions are detected and analyzed using a mass spectrometer by the radius of their movement under an applied combination of electric and magnetic fields. The film composition is determined by comparing the ions relative counts to the ones of a reference sample with a known composition. A depth profile of composition is obtained by monitoring the sputtering rate during the detection process. SIMS with a Cs^+ beam of 5.5 kV was used to determine the composition of the $LiCoO_2$ sputtered film.

4.3.7 X-Ray Photoemission Spectroscopy (XPS)

In XPS, X-ray photon beam, typically Al-Kα of 1486.6 eV or Mg-Kα of 1253.6 eV, under ultra high vacuum, is causing the emission of electrons from core energy levels of elements on a specimen's surface. The emitted electrons are detected, their characteristic kinetic energy is measured, and their binding energy is calculated from the conservation of energy law. XPS is useful to analyze the chemical composition of a surface layer and can also supply information on bonding types of an element by the shape and position of its characteristic peak. In this work, XPS technique, with an Al-Kα source, was used to analyze the chemical composition of the deposited LiPON films and their nitrogen content.

4.3.8 Electrical Measurements, I-V

An HP 4156A and 4156C parameter analyzers in conjunction with a probe-station were used to study the cells charge and discharge behavior. The cells leads were contacted with 5 or 10μm radius probe tips. Current and voltage measurements were performed by forcing a constant current while measuring the voltage formed between the electrodes, while one of them is grounded. An action of 'charge' is defined when a positive current is forced to flow from the parameter analyzer into the sample through the $LiCoO_2$ cathode and to the polysilicon in the first material system or to the V_2O_5 electrode in the second material system. A 'discharge' is accomplished by forcing a negative current, defined as such since it is flowing from the cell, from the lithiated polysilicon or V_2O_5, through the $LiCoO_2$ electrode to the parameter analyzer. A schematic illustration of the measurement setup for the first material system can be seen in Figure 4-9. In the second material system cells, the aluminum and platinum contacts were probed and a positive current were defined going from the $LiCoO_2$ electrode to the V_2O_5 one (charge).

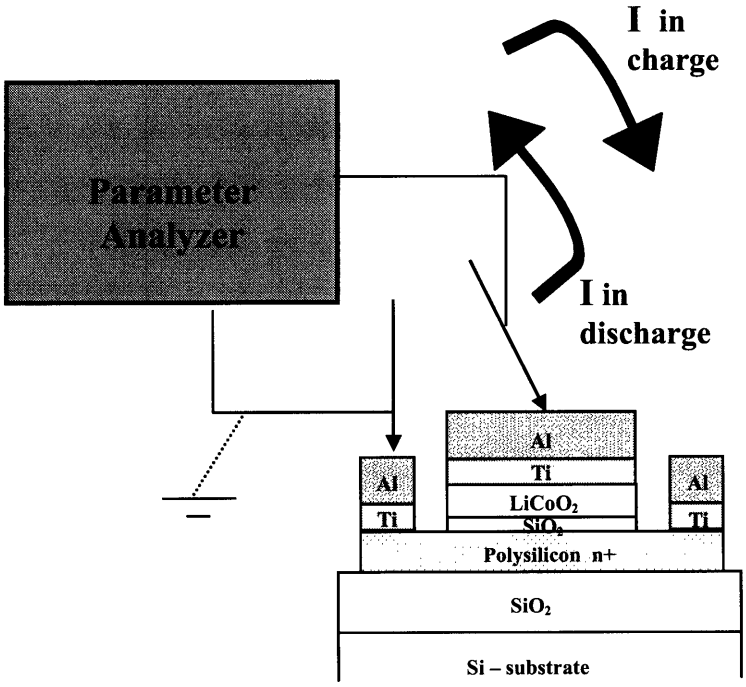


Figure 4-9: A schematic illustration of the I-V measurement set up

The cells were charged and discharged in rates from 0.05 C to 2 C, where 1 C rate is the current density required to charge or discharge the cell in one hour. The corresponding current values applied were in the range of 1.25 nA-2.5 μA depending on the active-area size of the cell and the rate required. In a specific case of studying precipitation appearance, an extreme rate of 15C was used. An explanation of the C rate calculation as well as a table describing the currents used for different sizes at different rates can be found in Appendix B. The apparatus used for charge and discharge measurements in this work is not designed or utilized for extremely long testing times as is the equipment used for battery testing; therefore, charge and discharge were performed for limited periods of time.

4.3.9 Impedance Measurements

The complex impedance of a pure capacitor under AC voltage is given by:

$$z = \frac{1}{i\omega C} = -\frac{i}{\omega C}$$ **Equation 4-5**

Where C is the capacitance and ω is the angular frequency:

$$\omega = 2\pi f$$ **Equation 4-6**

The complex impedance of a resistor is simply equal to its resistance:

$$z = R$$ **Equation 4-7**

The complex impedance of a resistor in series with a capacitor would be the sum of Equation 4-5 and Equation 4-7. The complex impedance of a resistor connected in parallel with a capacitor would be the reciprocal sum of their reciprocal impedances as shown in Equation 4-8 and Equation 4-9:

$$\frac{1}{z_p} = \frac{1}{R} + i\omega C$$ **Equation 4-8**

$$Z_p = \frac{R}{1 + R\omega C} - i\frac{R^2\omega C}{1 + R^2\omega^2 C^2}$$ **Equation 4-9**

Impedance measurements are a useful technique for modeling the electrical behavior of a battery using circuit elements, typically resistors and capacitors, to represent various elements of the cell. A small AC signal is applied to the cell and its AC current response is measured as well as the phase shift between the current and the voltage. The results are often presented in the complex plain as function of frequency in the form of a Cole-Cole or a Nyquist plot. The basic battery reactions can usually be modeled by a set of resistors and capacitors in series or in parallel. The electrolyte and electrodes contribute to the resistance and the interfaces contribute to the capacitance of the equivalent circuit. In the case of a resistor and a capacitor connected in parallel, the appropriate Cole-Cole plot will be in the shape of a semi-circle as can be seen in Figure 4-10. The imaginary component of the impedance falls to zero at high frequencies, because it presents no impedance, similar to a short in a circuit. All of the current is charging current and only the ohmic resistance is the significant one. At very low frequencies, the capacitor impedance contribution is high, similar to a disconnect in the circuit, therefore, current flows mostly through the resistor connected in parallel[123]. This is supported mathematically by Equation 4-9 in which the imaginary component is diminishing for very high or very low frequencies.

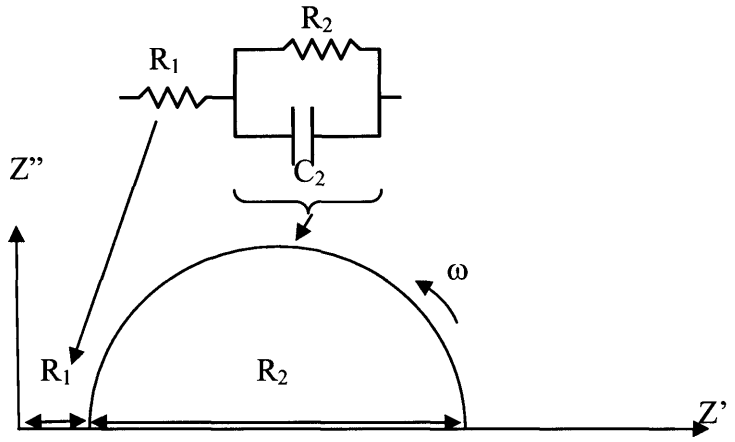


Figure 4-10: A schematic Cole-Cole plot of an equivalent circuit of a resistor and a capacitor connected in parallel in addition to a resistor connected in series

In this work, impedance measurements were used to characterize the $LiCoO_2/SiO_2$/polysilicon cells containing a 9 nm thick electrolyte. In the study of the second material system, impedance measurement techniques were used to obtain the ionic conductivity of the LiPON deposited films.

Samples for ionic conductivity measurements were prepared by depositing LiPON onto an aluminum foil, followed by punching out 14 mm diameter discs from the aluminum foil. The discs' edges were then covered by a ring of insulating tape with 10 mm and 18 mm inner and outer diameters respectively prior to aluminum sputtering on top creating an Al/LiPON/Al structure. An example of the Cole-Cole plot achieved from a LiPON film deposited at 350 W gun power and 40 sccm N_2 flow, at deposition pressure of 5×10^{-2} Torr, can be seen in Figure 4-11.

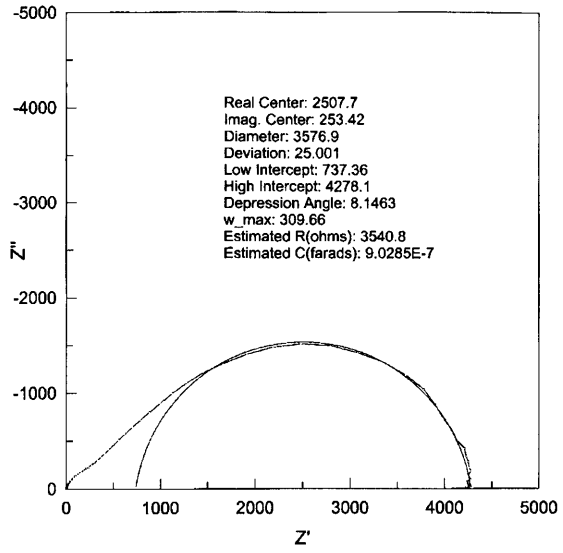


Figure 4-11: A Cole-Cole plot presenting the impedance of a LiPON film between two Al electrodes.

A semi-circle is fitted to the low frequency area of the curve in order to extract the film ionic resistance. The film ionic conductivity is then calculated by plugging the semi-circle diameter in:

$$\sigma = \frac{1}{R} \times \frac{t}{A}$$ **Equation 4-10**

Where t is the film thickness and A is the exposed area.

Impedance measurements of the first material system were performed by Sue Babinec from The Dow Chemical Company. A 1255B Solartron frequency response analyzer (FRA) was used. An AC voltage signal of 100 mV was applied and in the frequency range of $1\text{-}10^5$ Hz.

Impedance measurements for determining the LiPON conductivity were performed using a 1255 Solatron FRA or an SI 1260 Impedance/Gain phase analyzer. An AC voltage signal of 10 mA was applied in the frequency range of $0.1\text{-}10^6$ Hz. The results were plotted and analyzed by using the Z-Plot and Z-View program of Scribner Associates.

5 Electrochemically-Controlled Transport of Lithium through ultra-thin SiO2 for Novel Electronic and Optoelectronic Devices

5.1 Introduction

The objective of the work described in this thesis was to develop and study a thin-film solid state battery, compatible with silicon integrated circuit (IC) technology in terms of fabrication methods, materials, and performance. The low power requirements of CMOS-technology-based devices have allowed for new materials to be considered for battery applications, materials that are known to the microelectronic industry but are not used in power cells.

One of these materials, a most commonly used and well-studied material in silicon IC technology, is silicon dioxide (SiO_2). The process control for thin SiO_2 layers, which is a result of microelectronic advances, its insulating properties, and its permeability to light ions have been the motivation to investigate the usage of SiO_2 as a solid-state electrolyte in an integrated thin-film battery. Common solid-state electrolytes currently in use consist of lithium-containing or lithium-doped electronically insulating material, typically 1-2 μm thick[47,51,63,70,101,105,106], in which the charge-carriers migrate through a lithium-ions chain within the structure of the electrolyte. Examples of such solid-state electrolytes are described in detail in Section 2.3.3.

SiO_2 is an unconventional electrolyte in that it neither contains lithium nor is it doped with a lithium-containing salt. Ionic conduction in SiO_2 is performed via diffusion across the layer. One might expect that an electrolyte that does not inherently contain lithium ions would become positively charged when Li^+ ions diffuse through it, thereby creating an electric field that would halt the diffusion. However, the SiO_2 electrolyte layer can be created sufficiently thin to allow rapid diffusion of lithium ions through it.

This chapter describes the study of controlled transport of lithium through an ultra-thin lithium-free SiO_2, 9-40 nm thick, for electrolyte application. The SiO_2 is grown by thermal oxidation from a polysilicon layer, which serves as the anode in this nano-battery. The use of heavily-doped polysilicon as an electrode is highly advantageous from a processing perspective, since its formation can be readily integrated into conventional micro-device fabrication processes. Studies done on the lithium-silicon system are described in Section 3.1.2. The cathode in the studied thin-film battery stack is a nanocrystalline layer of $LiCoO_2$ (see Section 3.1.3). The $LiCoO_2/SiO_2$/polysilicon cells were fabricated and patterned using conventional microelectronics processing.

The work described in this chapter introduces SiO_2 as an interesting material candidate for battery applications and demonstrates the employment of an ultra-thin solid-state lithium-free electrolyte candidate in a lithium ion battery. In addition, the controlled ion transport demonstrated in this work can potentially be used for other novel electronic or optoelectronic devices.

5.2 Fabrication of the $LiCoO_2/SiO_2$/polysilicon cells

The method used to fabricate the $LiCoO_2/SiO_2$/polysilicon cells was described in Chapter 4. In this Chapter, the study of three thicknesses of SiO2 is presented, 7 nm, 9 nm, and 40 nm. Cells of three different sizes of active areas were studied: 5×5 mm^2, 2×2 mm^2, and 1×1 mm^2. The corresponding polysilicon anode areas were: 9×9 mm^2, 3.6×3.6 mm^2, and 1.8×1.8 mm^2. The cross section of the final structure of a cell with 9 nm thick SiO_2 layer grown from a 14 nm undoped polysilicon, can be see in Figure 5-1.

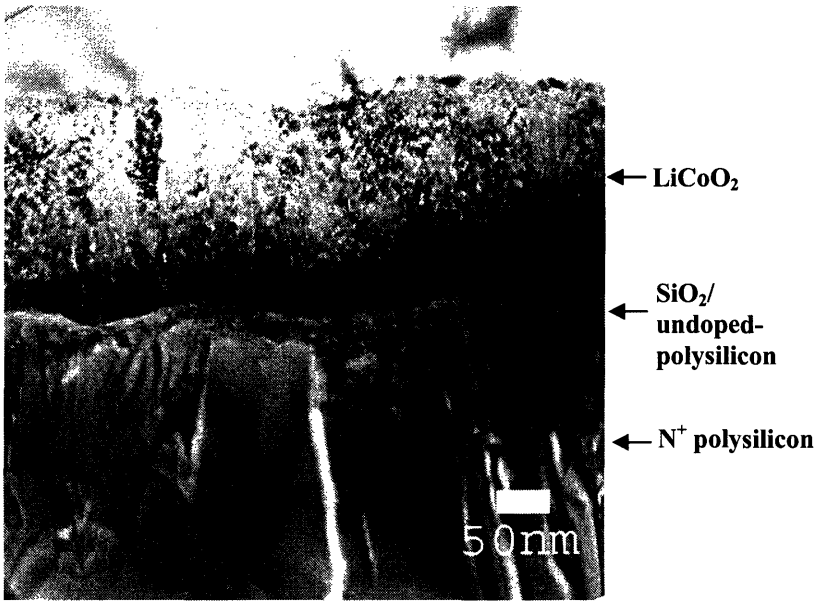


Figure 5-1: A XTEM image of the $LiCoO_2/SiO_2$/polysilicon cell consisting of a 9nm thick SiO_2 layer

The deposited cells consist of continuous films and high quality interfaces between the layers. Recall from Chapter 3, that LiCoO2 crystallographic structure is hexagonal in which the oxygen anions form a closed packed network with the lithium and cobalt cations on the alternating (111) planes of the cubic rock salt sub-lattice. The $LiCoO_2/SiO_2$/polysilicon cells were fabricated in their discharged state, in which lithium is intercalated in the CoO_2 host lattice.

For SiO_2 to function as an electrolyte lithium should be transferred during charging, that is, be de-intercalated from the Li_xCoO_2 cathode and while remaining in its ionic stage, it should pass through the electrolyte. The SiO_2 should remain electrically insulating throughout this process.

5.3 Electrical Testing

5.3.1 The Effect of Cell Active-Area Size

The cells were tested by forcing a constant current while monitoring the voltage between the electrodes in order to study their charge and discharge behavior. Shown in

Figure 5-2, are the charge and discharge plots obtained for different sizes of cells with a current density corresponding to a charge rate of 0.25C or full charge in four hours.

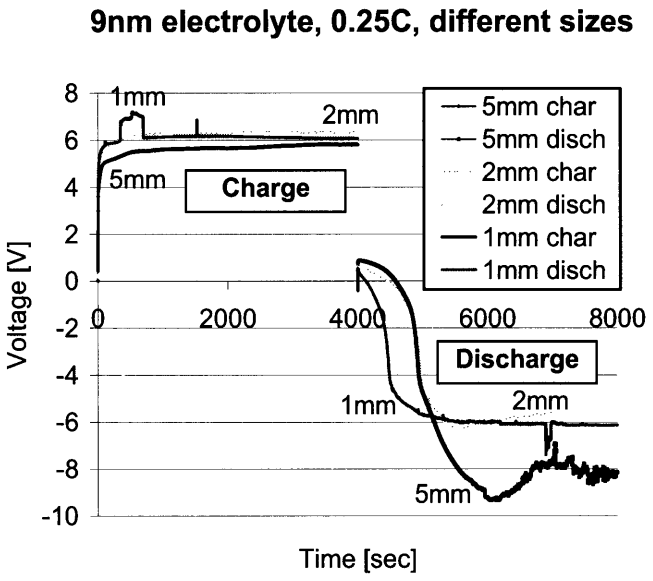


Figure 5-2: Charge and discharge behavior at 0.25C of cells of different sizes with 9nm thick SiO2 electrolyte

The cells were charged by forcing a positive current to flow into them for 4000 seconds and then discharged by forcing a negative current to flow from the cells into the parameter analyzer. The voltage between the electrodes is measured for the charge and discharge steps as function of time.

Upon charging the cell, electrons are released to the external circuit as lithium is de-intercalated. The lithium ions diffuse through the thin SiO_2 layer and receive electrons at the SiO_2/polysilicon interface. When receiving an electron, singly-charged Li^+ ions become electrically neutral and react with neighboring silicon atoms to form one of four Li-Si compounds: $Li_{12}Si_7$, Li_7Si_3, $Li_{13}Si_4$, or $Li_{21}Si_5$. To compensate for the lithium de-intercalation from the cathode, the oxidation state of the cobalt atoms changes from Co^{+3} to Co^{+4}. Upon charging, the difference in the lithium chemical potential between the electrodes is increasing and therefore the measured voltage is increasing with charge as can be seen in Figure 5-2. The OCV between elemental silicon and lithium has been measured to be approximately 1 V[38,92] and it was found to be dependent on silicon

morphology by Gao *et al.*[28]. The OCV between Li_xCoO_2 and lithium is typically in the range of 3.5-4.7 V[10,11,14,58,70-72,74,76,77,124] depending on lithium concentration and film morphology. Combining these together, we estimate the equilibrium voltage between the electrodes in the $LiCoO_2/SiO_2$/polysilicon cell to be about 2.5-3 V, a value which should increase further with charging. The higher measured voltage is due to the high series resistance of the cells, R_s, as well as other reaction and kinetic barriers, η, (polarization in battery terminology):

$$V_{measured} = V_{OC} + IR_s + \eta \qquad \textbf{Equation 5-1}$$

Discharge behavior measurements are performed by forcing a current from the cells into the parameter analyzer. The current flowing in that direction is defined by the parameter analyzer as negative. Upon discharging the cells, the lithium-silicon compounds, which are believed to form during charging, decompose and the lithium ions are transferred back through the SiO_2 where they are re-intercalated between the CoO_2 layers, at which point Co^{+4} reverts to Co^{+3}. The IR_s drop in this case is negative as the current forced by the parameter analyzer is negative. The discharge is characterized by a decreasing potential difference, V_{OC}. When V_{OC} becomes smaller than IR_s in their absolute values, the polarity of the voltage will change as can be seen in Figure 5-2.

Additional voltage drops can be created by kinetic barriers and partial loss of the lithium atoms in the polysilicon electrode; as the discharge progresses, greater electric fields are required to draw the constant current. In the initial stage of discharge process, the right side of Figure 5-2, where voltage is decreasing with time, the voltage values are lower for smaller cell sizes compared to larger cells. This voltage difference is due to the fact that there is more Li^+ in the larger area cell leading initially to higher current from the electrochemical process (therefore less voltage is required by the parameter analyzer to drive the constant current in this experiment). However, as the discharge process proceeds beyond ~6000 seconds, the correlation of discharge voltage to area size is now inverted. Recall that the measured-device geometry requires a lateral bottom contact (Figure 4-5), and therefore when device area gets large, a large series resistance will exist

between the outer anode ring contact and the center of the larger area. A large voltage will therefore be needed to extract lithium ions from the center of the device.

Note that the duration of the initially positive stage of the voltage is longer for larger active area cells due to both a larger volume of charge carriers. Since the charging voltage is increased by the series resistance and the discharging voltage is decreased by the series resistance, the overall cell resistance can be roughly estimated by half of the difference between the end value of the charging voltage and the starting discharging voltage for the different sizes of cells. The estimated cells resistance values are: ~4.25×10^6 Ω, ~2.85×10^7 Ω, and ~1×10^8 Ω for the 5 mm, 2 mm, and 1 mm square edge cells, respectively. Note that at the initial stage of the discharge, the lateral series resistance is less dominant and more lithium ions are available at larger cells, leading to higher positive voltage and lower cell resistance in this evaluation. Moreover, this estimation does not take into account kinetic barriers, which are lower when more lithium ions are present.

Measuring positive voltage values while driving current from the $LiCoO_2/SiO_2$/polysilicon deposited cell is a clear indication of power upon discharging. These measurements suggest that a thin layer of lithium-free SiO_2 can function as an electrolyte in an electrochemical cell.

5.3.2 Cell Stability

Measurements of the OCV with time were performed on 2 mm cells with 9 nm thick SiO_2 electrolyte. The cells were charged for 4000 seconds at 0.25C rate and the OCV measurement followed immediately and consisted of recording the voltage between the contacts every 2 seconds for 1800 seconds (half an hour) while the current was set to zero. The charge curve followed by the OCV measurement can be seen in Figure 5-3. It can be seen that the OCV measured did not vary over the course of the measurement time, which is an indication of good cell's stability.

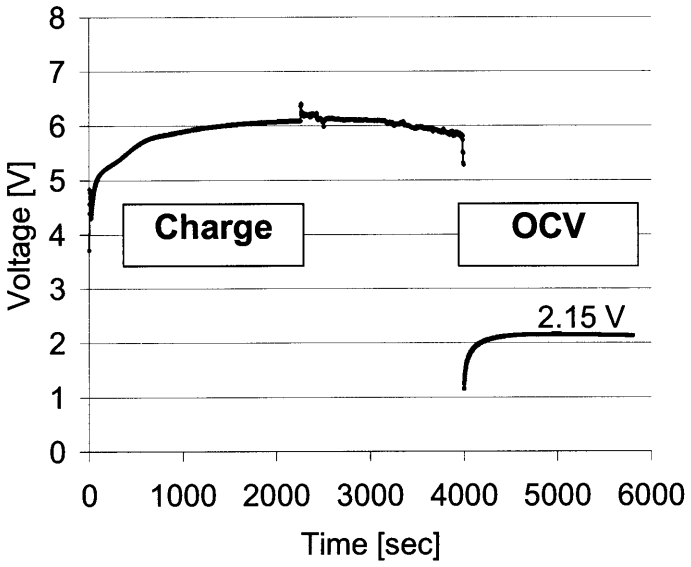


Figure 5-3: OCV measurement for 2 mm cells consisting of a 9 nm thick SiO_2 layer

5.3.3 Current Density Effect on Cell Discharge

In order to examine the effect of charge/discharge rate on the cells, the cells were tested at different rates, i.e. from 0.1C to 1C (current densities corresponding to 1-10 hours of charge). The discharge plots of the 2 mm cell with a 9 nm thick SiO_2 electrolyte in different rates are presented in Figure 5-4. Note that 10 V was set to be the compliance value in order to prevent extremely high voltage values from damaging the cells.

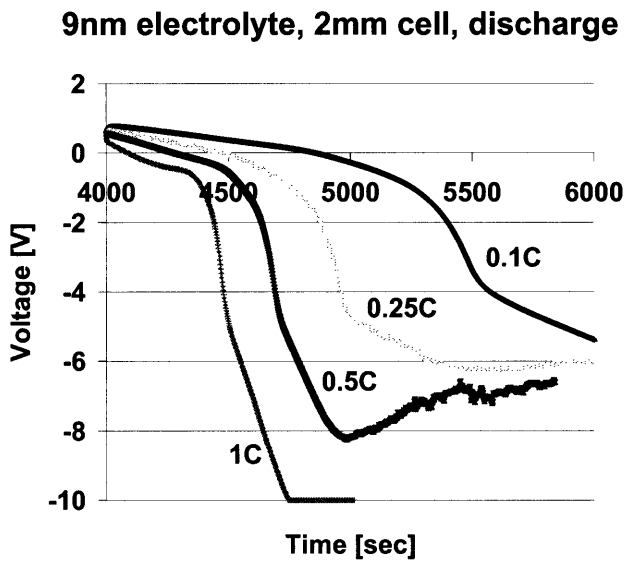


Figure 5-4: Discharge at different rates of the 2mm size cell with 9nm thick SiO_2

Due to technical constraints imposed by the probe station used in the measurements (as described in Chapter 4) the cells were charged to different levels of total charge. Therefore, when studying the rate affect, one should consider the percentage of charge transferred back during discharge in addition to the absolute value of the charge received by the cell. The time period of charging was multiplied by the current value to calculate the actual charge passing between the electrodes. In discharge, the charge was estimated by multiplying the current by the time in which the voltage was positive. The amount of charge passed through the cell when charging and discharging and the percentage of the reversible charge (discharge divided by charge) can be seen in Table 5-1:

Rate	Charge in Charging [Cb]	Charge in Discharging [Cb]	Percentage of reversible charge
0.1C	1.6×10^{-4}	3.39×10^{-5}	21.19
0.25C	4×10^{-4}	4.66×10^{-5}	11.65
0.5C	5.6×10^{-4}	5.4×10^{-5}	9.64
1C	1.2×10^{-3}	3.44×10^{-5}	2.86

Table 5-1: Charge exchange in charging and discharging the 2 mm size 9 nm thick oxide cell

These data shown in Figure 5-4 and in Table 5-1 indicate that slow charge and discharge rates result in more charge being stored and retrieved. Figure 5-4 demonstrates this by the longer period of positive voltage during discharging and the higher voltage during discharging, and Table 5-1 shows that there is a higher percentage of charge retrieved when discharging at lower rates.

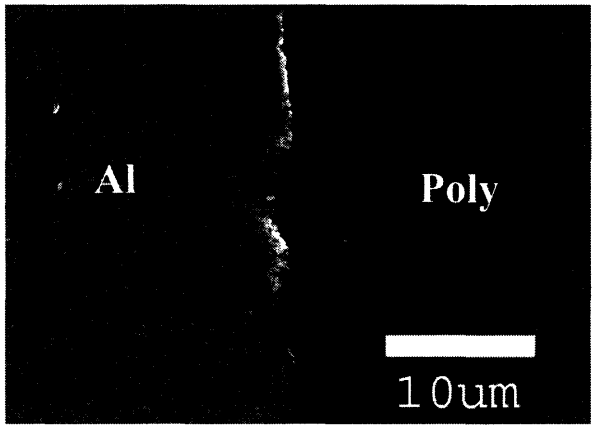
One possible explanation for this observation is that lower charging rates reduce kinetic barriers, thereby allowing the reactions to proceed at a pace closer to equilibrium. Other published examples of charge and discharge measurements involving Li_xCoO_2 also show higher capacities and higher voltage values for slower rates[26,70,71]. Takano *et al.* speculated that at large current densities, due to diffusion-controlled processes, lithium is plated on the surface of $LiCoO_2$ resulting in a large voltage drop in a carbon – $LiCoO_2$ battery with a liquid electrolyte[125]. Similarly, for the $LiCoO_2/SiO_2$/polysilicon cells, high discharge rates might lead to the formation of lithium-rich alloys clusters closer to the SiO_2/polysiliocn interface, thereby causing stresses and large local concentration gradients and inhibiting further lithium diffusion.

5.4 Precipitation on Polysilicon Surface

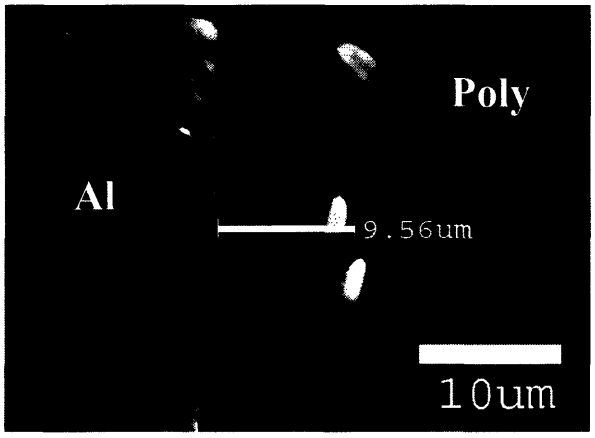
The top-contact geometry of the cell enables the observation of the polysilicon anode surface at the lower contact region, where lateral conductivity is necessary. At increasing charge and discharge rates, precipitates were observed forming at the edges of the active area in this region, on the surface of the polysilicon. Figure 5-5 shows SEM

images of the polysilicon surface at the vicinity of the active area edge of three cells; one of them was not tested, one was tested at a rate of 0.5C and the third was tested at an extreme rate of 15C. Shown in the left hand side of each image is the top aluminum cathode contact layer and shown in the right hand side is the polysilicon surface between the two contacts.

a)



b)



c)

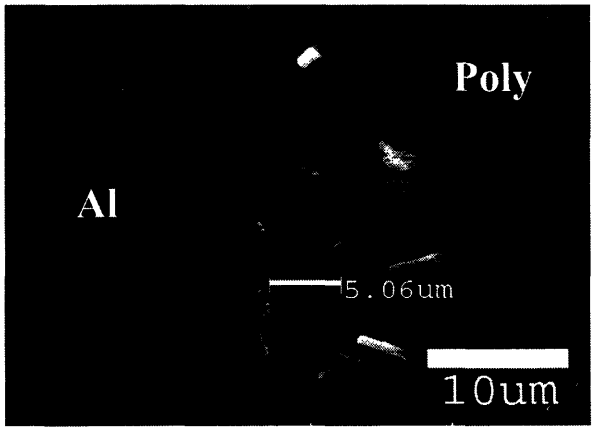


Figure 5-5: SEM pictures of 3 cell active area edges; a) not tested, b) tested at 0.5C rate and c) tested at 15C rate

As can be seen from looking at the micrographs, more precipitates were observed when testing at higher rates and they appear closer to the inner square active area edge. Those precipitates are believed to originate from the reaction between the lithium and silicon during the cells charge. A closer look at one of the precipitates in an SEM image taken at higher magnification is presented in Figure 5-6.

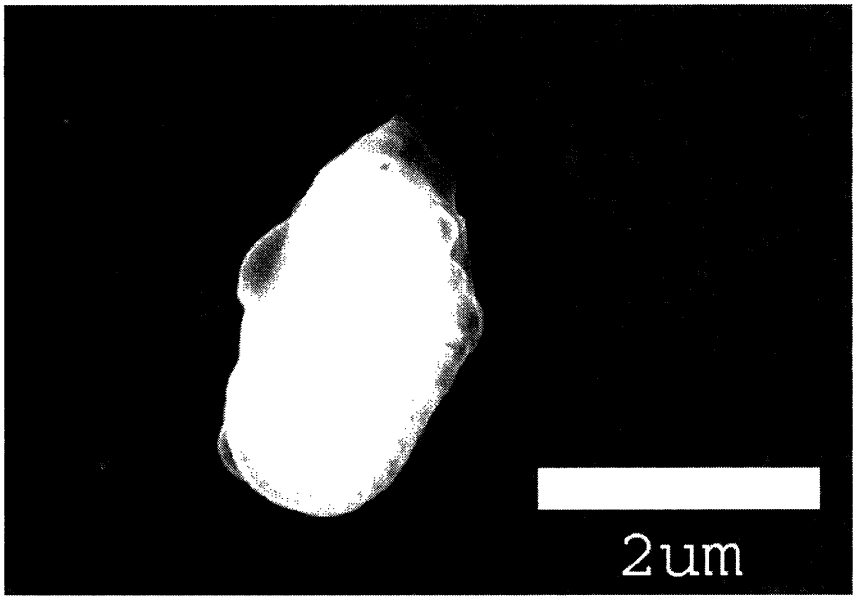


Figure 5-6: SEM image of one of the precipitates at higher magnification

Lithium and silicon form four different compounds mentioned previously and the formation reaction involves a large volume change of more than e.g. 200% for the orthorhombic $Li_{12}Si_7$. During the charge process, lithium ions are transported to the polysilicon electrode where they each receive an electron and react with silicon. The higher the charge rate is, the less time there is for the lithium ions to diffuse and spread homogenously within the polysilicon layer. Local areas with higher lithium concentrations are formed, leading to the nucleation and the eruption of the Li-Si precipitates to the surface at shorter distances from the active area edge. These precipitates do not dissolve upon discharging. This hypothesis is also supported by the low percentage or reversible charge that was measured and its dependence on the charging rate as was shown in Section 5.3.3.

5.5 Circuit Modeling of the Cell

5.5.1 Impedance Measurements

In order to model the complete set of capacitances and resistances in the structure and establish an electronic model of the device, impedance measurements were performed on cells with an active area of 2x2 mm^2 and a 9 nm thick electrolyte. An AC voltage signal of 100 mV was applied and the response current was measured at frequencies in the range of $1\text{-}10^5$ Hz. Due to the high series resistance of our cells, the applied voltage signal was increased higher than normal in order to obtain sufficiently strong signal for measurement. Linear response, i.e. an identical angular frequency for the response current and the applied voltage, was assumed. The complex plane representation of the impedance at different frequencies, also known as Cole-Cole or Nyquest plot, for one of the cells is shown in Figure 5-7. The data represented by filled diamonds are the negative of the measured imaginary part of the impedance versus the real part at different frequencies.

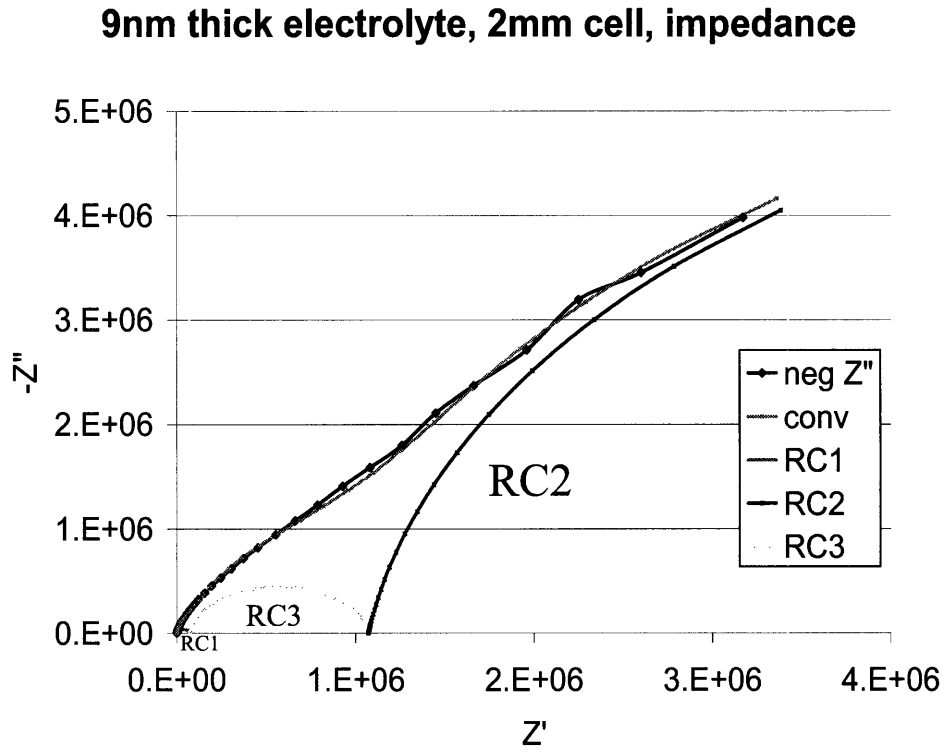


Figure 5-7: A cole-cole plot of one of the 2 mm edge cells (9 nm thick oxide) with three depressed semi-circles composing the theoretical plot corresponding to an equivalent circuit.

Using the values obtained from the above impedance measurements, an equivalent circuit for the $LiCoO_2/SiO_2$/polysilicon cell was formulated, the structure of which is presented in Figure 5-8. A theoretical impedance curve based on this suggested equivalent circuit was calculated using the software Z-view, the results of which are presented in Figure 5-7 as a bright filled diamond curve. Each component of the circuit consists of a resistor and a capacitor or a constant phase element (CPE) connected in parallel and corresponds to one of the depressed semi-circles in Figure 5-7.

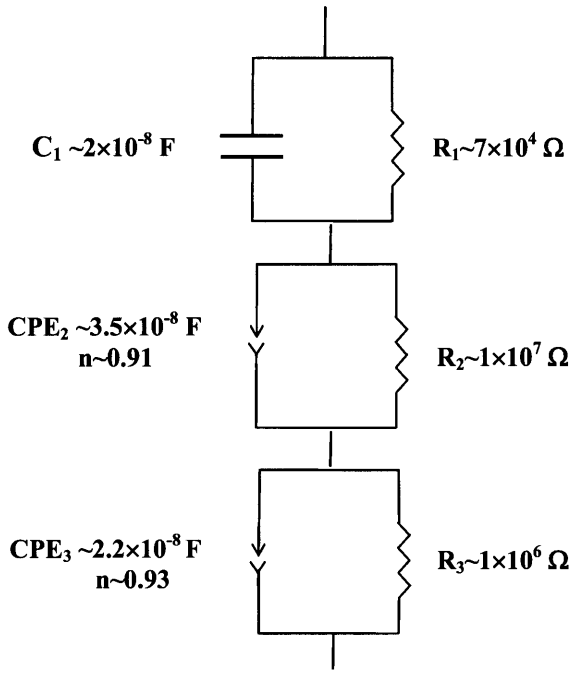


Figure 5-8: The $LiCoO_2/SiO_2$/polysilicon cell equivalent circuit based on impedance measurements

The three arcs, RC1, RC2, and RC3, are inseparable by frequency when convoluted as can be seen in the experimental plot. CPEs are usually used to describe interfacial impedances when a pure capacitor does not sufficiently describe the experimental plot. In practice, CPE can deviate from a pure capacitance by various forms of inhomogeneity such as roughness at the electrolyte/electrode interface. The impedance form of a CPE is described in:

$$Z(\omega) = A(j\omega)^{-n} \qquad \textbf{Equation 5-2}$$

where A is a frequency-independent constant and n is a constant between 0.5 and 1 (equal to 1 for a pure capacitor[126]).

The calculated plot of the equivalent circuit, shown with smaller and brighter filled diamond legends, was de-convoluted to three separate depressed semi-circles that are drawn as well in Figure 5-7. By looking at Figure 5-7, the plot based on the equivalent circuit describes quite well the measured data. However, it is unfeasible to directly attribute the different current-impeding components in the suggested equivalent

circuit to separate battery elements and processes. It can be assumed that the resistors in the circuit represent the electronic and ionic resistances of the electrodes, the ionic resistance of the electrolyte, as well as any kinetic barriers. The capacitors and constant phase elements in the circuit are representative of charge transfer across the electrolyte/electrode interfaces which include the capacitance induced by the polarization of the dielectric SiO_2 layer and its interfaces with the $LiCoO_2$ and polysilicon electrodes.

5.5.2 Circuit Elements Analysis

In the process of identifying some of the main components in the circuit model, the overall cell series resistance can be estimated by assuming that its largest contribution originates from the electrolyte series resistance. Cells with different oxide thickness were compared in order to confirm the cell resistance independently. Cells with 40 nm and 9 nm thick oxide electrolyte layers are discussed in this chapter. The initial voltage rise in charging is a result of the IR_s drop and directly depends on the electrolyte thickness. The other contribution to the over-potential, i.e. the addition to the voltage, due to kinetic hindrances can be minimized by charging at low rates, therefore estimating the voltage drop due to the cell resistance at low charging rates is more accurate.

Shown in Figure 5-9 are the cell response curves of two cells charged at 0.25C. With the exception of their oxide thickness values of 40 and 9 nm, the structures are otherwise identical. The initial voltage increase above 2.5 V which is the expected open circuit voltage, for these structures can be used in conjunction with Equation 5-1 to estimate the resistance of the cells with 40 and 9 nm thick oxide to be $9.4\times10^7\ \Omega$ and $4.1\times10^7\ \Omega$, respectively. The first value is higher than the theoretical equivalent circuit value given in Figure 5-8 for R_2 however, still suggests that the major contribution to the cell resistance comes from the oxide layer.

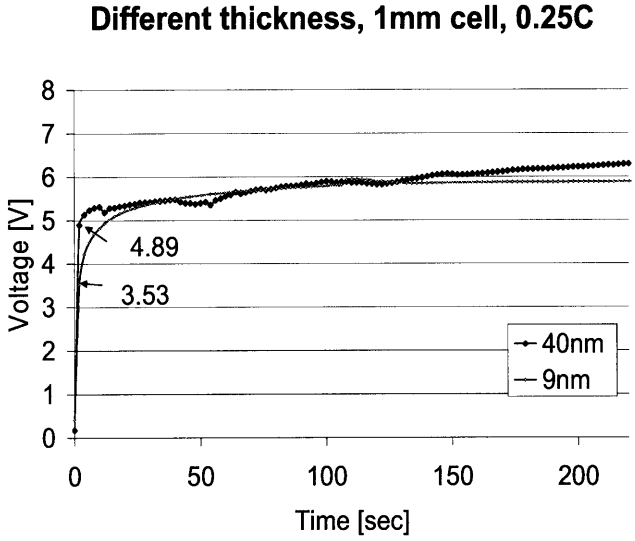


Figure 5-9: Initial voltage increase in charging two 2 mm edge cells with SiO_2 thicknesses of 9 nm and 40 nm

The bulk electronic resistivity of SiO_2 is $\rho \sim 10^{15} \Omega cm$[104]. Based on this value the resistance of a 9 nm and 40 nm thick SiO_2 can be roughly estimated as: $\sim 9 \times 10^8 \Omega$ and $4 \times 10^9 \Omega$, respectively. Those values are higher than the experimental result which represents both electronic and ionic contributions. The presence of lithium ions as charge carriers reduces the overall resistance which is normally measured with ions-clean ambience. Another reason for the difference can originate in the thin-film nature of the oxide and the fact that it was grown via the thermal oxidation of polysilicon as opposed to single crystal or epitaxial silicon layers.

Similarly, the capacitance of the electrolyte can be independently calculated and compared to the value obtained by the circuit modeling. The capacitance, C, of the SiO_2 layer is given by:

$$C = \frac{A \varepsilon_0 \varepsilon}{d}$$ **Equation 5-3**

Where $A = 4$ mm^2 is the active area of the 2 mm edge cell that was tested, $\varepsilon = 4$ is the relative dielectric constant of SiO_2, $d = 9$nm is the measured oxide thickness and

ε_0=8.85×10^{-14} F/cm is the permittivity of vacuum. Inserting these numbers results in a calculated capacitance value of ~ 6.29×10^{-8} F, which is comparable to the fitted values of the circuit presented in Figure 5-8. This value is, however, three orders of magnitude lower than the cell capacitance as shown in Figure 5-4 and Table 5-1, indicating that the majority of power was induced by electrochemical reactions and not by the oxide electronic capacitance.

Based on the calculations described above, we can identify the second element of the circuit model in Figure 5-8, composed of R_2 and CPE_2, as representing the electrolyte in the cell. It is clear that the SiO_2 electrolyte, as modeled in this structure for this thickness, is the highest barrier to current flow in the cell. The other two elements can be reasonably attributed to the effects of interfaces and kinetic barriers of the reduction-oxidation reaction and to conduction within the electrodes.

5.6 Reducing Cell's Resistance

The most dominant contribution to the cell's resistance originates from the electrolyte. Hence, one of the most effective ways to decrease the series resistance of a battery and improve the cell's performance would be to reduce the electrolyte thickness. However, an attempt of cell fabrication with a thinner SiO_2 layer resulted in the vast majority of the cells being shorted, thereby making their current-voltage behavior equivalent to that of a resistor. High resolution XTEM imaging revealed thickness variations in the ultra-thin SiO_2 that can be attributed to anisotropy in the oxidation rate of the polysilicon layer and its granular structure. A HRXTEM image showing the SiO_2 interfaces of the $LiCoO_2/SiO_2$/polysilicon structure can be seen in Figure 5-10.

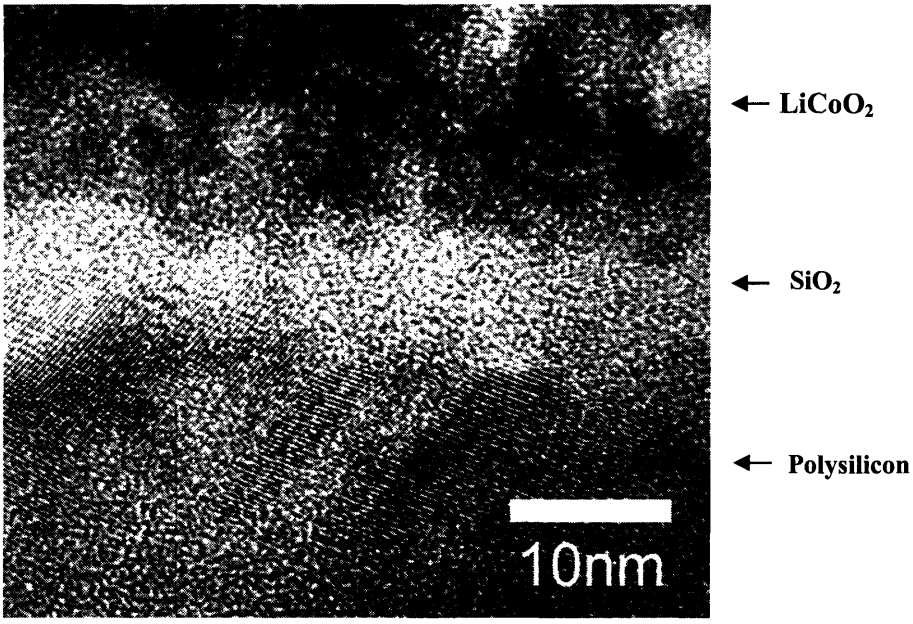


Figure 5-10: A HRXTEM image of the $LiCoO_2/SiO_2$/polysilicon layers with a 0-7 nm thick SiO_2

The SiO_2 thickness distribution varies between 0-7 nm leading to the creation of shorting paths between the electrodes. The dielectric breakdown strength of a thermally grown SiO_2 is ~10^7 V/cm[104]. The breakdown voltage of a 7 nm, high quality thermal SiO_2 is therefore approximately 7 V which is a value reached during charging and discharging of the cells. Furthermore, as 7 nm represents the thickest portion of the layer, the calculated breakdown voltage of 7 V represents an upper limit, and would therefore be much lower for thinner local areas of the oxide. Thus, the breakdown point of the SiO_2 is reached during the cell charging and discharging. This breakdown results in a transition of the SiO_2 from an insulating to an electronically conductive layer, thereby preventing it from functioning as the cell electrolyte under the measured voltage values.

5.7 Summary and Conclusions

Described above is the study of two existing CMOS materials and one new material for the construction of a potential battery or novel device structure. The study described in this chapter explored the use of thermal silicon dioxide as thin as 9 nm acting as an electrolyte layer in the solid state battery integrated on silicon. Other

components of the thin-film battery consisted of RF sputtered $LiCoO_2$ as the cathode and highly doped n-type polysilicon grown by LPCVD as the anode. All structures were fabricated using conventional microelectronics fabrication technology. The charge and discharge behavior of the $LiCoO_2/SiO_2$/polysilicon cells was studied. Impedance measurements were used to model the equivalent circuit for the potential ultra-thin battery and its structure and layer interfaces were evaluated by electron microscopy imaging. The series resistance of the SiO_2 electrolyte is high, even at thickness values as low as 9 nm, thus limiting the discharge capacity. A reduction of the electrolyte thickness is limited by the anisotropy of the oxidation rate of the polysilicon granular surface leading to creation of shorting paths in the electrolyte. Successful transport of lithium ions across the oxide is evidenced by the successful charging and discharging of the battery and by Li-Si precipitates appearing on the surface of the polysilicon layer.

This work described in this chapter demonstrates that a lithium-free electrically-insulating electrolyte is possible if the electrolyte layer is extremely thin and uniform. Further optimization of the microelectronics-compatible developed process, in particular improvement of interfacial quality, is described in Chapter 6.

6 Microelectronically Fabricated $LiCoO_2/SiO_2$/polysilicon Power Cells Planarized by Chemical Mechanical Polishing

6.1 Introduction

The second stage of the project focused on optimizing the fabrication process for the $LiCoO_2/SiO_2$/polysilicon cells and in particular addressing interfacial quality issues. The interfaces between the electrolyte and the electrodes in a battery are where the charge transfer reactions take place. The heterogeneous nature of the interfaces between the ion source (anode), the ionic conductor (electrolyte), and the working electrode (cathode), forms a potential barrier which limits the cell's capacity[5]. Furthermore, the interface quality affects the kinetics of the reactions, properties of sequentially grown films, and the chemical stability between the electrolyte and electrode materials. Smooth surfaces with continuous contact between the layers are therefore essential for optimum performance. In common solid-state batteries, the roughness of the electrodes' surfaces forces a minimal thickness limit on the electrolyte to prevent contact between the electrodes that would lead to shorting. Common solid-state electrolytes are, therefore, typically 1-2μm thick[18,20,51,70,101,106]. It is desirable to thin the electrolyte in a cell as the resistance will lower and the charging time will then decrease.

This chapter describes the continuation of the $LiCoO_2/SiO_2$/polysilicon cells study. The cells were manufactured using established microelectronics technologies and methods. Chemical mechanical polishing (CMP) is a well-known planarization method in silicon integrated circuit (IC) technology. The method was described in detail in Section 4.2.2. In the work described in this chapter, CMP was used as a planarization method of the polysilicon anode prior to the electrolyte layer formation from a thin amorphous silicon layer (α-Si). While CMP has been mentioned in some works as a method to smooth polysilicon layers for the fabrication of thin-film transistors (TFTs)[127,128], it has not yet been applied to the fabrication of batteries. Cells consisting of a SiO_2 electrolyte

with a thickness value in the range of 7-40 nm were studied. The effect of the additional CMP step on the structure quality and performance of the cells was evaluated. The study presented here shows that the application of CMP to thin-film battery fabrication is highly advantageous. The data presented in this chapter reinforce the great importance of controlling interfacial quality in an all-solid-state battery, in particular for batteries utilizing thin electrolyte layers.

6.2 Polysilicon Surface Roughness Reduction

The removal rate of polysilicon by CMP using NaOH slurry was found to be approximately ~0.86 nm/sec. This rate is highly subjected to change depending on the down force acting on the wafer and polishing speed. The roughness of the doped polysilicon films, as deposited and after polishing and removal of 30 nm was measured by AFM. The 1×1 μm RMS roughness values obtained were 8.06 nm for the as-deposited polysilicon film and 0.53 nm for the CMP polished layer. The necessity of CMP is illustrated by the fact that the pre-CMP RMS roughness value is on the order of the thickness of the electrolyte layer. CMP is therefore required to ensure that shorting between the anode and cathode does not occur. Figure 6-1 shows AFM images comparing the two polysilicon films.

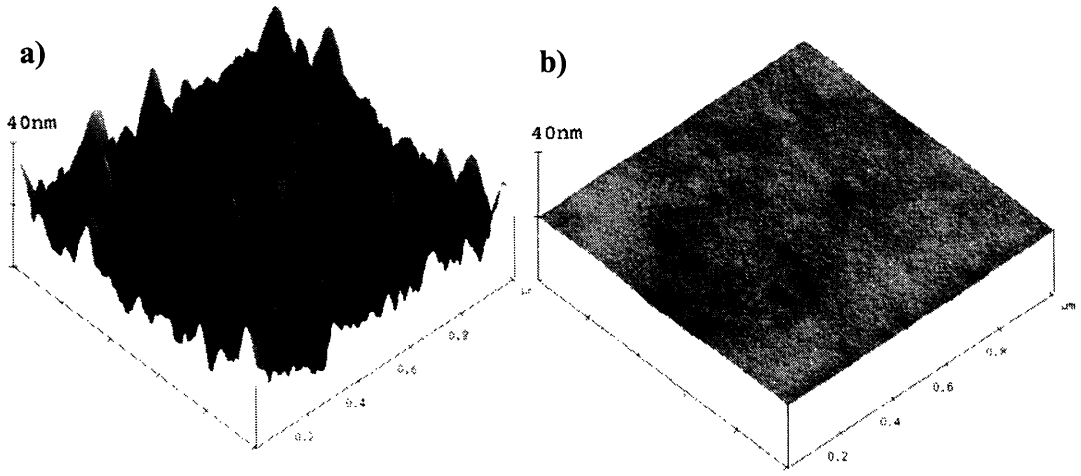


Figure 6-1: AFM images of the n^+ polysilicon layer: a) as deposited and b) after CMP

CMP is not merely a mechanical abrasion of slurry against the surface of the wafer but a process consisting of a complex mechanism both chemical and mechanical. Hydrogen bonds are formed between the native-oxide-covered polysilicon surface and the slurry particles' surface. This is followed by the formation of molecular bonds between the wafer and the slurry and the breaking of surface film's bonds when the slurry particles move away[122]. Planarization is achieved since only topographically higher points on the polysilicon layer come in contact with the polishing pad.

6.3 Cells Fabrication Process

The method used to fabricate the $LiCoO_2/SiO_2$/polysilicon cells for the work done in this chapter was described in detail in Chapter 4. In the second stage of the project, the doped polysilicon anode was polished by CMP, using NaOH slurry to reduce its roughness. The wafers were then cleaned (see Section 4.2.1) for removal of slurry and film particles. In order to obtain better quality of SiO_2 and to maintain better control over thickness and uniformity, the doped polysilicon layer was not directly oxidized for the electrolyte layer growth. Alternatively, a thin layer (14 nm) of α-Si layer was grown on top of the planarized doped polysilicon layer using ultra-high vacuum chemical vapor deposition (UHVCVD). Prior to α-Si deposition, the wafers were cleaned again as described in Section 4.2.1, leaving the surface oxide-free and hydrogen-terminated. The wafers were then loaded into the UHVCVD reactor and held in ultra high vacuum at 800°C for 10 minutes for desorption of hydrogen and in order to volatize any native silicon oxide that may have formed. The α-Si layer was grown at 550°C from a SiH_4 precursor. Following an additional RCA clean, the film was oxidized by wet oxidation at 700°C to create a uniform and high-quality layer of SiO_2.

In this part of the work the studies of SiO_2 as an electrolyte grown on planarized polysilicon and non-planarized ones were performed and compared. The thicknesses of SiO_2 in the evaluated cells were in the range of 7-40 nm. Cells of four different sizes of active areas were studied: 5×5 mm^2, 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2 with

corresponding polysilicon anode areas of: 9×9 mm^2, 3.6×3.6 mm^2, 1.8×1.8 mm^2, and 0.9×0.9 mm^2. Figure 6-2 shows a XTEM image of two $LiCoO_2/SiO_2$/polysilicon cells, with 9 nm thick SiO_2 layer, fabricated with and without a CMP planarization step.

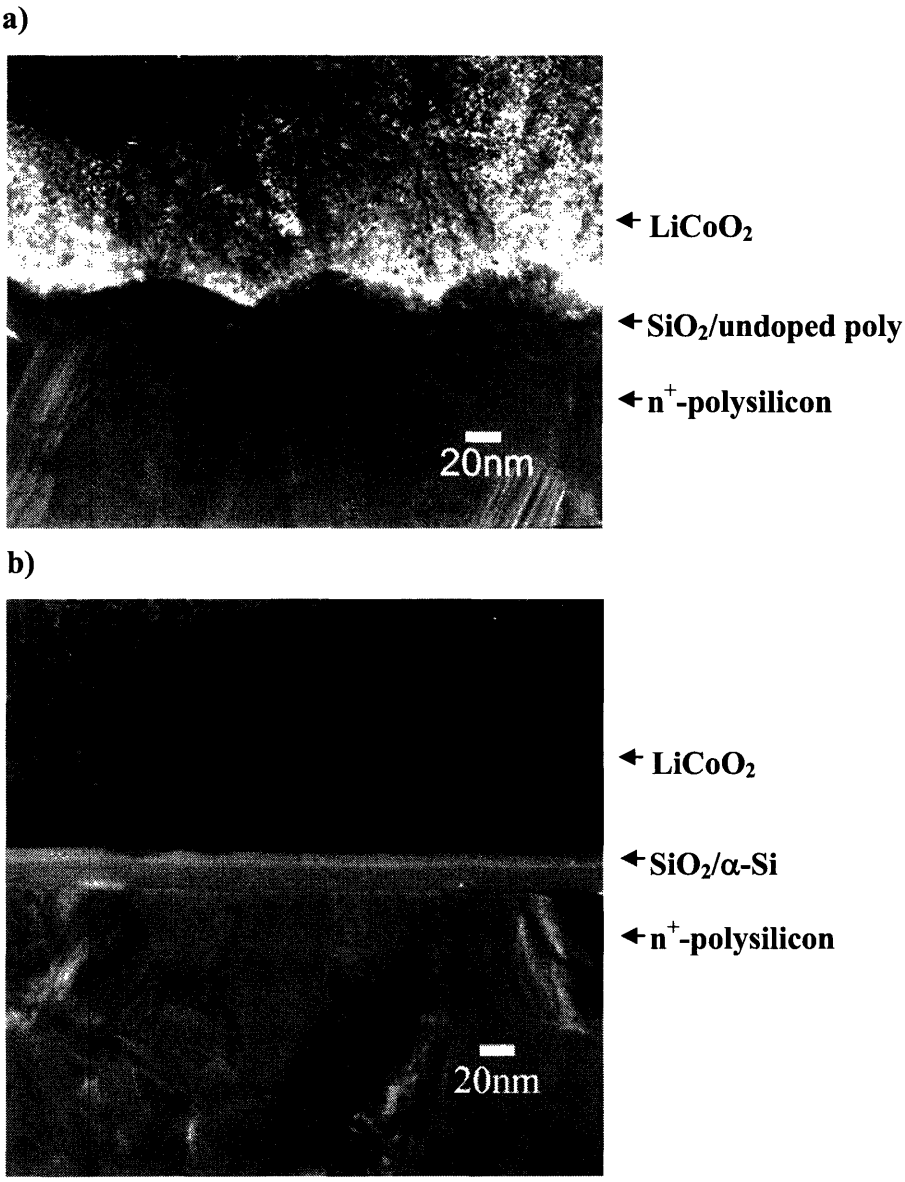


Figure 6-2: XTEM images of 9 nm thick SiO_2 cells: a) consisting of a polysilicon anode which was not planarized by CMP, and b) consisting of a ploysilicon anode which was planarized by CMP

The structure shown in Figure 6-2, part b, appears to consist of intact layers with high quality smooth interfaces.

6.4 Charge and Discharge Characterization of Planarized cells

6.4.1 Charge Rate Effect

The cells were fabricated in their discharged state, in which lithium is intercalated in the CoO_2 host lattice. In order to study the charge and discharge behavior of the fabricated cells, a constant current was forced by a parameter analyzer while monitoring the voltage between the electrodes. Cell charging was achieved by applying a positive current flow from the parameter analyzer into the cells, and within the cell from the $LiCoO_2$ into the polysilicon. Discharge was achieved by forcing a negative current to flow in the reverse direction, i.e. from the cell into the parameter analyzer. Displayed in Figure 6-3 is the charge and discharge plot measured at different rates for a 9 nm thick SiO_2 grown on top of a CMP planarized polysilicon with a 2 mm active area size.

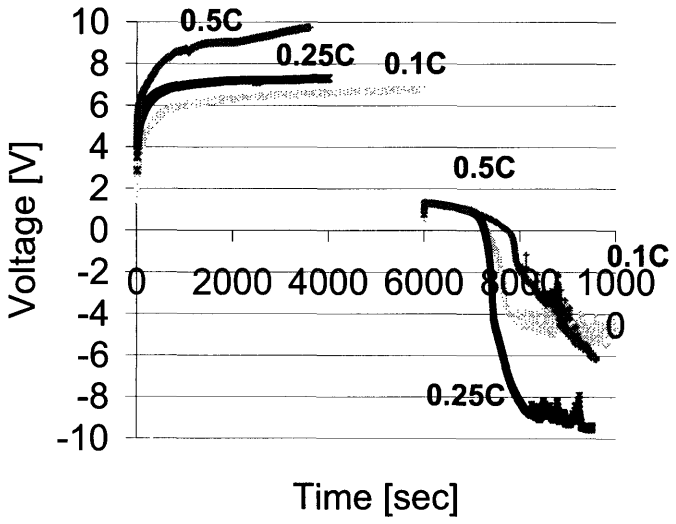


Figure 6-3: Charge and Discharge behavior at different current densities of 2 mm edge cells with 9 nm thick SiO_2

The electrical tests were performed at current densities corresponding to charge and discharge in 10, 4, and 2 hours, i.e. 0.1C, 0.25C, and 0.5C rate, respectively. The left part of the plot is the charging step. The open circuit voltage (OCV) between silicon and lithium in their elemental state is known to be ~1 V[38,92] and it depends on the silicon morphology as reported by Gao *et al.*[28]. The OCV between Li_xCoO_2 and lithium was measured to be in the range of ~3.5-4.7 V[10,11,14,58,70-72,74,76,77,124] depending on lithium concentration in the film and its morphology. Based upon these reported values, the expected equilibrium voltage between the electrodes in this cell is ~2.5-3 V. Upon charging, lithium ions are being de-intercalated from the $LiCoO_2$ and are transferred to the polysilicon electrode where they become neutral and react with silicon atoms. To compensate for the lithium ions absence in the cathode, cobalt changes its oxidation state from Co^{+3} to Co^{+4}. During charge, the potential difference between the electrodes is increasing as can be seen in Figure 6-3. The voltage measured was higher than the expected equilibrium value due to the high series resistance, R_s, of the cells as well as other reaction and kinetic impedances. As expected, the measured voltage in charge was higher for higher charge rates due to a larger IR_s.

The experimental OCV obtained from the cells in discharge was approximately 1.3 V, decreasing as the discharge advanced. Upon discharge, lithium-silicon compounds in the anode decompose and lithium ions are transferred back through the SiO_2 where they are re-intercalated between the CoO_2 layers and Co^{+4} is reduced back to Co^{+3}. The IR_s drop in the discharge part of the plot, which is the right side ($t > 6000$ sec), is negative since the current forced by the parameter analyzer is negative. When the potential difference, V_{OCV}, becomes less than IR_s in their absolute values, the polarity of the voltage will be reversed. The voltage polarity change in discharge for the three rates can be seen in Figure 6-3 after 1264, 1348, and 1764 seconds from the discharge starting point. Note that the discharge measurement followed the charge measurement with no delays; however, in order to compare different testing rates, the discharge curves are all plotted starting at 6000 seconds. At the first part of the discharge plot, the voltage measured is almost identical for the different rates. The series resistance is not dominant in determining the measured voltage at early stages of discharge due to an available continuous supply of lithium ions from the anode. As the discharge process progresses,

however, it becomes harder to draw the specified current and larger negative voltage values are subsequently required by the parameter analyzer. From the slopes of the different rate plots in discharge, it is safe to assume that if one measures the discharge voltages for a longer period of time, the values that will be obtained will correspond to the current densities, and IR_s drops will be the most dominant factor.

6.4.2 Electrolyte Thickness

Shown in Figure 6-4 are charge and discharge plots, measured at a rate of 0.25C, of 5 mm edge cells with SiO_2 thicknesses of 7 nm, 9 nm, and 26 nm, grown on a polysilicon anode polished by CMP. The left side of the plot is the voltage measured with time of charge and the right side (t > 4000 sec) of the plot is the voltage measured with time of discharge.

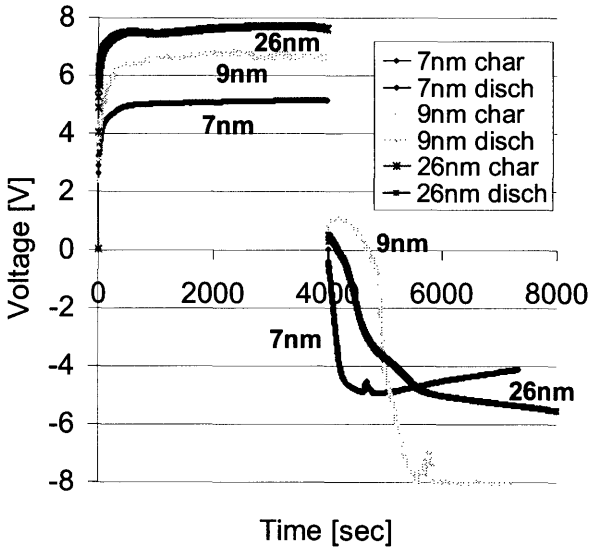


Figure 6-4: Charge and discharge at 0.25C rate, of 5mm edge cells with different electrolyte thicknesses

In charge, the voltage is increasing with time as expected when lithium ions are transferred from the cathode to the anode. The voltage values measured here, again, are higher than the expected potential difference due to the high series resistance of the cell. SiO_2 is a highly insulating material with a bulk resistivity of $\rho \sim 10^{15}$ Ωcm[104] and therefore

its contribution to the cell resistance R_{oxide} is high. However the resistance is minimized by the ultra-thin thickness while the cell consists of a truly insulating electrolyte. The electrolyte contribution to the cell's resistance can be described by:

$$R_{oxide} = \rho \frac{t}{A} \qquad \textbf{Equation 6-1}$$

Where ρ is the film resistivity, t is the film thickness and A is the area through which current flows which, in this geometry, is equal to the active area of the cell. The oxide resistance R_{oxide} increases with t, the oxide thickness, as can be seen in the charge process in the left side of Figure 6-4.

In the case of discharge, the contribution of the cell resistance is not straight forward. The overall cell voltage depends on the availability of lithium ions, as well as the properties of the cell layers after charge. Of those studied here, the cell containing the 9 nm thick SiO_2 electrolyte layer exhibited the best performance, exhibiting positive voltage while drawing current out of the device for 710 seconds. This is a shorter period of time compared to the 2mm edge cell with the same electrolyte thickness. This discrepancy can be explained by its larger area and therefore higher probability of oxide defects resulting in shorting paths. The cell with the thicker electrolyte layer, 26 nm, gave charge back for only 170 seconds. This is believed to be due to higher a series resistance that increased the negative IR_s drop thereby causing the polarity change point to occur at an earlier stage. The voltage measured for the thinner oxide-containing cell turned negative after four seconds of discharge. During discharge, the ultra-thin SiO_2 layer is subjected to high electric fields. The dielectric breakdown strength of high quality SiO_2, such as that used for CMOS gate oxides, is ~10^7 V/cm[104]. The breakdown voltage of a 7 nm thick layer of SiO_2 with that quality is therefore approximately 7 V. Although the charge portion of the plot does not indicate an oxide breakdown, it is reasonable to believe that the level of insulation and high quality of the oxide are being compromised by the relatively high voltages that are being applied in the process of electrical testing. This hypothesis is supported by the relatively low negative voltage required to continue

supplying the discharge current at longer discharge times and by its decreasing trend in its absolute value.

The voltage measured at the start of the charge process (after four seconds), displayed in Figure 6-4, was plotted against the electrolyte thickness of different cells and was linear as expected. The voltage versus electrolyte thickness with an added linear trend-line can be seen in Figure 6-5.

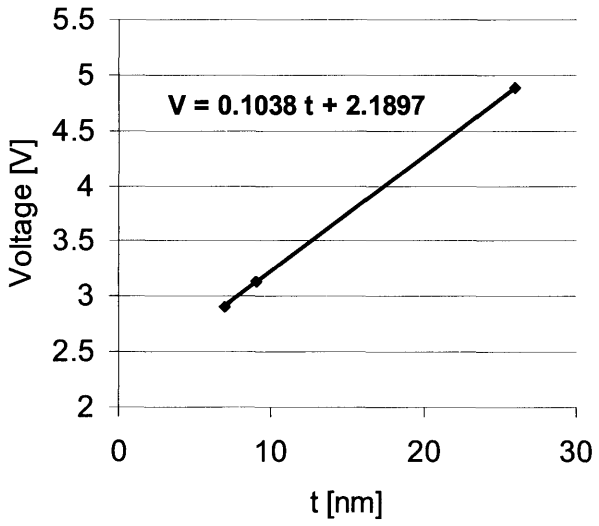


Figure 6-5: The initial charge voltage of cells with different SiO_2 thickness

Extrapolating the trend line of the three thicknesses to a theoretical zero thickness will give the expected equilibrium OCV of the $LiCoO_2/SiO_2$/polysilicon cell. At t = 0, no series resistance voltage drops need to be accounted for. That value, as can be seen from the trend line equation in Figure 6-5, is approximately 2.19 V. This OCV value is consistent with the estimated value based on those reported in the literatures for $LiCoO_2$ and silicon versus elemental lithium. From Figure 6-5, (dividing by the current used for the measurement) the series resistance can be estimated to be 1.66×10^5 Ω/nm of electrolyte thickness.

6.5 Planarization Effect on Cell's Discharge Capability

In order to study the planarization effect on cell performance, cells fabricated with a CMP step were compared with cells containing a SiO_2 layer with the same thickness grown on top of a non-planarized polysilicon. Two examples of such a comparison of cells with 9 nm thick SiO_2 layer can be seen in Figure 6-6 and in Figure 6-7. Figure 6-6 shows the charge and discharge plot of cells (planarized and non-planarized) with a 2×2 mm^2 active area size tested at a 0.25 C rate, while Figure 6-7 shows similar plots for cells with active area size of 1×1 mm^2 tested at a 0.5 C rate.

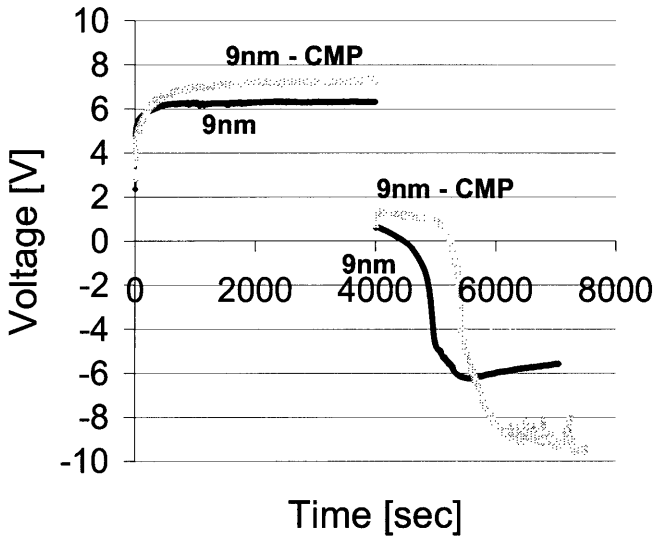


Figure 6-6: 2 mm cells with planarized and non-planarized polysilicon with 9 nm thick SiO_2 tested at 0.25C rate

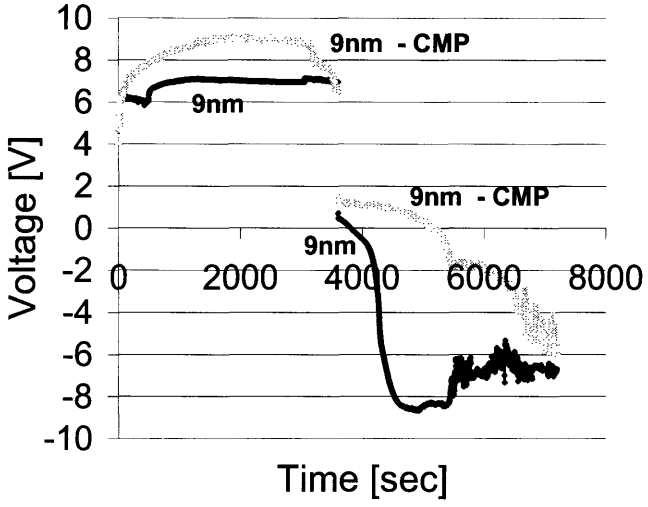


Figure 6-7: 1 mm edge cells with planarized and non-planarized polysilicon with 9 nm thick SiO_2 tested at 0.5C rate

During the charging stage, the voltage measured for the cells fabricated with a CMP step was higher than the voltage measured for the non-planarized ones. However, during the discharge stage the voltage obtained from the planarized cells was higher than the one obtained from the non-planarized ones. Moreover, the positive portion of the discharge measured voltage, which is the power obtained from the cell, is much longer than the one obtained for the cells fabricated without the CMP step.

One might expect that the IR_s drop on two cells with the same area and same thickness would be the same. However, this is not the case when the oxide thickness is not uniform leading to local variations in the thickness of the oxide. These variations become increasingly problematic as the thickness of the electrolyte layer decreases to extremely thin films, such as those used in this study. Using the Deal and Grove model, the silicon oxidation process can be described in three steps: transport of oxidizing species in the gas phase at a flux F_1, diffusion of the oxidizing species through the oxide to the Si/SiO_2 interface at a flux F_2, and reaction at the interface at a flux F_3[113]. At a steady state: $F_1 = F_2 = F_3$. Silicon oxidation is a surface reaction limited process. The flux of the limiting stage, that is the oxidation reaction at the Si/SiO_2 interface, is given by:

$$F_3 = k_s C_i$$ **Equation 6-2**

Where C_i is the oxidizing species concentration in the oxide close to the interface and k_s is the surface reaction rate, which is related to the interface reaction kinetics and depends on the rate of incorporation of silicon atoms in the growing oxide layer[113]. This rate is orientation-dependent since it depends on the atomic surface concentration of silicon which is a function of its orientation. Polysilicon grown at 625°C usually consists of a columnar granular structure with a {110} preferred orientation, with contributions from {111} and {113} orientations as well[122]. The polycrystalline silicon layer will, therefore, have an anisotropic oxidation rate depending on the orientation of each specific grain. This effect is enhanced by the different oxidation rates at high-angle grain boundaries compared to the oxidation rates at the grains themselves[122]. The ultra-thin SiO_2 films employed in these cells are highly sensitive to any thickness distribution. When the local thickness of SiO_2 in some areas is lower than 9 nm and in some areas higher, the charge carriers will choose the shortest path, i.e. the path of least resistance. Those shallow thickness areas appear in high frequency along the SiO_2 layer; therefore these thinner areas constitute preferable paths for charge carrier to cross the oxide and the actual IR_s drop due to SiO_2 would be slightly smaller. In discharge, the portion of the positive voltage is longer for the cells consisting of a uniform SiO_2 layer since they can withstand higher electric fields without compromising oxide quality. Sternheim *et al.* observed lower breakdown strength and higher leakage current for SiO_2 grown on a polysilicon layer, compared to oxide grown from single crystal silicon, due to interface roughness.[129]

In order to confirm this explanation, a SiO_2 thickness distribution was performed on HRXTEM images. The layer's thickness was measured in 45 points spaced evenly over the image. The analysis was performed for non-planarized cells with oxide thicknesses of 7 nm, 9 nm, and 40 nm and for planarized cells with oxide thicknesses of 7 nm, 9 nm, and 26 nm. The measured thickness values were plotted in the form of histograms shown in Figure 6-8. Part a of Figure 6-8 shows the histograms plotted for the thickness values of the SiO_2 grown on the non-planarized polysilicon anode and part b

shows the histograms plotted for the thickness values of the film grown from the planarized polysilicon.

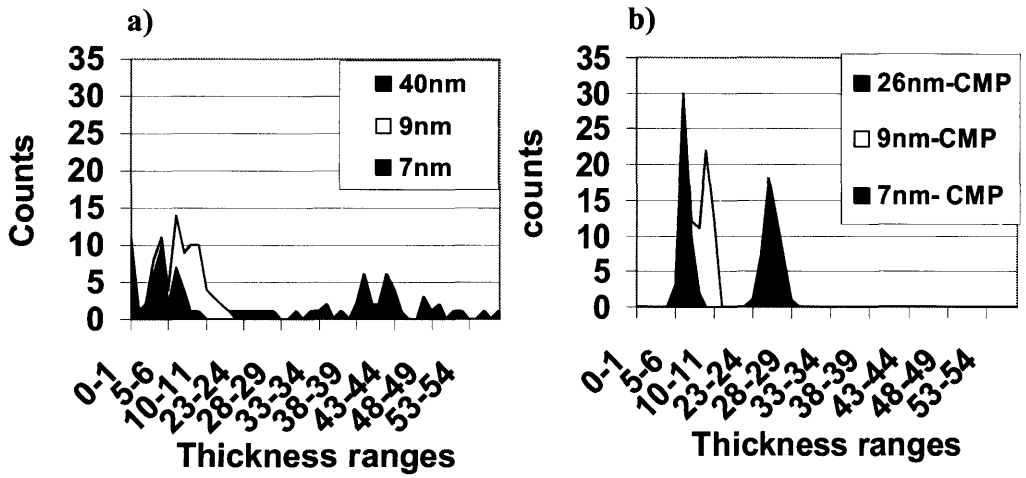


Figure 6-8: SiO_2 thickness distribution measured by HRTEM of: a) non-planarized cells and b) planarized cells

The large thickness distributions displayed by the histograms for the cells fabricated without a CMP step as compared to the smaller and sharper distributions displayed for the planarized ones support the mechanism suggested above. The oxide film grown on the polysilicon that was not polished by CMP consists of locally thinner regions that enable faster transfer of charge carriers and lower the contribution to the series resistance. At the same time, they degrade the performance of the electrolyte layer by lowering the breakdown voltage of the oxide. The thickness distribution in the SiO_2 can be treated as a set of resistors connected in parallel. The resistance of each 'resistor' can be calculated using Equation 6-1 and the effective resistance is the reciprocal of the sum of the resistance reciprocals. Based on the data shown in Figure 6-8, the effective resistance values were estimated to be: 1.7×10^7 Ω and 2×10^7 Ω for the cells grown without CMP and with CMP, respectively. This difference in the effective resistance supports the explanation suggested for the difference in voltage measured during charge. Similarly, the effective breakdown voltage will correspond with the thinner areas of the oxide and will be lower for the cells grown without a CMP planarization step.

As demonstrated in Figure 6-6 and in Figure 6-7, the positive voltage component of the discharge was longer for the planarized samples compared to the non-planarized ones. The charge transferred during charge and discharge was calculated by multiplying the current used to charge and discharge the cells by the time of charge and by the time of the initial positive voltage discharge. The results for the cells with 9 nm thick oxide of different sizes of active areas, tested at 0.25C rate, are given in Table 6-1:

Cell edge size [mm]	CMP / no CMP	Charge in Charging [Cb]	Charge in Discharging [Cb]	Percentage of charge back
5	No CMP	2.5E-03	3.6E-04	14.52
5	**CMP**	**2.5E-03**	**4.4E-04**	**17.76**
2	No CMP	4.0E-04	4.7E-05	11.65
2	**CMP**	**4.0E-04**	**1.3E-04**	**31.50**
1	No CMP	1.0E-04	4.2E-06	4.20
1	**CMP**	**1.0E-04**	**4.0E-05**	**40.00**
0.5	No CMP	2.3E-05	1.3E-08	0.06
0.5	**CMP**	**2.3E-05**	**5.7E-06**	**25.24**

Table 6-1: The amount of charge transferred in charging and discharging different sizes of cells fabricated with a CMP step compared with ones fabricated with no CMP step

The values given in Table 6-1 for the planarized cells indicate better performance than the performance of the cells deposited with no planarization step - a higher level of charge is being retrieved from the cells made with a CMP step. The plots presented in Figure 6-6 and in Figure 6-7, as well as the data displayed in Table 6-1, demonstrate the great impact of the improved interfacial properties achieved by introducing CMP into the cell fabrication process.

In order to rule out the possibility of the origin of charge simply existing within the structure as electrons stored in a regular capacitor with SiO_2 as the dielectric medium, the theoretical capacitance, C, of the SiO_2 layer was calculated from Equation 6-3:

$$C = \frac{A\varepsilon_0\varepsilon}{d} \qquad \textbf{Equation 6-3}$$

Where A is the active area of the cell, $\varepsilon = 4$ is the relative dielectric constant of SiO_2, $d =$ 9 nm is the measured oxide thickness, and $\varepsilon_0 = 8.85\times10^{-14}$ F/cm is the permittivity of vacuum. Calculated capacitance values using Equation 6-3 are presented in Table 6-2 with the estimated electrochemical capacitance obtained from the cells prepared with a

CMP step. The latter was estimated by dividing the charge obtained in discharge from Table 6-1 by 1 V which is the estimated average voltage obtained from the planarized cells.

Cell active area size [mm^2]	Calculated SiO_2 capacitance [F]	Measured electrochemical capacitance [F]
25	9.83E-08	4.4E-04
4	1.57E-08	1.3E-04
1	3.93E-09	4.0E-05
0.25	9.83E-10	5.7E-06

Table 6-2: Theoretical capacitance values of a capacitor with 9 nm SiO_2 with plate area corresponding to cells' active area size

Note that the electrochemical capacitance obtained from the discharge of the cells is four orders of magnitude higher than the theoretical electronic capacitance. This is an indication of the electrochemical nature of the cell and the participation of lithium ions as charge carriers in the process.

6.6 Summary and Conclusions

This chapter described the improved fabrication and characterization of integrated solid-state thin-film power cells of $LiCoO_2/SiO_2$/polysilicon. Cells consisting of an ultra-thin, lithium-free SiO_2 electrolyte with a thickness range of 7 nm – 40 nm with active area sizes of 5×5 mm^2, 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2 were created by using conventional microelectronics processing and expertise. The work described in this chapter demonstrates the implementation of a planarization step, using CMP, a well known planarization method in microelectronics, in the fabrication of the integrated $LiCoO_2/SiO_2$/polysilicon solid-state thin-film lithium ion battery. Polishing the polysilicon anode layer reduced its RMS roughness from 8.06 nm to 0.53 nm, thereby leading to smoother interfaces and to a subsequently higher quality SiO_2 electrolyte layer.

The OCV of the cells was estimated from comparing initial voltage values obtained from charging cells with different thickness of electrolyte and was found to be ~2.19 V. The cells exhibited improved performance when prepared with the CMP planarization step, and up to 40% of the charge was retrieved from the cells compared to a maximum of 14.52% retrieved from the non-planarized cells. To the author's knowledge, this is the first time CMP is applied to fabricating an electrochemical device. The results presented here reinforce the importance of interfaces in moving to the next generation of integrated power on a chip.

7 Integrated Rocking-Chair Battery with an Ultra-thin LiPON Electrolyte

7.1 Introduction

This chapter describes the application of microelectronic and thin-film technology to a more conventional battery material system. Lithium ion solid-state thin-film batteries typically consist of a 1-2 μm thick electrolyte[47,51,63,70,101,105,106] and electrolytes as thick as 1 mm have been reported as well.[54] Often, the quality of the interfaces between the electrodes and the electrolyte, and their roughness in particular, dictate a thickness limitation on the electrolyte so that a short between the electrodes is prevented. Reducing electrode surface roughness will improve the contact and adhesion to the electrolyte and will allow reduction of its thickness. Ionic conductivities of solid electrolytes are typically three to four orders of magnitude lower compared to those of liquid electrolytes (see Section 2.3.3) result, the electrolyte is responsible for a major part of cells impedance. By significantly reducing the electrolyte thickness, its contribution to the battery's series resistance can be decreased and charging at faster rates can be enabled. In this chapter the fabrication of a rocking-chair battery is described. The cells consist of $LiCoO_2$ and V_2O_5 electrodes and a lithium phosphorus oxynitride (LiPON) electrolyte. By employing thin-film technology to achieve greater interfacial quality, the electrolyte thickness was reduced down to approximately 100 nm. A surface morphology study of V_2O_5, the rougher of the two electrode materials, deposited at different conditions, was performed in order to obtain optimal conditions for a smooth film deposition. The V_2O_5/LiPON/$LiCoO_2$ cells were fabricated using microelectronics compatible processing and were electrically tested using a probe station and measurement equipment typically used in characterizing microelectronic devices. To the author's knowledge this is the first solid-state thin-film battery with an overall thickness, including electrodes and electrolytes, as thin as approximately 0.55 μm.

7.2 V_2O_5 Surface Morphology Study

V_2O_5 is a common lithium-ion electrode material. Detailed background and literature survey on V_2O_5 was given in Section 3.2.2. An amorphous layer or short-range order polycrystalline film is often used[63,64,106] and was reported to exhibit better electrochemical performance than crystalline films[7,130]. Kumagai *et al.* reported the appearance of a crystalline phase in heat-treated V_2O_5 films at temperatures above 200°C[8]. The purpose of the surface study was to achieve smooth films by tailoring deposition parameters and surface morphology and roughness. In addition to their reported better performance compared to crystalline films, amorphous or short-range order V_2O_5 films are expected to be flatter. Therefore, in order to obtain amorphous or short-range order V_2O_5 films, the surface morphology study was completed at a low temperature range. Figure 7-1 shows AFM surface images of 200 nm thick V_2O_5 films on silicon substrates deposited at different conditions. The height scale of the surface plots in parts a-e and g-h is 70 nm. In parts (f) and (i) the scale is 200 nm. The 1 μm × 1μm RMS roughness measured for the films deposited in different conditions is given next to the corresponding images. The surface morphology obtained for films deposited at room temperature appears uniform and consist of granular nature. As the substrate temperature increases, the films' surface becomes less uniform and islands are formed and are apparently growing favorably in one dimension.

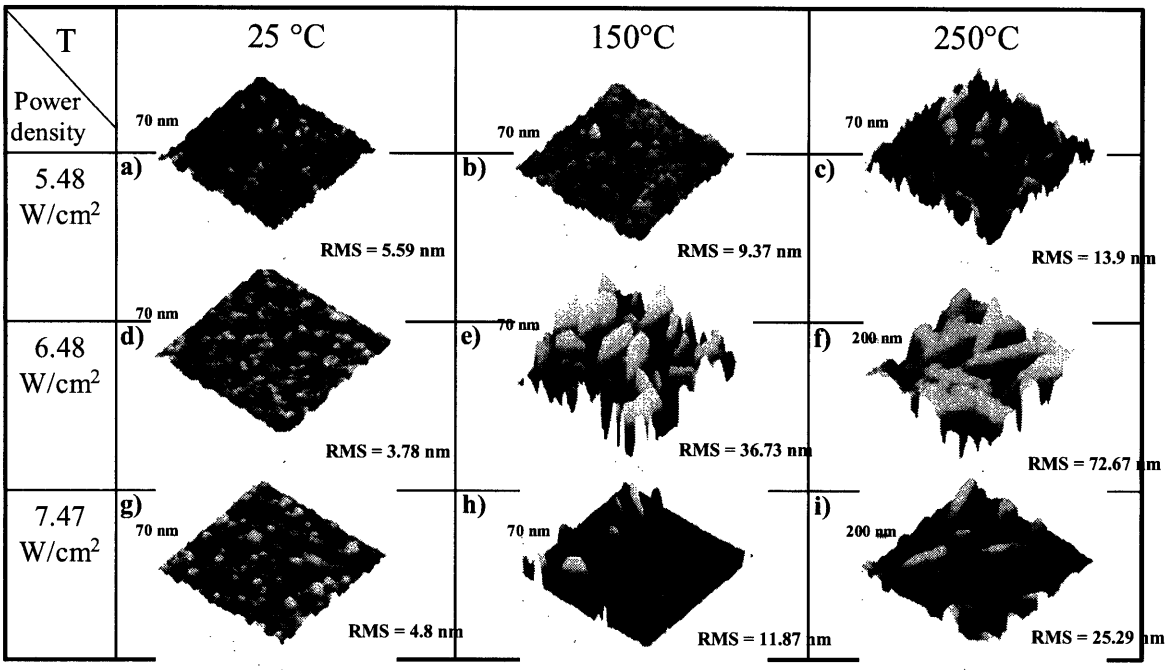
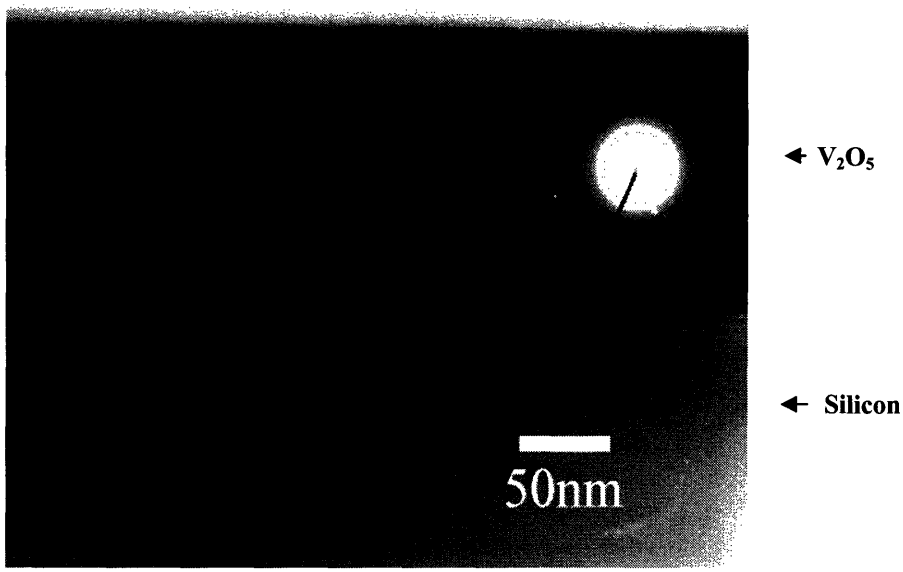


Figure 7-1: AFM surface images of 200 nm thick V_2O_5 films deposited at varying temperatures and gun power density values.

Figure 7-2 shows XTEM images of V_2O_5 film deposited at room temperature and a gun power density of 5.48 W/cm^2 (part a) and a V_2O_5 film deposited at 250°C and a gun power density of 6.48 W/cm^2 (part b). Note that the thickness of the film was calibrated at room temperature by XTEM for different power density values under the assumption that the overall film thickness does not change with substrate temperature. An electron diffraction image was taken from the film deposited at ambient conditions and is given in the inset of Figure 7-2, part a. The electron diffraction image taken from the film indicates short-range order in the microstructure.

a)



b)

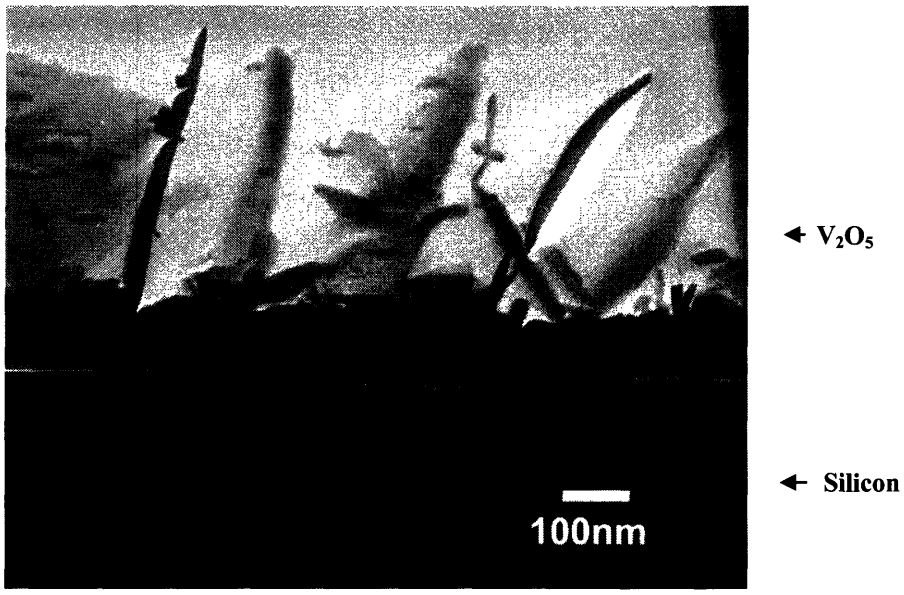


Figure 7-2: XTEM images of V_2O_5 200 nm thick films deposited on silicon at: a) room temperature and gun power density of 5.48 W/cm^2, and b) 250°C and 7.47 W/cm^2.

The thin film growth mechanism via sputtering deposition consists of adsorption of the sputtered species on the substrate surface, nucleation of the new phase, and growth of stable nuclei. The adsorbed atoms which are not resputtered from the substrate diffuse on the surface and form clusters. Once a critical size cluster is reached, a nucleus of the

new phase is formed. The critical nucleus size is determined by energetic considerations, i.e. when the energy released by the adsorption and coalescence process is larger than the surface energy required in creating the new nucleus. The fraction of the stable nuclei is given by:[122]

$$\frac{n_c}{n_0} = \exp\left(-\frac{\Delta G_{fc}}{kT}\right) \qquad \textbf{Equation 7-1}$$

Where n_c is the number of stable nuclei out of the total number of nuclei, n_0, ΔG_{fc} is the critical formation free-energy change for a stable nucleus, k is Boltzmann's constant, and T is the absolute temperature of the substrate. Equation 7-1 suggests that the substrate temperature is a key parameter in determining the final number of nuclei of the deposited film. The number of nuclei translates directly to the grain density and therefore greatly affects film's morphology as can be seen in Figure 7-1. The films deposited at 150°C and 250°C are polycrystalline in nature with columnar grain morphology. This implies that grain growth is happening mainly in one direction. As the temperature increases the number of stable nuclei formed is lower and the grain size is larger. The film's surface roughness increases with deposition temperature due to the bigger grain size formed at increasing temperature. The smoothest film was achieved at room temperature for gun power density of 6.48 W/cm^2. Depositions of V_2O_5 using reactive DC sputtering, from a vanadium target in oxygen background, were reported to produce higher quality films at room temperature as well[63,67], and Jeon *et al.* reported an RMS roughness of 2.68 nm[67].

The shape of the microstructure of the film deposited at 250°C, shown in Figure 7-2 part b, appears to have a dendritic nature to it. Dendritic morphology is typically observed in crystallization of an under-cooled melt, where a negative temperature gradient is formed at the solidification front[131]. In thin-film deposition, typically three dimensional growth of clusters is preferred thermodynamically, however, kinetic considerations may limit the growth and lead to dendrites formation[132]. Examples for those kinetic limitations on three dimensional growths can be faster diffusion on the particles compared to the substrate or a diffusion barrier at the aggregates edges or facets.

The adsorbed atom performs a random walk on the substrate but will be captured by the growing particle with very limited diffusion on the particle edges[132]. Crystalline V_2O_5 consists of an orthorhombic layered structure in which each vanadium atom is positioned in the center of a deformed pyramid of five oxygen atoms and is connected to a sixth one forming an octahedron[120]. See Section 3.2.2 for detailed background on V_2O_5 and Figure 3-6 for illustration of the structure. The octahedrons are connected between them forming layers along the a-b crystallographic plane of the film. Kumagai *et al.* observed preferred orientation of (110) for V_2O_5 films annealed at 200°C in which the a-b plane of the film grew perpendicular to the substrate[8]. It is, therefore, reasonable to believe that the dendrite-like shape of the V_2O_5 films deposited at 250°C originated from preferential growth and faster diffusion along the a-b plane of the film, forming the layered microstructure perpendicular to the silicon substrate.

7.3 V_2O_5/LiPON/$LiCoO_2$ Cells

7.3.1 Cell Fabrication

The V_2O_5/LiPON/$LiCoO_2$ cells were fabricated on silicon substrates, using microelectronics technology processing. The fabrication method was described in detail is Chapter 4 and may be utilized to incorporate the cell manufacturing as part of the back end process, possibly on the back of the silicon chip. A (100) silicon wafer was cleaned prior to the cells deposition. A metallization tri-layer consisting of 100 nm thick titanium layer, a 500 nm platinum layer, and an additional titanium layer of 30 nm, was then evaporated on the silicon wafer using e-beam evaporation. The thin titanium layers below and on top of the platinum contact layer were intended to enhance the adhesion to the silicon substrate below and to $LiCoO_2$ on top of the platinum contact layer. The choice of platinum as a current collector was made for facilitating the selective wet etching step in the fabrication process. However, the cells can be fabricated with a number of other metal contact layers, compatible with lithium ion batteries as well as microelectronic technology. A 250 nm thick $LiCoO_2$ layer was deposited on top of the 30 nm upper titanium adhesion layer employing RF sputtering from a commercially purchased $LiCoO_2$

target in an argon environment. LiPON was subsequently sputtered from a Li_3PO_4 target in a nitrogen environment. In this work cells consisting of electrolyte thicknesses of 350 nm and 100 nm were evaluated. The LiPON electrolyte ionic conductivity was measured to be 1.4×10^{-8} S/cm with nitrogen content of 1 at% (see Section 4.3 for study of LiPON deposition conditions and corresponding measured ionic conductivity values). Reported ionic conductivity values of LiPON were as high as 4×10^{-7}-2×10^{-6} S/cm, depending on the nitrogen content in the film[19,20,67,101,103,106]. The LiPON used in this work exhibits higher resistivity than these reported values, however, by decreasing its thickness, this difference in ionic conductivity is marginalized and a satisfying conductance level is achieved. The potential gain shown in this chapter by the electrolyte thickness reduction can be enhanced by utilizing a higher conductivity LiPON electrolyte.

The LiPON deposition was followed by RF sputtering of a 200 nm V_2O_5 in argon ambient with 3% oxygen background. The V_2O_5 contact layer was an aluminum layer deposited by DC sputtering. The wafer was then patterned using photolithography followed by a wet chemical etching step (see Section 4.3.2) in order to define square cells consisting of three different sizes of active areas: 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2. A top view of the fabricated cells with 0.5×0.5 mm^2 can be seen in Figure 7-3. A cross section view of the cell containing a 100 nm thick electrolyte can be seen in Figure 7-4. Since some non-uniformity typically occurs during sputtering, a thickness distribution of approximately ±10% of the nominal value in the layers' thicknesses across the wafers can be expected. This distribution is likely to be larger for rougher interfaces. The top layer of the square cells seen in Figure 7-3 is the aluminum contact to the V_2O_5 electrode and the darker appearing background is the titanium 30 nm adhesion layer on top of the platinum bottom contact layer. Figure 7-4 demonstrates the uniform, intact, and relatively smooth interfaces between the electrode films and the thin electrolyte.

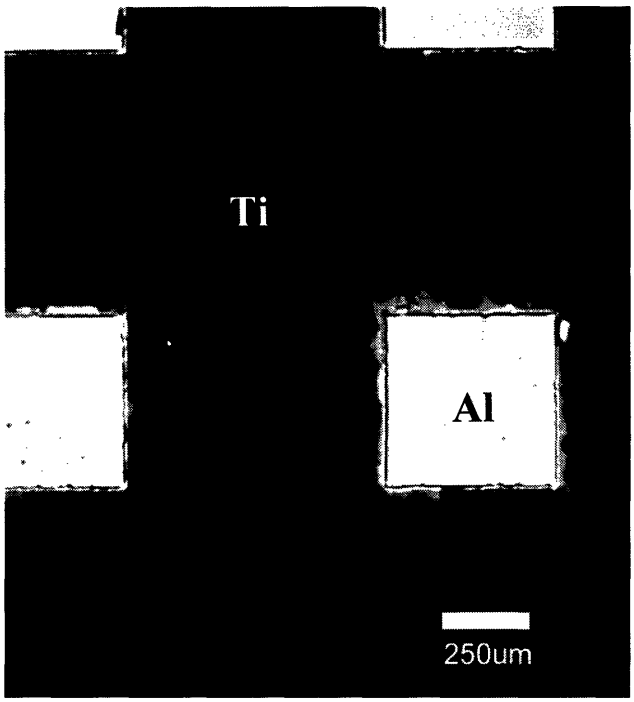


Figure 7-3: An optical microscope image showing a top view of 0.5×0.5 mm^2 cells.

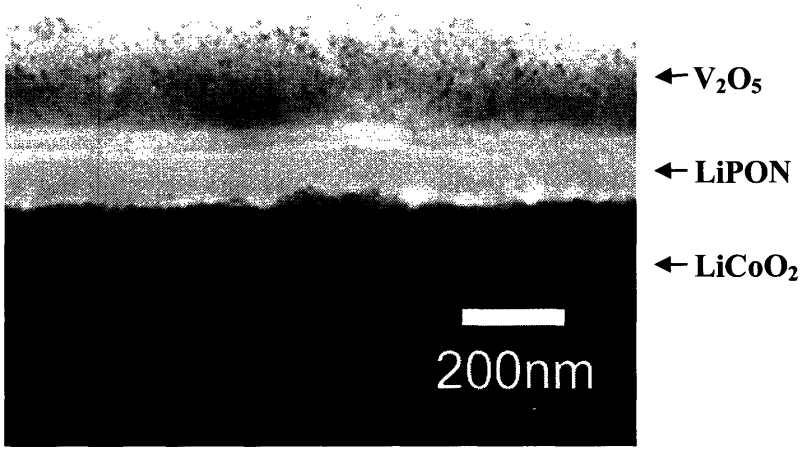


Figure 7-4: XTEM image of the V_2O_5/LiPON/$LiCoO_2$ cell consisting of a 100 nm thick LiPON electrolyte.

The microstructure of the $LiCoO_2$ was found to be polycrystalline (see Figure 4-4) and the LiPON layer amorphous (not shown), both by electron diffraction.

7.3.2 Electrochemical Characterization

The cells were fabricated in their discharged state and were charged and discharged using a parameter analyzer and a probe station typically used for microelectronic device testing (as described in Chapter 4). Since this measurement equipment utilized is not designed for long testing times, the charge and discharge times were limited and the cycling performance of the cells was not tested. Moreover, the charge and discharge was not restricted to a certain voltage range, as typically done in electrochemical testing, in order to allow better understanding of the cells behavior. V_2O_2 exhibits OCV of 3-3.7 V versus lithium[8,9,64,66] and $LiCoO_2$ was reported to have an OCV~3.6-4.7 V versus lithium depending on the deposition method and conditions[10,11,71,72,74,76,77]. Based on these values, the expected OCV for our system is 1-1.5 V which is ideal for current digital IC's. The first charge and discharge of 2×2 mm^2 cells (hereafter referred to as "2 mm cells") of cells with 100 nm thick electrolyte at different charging rates can be seen in Figure 7-5.

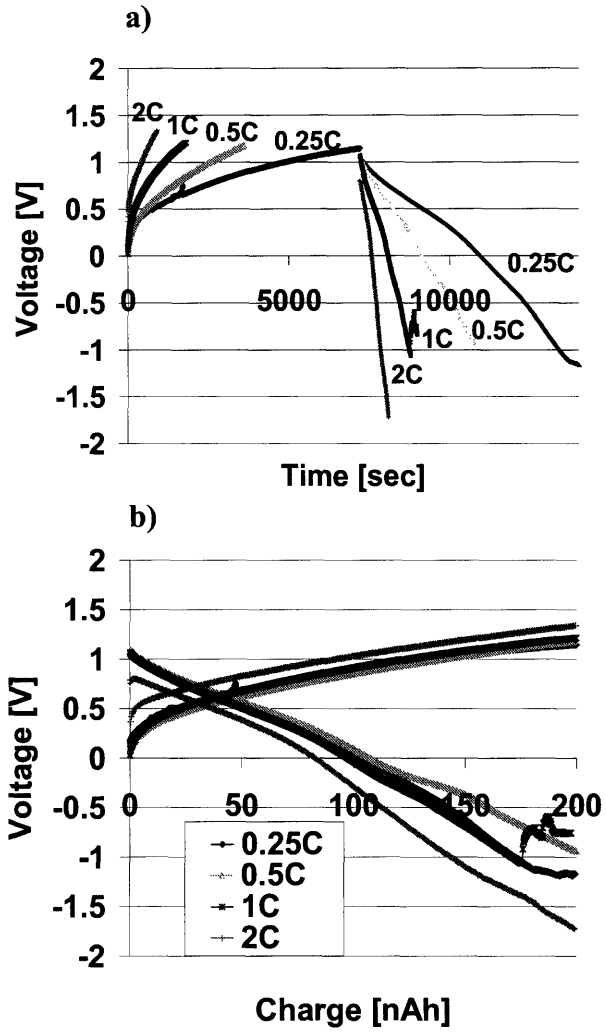


Figure 7-5: First charge and discharge of 2 mm edge cells with 100 nm LiPON: a) voltage versus time, and b) voltage versus charge.

Figure 7-5, part a shows the voltage measured versus time of charge and discharge whereas the left hand side of the plot is the charge and the right hand side of the plot is the discharge. Note that the discharge immediately followed the charge of each cell; however, for comparison of different rates, the discharge parts of different rates are plotted starting from the same point in the time axis (e.g. 7200 seconds). Figure 7-5, part b shows the voltage measured versus charge in units of nAh. The apparent OCV = 0 is an artifact caused by the parameter analyzer. Due to the small features of the cell, the amount of charge that can be attained from one cell is limited. Higher values can be obtained by either fabricating cells consisting of lager areas, or by connecting cells in

parallel using multilevel fabrication technology typically used in microelectronic device processing, or by both. The nano-cell is created in the discharged state in which lithium ions are intercalated in the $LiCoO_2$ electrode. During charge, the parameter analyzer forces a positive current to flow into the cell, from the $LiCoO_2$ electrode to the V_2O_5 one. The charge is conducted through a lithium ion chain within the LiPON. For every lithium ion that enters the LiPON layer from the $LiCoO_2$ side, another lithium ion exits the LiPON layer from the V_2O_5 side, receives an electron from the external circuit, and gets intercalated in it. $LiCoO_2$ was reported to have an open circuit voltage (OCV) versus lithium in the range of 3.6-4.7 V depending on the deposition method and conditions[10,11,71,72,74,76,77], and V_2O_5 exhibits OCV versus lithium in the 3-3.7 V range[8,9,64,66]. Based on that, a reasonable expected voltage that can be obtained from the V_2O_5/LiPON/$LiCoO_2$ cell is in the range of ~1-1.5 V as is confirmed by the plots shown in Figure 7-5. During discharge, the parameter analyzer forces a negative current to flow from the cell. As long as there is a constant supply of lithium ions from the $Li_xV_2O_5$ electrode of the charged cell, current is flowing naturally from the cell to the parameter analyzer and the voltage measured is positive. When there are insufficient charge carriers to maintain the constant negative current, as can be seen at the right hand side of the discharge part of the plot, the parameter analyzer will apply a negative electric field in order to keep the current flowing, and the polarity of the voltage measured will be reversed. The discharge voltage decreases monotonically with no plateaus, as commonly observed for amorphous transition metal oxide cathodes. The charge and discharge curves presented in Figure 7-5 have a similar shape to plots showed by Baba *et al.* for a V_2O_5/LiPON/$Li_xV_2O_5$ rocking chair battery[106]. Due to the low thickness of the electrolyte, the series resistance added by the electrolyte is minimized. This is apparent in the small voltage change between the charge ending value and the discharge starting value which is equal to twice the voltage drop (positive drop for charge and negative for discharge) originated from the cell's series resistance. The extracted voltage drop values corresponding to the plots shown in Figure 7-5 can be seen in Table 7-1. At higher rates which correspond to high current densities, the voltage drops are larger as described in Equation 7-2 which is an extension of Equation 5-1.

Charging rate	Voltage drops [mV]
0.25C	44
0.5C	40.81
1C	70.81
2C	268.09

Table 7-1: Experimental values of voltage drops extracted from Figure 7-5

$$V_{measured} = V_{OC} + V_{polarization} = V_{OC} + IR_s + \eta \qquad \textbf{Equation 7-2}$$

Where V_{OC} is the equilibrium potential difference between the electrodes, $V_{polarization}$ is the addition to the voltage originating from the cell's series resistance, R_s, and from other types of polarization, such as kinetic and reaction energetic barriers noted at η in Equation 7-2. I in Equation 7-2 is the current forced by the parameter analyzer during measurement, which is positive during charge and negative during discharge.

The electrical characterization of the cells was performed in ambient conditions in air. The observed capacity loss, 48% to 59% depending on charging rate, for the initial charge can be explained in two ways; it can be attributed to fewer available lithium sites in the cathode, possibly due to irreversible phase transitions in the film, or fewer lithium ions free to be intercalated due to irreversible oxidation reactions as a result of exposure to the environment:

$$Li^+ + e^- + H_2O \rightarrow LiOH + \tfrac{1}{2} H_2 \qquad \textbf{Equation 7-3}$$

The inability to reinsert all the extracted lithium ions after first charge has been observed in the past; for example, a capacity loss of 8-41%[71], 60%[70], and 70%[12] in the first cycle were reported. A protective coating such as a parylene over-layer or glassy LiPON layer was reported by Neudecker *et al.* to reduce that capacity loss and improve the battery cycling performance[70]. As expected, at higher charge rates which correspond to higher current densities, less charge is retried back from the $Li_xV_2O_5$ electrode. Slower

rates allow for sufficient charge transport time and electron transfer reactions occur at conditions closer to equilibrium.

Shown in Figure 7-6 is the first charge and discharge at rate of 0.5C of cells with 2 mm, 1 mm, and 0.5 mm active area edges. The cells contain LiPON electrolyte 350 nm thick. The left hand side of the plot shows the charging part and the right hand side shows the discharging part.

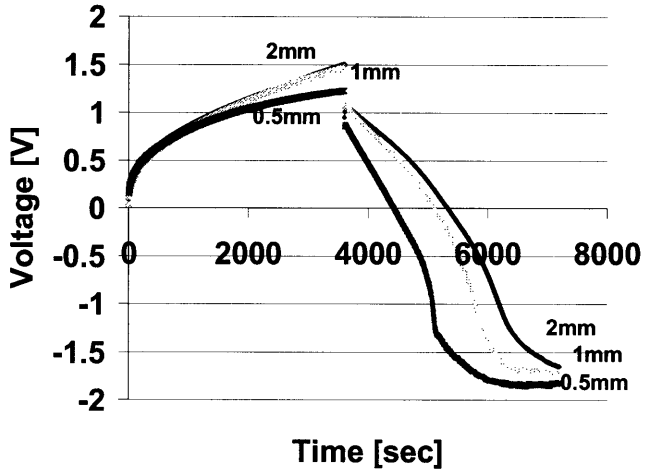


Figure 7-6: First charge and discharge at 0.5C rate of cells with 350 nm thick electrolyte and different active area sizes.

The voltage values measured in charging are similar for different cell sizes; however, it appears that the smallest size cell, the 0.5 mm cell is not charging to the same level as the bigger cells. There also appears to be a small difference between the 2 mm cell and 1 mm cell as well, that is, the 2 mm cell charges to a slightly higher voltage level than the 1 mm cell. The difference between cells of different sizes is more apparent in the discharge plot. The positive portion of the measured voltage extends for longer times with increasing cell size. The larger cells supply power for longer periods of time. If lithium ions are indeed lost through irreversible oxidation as is described in the reaction in Equation 7-3, smaller cells have smaller exposed surface compared to the volume containing lithium ions as can be seen in Table 7-2:

Cell edge size [mm]	Exposed area [cm^2]	Ratio of exposed area to active volume
2 mm	2×10^{-5}	20
1 mm	1×10^{-5}	40
0.5 mm	5×10^{-6}	80

Table 7-2: Area of cells exposed to the environment and ratio to active volume

As the ratio of area exposed to the environment to the active volume of the electrodes is greater, the percentage of lithium ions that can be retrieved back in discharging is lower. A protective coating to prevent exposure to moisture and oxygen in the environment, such as a thin polymer layer, might improve the cell performance without significantly adding to its weight.

Thickness reduction of solid electrolyte can be advantageous in terms of decreasing the cell's overall resistance and allowing for charging at higher rates. Figure 7-7 compares two 2 mm cells charged and discharged at 2C rate. One of the cells consisted of an approximately 350 nm thick electrolyte and the electrolyte thickness of the in the other cell was approximately 100 nm. The left hand side of the plot is the first charge of the cells and the right hand side is the first discharge of the cells.

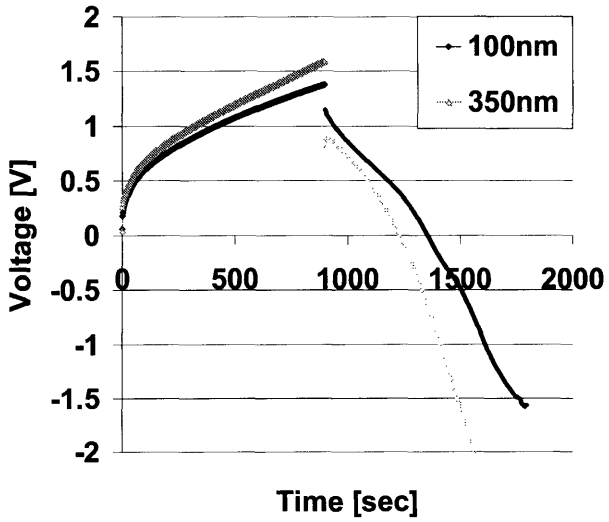


Figure 7-7: First charge and discharge for 2 mm cells with different electrolyte thickness at 2C rate.

In charge, the voltage measured for the thicker electrolyte is higher due to higher series resistance of the cell and the electrolyte in particular (higher IR_s in Equation 7-2). The voltage change between the end value of the charge and the starting value of the discharge is larger for the thicker electrolyte as expected. This indicates higher series resistance and hence increased voltage drops in charge and discharge. In discharge, the voltage measured for the thicker electrolyte is lower and remains positive for a shorter period of time. Since the electrolyte is thinner, the equilibrium charge transport time in the layer is shortened allowing for fewer deviations from the expected charge motion path at a forced higher rate. Figure 7-7 suggests that a reduction of the electrolyte thickness both reduces the cell's series resistance, and allows for more stable charge and discharge at faster rates. The electrolyte thickness can be reduced further by applying CMP to planarize the battery layers and achieving high quality smooth interfaces as was shown in Chapter 6.

7.3.3 Multi-Layer Thin-Film V_2O_5/LiPON/$LiCoO_2$ Cells

Studies done on cells with different electrode thicknesses have shown improved performance with thinner electrodes. Thicker electrodes exhibit lower discharge capacity due to limited diffusivity in the electrode as was shown for both $LiCoO_2$[133] and V_2O_5[9]. Thicker electrodes have a higher contribution to cell's resistance and exhibit capacity loss for the same charging rate. Reducing the thickness of all battery functional layers and connecting cells in parallel or in series to achieve higher capacity or voltage, respectively, will significantly improve battery performance. Shown in Figure 7-8 is a suggested schematic illustration of three V_2O_5/LiPON/$LiCoO_2$ cells connected in parallel with a bi-metal contact layer consisting of e.g. 30 nm of titanium and 500 nm of aluminum for both electrodes and a silicon oxide layer between the cells as an inter-level insulating layer. The cells are interconnected by metal vias with insulating material such as SiO_2 or Si_3N_4 coating the vias' sidewalls. Such via and interconnect technology is fairly similar to back-end processing for interconnects in silicon IC's. An external protective coating from the environment is not shown here but can be added. Note that the thicknesses of the layers in Figure 7-8 are not to scale.

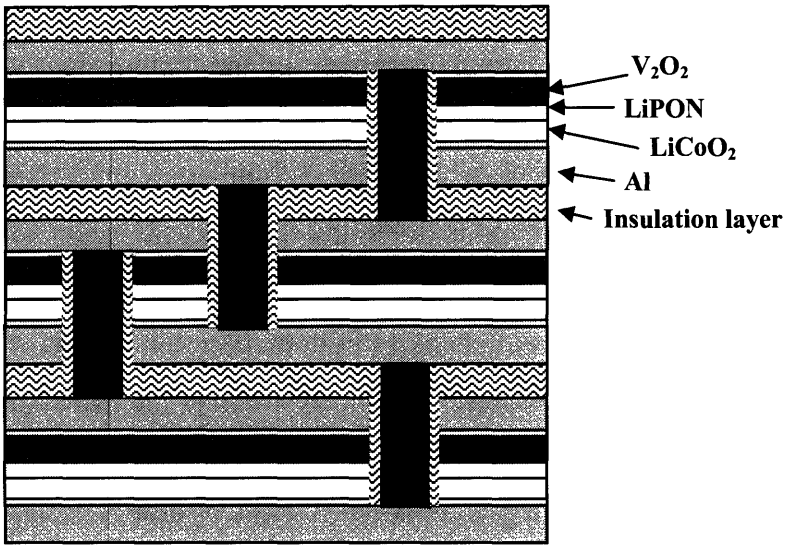


Figure 7-8: Schematic illustration of multi-level stack of three cells connected in parallel.

To put these thin-film batteries into perspective, the structure necessary to eliminate a typical laptop battery is now estimated. Although it is unlikely that this will be the initial application of these nano-batteries, it is an instructive exercise to calculate this equivalent structure.

A typical laptop lithium-ion battery, with a specified capacity of 6600 mAh is 2 cm thick with an area of 184 cm^2 and weighs 500 g (1.1 lbs) mostly due to heavy electrolyte and massive packaging. The theoretical capacity available from a 250 nm thick $LiCoO_2$ electrode on an area of 184 cm^2, assuming only 50% of the lithium is free to leave the layer, is 2.613 mAh. Based on that, 2526 layers, connected in parallel, in a similar manner to the one depicted in Figure 7-8, will be required in order to achieve 6600 mAh. In spite of the large number of layers, the total thickness of the 2526 layers stack will only be 0.53 cm and the expected weight of the stack is 295.18 g. The weight calculation is based on assuming density values of 4 g/cm^3, 2.5 g/cm^3, and 3 g/cm^3 for $LiCoO_2$[25], LiPON[19], and V_2O_5[63] respectively. The multi-layer rocking chair battery is expected to be four times thinner than a typical commercial lithium ion battery and 41% lighter in weight in addition to its improved performance in terms of reduced overall cell's resistance and shorter charge periods. The detailed calculation can be found in Appendix C. Note that due to the large number of layers required in order to achieve a comparable

capacity values to a commercial battery, the cost of production of such a battery may be high. In order to reduce the cost and still maintain the required capacity level, the layers thicknesses can be optimized to decrease the number of layers required and still obtain a satisfying performance improvement. There are many applications requiring lower power levels, thus not requiring the complete elimination of the entire bulk battery. For example, optimization of power management can be improved by moving some power to local chip regions, and thus lowering the requirements of the number of layers.

One example for a lower power application is a cellular phone battery. A typical cellular phone battery with a specified capacity of 700 mAh consists of an area of 18.5 cm^2, thickness of 1 cm, and weighs 227 g (8 Oz). To reduce the number of layers of the thin-film battery required to power a cellular phone, a thicker layer of $LiCoO_2$ may be used, for example 500 nm. With that thickness over an area of 18.5 cm^2, 1332 layers are required to supply the same capacity value of 700 mAh (assuming only half of the lithium ions are free to leave the $LiCoO_2$ layer). Assuming the same battery structure design such as the one illustrated in Figure 7-8, the total thickness of the multi-level thin-film battery would be 0.3 cm and its weight 36 g compared to 1 cm and 227 g respectively. This exercise demonstrates possible reduction of approximately 69% in thickness and 84% in weight by tailoring the multi-level thin-film battery structure and design to its requirements. The detailed calculation for this exercise can be found in Appendix D.

7.3.4 On-Chip Power

In search of the most suitable applications for an integrated thin-film battery on a chip, it is interesting to match the powering ability of the battery with existing technology requirements. For example, for the technology generation (node) of 0.13 μm, the dynamic random access memory (DRAM) ½ pitch length, a typical chip size will be 1.27 cm^2 and will consist of 9.7×10^7 transistors, which are $7.6 \times 10^7/cm^2$ [134]. The clock speed of such a chip is 1.684 GHz and it consumes 2.4 W for portable applications, which are 2.182 A for an operation voltage of 1.1 V[134].

The multi-layer thin-film battery as illustrated in Figure 7-8 consists of a 250 nm thick $LiCoO_2$, which on the area of 1.27 cm^2 consists of 1.27×10^4 g and gives a cell capacity of 0.018 mAh for one layer. In order to power a whole chip with 9.7×10^7 transistors operating at 1.684 GHz for an hour, 1.21×10^5 layers are needed. This unrealistic number shows that for the existing technology in the specified transistor density and clock speed, on-chip powering is not practical. However, for certain applications, fewer transistors operating at lower frequencies are sufficient. According to the data presented above, each transistor consumes 2.47×10^{-8} W, which for a voltage of 1.1 V are 2.25×10^{-8} A. This means that each batter layer can power 801 transistors at 1.684 GHz. For applications of portable communication chip, for example, operating at 10 MHz, 1.35×10^5 transistors can be powered by using 10 layers of the thin-film battery. In conclusion, for certain applications at certain operation conditions, the use of a multi-layer thin-film battery is practical and advantageous.

7.4 Summary and Conclusions

Using thin-film technology, a rocking-chair battery was fabricated consisting of high quality smooth interfaces and an ultra-thin electrolyte. The battery comprised of an approximately 250 nm thick $LiCoO_2$ anode, a 200 nm thick V_2O_5 cathode, and a 100 or 350 nm thick LiPON electrolyte. A surface morphology study of V_2O_5 was presented in this chapter showing that temperature had a major impact on surface roughness of amorphous or short-range order films. The fabrication of the V_2O_5/LiPON/$LiCoO_2$ cells was performed using microelectronics compatible processing and the they were electrically tested using a probe station and measurement equipment typical for microelectronic device testing. Not all lithium ions were inserted back into the $LiCoO_2$ upon first discharge and that may be due to irreversible lithium oxidation at the cell edges, exposed to the environment. The amount of charge retrieved at discharge has decreased with increasing charge rate corresponding to higher current densities and less stable conditions. The active area size was linked to the amount of retrieved charge as well; the larger the cell size, more charge was retrieved due to a smaller ratio of area

exposed to the environment and the volume containing lithium ions. An external thin coating may reduce that capacity loss. The 100 nm thick LiPON exhibited larger discharge capacity at high charging rate compared to the 350 nm. This chapter demonstrated that reducing the electrolyte thickness decreases the cell's series resistance and allows for charging and discharging at faster rates. These solid-state thin-film batteries have an overall thickness, including electrodes and electrolyte, of approximately 0.55 μm, the thinnest solid state battery that is known of to date. A theoretical calculation showed that 2526 layers of the rocking chair battery explored in this chapter can supply a comparable capacity to a commercial laptop lithium ion battery with one quarter of the thickness and 40% less weight. Moreover, a 0.13 μm node chip consisting of 1.35×10^5 transistors, operating at 10 MHz can be powered by only 10 layers of the thin-film battery. In additions, such a battery would likely have extremely fast charging times due to the very thin layer thicknesses.

8 Summary of Results, Conclusions, and Future Work

8.1 Overview

In the scope of monolithic integration, this work focused on creating a power unit on a silicon chip. The research described in this thesis was performed by approaching the subject from the microelectronic field, using thin-film technology, and processing and characterization methods to develop and study an integrated thin-film lithium ion battery. Two material systems were explored: one new to the battery field and composed of microelectronic compatible materials, and the second one, a more conventional lithium ion material system. In this thesis, Chapter 2 gave a background for batteries in general, solid-state batteries, and lithium ion batteries in particular. The materials that are used for the different functionalities of the battery are described as well as deposition methods and performance characteristics. Chapter 3 focused on the material systems selected for this work: $LiCoO_2/SiO_2$/polysilicon and V_2O_5/LiPON/$LiCoO_2$. A detailed background and literature survey was given as well as the reasoning for the systems' selection. In Chapter 4 the experimental procedures used to fabricate the cells are described and early materials characterization results were presented. Also in Chapter 4, the analysis techniques used for characterization in this work were described. Chapter 5 reported the study of lithium transport in SiO_2 for electrolyte applications. The first results of the $LiCoO_2/SiO_2$/polysilicon cells were presented. Chapter 6 focused on improving the fabrication process for the $LiCoO_2/SiO_2$/polysilicon cells as well as their interfacial quality by introducing CMP as a planarization method. Chapter 7 utilized thin-film knowledge and technology in fabricating a thin-film rocking-chair V_2O_5/LiPON/$LiCoO_2$ battery with an ultra-thin electrolyte. This Chapter summarizes the main results presented in the three stages of the project (Chapters 5-7) and suggests paths for future extension of this work.

8.2 Summary of Results and Conclusions

8.2.1 Lithium Transport in SiO_2 for Electrolyte Applications

Two existing CMOS materials and one new material were explored for the construction of a potential battery or novel device structure. Thermally grown silicon dioxide as thin as 9 nm was studied in order to act as an electrolyte layer in the solid state battery integrated on silicon. The $LiCoO_2$ cathode was RF sputtered and a highly doped n-type polysilicon anode was grown by LPCVD. All structures were fabricated using conventional microelectronics fabrication technology. Cells consisting of active area sizes of 5×5 mm^2, 2×2 mm^2, and 1×1 mm^2, and SiO_2 thickness of 9-40 nm were analyzed. The charge and discharge behavior of the $LiCoO_2/SiO_2$/polysilicon cells was studied using a probe station and measurement equipment typical for microelectronic device testing. The charge and discharge plots indicated that lithium ions were successfully transported back and forth through the SiO_2 layer. Impedance measurements were used to model the equivalent circuit for the potential ultra-thin battery and its structure and layers interfaces were evaluated by electron microscopy imaging. The high series resistance of the SiO_2 electrolyte led to an over-potential measurement and limited the discharge capacity. A reduction of the electrolyte thickness was shown to be limited by the anisotropy of the oxidation rate of the polysilicon granular surface due to creation of shorting paths in the electrolyte. Successful transport of lithium ions across the oxide was demonstrated by the charging and discharging of the cell and by Li-Si precipitates appearing on the polysilicon surface. The first stage of the project demonstrated the concept of an ultra-thin as-deposited-lithium-free electrically insulating electrolyte compatible with microelectronic materials, fabrication and characterization methods.

8.2.2 LiCoO2/SiO2/polysilicon Cells Planarized by Chemical Mechanical Polishing

The second stage of the project dealt with improving the fabrication process as well as the interfacial quality of integrated solid-state thin-film $LiCoO_2/SiO_2$/polysilicon power cells. Cells consisting of an ultra-thin, lithium-free SiO_2 electrolyte with a

thickness range of 7–40 nm with active area sizes of 5×5 mm^2, 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2 were created by using conventional microelectronics processing and expertise. In order to improve interfacial quality, in particular to reduce interface roughness, a planarization step was implemented in the fabrication process. The planarization step utilized CMP, a well known planarization method in microelectronics, in polishing the polysilicon anode layer. The polysilicon RMS roughness was reduced from 8.06 nm to 0.53 nm, thereby leading to smoother interfaces and to a subsequently higher quality SiO_2 electrolyte layer with an overall more uniform thickness. The OCV of the cells was found to be ~2.19 V. The $LiCoO_2$/SiO_2/polysilicon cells exhibited improved performance when prepared with the CMP planarization step, and up to 40% of the charge was retrieved from the cells compared to a maximum of 14.52% retrieved from the non-planarized cells. The second stage of the project demonstrated the first application of CMP to fabricating an electrochemical device and its contribution to considerably improved performance.

8.2.3 Integrated V_2O_5/LiPON/$LiCoO_2$ Thin-Film Battery

Thin-film and microelectronic technology was utilized to fabricate a rocking-chair battery with high quality smooth interfaces and an ultra-thin electrolyte. The battery comprised of an approximately 250 nm thick $LiCoO_2$ anode, 200 nm thick V_2O_5 cathode, and a 100 or 350 nm thick LiPON electrolyte. Cells with active area sizes of: 2×2 mm^2, 1×1 mm^2, and 0.5×0.5 mm^2 were studied. A surface morphology study of V_2O_5 was conducted and revealed the substrate temperature as an important deposition parameter in controlling the amorphous or short-range order morphology of the films. The fabrication of the V_2O_5/LiPON/$LiCoO_2$ cells was performed using microelectronics-compatible processing and they were electrically tested using a probe station and measurement equipment standard for microelectronic device testing. First discharge capacity loss was observed and attributed to irreversible lithium oxidation at the cell edges, which were exposed to the environment. The amount of charge retrieved at discharge was shown to decrease with increasing charge rate corresponding to higher current densities and more extreme conditions. The larger the active area size was, more charge was retrieved. This

observation was attributed to a smaller ratio of area exposed to the environment to the volume containing lithium ions. The 100 nm thick LiPON exhibited larger discharge capacity at high charging rate compared to the 350 nm. A theoretical calculation compared a typical laptop lithium battery to 2526 layers of the V_2O_5/LiPON/$LiCoO_2$ rocking chair battery. The battery thickness can be reduced to one fourth and its weight can be lowered by 40%. Manufacturing a 2526 layered battery can be considerably expensive. However, an optimization of the battery structure can be made in order to maintain the improved performance while decreasing the number of layers and hence the cost of production. A calculation compared the technology requirements and the power ability of the multi-layer thin-film battery and found that a 1.3 μm technology generation chip consisting of 1.35×10^5 transistors operating at 10 MHz can be powered by 10 layers of the thin-film battery. The third stage of this work demonstrated the application of thin-film technology to a conventional material system battery with an overall thickness (including electrodes and electrolyte) of approximately 0.55 μm. The integration of this battery can be practical for certain applications at certain operation conditions. The reduction of electrolyte thickness was shown to be essential to improving cell's performance by decreasing the cell's series resistance and allowing for charging and discharging at faster rates.

8.3 Suggestions for Future Work

8.3.1 Improving Cell Performance

All cells studied in this work exhibited a significant capacity loss upon the first charge and discharge cycle. This has been observed in the past by various researchers[71,70,12]. One of the solutions proposed to reduce this capacity loss and increase the percentage of charge retrieved at discharge, is to use a protective coating on the battery to prevent its exposure to moisture and oxygen in the environment. Such an over-layer can be especially useful for the V_2O_5/LiPON/$LiCoO_2$ cells in which lithium ions are believed to be lost via an oxidation reaction at the cell edges which are in contact with the atmosphere. An example for such a coating can be a thin polymeric layer such as a clear

photoresist that can be applied by spin coating and patterned in order to allow external access to cells' contacts. In the $LiCoO_2/SiO_2$/polysilicon material system, precipitates were observed on the polysilicon surface and are responsible for lithium loss and decrease in charge retrieval. Those precipitates were believed to be Li-Si compounds that erupted from the polysilicon surface as a result of a large volume change accompanying their formation reaction. A protective coating may be applied to this material system as well, although it will not address the volume change problem and therefore might not affect the discharge performance.

The implementation of CMP as a planarization step in the $LiCoO_2/SiO_2$/polysilicon cells was shown to be beneficial. Cells performance was significantly improved when they consisted of a planarized polysilicon layer. Ideally, CMP can be applied to other battery layers and in particular to the V_2O_5/LiPON/$LiCoO_2$ material system. Planarizing of $LiCoO_2$ prior to LiPON deposition can allow further reduction of electrolyte thickness reducing cell's resistance and improving overall performance. When continuing to deposit several battery layers, the top electrode, V_2O_5 in this work, should be planarized as well. This requires the practice of a working CMP system that can withstand lithium contamination as well as tailoring planarization parameters and chemical solution to $LiCoO_2$ or V_2O_5 polishing.

As is known from CMOS processing, interfacial quality and device performance are highly sensitive to contamination. The deposition system utilized in this work consisted of a single RF sputtering gun and two DC guns. In the second material system, this imposed the need to vent the vacuum chamber and replace the RF sputtering targets between depositions of each layer. An improved performance can be achieved by depositing the whole battery sequence under high vacuum without opening the chamber and exposing the battery to contaminating air. A deposition system containing three RF guns can allow the deposition of the V_2O_5/LiPON/$LiCoO_2$ cells with no breaking of the vacuum. A system consisting of two RF guns and one DC gun can also be used and a reactive sputtering for the V_2O_5 layer (vanadium target in oxygen ambience) can be explored.

8.3.2 Further Testing and Characterization

Electrical characterization of the cells was performed using a standard probe station and a parameter analyzer typically used for microelectronic device characterization. This allowed for deeper understanding of some aspects of the research, however was limiting in terms of more extensive and longer electrochemical characterization. Ideally, a probe station can be used in conjunction with typical electrochemical testing equipment. This way, the thin-film cells can be contacted with delicate probes while conventional battery testing can still be performed in parallel to the ones performed in this work. Additional electrochemical testing that can be facilitated by such an apparatus can include cycling of the battery for longer periods of times (e.g. a few days) and hence utilizing lower charge and discharge rates, as well as extensive impedance measurement characterization.

An *in-situ* TEM analysis of charging and charging miniature TEM battery samples can lead to more understanding regarding the microstructure and the internal reactions which occur in a thin-film battery. This requires a combination of a probe station to contact the sample and initiate the electrochemical process and a TEM to examine it in real time. Such a combination might not yet exist, however it might be possible in the future.

8.3.3 Cell Integration

This work dealt with developing an integrateable thin-film battery in terms of choice of materials, performance requirements, and processing methods. Future work may concentrate on taking the integration one step further. Initially, a few levels cell such as the one described in Figure 7-8 can be fabricated, using silicon as an inter-level insulation. The layers can be connected in parallel, to increase battery capacity, by vias made of a metal and sidewalls coated with an insulating material such as Si_3N_4.

The next step of integration can be fabricating an integrated cell on the back of a silicon substrate integrating a solar cell and an LED diode using a SiGe virtual substrates used in our group. The battery can power a yellow green LED for example, fabricated

from InGaP/GaP[135], while the solar cell, e.g. from GaAs, can charge the battery. A schematic illustration of this integrated unit can be seen in Figure 8-1.

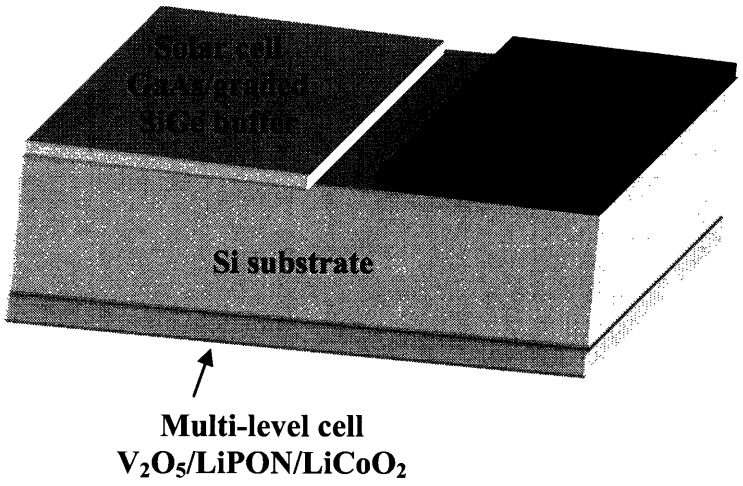


Figure 8-1: Schematic illustration of an integrated unit consisting of an LED, a multi-level battery, and a solar cell

8.3.4 Additional Material Systems and Further Applications

This work demonstrated that SiO_2, thermally grown from silicon is an interesting candidate for electrolyte applications. However, volume changes issues are associated with the use of a silicon electrode. When considering the two material systems studied in this work, it might be interesting to explore an ultra-thin SiO_2 electrolyte grown by CVD or RF sputtered in an integrated $V_2O_5/SiO_2/LiCoO_2$ battery. The low voltage requirements of microelectronics allows for many new materials to be explored. One interesting group of materials to explore which is suitable for the scope of our group is III-V semiconductors. AlSb and InSb are two examples of the III-V group materials that were studied as anodes in lithium batteries[42].

Controlled ion transport in SiO_2 can be applied to the creation of alternative complex devices. Lithium presence in silicon may alter its optical properties, for example its refractive index. A voltage signal can induce lithium transport into silicon, change its

refractive index, and hence alter the optical path of light traveling through it. This could be applied to electro-optical devices such as an optical switches or light modulators.

Appendix A: Calculations of theoretical specific energy and capacity

Energy density in cathodes:

$$E_{th} = \frac{nF \times V_{AVG}}{M_{cathode}}$$

n – number of lithium ions inserted

F – Faraday constant = 96487 C/mole

V_{AVG} – the average voltage against lithium

$M_{cathode}$ – molecular mass of the cathode [g/mole]

For example, 1 lithium inserted in V_2O_5 assuming an average voltage of 2.8 V versus lithium:

$$\frac{1 \times 96487 \times 2.8}{182} \times \frac{1000}{3600} = 412 \frac{Wh}{Kg}$$

Note that the conventional units for energy densities are Wh/Kg, therefore, a unit adjusting factor is added.

Capacity density of Anodes:

Similarly, the specific capacity of an anode is given by:

$$C_{th} = \frac{nF}{M_{cathode}}$$

For example, the $Li_{21}Si_5$ phase consist of 4.2 lithium per 1 silicon. The theoretical capacity density for this phase is therefore:

$$\frac{4.2 \times 96487}{28} \times \frac{1000}{3600} = 4020 \frac{mAh}{g}$$

Note that the conventional units for capacity densities are mAh/g, therefore, a unit adjusting factor is added.

Appendix B: Calculations of current values corresponding to C –rates

Current calculation example for 1 C rate and 0.5×0.5 cm^2 area:

The available lithium mass in grams is given by:

$$M_{Li} = A \times t \times \rho$$

A – Active area of the cell

t – $LiCoO_2$ thickness

ρ – Film's density.

The current corresponding to a 1 C rate in [mA] would be:

$$I = M_{Li} \times C_{LiCoO_2} \times x$$

M_{Li} – the available lithium mass

C_{LiCoO2} – $LiCoO_2$ capacity (for 0.5 lithium) in [mAh/g]

x – constant (for lithium content in the film)

For 1 C rate and 0.5×0.5 cm^2 area:

$$I = 0.25cm^2 \times 2.5 \times 10^{-5} cm \times 4gcm^{-3} \times 142mAhg^{-1} \times 0.7 \times 10^{-3} = 2.485 \times 10^{-6} A$$

Currents used for different active-area size cells and their corresponding C rates:

Size of active area [cm^2]	C/20	C/10	C/4	C/2	1C	2C
0.25	125 nA	250 nA	625 nA	1.25 μA	2.5 μA	5 μA
0.04	20 nA	40 nA	100 nA	200 nA	400 nA	800 nA
0.01	5 nA	10 nA	25 nA	50 nA	100 nA	200 nA
$2.5X10^{-3}$	1.25 nA	2.5 nA	6.25 nA	12.5 nA	25 nA	50 nA

Appendix C: Calculations of theoretical capacity in a V_2O_5/LiPON/$LiCoO_2$ cells stack:

From an internet website selling laptops:

(http://www.costcentral.com/proddetail/IBM/08K8197/894190/)

Li ion laptop battery dimensions: 8.9" × 3.2" × 0.8" (22.606 × 8.128 × 2.032 cm^3)
Battery weight: 1.1 lbs which are 500 g
Battery capacity: 6600 mAh

The battery area: 184 cm^2, thickness: 2.032 cm

The V_2O_5/LiPON/$LiCoO_2$ battery on the same area:

The lithium ions originate in the $LiCoO_2$ layer.

$LiCoO_2$ volume: 0.0046 cm^3, area – 184 cm^2, thickness – 250 nm
$LiCoO_2$ density: 4 g/cm^3 (estimated from averaging several reports in the literature)

$LiCoO_2$ weight in 250 nm and 184 cm^2 : 0.0184 g

$LiCoO_2$ theoretical specific capacity: 142 mAh/g (for 0.5 Li)

Capacity in 250 nm $LiCoO_2$ (for 0.0184 g): 2.6128 mAh

Number of layers needed for 6600 mAh (the laptop battery capacity): 2526

Thickness of one layer (including: 500 nm Al, 30 nm Ti, 250 nm $LiCoO_2$, 100 nm LiPON, 200 nm V_2O_5, 500 nm Al, 30 Ti, and 500 nm SiO_2 inter-level layer):

2150 nm which are 2.15×10^{-4} cm

Thickness of 2526 layers: 0.543 cm compared to ~2 cm thickness of the laptop battery. Reduction of ~72% of thickness

Comparison of weight:

Al weight in 500 nm thick layer: 0.0248 g
Ti weight in 30 nm thick layer: 0.0109 g
LiPON weight in 100 nm thick layer: 0.0046 g
V_2O_5 weight in 200 nm thick layer: 0.011 g
SiO_2 weight in 500 nm thick layer: 0.0202 g
$LiCoO_2$ weight in 250 nm thick layer: 0.0184 g

Total weight of one layer of battery stack (two Al, two Ti, one active cell, and one SiO_2 inter-level layer): 0.1161 g

Total weight of 2526 layers: 295.183 g compared to 500gr weight of the laptop battery. Weight in pounds: 0.645 lbs or 10.323 Oz compared to 1.1 lbs of the laptop battery.

~59 % of the weight which is a ~41 % reduction of the battery weight

Appendix D: Calculations of theoretical capacity in a V_2O_5/LiPON/$LiCoO_2$ cells stack – different design and different application:

From an internet website selling cell phone accessories:

(http://www.batteries4less.com/siements/S56/batteries/siements-S56-oem-standard-li-ion-battery-V30145-k1310-x250.html)

Li ion cell phone battery dimensions: $5 \times 3.7 \times 1$ cm^3

Battery weight: 8 Oz which are 227 g

Battery capacity: 700 mAh

The battery area: 18.5 cm^2, thickness: 1 cm

The V_2O_5/LiPON/$LiCoO_2$ battery on the same area:

The lithium ions originate in the $LiCoO_2$ layer.

$LiCoO_2$ volume: 0.000925 cm^3, area – 18.5 cm^2, thickness - 500nm

$LiCoO_2$ density: 4 g/cm^3 (estimated from averaging several reports in the literature)

$LiCoO_2$ weight in 500 nm and 18.5 cm^2 : 0.0037 g

$LiCoO_2$ theoretical specific capacity: 142 mAh/g (for 0.5 Li)

Capacity in 500 nm $LiCoO_2$ (for 0.0037 g): 0.5254 mAh

Number of layers needed for 700 mAh (the cell phone battery capacity): 1332

Thickness of one layer (including: 500 nm Al, 30 nm Ti, 500 nm $LiCoO_2$, 100 nm LiPON, 200 nm V_2O_5, 30 nm Ti, 500 nm Al, and 500 nm SiO_2 inter-level layer):

2360 nm which are 2.36×10^{-4} cm

Thickness of 1332 layers: 0.3144 cm compared to 1 cm thickness of the cell phone battery.
Reduction of ~69% of thickness

Comparison of weight:

Al weight in 500 nm thick layer: 0.0025 g
Ti weight in 30 nm thick layer: 0.0066 g
LiPON weight in 100 nm thick layer: 0.00044 g
V_2O_5 weight in 200 nm thick layer: 0.0011 g
SiO_2 weight in 500 nm thick layer: 0.00204 g
$LiCoO_2$ weight in 500 nm thick layer: 0.0037 g

Total weight of one layer of battery stack (two Al, two Ti, one active cell, and one SiO_2 inter-level layer): 0.0136 g

Total weight of 1332 layers: 36.24 g compared to 227 g weight of the laptop battery.
Weight in pounds: 0.0797 lbs or 1.28 Oz compared to 8 Oz of cell phone battery.

~16 % of the weight which is a ~84 % reduction of the battery weight

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