A Circular Electrostatic Zipping Actuator for the Application of a MEMS Tunable Capacitor

by

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Abstract

Micromechanical circuits such as MEMS switches, tunable capacitors (varactors) or resonators in general have lower loss and consume less power than their CMOS counterparts and have seen an increase of applications in high-value communication systems as well as low-cost commercial communication networks. Significant advances have been made in the areas of MEMS switches. However, MEMS resonators that operate in GHz range, have high quality factor and are highly tunable are still under active pursue. In this thesis, we study the design of a tunable capacitor that can be integrated with a resonant cavity to form a tunable electromagnetic cavity resonator. The design, fabrication, modeling and testing of a proof-of-concept MEMS tunable capacitor are presented.

The tunable capacitor consists of a circular fulcrum that acts as a pivot for a thin silicon plate. The outer plate is an electrostatic, circular zipping actuator that bends the center plate through the fulcrum. By doing so, it opens the gap of the capacitor, which is formed by two smooth surfaces, one being the center plate, that are initially separated by a dielectric layer. The design is enabled mainly by the deep reactive ion etching and anodic bonding microfabrication techniques.

The structure of the device is modeled using both numerical methods with Matlab boundary value problem (BVP) and finite element analysis with ANSYS. The Matlab results match well with the ANSYS results for the before pull-in and the zip-in actuation stages. The Matlab model is used to perform parametric design studies.

Two types of assembly methods are used to construct the final devices: wafer-level and die-level. Depending on how they are assembled, the devices operate in different actuation stages. A laser interferometer system is used to measure the center displacement of the plate and an impedance analyzer is used to measure the capacitance change. Testing results are comparable with the ANSYS simulations.

Based on the lessons learned from the proof-of-concept tunable capacitor, a design of the electromagnetic cavity resonator with an integrated tunable capacitor is proposed.

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There have been many people who helped me in different ways for my thesis work. I need to thank James White, Hong Ma and Jian Li for their inspiration of the project idea, and David Wentzloff for his contributions to anything electromagnetic. Hanqing Li deserves my most respect for his many valuable inputs and unconditional help and advises related to fabrication. The people who have made my research more lively include Lodewyk Steyn for his generous help with the Pogo pins and the die-level anodic bond system; Alex Sprunt and Alexis Webber for their valuable inputs, and Ole Nielsen for all the casual discussions. I especially have to thank Kate Thompson. It was her who made ANSYS available to many students in the institute, and it was her who taught a lot of us its basics. She was undoubtedly the ANSYS "queen." I also need to thank the rest of the PERG and Schmidt group members for their friendship. Life would have been dull without them.

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opinion, she is the role model for all women engineers/professors.

I owe the most to my family. I could not see an end to my thesis work until into my life came the beginning of a new life - my daughter Claire. She has changed my life by dividing it into two worlds, each of which is often enclosed to itself, and then binding them together into one reality that is surprisingly harmonious. She is the beacon in my life, and my source of strength and determination and all other emotions. Not any less important to me is Simon's love and sacrifice. Nothing is more soothing than seeing him cooking, doing laundry, biking Claire to school and taking a bath for Claire. Je t'aime, Simon! We did not do this thesis alone - it would have been impossible without our families, who besides being very proud grandparents, provide unconditional help and support to us. To my parents and Mado et Marcel, I do not know how I could ever express my gratitude.

This thesis is dedicated to my grandma and is woven with memories of her. Nothing I did or will do could ever compare with what she did throughout her life. I will always miss her.

The printout of this thesis is delayed and so I must append one more part to the acknowledgements. Before I had the chance to print this thesis out, my mother was diagnosed with Glioblastoma Multiforme - the most malignant type of brain cancer. In a strange way, I had been denying the possibility of a serious illness and had chosen to listen to my mother's "doing fine; don't worry" message over the phone, while I was entirely focused on my work - but deep down, I always felt that I was competing with something. Only when I finished I realized that it was the tumor that I tried to outrun. I'm left powerless to try to prove that my mother would have had much greater chance of survival if I would have been there for her much earlier. There is only one thing I know for sure, she sacrificed herself, even long before the tumor was there, for me to fulfill my dream.

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Nomenclature

Greek

β	a constant for the fulcrum
δ	axial deflection of the fulcrum
ε	permittivity of air
ε_{ox}	permittivity of oxide
θ	phase of the impedance
λ	wavelength of the laser measurement beam
ρ	sheet resistivity of silicon
σ_{Au}	electrical conductivity of gold
σ_{Si}	electrical conductivity of silicon
μ_o	vacuum permeability
ν	Poisson ratio
ξ	normalized value
ϕ	rotation at the joint between the fulcrum and the plate
ω	frequency
ω_o	resonant frequency

Roman

a	inner radius of the actuator
A	normalized value
b	outer radius of the actuator
c	thickness of the oxide insulator
C	capacitance
C_{11}	capacitance between the silicon plate and the central capacitor metal surface

C_{22}	capacitance between the silicon plate and the actuator metal surface
C_{12}	mutual capacitance between the capacitor and actuator metal surfaces
C_{cap}	measured capacitance between the CAP and GND terminals
C_{act}	measured capacitance between the ACT and GND terminals
C_f	final capacitance
C_i	initial capacitance
C_{ox}	capacitance across the oxide layer during anodic bond
C_{p1}	parasitic capacitance between the actuator metal surface and all other surfaces except the actuator metal surface
C_{p2}	parasitic capacitance between the actuator metal surface and all other surfaces except the capacitor metal surface
C_{scr}	capacitance across the space charge layer
d	depth of the cavity resonator
D	flexural rigidity of the plate
D_f	flexural rigidity of the fulcrum
E	young's modulus of silicon
f	frequency
f_o	resonant frequency
F	electrostatic force
F_1	the nominal vacuum wavelength of one polarized laser beam
F_2	the nominal vacuum wavelength of the other polarized laser beam
g	initial air gap of the actuator
h	thickness of the top plate
L	inductance
I	current
m	width of metal interconnect
M_1	bending moment per unit length acting at the joint by the outer plate
M_2	bending moment per unit length acting at the joint by the fulcrum
M_3	bending moment per unit length acting at the joint by the center plate
M_r	radial bending moment per unit length of the plate
M_t	tangential bending moment per unit length of the plate

M_x	bending moment per unit length of the fulcrum of a section perpendicular to the x axis.
M_φ	bending moment per unit length of the fulcrum of an axial section
p	displacement measured by the laser interferometer
Q	shear force per unit length of the plate
Q	quality factor
r	radius of the plate
r_o	outer radius of the bottom electrode
R	normalized radius of the outer plate, also series resistance
R'	normalized radius of the center plate
R_1	radius of capacitor
R_2	radius of toroid
R_C	resistance of capacitance
R_L	resistance of toroid
R_{glass}	resistance across the glass wafer
R_{ox}	leakage current resistance during anodic bond
R_{scr}	leakage current across the space charge layer
r_a	radius of the fulcrum
r_c	radius of the capacitor
s	radial pin-down position of the plate after zip-in
t	thickness of the fulcrum
V	actuation voltage
w	vertical displacement of the plate
W	normalized vertical displacement of the plate
w_{Au}	skin depth of gold
x	axial coordinate of the fulcrum
X	normalized axial coordinate of the fulcrum
y	radial deflection of the fulcrum
Y	normalized radial deflection of the fulcrum
z	vertical deflection of the center plate
Z	normalized vertical deflection of the center plate

$\|Z\|$	magnitude of the impedance

Acronyms

ACT	the terminal that connects to the bottom electrode of the actuator
BOE	buffered oxide etch (HF)
BOX	buried oxide
BVP	boundary value problem
CAP	the terminal that connects to the bottom electrode of the capacitor
DI	deionized water
DRIE	deep reactive ion etch
FEM	finite element analysis
GND	the terminal that connects to the silicon plate
LC	inductor-capacitor
LPCVD	low pressure chemical vapor deposition
MEMS	micro-electro-mechanical system
MOS	metal-on-semiconductor structure
MTL	microsystems technology laboratories at MIT
MTR	maximum tuning ratio
ODE	ordinary differential equation
PCB	printed circuit board
PECVD	plasma enhanced chemical vapor deposition
PSI	phase-shifting interferometry for the *Wyko* system
RF	radio frequency
SEM	scanning electron microscopy
SOI	silicon on insulator
STS	deep reactive ion etcher from Silicon Technology Limit
UWB	ultra wide band communication
VCO	voltage controlled oscillator

VSI	vertical-scanning interferometry for the *Wyko* system
ZMI	Zygo motion interferometer system

Chapter 1

Introduction

In this thesis, design, fabrication, modeling and testing of a proof-of-concept MEMS tunable capacitor are presented. The capacitor, together with a separate project on an externally actuated, tunable cavity resonator, is originally a joint effort in the development of a MEMS tunable electromagnetic cavity resonator. The idea of such a cavity resonator is inspired by the Nanogate and the electrostatic ziping-actuated micro relay, two devices that have been developed in our group. In this chapter, we will first elaborate on our inspirations for a cavity resonator and motivations for developing the tunable capacitor. And then literature research on tunable capacitor as well as resonators will be presented.

1.1 The Nanogate

The concept of implementing a tunable capacitor with circular zipping actuation traces back to a micro fluidic valve developed by J. White in our group [1]. The structure of the valve is dubbed "the Nanogate." It is a silicon-based MEMS device capable of nanometer-scale control over separation of two mm-scale polished surfaces. The separation between the surfaces can range from contact to several microns, controllable with nanometer resolution.

The function of the Nanogate can be illustrated by the two cross-sectional schematics as shown in Figure 1.1. In the figures, the axis of revolution is through the center of the device. The device comprises a circular silicon diaphragm that is supported by a circular fulcrum as shown in Figure 1.1 a). The fulcrum acts as the torsional spring and allows the diaghragm to bend when a deflection is applied on the periphery by an external piezoelectric servo actuator, as shown in Figure 1.1 b). The center boss is hence lifted away from the glass base, creating a fluidic path. The device is fabricated by anodically bonding an etched silicon wafer to a Pyrex glass substrate. The lever-fulcrum action of the structure allows precise control of the gap opening. The opening and closing motion of the Nanogate has been measured in increments as small as 2.4 nm, the resolution of the laser measurement unit [2]. A capacitor sensor that measures the gap separation by detecting the capacitance change has also been developed in the group [3].

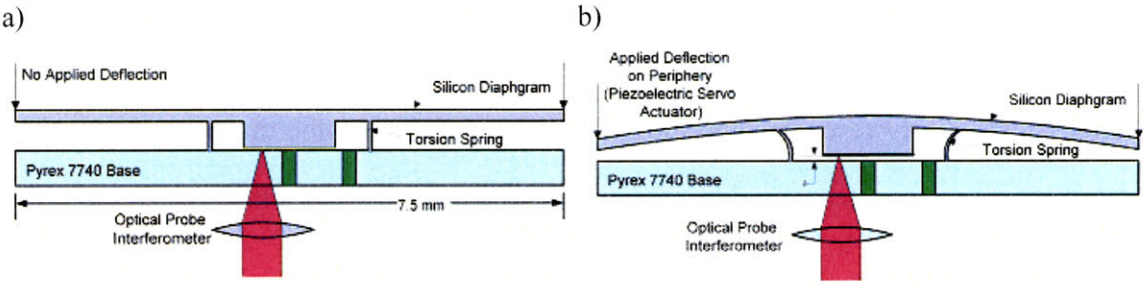


Figure 1.1. Operation principle of the Nanogate showing a) undeflected mode and b) deflected mode. (Courtesy of J. White)

The observation that the high-aspect-ratio gap of the Nanogate can be precisely controlled has sparked the idea of a high tuning-ratio capacitor. A laterally-moving electrostatic zipping actuator using two opposing actuation surfaces etched with deep reactive ion etching techniques designed to actuate a micro relay was also developed in our group [4]. Combining these two ideas, a tunable capacitor with embedded actuator becomes a

solid concept. In the next section, we will explain how the device could be transformed from a micro fluidic valve to a tunable electronic device.

1.2 Electrostatic zipping actuator for a tunable capacitor

The Nanogate valve uses an external piezoelectric actuator to apply a deflection to the periphery of the circular lever. While this is acceptable for a valve which will be installed in a much larger system, an external actuator will not be practical for a tunable capacitor that will be used inside a wireless transceiver, for example. If the actuator can be embedded into the device, lots of space can be saved. This can be best done by using the silicon diaphragm as an electrostatic zipping actuator.

It follows that we can design a capacitor that is formed by two smooth surfaces initially separated by a dielectric layer. It can be tuned by applying voltage to a zipping actuator that is electrically isolated from the capacitor. The actuation causes one capacitor surface to pry apart from the other and controls the gap between the surfaces in the nanometer range. Furthermore, it is possible to integrate an inductor within the device to form an integrated LC tank. A preliminary concept is shown in Figure 2, where a variable capacitor is located at the center of the device. A single-turn inductor is embedded in the lever-fulcrum structure. The inductor operates as a resonant cavity, with a Q on the order of a hundred.

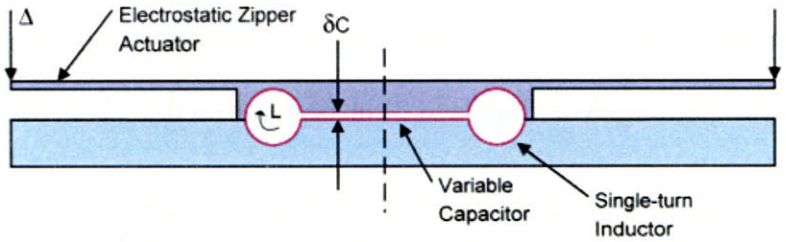


Figure 1.2. Schematic of the conceptual design of the tunable LC tank. (Courtesy of J. White).

The concept of an integrated, electrostatically actuated tunable capacitor and that of an electromagnetic resonator tuned by external piezoelectric transducer are being studied independently. In this thesis, only the tunable capacitor will be presented. We will introduce briefly the work of the resonator using a single-turn, toroidal inductor by another colleague. In the following sections, we will explore the applications for a tunable capacitor and a tunable LC tank or resonator.

1.3 Magnetically Coupled Electromagnetic Cavity Resonator

The quasistatic electromagnetic cavity resonator consists a parallel-plate capacitor surrounded by a single-turn, toroidal inductor. It is fabricated using processes such as KOH etch, shallow reactive ion etch, sputtered gold metallization and thermal compression wafer bonding [5].

Figure 1.3 shows a cross-sectional view of the concept of the cavity resonator. The toroidal cavity is formed by joining two KOH-etched wafers using thermal compression bonding of gold surfaces. Gold covers the entire the cavity for high-Q operation. The center capacitor plates are pushed to close the gap by an external piezoelectric transducer. Experiments showed that the resonator exhibited Q ranged from 110 to 240 with a frequency tuning range from 2.5 GHz to 4.0 GHz. However, because the current design uses a wire loop to magnetically couple the EM field in the cavity, it requires a delicate pick-and-drop process, which limits the practicality of the design. What can be done to improve the function of the device include 1) use electrical coupling to the capacitor instead of magnetic coupling through wire loop and 2) incorporate an integrated tunable capacitor to replace the external transducer.

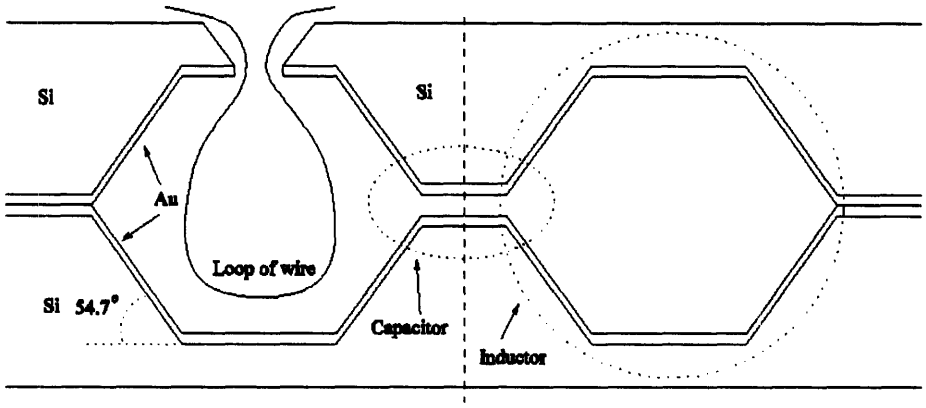


Figure 1.3. Cross-sectional schematic of the cavity resonator with magnetic coupling [5].

1.4 Tunable capacitor

A tunable capacitor (or varactor) is a widely used component in transceiver circuits for RF communication devices. Its applications include low noise amplifiers, band pass filters, voltage-controlled oscillators (VCO), etc. Traditional solid-state varactors are made with p-n or Schottky-barrier junction types of semiconductor structures. A voltage bias applied to the p-n or Schottky diodes modifies the charge in the junction and hence changes the junction capacitance. These kinds of solid-state varactors, however, have large losses and a low tuning range (typically 30% or less), which are often the limiting factors in RF circuit design [6]. As the RF electronics consumer market continues to grow, there is a clear demand for new generations of consumer electronics to operate over a wide variety of Internet Protocol networks and standards, and as a result, they must possess multimode, multiband capabilities [7]. One solution that could make a frequency-hopping transceiver design a reality is to develop a new generation of tunable capacitors that have a large tuning ratio, high quality factor, linear response to RF power, low power consumption, and occupy a small space. Tunable capacitors fabricated with MEMS technology have shown

many merits in this respect.

MEMS tunable capacitors are mechanical devices that use various actuation methods, such as electrostatic or thermal actuation, to physically move the position of the plates or the dielectric constituents of a capacitor. For a parallel plate type of capacitor, if we define the plate area as A, the gap between the plates as g, and the permittivity of the media between the plates as ε, then the capacitance is expressed as,

$$C = \varepsilon \frac{A}{g} \tag{1.1}$$

If we define the unbiased capacitance as C_i, and the capacitance after tuning as C_f, then the tuning range is defined as [6],

$$\frac{C_f - C_i}{C_i} = \frac{C_f}{C_i} - 1 \tag{1.2}$$

and MTR is the maximum tuning range that can be achieved with the tuning capacitor. Another commonly used measure of capacitance change is the capacitance ratio, which is defined as the ratio of C_f: C_i.

For a resonator with an inductor L and a capacitor C in series or in parallel, the resonant frequency is $\omega_o = \frac{1}{\sqrt{LC}}$. If we would use this resonator for the application of Ultra Wide Band (UWB) communication, which requires tuning from 3.1-10.6 GHz with a 500 MHz band, we would need a tuning range of the capacitance that exceeds 11. Such a tuning range is impossible with solid-state varactors, but within reach using MEMS technologies. However, the figures of merits of a tunable capacitor include more than simply the tuning range. The Quality factor Q, which determines the loss of power in the device, is

critical to the performance of any band pass filter or VCO. Q is directly related to the parasitic resistance R in the circuit for series and parallel LC resonators respectively,

$$Q_{series} = \frac{1}{\omega_0 RC} \tag{1.3}$$

$$Q_{Parallel} = \omega_0 RC \tag{1.4}$$

Furthermore, it is also desirable for the capacitor to attain linear response or remain constant to RF power. In summary, it is important to evaluate the overall system performance when designing a tunable capacitor component.

Reports on MEMS tunable capacitors with tuning range greater than the traditional solid-state varactors have proliferated in recent years. A few of the papers also demonstrated the system performance of tunable filters or VCO's using MEMS tunable capacitors. Tunable capacitors can be roughly grouped into two types, analog-tuned and digital-tuned. Three different technologies are identified so far for building these capacitors: based on parallel-plate approach (by changing the vertical gap), interdigital design (by changing the horizontal gap), and fixed capacitor with switch (digital) type [8].

1.4.1 Analog-Tuned Capacitors

We will show examples of analog-tuned capacitors and summarize the findings of part of the vast amount of literature available on this topic using a chart.

Young & Boser reported an electrostatic-actuated analog-tuned capacitor with two parallel plates as shown in Figure 1.4 [9]. The actuation voltage was 5 V but a tuning range of only 16% was achieved. They later integrated the capacitor and an off-chip inductor and demonstrated a functional VCO with frequency tunable from 707 to 721 MHz [10]. Dec & Suyama reported a three-plate analog-tuned capacitor with 2-4 V actuation voltage and a tuning range of 1.87 [11]. The schematic of the capacitor is shown in

Figure 1.5. The VCO circuit built using this capacitor and a spiral inductor achieved a quality factor of about 20 at 1-2 GHz [12].

Figure 1.4. Parallel plate tunable capacitor by Young & Boser.

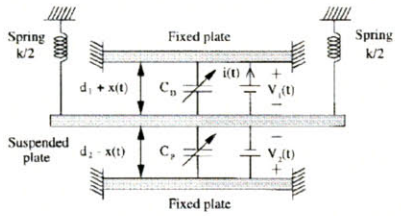


Figure 1.5. Three-plate tunable capacitor by Dec & Suyama.

Hung and Senturia conducted simulation and shape-optimization for an electrostatic zipping-actuated tunable capacitor [13]. A cantilever type zipper actuator is used and capacitance tuning is achieved in the zipping regime, as shown in Figure 1.6. By changing the shape of the bottom electrode, it is shown that optimized performance of the capacitance, such as linear C-V characteristics, or linear f-V characteristics, can be achieved. Hung reported an automated procedure for simulation, optimization and layout for the design of the bottom electrodes. The simulation was done using a finite-difference approximation. Using his method, the layouts for the bottom electrodes for three different optimization criteria are shown in Figure 1.7. The simulated performance is plotted in Figure 1.8.

A chart is used to summarize the published tuning capacitors as shown in Figure 1.9. The maximum and minimum capacitances for analog-tuning capacitors are plotted against maximum actuation voltage, comparing the different actuation method.

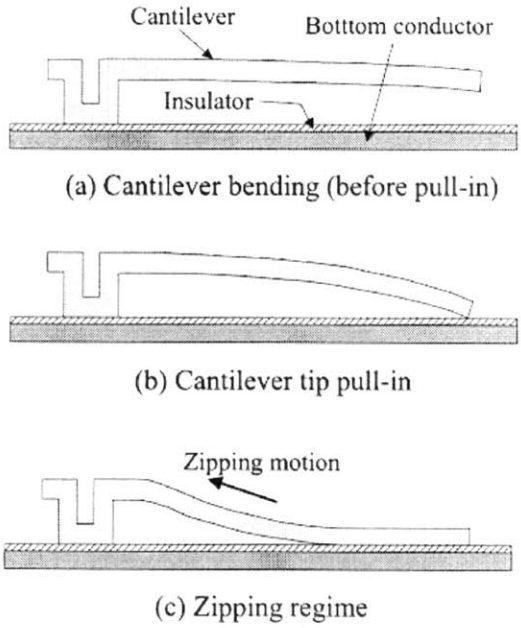


Figure 1.6. Zipper actuator operation with increasing voltage.

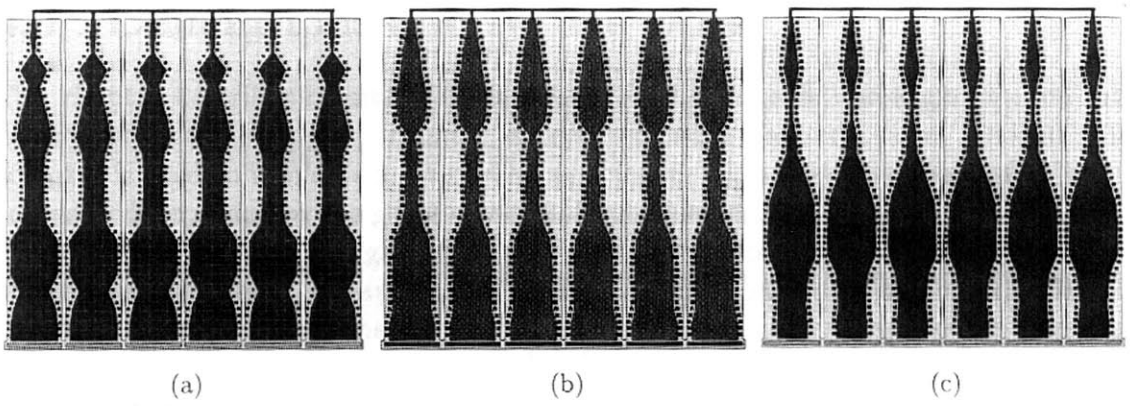
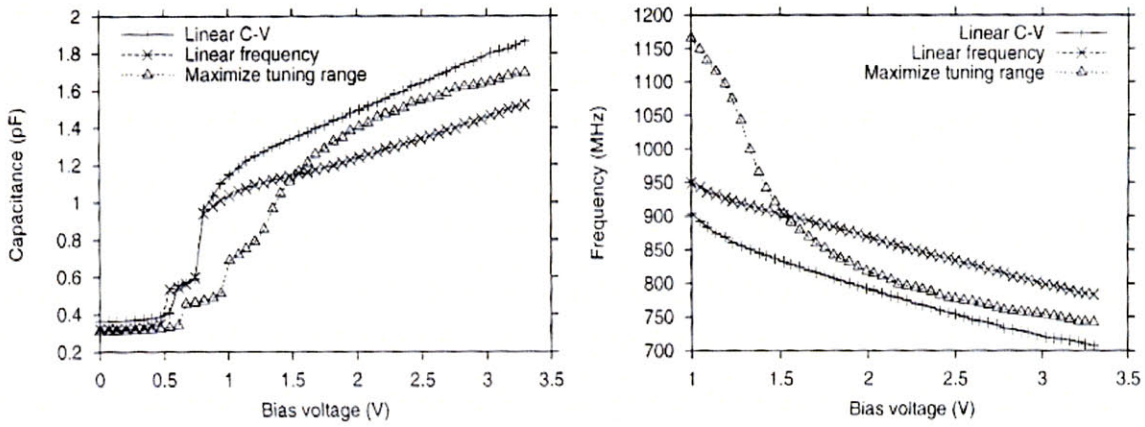


Figure 1.7. The shapes of the optimized bottom electrode for (a) linear C-V characteristics, (b) linear f-V, and (c) maximum tuning range.



(a) (b)

Figure 1.8. Simulation results of the tunable capacitor using the shapes in Figure 1.7, showing (a) C-V and (b) f-V characteristics.

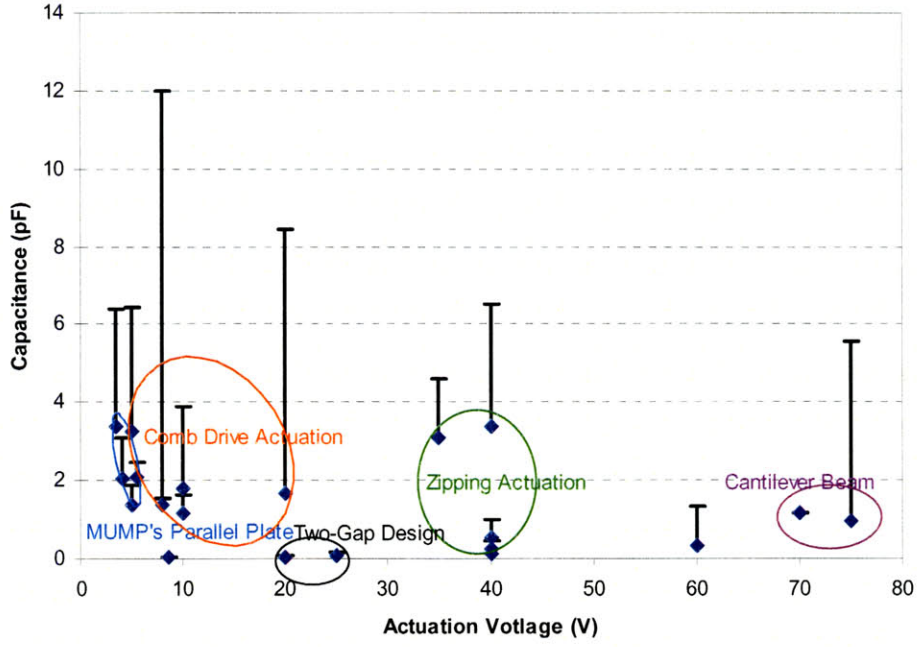


Figure 1.9. Summary of published analog-tuning capacitors [14]-[25].

1.4.2 Digital-Tuned Capacitors

We will also show examples of digital-tuned capacitors and compare them with the analog-tuned capacitors.

Goldsmith et al from Raytheon Systems Corporation reported an RF MEMS variable capacitor with a 22:1 tuning range with digital capacitance selection, using bistable MEMS membrane capacitors with individual tuning ranges of 70:1 to 100:1 [26]. A cross-section of the individual capacitor in both actuated and unactuated states is shown in Figure 1.10. The substrate is high resistivity silicon substrates (>10 kΩ cm) to reduce parasitic loss. The buffer layer is a 1 μm thick silicon oxide layer. The bottom electrode is a layer of refractory metal less than 0.5 μm thick to provide good conductivity as well as smooth contact surface. The interconnects are 4 μm thick aluminum and the membrane is a thin aluminum layer less than 0.5 μm thick for good conductivity and mechanical properties. A top view of the capacitor is shown in Figure 1.11. The capacitor has a ratio of on-state to off-state capacitance range from 70:1 to 100:1, a pull-in voltage range from 30 to 55 V, and a switch time range from 3 to 6 μs.

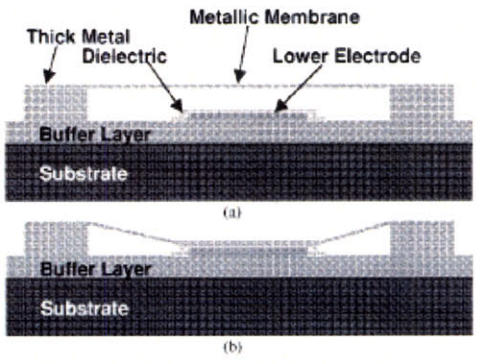


Figure 1.10. The Goldsmith bistable capacitor.

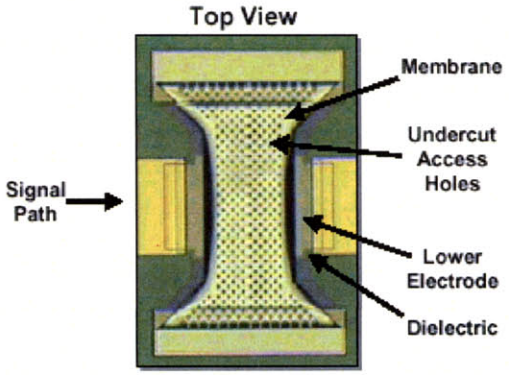


Figure 1.11. Top view of the fabricated capacitor.

A varactor is constructed using these switchable MEMS capacitors as the control element. The configuration for a 6-bit varactor is shown in Figure 1.12. Each bit contains one

or more MEMS capacitors in series with a fixed capacitor, which is used to yield the desired capacitance for each bit. In this example, the bits contain 16, 8, 4, 2, 1 and 0.5 pF of capacitances. Each capacitor is actuated by a control voltage, which is decoupled from the RF signal through a 5 kW thin-film resistor. The capacitance of the varactor ranges from 1.5 pF with none of the bits actuated to 33.2 pF with all of the bits actuated. And a linear capacitance response in between these two values is obtained. The quality factor of the varactor is less than 20 at 1 GHz. The same group later demonstrated a 4-bit capacitor for 6 pole tunable filter using the same technology [27]. Goldsmith's example showed one of the early efforts in achieving desired capacitance characteristics by optimizing the circuit design. However, a high actuation voltage and low quality factor were the limiting factors for wider applications of the bistable membrane capacitor.

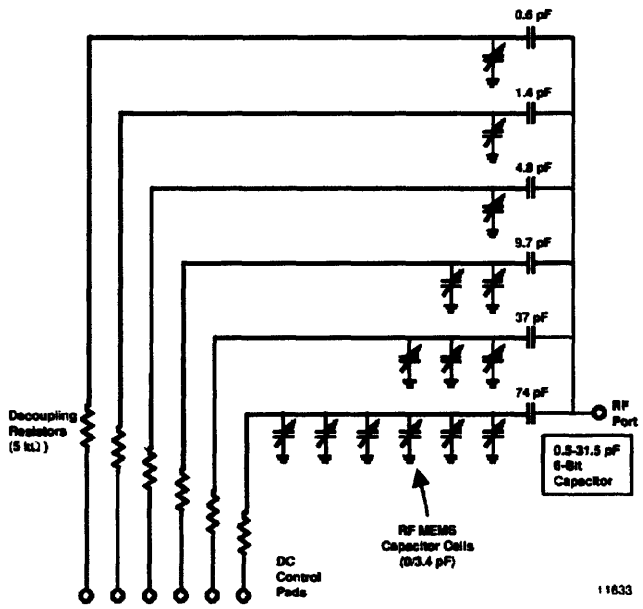


Figure 1.12. Configuration of the variable capacitor using individual MEMS capacitors.

Rizk and Rebeiz reported a digital type RF MEMS switched capacitor built in a CPW configuration [28]. A 2-bit capacitor array is constructed using the switched capacitors. In

this design, a MEMS shunt bridge is fabricated over an MIM capacitor that allows for high capacitance ratio and also ensures a fixed down-state capacitance. A cross section of the switched capacitor is shown in Figure 5. Here the substrate is a 400-μm thick high-resistivity silicon wafer (2-3 kΩ cm). The pull-down electrodes are 0.6 μm thick layer of Ti/ Au/Ti layers. The dielectric is 0.2 μm thick silicon nitride. The MEMS bridge is fabricated using a 0.8 μm thick sputtered layer of gold using PMMA as sacrificial layer. The center conductor, the ground planes and the anchors are electroplated with 2 μm of gold. A 2-bit digital capacitor array is constructed using 300 fF and 600 fF switched capacitors. An equivalent circuit model is shown in Figure 6. The array is suitable for a digital tunable matching network at 0.5-3 GHz.

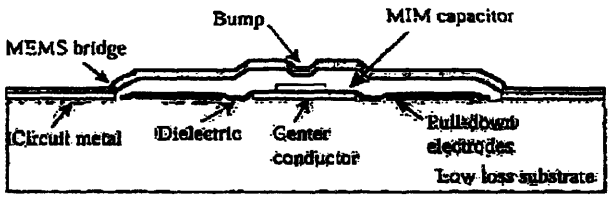


Figure 1.13. Cross section of the CPW shunt MEMS switched capacitor.

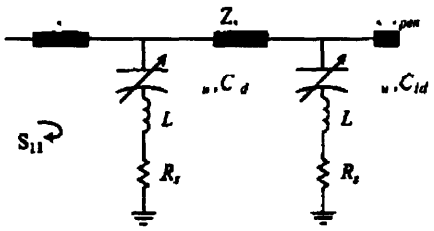


Figure 1.14. 2-bit circuit model.

Hoivik *et al.* reported a digitally controllable variable capacitor [29]. In this case, electrostatic actuation is used for analog tuning of the capacitor. Individual capacitor plates are connected to the bond pads using beam flexures of different widths as shown in Figure 1.15. As applied voltage is increasing, the top capacitor plates move towards the substrate in a cascading manner depending on the stiffness of the individual support beam. The device is fabricated using MUMPs technology. It includes three layers of polysilicon, two layers of oxide and one layer of gold. A plot of the capacitance ratio vs. voltage is shown in Figure 1.16.

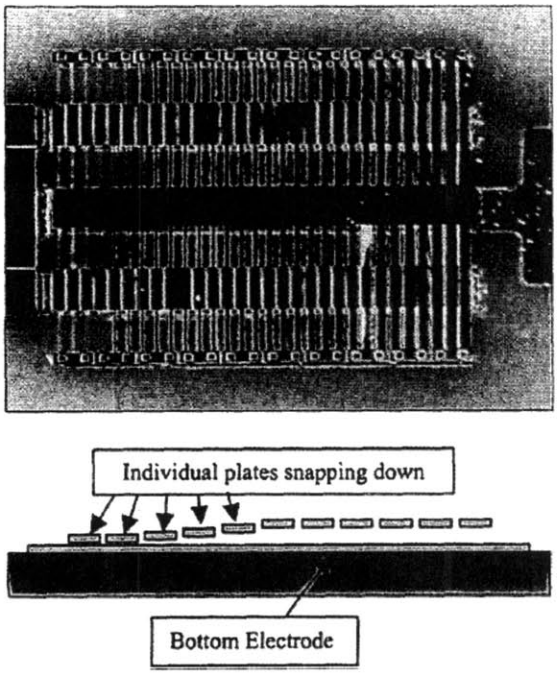


Figure 1.15. Top and cross-sectional view of the capacitor.

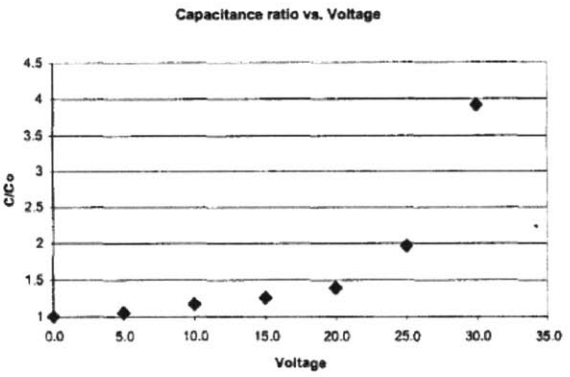


Figure 1.16. Capacitance ratio vs. Voltage.

In general, analog-tuned capacitors use lower actuation voltage and allow continuous frequency tuning; however, they possess lower tuning ranges than digital-tuned capacitors. On the other hand, digital-tuned capacitors have lower quality factors, and a lot of research effort will still be needed in achieving the desired frequency characteristics.

1.5 Integrated LC Resonator

Although a lot of work has been done to improve the performance of tunable capacitor with either analog- or digital-tuned functions, few paper reports on integrated LC resonator on a chip. This is because on-chip spiral type of inductors are often very lossy due to large resistance resulted from long spiral wires. Ketterl et al. reported a micromachined tunable CPW resonator which consists of a CPW spiral inductor with an electrostatic zip-

ping cantilever type tunable capacitor [30]. Frequency tuning between 3 and 7 GHz was achieved with 40 V actuation voltage. However, the quality factor was between 17 and 20. There is a demand for a high-Q, highly tunably LC tank, conceivably in the wireless communication applications.

Portable wireless communication transceivers today continue to rely on off-chip resonator components (e.g., Surface Acoustic Wave, or SAW, filters) for high frequency selectivity and low noise performance. However, these off-chip passive components often occupy substantial space and consume substantial power. In a RF front end receiver, for example, a voltage controlled oscillator (VCO) generates a design frequency that upon mixing with the pre-filtered and amplified incoming radio signal, down converts the high frequency carrier signal to intermediate frequency (IF) before further signal processing. Currently, this is commonly done using off-chip LC tanks, and a charge-pump PLL (phase lock loop) implemented with an off-chip crystal frequency reference is needed in order to control the frequency and reduce phase noise. There could be substantial advantage in replacing the off-chip LC tank with IC-integrated on-chip LC tank in terms of space and power consumption. It is foreseeable that the RF transceiver architecture we use today will have to be re-designed to maximize the use of micromechanical circuits, e.g., MEMS varactors, switches and resonators, etc. [31]. A lot of research is also being done on micromechanical resonators, which possess exceptionally high Q and thermal stability, but often with very low tunability.

1.6 Summary

In this chapter, we have explained the enabling technologies for the concept of a tunable LC tank, which are the Nanogate structure and the zipping actuator developed in our group. The idea of the LC tank prompted separate studies on the single-turn inductor and

the tunable capacitor with integrated actuator. This thesis presents the study on the tunable capacitor. The chapter also provides an overview for the application of tunable capacitors and compares the many reported tunable capacitors in the literature, which can be grouped into several actuation methods in general. Our design of the tunable capacitor takes a rather different approach compared to the literature, because it is designed to be an integrated part of a cavity resonator. Lastly, we show that there is potential application for an integrated LC tank in the future wireless transceiver design.

1.7 Thesis Organization

We will start the thesis work by a chapter on design and fabrication. This is not because they proceed modeling, rather, the design, fabrication and modeling processes for a MEMS device are often entangled and there is no exception here. However, in particular to this thesis work, the reader should keep in mind that it is initially enabled by known technologies or designs, although it is driven by applications as well. Therefore, an introduction to the design and fabrication of the device will give a good overview on why the specific design is chosen and why we think we can make it. Having such knowledge would be essential to the understanding of the modeling and simulation, which is introduced the next. We will then present the testing of the device and compare the test results with the simulation results. The goal is to understand the function of the designed tunable capacitor, and from there, propose improved design schemes for an integrated cavity resonator, which will be described in the last chapter.

Chapter 2

Design and Fabrication

We have mentioned about the design concept of the tunable capacitor in the previous chapter. In this chapter, we will put the concept into a solid design and describe the micro-fabrication process that supports the design. The actual fabrication process, like with any other MEMS device, is an iteration process where both design and fabrication have to compromise until they find an agreement. We will present the fabrication results and describe some important fabrication issues and how they are resolved. The assembly and packaging methods will be presented last.

2.1 Design

Based on the ideas of the Nanogate and the zipping actuator described in the previous chapter, a design of the electrostatically actuated tunable capacitor is devised. A cross-sectional schematic of the original design is illustrated in Figure 2.1. A 3-D bisected schematic of the device is shown in Figure 2.2. We will first briefly describe the structure of the device as well as its functions by referring to these two schematics.

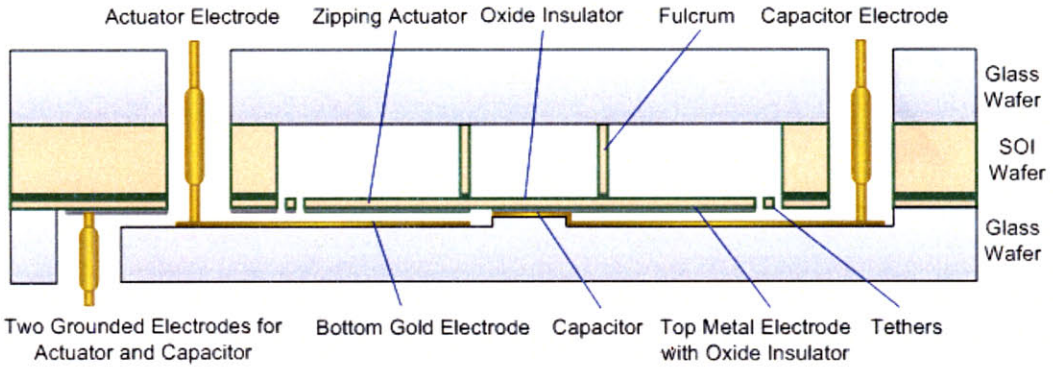


Figure 2.1. Cross-sectional schematic of the design of the tunable capacitor (dimensions not to scale).

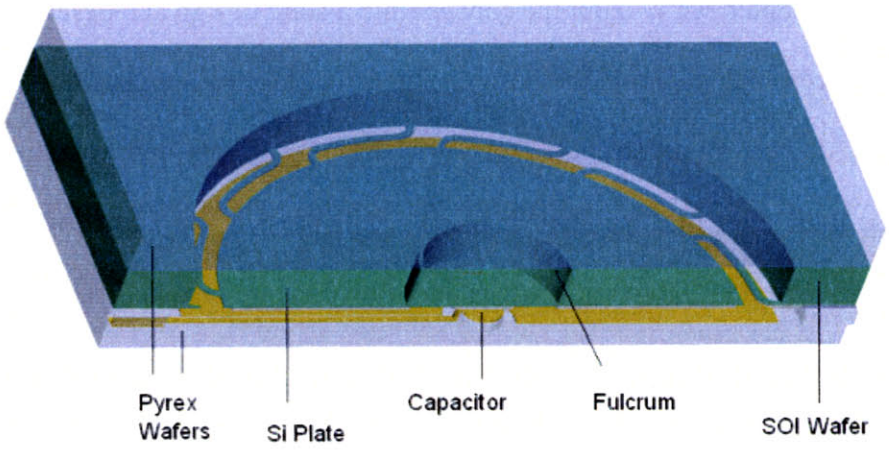


Figure 2.2. 3-D bisected view of the tunable capacitor (dimensions not to scale).

As shown in Figure 2.1, the device consists of three wafers: a SOI (Silicon-On-Insulator) wafer sandwiched by two glass wafers that are anodically bonded together. In the center of the device is a circular plate that is supported by tethers that are connected to the outer walls. A cylindrical fulcrum, to be fabricated by the deep reactive ion etching technique, acts as the pivot for the plate and divides the plate into the outer actuator region and the center capacitor region. The top of the fulcrum is bonded to the top glass wafer for structural rigidity. The SOI layer is used as the zipping actuator because of its uniform

thickness and the low stress of single-crystal silicon. Metal (aluminum) is deposited on the SOI layer facing the bottom glass wafer as electrodes for both actuator and capacitor. Silicon dioxide is used as dielectric material and it can be deposited on top of the metal by chemical vapor deposition. The bottom wafer contains the bottom electrodes for the actuator and the capacitor. The actuator electrode is etched into the glass to form the gap of the actuator. Gold is deposited on top of the etched pit as actuator and capacitor electrodes. Voltage is applied between the top and the bottom actuator electrodes. At a certain voltage threshold, the outer plate snaps down. With increasing actuation voltages, the plate zips along the radial direction and results in the separation of the two capacitor surfaces. It is known that gold adheres to oxide poorly, making it necessary to use an adhesion layer such as chromium when depositing gold onto silicon or oxide surface [32]. With such property, the plate does not bond to the gold surface although the two surfaces are in close contact during operation. Thus the design makes it possible to have two initially closely-contacted surfaces that can be pried apart. By changing the gap between the two plates of the capacitor, the capacitance can be tuned.

The actual fabricated device, however, is a simpler version that is without the top metal electrode due to facilities and cost constraints, which will be explained in the next section.

2.2 Fabrication Process

The device uses 2 glass wafers and 1 silicon wafer that are anodically bonded together. The top and bottom wafers are 500-μm thick Pyrex® Borosilicate 7740 wafers from Corning Inc. The middle wafer is a SOI wafer that has 340 μm thick handle, 1.5 μm thick buried oxide and 10 or 20 μm thick SOI layer. Both the handle and SOI are Boron doped with a resistivity of 5-18 mΩ cm.

A total of 7 chrome masks were used for the fabrication of the device although 9 were designed. The wafer layout and all the masks used are shown in Appendix A, which also includes a list of the dimensions and different designs used in the layout. A detailed fabrication log can be found in Appendix B. Fabrication steps for the three wafers are listed below, and fabrication results will be presented in the next section.

2.2.1 Top Wafer

The top glass wafer contains access holes for the electrodes that are 3.25 mm in diameter. The holes are drilled by Bullen Ultrasonics Inc., which creates cutting tools for the holes and uses ultrasonically-induced vibrations delivered to the tool to achieve microscopic grinding [33]. The process schematic is shown in Figure 2.3.

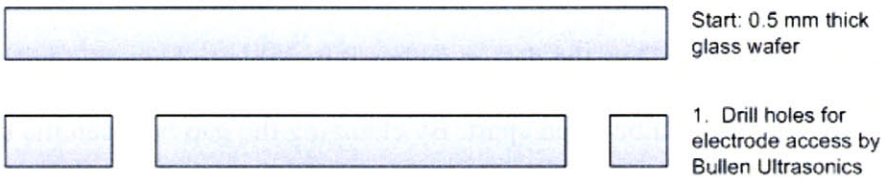


Figure 2.3. Process schematic for the top wafer.

2.2.2 Device Wafer

The middle wafer contains the structural plate that acts as the zipping actuator and the fulcrum that acts as the torsional spring. We will show the fabrication plan for the original design with metal. The schematic of the original fabrication process is shown in Figure 2.4, with fabrication steps followed.

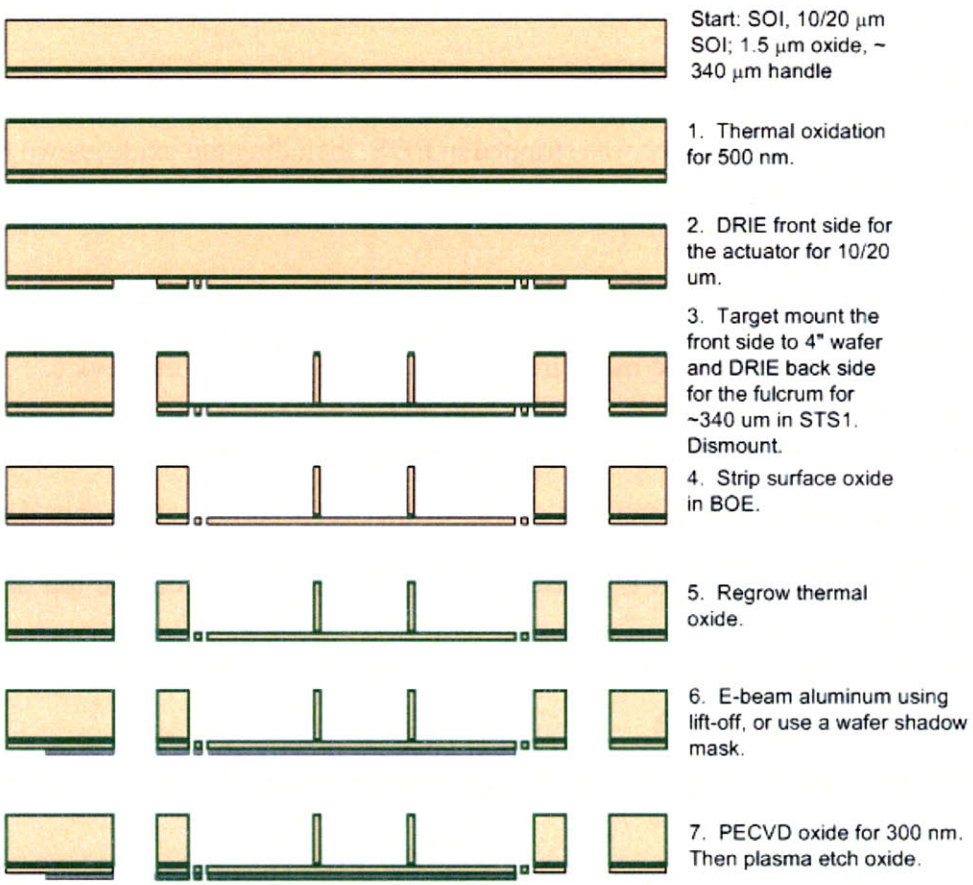


Figure 2.4. Schematic of the fabrication steps for middle wafer.

1. Oxide was thermally grown under wet conditions at 1100 °C for 0.5 μm. This oxide layer was used as a hard mask to protect the silicon surface for later anodic bonding after a deep reactive ion etch. After oxide growth, alignment marks were etched on the bottom side with mask 1: ALIGN, and the top side was etched with mask 2: STREETS, which partitioned the devices for die sawing. Both sides had alignment marks for aligning the wafers when bonding to the top and bottom glass wafers.

2. Deep reactive ion etch was used to etch the SOI layer to define the plate and tethers. The mask used was mask 3: ACTUATOR_TOP.

3. The wafer was mounted to 4" quartz wafer and deep reactive ion etch was used to etch the fulcrum. The wafers were dismounted in oxygen plasma and then cleaned in piranha solution. Mask 4: FULCRUM.

4. All oxide on the surface was stripped in BOE, including the oxide grown in step 1 as well as the exposed buried oxide.

5. Then thermal oxide was grown again, covering the whole wafer for about 0.3 μm. This oxide layer insulates the metal from the rest of the silicon in the device.

6. To deposit aluminum on the top surface, lift-off using photoresist can be one option, which involves spraying photoresist on top of the wafer surface since spin deposition is not possible. Another option is to use a wafer shadow mask placed on top of the wafer using drops of photoresist as adhesive. Then e-beam evaporation is used to deposit aluminum. Mask 5: METAL_TOP.

7. PECVD oxide for 300 nm then etch oxide in plasma. Mask 6: OXIDE.

The actual fabrication process omitted steps 6 and 7 because of practical reasons that will be explained in the section followed.

2.2.3 Bottom Wafer

Fabrication of the bottom wafer is shown in Figure 2.5. Two batches of the bottom wafer were fabricated; one with the center capacitor etched for 1 μm, and the other without the initial etch. The rest of the process was the same for the two batches and the general fabrication steps are as follow.

1. For one batch, a 1-μm deep circular pit was first etched in BOE to define the height of the capacitor plate as in step 1a) in the figure. Mask 7: CAPACITOR_SEAT was used. For another batch, step 1a) was omitted. For both batches, a 10 μm pit was etched to define the gap of the actuator using mask 8: ACTUATOR_BOTTOM.

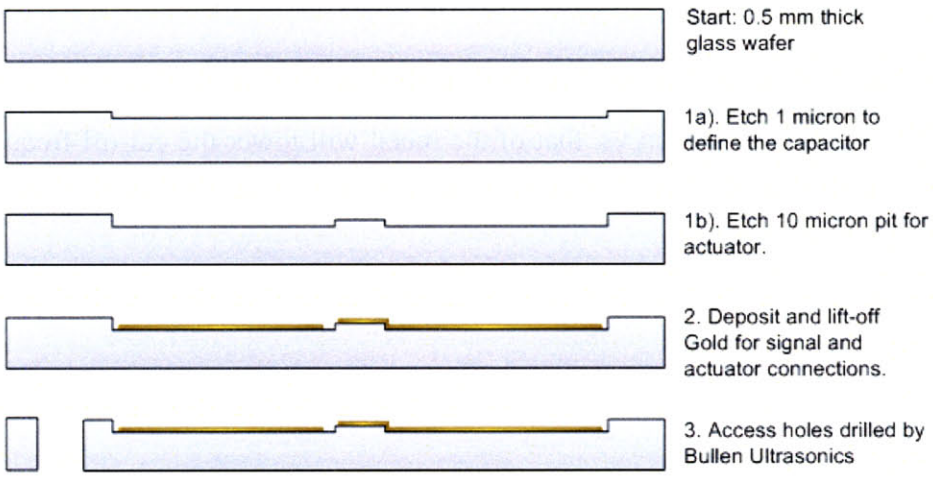


Figure 2.5. Schematic of the fabrication steps for the bottom wafer.

2. Gold was deposited using physical evaporation and then lift-off was used to define the actuator and capacitor electrodes. Mask 9: METAL_BOTTOM.

3. The wafers were then sent out to Bullen Ultrasonics Inc. for drilling the holes for electrical connection.

2.3 Fabrication Results

In this section, we will elaborate on the main challenges in our fabrication process and the approaches employed in our attempts in resolving them.

2.3.1 Aluminum Deposition

Our original plan was to deposit metal such as aluminum on top of the silicon plate as the electrodes. However, because of our initial decision to use 4" wafers, the transition to 6" wafers in the MTL facility left some of the CVD and plasma etch tools unavailable to 4" wafers at the time of fabrication. Blanket deposition of a dielectric layer such as oxide or nitride on the metal with good uniformity and coverage was not achievable after a series of experiments with an old PECVD machine. Because of time and cost constraints, the

fabrication was modified such that there would be no metal deposition for the silicon plate. Instead, the single-crystal silicon layer would be used as the actuator and sensing capacitor, meaning that the two electrodes will be electrically connected to ground. The high resistivity of the silicon vs. that of the metal will lower the cut-off frequency of the capacitor device and affect the electrical tests. However, the simplification of the fabrication compared to that of metal is a plus. Furthermore, it will still allow us to verify the zipping actuator concept.

2.3.2 Fulcrum Etch

The fulcrum is designed to be a cylindrical column that is 35 or 50-μm wide and about 340-μm deep. Etching of the fulcrum was done using an STS machine available in our microfab facility, which utilizes the time-multiplexed deep etching technique developed by Robert Bosch GmbH. One commonly encountered problem using the deep reactive ion etching technique arises when a nonconducting material is used as an etch stop. This is due to the depleted charging of electrons at the bottom of the trench, causing distortion of ion trajectories such that etching proceeds along the interface, resulting in what is known as "footing effect" [34]. Footing is more prominent when etching a wide trench with high aspect ratio. In our case, we used a buried oxide layer as the etch stop, and since we intended to etch a column instead of a trench, footing could be more severe due to the openly exposed area to a larger pool of depleted ions. When designing the masks for the device, the width of the fulcrum is chosen to be more generous then desired from the design, because of the consideration of surviving the etch. We conducted an experiment to find out the effect of overetch on footing. In the experiment, we compared the profiles of the fulcrum without overetch and with some overetch.

To prepare for the experiment, a 4" wafer with thermal oxide grown on both sides was patterned with fulcrums and then mounted to a 6" quartz wafer for etching in a STS machine. The recipe used to etch the fulcrum has the following parameters. The APC angle is fixed at 75%. During the etching cycle, the SF_6 flow rate is 140 sccm for 14 sec, with 12 W electrode power and 600 W coil power. During the passivation cycle, the C_4F_8 flow rate is 95 sccm for 11 sec, with 0 W electrode power and 600 W coil power. This recipe was chosen because it etched more uniformly across the wafer and also it did not produce black silicon etching surfaces like other recipes that were tried. Then care was taken to observe the etching as it approached the end. And one could see, through the quartz window in the machine, the grey-colored silicon front that was receding, exposing the bluish oxide surface, much the same way as ocean waves gently wash up on sand beach. As soon as the oxide around the fulcrum appeared across the pit, etch was stopped. Photoresist would be applied to cover the fulcrum to prevent it from overetch. Then the wafer would be baked to cure the resist and placed again into the chamber, and this time, we observed another device on the wafer. We timed the minutes of overetch by starting to count the time as soon as the oxide became all visible around the fulcrum. After etching was finished, the wafer was dismounted in acetone and cleaned in piranha solution. It was then further cleaned and anodically bonded to a pristine top glass wafer and then epoxy glued to a bottom silicon wafer for diesawing. The fulcrum was diced across and the SEM micrographs were obtained as shown in Figure 2.6. Because of the coarse blade used in diesaw for the glass wafer, the edges of the cut appear to be chipped. The figures show the cross section of one fulcrum that was without overetch and one that was overetched by 8.5 minutes. It is seen that even though we took out the wafer as soon as all the oxide appeared in the pit, some undercut was still present. And after 8.5 minutes of overetch, the bottom of the fulcrum was severely overetched. And if the fulcrum was left to etch for few more

minutes, the fulcrum would be etched away and landed somewhere else on the wafer. Because of etch non-uniformity in the STS machine, intolerance to overetch was a serious challenge for the device fabrication process.

a) b)

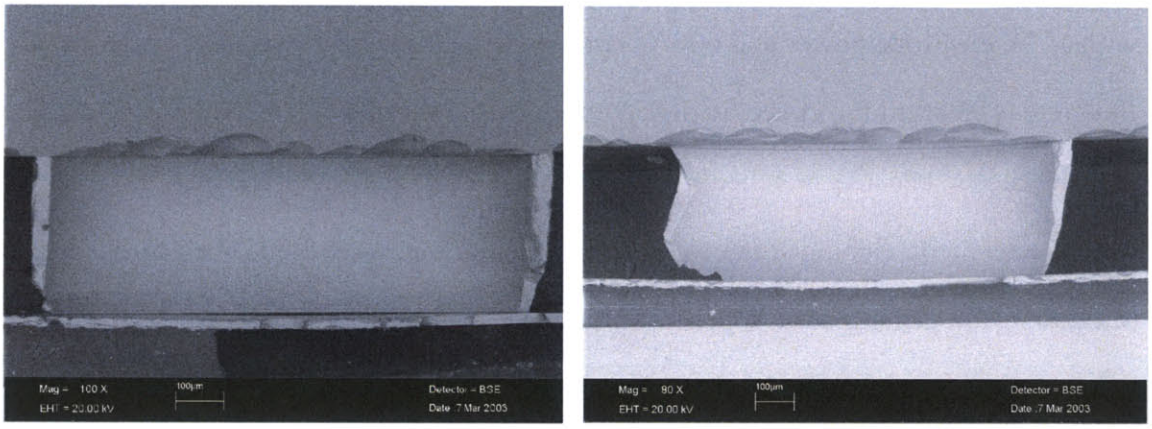


Figure 2.6. Cross-sections of the fulcrum showing the etch profiles for a), without overetch, and b), with 8.5 minutes of overetch.

To attempt to solve the footing problem due to overetch, 15-µm thick guard rings were used to serve as sacrificial etching materials surrounding the fulcrum from both the inner and outer circles. A top view of the fulcrum and the surrounding guards rings are shown in the schematic of Figure 2.7. The results are presented in Figure 2.8. When there is no overetch, the guard rings are present as shown in a). For 4 to 8.5 minutes of overetch, the guards rings are etched away, leaving straight sidewalls for the fulcrum as shown in b) and c). And for 28.5 minutes of overetch, footing effect causes the bottom of the fulcrum to thin down as shown in d). Results with the guard rings suggested that such method was more tolerant to overetch and hence was more advantageous to the fabrication process. Guard rings were used in the mask layout of the middle wafer for part of the devices. However, despite the use of guard rings, careful observation of the etch as well as timing were still necessary in order to produce good results. And when a fulcrum was finished etching, photoresist patching was necessary to prevent further overetch. One thing that the

author found out about etching using a STS machine was that the wafer bow could play a role in the etching result. Because the wafers used had larger wafer bows (on the order of 80 μm higher at apex than edge) than expected, it failed to match with the bowed chuck of the STS machine after being clamped down and resulted in poor cooling for the wafer and hence overetch was a more severe problem. After switching to another STS machine that did not have a bowed chuck, it was found that overetch was much more tolerated. The moral is that there are many factors affecting the etching results. While the guard rings might be used to solve the problem with one machine, their use was less critical for another machine. However, they are recommended to make the deep etching of a high-aspect-ratio column a more robust process.

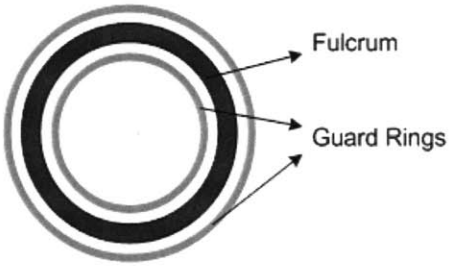


Figure 2.7. Top view of fulcrum and surrounding guard rings in the mask layout (not to scale).

2.3.3 Plate and Tethers

The thin silicon plate was supported by 8 slim tethers and must survive the cleaning and drying processes. Mechanical resonant frequencies of the fulcrum, membrane and tether structure were obtained using the model analysis from ProMechanica. In the analysis, a fulcrum diameter of 500 μm and membrane diameter of 2 mm are used. It was shown that the fundamental mode of vibration is 1.82 KHz, and the second mode is 2.93 KHz. The resonant modes are shown in Figure 2.9.

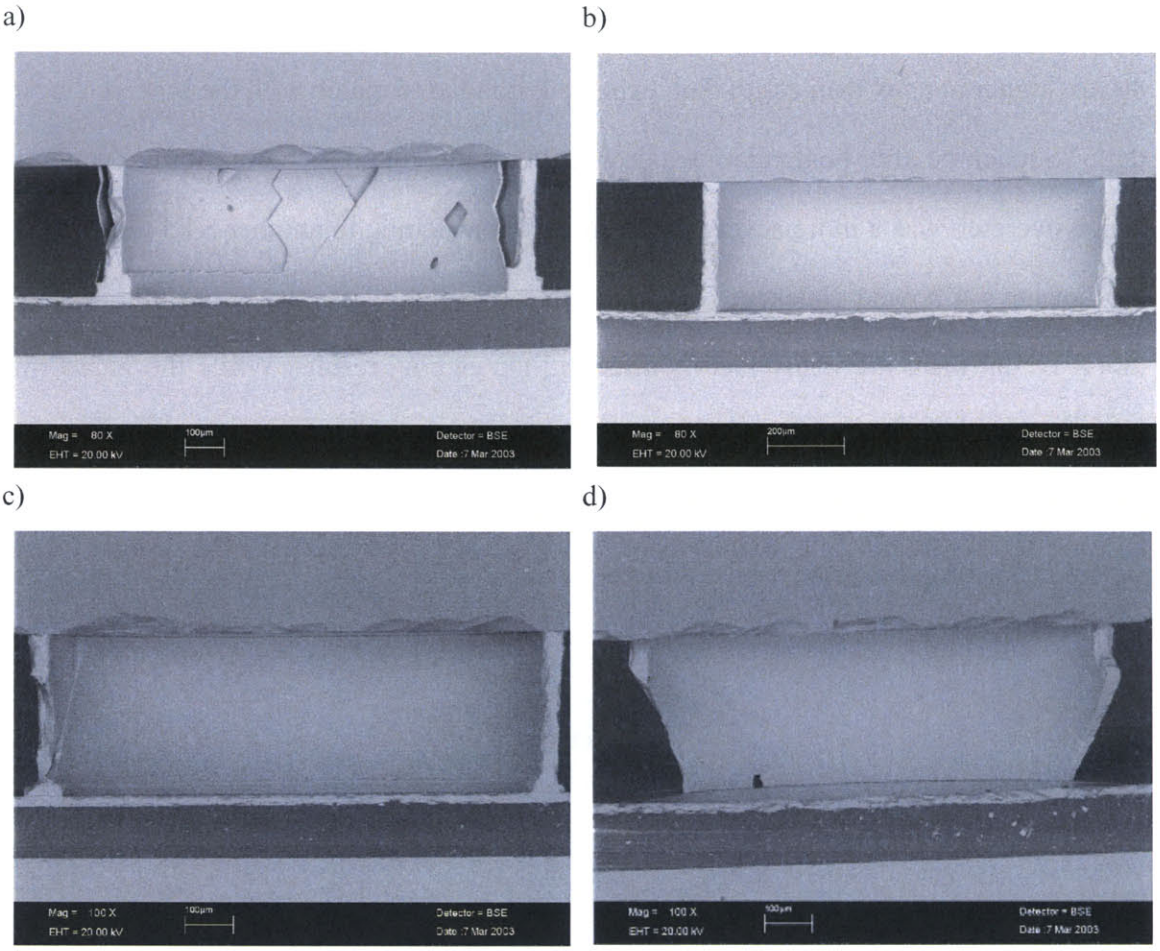


Figure 2.8. Cross-sections of the fulcrum with guard rings showing the etch profiles for (a), without overetch, (b), with 4 min. overetch, (c), with 8.5 min. overetch, and (d) with 28.5 min. overetch.

This is not a very stiff device and care was taken during fabrication to ensure its survival. For example, after the plate was fabricated, it was cleaned in diluted Piranha instead of the regular Piranha or RCA cleaning procedures. During drying in the spin dryer, pristine wafers were placed beside each devices in order to prevent the nitrogen from blowing on the devices directly. With these precaution, the plate and tether structure survived the cleaning and drying fabrication process.

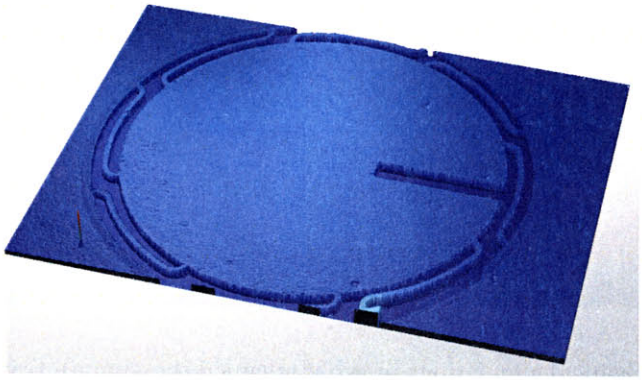
a) b)

Figure 2.9. Mechanical simulations in ProMechanica showing a), first resonant mode and b), second resonant mode of the fulcrum, membrane and tether structure.

2.3.4 Plate Bow

After the device wafer was fabricated, the bow of the silicon plate was examined. Single crystal silicon has very low residual stress, so it was expected that the plate should be relatively flat. However, because of thermal oxidation in the last step of the process, unevenly grown oxide on both sides might cause uneven stress distribution. Furthermore, because the glass wafer has a total thickness variation of 20 μm [35], after the device was bonded to the top glass wafer, the anchoring of the fulcrum might also change the shape of the plate. We measure the surface profiles of the silicon plate with a *Wyko* white light optical surface profilometer. For our measurement, the vertical-scanning interferometry mode was used, which could measure surfaces with large change in height because the objective, controlled by a piezoelectric transducer, actually moves during measurement to focus on the different heights. Figure 2.10 shows the surface profile of the plate for a device that had the fulcrum detached after being overetched, showing that the bow of the plate was about 0.5 μm high. Figure 2.11 shows a device with the fulcrum bonded to the top glass wafer. Clearly, the bonded fulcrum imposed constraints to the fulcrum area in the plate, causing the plate to deform in a bifurcation shape.

a)



b)

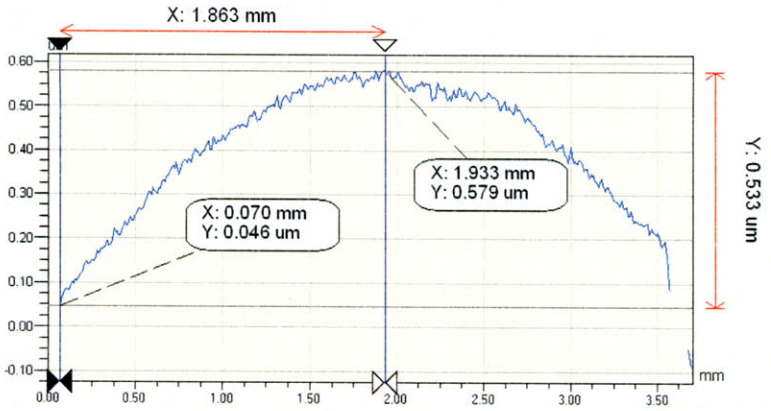
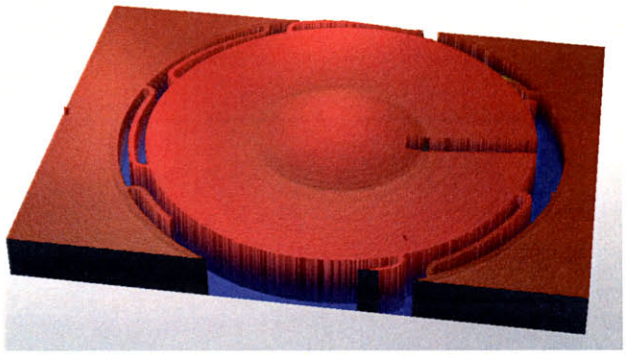


Figure 2.10. a) 3-D images and b) a cross section of the silicon plate without fulcrum.

The device shown in Figure 2.11 has a fulcrum radius of 750 μm. Other devices on the same wafer have a fulcrum radius of 500 μm. For these devices, the center plate is completely enclosed by the fulcrum. During anodic bonding, temperature rose and bonding was accomplished in high temperature, and hence hot air was trapped inside the enclosed cavity bounded by the center plate, the fulcrum and the top glass wafer. As the air was cooled down, the pressure difference bent the center plate toward the top glass wafer, as shown in Figure 2.12. This shows that a fully enclosed space should not be used when anodic bonding is used. A pressure relief cut should be made.

a)



b)

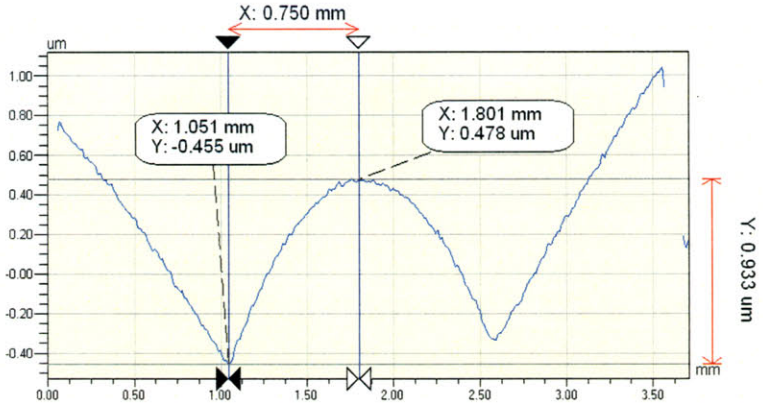


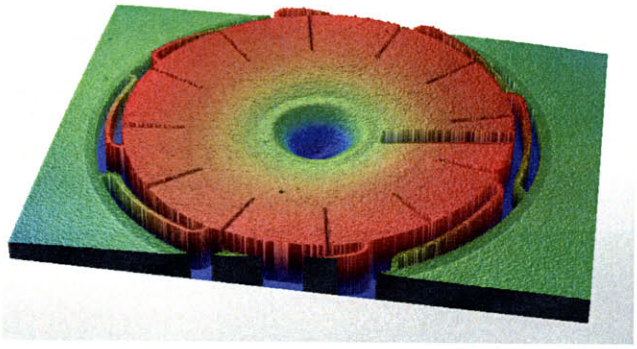
Figure 2.11. a) 3-D images and b) a cross section of the silicon plate after bonded fulcrum to top glass wafer.

2.3.5 Bottom Metal

For fabrication of the bottom wafer, physical evaporation with an electron beam was used to deposit gold on the surface and lift-off was used to pattern both the actuator and sensing capacitor electrodes. Because the center capacitor protruded above the etched pit by about 10 um, one challenge was to ensure that the gold layer covers the step height. After fabrication, a photo taken from a microscope is compared with a micrograph taken by SEM as shown in Figure 2.13. The photos show that although from the microscope, the

interconnect did not appear to be continuous along the step, it was actually continuous as shown from the SEM graph as well as from electrical tests.

a)



b)

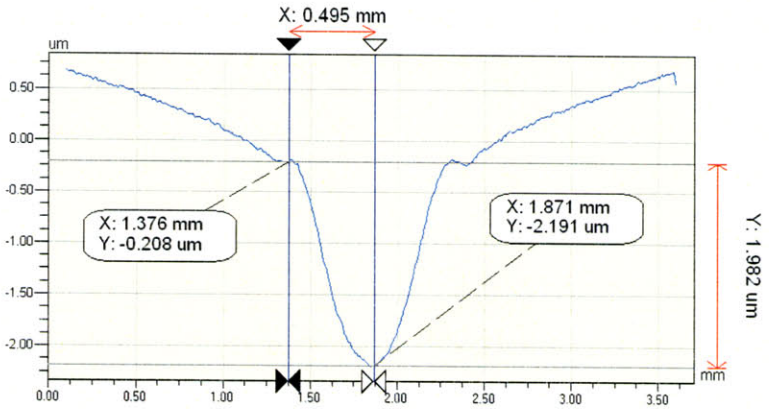


Figure 2.12. a) 3-D images and b) a cross section of the silicon plate with enclosed fulcrum after bonded fulcrum to top glass wafer.

2.3.6 Summary of Fabrication Results

We have explained various fabrication related issues pertinent to our original design. Some of the problems were foreseen before fabrication and were better controlled, some of the problems were discovered during fabrication and others were only learned after fabrication was accomplished. Through trial and error, a first generation of the tunable capacitor was fabricated. It was not an exact version of the original design in terms that 1) there

would be no metal on the silicon plate and hence the plate itself will be used as an electrode and 2) because of the enclosed cavity, some of the plates were initially deflected after anodic bonding. Next we will present the assembly methods and explain further issues during assembly.

a) b)

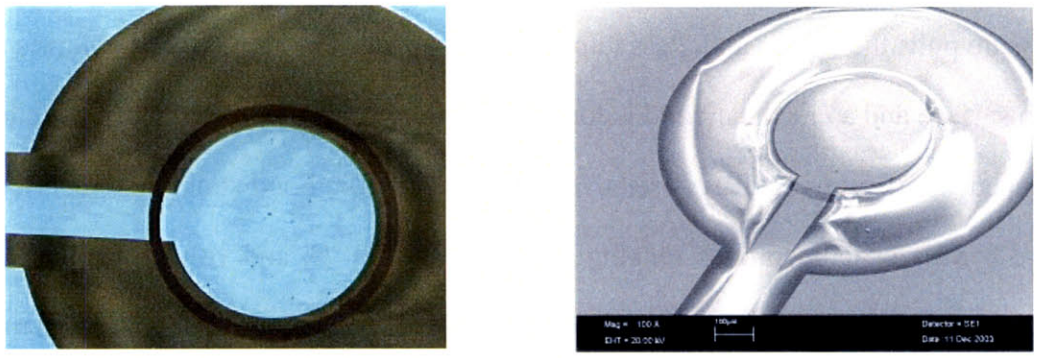


Figure 2.13. a) A top view of the center capacitor area taken from a microscope and b) a micrograph of the same device taken from SEM.

2.4 Anodic Bond and Wafer Assembly

After the three wafers were fabricated, anodic bonding was used to bond the wafers together. Two methods of assembling the wafers were used: wafer level and die level. We will explain the process for both methods, as well as the effect of anodic bond in both cases.

2.4.1 Anodic Bond With Oxide

In this section, we will examine the effect of intermediate layers between the glass wafer and the silicon wafer on the anodic bonding. A general description of how anodic bonding works can be found in [36]. In essence, the time needed to complete the anodic bond strongly depends on temperature and voltage applied. At elevated temperature, the sodium ions in the glass wafer become mobile. With a high potential applied to the silicon and a low potential applied uniformly to the glass side, the positively charged sodium ions will

move toward the low potential (or away from the silicon), resulting in a surge of current, which gradually drops down with time due to depletion of sodium ions. As the sodium ions migrate, a space charge layer of less mobile, negatively charged oxygen ions at the silicon/glass interface is formed. A large electric field hence exists between the positively charged silicon surface and the negatively charged space charge layer. The electrostatic pressure pulls the silicon and glass into intimate contact. The oxygen ions oxidizes the silicon surface and a chemical bond is formed. Bonding is accomplished when the current is dropped significantly and stays relatively unchanged. The bond strength is reported to be 0.9-3.8 MPa at temperatures ranging from 300 to 450 °C, and voltage applied ranging from 175-1050 V under atmospheric conditions [37]. At higher temperature, ion mobility increases, which in turn increases bonding current and bond strength. Higher voltage increases the electrostatic pressure and results in similar effects. Alternatively, external pressure could also be applied to bring the surfaces in close contact. With contact force of 200 N applied to 4 inch wafers, it is found that the bond strength could be greater than 10 MPa at temperatures higher than 200 °C at 600 V [38]. Hence, strength greater than the bulk glass (15 MPa) can be achieved. It is also found that increase of bonding time after an effective amount (about 10 minutes) does not further affect the bonding results. In fact, increase of bonding time could potentially cause dielectric breakdown of the bonding interface [36].

The presence of any dielectric layer, such as silicon dioxide or silicon nitride, between the silicon and glass wafers reduces the electrostatic pressure and slows down the bonding process. Lee et al. compared the effect of different intermediate layers as well as applied voltages and cleaning methods [39]. It was found that higher voltage reduces bonding time needed, and cleaning with piranha and HF results in better bonding performance than simply using acetone. With a 100 nm thick thermal oxide grown at 900 °C, the bonding time

needed at 300 °C and 500 V after piranha cleaning was 15 minutes. There was no mention of dielectric breakdown of oxide for the reported experiments.

The dielectric strength of thermally grown wet oxide is reported to be 3 MV/cm [36], and in general, about 3-5 MV/cm. For an oxide layer that is 0.27 μm thick, the breakdown voltage is around 80-135 V. As temperature increases, it is reported that the dielectric strength of the oxide decreases [40]. In his study to bond two silicon wafers with oxide as intermediate layers using anodic bonding, Anthony used voltage between 30-50 V at 850-950 °C to avoid oxide breakdown [40]. While in the case of having oxide between two silicon wafers, voltage drop is applied directly across the oxide layers, in the case of bonding silicon to glass, the situation is somewhat different. To predict the actual voltage drop across the dielectric layer during anodic bonding, we can model the bonding process with an equivalent circuit, modified from [41] to include the dielectric layer, as shown in Figure 2.14. In the figure, C_{ox} is the capacitance across the oxide, R_{ox} is the leakage current resistance. C_{scr} is the capacitance across the space charge layer and R_{scr} represents its leakage current. R_{glass} is the resistance across the glass wafer. According to the data from Corning Inc., the resistivity across a Pyrex® 7740 glass wafer at 250 °C is 6.1 Ωcm. We can estimate that R_{glass} is on the order of 0.8 Ω for the die-level bonded devices. As voltage is turned on, sodium ions migrate toward the cathode, and the sodium depletion layer thickness gradually increases. The growth of the depletion layer saturates due to decreasing electrical-field strength across the layer and the saturation-thickness increases at higher temperature, in the range of a few microns across [42]. Applying these observations to the circuit shown, we can deduce that the voltage across the capacitors increases as the current decreases exponentially and approaches the applied voltage level while the current drops significantly. At the beginning, most of the voltage drop is across the oxide layer as well as the air gap. At this stage, breakdown of the oxide layer could occur if the samples are

brought very close to each other to begin with, but since the current is usually limited by the power supply, damage to the oxide might not be apparent, especially because this might only last a very short amount of time. If the voltage applied is not high enough or the samples are not brought close enough, breakdown of the oxide might not occur. For example, if we neglect the depletion layer and assume that the air gap is on the order of 1 μm thick, then the ratio of voltage drop across the air gap over voltage drop across the oxide is 14.4:1, and hence the voltage drop across the oxide is relatively small compared to its breakdown voltage. As the thickness of the depletion layer increases, voltage across it also increases. The electric field pulls the glass and silicon surfaces close to each other and reduces the air gap. As a result, more voltage is distributed to the space charge layer and the voltage drop across the oxide might also increase. A thicker depletion layer will decrease the voltage drop across the oxide layer. Therefore, it is advantageous to perform anodic bonding at higher temperatures. In our case, if we assume a saturation-layer thickness of 2 μm thick, with the relative permittivity of glass being 4.6, for a voltage of 800 V, the steady-state voltage drop across the oxide layer is 110 V. This is the case when there is no current in the circuit. If the bonding pair is not left with the voltage on for a long time, the actual voltage across the oxide could be less and it is possible that oxide breakdown may not occur.

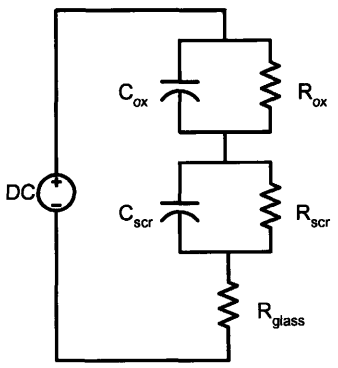


Figure 2.14. Circuit model of anodic bonding silicon to glass with oxide as intermediate layer.

2.4.2 Oxide As A Dielectric Layer For Touch Mode Operation

Since we have explained anodic bonding using oxide as an intermediate layer, we will also include here why we use oxide in the first place and what problems it might cause during operation.

When oxide is used as the dielectric for touch mode operation, ions or charges trapped inside the oxide could cause unpredictable function of the device. Cabuz compared the use of different dielectrics for touch mode operation of electrostatically actuator [43]. She experimented with thermal oxide, PECVD oxide, LPCVD nitride, sputtered SiN and PECVD SiN and measured the C-V curves of the dielectric layers. Among these dielectrics, it was found that only thermal oxide is free of signs of charge injection and retention. The study, however, didn't take into consideration environmental factors. We will examine the possible causes of trapped charges for the oxide. We will discuss three possible sources here: 1) sodium diffusion from anodic bond process, 2) charge injection if electric field is high enough and 3) parasitic charging at breakdown or static electrification. We will then discuss the effect of humidity.

Sodium Diffusion

It's known that amorphous silicon dioxide is prone to diffusion of impurities, especially alkali ions such as sodium [36]. On the other hand, silicon nitride is an excellent ionic barrier material and is often deposited on top of oxide to prevent ion diffusion. In our device, however, only thermally grown oxide is used as the dielectric. Although in most of the device areas, gold is deposited on top of the glass wafer, and hence sodium diffusion from glass to oxide could be eliminated, there are exposed areas where the oxide could touch down on the glass during anodic bond, and sodium contamination in these areas are possible.

A study on the contamination of silicon dioxide as a measure of feasibility of using anodic bond as the packaging method in monolithically integrated MEMS devices shows that sodium concentration on the gate oxide could increase by 3 fold after anodic bond, depending on where the MOS device is situated with respect to a glass cavity [44][45]. Charge concentration of the oxide as well as surface traps increase by a similar ratio. The minimum oxide charge was obtained by using a nitride-overcoat, or by placing the device far below from inside the glass cavity. However, there is no study on what happens to the oxide when it is used as the intermediate layer for an anodic bond. It can be expected that since oxide is in direct contact with the glass, sodium diffusion would be more efficient. Although the area of contamination in our case is very small compared to the area of the silicon plate, it can be expected that some contamination of the oxide with sodium took place during the bonding process.

Charge Injection

Charges can be injected into the dielectric when the electric field is sufficiently high, such as greater than 1 MV/cm [46]. If breakdown through the oxide does occur during the anodic bonding process, it is likely that boron ions from the silicon would inject into the oxide, causing more positively charged ions being trapped in the oxide.

Parasitic Charging

Parasitic charges can be trapped in the oxide layer during gas discharging at breakdown or simply static electrification [48], which could cause a certain amount of offset in the actuation voltage, depending on the density of the trapped charges. With breakdown, the offset can be a few hundred volts. It is shown that after breakdown occurs, positive charges trapped in silicon dioxide monolayers decay rapidly in the first 5 hours, up to 1% left after 3 days. Negative charges takes 10 days for the same drop. On the other hand, multilayer

dielectrics (with oxide and nitride) have a dramatically longer charge storage time.

Other sources of parasitic charging include contact electrification, which occur due to contact and separation of the electrodes during an operation cycle when the materials of the electrodes have different work function, such as in our case here.

Wu and Shannon model the static charges in the form of space charge layers of an electrostatic actuator with the configuration of metal/gap/dielectric/doped silicon [46]. It is found that the static charges within the dielectrics can be captured by a characteristic voltage, which is determined by the surface potential of the dielectrics and the doping concentration of the silicon. They further show that if the applied voltage is within an order of magnitude from this characteristic voltage, the actual electric field within the gap can differ dramatically with theory without considering the static charges. And depending on the parasitic charge density, the characteristic voltage can vary from very little to tens of volts.

Effect of Humidity

Humidity plays an important role in touch-mode electrostatic actuators and is often the culprit for stiction and failure. Cabuz showed that with DC driving method, humidity levels above 35% is detrimental [47]. With AC driving method, more humidity (55%) can be tolerated but electrostatic pressure is greatly reduced and hence it can not overcome the humidity effect.

2.4.3 Wafer-Level Assembly

For this assembly, a device wafer with 20 μm SOI was bonded to a bottom glass wafer with center capacitor area etched down for 1 μm. The device wafer was first aligned and anodically bonded to a top glass wafer, at 350 °C with 800 V in 6 minutes. This was done using an Electronic Visions EV620-501 Wafer Aligner and Bonder. Then the two-wafer stack was aligned to a bottom glass wafer. Metal tabs were inserted between the top stack

and the bottom wafer in order to separate them during alignment. During anodic bond, the to-be-bonded glass wafer was placed on top. The metal tabs were kept in place (instead of being removed in the normal process) and were conveniently used to provide ground potential for the silicon wafer. A graphite plate was placed on top of the glass wafer with a negative potential applied to it. The wafers were heated to 350 °C, 800 V was applied and bonding was accomplished in 8 minutes. The metal tabs were removed (either easily or forcefully by breaking a little chip off the glass wafer, depending on the strength of the bond surrounding them) after the bonding process. After the wafers were bonded and die-sawed, gold was evaporated onto the back side of the dies to provide electrical contact to the SOI plate.

After bonding, it was observed using a microscope that some parts of the silicon plate was stuck down on the glass surface. Apparently the silicon plate snapped down toward the bottom gold surface when voltage was applied during anodic bonding. Where the silicon plate and tethers touched the glass area, such as the outer edge or the tether areas, bonding occurred. As a result, for the wafer-level assembled devices, the plate would operate only in the zip-in region and would not experience pull in. A cross-section of the wafer-level bonded device when the outer edge is bonded is shown in Figure 2.15.

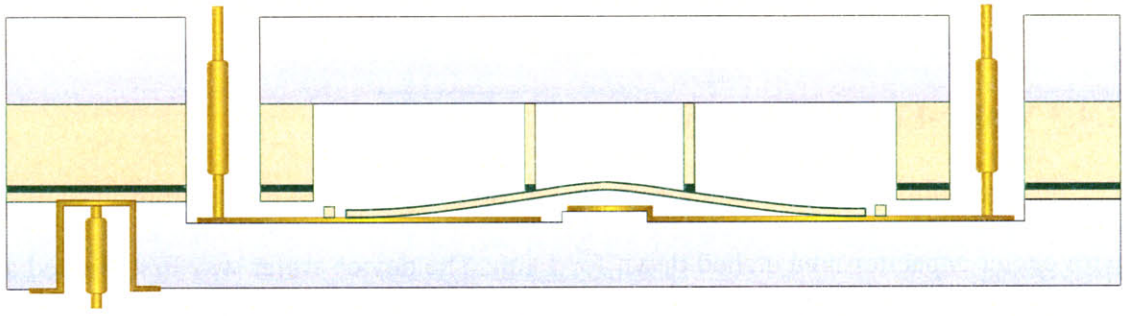
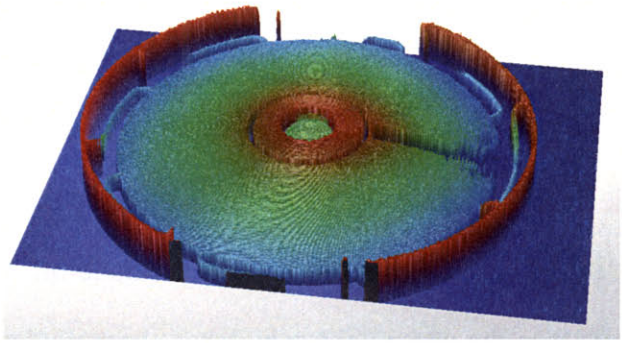


Figure 2.15. Cross-sectional schematic of the device after wafer-level bond.

The surface profiles of a wafer-level bonded devices is shown in Figure 2.16. Note that unlike the images in Figure 2.11, where the white light shined from the side of the plate without fulcrum, the images below were obtained where the light shined through the top glass glass. Because of the glass wafer, poor light reflectivity obscured the interference fringes. A red light filter (PSI Low Mag filter at 633 nm) was used to produce stronger fringes and hence legible surface scans. However, the trade-off by using the red light is that it is less accurate than the white light, which has shorter coherent length and is more suitable for the VSI mode. Note that in the surface profile images, there are two rings present on the plate. The bigger one corresponds to the fulcrum area, and the inner one is an artifact because the top glass wafer that the white light goes through has an etched pit in it. The artifact does not prevent us from measuring the center deflection of the plate. We can estimate the bow of the center plate by translating the center ring.

After the three wafers were anodically bonded together, the wafers were die sawed into 20.2×20.2 mm^2 dies, each of which contains 3 devices. In order to obtain a cross-section of the fulcrum-plate structure, one die was die-sawed across the middle of the plate, and the SEM micrographs were taken as shown in Figure 2.17. We can clearly see that in the actuator area, the membrane was elevated above the gold surface, proving that the silicon plate did not stick to the bottom surface that was covered with gold as expected. It also suggested that bonding of the tethers and outer edge of the plate should not affect the functionality of the device.



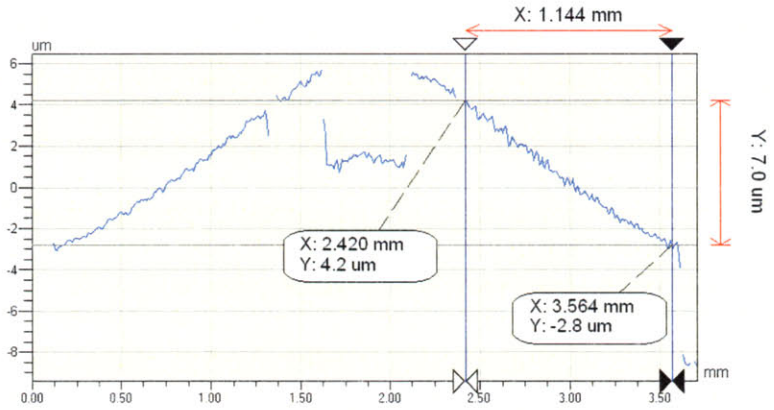


Figure 2.16. Surface profiles and cross-sections for a wafer-level bonded device.

a) b)

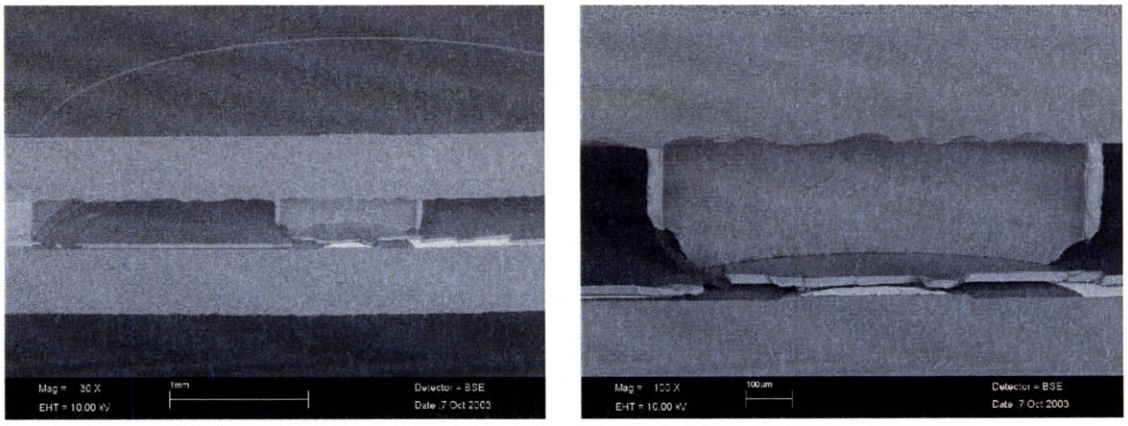


Figure 2.17. Cross-sections of the tunable capacitor as fabricated showing a), the device area and b) the fulcrum area.

2.4.4 Die-Level Bonded Device

In order to prevent the plate from sticking down on the gold electrode during anodic bonding, die-level anodic bonding with extra wiring to the actuator electrode was used. For this assembly, a device wafer with 10 μm SOI and a bottom wafer without the center capacitor being etched were used. As before, the silicon wafer was first anodically bonded to a top glass wafer, and then both the bonded stack and a bottom glass wafer were die-sawed separately. The two dies were then cleaned firstly in alcohols and in Nanostrip for an hour, and finally rinsed in DI water and dried in an oven at 120 °C. The die-level bonding setup is shown in the photo in Figure 2.18. The bonded stack was first placed on top of a graphite plate, which as connected to the chuck electrically as ground. The top die was then aligned to the bottom stack using two ceramic blocks. Because alignment relies on two die-saw edges, we could expect a large alignment error (on the other of 100 μm) for this device. Electrical connection to the SOI plate was achieved from the side of the die, where silver paste was applied to ensure electrical connection. Wires were used to apply same positive voltage to the side of the die as well as the gold electrodes from the top. They remained in contact with the die during bonding by spring force. For the device shown in the photo, we only used one die out of the three, but potentially we can apply same voltage to other dies as well. The chuck would then be placed in an oven and heated to 300 °C and 600 V was applied. Bonding was accomplished between 4-5 minutes and the bonding yield was usually very good.

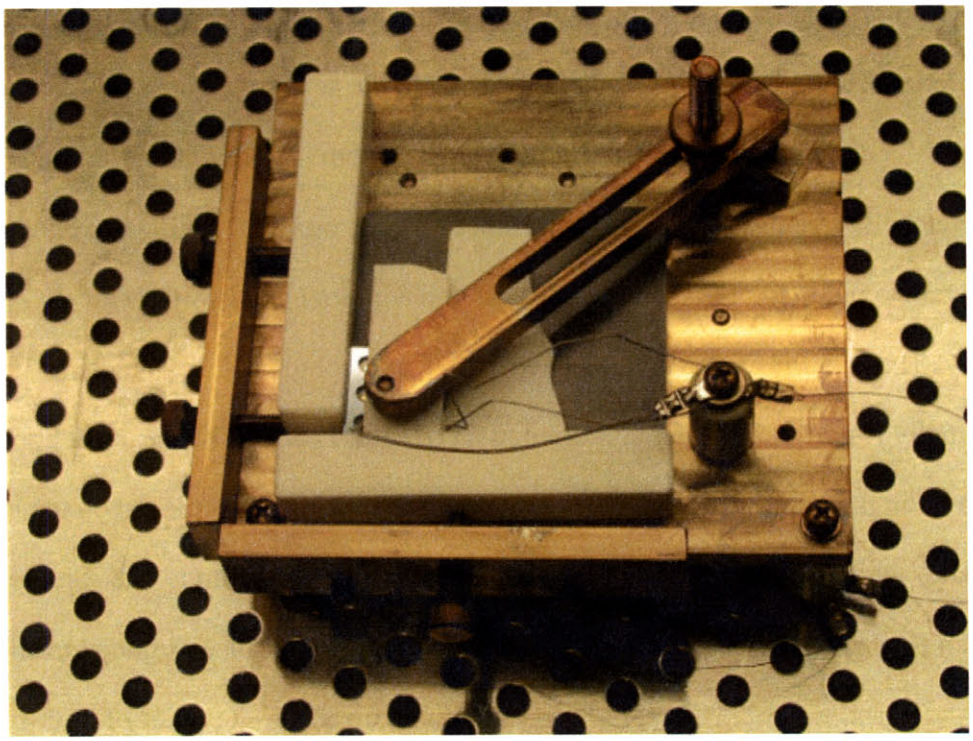


Figure 2.18. Die-level anodic bond setup.

It was found that even though the two electrodes were applied with the same potential, the problem was not entirely solved. If the tethers were hanging on top of the glass area, they would still be pulled down during anodic bonding, causing the outer part of the plate to be stuck to the bottom electrode. The solution to this would be to cover gold on the bottom glass everywhere below the plate and the tethers. However, given the design we had, this was not fully achievable. The surface profile of a die-level bonded device is shown in Figure 2.19. Note that the plate is rather flat in most area except at a corner, where it seems that the tethers are stuck down because the bottom area has glass exposed due to poor alignment.

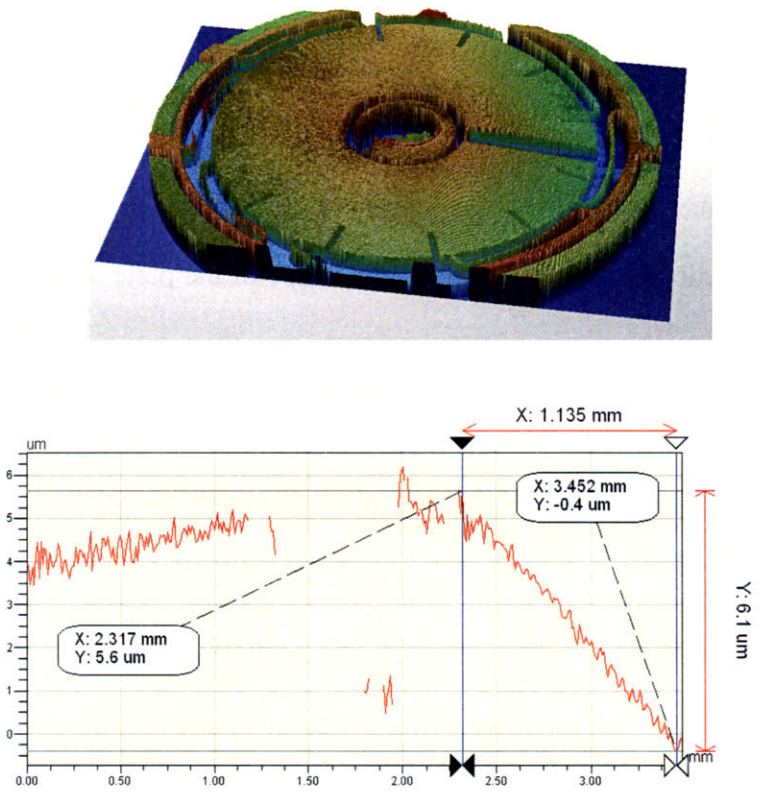


Figure 2.19. Surface profiles of the plate after die-level bond.

In future devices where it is desired that the two electrodes remain intact during anodic bonding on the wafer-level, we can use metal interconnects to connect both electrodes to a common node. And during anodic bonding, this common node will be applied the same potential as the either the silicon or the glass depending on the design. And after die saw, the two electrodes will be separated. Clever layouts such as connecting adjacent devices onto a single interconnect could potentially make the task simple without clogging the wafer with metal interconnects.

2.4.5 Clamped Device

For this assembly, a device wafer was first aligned and anodically bonded to a top wafer, then the two wafer stack was mechanically clamped to the bottom glass wafer inside the package, as shown in Figure 2.20. For this assembly, a device wafer with 10 μm SOI and a bottom wafer without the center capacitor being etched were used. With this assembly, no anodic bond effect on the initial shape of the plate or charge of oxide would occur.

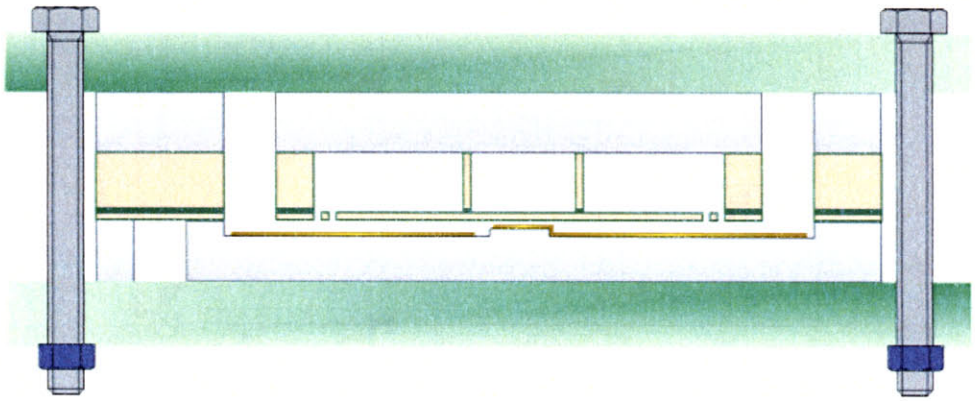


Figure 2.20. Cross section schematic of the clamped device.

2.5 Packaging

For the first proof-of-concept device, we intended to test the function of the circular zipper actuator and demonstrate capacitance change only in low frequency. Three packaging concepts have been investigated.

The first package used a plastic housing to enclose the chip and provide access for electrical contacts. Because the chip was designed such that electrical contacts needed to be made from both the top side and the bottom side, plastic housing was needed for both sides. Pogo pins were used to provide electrical signals. The schematic of the package was shown in Figure 2.22. The package was also designed to be able to assemble the devices

by clamping the die pieces. During testing, however, it was found that the long pogo pins with wires attached at the end caused the capacitance readings to be unstable. Hence, an improved package was needed to correct this problem.

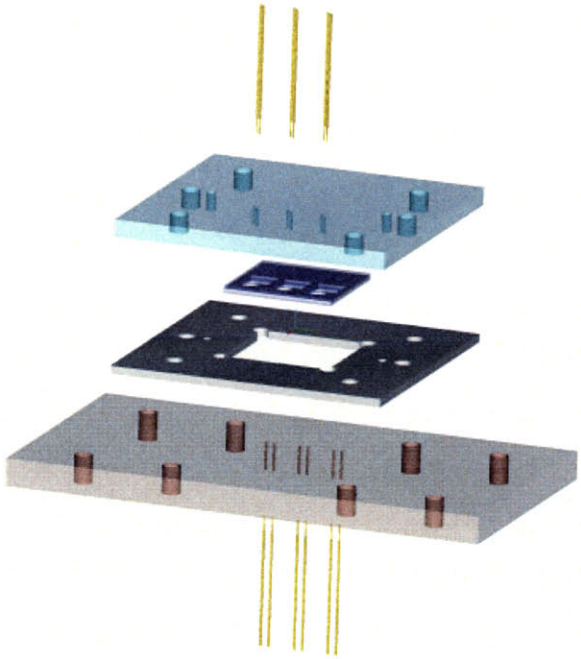


Figure 2.21. Schematic of the first package.

The second package had a similar plastic housing, but used much shorter pogo pins that protruded out of the plastic plates for only couple millimeters on each side to provide sufficient contact force. The schematic of the package is shown in Figure 2.22. Two printed circuit boards with wirings to BNC connectors were used to sandwich the plastic housing, as shown in Figure 2.23. This package proved to be much more robust during electrical tests. However, although this package was designed for the clamped-die assembly, it proved to cumbersome during mechanical and electrical testing. For the wafer or die level bonded devices, a third package was devised.

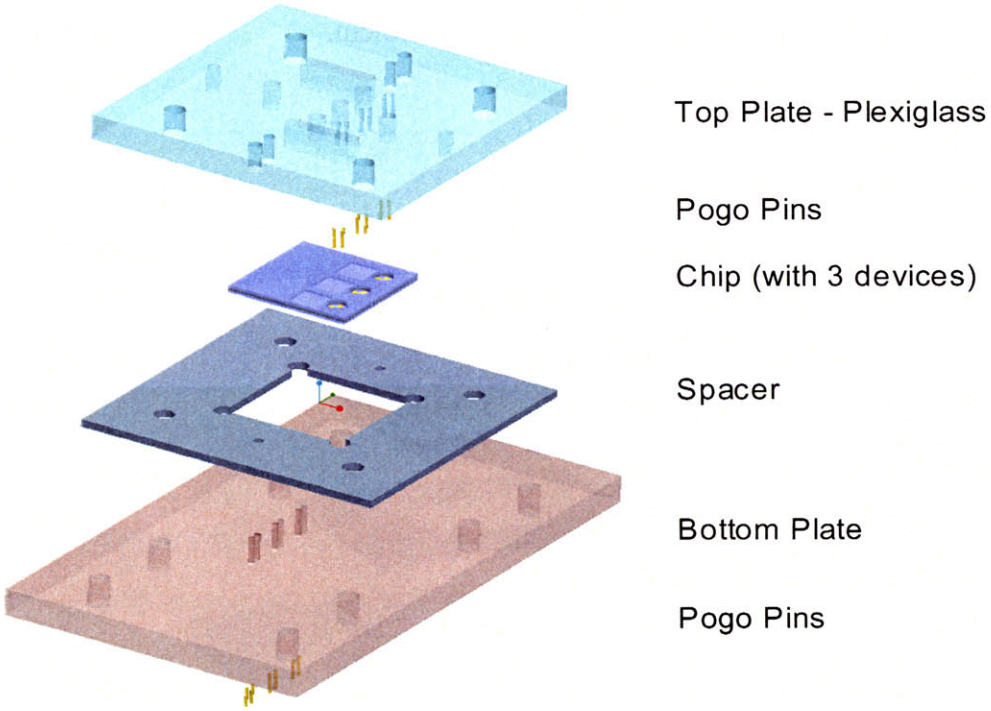


Figure 2.22. Schematic of the second package.

a) b)

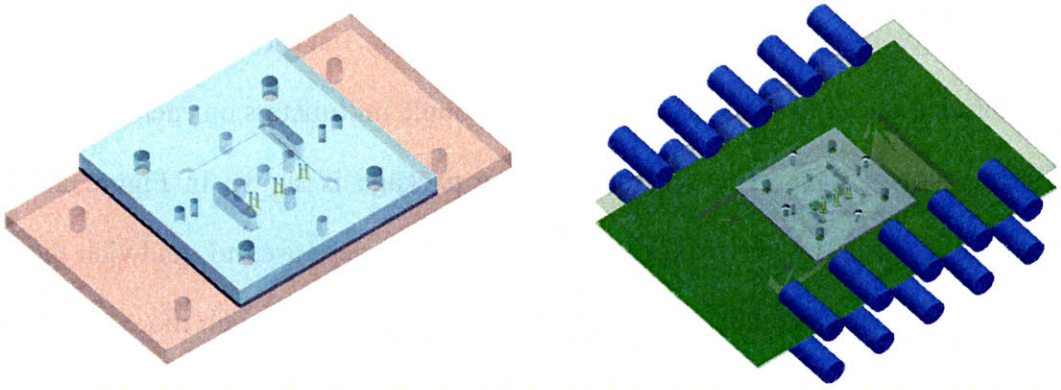


Figure 2.23. a), the assembled chip enclosed in the plastic housing, and b), the plastic housing is sandwiched between two PCB's with BNC connectors.

For the third package, only one PCB was needed, and the die was attached to the PCB using 3M conductive adhesive tape. Electrical connection was achieved by wire bonding gold wires from the electrode pads to the PCB or by soldering shielded electrical wires. This package would not be able to clamp the die pieces for testing. Figure 2.24 shows a picture of the bonded die taped to the PCB and with the middle device connected to the BNC with soldered wires. The testing leads are used for fixture compensation for capacitance measurement. With this package, electrical parasitics are minimized, and it also allows for better alignment during laser interferometer testing, which will be explained in the next chapter.

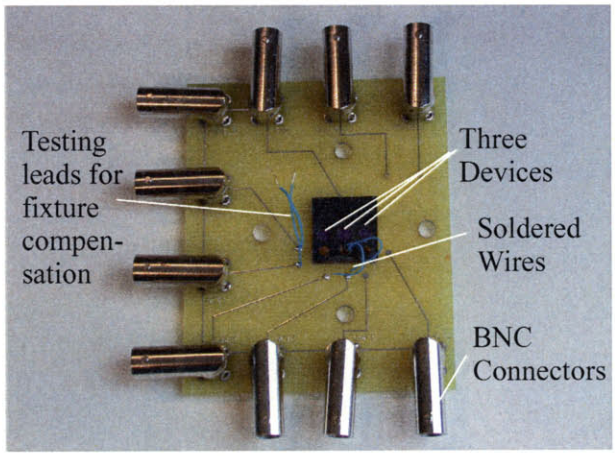


Figure 2.24. Picture of the new package.

2.6 Summary

This chapter introduces the design of the tunable capacitor and the fabrication process. Because of various constraints, the actual fabrication process was simplified, omitting the deposition of metal layer on the silicon plate. As a result, the actual device relies on the silicon plate to act as the ground for both the actuator and the capacitor. We have also explained other fabrication issues and the different approaches attempted to solve these problems. Three assembly methods were used: wafer-level bonded, die-level bonded and

clamped, and we have devised two different packages to test them. The testing results will be presented in the next chapter.

Chapter 3

Modeling and Simulation

In this chapter, we aim to understand the function of the fulcrum-lever structure with electrostatic zipping actuator by using a mathematical model and a finite element model. The mathematical model is solved with numerical methods with Matlab and the finite element model is done using ANSYS. The goal is to compare the results using these two independent methods and verify each other, although the numbers used in both simulations do not necessary represent the actual fabricated devices. By verifying our Matlab model, we could use Matlab to perform parametric design studies. On the other hand, by verifying the ANSYS model, we can use it to predict the behavior of the actual fabricated devices as will be explained in the next chapter. Furthermore, by understanding the function of the structure, we can realize the potential use of our design. It is found that because of electrostatic hysteresis, the actual useful tuning range of the device will be limited to within each of the actuation stage, which is about -10% for the before pull-in and zip-in stages. If capacitance hopping is desired, the tuning range is limited to actuation voltages less than the release voltage and those larger than the zip-in voltage, and in this case, a large jump of capacitance (with a tuning ratio of 1:1.66) can be achieved, but at each end, only small capacitance tuning (less than or close to -10%) can be achieved. However, the actual change of capacitance will depend on the specific design.

3.1 Mathematical Modeling

The operation of the device can be described by a lever-pivot structure. The silicon plate is effectively a lever that is pivoted by the fulcrum and bent by unevenly distributed electrostatic pressure exerted on the outer plate. The fulcrum is clamped at one end to anchor the structure, and is mated to the plate at the joint. Hence, part of the external moment exerted at the joint is lost to the fulcrum, and the rest is used to bend the center plate, the displacement of which determines the tuning effectiveness of the built-in capacitor. We are interested in the deflected profile of the plate as voltage is applied to its outer part. Such a profile depends on the mechanical properties and sizes of the plate and the fulcrum, properties and dimensions of the dielectric materials and the actuation voltage. In this chapter, we will describe the electro-mechanical model using a set of differential equations and will solve them simultaneously using the Matlab boundary value problem. The results from Matlab will then be compared with the finite element model using ANSYS.

A simplified cross-sectional schematic of the device is shown in Figure 3.1. The structure is divided into three regions, namely (1) the electrostatic actuator, (2) the fulcrum, and (3) the center plate. In the following analysis, we will use Timoshenko's elastic plate theory [49] with the following assumptions: 1) the structure is axisymmetric; 2) linear isotropic elastic properties apply (a Young's modulus of silicon of 169 GPa is used for comparison purpose; an average value of 145 GPa is equally appropriate); 3) the deflection of the plate is smaller than its thickness, and hence small deflection applies; 4) the fulcrum behaves as a shell and hence rotation of the fulcrum and the plate is the same at the joint; 5) there is no initial stress in the structure; 6) the fulcrum has square profile (although this is not necessarily the case after fabrication); and 7) the stiffness of the tethers are neglected (this is valid since we are only interested in comparing the Matlab model to the ANSYS model.)

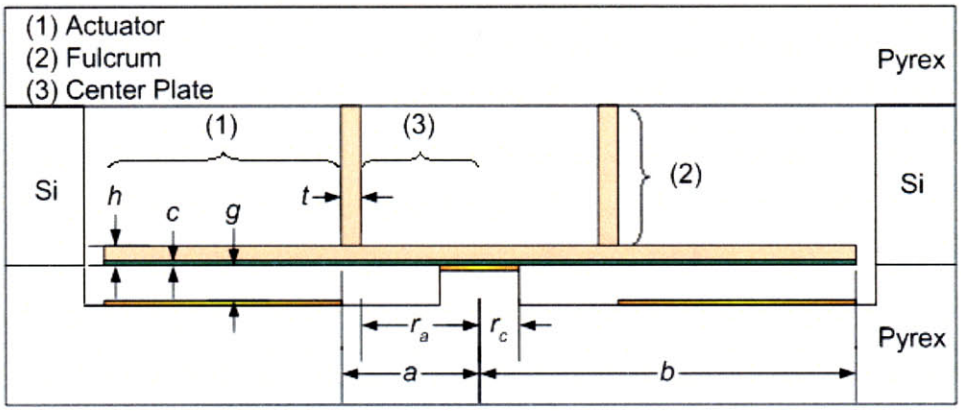


Figure 3.1. Simplified cross-sectional schematic of the actuator structure showing the three regions used in Matlab modeling.

Table 3.1. Dimensions used in design and modeling.

Item	Symbol	Value (μm)
Radius of capacitor	r_c	200
Radius of fulcrum	r_a	500
Thickness of fulcrum	t	50
Inner radius of actuator	a	$r_a + t$
Outer radius of actuator	b	1750/2000
Thickness of the top plate	h	17
Air gap	g	10
Thickness of oxide insulator	c	0.27

A simplified schematic is illustrated in Figure 3.2, which shows the coordinate systems used for each of the three regions. In the following sections, we will derive the formulation for solving with numerical methods in Matlab with boundary value problems.

3.1.1 Modeling of Actuator

During steady-state actuation by DC voltage, the zipping actuator has four stages: 1) before pull-in, 2) touch-down, 3) zip-in and 4) release. Using Matlab, we will analyze only three: 1) before pull-in, 2) zip-in and 3) release.

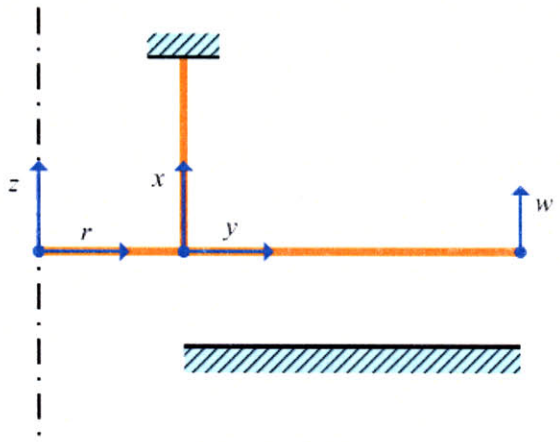


Figure 3.2. Simplified schematic of the actuator structure.

The governing differential equation for the outer region of the plate under electrostatic actuation is,

$$\frac{d^4w}{dr^4}+\frac{2}{r}\frac{d^3w}{dr^3}-\frac{1}{r^2}\frac{d^2w}{dr^2}+\frac{1}{r^3}\frac{dw}{dr}=\frac{\varepsilon V^2}{2D}\frac{1}{(g+w+c/\varepsilon_{ox})^2} \tag{3.2}$$

where w is the vertical displacement and is negative as defined from our coordinate system, r is the radius, ε is the vacuum permittivity, ε_{ox} is the relative permittivity of silicon dioxide and D is the flexural rigidity of the plate, which is defined by,

$$D=\frac{Eh^3}{12(1-\nu^2)} \tag{3.3}$$

where E is the average modulus of elasticity of silicon, and ν is the Poisson ratio.

Figure 3.3 compares the boundary conditions applied to Eq. (3.2) for the three stages of actuation. In all three cases, the rotation of the plate at $r=a$ is unknown and can be found only when the differential equations for all three regions are solved. The vertical deflection of the fulcrum (at $r=a$) is first assumed to be zero to facilitate the simulation.

After the system is solved, we can then compensate for the axial deflection of the fulcrum by calculating the total tension force acting on it.

For pure bending of a circular plate, the internal bending moments per unit length as function of radius can be expressed as,

$$M_r = -D\left(\frac{d^2w}{dr^2} + \frac{\nu}{r}\frac{dw}{dr}\right) \tag{3.4}$$

$$M_t = -D\left(\frac{1}{r}\frac{dw}{dr} + \nu\frac{d^2w}{dr^2}\right) \tag{3.5}$$

where M_r is the bending moment that acts along the circumferential sections of the plate, and M_t acts along the diametrical sections of the plate. The two moments relate to each other by a factor of Poisson's ratio. In our analysis, we chose to use M_r for moment balance calculation, and will ignore the use of M_t. For convenience, we use the letter M to represent the internal circumferential bending moment M_r. And M_1 is such bending moment for the outer plate at $r=a$. For case a), because there is no moment acting on the outer edge $r=b$, $M(b)$ is zero. For case b), since the pin-down point s is also unknown, five boundary conditions will be needed in order find this extra parameter using Matlab BVP. The fifth boundary condition is zero total moment at the outer radius. At the pin-down position, the slope is zero, and furthermore, since the plate lies flat at that position outward, the radius of curvature is infinity, and therefore, the derivative of the slope is also zero. We hence conclude that the total moment at the pin-down position must be zero. This boundary condition, however, will be discussed more in detail in 3.5.1.

The shear force per unit length of circumference at a radius r can be expressed as,

$$V = D\left(\frac{d^3w}{dr^3} + \frac{1}{r}\frac{d^2w}{dr^2} - \frac{1}{r^2}\frac{dw}{dr}\right) \tag{3.6}$$

For cases a) and c), the shear force acting at the outer edge is zero.

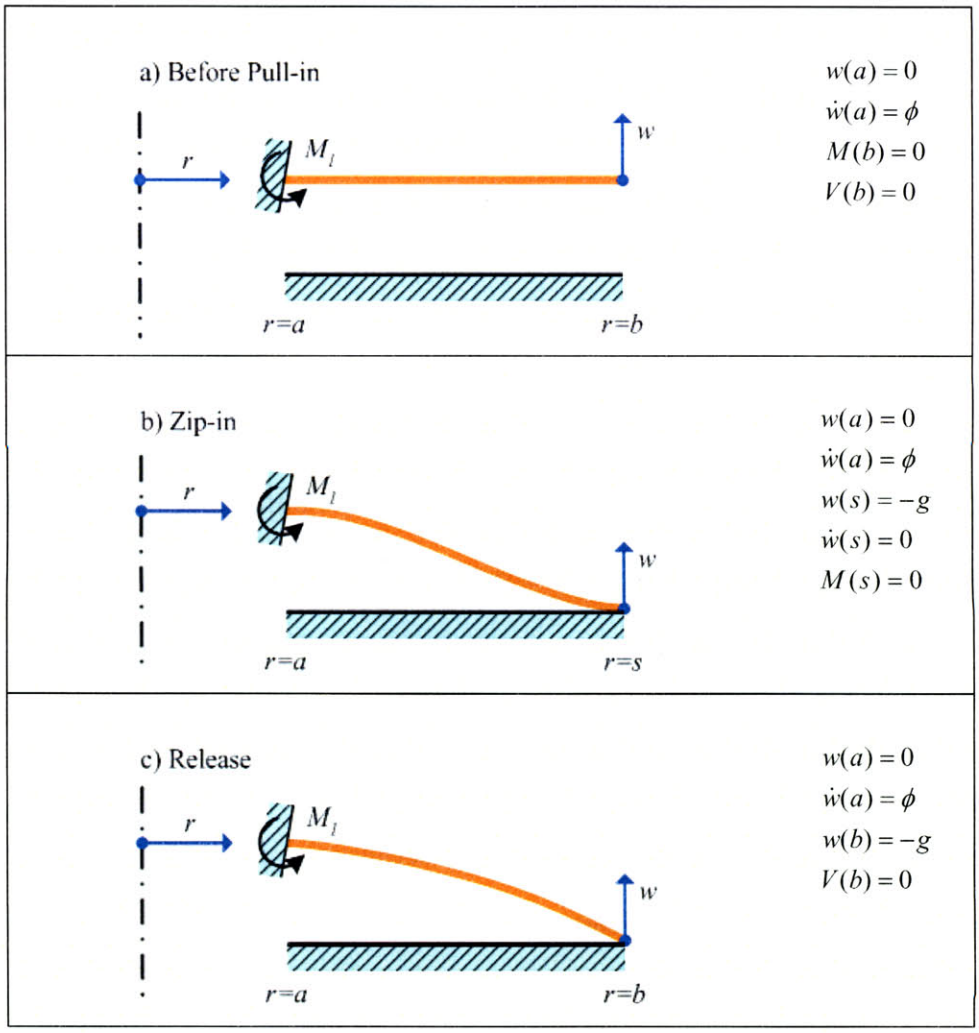


Figure 3.3. Boundary conditions of the outer membrane for the three cases a) before pull-in, b) zip-in and c) release.

Knowing the plate deflection, the total electrostatic force acting on the plate can be expressed as,

$$F = \int_a^b \frac{\varepsilon V^2}{2D} \frac{1}{(g + w + c/\varepsilon_{ox})^2} 2\pi r dr \qquad (3.7)$$

For the zip-in case, the total force becomes,

$$F = \int_a^s \frac{\varepsilon V^2}{2D} \frac{1}{(g + w + c/\varepsilon_{ox})^2} 2\pi r dr + \int_s^b \frac{\varepsilon V^2}{2D} \frac{1}{(c/\varepsilon_{ox})^2} 2\pi r dr \qquad (3.8)$$

3.1.2 Modeling of Fulcrum

For simplification, the fulcrum is modeled as a long cylindrical shell, which is governed by the following differential equation,

$$D_f \frac{d^4 y}{dx^4} + \frac{Et}{a^2} y = 0 \Rightarrow \frac{d^4 y}{dx^4} + 4\beta^4 y = 0 \tag{3.9}$$

where,

$$\beta = \left(\frac{Et}{4a^2 D_f} \right)^{1/4} \tag{3.10}$$

and the flexural rigidity for the fulcrum is,

$$D_f = \frac{Et^3}{12(1-\nu)^2} \tag{3.11}$$

The axial and circumferential internal bending moments per unit length can be expressed as,

$$M_x = -D_f \frac{d^2 w}{dx^2} \tag{3.12}$$

$$M_\varphi = \nu M_x \tag{3.13}$$

respectively. Similar to the plate case, we use M to represent the internal axial moment for the moment balance calculation. Specifically, M_2 is the internal axial bending moment at $r=a$ for the fulcrum.

Figure 3.4a) shows the boundary conditions for the fulcrum, which apply to all the three stages of actuation mentioned in 5.1.1. As mentioned before, we have assumed that the vertical deflection at $x=0$ is negligible. Assuming that after deflection, the fulcrum remains perpendicular to the membrane at $x=0$, we can derive that the rotation at the joint is the same for both the fulcrum and the membrane.

After the deflection is solved and the net electrostatic force is obtained, we can estimate the axial deflection of the fulcrum by simply accounting for the tension,

$$\delta = \frac{FL}{\pi atE} \tag{3.14}$$

where F is the electrostatic force as calculated by Eq. (3.7). For the zip-in case, b is substituted by λ and the result is the net electrostatic force.

Because we use a shell structure to represent the fulcrum in the Matlab model, the location of the shell impacts the solution slightly. For simplification, we have chosen to place the fulcrum at its outer edge, i.e., at $r=a+t$ instead of the center, i.e., at $r=a+t/2$, which is more realistic. In order to take into consideration of the effect of the fulcrum location, after the deflection is solved, we can define that the displacement of the center of the fulcrum, instead of the outer edge, is zero, and translate the deflection by that amount.

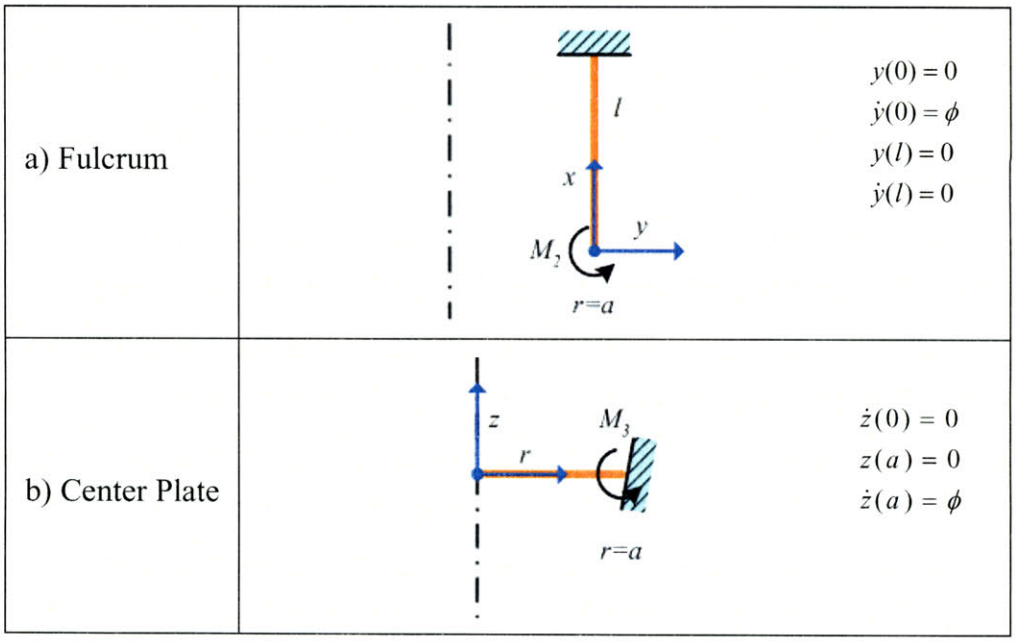


Figure 3.4. Boundary conditions for a) the cylindrical fulcrum and b) the center plate.

3.1.3 Modeling of Center Plate

The center plate is subjected to a moment applied to its outer edge. We can write the governing equation as,

$$\frac{d}{dr}\left[\frac{1}{r}\frac{d}{dr}\left(r\frac{dz}{dr}\right)\right]=0 \qquad (3.15)$$

The boundary conditions for the center plate are shown in Figure 3.4 b). In the figure, M_3 is the internal circumferential bending moment at $r=a$, and $M_3=M_1-M_2$.

The compensated center deflection is obtained by subtracting the axial deflection of the fulcrum as calculated from Eq. (3.14) as well as the center translation as explained above.

3.2 Solution Using Matlab

In order to find the deflection profile of the plate, the governing equations for the three regions must be solved simultaneously. However, because Eq. (3.2) is nonlinear and an analytical solution is not possible, numerical simulation with Matlab boundary value problem (BVP4C) is used to obtain a closed form solution.

BVP4C uses a collocation method (also called the Simpson method) to solve a system of ODE's of the form $y' = f(x,y,p)$ on the interval [a,b], subject to general two-point boundary conditions of the form $\mathrm{bc}(y(a),y(b),p) = 0$, provided that an initial guess of the mesh and corresponding values are provided. Note that p is a vector of unknown parameters. The approximate solution is a continuous function that is a cubic polynomial on each subinterval of the mesh. The function satisfies the boundary condition and the differential equations at both ends and the midpoint of each subinterval. The program uses linear equation solvers for solving nonlinear algebraic equations. It allows a system of ODE's to be solved simultaneously, given that the boundary conditions are well defined, a good

guess is provided, and that all ODE's are evaluated in the same interval. It can also be used to solve for unknown parameters in the ODE's. These demonstrate that the BVP4C can be a powerful tool in solving elastic engineering structures with relatively complicated patterns and loads.

3.2.1 Formulation with BVP4C

Because all ODE's need to be defined in the same interval in order for them to be solved simultaneously using BVP4C, it is necessary to normalize the three governing equations such that the range is defined at [0,1] for each ODE. To do this, we will introduce corresponding normalized variables and obtain the normalized equations.

1. Actuator. The normalized variables are,

$$W = \frac{w}{g}$$

$$R = \frac{r-a}{b-a}, \text{ or } R = \frac{r-a}{s-a} \text{ for zip-in case}$$

the normalized plate equation becomes,

$$\frac{d^4W}{dR^4} + \frac{2}{R+A}\frac{d^3W}{dR^3} - \frac{1}{(R+A)^2}\frac{d^2W}{dR^2} + \frac{1}{(R+A)^3}\frac{dW}{dR} = -\frac{\xi}{\left(1+W+\frac{c/\varepsilon_{ox}}{g}\right)^2} \qquad (3.16)$$

where,

$$A = \frac{a}{b-a}, \text{ and}$$

$$\xi = \frac{(b-a)^4 \varepsilon V^2}{2Dg^3}$$

and again, b is substituted by λ for the zip-in case.

2. Fulcrum. The normalized variables are,

$$X = \frac{x}{l}; Y = \frac{y}{g}$$

The normalized equation becomes,

$$\frac{d^4Y}{dX^4} + 4\beta^4 l^4 Y = 0 \tag{3.17}$$

3. Center Plate. The normalized variables are,

$$R' = \frac{r}{a}; Z = \frac{z}{g}$$

The normalized equation becomes,

$$\frac{d^3Z}{dR'^3} + \frac{1}{R'}\frac{d^2Z}{dR'^2} - \frac{1}{R'^2}\frac{dZ}{dR'} = 0 \tag{3.18}$$

Written in the form of state equations, the ODE function to be solved by Matlab BVP4C is as shown in Eq. (3.19), where state $y(1)$ corresponds to W, the normalized deflection of the actuator, state $y(5)$ corresponds to Y, the normalized deflection of the center plate, and state $y(8)$ corresponds to Z, the normalized deflection of the fulcrum, and so forth.

$$\frac{d}{dx}\begin{bmatrix} y(1) \\ y(2) \\ y(3) \\ y(4) \\ \\ \\ y(5) \\ y(6) \\ y(7) \\ \\ y(8) \\ y(9) \\ y(10) \\ y(11) \end{bmatrix} = \begin{bmatrix} y(2) \\ y(3) \\ y(4) \\ -\dfrac{\xi}{\left(1+\dfrac{c/\varepsilon_{ox}}{g}+y(1)\right)^2} - \dfrac{2}{x+A}y(4) + \dfrac{1}{(x+A)^2}y(3) - \dfrac{1}{(x+A)^3}y(2) \\ y(6) \\ y(7) \\ -\dfrac{1}{x}y(7) + \dfrac{1}{x^2}y(6) \\ y(9) \\ y(10) \\ y(11) \\ -4\beta^4 l^4 y(8) \end{bmatrix} \tag{3.19}$$

The boundary conditions after normalization are listed in Table 3.2 for each of the different regions and actuation stages. Note that the bending moment at $r=a$ is derived as well. M_1 represents the moment acting at the joint by the outer plate, M_2 represents that by the fulcrum, and M_3 represents that by the center plate. The total moment at $r=a$ must be zero at equilibrium.

Table 3.2. Boundary conditions for the actuator, fulcrum and center plate after normalization.

1) Actuator	a) Before Pull-in	$W(0)=0$ $\dot{W}(0)=\frac{b-a}{g}\phi \Rightarrow \phi=\frac{g}{b-a}\dot{W}(0)$ $M(1)=0 \Rightarrow \ddot{W}(1)+\frac{\nu}{1+A}\dot{W}(1)=0$ $V(1)=0 \Rightarrow \dddot{W}(1)+\frac{1}{1+A}\ddot{W}(1)-\frac{1}{(1+A)^2}\dot{W}(1)=0$ $\Rightarrow M_1=-D\frac{g}{(b-a)^2}\left[\ddot{W}(0)+\frac{\nu}{A}\dot{W}(0)\right]$
	b) Zip-in	$W(0)=0$ $\dot{W}(0)=\frac{s-a}{g}\phi \Rightarrow \phi=\frac{g}{s-a}\dot{W}(0)$ $W(1)=-1$ $\dot{W}(1)=0$ $M(1)=0 \Rightarrow \ddot{W}(1)=0$ $\Rightarrow M_1=-D\frac{g}{(s-a)^2}\left[\ddot{W}(0)+\frac{\nu}{A}\dot{W}(0)\right]$
	c) Release	$W(0)=0$ $\dot{W}(0)=\frac{b-a}{g}\phi$ $W(1)=-1$ $M(1)=0 \Rightarrow \ddot{W}(1)+\frac{\nu}{1+A}\dot{W}(1)=0$ $V(1)=0 \Rightarrow \dddot{W}(1)+\frac{1}{1+A}\ddot{W}(1)-\frac{1}{(1+A)^2}\dot{W}(1)=0$

Table 3.2. Boundary conditions for the actuator, fulcrum and center plate after normalization.

2) Fulcrum	$Y(0)=0$ $\dot{Y}(0)=\frac{l}{g}\phi \Rightarrow \phi=\frac{g}{l}\dot{Y}(0)$ $Y(1)=0$ $\dot{Y}(1)=0$ $\Rightarrow M_2=-D_f\frac{g}{l^2}\ddot{Y}(0)$
3) Center Plate	$Z(1)=0$ $\dot{Z}(0)=0$ $\dot{Z}(1)=\frac{a}{g}\phi \Rightarrow \phi=\frac{g}{a}\dot{Z}(1)$ $M_3=M_1-M_2$ $\Rightarrow -D\frac{g}{a^2}\left[\ddot{Z}(1)+v\dot{Z}(1)\right]$ $=M_1-M_2$

With Matlab BVP4C, the boundary condition function is expressed as $bc(y(a),y(b),p) = 0$, where $[a,b]$ is the interval on which the ODE's are defined. Because the three ODE's are solved simultaneously, continuation at the location $r=a$ is used as the boundary condition, i.e., rotations are the same for all three regions, and the total circumferential moment is zero. Note that we have assumed that the fulcrum has rigid rotation at its end because it is much more stiffer than the plate. However, this might not hold true for large deflections. Applying these continuation conditions, the boundary functions used for each of the three actuation stages can be derived as listed in Table 3.3.

Table 3.3. Boundary functions used in Matlab BVP4C for the three stages a) before pull-in, b) zip-in and c) release

a) Before Pull-in	$0 = \begin{bmatrix} y_a(1) \\ y_b(3)+\frac{\nu}{1+A}y_b(2) \\ y_b(4)+\frac{1}{1+A}y_b(3)-\frac{1}{(1+A)^2}y_b(2) \\ \frac{1}{b-a}y_a(2)-\frac{1}{a}y_b(6) \\ y_b(5) \\ y_b(6) \\ y_a(8) \\ y_b(8) \\ y_b(9) \\ \frac{1}{b-a}y_a(2)-\frac{1}{l}y_a(9) \\ -D\frac{1}{(b-a)^2}\left[y_a(3)+\frac{\nu}{A}y_a(2)\right]-D_f\frac{1}{l^2}y_a(10)+D\frac{1}{a^2}\left[y_b(7)+\nu y_b(6)\right] \end{bmatrix}$
b) Zip-in	$0 = \begin{bmatrix} y_a(1) \\ y_b(1)+1 \\ y_b(2) \\ y_b(3) \\ \frac{1}{s-a}y_a(2)-\frac{1}{a}y_b(6) \\ y_b(5) \\ y_a(6) \\ y_a(8) \\ y_b(8) \\ y_b(9) \\ \frac{1}{s-a}y_a(2)-\frac{1}{l}y_a(9) \\ -D\frac{1}{(s-a)^2}\left[y_a(3)+\frac{\nu}{A}y_a(2)\right]-D_f\frac{1}{l^2}y_a(10)+D\frac{1}{a^2}\left[y_b(7)+\nu y_b(6)\right] \end{bmatrix}$

Table 3.3. Boundary functions used in Matlab BVP4C for the three stages a) before pull-in, b) zip-in and c) release

c) Release	$0 = \begin{bmatrix} y_a(1) \\ y_b(1)+1 \\ y_b(3)+\frac{\nu}{1+A}y_b(2) \\ y_b(4)+\frac{1}{1+A}y_b(3)-\frac{1}{(1+A)^2}y_b(2) \\ \frac{1}{b-a}y_a(2)-\frac{1}{a}y_b(6) \\ y_b(5) \\ y_a(6) \\ y_a(8) \\ y_b(8) \\ y_b(9) \\ \frac{1}{b-a}y_a(2)-\frac{1}{l}y_a(9) \\ -D\frac{1}{(b-a)^2}\left[y_a(3)+\frac{\nu}{A}y_a(2)\right]-D_f\frac{1}{l^2}y_a(10)+D\frac{1}{a^2}\left[y_b(7)+\nu y_b(6)\right] \end{bmatrix}$

In addition to defining the ODE functions and boundary functions, BVP4C requires an initial guess function that corresponds to a guess mesh, because boundary value problems can have more than one solution. BVP4C uses residual control, i.e., by evaluating the residuals of the approximate solution, and controlling their sizes, to control the errors due to poor guesses. However, a good guess for an initial mesh is important in obtaining desired solutions, and often this is the hardest part in solving the boundary value problems with BVP4C. It turns out that for the before pull-in case, a zero initial guess is sufficient, for the zip-in and release cases, however, a fourth order polynomial is needed for the actuator.

3.2.2 Matlab Results

Simulation results using Matlab BVP4C are demonstrated below.

a) Before Pull-in. In order to find the pull in voltage, voltage is increased in steps, and each solution is used as the guess function for the following solution. The Matlab script is enclosed in Appendix C.1. Figure 3.5a) shows the displacement of the plate with increasing voltage. Because the plate is axisymmetric, only displacement from the center to the outer edge is shown. b) shows the rotation of the plate. A continuous rotation at the anchor manifests acceptable residual control. c) and d) show the displacement and rotation of the fulcrum over its length. Notice that we have neglected the horizontal displacement at the anchor point. e) shows the end deflection as function of voltage. Because pull-in is when the system becomes unstable, we should expect that the solution starts to diverge when it occurs. In this case, it occurs when the voltage reaches 110.2 V. f) shows the center displacement as function of voltage. At pull-in, the center displacement is about 10.78 nm in this case. The center deflection after compensating the axial deflection of the fulcrum as well as translation of the fulcrum center displacement is also shown in the figure, but no obvious difference is observed since the axial deflection is much smaller.

b) Zip-in. The zip-in case is a little more complicated because it involves an unknown parameter - the pin down position, and hence, an initial guess for that parameter. The initial guess turns out to be very critical in finding the right solution. If the guess value is not chosen carefully, the results might appear to have irrational profiles, or the residuals of the solution might be out of tolerance. In order to find the appropriate guess, an iterative approach is used where the guess is compared to the solution until they agree. This derived parameter will then be used as the first guess and each derived parameter will then be used as the guess parameter for the next incremental solutions. Furthermore, a fourth order polynomial for the displacement of the outer plate is necessary in order to obtain good residual control.

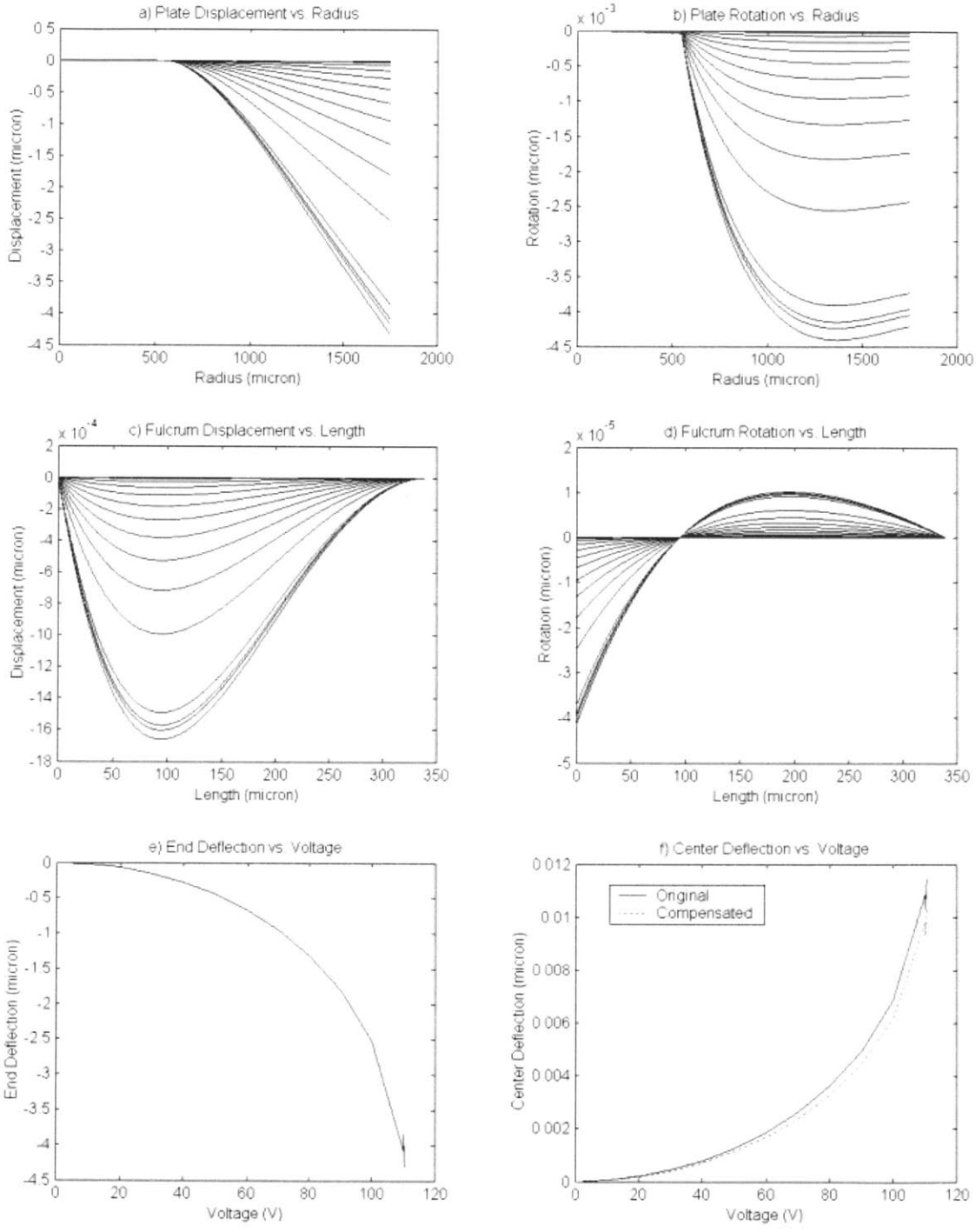


Figure 3.5. Simulation results for the plate and fulcrum before pull-in.

A voltage range from 110 to 180 volts with 10-volt increment is applied. See Appendix C.2 for the Matlab script. The results are plotted in Figure 3.6, where a) shows the deflection profiles, and b) shows the rotation. c) plots the normalized deflection profiles and shows that they converge to a fourth polynomial shape, which has important implication for solving the problem with energy methods. d) shows the pin-down position as function of voltage and e) shows the center deflection. Note that the normalized outer deflection is not set at 1, but rather a number that is determined by the ANSYS program, such that the two results can be compared. Refer to the ANSYS section for details. For a pin-down position r=1750 μm, which is the outer radius of the plate used in the design, the zip-in voltage is found to be 110V, and the center defection is 49.69 nm. In plot e), we added a curve that shows the center deflection by compensating the axial deflection of the fulcrum as well as translation of fulcrum center displacement, and that reduces the center deflection to 42.67 nm.

c) Release. The release case is similar to the zip-in case in that it also has an unknown parameter - voltage. For r=1750 μm, it is found that the release voltage is 65.33 V. The center deflection is 21.5 nm and after compensated for axial deflection and center translation, 19.3 nm. The plate and fulcrum displacement and rotation are plotted in Figure 3.7. The Matlab code can be found in Appendix C.3.

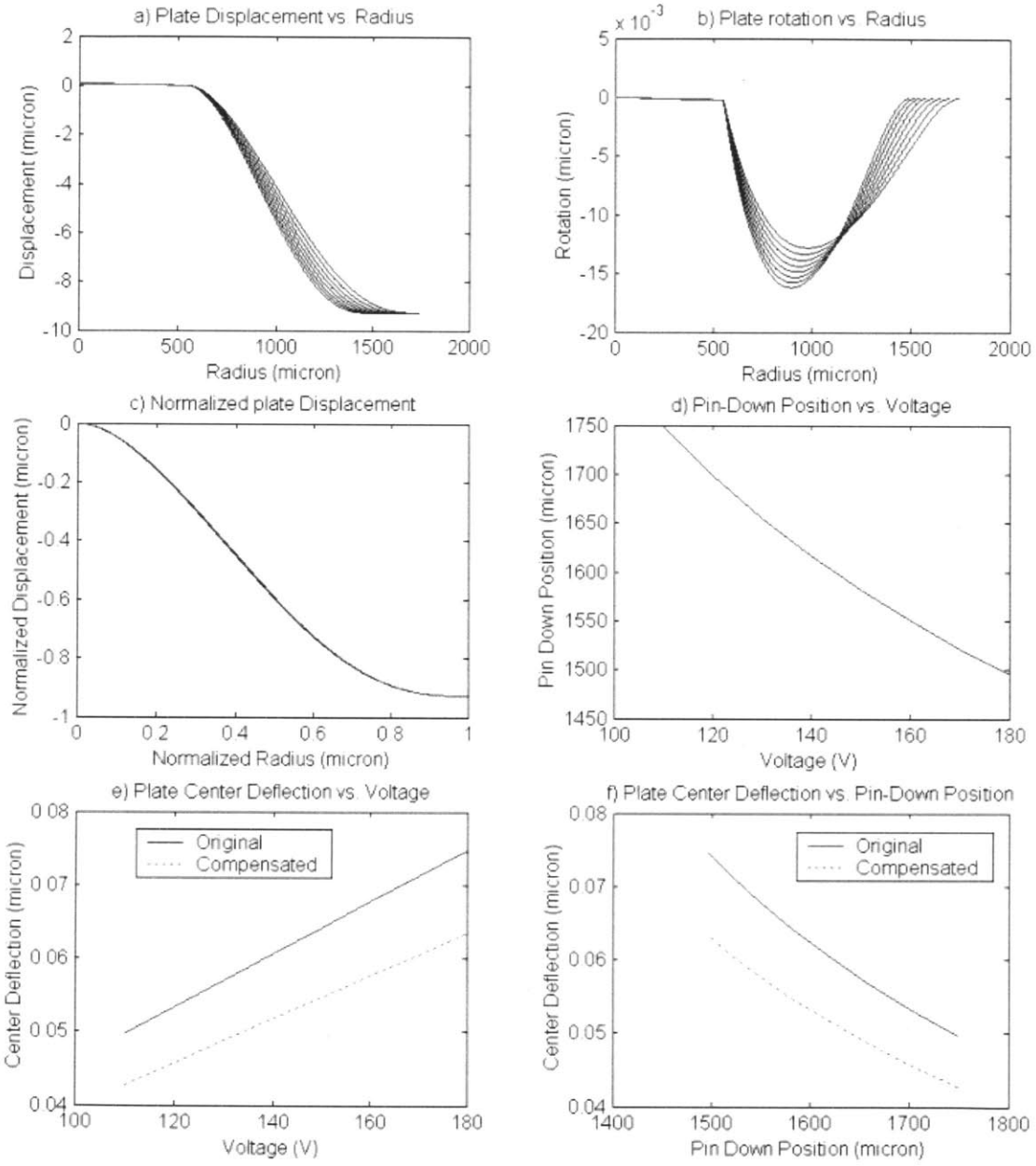


Figure 3.6. Simulation results for the zip-in case.

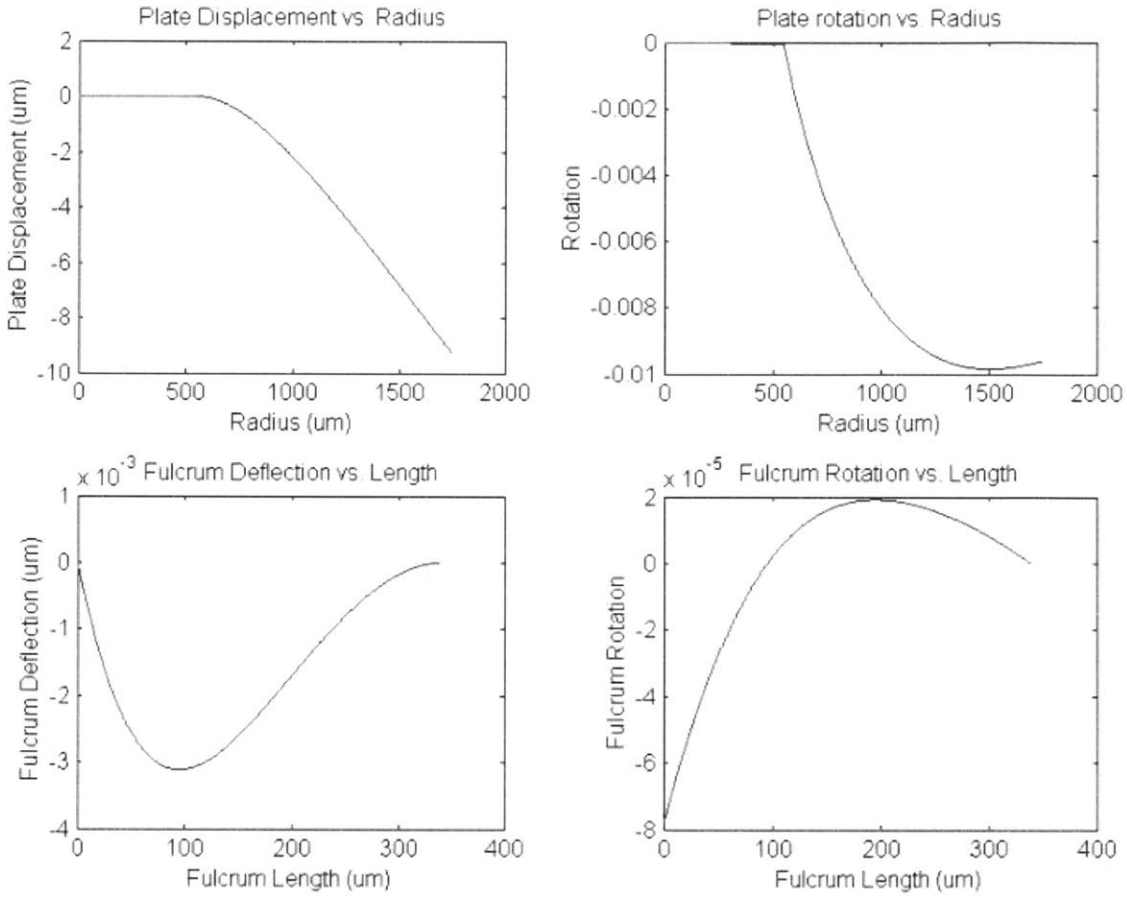


Figure 3.7. Simulation results for the release case.

3.3 MOS Structure Analysis

The silicon plate actuator is effectively a metal/oxide (with air)/p-type semiconductor structure. For such structure, the charge distribution within the silicon might affect the electric field strength. To find out whether such an effect could be significant, we will do an analysis using a MOS structure. Firstly, we need to calculate the threshold voltage for charge inversion to occur in order to determine the operation regime when an external voltage is applied.

The properties of the materials are as follow. The silicon is Boron doped to have resistivity 5-18 mΩcm. This in turn corresponds to an acceptor concentration of $N_A = 7 \times 10^{18} cm^{-3}$ [50]. The relative permittivity of silicon is 11.9 and that of oxide is 3.9. The oxide is 270 nm thick, and the air is originally 10 μm thick. The work function of gold is about W_m=4.7 eV and for silicon, W_s=5.12 eV.

Voltage applied to a MOS structure changes the equilibrium charge distribution, which depends on the applied voltage in relation to the threshold voltage. Threshold voltage is the voltage required to bring the structure to the edge of inversion. By carrying out the calculation, we can find that the built-in potential for the MOS structure, which is the total potential drop across the structure in thermal equilibrium, is 0.44 eV. The calculated threshold voltage for the case when the silicon plate is not in contact with gold is 1.7×10^4 V, and for the case when the silicon plate is in contact with gold, it is about 117 V. See Appendix C.4 for the Matlab script. Since voltage less than 100 V is applied to our device, we can conclude that our device operates in the depletion regime. The depletion layer may alter the electric field as well as the force applied to the actuator. Figure 3.8a) shows the depletion layer thickness as a function of voltage assuming that the silicon is in contact with gold throughout application of the actuation voltage, which is the worst-case scenario. At 100V, the depletion layer thickness could reach 12 nm. To see how significant these numbers are, we can calculate the surface potential of the silicon. The surface potential relates to the charge distribution inside the silicon and can be regarded as the potential drop across the silicon. Figure 3.8b) shows the surface potential as function of applied voltage. It shows that at 100 V, the potential drop across the silicon is only 0.7 V, which is insignificant compared to the applied voltage. We hence can conclude that the presence of the MOS structure should not affect the applied electric field in a significant level.

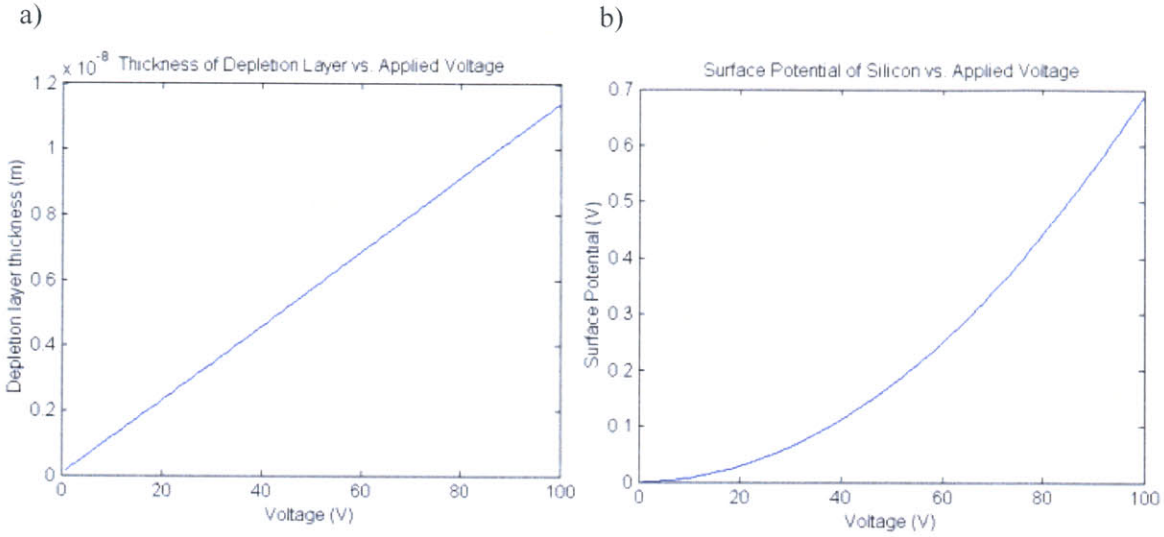


Figure 3.8. MOS structure analysis showing a) depletion thickness and b) surface potential of silicon as function of applied voltage.

Applying the same analysis to the capacitor, where a measurement voltage signal on the order of 0.5 V is used, it is found that the presence of the depletion layer does not change the total capacitance significantly. In fact, no obvious difference in the total capacitance can be found before and after considering the MOS structure in the capacitor. See Appendix C.5 for the Matlab script.

3.4 ANSYS Simulation

Static deflection of the fulcrum-plate structure is simulated with the finite element analysis package ANSYS University Advanced version 8.0. In the simulation, similar to the Matlab case, the structure is modeled using 2-D axisymmetric elements. The goal of the simulation is to compare it with numerical results from Matlab and estimate any discrepancies between the two. We will first explain the sequential coupled electrostatic field and structural analysis in ANSYS, then the use of surface-to-surface contact analysis. Results and comparison with Matlab will then be presented.

3.4.1 Model Setup

ANSYS is equipped with a command macro ESSOLV to solve coupled electrostatic field and structural problems using sequentially coupled physics analysis. The ANSYS help manual explains how it works: "The macro will automatically iterate between an electrostatic field solution and a structural solution until the field and the structure are in equilibrium. The macro automatically updates the electrostatic field mesh to conform to the structural displacements using the morphing procedure" (ANSYS coupled-field guide, Chapter 2). A simple description of our basic analysis procedure entails: 1) build a solid model with both electrostatic and structural domains and mesh both domains; 2) create the electrostatic physics environment by assigning element types to the meshed region, defining material properties, defining boundary conditions and loads, etc.; 3) clear the electrostatics physics and repeat step 2) for creating the structural physics environment; and 4) solve with ESSOLV macro. A flow chart of the data flow algorithm of the ESSOLV macro is illustrated in Figure 3.9. One can refer to the ANSYS manual for more detailed procedures.

The geometry of the FEM model for the device is shown in Figure 3.10. Elements used for the different regions are labelled on the schematic. The global y axis is the axisymmetric axis. Element PLANE121 is used to model the air region, which is grouped as a component for mesh morphing during the iteration process. PLANE121 is a 2-D, 8-node electrostatic solid element that has only voltage degree of freedom at each node. The only material input for the element is the relative permittivity. A triangular form of the element is used for our simulation. Notice that the air region starts short of the y axis, this is to prevent warning message "negative radius element" during mesh morphing. Element PLANE82, a 2-D, 8-node, structural solid element, is used to model the fulcrum and the plate, which is treated as one region to ensure proper boundary condition at the joint.

Oxide deposited on the outside of the fulcrum and plate as well as the buried oxide layer are neglected structurally because they are much thinner than the silicon plate. As in the Matlab version, an equivalent air gap height of 10.07 μm is used. This is done by converting the oxide thickness into equivalent air thickness without modifying the electric field. By neglecting the oxide in the picture, simulation was much more efficient and the CPU time was greatly reduced. As can be seen in the next paragraph, the error introduced by using only air as dielectric is minimal. The bottom electrode is not meshed and is used only for voltage application purpose.

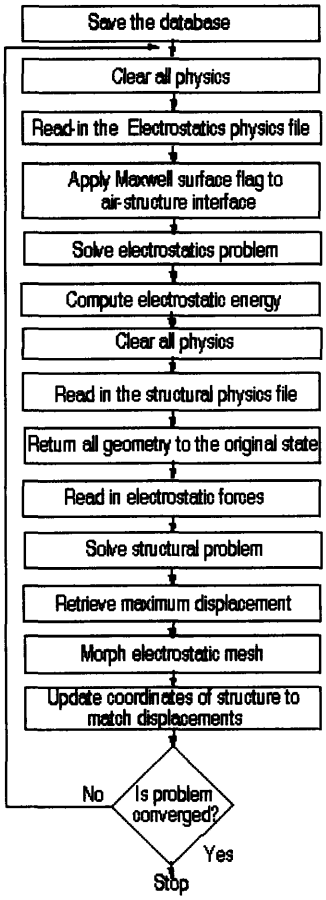


Figure 3.9. Flow chart of the data flow algorithm of the ESSOLV macro (ANSYS manual, Chapter 2, coupled-field guide).

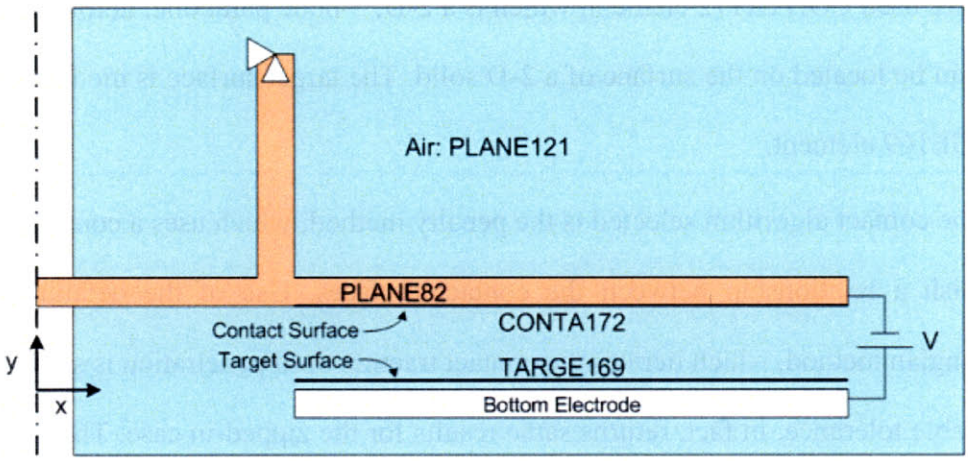


Figure 3.10. Schematic of the actuator used in FEM model.

Because of the touch-mode operation nature of the device, a surface-to-surface contact analysis is needed. ANSYS does the contact analysis by establishing contact and target surfaces that form the contact pairs. The contact and target elements are associated with each other via a shared real constant set. Details on contact analysis can be found in Chapter 11 of the structural guide of the ANSYS manual. In our model, the contact surface is the lower surface of the axisymmetric silicon plate and the surface is deformable. The target surface is an "imagined" rigid surface above the ground plate, as shown in Figure 3.10. During simulation, it is found there needs to be a minimum clearance between the target surface and the bottom electrode in order to ensure proper mesh morphing. A 0.8-μm clearance is used, although 0.5 μm is sufficient in most cases. Therefore, instead of 10 μm, the zipping plate only has a travel range of 9.27 μm in the simulation model. A more realistic model with the 0.27 μm oxide included as to ensure 10-μm travel was also obtained. And as mentioned above, the simulation was much more time-costly because of the added elements for the thin oxide. We found that for an input voltage of 60 V, the outer deflection of the plate is 0.6824 μm with oxide included, compared to 0.6828 μm using only air.

Therefore, the error caused by neglecting the oxide is negligible. To model the contact surface, we used CONTA172 element, which is a 2-D, 3-node parabolic, deformable element that can be located on the surface of a 2-D solid. The target surface is modeled using 2-D TARGE169 element.

The contact algorithm selected is the penalty method, which uses a contact stiffness to establish a relationship between the contact surfaces. Use of the default augmented Lagrangian method, which iterates the contact traction until penetration is smaller than the allowable tolerance, in fact, returns same results for the zipped-in case. The other options for the contact element could use default values. For example, changing the option of the contact surfaces from "no separation contact" to "unilateral contact" (default) does not change the results. A long list of real constants associated with the contact pairs are available. Default values are also used for all real constants except the contact stiffness. ANSYS suggests that if bending deformation dominates, such as the case for our model, a smaller contact stiffness is suggested. A value of 0.05 is chosen but a value of 0.1 returns same results.

3.4.2 Simulation Results

The ESSOLV macro has the capability of solving problems with incremental load steps. When the RUSEKY is selected to 1, and multiple load steps are defined, each run is a continuation of a previous run, whereby the morphed geometry is used for the initial electrostatic simulation. μMKSV units were used in the simulation. The ANSYS code for the simulation of an input voltage can be found in Appendix D.1, and that for the simulation of a sweep voltage input can be found in Appendix D.2.

To simulate pull-in, zip-in and release processes, incremental voltages from 20 V to 180 V and back to 20 V were used. The profiles of the silicon plate at different sweeping

voltages are plotted in Figure 3.11. Note that at pull-in, contact penetration is observed due to the small contact stiffness used. However, variations in results caused by the penetration are likely to be negligible. One can decrease the tolerance for penetration, but this will increase the CPU time further.

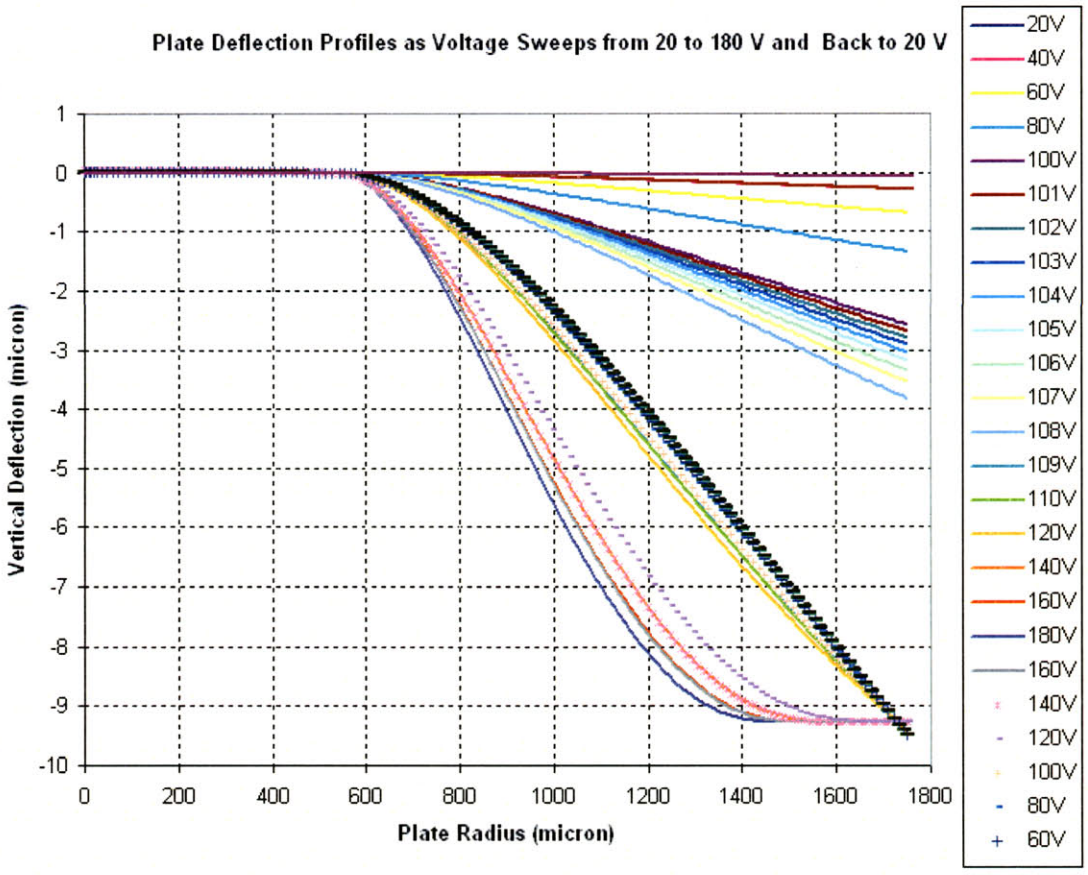


Figure 3.11. Deflection profiles of silicon plate for different sweep voltages.

Electromechanical hysteresis can be seen more obviously as the end deflection is plotted as a function of sweeping voltage, as shown in Figure 3.12. The results from the Matlab simulation is also plotted. The dotted lines represent the regions in Matlab that are not simulated. From ANSYS, pull-in occurs at 108.5 ± 0.5 V with tip touch-down, followed by zip-in at 130 ± 10 V, and release at 42.5 ± 2.5 V. The pull-in curve from both simula-

tions match very well. The discrepancy of the pull-in voltage between the two simulations is 1.7 V. For the release case, a discrepancy of 22.8 V is observed.

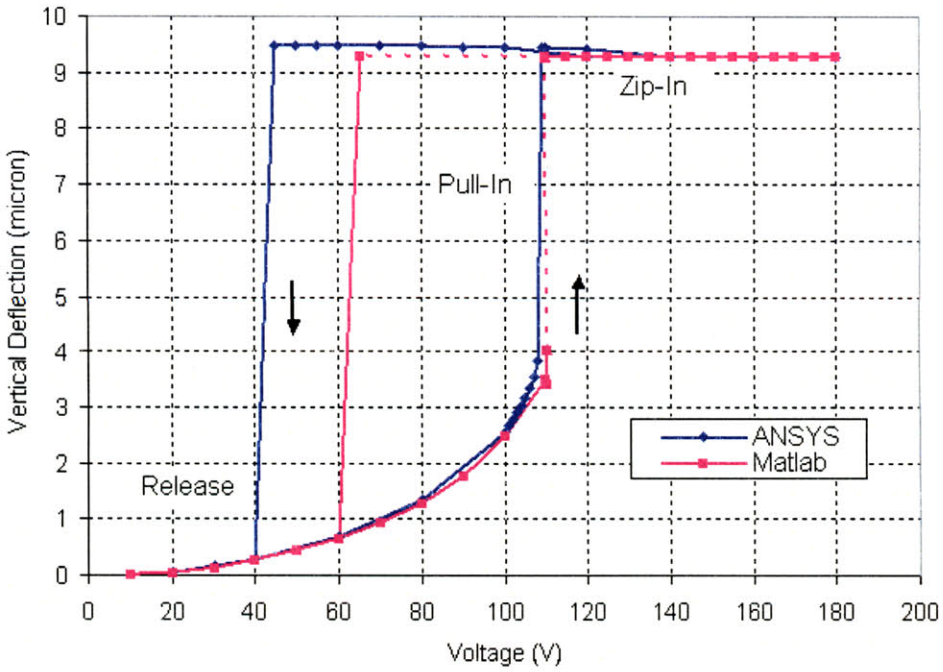


Figure 3.12. The end deflection of the plate as function of sweeping voltage comparing Matlab to ANSYS.

A plot of the center deflection comparing the ANSYS results with the pull-in and zip-in simulations from Matlab is shown in Figure 3.13. The center deflection from both simulations match very well until zip-in. At zip-in, a discrepancy of about 2.5 nm is observed. The discrepancy can be attributed to the fact that in the Matlab model, the fulcrum is modeled as a shell with rigid rotation at the joint, while in the ANSYS model, it is a 2-D cylinder with 50 μm thickness.

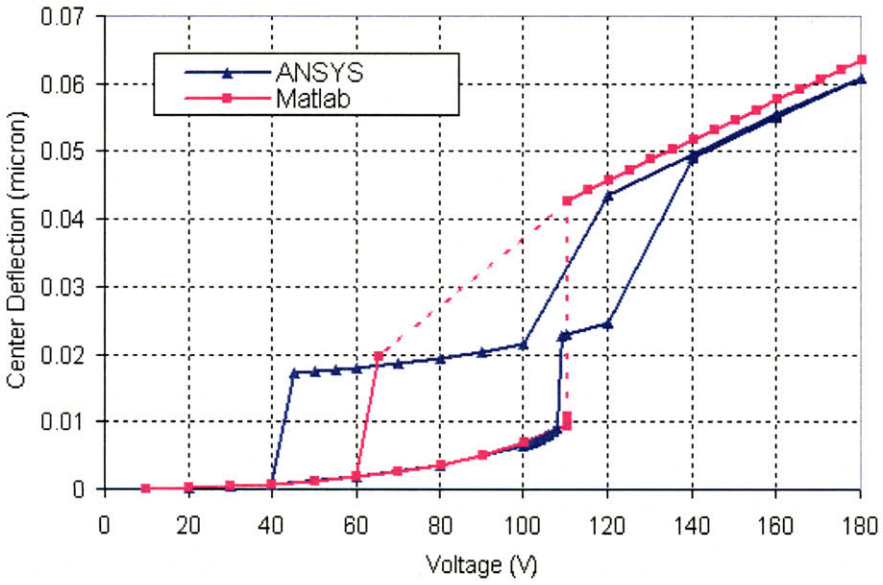


Figure 3.13. Center deflection of plate after zip-in comparing Matlab to ANSYS.

In order to explain the hysteresis seen above, we can plot the electrostatic force and spring force as function of the outer plate deflection in the same plot as shown in Figure 3.14. Note that the electrostatic force is a log plot because the range that it spans is too large. In this plot, we use the displacement data obtained from ANSYS as shown in Figure 3.11. We then integrate the function as in Eq. (3.7) to obtain the electrostatic force as function of voltage. Note that because the deflections between the pull-in and touch-down stages are not stable solutions, they are not directly obtainable from ANSYS, and instead, they are estimated using the deflection from the before pull-in stage by assuming that the normalized deflection against the outer deflection is the same, which is a very good estimate. The spring force as function of displacement is obtained by Matlab; these are obtained by using the stable solutions as shown in Figure 3.5 and Figure 3.6. ANSYS

results can also be used but since we have more data points using Matlab, the Matlab solutions are chosen to use here.

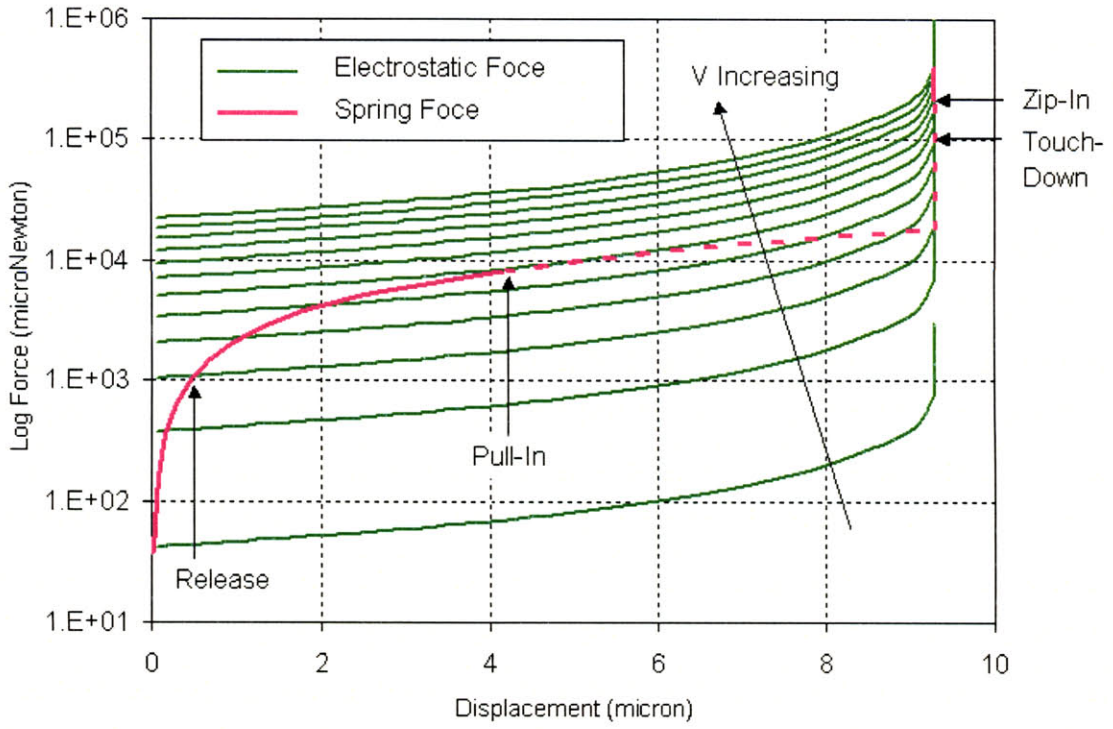


Figure 3.14. Electrostatic hysteresis of the zipping actuator.

The plot reveals the following. 1) The electrostatic curve intersects the spring force curve at two points, but only one point is stable. At the stable point, if deflection is slightly increased, the spring force should be larger than the electrostatic force in order for the restoring force to bring the structure back to equilibrium. If the electrostatic force would be larger, then the displacement will keep increasing until the structure collapses. 2) Pull-in occurs when the electrostatic force curve is tangent with the spring force curve. 3) As voltage keeps increasing beyond the pull-in point, touch-down occurs, followed by the zip-in stage. 4) As voltage starts to decrease, the outer-deflection stays the same. At the point where the vertical spring force line intersects the sloped one, release will occur

because that is not a stable point as explained earlier. In Matlab simulation, we are trying to find the release voltage by making this point a stable point. But because that's not the case, the Matlab solution fails to capture the condition of release, in fact. It is therefore not unreasonable that the release voltage predicted by Matlab is off comparing to ANSYS. Because the point is not stable, at release, the final outer-deflection will be where it's labeled on the plot.

3.5 Discussions

The differences between the Matlab model and the ANSYS model are summarized as the following. 1) The Matlab model considers the fulcrum as a shell and neglects the effect of its width at the joint, while the ANSYS model considers 2-D structures for both the fulcrum and the plate; 2) The Matlab model omits the contact mechanism between the plate and the bottom electrode, while ANSYS takes into consideration the contact stiffness between the two; 3) The Matlab model assumes parallel electrostatic field lines, while the ANSYS model solves Maxwell's equations and uses energy methods to derive the capacitances. By comparing the Matlab results with the ANSYS results, we will first verify the zero-moment boundary condition for the zip-in case, and then we will compare the electrostatic forces for both cases.

3.5.1 Boundary Condition

In the Matlab model for the zip-in case, because we have an extra unknown - the pin-down position, a fifth boundary condition is required. This boundary condition is a zero moment at the pin-down position. To verify this argument, we will look at the radial strain distribution at different cross-sections of the plate from ANSYS results. If a moment is present, uneven distribution of radial strain will be present.

In this example, an actuation voltage of 160V is used. The deflection profiles of the plate for both ANSYS and Matlab simulations are plotted in Figure 3.15. Note that in this simulation, a target clearance of 0.5 μm is used. To pin point the pin-down position, a zoomed-in plot of the deflection from 1350 to 1500 μm is shown in Figure 3.17. For ANSYS, the plot shows that the plate touches down onto the target plane at a radius of 1420 μm and penetrated into the target. At 1460 μm, it reaches the final depth. For Matlab, at 160V, the pin-down position is 1423 μm.

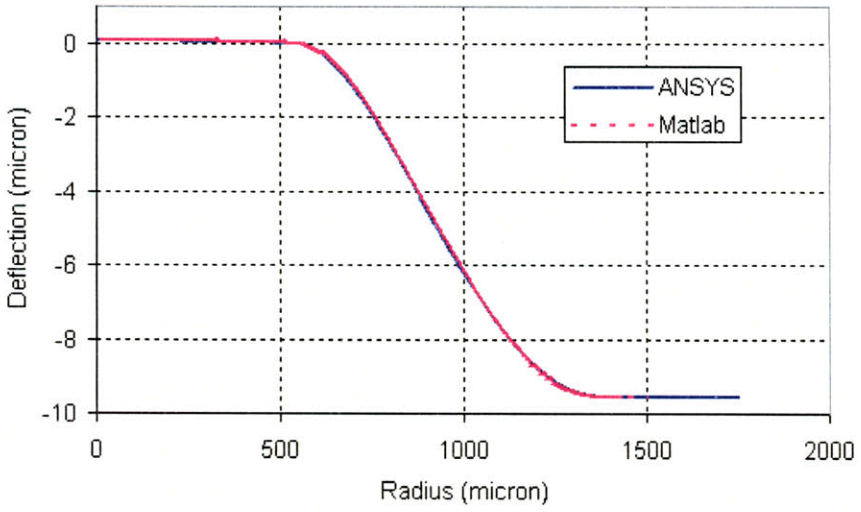


Figure 3.15. Deflection profile of the plate simulated with an applied voltage of 160 V.

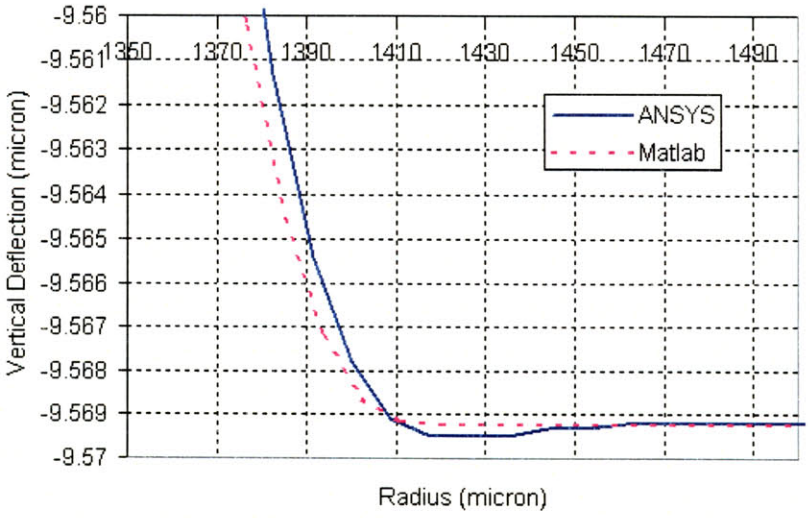


Figure 3.16. Zoomed-in plot of the deflection from 1350 to 1500 μm.

Figure 3.17 and Figure 3.18 show the plots of radial strain vs. plate thickness at different radius with a vertical strain division of 1×10^{-6}. At the outer edge, strain distribution is present. And as the radius moves inward, there is very small strain variation across the thickness, suggesting negligible internal bending moment. Figure 3.18 shows the plots for different radii from the pin-down position inward. In these plots, the vertical strain division is 1×10^{-4}. At a radius less than 1450 μm, the strain distribution starts to grow and becomes linear, corresponding to an increase of the internal bending moment. Using the strain plot, we can calculate that the total moment per unit length at radius 1420 μm is 1519.44 μN. If we would use this moment as the boundary condition for calculating the pin-down position for 160 V in Matlab, the new pin-down position is 1436 μm instead of 1423 μm. In conclusion, the contact between the plate and the bottom surface near the pin-down region imposes a finite internal moment at the region. However, this moment is rather small and does not significantly affect the result. Since the assumption of zero-moment boundary in Matlab results in good agreement with ANSYS, we conclude that the boundary condition is valid in our analysis.

In fact, other studies of zipping motion of a cantilever beam also demonstrate zero moment where the beam touches down on the substrate. In their calculation of the deflection and adhesion energy of a cantilever beam, Knapp and de Boer derive that the moment is zero throughout the touched-down length, except when there exists internal stress gradient in the beam, which would results in a constant internal moment throughout the beam [51].

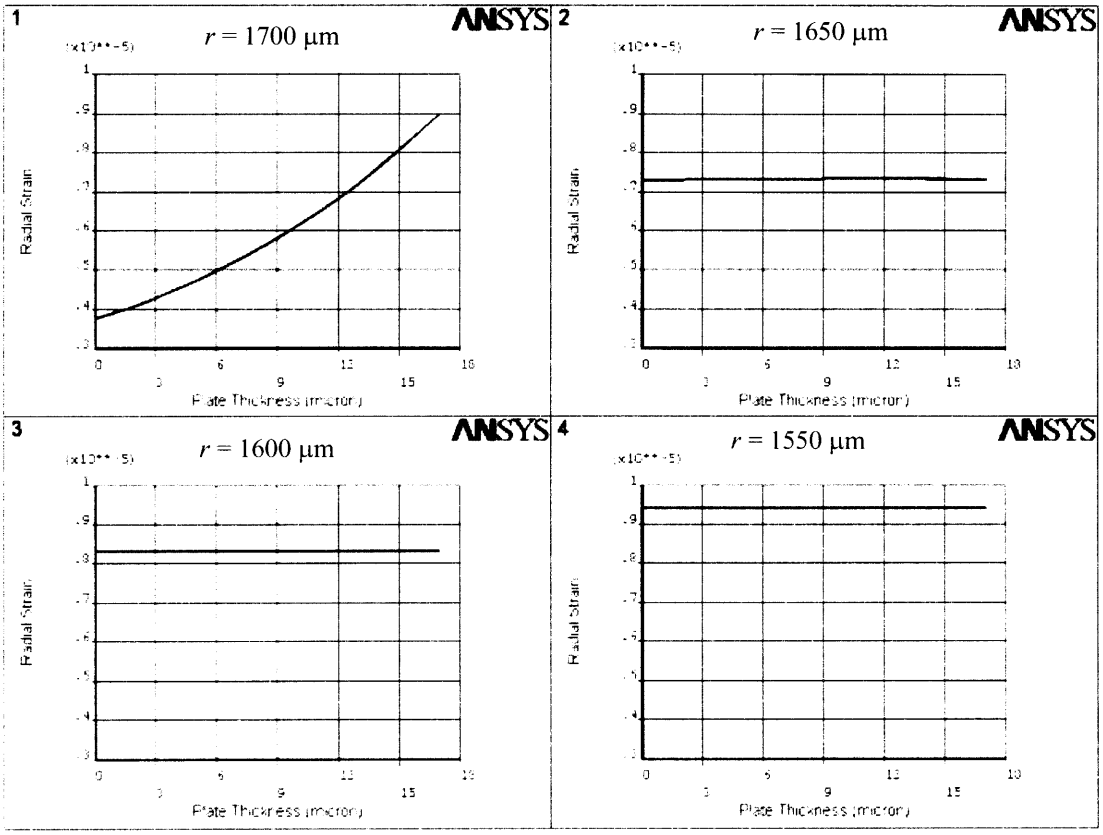


Figure 3.17. Plots of the radial strain vs. plate thickness for radius r = 1700, 1650, 1600 and 1550 μm.

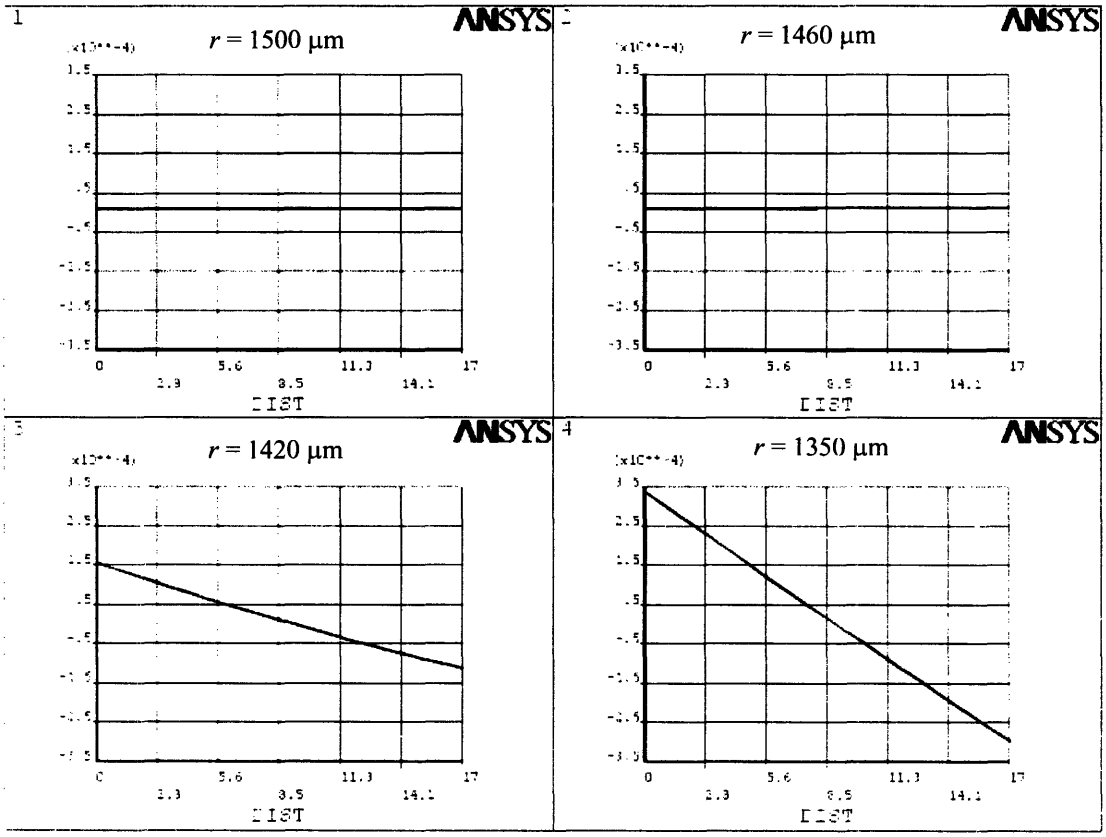


Figure 3.18. Plots of the radial strain vs. plate thickness for radius r = 1500, 1460, 1420 and 1350 μm.

3.5.2 Electrostatic Force

In the formulation of the actuator model, electrostatic force is exerted on infinitesimal parallel plates and the electric field lines are assumed to be parallel. However, since the plate bends during actuation, we know that the electric field lines are not necessary parallel. In this section, we will examine the effect of the parallel-plate assumption.

Using 160 V as the actuation voltage, we can find that the total electrostatic force acting on the plate after zip-in from the Matlab model is 2.042 N. For ANSYS, the resultant of vertical force is 2.04114 N and the horizontal force, 0.0016 N. The difference in the

total force from both simulations is minimal. These results suggest that the parallel-plate assumption used in Matlab is valid.

3.6 Capacitance Tuning

In this section, we will examine the capacitance tuning capability of the system using Matlab and ANSYS simulations.

So far we have looked at the displacement of the plate and the fulcrum. Knowing the shape of the plate from ANSYS allows us to calculate the capacitance change using Matlab. Figure 3.19 shows the capacitance change as a result of the plate deflection as voltage sweeps up and down. These curves allow us to see the general trend of change of capacitance. Plot a) shows the capacitance change of capacitor and b), that of the actuator. Note that because of hysteresis as explained in the previous section, the up-sweep and down-sweep curves do not coincide everywhere. Instead, they only coincide at voltages that are smaller than the release voltage and larger than the zip-in voltage. The potential use of a tunable capacitor with such characteristics is where frequency hopping between two frequencies is desired and at each frequency, small tuning is necessary. In this case, the capacitance can hop between 15.75 pF and 9.5 pF, and with a tuning range of -6.4% and -10.5% at each end by rough estimate. If electrostatic hysteresis is to be avoided, then the tuning range is limited to within each actuation stage. For example, within the before pull-in stage, the tuning range is -11.1% and within the zip-in stage, -10.5% (the number also depends on the actuation voltage in the zip-in stage). However, since a large voltage is needed to zip-in the actuator, it is not pragmatic for the device to operate in the zip-in stage, unless the device is originally zipped down as fabricated, as what we have fabricated. Notice also that the capacitance span of the actuator is much larger than that of the capacitor due to the larger size of the actuator.

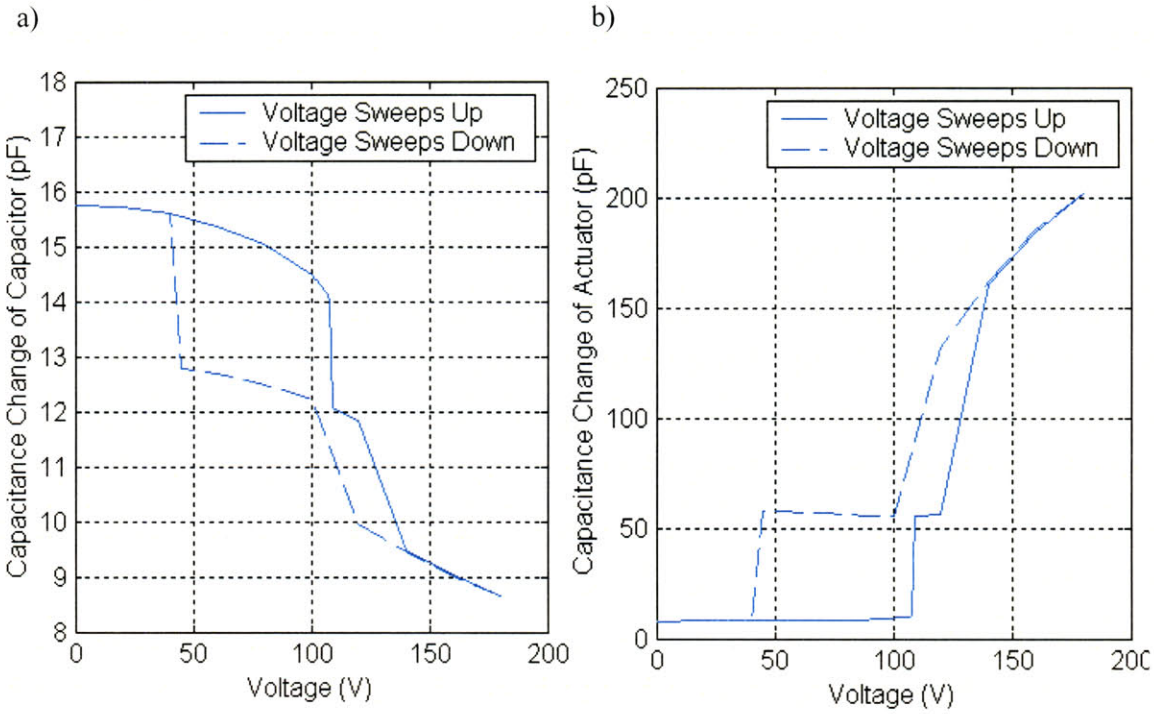


Figure 3.19. Capacitance change of the a) capacitor and b) actuator as actuation voltage sweeps up and down.

The sensitivity of capacitance change as the gap changes is a strong function of the thickness of the dielectric material, and in our case, thermally grown oxide. The thinner the oxide, the larger change is the capacitance given the same displacement. However, the thickness of the oxide is limited by dielectric breakdown at desired actuation voltage.

The self and mutual capacitances of the system is also simulated using the CMATRIX command macro in ANSYS. The ANSYS model used is shown in Figure 3.20. The model contains 3 conductors: the actuator bottom electrode, the capacitor bottom electrode and the silicon ground plate. A relative permittivity of 4.6 is used for the Pyrex glass region. In the non-actuated state, the capacitances are: C_{11}=7.72 pF, C_{22}=16.08 pF, and C_{12}=3.36 × 10^{-5} pF. The self capacitances of the capacitor and the actuator correspond well with the Matlab model. See Appendix D.3 for the ANSYS code.

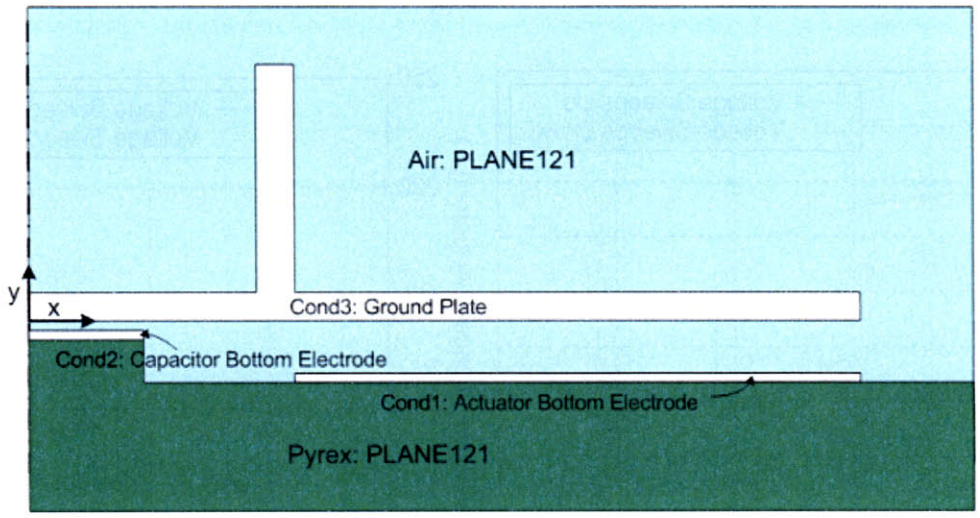


Figure 3.20. ANSYS model used in capacitance simulation.

3.7 Matlab Design Study

Now that we understand the mathematical model of the structure and have double checked the model with ANSYS, Matlab can be used to conduct parametric studies for the effect of the design parameters such as the fulcrum thickness, plate thickness or air gap thickness, to determine which are the most critical parameters. In the first study, we will set the plate outer radius at 1750 μm and we will find the pull-in voltage as a measure of the effect.

As explained before, because the fulcrum is effectively attached to the plate, part of the moment exerted on the joint is lost to the fulcrum. We can predict that the fulcrum thickness plays an important role because it affects its stiffness. With smaller fulcrum thickness, more moment will be transmitted to bend the center plate instead. Another direct result is the reduction of the pull-in voltage. In this study, a fulcrum thickness from 5-50 μm is used with 5 μm increment. The rest of the parameters are the same. The pull-in voltage vs. the fulcrum thickness is plotted in Figure 3.21 a), showing that the pull-in voltage dropped to 80 V for a 5-μm thick fulcrum. The moment transmission ration M3/M1 is

plotted in Figure 3.21 b), showing that the ratio is significantly higher when smaller fulcrum thickness is used. Accordingly, the center deflection increases from 47.1 nm to 2.07 μm when the fulcrum thickness changes from 50 μm to 5 μm. This is a gain of 44 times in displacement.

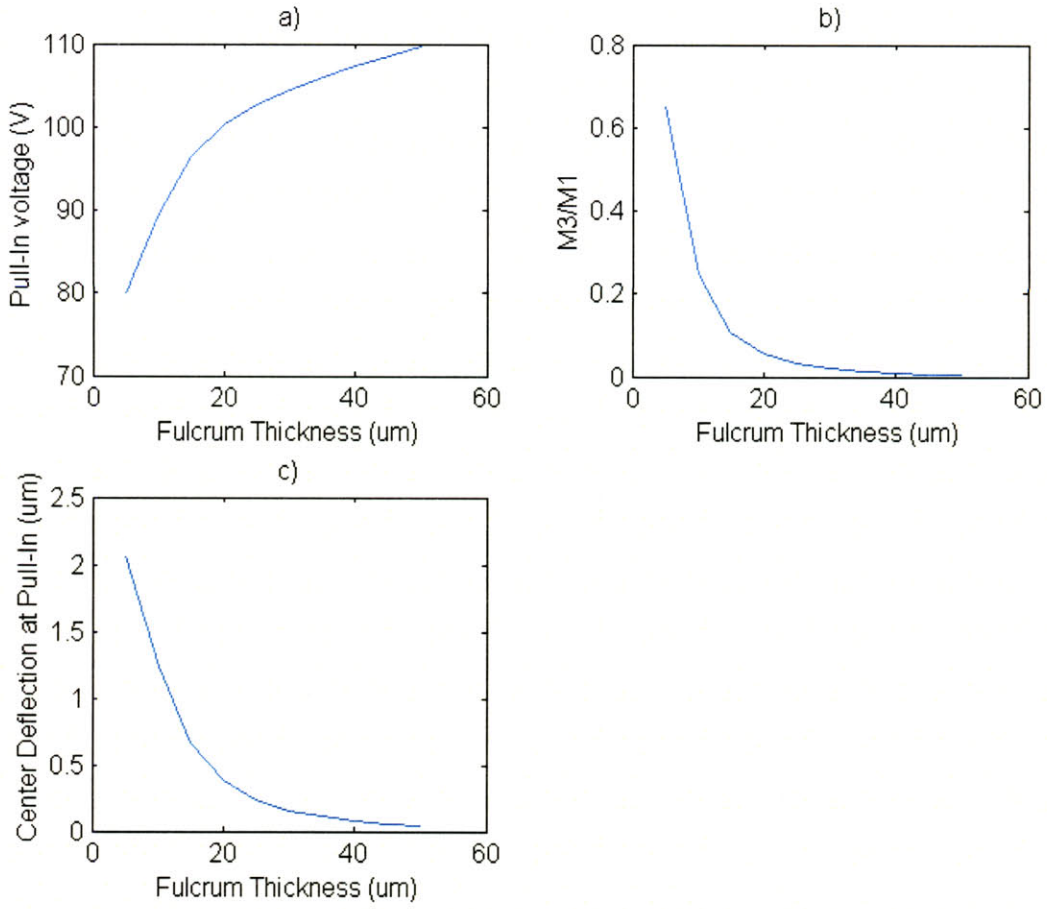


Figure 3.21. The effect of fulcrum thickness on a) pull-in voltage and b) the moment transmission ratio and c) center deflection.

Reducing the air gap of the actuator reduces the pull-in voltage. However, it also decreases the electrostatic force and the center displacement. Figure 3.22 shows that the pull-in voltage reduces from 110 V to 40 V as the air gap reduces from 10 to 3 μm. The center deflection, however, reduces from 41.6 to 8.2 nm. Unlike the case of the fulcrum thickness, there is a trade-off when selecting the air gap thickness in order to obtain

acceptable pull-in voltage as well as center displacement. Also unlike the case of the fulcrum thickness, which has an exponential effect on the outcome, the air gap thickness exhibits a more linear effect. Overall, we can say that the fulcrum thickness is a more heavily weighted factor for the center displacement while the air gap thickness is so for the pull-in voltage.

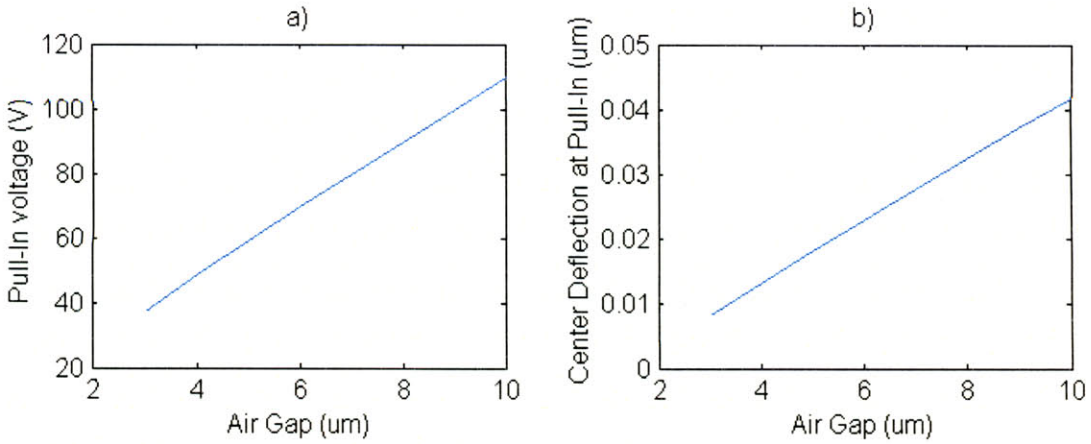


Figure 3.22. The effect of air gap on a) the pull-in voltage and b) the center deflection.

Combining the effect of the fulcrum thickness and air gap thickness, we can obtain 3-D plots of the pull-in voltage and center displacement, as shown in Figure 3.23. Two silicon plates with different thickness are used and the results are both displayed. To reduce the pull-in voltage, thinner plate, thinner fulcrum and thinner gap are desired. To increase the center displacement at pull-in, however, thicker plate, thinner fulcrum and thicker gap are desired. See Appendix C.6 for the Matlab script.

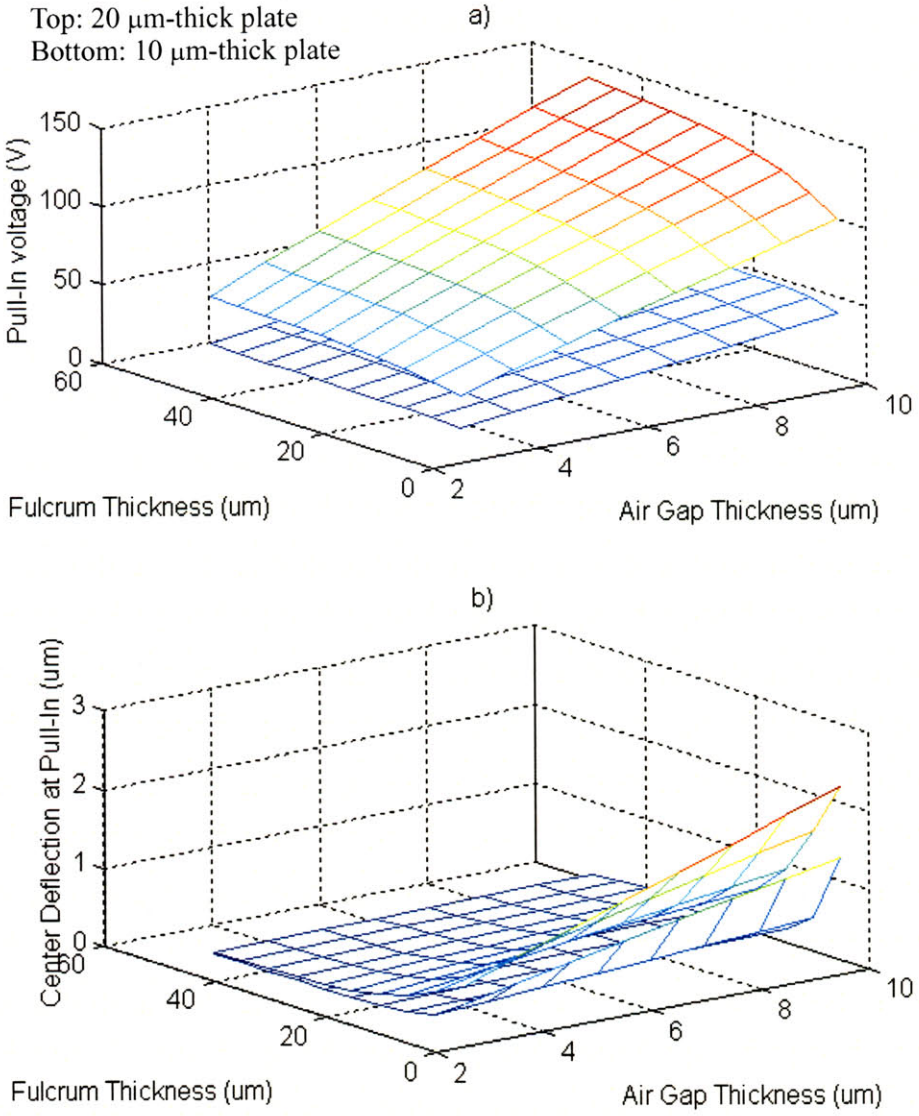


Figure 3.23. The combining effect of fulcrum thickness and air gap thickness for a) pull-in voltage and b) center displacement for two different plate thickness at a pin-down position of 1750 μm.

If we limit the actuation voltage to 40 V, and want to find out what are the possible design dimensions, we can plot the pin-down position and the center displacement as a function of fulcrum thickness and gap thickness as shown in Figure 3.24. If we would

limit the outer radius at 1750 μm, in order to maximize the center deflection, we would choose a 10 μm-thick silicon plate and a fulcrum thickness of 10 μm, an air gap of 9 μm to achieve a maximum center deflection of 375 nm.

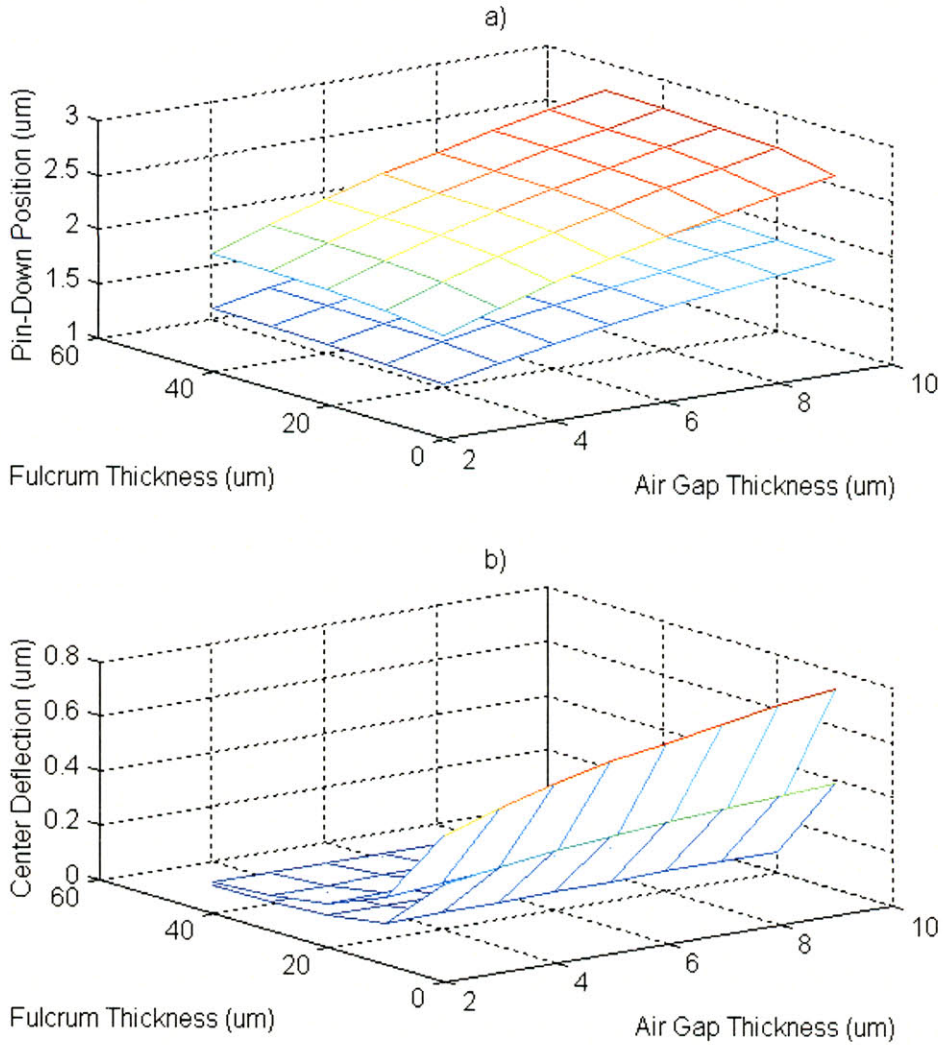


Figure 3.24. The effect of fulcrum thickness and gap thickness on a) pin-down position and b) center displacement at two different plate thickness using 40V.

3.8 Design Layout

The actual dimensions used in the mask layout for fabrication are listed in Table 3.4. Details on the dimensions and designs used for each device can be found in Table A.1.

Table 3.4. Dimensions used in the mask layout.

Item	Symbol	Value (μm)
Radius of capacitor	r_c	200
Radius of fulcrum	r_a	500/750
Thickness of fulcrum	t	50/35
Inner radius of actuator	a	500
Outer radius of silicon plate	b	1750/2000
Outer radius of bottom electrode	r_o	1700/1950
Thickness of the top plate	h	20/10
Air gap	g	10
Thickness of oxide insulator	c	0.27
Width of metal interconnect	m	100

3.9 Design with Slits

In order to reduce the stiffness of the plate and lower the actuation voltage, slits are cut from the outer plate as shown in Figure 3.25. In the mask layout, two designs are used, one has a cut of 300 μm long and the other, 550 μm, and both have 12 cuts.

Using a simple model by applying uniform pressure to the outer plate, we can simulate the effect of the slits using ProMechanica. In this case, a fulcrum width of 20 μm wide is used, and the plate outer diameter is 4 mm. A pressure of 1 atmosphere is used. It is shown that with 300 μm-long slits, the center deflection is 4.13 μm instead of 1.92 μm when there is no slit. Hence, a reduction of 2.15 times in stiffness is resulted. With 550 μm-long slits, a reduction of 2.43 times is resulted, corresponding to center deflection of 4.67 μm. These results show that cutting slits is an effective way of reducing the stiffness of the plate and hence the actuation voltage of the zipping actuator.

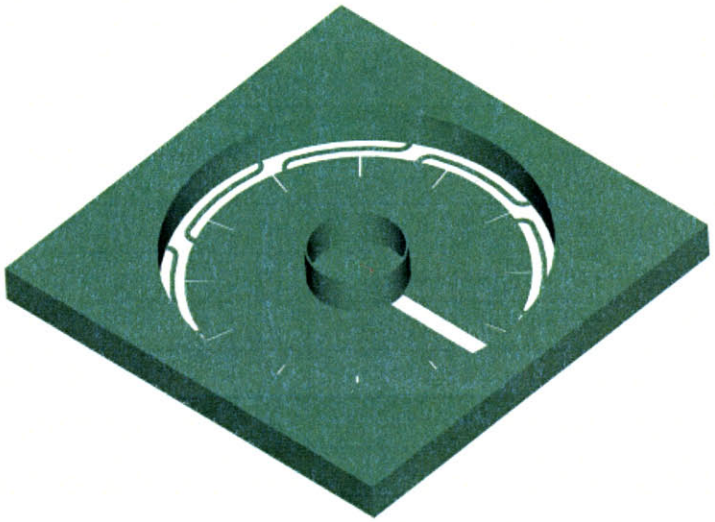


Figure 3.25. Design of the plate with slits cut at the outer plate.

3.10 Summary

In this Chapter, we model the fulcrum-plate structure using elastic plate theory and solved for the plate profiles as function of actuation voltage using Matlab boundary value problem solver. A finite element model using ANSYS is also created. Matlab BVP is well suited to solve multiple nonlinear differential equations with unknown parameters, and ANSYS is equipped to solve coupled physics problem as well as structures that involve contact mechanism. The simulations results using Matlab and ANSYS are in good agreement in the before pull-in and zip-in actuation stages of the electrostatic zipping actuator, confirming both models. Our simulations show that because of electrostatic hysteresis, the potential use of the design would be limited to within each actuation stages, i.e., within the before pull-in, touch-down or zip-in stages where jumping from one stage to the other is not the case, but because the most capacitance change occurs while the actuation is jumped from one stage to the other, the useful tuning ratio of the device is actually much

smaller as will be shown in the next chapter. However, if capacitance hopping is desired, a large capacitance jump could be obtained, but the actuation voltage will be limited to before release and after zip-in where there is no hysteresis in these regions. In other words, the hysteresis in the system could limit the use of the device, but it might also provide new opportunities. Using the Matlab model, we can perform design studies of the different parameters and obtain the optimal dimensions. On the other hand, with ANSYS, we could obtain a more realistic model for example, by using the actual fabricated shapes and dimensions, as will be shown in the next chapter.

Chapter 4

Testing Results

In this chapter, we will first present the test setup used, mainly the capacitance meter and the laser interferometry system that is used to measure the center displacement of the plate. Then the testing results using two different packages for both wafer-level-bonded and die-level-bonded devices will follow. The results from the first package turned out to be erratic but its lessons helped the design of the second package which allowed us to perform the experiments. As explained in Chapter 2, the wafer-level-bonded device has the plate initially touched down as a result of the anodic bonding process, and consequently, it only operates in the after pull-in stage. The die-level-bonded device, on the other hand, has the plate suspended, and hence it could operate across the before pull-in, touch-down and zip-in stages. The wafer-level-bonded device was tested more extensively and after so, its cross-section was obtained so that the actual fulcrum profile could be measured. Dimensions obtained from both SEM and Wyko measurements were used to construct a more realistic ANSYS model and the simulation results compared well with the laser interferometry measurements. On the other hand, the experimental results of the die-level-bonded device was limited to capacitance measurement because the device was debonded after those measurements and further testing was not available.

4.1 Test Setup

To measure the capacitance change of the actuated device, two types of impedance analyzer were used. One was a HP 4294A 110 MHz precision impedance analyzer which was used to scan the frequency and obtain impedance plots. Another was a HP 4284A 1 MHz LCR meter which was used to obtain spot impedance measurements. Both meters could apply internal DC bias up to ±40 V. A floating DC power supply (made of batteries) was used to supply DC voltage to the device. A laser interferometer system was used to measure the center displacement of the plate. The laser system will be described in the next section. A schematic of the test setup is shown in Figure 4.1.

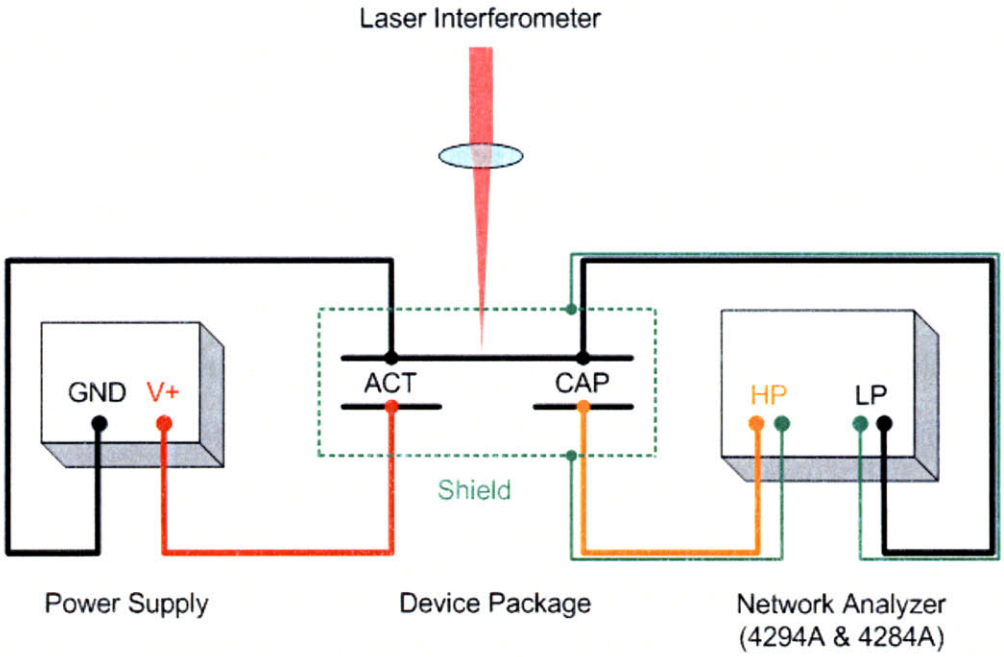


Figure 4.1. Schematic of the test setup.

As mentioned in Chapter 2, the silicon plate had no metal deposited on it and hence would act as the ground for both the actuator and the capacitor. During testing, however, we found that using a grounded voltage supply caused havoc to the impedance measurement. This lead to the creation of a floating power supply with a handful of batteries and a

potentiometer. The use of a floating voltage supply relieved some of the problems but added parasitics to the capacitance measurement.

4.1.1 Capacitance Measurement

We will present the capacitance measurement results without the use of a power supply and provide the capacitance model of the device.

The HP 4294A was used to scan the impedance across the terminals. Figure 4.2 shows the magnitude and phase plots when the high potential of the meter was connected to the CAP terminal and the low potential was connected to the silicon plate. The measurement was fitted with a series RC model with C=7 pF, and R=150 Ω, where the impedance and phase can be calculated by,

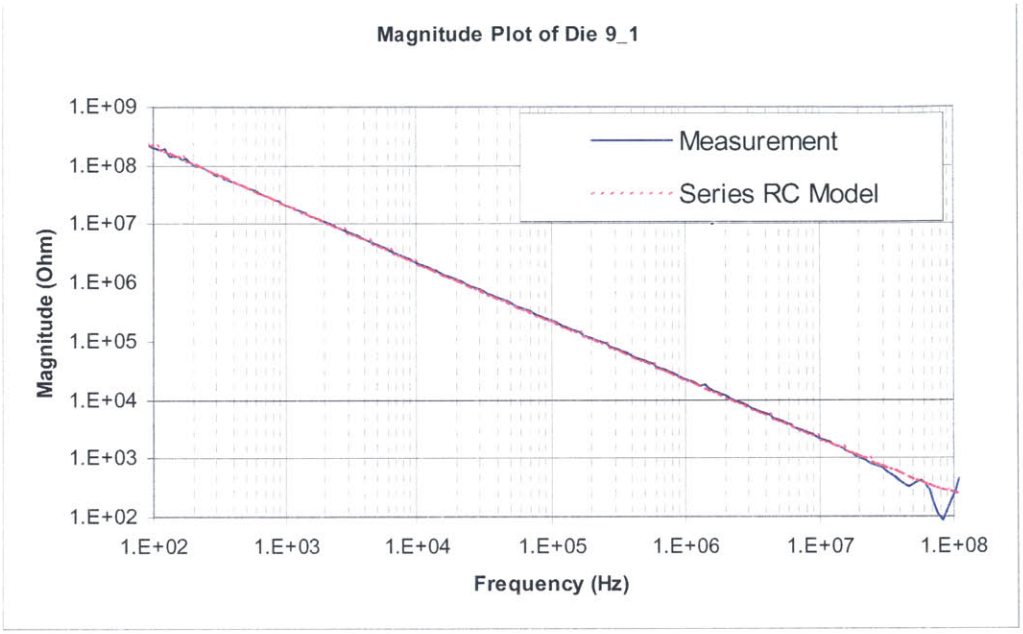
$$|Z| = \sqrt{\frac{1+R^2C^2\omega^2}{C\omega}}$$
$$\theta = \arctan\left(-\frac{1}{RC\omega}\right) \qquad (4.1)$$

The large resistance could be explained by the fact that silicon was used for the ground. The plot shows that at frequency lower than 10 MHz, the series model fits the measurement very well. We hence used the series model in subsequent capacitance measurements.

A simple capacitance model of the device is shown in Figure 4.3. There are three terminals for each device: the CAP terminal represents the central capacitor metal electrode at the bottom pyrex wafer, the ACT terminal represents the metal actuator electrode at the bottom wafer, and the 2 GND terminals (they are one terminal essentially) represent the silicon plate ground which has the same potential as the gold surface deposited at the back

of the chip (see Figure 2.15 for a cross section schematic of the device). Each of the symbol will be explained as follow.

a)



b)

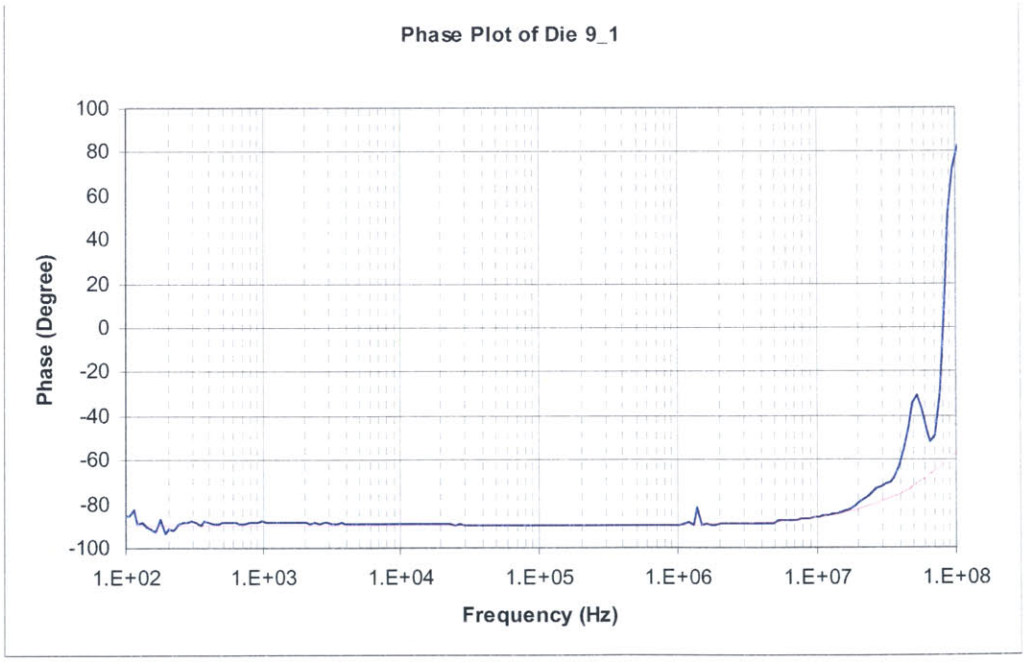


Figure 4.2. a) Magnitude and b) phase plots of the center capacitor comparing the measurement to a series LCR model.

C_{11}: capacitance between the silicon plate and the central capacitor metal surface;

C_{22}: capacitance between the silicon plate and the actuator metal surface;

C_{12}: mutual capacitance between the capacitor and actuator metal surfaces;

C_{p1}: parasitic capacitance between the capacitor metal surface and all other surfaces except the actuator metal surface;

C_{p2}: parasitic capacitance between the actuator metal surface and all other surfaces except the capacitor metal surface.

C_{11} is the designed tunable capacitor and its capacitance varies with the air gap. As mentioned in Chapter 3, the silicon plate was not flat as fabricated and its warp complicates the calculation of the capacitance; its value ranges from 1-16 pF. And for C_{22}, it ranges from 5-400 pF. As shown in Section 3.6, the mutual capacitance between the two metal surfaces is very small (on the order of 10^{-5} pF), such that it can be neglected. Our measurement further confirmed that it is so small that it simply couldn't be derived from measurement without showing a negative capacitance value. For this reason, we could omit it in the model. We can lump C_{p1} with C_{11} to become C_{cap}, and likewise, C_{p2} and C_{21} can be lumped to become C_{act}. The simplified capacitance model is shown in Figure 4.4. For our measurement, we could only measure C_{cap} and C_{act}, and the value of C_{11} and C_{22} are not known directly.

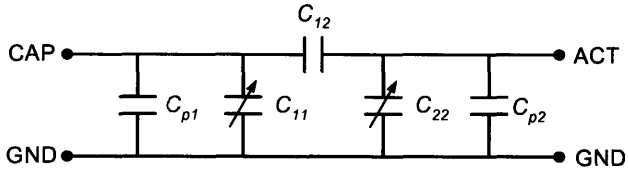


Figure 4.3. Capacitance model of the device.

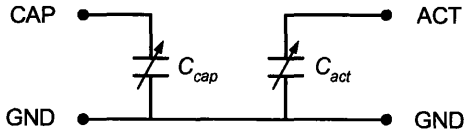


Figure 4.4. Simplified model.

Because an electrical connection is made through gold-coated silicon, a metal/semiconductor interface is inevitably present where the contact is made. This will present an

extra parasitic capacitance in the ground line. And since no potential difference is applied between the metal and silicon terminals, the diode is in thermal equilibrium, regardless of the external voltage applied to the actuator during operation. We can find that the depletion capacitance in this case to be about 82 nF. Since this capacitance is in series with the capacitance of the device capacitor, and the capacitance of the device is on the order of 10 pF, the diode capacitance affects about 0.01% of the measurement and hence could be neglected in our capacitance model.

4.1.2 Displacement Measurement

The mechanical displacement of the silicon plate was measured using a Zygo Motion Interferometer (ZMI) system. For details on the system, please refer to the Zygo manual. A brief description of the system is presented next.

4.1.3 The ZMI System

The ZMI system consists of a laser head, an optical probe and a ZMI 2000 measurement board. The laser head uses a Helium-Neon source that generates a 3-mm diameter beam with two orthogonally polarized frequencies. One frequency is 20 MHz higher than the other. The nominal vacuum wavelength of F_1 is 632.991501 nm and F_2 is 632.991528 nm.

The optical probe uses a lens to focus the laser beam onto the moving test object. The one we used has a focus length of 154.6 mm and a linear displacement range of ±0.25 mm. It consists of a polarization beamspitter, a quarter waveplate retroreflector assembly and a lens assembly, as shown in Figure 4.5. The laser beam (with two orthogonally polarized frequencies) enters the polarization beamsplitter and is divided into two perpendicular beams. One beam hits the retroreflector and is reflected back to the beamsplitter where its polarization rotates by 90°. Another beam passes through the lens assembly and is

focused onto the test object and then reflected back to the beamsplitter where the two beams are recombined. The recombined beams enter a fiber optic receiver, which converts the counts of interference fringes into an electrical signal and is processed by the ZMI measurement board. If N is the counts of interference fringes, λ is the wavelength of the measurement beam in air (which could be manually compensated for environmental conditions such as temperature, pressure and humidity at the time of measurement by the data acquisition software), then for our system, the displacement p can be expressed as,

$$p = \frac{N\lambda}{1024} \tag{4.2}$$

The sign of the output signal depends on the measurement beam used, which in turn depends on the setup of the interferometer. In our case, we used F_2 as the measurement beam, and the sign is positive when the test object is moving away from the laser source. A ZMI software was used for data acquisition and interface. Because of the limitation of the measurement board, dynamic data acquisition is not available. Our data acquisition rate is limited to about 0.2 sec/data.

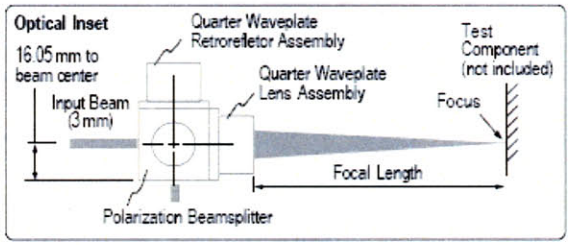


Figure 4.5. Schematic of the optical probe. (source: ZMI optical probe accessory manual OMP-0238B)

4.1.4 Laser Setup

The challenge in preparing the laser interferometer experiments is aligning the laser to the optical probe and test object. The optical probe must be mounted so that the bottoms or sides are parallel or perpendicular to the plane defined by the laser head to within ±1

degree. The user manual also states that when performing alignment, it is necessary to adjust the position of the probe, and it is important to clear the optical probe of thermal fluctuation or machine vibrations. The test object must be placed at a distance as close as possible to 154.6 mm to the assembly.

Originally, a fixture for the optical probe was designed such that it sat on a linear stage, which allowed the probe to be displaced toward or away from the laser head. The linear stage fitted into a tilt stage, which provided pitch and roll movement. Furthermore, the height of the stage could be adjusted from the air table by a thumb screw on the side of a half inch diameter support post. The design of the stage is shown in the schematic in Figure 4.6. Although optical alignment was successful with this design, it was found that the noise level in the measurement was too large to be acceptable. This might be due to the fact that the added degrees of freedom compromised the stiffness of the fixture and hence the ability to isolate mechanical vibrations.

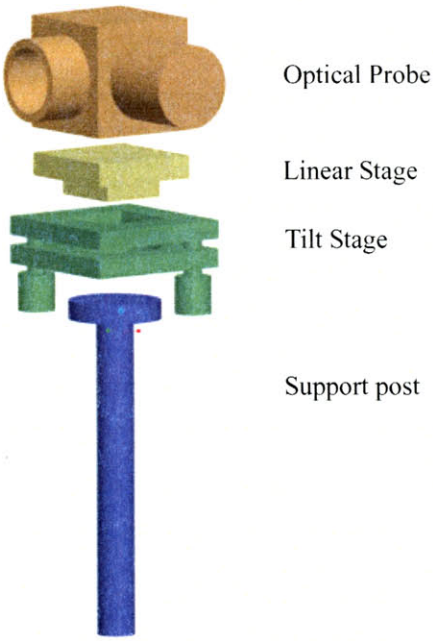


Figure 4.6. Exploded view of the original design for the probe fixture.

A second design turned out to be a lot simpler. It had one machined aluminum piece onto which the optical probe was bolted onto and its position was not adjustable. With this fixture, the noise was greatly reduced and alignment turned out to be easier and accurate as well. A schematic of the final experimental setup can be seen in Figure 4.7.

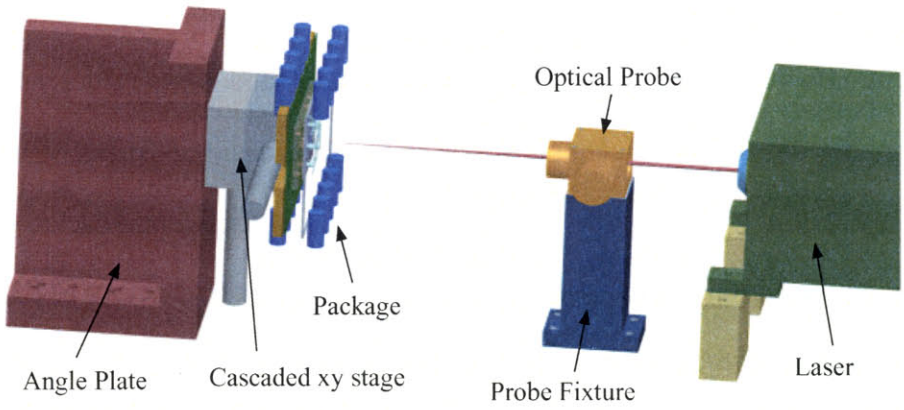


Figure 4.7. Schematic of the laser interferometer experiment set up.

We had three devices in one single die and we wanted to be able to adjust the position of the package laterally. The ability to adjust the height of the package would also be necessarily during alignment. To achieve movement in both directions, the package was mounted on top of a xy stage. In our case, we cascaded two one-axis stages to achieve the two-dimensional motion. Finally, the xy stage was mounted to a 20 lbs cast iron angle plate for rigidity. During alignment, metal shim might be needed to place underneath the angle plate to provide tilting, while yawing the angle plate before tightening the bolts on the air table might be necessary as well. But because the adjustment required was usually small, it was manageable with the angle plate.

During testing, it was found that thermal drift could be a severe problem in the output signals. This could be improved by 1) shielding the laser path by a plastic tubing and 2)

cover the whole setup inside a box made by thermally insulating materials. Thermal drifts were reduced significantly after these approaches.

4.2 Testing Results

As mentioned in Chapter 3, we have tried three different packages for the device. The first two had the device sandwiched between two printed circuit boards and were designed to house the Pogo Pins for electrical connection from both top and bottom sides, as well as be able to assemble die pieces by clamping. The first package did not produce meaningful results and we will not present it here. Testing results using the second package were not conclusive and the lessons learned drove us to develop a third package. We will focus on the testing results with the third package in the next section. We also mentioned that the test devices were assembled in three different ways: one was by wafer bond in the wafer-level, one by die-level, and one by clamping. Testing results for the first two assembly types will be the focus of the next sections.

As shown in Figure 2.23, the double-PCB package has the die sandwiched between two PCB's in order to house the Pogo pins needed for both sides of the die. With the top PCB blocking the view of the die, finding the center of the plate for laser interferometry measurement became a daunting task. Ideally, we could use the xy stage to scan the package horizontally and vertically to find the local minima for both directions, where such a minima was undoubtedly the center of the plate. However, looking for the minima was not a trivial task. Any particle residing on top of the plate would deflect the laser beam and result in misalignment of the reference and measurement beams, and the same applies if the change of height was too steep. As a result, continuous profiles were not always achievable and readjustment of alignment was needed. Furthermore, because the laser interferometer system was very sensitive to movement, turning of the knobs of the xy

stage inevitably exerted some stray displacement, which could cause confusion, if not mistake, in the judgement of the center. In summary, testing with the double-PCB package is not conclusive, due to 1) the top Plexiglas housing obscured the view of the device and locating the center by relying on the laser data was not reliable, and 2) the ground metal deposited on the PCB could interfered with the real actuation signal. For these reasons, a new package was devised as mentioned in Chapter 3 and we will present the testing results using the new package in the following sections.

With the single-PCB package, a picture of the test setup is shown in Figure 4.8. The package and the setup have been discussed before and will not be repeated here. The new package proved to have resolved the problem aforementioned with the old package and we are able to compare the testing results with theories. These results will be demonstrated below.

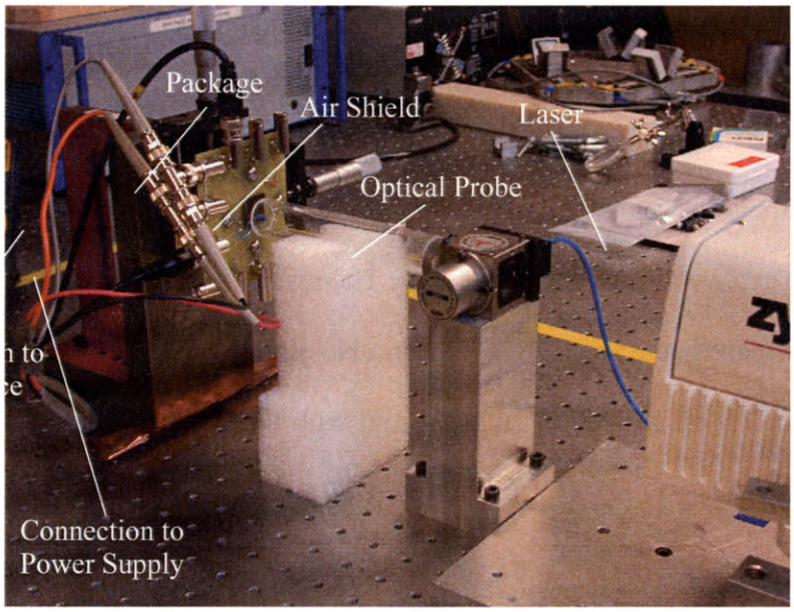


Figure 4.8. Picture of the test setup with the new package.

4.2.1 Wafer-Level Bonded Device

For the wafer-level assembled device, the plate touched town on the bottom electrode after assembly and hence the device only operates in the touch-down and zip-in stages. For this assembly method, device 9_1 was tested and the results will be presented here.

4.2.1.1 Capacitance Measurement

In this test, we used the HP 4294A to measure the capacitance change of both the CAP and ACT terminals by using the bias voltage from the meter. Elimination of the power supply reduces the parasitic capacitance that it introduces. The package is calibrated using the two bond wires as shown in Figure 4.8. It is worth noting that there was no apparent difference of the capacitance measurement between the old package and the new package.

We connected the CAP terminal to high potential and GND terminal to low potential and measured the capacitance change by applying bias. The oscillation frequency was 100 kHz. Bias from - 40 V to 40 V and then from 40 V to -40 V was used and 0.5 sec of delay between each data point was used, enough for mechanical equilibrium to occur. Note that in between, the bias was turned off when data was being saved and hence no voltage was applied. The cycle was then repeated twice. The results are shown in Figure 4.9. The measurement compared with the HP 4284A was also plotted. With the 4294A, the capacitance changed from 7.9 pF to 15.0 pF at 40 V, and with the 4284A, it changed from 7.6 pF to 14.8 pF.

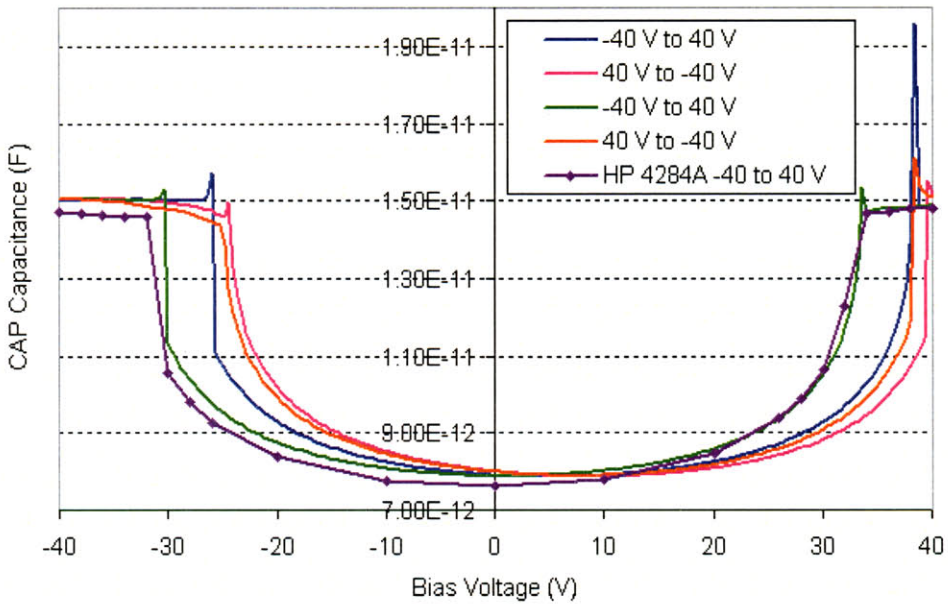


Figure 4.9. Capacitance of the capacitor measured by HP 4294A as bias voltage scans from -40 V to 40 V, then 0, and then 40 V to - 40 V twice, compared with measurement by HP 4284A.

From the plot, we observe that 1) the pull-in voltage is lower when voltage is negative or in other words, the curves are shifted toward the positive side. This is consistent with the fact that the positive charges such as the sodium and boron are trapped in the oxide. Hence, when the GND terminal is connected to high potential, lower voltage is required to actuate the CAP plate. 2) The release voltage is higher than the pull-in voltage. This may seem strange, because for the case of parallel plate actuator, when electrostatic force starts to decrease, it will decrease up to the point where the electrostatic force is less than the mechanical restoring force, then the plate releases. A detailed explanation of the hysteresis for the parallel plate case can be found in [52]. The release voltage in this case is always less than the pull-in voltage because the force is always linear with displacement. However, this is not necessarily the case for our capacitor. Figure 4.10 shows the actual geom-

etry of the center capacitor. The center plate deflects upward as shown in Figure 4.18. And because the initial capacitance is closed to 8 pF, we can derive that the bottom plate is very close to the top plate, as shown in Figure 4.10. When this capacitor is used as actuator, there are two stages of actuation. Stage 1 is the pull-in stage to close the minimum gap. Stage 2 is more complicated. When voltage keeps increasing, the center will continue to pull down and cause the plate to saddle, changing the mechanics of the plate. Therefore, beyond the pull-in point, the force-displacement curve changes shape. Our tests show that if we stop increasing the voltage as soon as pull-in occurs, and start to reduce the voltage, then the release voltage is lower than the pull-in voltage. On the other hand, if we keep increasing the voltage after pull-in beyond a certain value, then when we reduce the voltage, the new release voltage is larger than the pull-in voltage. This suggests some kind of bistable behavior in the plate. However, since we are not interested in using the capacitor as the actuator, we will not study what exactly happens here further.

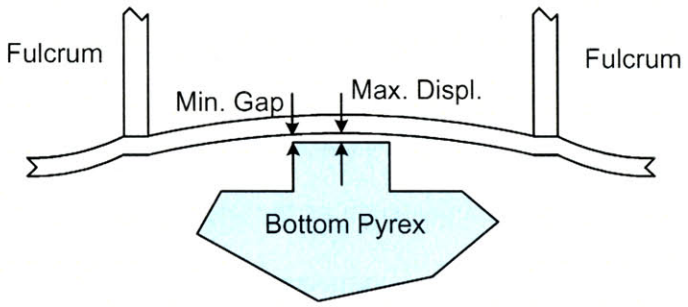


Figure 4.10. The actual geometry of the capacitor as predicted by the Wyko image and initial capacitance.

It is also observed that the capacitance changed from about 7.9 pF to 7.6 pF when the package was put on top of the xy stage that's made of metal. Wrapping the stage with insulating tape did not help the situation very much. We have to accept such parasitic in the capacitance measurement.

Next we connected the ACT terminal to high potential and GND terminal to low potential and measured the capacitance change by applying bias. Figure 4.11 shows the measurement data. The capacitance changes from 62.2 pF to 65.1 pF, corresponding to the prediction between the touched-down to zip-in stages in Figure 3.19 b). Note that the curves are also shifted slightly to the right as in the case of the capacitor. Furthermore, because there is no pull-in in this case, no hysteresis is observed.

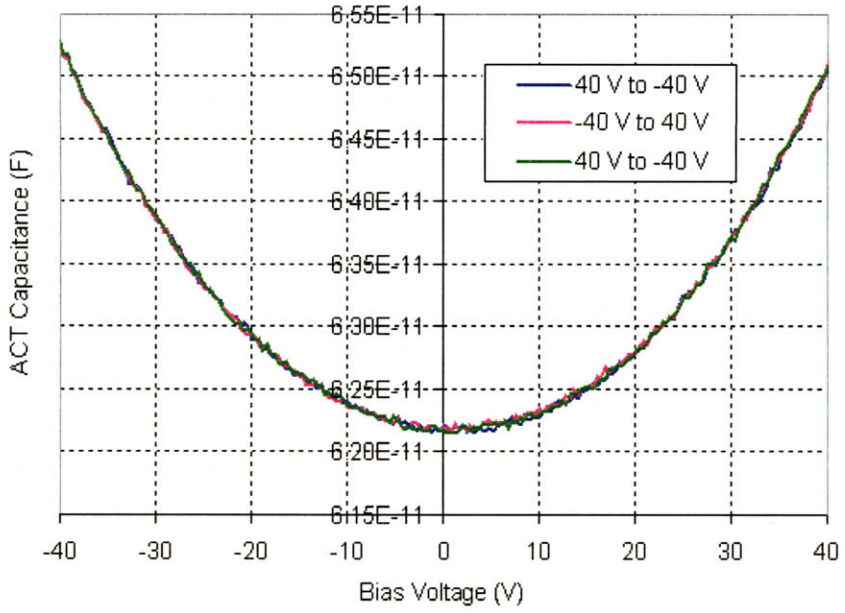


Figure 4.11. Capacitance of the actuator measured by HP 4294A as bias voltage scans from 40 V to -40 V, then 0, and then -40 V to 40 V, and repeat to -40 V again.

4.2.1.2 Laser Interferometer Results

Because the top pcb is eliminated in the new package, aligning laser to the center of the device was done by eyes using the following procedure. The laser was first shined on the top side of the fulcrum at the outer edge, then on the bottom of the fulcrum at the outer edge. This could be done because the laser path through the top Pyrex wafer could be easily seen when it shined outside of the fulcrum. We then calculated the median of the dis-

tance and translated that distance vertically. That became the center in y direction. Repeated for the horizontal x and then again the vertical y axis and the new location should be very close to the real center. An error on the order of 20 μm was estimated, which is less than the thickness of the fulcrum (50 μm) itself. Such an error should result in negligible displacement error for our measurement. Furthermore, we estimated that the actual distance from the lens to the plate could be off by 0.5 mm due to machining tolerance and thickness tolerance of the various packaging and mounting pieces. This would result in a 10-μm laser diameter at the plate. In other words, we are averaging the displacement of the plate for a 10-μm diameter area.

We started by measuring the center deflection when bias voltage was applied to the CAP and GND terminals as before using HP 4284A. In order to eliminate charging of the oxide, in these tests, only voltage sequence from -40 V to 40 V was applied. The raw data of two different tests is plotted in Figure 4.12. Plotted on the left axis is the displacement measured by the laser interferometer and plotted on the right axis is the bias voltage applied at each interval. Obviously, test 1 has fewer thermal drift during testing while test 2 was overcasted by downward drift. The displacement fluctuation for both cases was 3 nm.

To obtain the displacement, each step height in the displacement curves was obtained by subtracting the averaged values on both ends using 10 or more data points depending on the degree of the drift. And then the steps were added up to obtain actual displacement data. The displacement is plotted against the bias voltage in Figure 4.13 together with the capacitance values for the two tests shown in Figure 4.12. Repeatably, the capacitance changes from 7.65 pF to 14.75 pF at 40 V with ±0.05 V error, measured at 100 kHz. And

the displacement for both cases is 130.0 nm with ±1.5 nm error. Test 2 shows that the pull-in voltage is 32 V while the release voltage is -30 V.

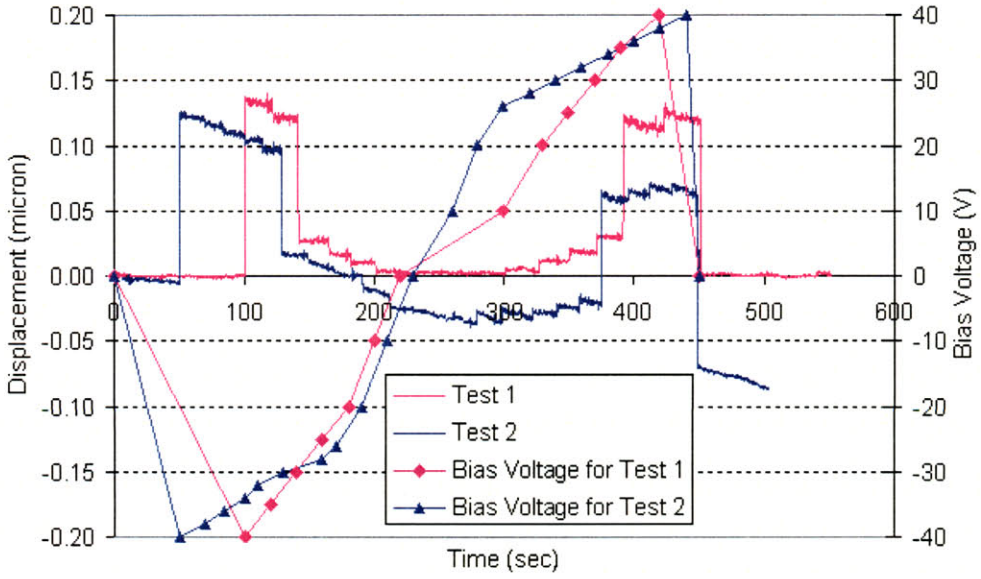


Figure 4.12. Displacement of the plate center measured using the laser interferometer as bias voltage is applied to the CAP and GND terminals for two tests.

In order to study the pull-in and release voltages of the capacitor more thoroughly, cyclic tests by applying voltage from -40 V to 40 V and back to -40 V as well as from 40 V to -40 V and back to 40 V were performed. All tests showed consistently that when voltage is positive, the pull-in voltage is between 30 and 32 V and the release voltage is 36 V, and when voltage is negative, the pull-in voltage is -26 V while the release voltage is -30 to -32 V. The pull-in voltage in the negative side is less than that in the positive side as expected. And in all cases, the release voltage is greater than the pull-in voltage as explained previously. This is also the case when voltage was applied from 0 to 40 V and back to 0 or 0 to -40 V and back to 0.

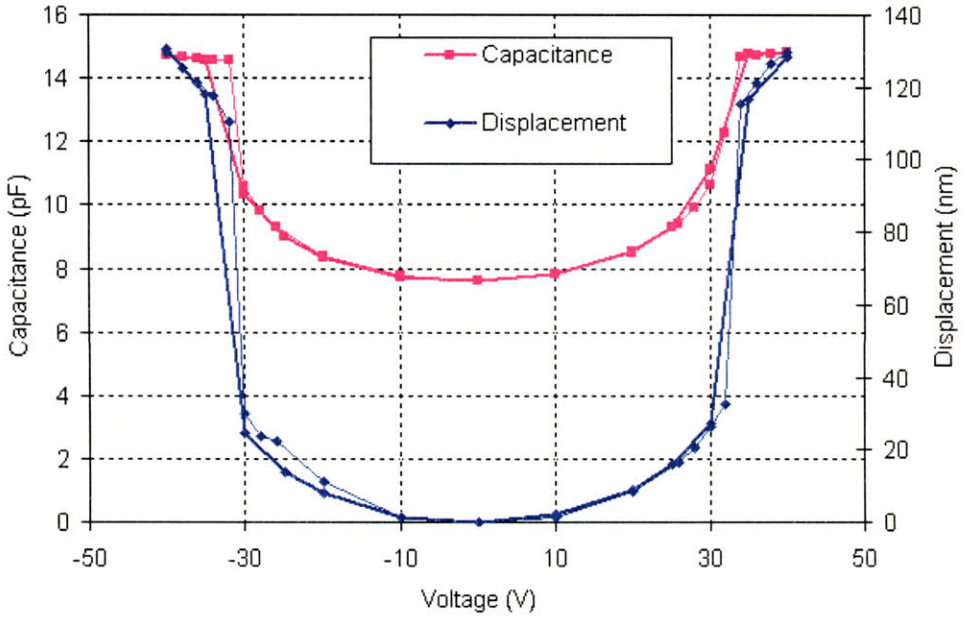


Figure 4.13. Capacitance change and center displacement when bias voltage is applied between the CAP and GND terminals; the thicker lines are for test 1 in Figure 4.12 and the thinner lines are for test 2.

Next we applied bias to the ACT and GND terminals and measured the center displacement as well as capacitance change of the CAP. For this test, we had to use the external power supply to apply voltage to the ACT, and we used the HP 4284 A to measure the capacitance at 100 kHz. Figure 4.14 shows the raw data from the laser interferometer for two tests. Test 1 scanned the voltage from 0 to -65 V while test 2 scanned the voltage from 65 V to 0. Note that both testing data have inherent drifts and interpretation of the actual displacement was done as in the case for the CAP.

The extracted displacement vs. applied voltage is plotted in Figure 4.15. Plotted in the same figure also is the capacitance change. Note that after the external power supply was plugged in, the capacitance of the CAP changed from 7.65 pF to 7.35 pF, affecting the reading by 3.3%. Again we accepted the parasitic caused by the power supply and went

ahead and measured the change of capacitance. The CAP capacitance changed from 7.35 pF to 6.89 pF at 65 or -65 V, with a tuning range of 6.3%. The plate center displaced 25 nm when voltage was increased gradually from 0 to -65 V and 27 nm when it was switched to 65 V. Note that an error of 3 nm in the laser displacement measurement is expected so the displacement for both cases overlap. The actuator broke down at 70 V, corresponding to an electrostatic field strength of 2.6 MV/cm, which is closed to, but lower than, the reported value of 3 MV/cm.

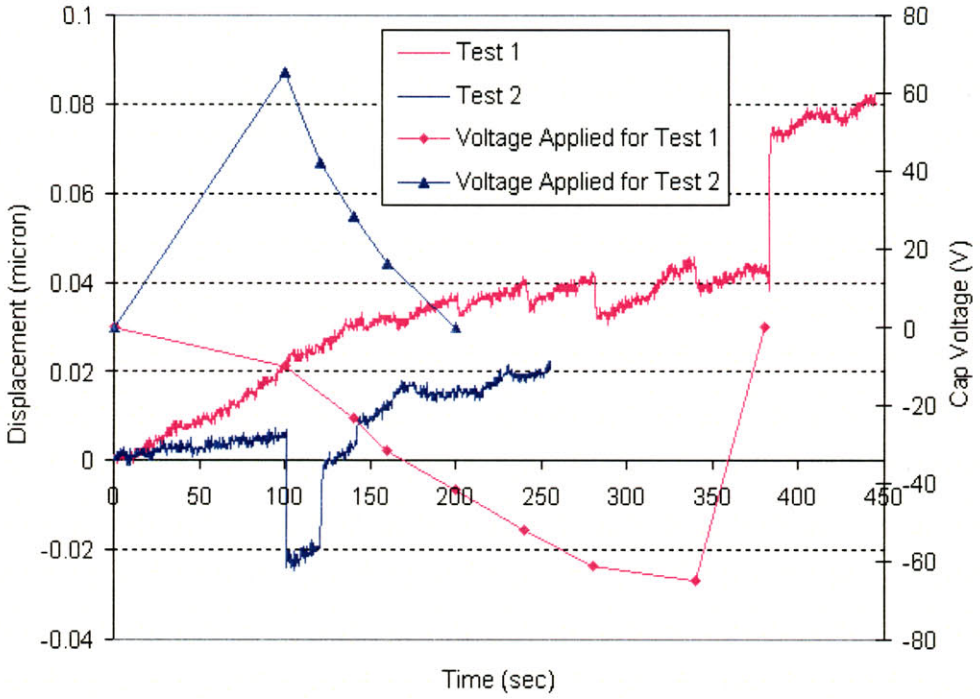


Figure 4.14. Displacement of the plate center measured using the laser interferometer as bias voltage is applied to the ACT and GND terminals for two tests.

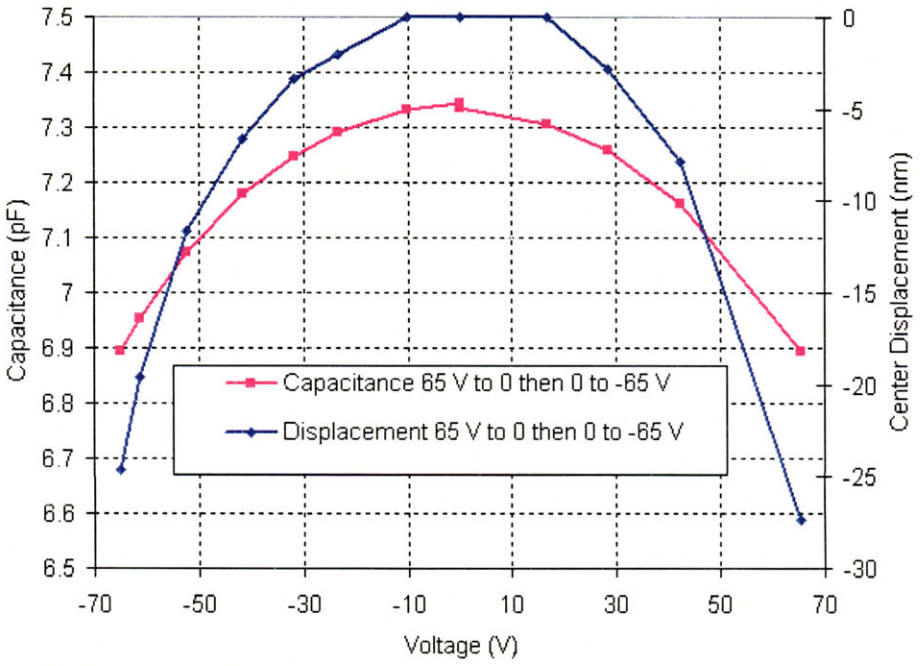


Figure 4.15. Capacitance change and center displacement when external voltage is applied between the ACT and GND terminals. In the plot, test 1 and test 2 as shown in Figure 4.14 are plotted the same color.

4.2.1.3 Comparison Between ANSYS and Experiment

After the experiments, die 9_1 was die-sawed across the middle of the fulcrum and SEM photo of the cross-section was obtained as shown in Figure 4.16. As seen in the figure, the fulcrum has tapered profile, with the top being 46 μm wide and the bottom, 12 μm.

Besides the fulcrum profile, other factors that we would want to include in the ANSYS model are illustrated in Figure 4.17. These include the anisotropic elastic properties of silicon, the residual stress in the silicon plate with thermal oxide, the initial deflection and the pressure differential applied to the center plate because of the anodic bonding process. Next we will address these issues and explain how each values are obtained in the ANSYS model.

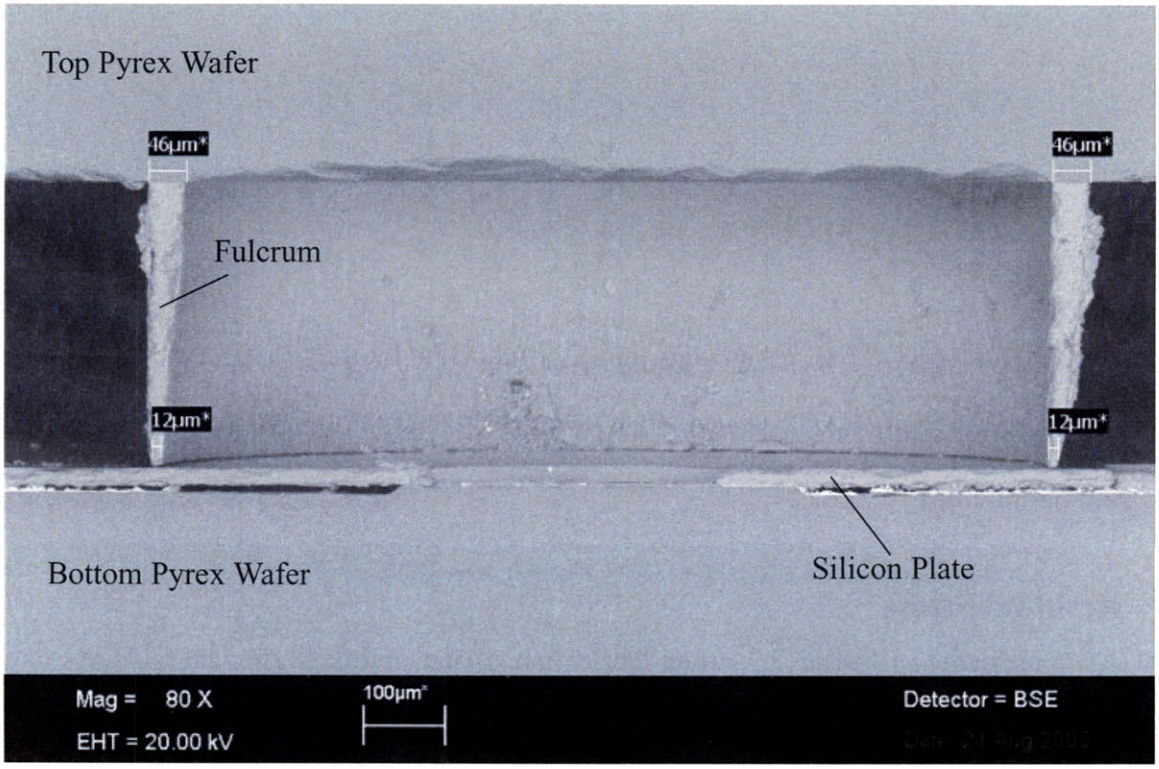


Figure 4.16. SEM photo of the cross-section showing the actual profile of the fulcrum.

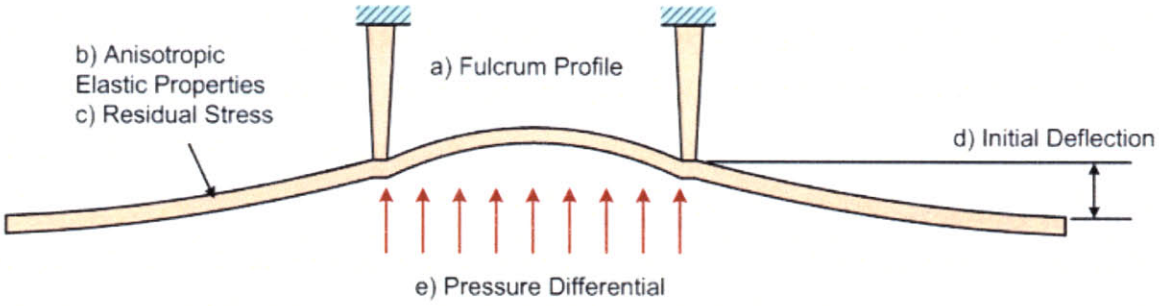


Figure 4.17. The factors that are considered in the ANSYS model for the wafer-level-bonded device.

Anisotropic Elastic Properties

Because single-crystal silicon is a cubic material, the stiffness coefficients of silicon can be described using three independent quantities [53],

$$C = \begin{bmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{bmatrix} \quad (4.3)$$

where C_{11} = 166 GPa, C_{12} = 64 GPa, and C_{44} = 80 GPa. In order to simulate the properties of anisotropic material, instead of PLANE82, PLANE183 element is used for the plate and the fulcrum.

Residual Stress

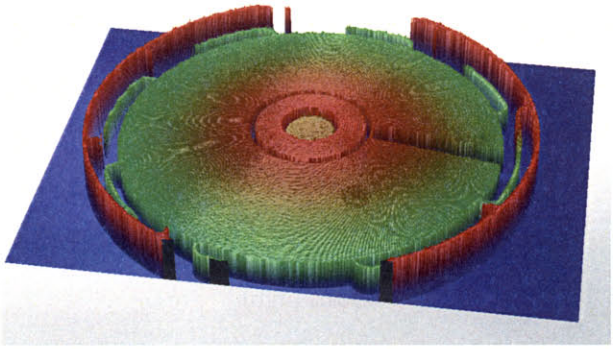
As explained in Chapter 2.3, after fabrication of the middle wafer, the silicon plate is bowed. In Figure 2.10, the cross-section of the plate when the fulcrum is detached shows that the bow of the plate is about 0.5 μm. In ANSYS, we can simulate the initial stress using a uniform pressure that is applied to the plate. It is found that about 1/500 ATM of pressure difference is enough to result in the 0.5 μm bow. The residual stress is very small such that it is almost negligible.

Initial Deflection After Fabrication

An image of the plate of device 9_1 using the Wyko profilometer is shown in Figure 4.18a). A cross-section is shown in Figure 4.18b). As explained before, the center dip is an artifact that is caused by an etched pit in the top Pyrex wafer used. We can translate the center area upward to obtain a curve that should be more realistic as shown in Figure 4.19, where the curves are centered and zeroed at the middle of the fulcrum. This only shows one cross section. Because the plate is not exactly axisymmetric, and also because of the reduced resolution caused by the red light filter with the Wyko profilometer, we estimate

that the outer deflection of the plate is 8.3 ± 1.0 μm after taking an average of 20 cross sections. The initial gap, however, must be greater than the outer deflection because of roughness of the surface and possibly particles on the surface. We estimate that the air gap is on the order of 9.3-10.1 μm and we will show that the displacement is very sensitive to the initial air gap.

a)



b)

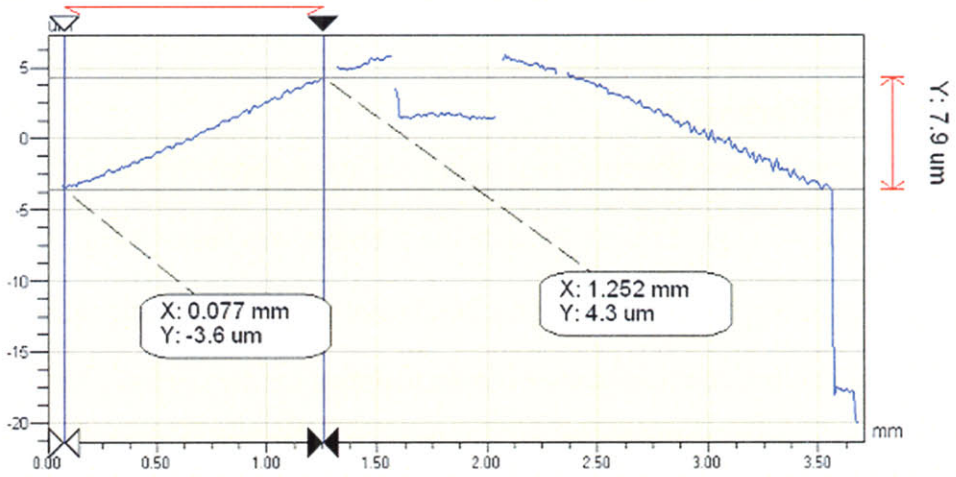


Figure 4.18. Deflection of the plate of device 9_1 using the Wyko interferometer showing a) 3-D image and b) a cross-section.

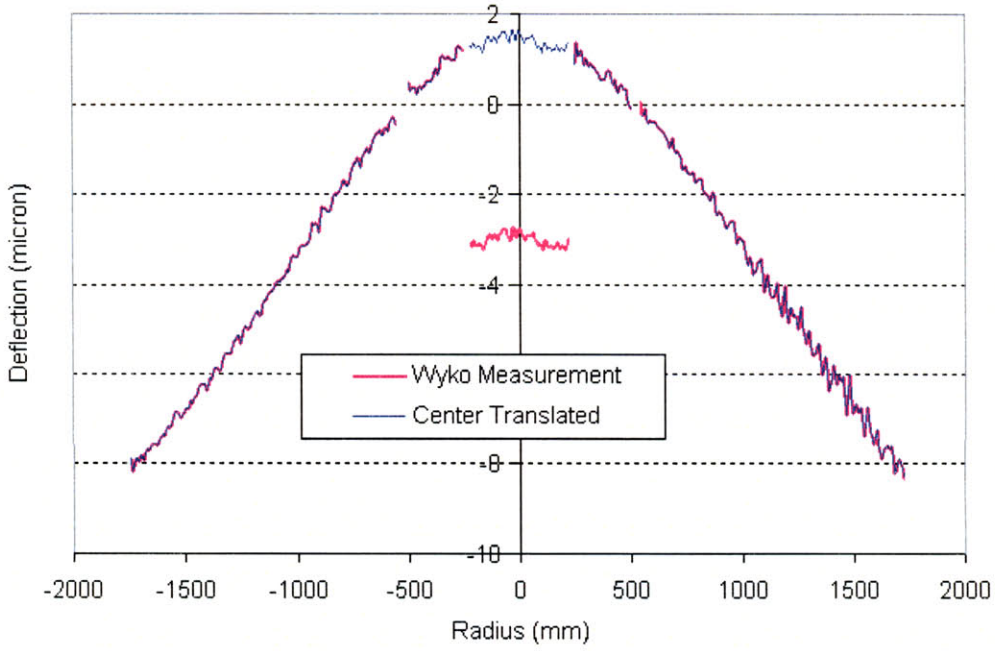


Figure 4.19. Profile of the plate at a cross-section after translation.

Pressure Differential

The wafer-level anodic bonding occurred inside an enclosed chamber that was supposed to be air tight. The initial pressure inside the chamber was atmospheric. According to the ideal gas law, the pressure inside the enclosed cavity of the device should return to 1 atmosphere after cooling down. However, during temperature rise, air must have found its way out of the chamber such that the pressure inside the chamber was reduced, causing the pressured inside the enclosed cavity after cooling down to be less than an atmosphere. However, exactly how much less is not known. We could at best derive this value using the measured cross-section from the Wyko profilometer. Figure 4.20 shows the cross-section of the plate as simulated by ANSYS. Here we have assumed two different initial conditions: the edge is bonded and the edge is touched down. It seems that the measured cross-section lies in between of these two states. An explanation could be that the bond,

which is only 50 μm wide, is not that strong and hence it is only partially bonded. This is further verified by the fact that after die-sawing, the plate is usually unbonded at the edge. In order to match the center deflection of the plate, for the edge-bonded case, a pressure differential of 0.625 ATM is used, while for the touched-down case, 0.5 ATM is used.

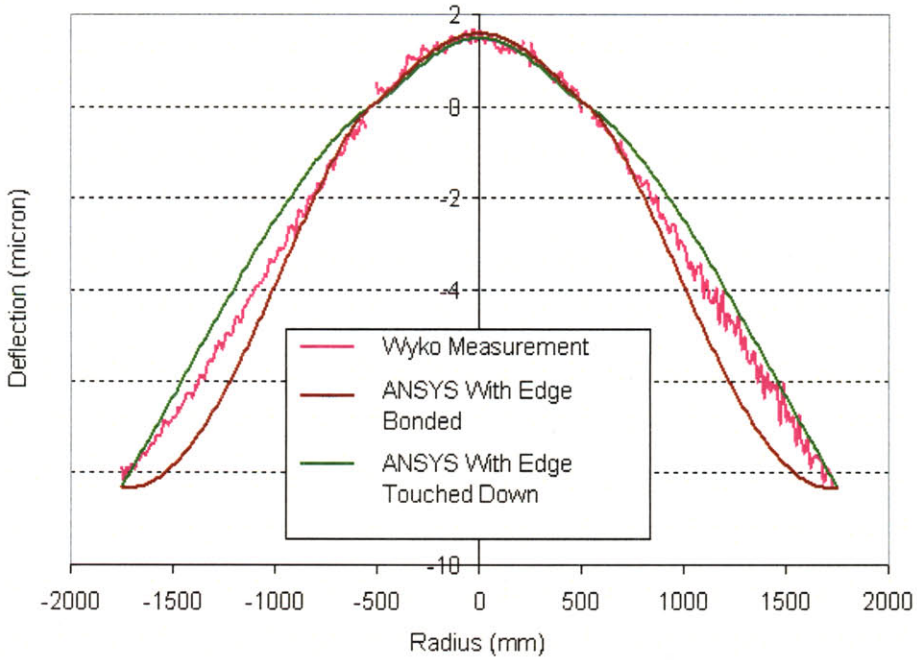


Figure 4.20. A cross-section of the plate as fabricated comparing the Wyko measurement to ANSYS simulation.

Combining all the findings above, we can simulate the center displacement of the plate with an ANSYS model. The code can be found in Appendix D.5. The center displacement as a function of actuation voltage is shown in Figure 4.21. In the figure, we plot the measurement data with errors estimated to be -3 nm and +1 nm, due to noise as well as misalignment of laser. We also plot the ANSYS simulation results with both the edge touched-down and edge bonded cases, and for each case, we show the difference between using a 10.1 μm of air gap versus 9.3 μm. Note that because the actual fabricated plate has a slit cut into it, in order to compare with the experimental data, the ANSYS results plotted

here are multiplied by an area factor by assuming that the electrostatic pressure is proportional to the actuation area. It is shown that with an initial air gap of 10.1 μm, the measured displacement lies in between the touched-down and bonded cases, as expected. With the air gap 0.8 μm less, the displacement increases by 15-20 nm at 40 V, which is doubled the value of the measurement. Because an air gap of 9.3-10.1 μm is within the error of fabrication and measurement, we conclude that the ANSYS simulation comply well with the experiments.

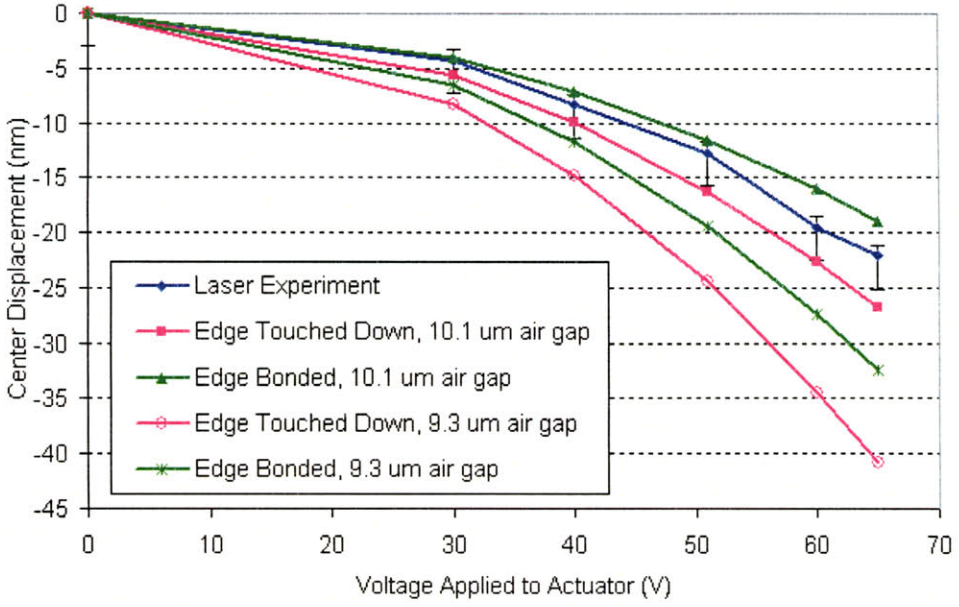


Figure 4.21. Center displacement of the plate vs. actuation voltage comparing laser experiments to various ANSYS simulations.

With the ANSYS model verified by experiments, we would like to find out what happens if the pressure differential would be avoided during fabrication, as well as if there would be no initial deflection of the outer plate. In this simulation, an air gap of 10.1 μm is used. It is shown that the difference in displacement caused by the pressure differential of the center plate is a couple of nanometers at most. However, by actuating the plate in the before pull-in stage instead of after pull-in, the center displacement is improved by twice

at the same voltage. It is therefore more advantageous to operate the device in the before pull-in stage.

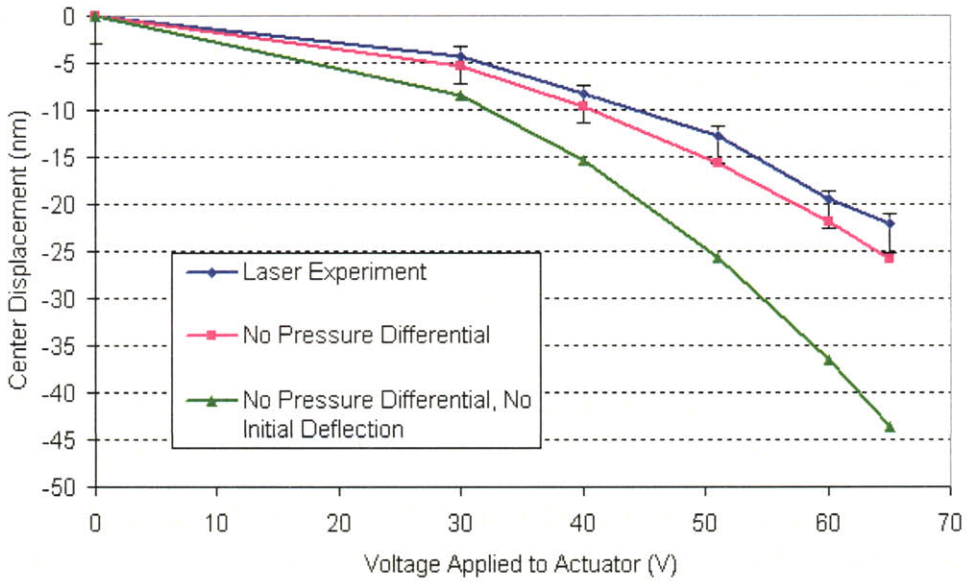


Figure 4.22. Center displacement of the plate predicted by ANSYS.

4.2.2 Die-Level Bonded Device

As shown in Figure 2.19, the die-level bonded device (device 6_1 in this case) has the plate initially suspended in most areas except for a corner where the tethers touch down because of exposed Pyrex at the bottom. We applied bias voltage from the meter and measure its change of capacitance and the result is shown in Figure 4.23. The curve on the right had 0.5 sec delay between each data point from 0 V to 40 V, and the curve on the left had 0.2 sec delay between each data point from -40 V to 0 V.

The up-sweep curve clearly shows the regions of pull-in, touch-down and zip-in. While for the case of down-sweep, the regions are not as distinct. However, electrostatic hysteresis is clearly visible. The capacitance changes from 13.3 to 315 pF when voltage sweeps up to 35 V, but then drops a little, which might due to the fact that the plate is not

mechanically stable. For down-sweep, the capacitance changes from 372 to 16.6 pF. This is a much larger change of capacitance compared to that of the center capacitor itself.

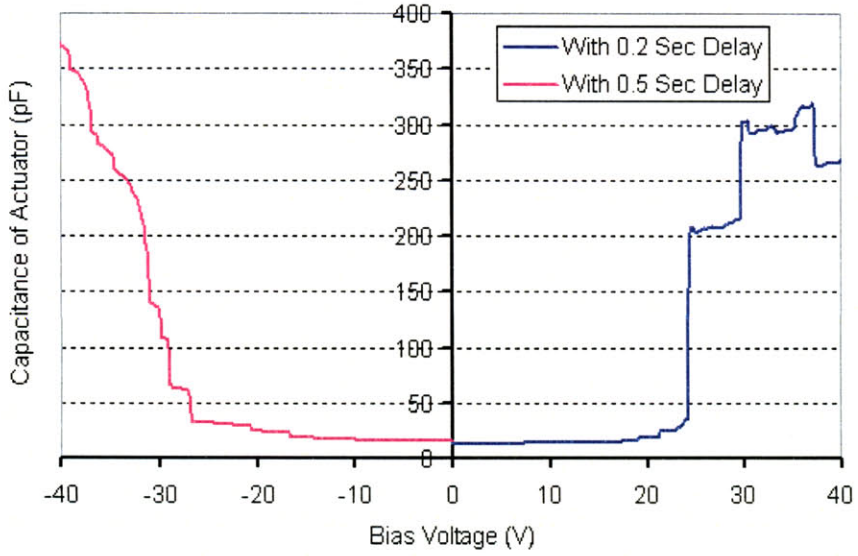


Figure 4.23. Capacitance of the actuator as bias voltage is applied to actuator of the die-level-bonded device.

The results of device 6_1 shows that with care, it is possible to bond the electrostatic actuator with anodic bonding while making sure that the two electrodes would not touch each other during the bonding process. The capacitance measurement result shows that the device operates in all three actuation stages. Its low pull-in voltage might result from the fact the the initial gap is much reduced due to the initial partial deflection of the plate, and that the plate has slits cut, which reduce its stiffness. Unfortunately, further testing of the device with the laser interferometer is not available because the device was debonded and replication of the device failed.

A clamped device was also tested. Because of the large initial gap, it was found that voltage greater than 100 V was needed to actuate the plate and as soon as the plate was pulled down, breakdown would occur. We did not test any clamped device further.

4.3 Summary

In this Chapter, we have shown the test setup used for measuring the capacitance and the displacement of the plate center. The capacitance was measured using two different meters, the HP 4294A and the HP 4284A. Voltage was applied either from the bias of the meter or an external power supply. The displacement was measured using a laser interferometer system equipped with an optical probe. Two different packaging methods were used to test the devices. The old package using Pogo Pins proved to be problematic because the Plexiglas housing obscured the laser alignment and the ground plates interfered with the actuation signal. Testing with the new package removed those problems and we tested a wafer-level bonded device extensively, which was originally touched down and would not experience pull-in during testing. Testing of the actuator and capacitor individually was demonstrated. And a capacitance change from 7.35 pF to 6.89 pF was observed when 65 V was applied to the actuator, resulting in a tuning ratio of 0.94:1, or a tuning range of -6%. The device was then die sawed and the actual shape of the fulcrum was obtained using SEM. With our measurements from both SEM and Wyko profilometer, we could estimate the initial deflection of the outer plate, the initial air gap and the pressure differential applied to the center plate due to the anodic bonding process. With these parameters, we could predict the displacement using an ANSYS model and then compare the results with experiments. It is found that within measurement error, the ANSYS results comply well with the experiments. Using the ANSYS model, we further predict the function of the device that operates in the before pull-in stage. We also tested the die-level bonded device, which operates across all three actuation stages. Our experiments show that for a device that operates within one actuation stage, the capacitance change is limited, and for a device that operates across the actuation stages, the capacitance change has a much larger span. However, the larger tuning ratio is accompanied by electro-mechani-

cal hysteresis. We also show that the device could operate in different regimes depending on how it is bonded. And it is possible to use anodic bonding to assemble out-of-plane electrostatic actuators while keeping the electrodes intact.

Chapter 5

Summaries, Conclusions and Future Work

5.1 Summaries

A proof-of-concept tunable capacitor for a tunable electromagnetic cavity resonator was designed, modeled, fabricated and tested. The design was based on the concepts of the Nanogate structure with an integrated electrostatic zipping actuator and was enabled mainly by the deep reactive ion etching and anodic bonding microfabrication techniques. Deep reactive ion etching was used to etch the high-aspect-ratio fulcrum that had the shape of a circular column. Survival of the footing effect during the etch was relieved to some degree by the use of guard rings surrounding the inner and outer sides of the column. Anodic bonding was used to assemble the three wafer layers used, because it allowed us to use a low-loss glass wafer in terms of electrical performance, although it was generally avoided for electrostatic devices. We found, however, that anodic bonding did not necessarily destroy the electrostatic actuator although it might introduce parasitic charges during the bonding process. By connecting both electrodes to the same potential during bonding to avoid actuation, and covering metal underneath the silicon electrode during design layout to minimize sodium ion diffusion, anodic bonding should be able to be used

with many electrostatic devices. The fabricated device was a simpler version of the design in that only one metal layer was used for the actuator and the capacitor, and the other part of the electrodes was a silicon plate, which was used both for structural and electrical purposes. This was due to the constraints of the facility at the time of fabrication. The simplified version, however, still allowed us to test the concept of the device without major drawback, except that grounding the actuator and capacitor introduced parasitics into the capacitance measurement, and series resistance was increased because of the use of silicon.

We modeled the structure using both Matlab numerical simulation and ANSYS finite element analysis. The structure could be described by using three ordinary differential equations using Timoshenko's elastic plate theory. However, since they are not linear, a closed form solution is not possible. On the other hand, the Matlab command BVP (boundary value problem) can be used to solve multiple ODE's with unknown parameters numerically and is well suited to our purpose. Different boundary conditions were used to model three actuation stages: before pull-in, zip-in and release. To double-check the Matlab results, an ANSYS model was also used. ANSYS is equipped to solve coupled physics problem as well as structures that involve contact mechanism. Furthermore, voltage sweep can be used to simulate the hysteresis of an electrostatic actuator. The Matlab results compared very well with the ANSYS results for our simulation. The Matlab model could be further used to perform parametric design studies to find out the optimal dimensions for a design.

The device was tested using a power supply, a capacitance meter (the HP 4294A and the HP4284A were both used for this purpose) and a laser interferometer system to measure the center displacement. The package used to test the device evolved over time. The first package used long Pogo Pins and proved to be unstable with parasitic. The second

package used shortened Pogo Pins and sandwiched the device in between two printed circuit boards, where BNC connectors were mounted for electrical signals. However, testing of the second package was not conclusive because it obscured the view of the laser for alignment purpose, and it introduced other parasitics to the device because of the metal shield used. A third package was designed to alleviate these problems by adhering the die on top of a PCB with conductive tape. With this package, we were able to test the performance of the devices.

Two different types of devices were tested. One was a wafer-level-bonded device, where the outer plate was snapped down onto the bottom electrode during anodic bonding because of the way the mask was laid out and therefore, the device would only operate in the after-pull-in stage. With this device, we found that the capacitance of the capacitor changed from 7.6 to 14.8 pF when 40 V was applied to the capacitor, with about 130 nm of displacement. When voltage was applied to the actuator, the capacitor changed from 7.35 to 6.89 pF, corresponding to a displacement of about 25 nm. No hysteresis was observed in this device because it only operated in the after pull-in stage. Using an ANSYS model, the displacement predicted by simulation matched with the experiments subjected to fabrication and measurement errors. We also tested a die-level-bonded device, where the two electrodes were applied the same potential during anodic bonding and hence the outer plate was elevated above the bottom electrode in most places except where Pyrex was exposed due to misalignment. Results showed that the device operated across the before pull-in, touch-down and zip-in stages and electromechanical hysteresis was observed.

5.2 Conclusions

Our simulation and test results have shown that the lever-fulcrum structure with electro-

static zipping actuator works as expected, and it has some, although very limited, capacitance tuning capability. The device could operate in before pull-in or after pull-in actuation stages depending on how anodic bonding is done.

While numerical simulation using Matlab BVP is more time-efficient when it comes to perform design studies, ANSYS model is more encompassing and realistic when it comes to predict the actual performance of the device.

We have shown that anodic bonding can be used to assemble out-of-plane electrostatic actuators even on the wafer-level. Careful mask layout can be done to short the electrodes together during bonding and separate each device after die sawing. Furthermore, in the actuator areas, no Pyrex should be exposed. With these precautions, there is no reason to avoid using anodic bonding for this purpose.

It is also clear to us that because of electromechanical hysteresis of the electrostatic zipping actuator, the capacitance tuning capability of the device is very limited, and its full range of capacitance change cannot be fully applied. In order to avoid the electrostatic hysteresis, the device should operate within each actuation stages, namely, the before pull-in stage, the touch-down stage, and the zip-in stage. If capacitance hopping is desired, the actuation voltages will be limited to less than the release voltage and larger than the zip-in voltage. The zipping actuator has been demonstrated to be superior in its performance to actuate a bistable micro relay, however, its use as a proportion control actuation for a tunable capacitor is less advantageous. Furthermore, in order for the electrostatic-zipping-actuated fulcrum-lever structure to be effective, the fulcrum width is critical and it must be small compared to other dimensions. However, this imposes fabrication challenges because small width increases the aspect-ratio as well as the risk of overetching.

In conclusion, the fulcrum-lever structure is well suited to controlling very small flow of a microfluidic valve because it allows for nanometer resolution displacement. However,

integration of the structure with a zipping actuator limits the use of the structure as a tunable capacitor because of electromechanical hysteresis and the fact that the fulcrum itself is a limiting factor in terms of efficiency of bending the center plate. Furthermore, there is a trade-off between how thin a fulcrum is desired and its manufacturability using microfabrication. To eliminate these problems, a new design of the tunable capacitor and its integration with the LC cavity resonator is proposed and will be described next.

5.3 Future Work

During testing of Die 9_3, we found that an actuator placed within the fulcrum area would be a more effective actuator than placing the actuator outside of the fulcrum and relying on the fulcrum to act as the pivot and bend the inner plate. This is supported by ANSYS simulations.

Accordingly, a design of a new actuator is shown in Figure 5.1. The circular silicon plate is supported by tethers shown here similar to that of the zipping actuator, but no fulcrum is needed in this design. As will be shown later, the bottom part of the plate will act as the electrostatic actuator, which operates in the before pull-in stage, and the top part of the plate forms the capacitor plate. An axisymmetric 2-D model of the new actuator design is simulated with ANSYS, as shown in Figure 5.2. In this 2-D model, the tethers are represented by a thin bridge that has equivalent spring constant as the tethers. The outer edge of the tethers is a clamped support. Voltage is applied between the silicon plate and the bottom electrode. The actuator would only operate before pull-in, and hence no dielectric insulation would be needed.

We used the following dimensions shown in Table 5.1 in our simulations. With 40 V, the center deflection is found to be 750 nm. A profile of the plate after actuation is shown in Figure 5.3. The ANSYS code can be found in Appendix D.5.

Figure 5.1. A design of the new electrostatic actuator.

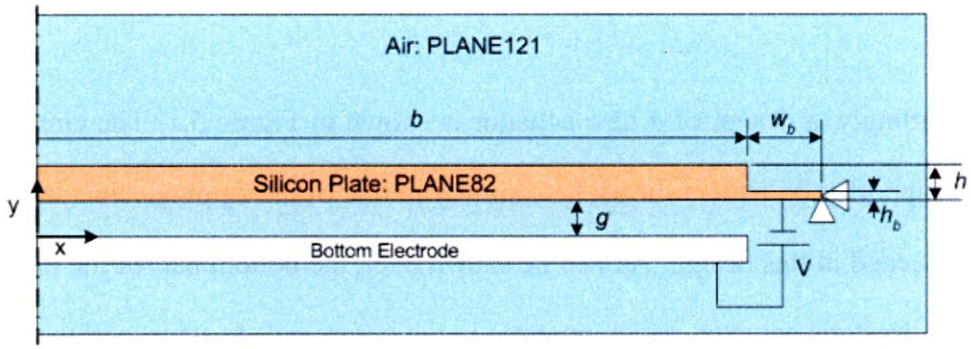


Figure 5.2. Axisymmetric 2-D equivalent model of the new actuator design.

Table 5.1. Dimensions used in the simulation of the new actuator design.

Item	Symbol	Value (μm)
Outer plate diameter	b	500
Width of bridge	w_b	50
Thickness of plate	h	10
Thickness of bridge	h_b	1
Air gap	g	2.5

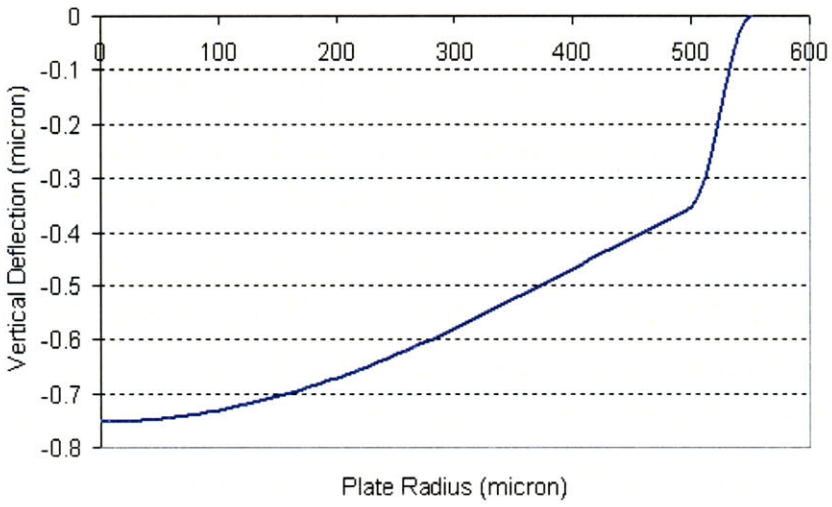


Figure 5.3. The deflection profile of the plate with the new design using ANSYS.

With this design, the size of the actuator is significantly reduced and the center deflection is improved as well. To apply this actuator to the LC tank, a concept is shown in Figure 5.4. The tank is comprised of three wafers, with a SOI sandwiched by two Pyrex wafers as before. The toroidal resonator cavity situates above the silicon plate, the center of which is the tunable capacitor area. The LC tank is coupled through the capacitor, where the top capacitor is connected through a copper via in the middle of the device. Next we will examine the function of this LC resonator and will present the fabrication process.

5.3.1 Theory of the LC Resonator

A schematic of the LC resonator is shown in Figure 5.5. For simplification, the gap g is assumed to be uniform in the analysis, but the actual curvature of the silicon plate will be considered in the capacitor calculation.

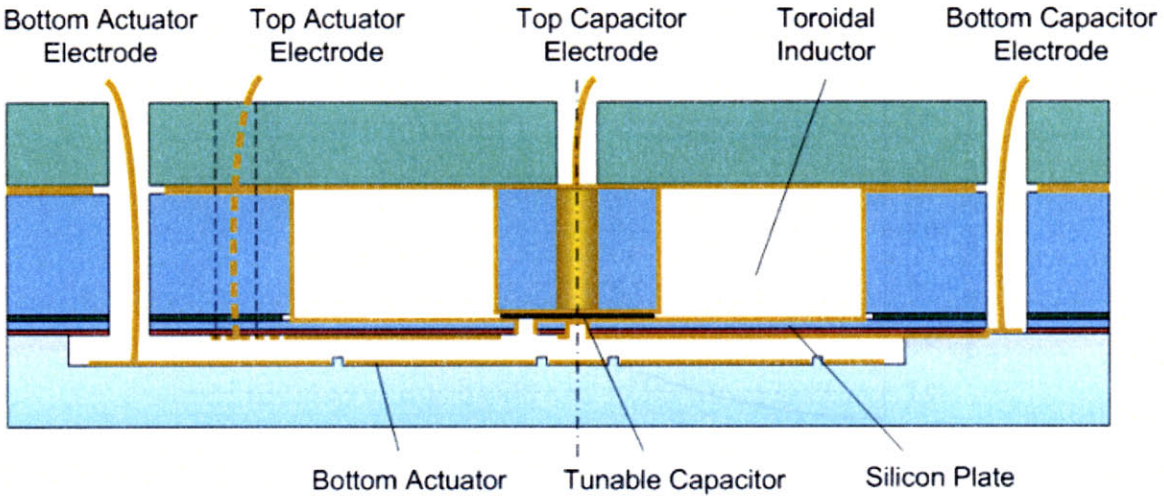


Figure 5.4. A 2-D cross section of the conceptual LC tank.

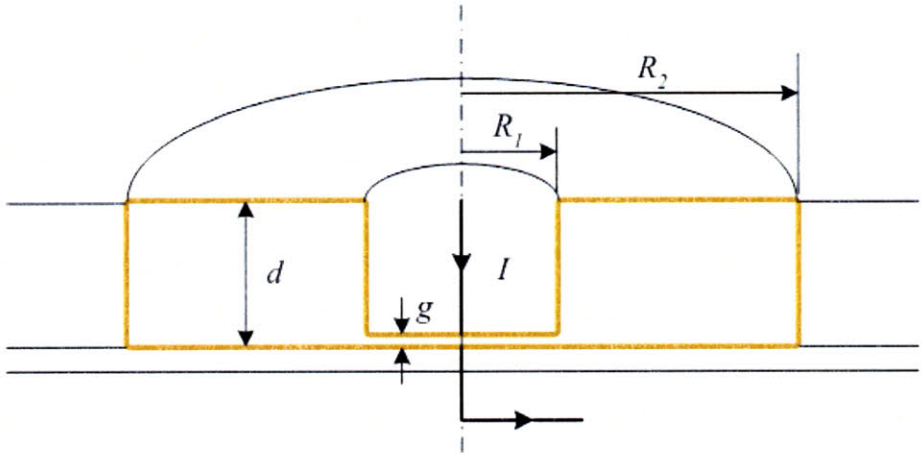


Figure 5.5. Simplified schematic of the LC resonator.

In our analysis, we will make the following assumptions. 1) The current I flows into the top capacitor plate and out of the bottom. This current distributes evenly across the capacitor, forming a surface current K in the gold plating inside the capacitor. 2) The magnetic flux lines are contained inside the toroid and outside the gold plating, there is no H

field. We can then derive that the H field inside the toroid is $H=K$. The surface current K is a function of the radius,

$$K = H = \frac{I}{2\pi r} \tag{5.2}$$

The flux density is,

$$B = \mu_o H = \frac{\mu_o I}{2\pi r} \tag{5.3}$$

To calculate the inductance, the total flux inside the toroid must be calculated. This is done by integrating the flux density across the cross-sectional area of the toroid. Dividing the flux-linkage by the current gives the inductance,

$$L = \frac{\int_0^d \int_{R_1}^{R_2} \frac{\mu_o I}{2\pi r} dr dz}{I} = \frac{\mu_o d}{2\pi} \ln \frac{R_2}{R_1} \tag{5.4}$$

where μ_o is the vacuum permeability.

The capacitance of the capacitor by assuming uniform gap can be expressed as,

$$C = \frac{\varepsilon A}{g + c/\varepsilon_{ox}} \tag{5.5}$$

by taking into account the thickness of the insulating oxide (or nitride) c.

The resistance of the toroid is calculated below. The skin depth of gold w_{Au} is a function of resonant frequency. Note that the loss calculated here does not include dielectric

hysteresis, radiation, charge relaxation time constants and leakage through silicon, all of which could reduce the Q of the LC tank.

$$R_L = \frac{1}{2\pi\sigma_{Au} w_{Au}} \left(\frac{d}{R_1} + \frac{d}{R_2} + 2\ln\frac{R_2}{R_1} \right) \tag{5.6}$$

where the skin depth of gold is expressed as,

$$w_{Au} = \sqrt{\frac{2}{\omega\mu_o\sigma_{Au}}} \tag{5.7}$$

and σ_{Au} is the electrical conductivity of gold.

The series resistance associated with the capacitor is dominated by the silicon column and can be expressed as,

$$R_C = \frac{d}{\sigma_{Cu} A} \tag{5.8}$$

where σ_{Cu} is the electrical conductivity of copper.

With the derived parameters of the tank, we can describe the tank with a lumped parameter model as shown in Figure 5.6.

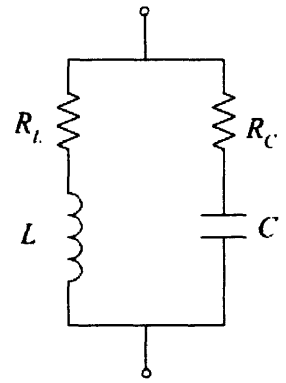


Figure 5.6. Lumped parameter model of the LC tank.

Using Matlab, we can simulate the frequency response of the tank. The following dimensions and parameters are used or derived in the simulation. The Matlab script can be found in Appendix C.7.

Table 5.2. Dimensions used and parameters derived in the Matlab simulation.

Item	Symbol	Value
Radius of capacitor	R_1	200
Radius of toroid	R_2	550
Height of toroid	d	300
Thickness of oxide	c	50 nm
Change in gap	g	10 to 750 nm
Inductance of toroid	L	60.7 pH
Resistivity of gold	ρ_{Au}	$2.44\times10^{-8}\Omega$m
Resistance of toroid	R_L	11.0 mΩ to 25.4 mΩ
Capacitance change	C	48.8 pF to 1.6 pF
Resistivity of copper	ρ_{Cu}	$1.72\times10^{-8}\Omega$m
Resistance of capacitance	R_C	0.04 mΩ
Resonant frequency	f_o	2.9 GHz to 16.4 GHz
Quality Factor	Q	21 to 63

The frequency response is plotted in Figure 5.7. We use a gap of 10 nm to start, to take into consideration of roughness even two surfaces are mated. When the gap changes from 10 to 750 nm, the resonant frequency changes from 2.9 to 16.4 GHz, which covers the UWB spectrum. The corresponding quality factor is 21 to 63, which can be improved by the design. It can be shown that quality factors can exceed 100 when the size of the cavity increases.

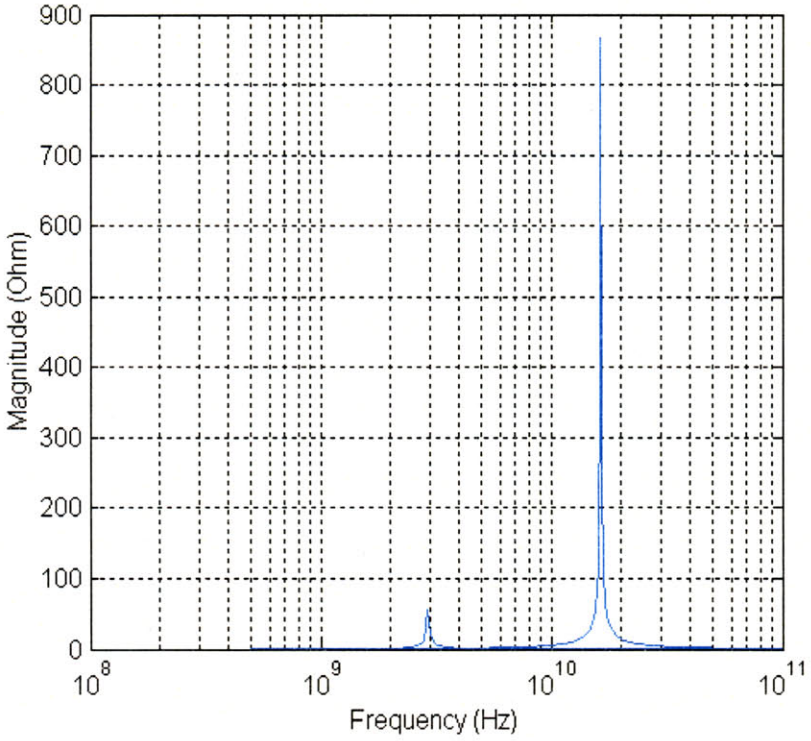


Figure 5.7. Magnitude response as capacitance is tuned from its initial value (the curve to the left) to the final value (the curve to the right).

5.3.2 Proposed Fabrication Process

The fabrication process for the LC cavity resonator is proposed here. It could be a rather complicated process and we will only describe the major steps.

The new resonator design also consists of three wafers, including a middle SOI wafer and a bottom Pyrex wafer, but instead of top Pyrex wafer, a DSP wafer is used instead. The entire process is illustrated in Figure 5.8. We will start the fabrication process with the middle wafer and provide a brief description of each step.

1. We will first deposit PECVD nitride and pattern it with a plasma etcher to define the top actuator electrode. 2. In order to access the top capacitor electrode, DRIE is used to

open a hole, then electroplating is used to fill the hole with copper. Chemical-mechanical polishing will then be used to polish the top surface. For a detail explanation of the copper via process, refer to [54]. 3. Using DRIE, we will pattern the SOI layer to form the silicon plate. 4. We will then deposit gold and use life-off to pattern it to define the top actuator electrode as well as access to the bottom capacitor electrode. 5. DRIE is used to etch the cavity as well as access holes for electrical connection. Then gold is deposited on top of the center disk using a shadow mask. 6. For the top wafer, DRIE is used to open an access hole, and then lift-off is used to deposit gold surrounding this hole. 7. Now we will bond the top and the middle wafer using thermal compression, and only the center disk area will be bonded because that is where the gold is deposited. 8. We will then release the oxide layer using BOE, after which, the center disk will be attached to the top wafer and the top stack will be separated from the middle wafer. 9. Sputter gold to the top stack using a shadow mask, and then deposit PECVD oxide to the top stack also using a shadow mask. 10. Sputter gold to the bottom stack using a shadow mask to cover the cavity with gold. 11. Now bond the top stack and the middle wafer again using thermal compression. This way, the gap between the center disk and the silicon plate can be accurately controlled, provided that metal deposition on both sides does not deform the plate significantly. 12. Using a Pyrex wafer, etch a bottom pit with dimples on it using BOE. Then deposit gold using lift-off. 13. Anodic bond the top stack to the bottom Pyrex wafer, finishing the finally assembly of the device.

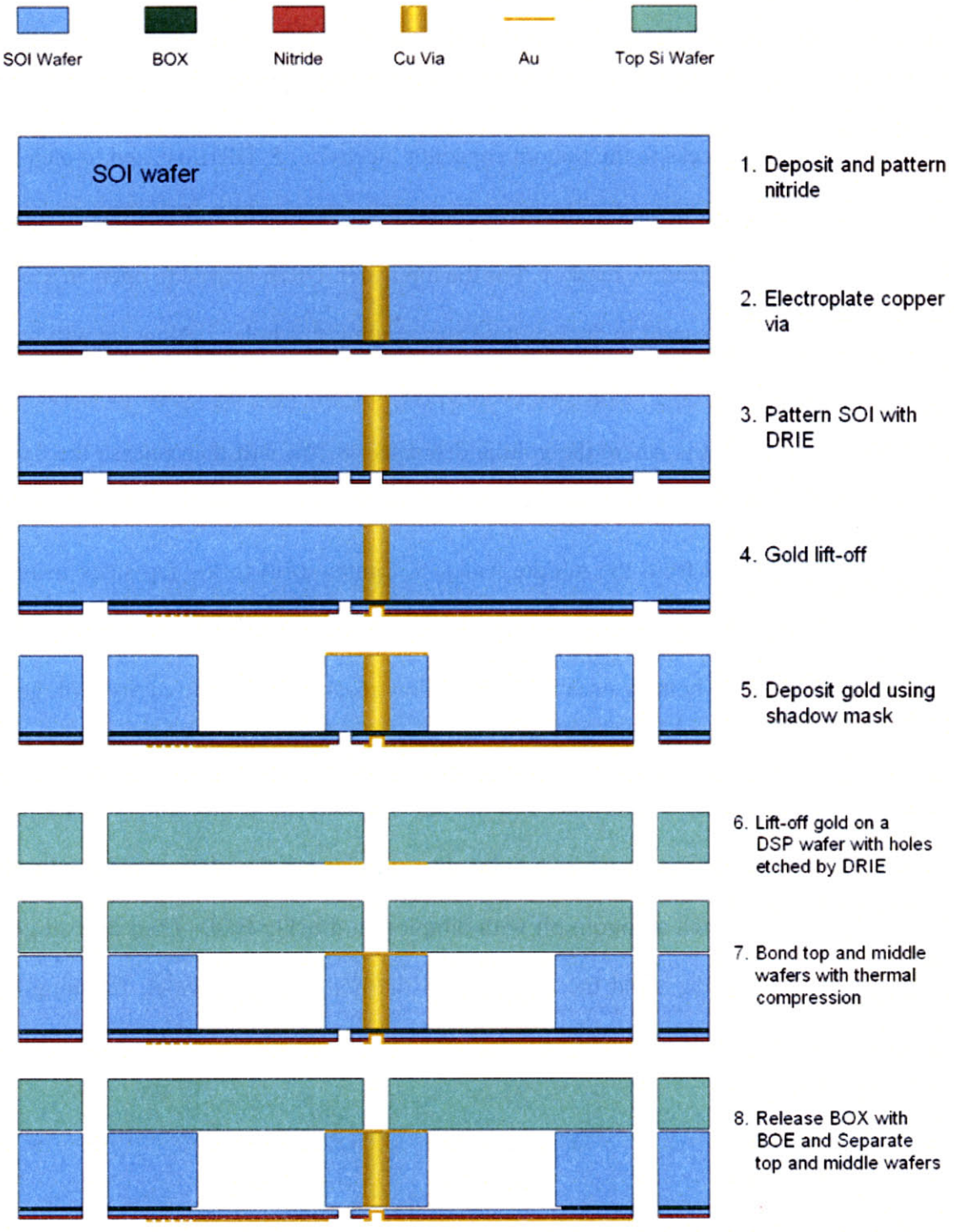


Figure 5.8. Fabrication process of the new LC cavity resonator.

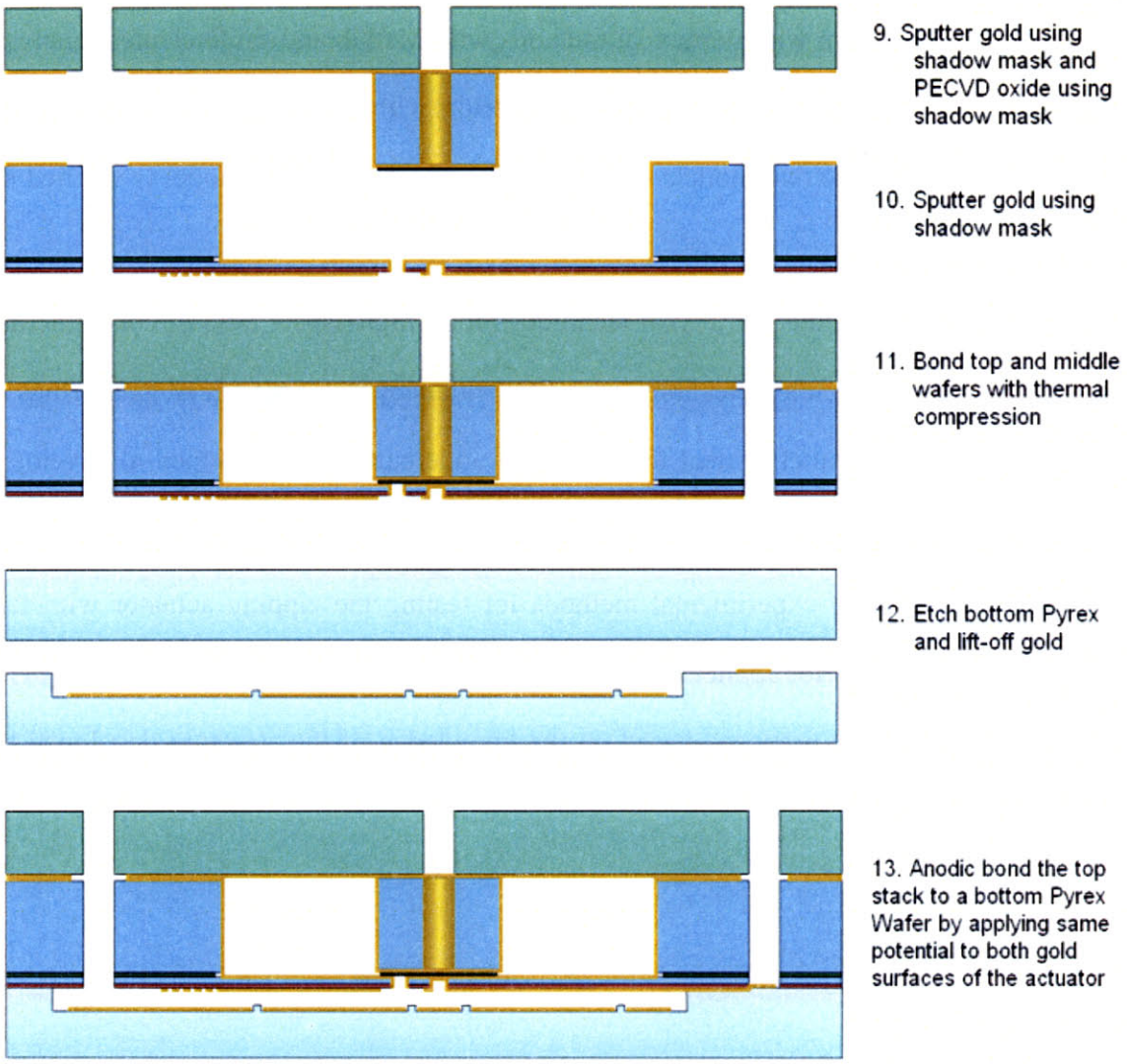


Figure 5.8. Fabrication process of the new LC cavity resonator.

As shown, the new device involves a series of DRIE etch, electroplating, gold deposition, thermal compression and anodic bonding. The process is complicated, and it is to the author's best knowledge how the proposed cavity resonator can be fabricated.

5.4 Contributions

The author's contribution in this thesis can be summarized to the following:

1. A design for a novel circular electrostatic zipping actuator and its application to actuate a MEMS tunable capacitor.

2. Development of a model for the zipping actuator and the fulcrum-lever mechanism by modeling the system with numerical methods with Matlab and finite element analysis with ANSYS and comparison of the simulation results with experiments. Good agreement is obtained between the two models in most areas. And the ANSYS model is verified by experiments.

3. Development of the fabrication techniques for a high-aspect ratio circular fulcrum with deep reactive ion etching techniques on SOI wafers by using sacrificial guard rings to protect the inner and outer critical features from undercutting. Also helped to develop a method of anodic bonding an out-of-plane electrostatic actuator.

4. Development of experimental methods for testing the zipping actuator with fulcrum-lever mechanism for application to a tunable capacitor. Improvement in design of an LC cavity resonator is proposed based on the knowledge of the structure developed by modeling and testing.

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Appendix

A

Mask Layout and Drawings

Table A.1. Dimensions and the designs used for each device in the mask layout. All dimensions are in μm.

Die #	Device #	Plate Dimensions			Guard Rings	Slit Width	Slit Length	Number of Slits
		Fulcrum Inner Radius	Plate Outer Radius	Fulcrum Thickness				
1	1	500	1750	50	yes			
	2	500	2000	50	yes			
	3	750	1750	50	yes			
2	1	500	1750	35	no	25	550	12
	2	500	1750	35	no	25	300	12
	3	750	2000	35	no			
3	1	500	1750	50	yes			
	2	500	2000	50	yes			
	3	750	1750	50	yes			
4	1	500	1750	35	yes	25	550	12
	2	500	1750	35	yes	25	300	12
	3	750	2000	35	yes			
5	1	500	1750	50	no			
	2	500	2000	50	no			
	3	750	1750	50	no			
6	1	500	1750	35	yes	25	550	12
	2	500	1750	35	yes	25	300	12
	3	750	2000	35	yes			
9	1	500	1750	50	no			
	2	500	2000	50	no			
	3	750	1750	50	no			
1	4	500	1750	50	yes			
	5	500	2000	50	yes			
	6	750	1750	50	yes			
2	4	500	1750	35	no	25	550	12
	5	500	1750	35	no	25	300	12
	6	750	2000	35	no			
3	4	500	1750	50	yes			
	5	500	2000	50	yes			
	6	750	1750	50	yes			
4	4	500	1750	35	yes	25	550	12
	5	500	1750	35	yes	25	300	12
	6	750	2000	35	yes			
5	4	500	1750	35	no	25	550	12
	5	500	1750	35	no	25	300	12
	6	750	2000	35	no			
6	4	500	1750	35	yes	25	550	12
	5	500	1750	35	yes	25	300	12
	6	750	2000	35	yes			
9	4	500	1750	50	no			
	5	500	2000	50	no			
	6	750	1750	50	no			

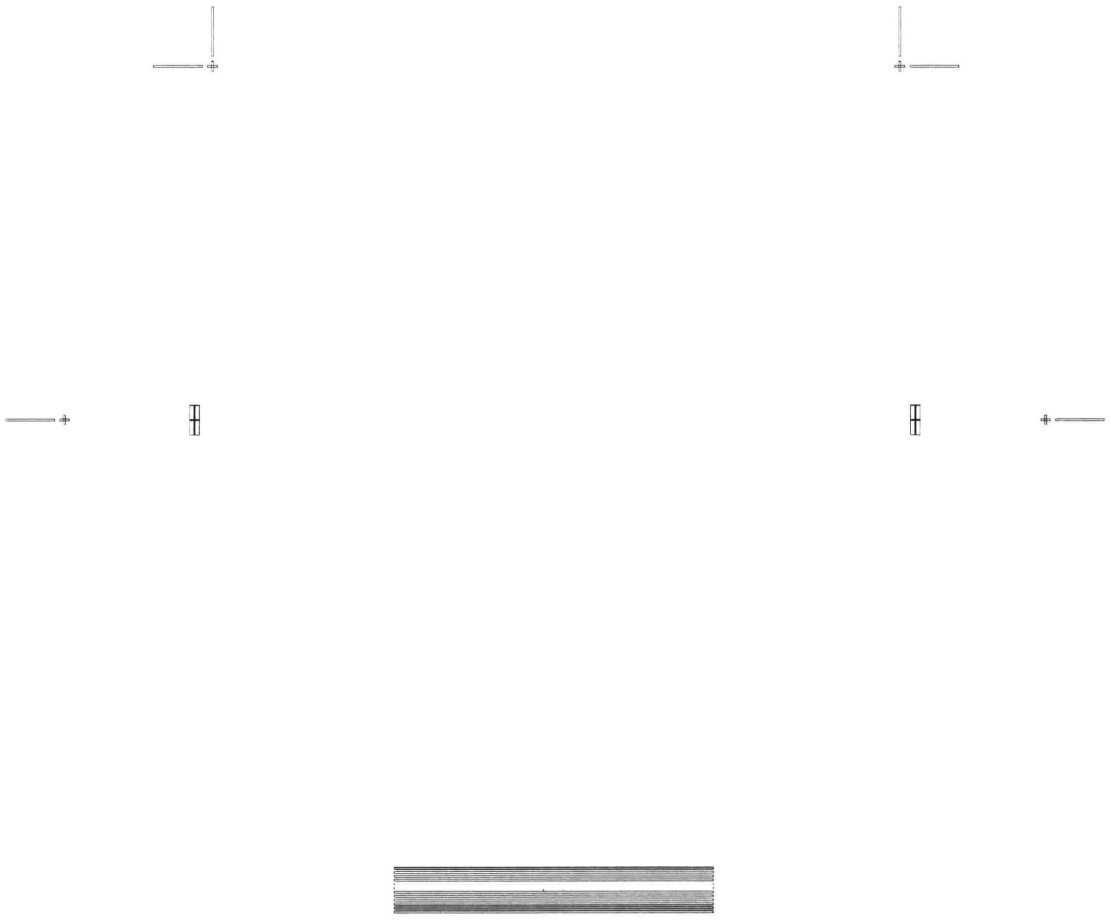

Figure A.1. Mask 1: ALIGN, wafer level

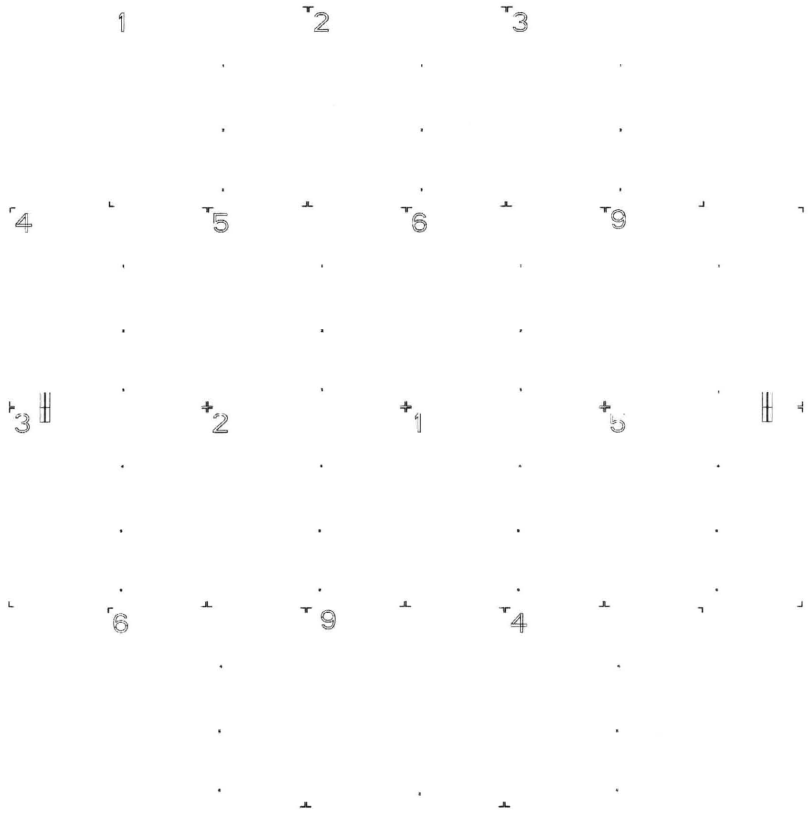

Figure A.2. Mask 2: STREETS

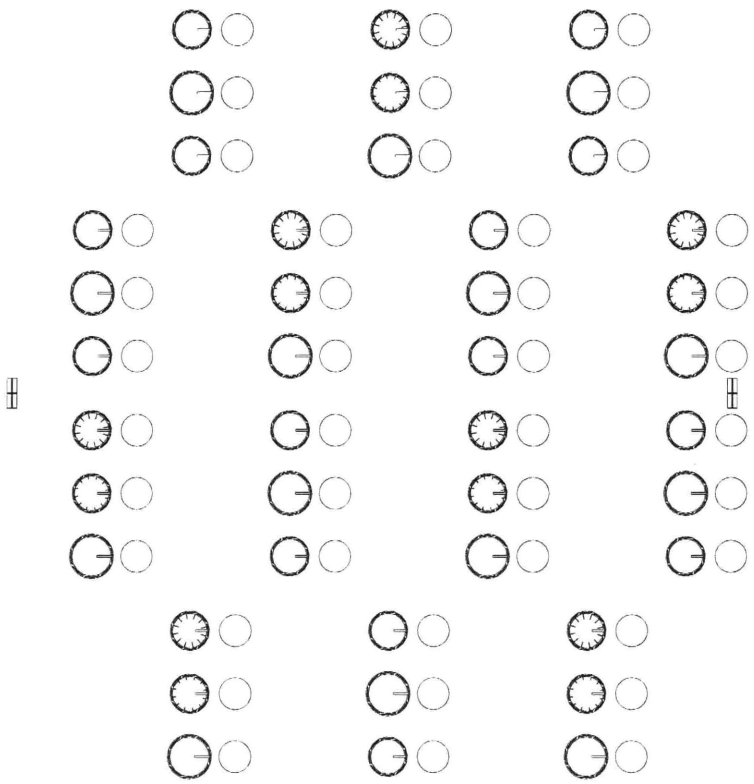

Figure A.3. Mask 3: ACTUATOR_TOP, wafer level

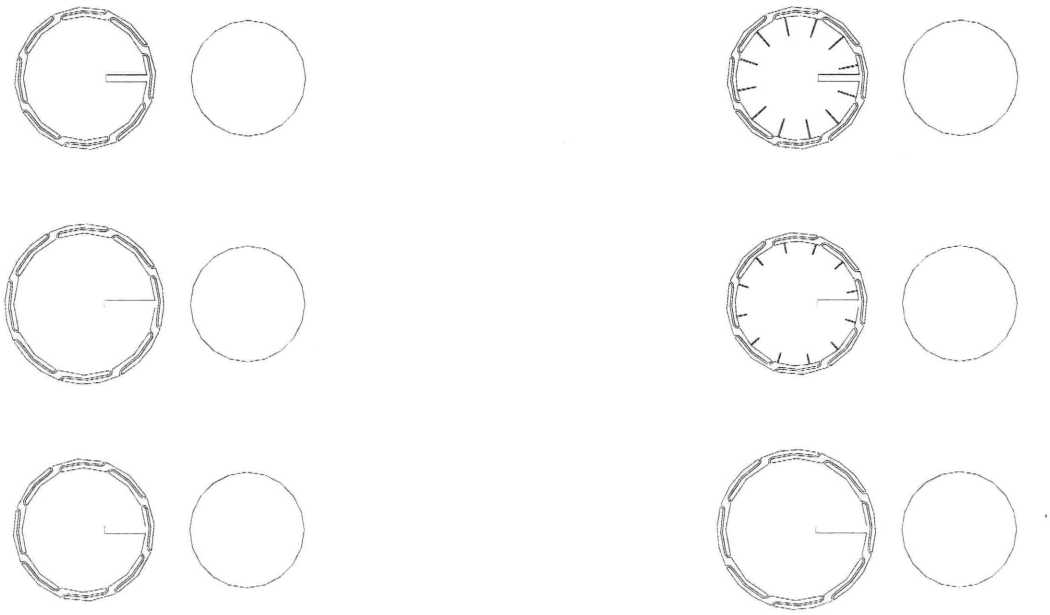

Figure A.4. Mask 3: ACTUATOR_TOP, die level (showing two different dies)

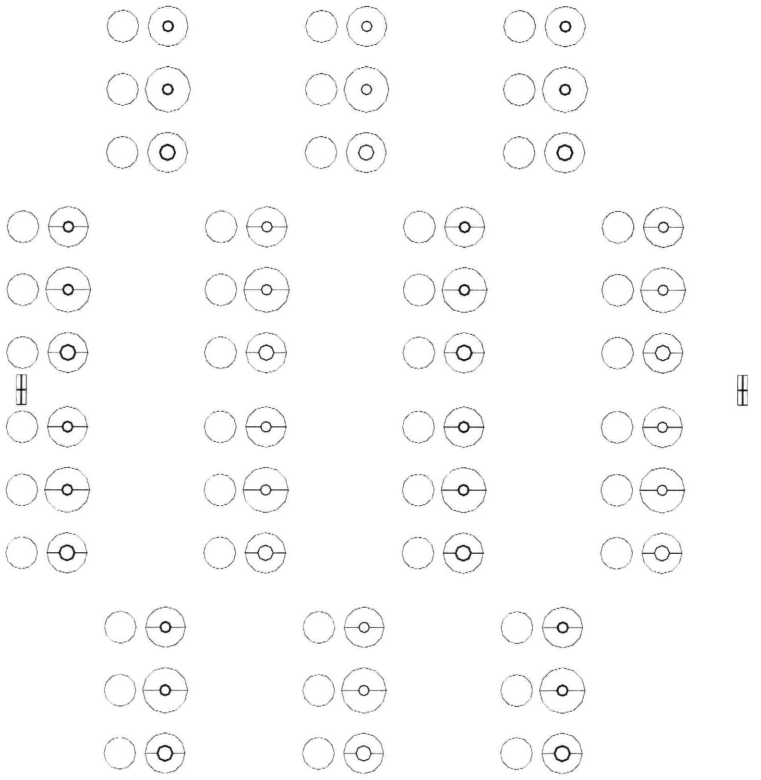

Figure A.5. Mask 4: FULCRUM, wafer level

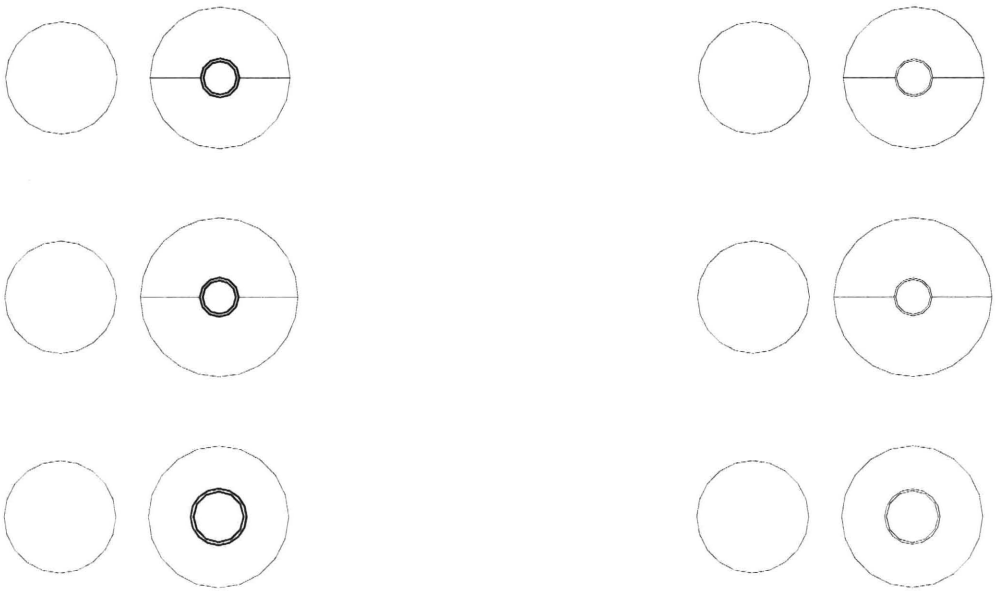

Figure A.6. Mask 4: FULCRUM, die level (showing two different dies)

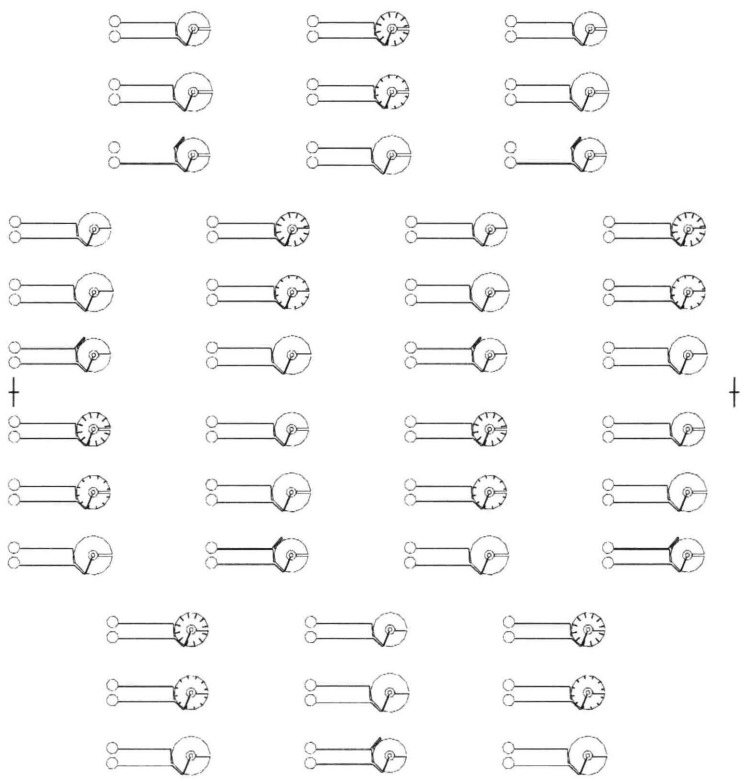

Figure A.7. Mask 5: METAL_TOP, wafer level

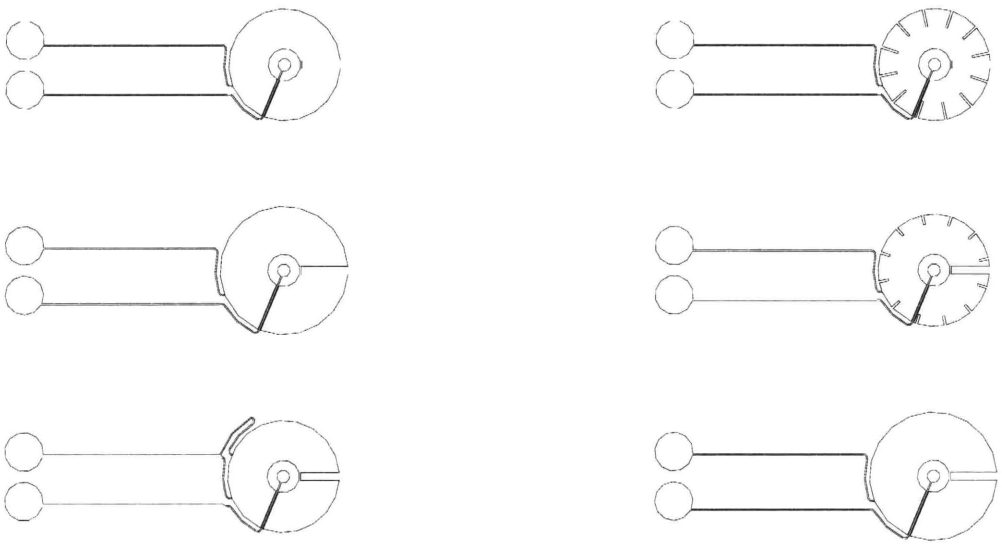

Figure A.8: Mask 5: METAL_TOP, die level (showing two different dies)

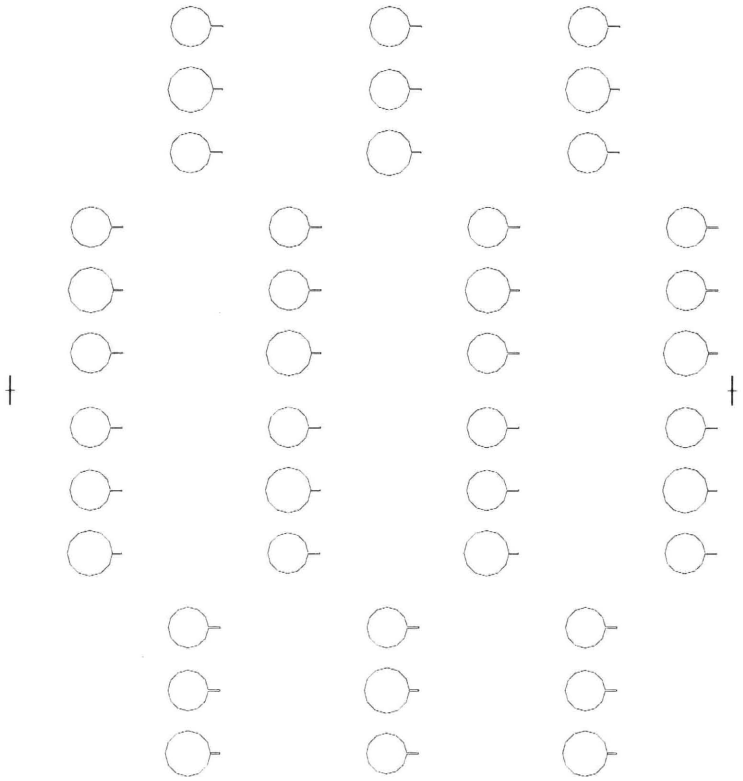

Figure A.9. Mask 6: OXIDE, wafer level

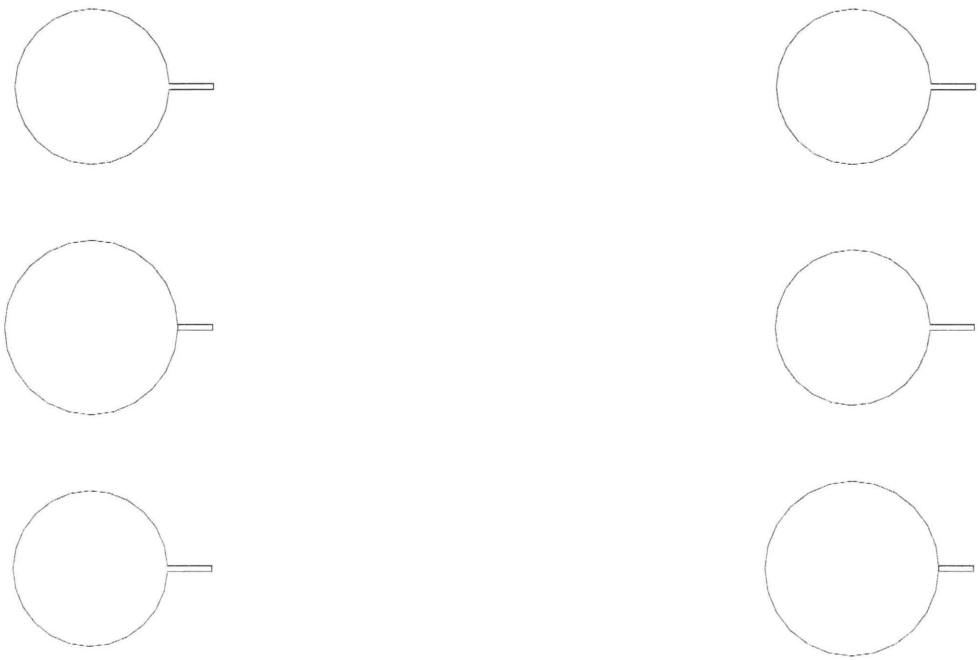

Figure A.10. Mask 6: OXIDE, die level (with two different dies)

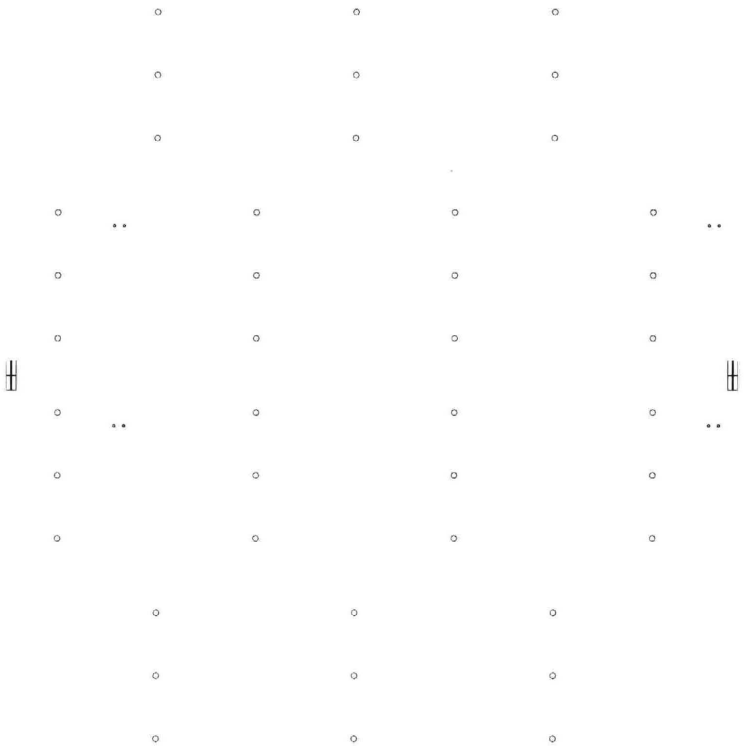

Figure A.11. Mask 7: CAPACITOR_SEAT, wafer level

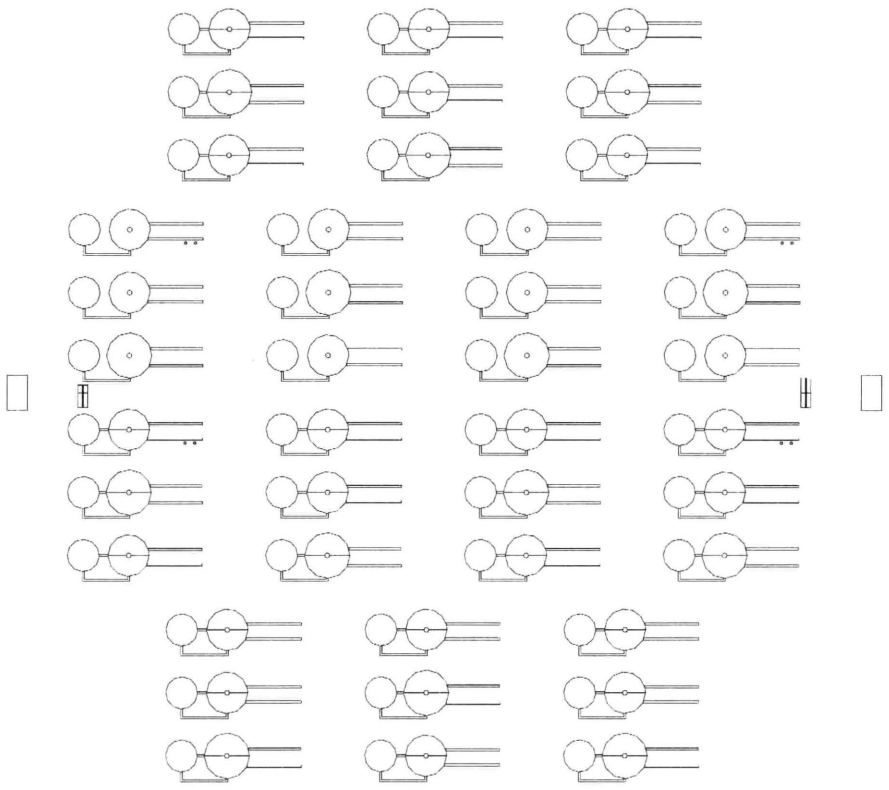

Figure A.12. Mask 8: ACTUATOR_BOTTOM, wafer level

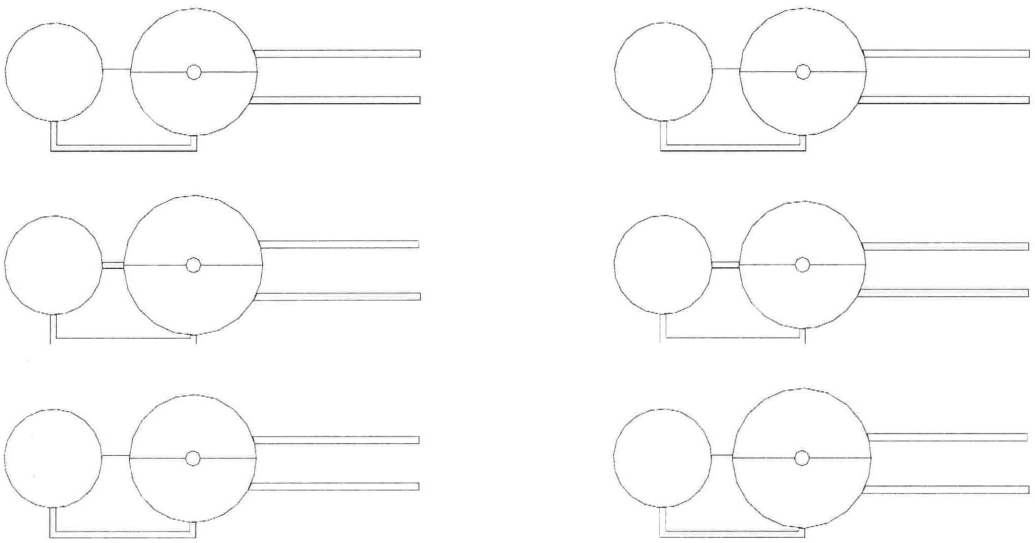

Figure A.13. Mask 8: ACTUATOR_BOTTOM, die level

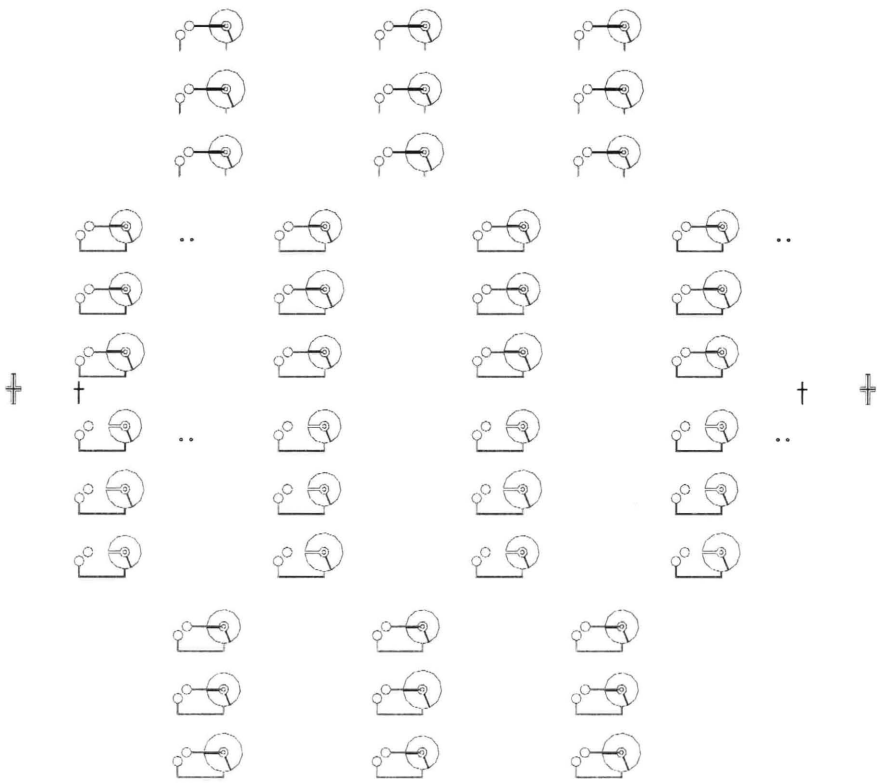

Figure A.14. Mask 9: METAL_BOTTOM, wafer level

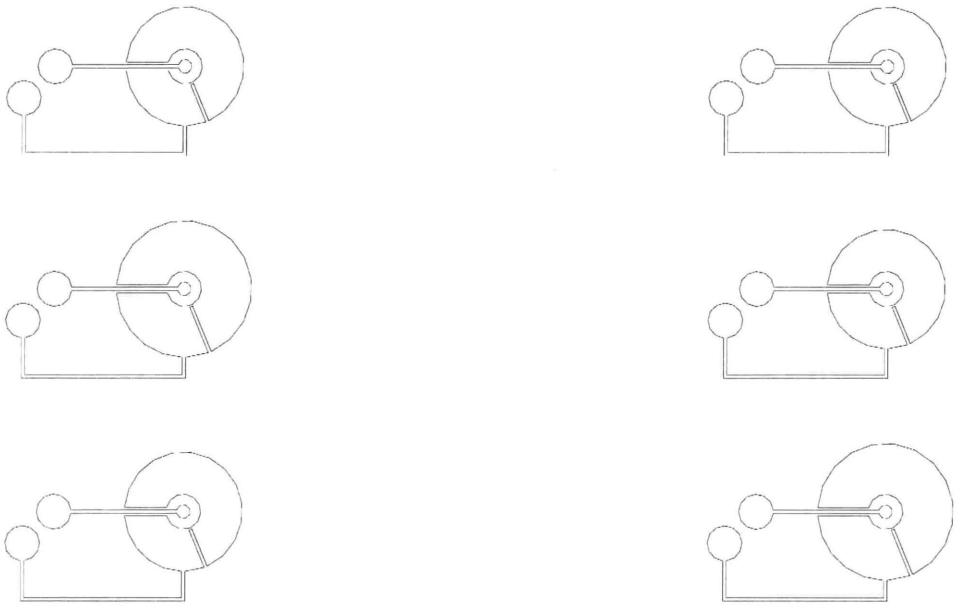

Figure A.15. Mask 9: METAL_BOTTOM, die level (showing two different dies)

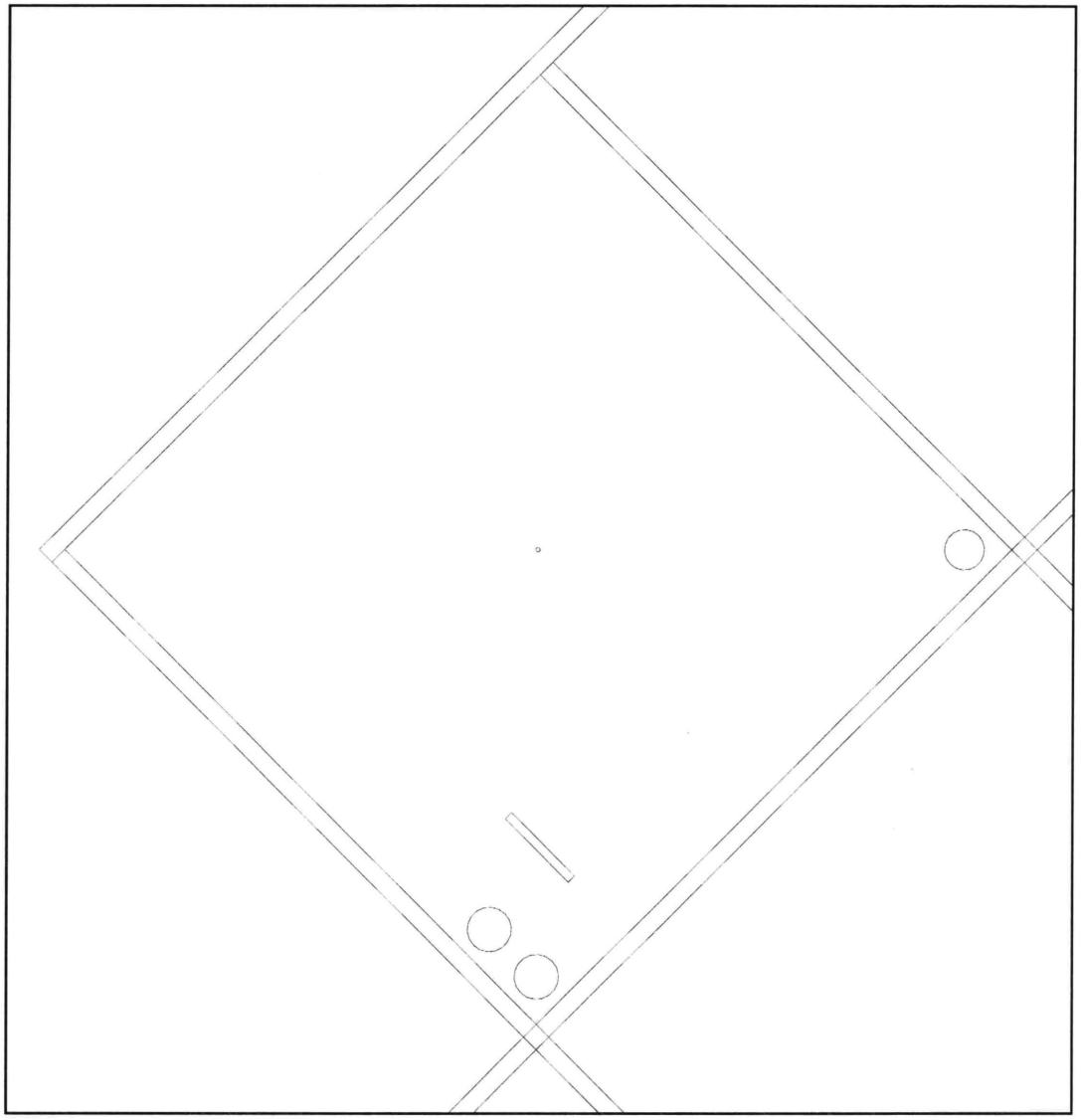

Figure A.16. . Mask: SEAL_BACK, die level, with streets

Appendix B

Process Flow

B.1 Fabrication Process for Middle Wafer

Initial wafer conditions:
B doped (p type)
<100> orientation
5-18 mΩ cm

Wafer#	Type	SOI (mm)	BOX (mm)	Thickness (mm)	Wafer Bow (mm)
TC3_2	SOI	20	1.5	344	83.46
TC3_3	SOI	20	1.5	345	74.84
TC3_5	SOI	10	1.5	338	77.15

1. Thermal oxidation: 0.5 um

Piranha clean, TRL
RCA clean, TRL

Thermal oxidation, TRL, Tube A2
Step 1: 1 min N2
Step 2: 20 min O2
Step 3: 11 min N2
Step 4: 68 min H2 + O2
Step 5: 20 min O2
Step 6: 20 min N2

Oxide thickness in Nanospec for dummy wafer:

Wafer	flat	right	top	left	center
Dummy1	0.5043	0.5001	0.4930	0.5027	0.5008 (source side)
Dummy2	0.4851	0.4813	0.4837	0.4835	0.4865
TC3_2	0.5064	0.5078	0.5055	0.5069	0.5067

2. Masks: Align & Streets
   Photolithography
      HMDS
      Coat one side: Standard thin resist @ 3Krpm
      Prebake: 10 min @ 90 degC
      Coat the other side: @ 3Krpm
      Prebake: 30 min @ 90 degC
      Expose alignment marks: EV1 for 2 sec
      Develop: OCG 934 for 10 sec
      Expose Streets: 2 sec
      Develop: 1 1/2 minutes
      Postbake: 30 min @ 120 degC

   BOE TRL: 7 min

   STS1 etch
      Recipe: Almark
      Time: 20 sec (put back to about 16 sec to avoid CF4)
      Depth: 3.3 um w/ resist & oxide

   Piranha clean

3. Mask: Tethers
   Photolithography
      HMDS for thick resist
      Spin coat: thick resist @ 2 krpm
      Prebake: 60 min @ 90 °C
      Expose: EV1 for 20 sec
      Develope: 150 sec
      Back side resist coating: thin
      Post bake: 25 min @ 90 degC
      Patch alignment marks w/ thin resist
      Post bake: 10 min @ 90 degC
      Patch alginment marks again for a 2nd time
      Post bake again for 10 min

   BOE TRL: 7 min w/ 10 sec degas at level 5

STS1 etch tethers
Recipe: MIT 37
Time: 10 min (actual time varies from 6-8 min)

Wafer #	Actual Time (min)
TC3_5	< 3min by SF6 withouth RF power
TC3_2	7 min 30 sec
TC3_3	8 min 35 sec

4. Mask: Fulcrum
Wafers: TC3_2, TC3_5
Photo
HMDS
Spin coat: old resist @ 2 Krpm
Expose 20 sec
Develop: 2 1/2 min
Backside coating: thick resist @ 2krpm
Target mount to 4" quartz

STS1 etch
Recipe: MIT 59
TC3_2: 1 + 2 + 8 min + 5 min + 5 min + 10min+10min+5min+10min
with a lot of patch and etch
TC3_5: 60 min + 90+18

Asher remove resist
All wafers are detached from quartz mount wafer

Nanostrip clean: 4 hrs

BOE etch:
TC3_2, TC3_5: 20 min (for 1.5 um)

Piranha: 5:1 : H2SO4:H2O2

Spin dry: 4 min at 1 Krpm sandwiched between dummy wafers

5. Thermal Oxidation

Clean wafers for thermal oxidation per Bernard
1. Piranha clean 5:1 for 10 min
2. Rinse in bucket of water

3. HF dip: 10:1 for 10 sec
4: Rinse in bucket of water
5. Spin dry 5 min @ 1 krpm, one by one sandwiched by quartz wafers

Thermal oxidation
Target: 300 nm
Sequence:

Step	Time (min)	Gas
1	1	N2
2	20	O2
3	11	N2
4	38	H2+O2
5	20	O2
6	20	N2
7	Halt	

Oxide thickness: source side (mm)

flat	right	top	left	bottom
.2686	.2686	.2678	.2693	.2699

6. Anodic bond
1. TC3_2+TCB_9
(TCB_9: with seat etched; etch pit 10. 6852 mm)
a. Bond TC3_2 to a top pyrex: 6 min
b. Bond stack to TCB_9: 8 min

2. TC3_5+TCB_1
(TCB_1: no capacitor seat etched; etch pit 11.68 mm)
a. Bond TC3_5 to top pyrex wafer
b. Mechanically clamped or die-level bond to TCB_1 pieces

7. Plasmaquest etch oxide
Recipe: xyoxide
Target: .28 um
Total time: 12 min

8. Diesaw TC3_2 stacks
Diesaw TC3_5 stack and TCB_1

B.2 Fabrication process for bottom wafer

Wafers #: 10 device wafers

1. Piranha clean all pyrex wafers received (50 total)

2. Mask 1: Align
   TCB1 - TCB10
   Photolithography
      Spin Coat: thin resist @2 Krpm
      Prebake: 30 min @ 90 degC
      Expose: EV1 for 2 sec
      Develope: + 1 1/2 min

   Mask 2: Capacitor Seat
   Only for TCB5 - TCB10
      Expose: EV1 for 2 sec
      Develope: 2 1/2 min

      Postbake all wafers: 60 min @ 90 degC

   BOE etch
   TC1-P1 - TC1-P5
   Time: 30 min
   Depth:

	Wafer 1	Wafer 2
Avg	0.80035	0.7647
Etch rate	0.0267 um/min	0.0255 um/min

   TCB5 - TCB10
   Target: 1 mm
   Time: 40 min
   Depth: ~1.04 um

   TCB10 demolished

3. Mask 3: Actuator Bottom
   Ebeam feature side
   Target: Cr: 200 A
      Au: 1000 A
   Deposition rate: Cr: 5 A/sec
      Au: 10 A/sec

Ebeam back side
Target: same
Deposition rate: Cr: 5 A/sec
Au: 5 A/sec

Photolithography
Spin Coat: thin resist @3 Krpm
Prebake: 30 min @ 90 degC
Expose: 2 sec
Develope: 3 min (1 1/2 should be enough)
Back side resist: standard 3 Krpm
Cover alignment marks with thin pr
Postbake: 30 min @ 120 degC

Pyrex Etch
Solutions: 1. Aqua regina for gold etch
HCL:HNO3=3:1
2. Cr-7 etchant for Cr etch
3. Pyrex etchant
H2O:HNO3:HF=660:140:200
Temperature: ~33 °C (kept in a water bath)
a. Use the small beaker mixing pyrex etchant
b. Use the ultrasonic heater and heat up a buck of water and the beaker with solution to 38 degC; monitor the temperature of the solution constantly.

First batch: TCB1, TCB2
Temperature: 33.5 degC
Time: 12.67 min

	TCB1	TCB2
Etch depth (um)	11.68	11.96
Etch rate (um/min)	0.92	0.94

2nd batch: TCB3,4,5
Temperature: 33 degC
Time: 11.69 min

	TCB3	TCB4	TCB5
Etch depth	10.25	9.83	10.23
Etch rate	0.88	0.84	0.88

3rd batch: TCB6,7,8,9
Temperature: 33 degC
Time: 12.45 min

	TCB6	TCB7	TCB8

Etch depth	10.41	10.15	10.30
Etch rate	0.84	0.82	0.83

4. Mask 4: Metal_Bottom

Photolithography

Spin coat: image reversal resist @ 1 Krpm

Prebake: 90 °C for 30 min

Expose with mask Metal_Bottom: EV1 for 3 sec

Postbake: 20 min @ 105 degC (Note: Kurt changed this to 30 min @ 90/95 °C recently)

Flood exposure: EV1 for 1 min

Develop: AZ 422 for 5 min

Ebeam metal

Target:

Ti: 100 A

Au: 5000 A

Acetone lift-off (soak in acetone for a day, then place in an ultrasound bath at low power setting to shake off the metal for about 1 min. Then clean in acetone, methanol and isopropanol)

Appendix C

Matlab Scripts

C.1 Before Pull-In

1. pullin.m

```
function [center_deflection]=pullin(V)
clear all
close all
clc
%  This program finds the pull-in voltage of the electrostatic zipping actuator
%  actuator.
% Definitions:
%  a=fulcrum outer radius (also fulcrum location)
%  b=plate outer radius
%  D=flexural rigidity of the plate D=E*h^3/12*(1-nu^2)
%  nu=Poisson ratio
%  g=air gap thickness
%  h=thickness of plate
%  t=thickness of shell
%  l=height of fulcrum
%  c=thickness of oxide
%  g_eq=equivalent air gap thickness (air+oxide)
%  V=input voltage
%
global epsilon epsilon_ox g g_eq a b c t h l A D Df E V nu zeta beta yi step
%----------------------------------
% Enter design parameters:
Actuator_inner_radius=500;     %um
Actuator_outer_radius=1750;    %um
Top_Plate_thickness=17;        %um
Fulcrum_thickness=50;          %um
Gap=10;                        %um
```

```
Capacitor_diameter=400;       %um
Oxide_thickness=0.27;         %um
Fulcrum_height=340;           %um
Capacitor_initial_gap=0;      %um
%---------------------------------
% Dimensions of the plate
a=Actuator_inner_radius+Fulcrum_thickness;      %um
b=Actuator_outer_radius;      %um
h=Top_Plate_thickness;        %um
t=Fulcrum_thickness;          %um
g=Gap;                        %um
cd=Capacitor_diameter;        %um
c=Oxide_thickness;            %um
go=Capacitor_initial_gap;     %um
l=Fulcrum_height;             %um
%---------------------------------
% Material properties of the plate, uMKS units
nu=0.25;
E=169*10^3;
D=E*h^3/(12*(1-nu^2));
Df=E*t^3/(12*(1-nu^2));
epsilon=8.85*10^-6;
epsilon_ox=3.9;
g_eq=g+c/epsilon_ox;
%---------------------------------
% Derived values
beta=(E*t/(4*a^2*Df))^.25;
A=a/(b-a);
%---------------------------------
%*********************************************************************
V0=0;
x=[0:0.01:1];
yi=x*0;
step=0;
%apply incremental voltage to find the pull-in voltage
for i=1:15
   U(i)=V0
   step=i;
   zeta=(b-a)^4*epsilon*U(i).^2/(2*D*g^3);
%call the function
   [xint,sxint]=pullin_fun(V);
   %use the solution for the next guess function
   yi=sxint;
   if V0<101
   V0=V0+10;
   else
```

```
    V0=V0+0.2;
  end
%plot the results
  W=sxint(1,:);      %deflection
  dW=sxint(2,:);     %rotation
  ddW=sxint(3,:);    %2nd derivative
  r=xint*(b-a)+a;
  w=W*g;
  dw=dW*g/(b-a);
  ddw=ddW*g/(b-a)^2;
%resulted (internal) moment
  M_outerplate=-D*(ddw+nu./r.*dw)*2*pi.*r;
  M1=-D*(ddw(1)+nu/a*dw(1))*2*pi*a;
%the outer deflectioin
  outer_deflection=w(1001);
  delta_outer(i)=outer_deflection;
  rotation_at_a_outerplate=dw(1);
%compute capacitance change of the actuator
  Cact(i)=0;
  for j=1:1:1000
    Cact(i)=epsilon*2*pi*r(j)*(r(j+1)-r(j))/(w(j)+g+c/epsilon_ox)+Cact(i);
  end
  Cact(i);
%total force
  F(i)=force_intg(r,w,U(i));
%vertical deflection of fulcrum
  axial_defl(i)=F(i)*l/2/pi/a/t/E;
%center plate
  W3=sxint(5,:);
  dW3=sxint(6,:);
  ddW3=sxint(7,:);
  r3=xint*a;
  w3=W3*g;
  dw3=dW3*g/a;
  ddw3=ddW3*g/a^2;
  center_defl=w3(1);
  delta_center(i)=center_defl;
  center_translation(i)=w3(955);
  %compensated center deflection
  center_defl_comp(i)=delta_center(i)-axial_defl(i)-center_translation(i);
  rotation_at_a_centerplate=dw3(101);
  if r3==0
    M_centerplate=0;
  else
    M_centerplate=-D*(ddw+nu./r3.*dw)*2*pi.*r3;
  end
```

```
%compute capacitance change of the capacitor
   Ccap(i)=0;
   for j=1:1:364
      Ccap(i)=epsilon*2*pi*r3(j)*(r3(j+1)-r3(j))/(w3(j)+go+c/epsilon_ox)+Ccap(i);
   end
   Ccap(i)
%
%fulcrum
   W2=sxint(8,:);
   dW2=sxint(9,:);
   ddW2=sxint(10,:);
   x=xint*l;
   y=W2*g;
   dy=dW2*g/l;
   ddy=ddW2*g/l^2;
   rotation_at_a_fulcrum=dy(1);
   M_fulcrum=-Df*ddy*2*pi*a;
%
%plot the deflection
   figure(1)
   subplot(3,2,1)
   plot(r,w,r3,w3)
   title('a) Plate Displacement vs. Radius')
   xlabel('Radius (micron)')
   ylabel('Displacement (micron)')
   hold on
%
%plot the rotation
   figure(1)
   subplot(3,2,2)
   plot(r,dw,r3,dw3)
   title('b) Plate Rotation vs. Radius')
   xlabel('Radius (micron)')
   ylabel('Rotation (micron)')
   hold on
%
%plot the fulcrum deflection
   figure(1)
   subplot(3,2,3)
   plot(x,y)
   title('c) Fulcrum Displacement vs. Length')
   xlabel('Length (micron)')
   ylabel('Displacement (micron)')
   hold on
%
%plot the fulcrum rotation
```

```
    figure(1)
    subplot(3,2,4)
    plot(x,dy)
    title('d) Fulcrum Rotation vs. Length')
    xlabel('Length (micron)')
    ylabel('Rotation (micron)')
    hold on
%
%plot the moment of the plate and the fulcrum
    figure(2)
    subplot(2,1,1)
    plot(r,M_outerplate,r3,M_centerplate)
    title('a) Plate Moment vs. Radius')
    xlabel('Radius (micron)')
    ylabel('Internal Moment (microNewton*micron)')
    hold on
%
    figure(2)
    subplot(2,1,2)
    plot(x,M_fulcrum)
    title('b) Fulcrum Moment vs. Length')
    xlabel('Length (micron)')
    ylabel('Fulcrum Moment (microNewton*micron)')
    hold on
end
%save U, outer deflection and center deflection in a text file
    defl=[U;delta_outer;center_defl_comp;Cact;Ccap;F];
    fid=fopen('pullin_data.txt','w');
    fprintf(fid,'%6.2f %12.5f %12.5f %12.5f %12.5f %12.5f\r',defl);
    fclose(fid);
%**************************************************************************
%plot the outer deflection as function of voltage
figure(1)
subplot(3,2,5)
plot(U,delta_outer)
title('e) End Deflection vs. Voltage')
xlabel('Voltage (V)')
ylabel('End Deflection (micron)')
%
%plot the rotation of the fulcrum
figure(1)
subplot(3,2,6)
plot(U,delta_center,U,center_defl_comp,':')
title('f) Center Deflection vs. Voltage')
xlabel('Voltage (V)')
ylabel('Center Deflection (micron)')
```

```
legend('Original','Compensated')
%
%plot the capacitance change
figure
subplot(1,2,1)
plot(U,Cact)
title('Capacitance Change of Capacitor vs. Voltage')
xlabel('Voltage (V)')
ylabel('Capacitance (pF)')
%
subplot(1,2,2)
plot(U,Ccap)
title('Capacitance Change of Actuator vs. Voltage')
xlabel('Voltage (V)')
ylabel('Capacitance (pF)')
%
%plot the total electrostatic force
figure
subplot(1,2,1)
plot(U,F)
title('Total Electrostatic Force vs. Voltage')
xlabel('Votlage (V)')
ylabel('Force (uN)')
%plot electrostatic force as function of center deflection
subplot(1,2,2)
plot(center_defl_comp,F)
title('Total Electrostatic Force vs. Center Deflection')
xlabel('Center Deflection (micron)')
ylabel('Force (uN)')
%**************************************************************************
%function to find the total electrostatic foce
% ------------------------------------------------------------------
function force=force_intg(r,w,v)
%
global epsilon g epsilon_ox c A b g_ansys
force=0;
for j=1:1:(size(r,2)-1)
   force=1/2*epsilon*v^2/(g+w(j)+c/epsilon_ox)^2*2*pi*r(j)*(r(j+1)-r(j))+force;
end
%**************************************************************************
```

2. pullin_fun.m

```
function [xint,Sxint]=pullin_fun(a)
%
%  Solve del^4 W = B / (g_eq - W)^2
```

```
%  subject to W(a)=0          assume zero fulcrum end deflection
%             W'(a)=-phi      rotation at fulcrum end
%             M(b)=0;         zero shear force at outer edge
%             V(b)=0;         zero moment at outer edge
%  here B=epsilon*V^2/(2*D)--D is bending stiffness
%
global epsilon epsilon_ox g g_eq a b c t h l A D V nu zeta yi step
%*************************************************************************
   solinit = bvpinit([0:0.01:1],@allinit);
   sol = bvp4c(@allode,@allbc,solinit);
   xint = [0:0.01:1];
   Sxint = bvpval(sol,xint);
%*************************************************************************
%define the function elements of the radial outerplate
%*************************************************************************
%first, need to supply a guess function
% ------------------------------------------------------------------------
function yinit = allinit(x);
global yi step
if step > 1
   num=round(x*100+1);
   yinit=yi(:,num);
else
yinit = [0;
       0;
       0;
       0;
       0;
       0;
       0;
       0;
       0;
       0;
       0];
end
%*************************************************************************
%next, set up odes for the problem
% ------------------------------------------------------------------------
function dydx = allode(x,y)
global epsilon g_eq B zeta A g beta l
dydx = [y(2);
   y(3);
   y(4);
   -zeta/(g_eq/g+y(1))^2-2*y(4)/(x+A)+y(3)/((x+A)^2)-y(2)/((x+A)^3);
   y(6);
   y(7);
```

```
   0;
   y(9);
   y(10);
   y(11);
   -4*beta^4*l^4*y(8)];
if x==0
   dydx(7)=0;
else
   dydx(7)=-y(7)/x+y(6)/x^2;
end
%
%*************************************************************************
%enforce boundary conditions
% -------------------------------------------------------------------------
function res = allbc(ya,yb)
global epsilon g epsilon_ox phi a b nu A D Df l
res = [ya(1); %deflection at r=a is zero
   D*(ya(3)+nu/A*ya(2))-(D*(yb(7)+nu*yb(6))/a^2-Df*ya(10)/l^2)*(b-a)^2;
   yb(3)+nu/(1+A)*yb(2);
   yb(4)+1/(1+A)*yb(3)-1/(1+A)^2*yb(2);
   yb(5);
   ya(6);
   yb(6)-ya(2)/(b-a)*a;
   yb(8);
   yb(9);
   ya(8);
   ya(9)-ya(2)/(b-a)*l];
%
```

C.2 Zip-in

1. zipin.m

```
function [center_deflection]=zipin(V)
clear all
close all
clc
%  This program finds the pin-down position of the electrostatic zipping actuator
%  actuator during zip-in actuation stage.
global epsilon epsilon_ox g g_eq a b c t h l A D Df E V nu beta g_ansys gamma_guess
%---------------------------------
% Enter design parameters:
Actuator_inner_radius=500;      %um
Actuator_outer_radius=1750;     %um
Top_Plate_thickness=17;         %um
```

```
Fulcrum_thickness=50;          %um
Gap=10;                        %um
Capacitor_diameter=400;        %um
Oxide_thickness=0.27;          %um
Fulcrum_height=340;            %um
Capacitor_initial_gap=0;       %um
%---------------------------------
%---------------------------------
% Dimensions of the plate
a=Actuator_inner_radius+Fulcrum_thickness;      %um
b=Actuator_outer_radius;       %um
h=Top_Plate_thickness;         %um
t=Fulcrum_thickness;           %um
g=Gap;                         %um
cd=Capacitor_diameter;         %um
c=Oxide_thickness;             %um
go=Capacitor_initial_gap;      %um
l=Fulcrum_height;              %um
%---------------------------------
% Material properties of the plate, uMKS units
nu=0.25;
E=169*10^3;
D=E*h^3/(12*(1-nu^2));
Df=E*t^3/(12*(1-nu^2));
epsilon=8.85*10^-6;
epsilon_ox=3.9;
g_eq=g+c/epsilon_ox;
g_ansys=g_eq-0.8;
%---------------------------------
% Derived values
beta=(E*t/(4*a^2*Df))^.25;
A=a/(b-a);
%---------------------------------
%*********************************************************************************
V0=110;
gamma_guess=(1750-a)^4*epsilon*V0^2/(2*D*g^3)
for i=1:8
   V=V0;
   U(i)=V0;
%call the function
   [xint,sxint,s]=zipin_fun(V);
   Pin_down_pos(i)=s;
   gamma_guess=(s-a)^4*epsilon*V^2/(2*D*g^3);
%the outer plate
   W=sxint(1,:);
   dW=sxint(2,:); %rotation
```

```
  ddW=sxint(3,:);
  dddW=sxint(4,:);
  r=xint*(s-a)+a;;
  w=W*g;
  dw=dW*g/(s-a);
  ddw=ddW*g/(s-a)^2;
  dddw=dddW*g/(s-a)^3;
  d2w_dr2_end=ddw(1001);
%net electrostatic force
  F(i)=force_intg(r,w,V)
%vertical deflection of fulcrum
  axial_defl(i)=F(i)*l/2/pi/a/t/E
  V0=V0+10;
%resulted (internal) moment at r=a
  M1=-D*(ddw(1)+nu/a*dw(1))*2*pi*a;
  Mend=-D*ddw(1001);
%resulted shear force at r=s
  Q_s=D*(dddw(1001)+1/s*ddw(1001)-1/s^2*dw(1001));
%the outer deflectioin
  outer_deflection=w(1001)
  delta_outer(i)=outer_deflection;
  rotation_at_a_outerplate=dw(1);
%compute capacitance change of the actuator
  Cact(i)=0;
  for j=1:1:1000
    Cact(i)=epsilon*2*pi*r(j)*(r(j+1)-r(j))/(w(j)+g+c/epsilon_ox)+Cact(i);
  end
  for k=1:1001
    R(k)=s+k*(b-s)/1000;
  end
  for m=1:1000
    Cact(i)=epsilon*2*pi*R(l)*(R(l+1)-R(l))/(c/epsilon_ox)+Cact(i);
  end
  Cact(i)
%center plate
  W3=sxint(5,:);
  dW3=sxint(6,:);
  r3=xint*a;
  w3=W3*g;
  dw3=dW3*g/a;
  center_defl=w3(1);
  %center translation
  center_translation(i)=w3(955);
  delta_center(i)=center_defl;
  %compensated center deflection
  center_defl_comp(i)=delta_center(i)-axial_defl(i)-center_translation(i);
```

```
    rotation_at_a_centerplate=dw3(1001);
  %compute capacitance change of the capacitor
    Ccap(i)=0;
    for j=1:1:365
      Ccap(i)=epsilon*2*pi*r3(j)*(r3(j+1)-r3(j))/(w3(j)+go+c/epsilon_ox)+Ccap(i);
    end
  %
  %fulcrum
    W2=sxint(8,:);
    dW2=sxint(9,:);
    x=xint*l;
    y=W2*g;
    dy=dW2*g/l;
    rotation_at_a_fulcrum=dy(1)
  %
  %plot the deflection
    subplot(3,2,1)
    plot(r,w,r3,w3)
    title('a) Plate Displacement vs. Radius')
    xlabel('Radius (micron)')
    ylabel('Displacement (micron)')
    hold on
  %
  %plot the rotation
    subplot(3,2,2)
    plot(r,dw,r3,dw3)
    title('b) Plate rotation vs. Radius')
    xlabel('Radius (micron)')
    ylabel('Rotation (micron)')
    hold on
  %
  %plot the normalized deflection
  polyfit(xint(1,:),sxint(1,:),4)
    subplot(3,2,3)
    plot(xint(1,:),sxint(1,:))
    title('c) Normalized plate Displacement')
    xlabel('Normalized Radius (micron)')
    ylabel('Normalized Displacement (micron)')
    hold on
  %
  end
  %save U, outer deflection and center deflection in a text file
    defl=[U;delta_outer;center_defl_comp;Pin_down_pos;Cact;Ccap;F];
    fid=fopen('mat_defl_zipin.txt','w');
    fprintf(fid,'%6.2f %12.5f %12.5f %12.5f %12.5f %12.5f %12.5f\r',defl);
    fclose(fid);
```

```
%*************************************************************************
%plot s as function of voltage
subplot(3,2,4)
plot(U,Pin_down_pos)
title('d) Pin-Down Position vs. Voltage')
xlabel('Voltage (V)')
ylabel('Pin Down Position (micron)')
%
%plot the center deflection as function of voltage
subplot(3,2,5)
plot(U,delta_center, U, center_defl_comp, ':')
title('e) Plate Center Deflection vs. Voltage')
xlabel('Voltage (V)')
ylabel('Center Deflection (micron)')
legend('Original','Compensated')
%
%plot the center deflection as function of s
subplot(3,2,6)
plot(Pin_down_pos,delta_center,Pin_down_pos,center_defl_comp, ':')
title('f) Plate Center Deflection vs. Pin-Down Position')
xlabel('Pin Down Position (micron)')
ylabel('Center Deflection (micron)')
legend('Original','Compensated')
%
%plot the capacitance change
figure
subplot(1,2,1)
plot(U,Cact)
title('Capacitance Change of Actuator vs. Voltage')
xlabel('Voltage (V)')
ylabel('Capacitance (pF)')
%
subplot(1,2,2)
plot(U,Ccap)
title('Capacitance Change of Capacitor vs. Voltage')
xlabel('Voltage (V)')
ylabel('Capacitance (pF)')
%
%plot the total electrostatic force
figure
subplot(1,2,1)
plot(U,F)
title('Net Electrostatic Force vs. Voltage')
xlabel('Votlage (V)')
ylabel('Force (microNewton)')
%plot the net electrostatic force vs. center deflection
```

```
subplot(1,2,2)
plot(center_defl_comp,F)
title('Net Electrostatic Force vs. Center Deflection')
xlabel('Center Deflectioin (micron)')
ylabel('Force (microNewton)')
%*************************************************************************
%function to find the net electrostatic foce
% ----------------------------------------------------------------------
function force=force_intg(r,w,v)
%
global epsilon g epsilon_ox c
force=0;
for j=1:1:(size(r,2)-1)
   force=1/2*epsilon*v^2/(g+w(j)+c/epsilon_ox)^2*2*pi*r(j)*(r(j+1)-r(j))+force;
end
%*************************************************************************
```

2. zipin_fun.m

```
function [xint,Sxint,s]=zipin_fun(V)
%
global epsilon epsilon_ox g g_eq a b c t h l A D Df V nu gamma g_ansys s
%*************************************************************************
   solinit = bvpinit([0:0.01:1],@allinit,gamma);
   sol = bvp4c(@allode,@allbc,solinit);
   xint = [0:0.01:1];
   Sxint = bvpval(sol,xint);
   zeta=sol.parameters;
   s=zeta*(2*D*g^3/(epsilon*V^2))^(1/4)+a;
%*************************************************************************
%define the function elements of the radial outerplate
%*************************************************************************
%first, need to supply a guess function
% ---------------------------------------------------------------------------
function yinit = allinit(x);
%
global g g_ansys g_eq
rotation=-0.001;
p=[ 1 1 1 1; 1 0 0 0; 1 2 3 4; 0 2 6 12]^(-1)*[-g_ansys/g; rotation; 0; 0 ];
yinit =[ p(1)*x+p(2)*x^2+p(3)*x^3+p(4)*x^4;
      p(1)+2*p(2)*x+3*p(3)*x^2+4*p(4)*x^3;
      2*p(2)+6*p(3)*x+12*p(4)*x^2;
      6*p(3)+24*p(4)*x;
      0;
      0;
      0;
```

```
      0;
      0;
      0;
      0];
%
%*************************************************************************
%next, set up odes for the problem
% -------------------------------------------------------------------------
function dydx = allode(x,y,zeta)
%
global epsilon g_eq g beta l D V a
s=zeta*(2*D*g^3/(epsilon*V^2))^(1/4)+a;
A=a/(s-a);
%
dydx = [y(2);
  y(3);
  y(4);
  -zeta^4/(g_eq/g+y(1))^2-2*y(4)/(x+A)+y(3)/((x+A)^2)-y(2)/((x+A)^3);
  y(6);
  y(7);
  0;
  y(9);
  y(10);
  y(11);
  -4*beta^4*l^4*y(8)];
if x==0
  dydx(7)=0;
else
  dydx(7)=-y(7)/x+y(6)/x^2;
end
%
%*************************************************************************
%enforce boundary conditions
% -------------------------------------------------------------------------
function res = allbc(ya,yb,zeta)
%
global epsilon g epsilon_ox phi a nu D Df l c V a g_ansys
H=sqrt(epsilon*epsilon_ox/(2*D*c));
s=zeta*(2*D*g^3/(epsilon*V^2))^(1/4)+a;
A=a/(s-a);
res = [ya(1);
  D*(ya(3)+nu/(A)*ya(2))-(D*(yb(7)+nu*yb(6))/a^2-Df*ya(10)/l^2)*(s-a)^2;
  yb(1)+g_ansys/g;
  yb(2);
  yb(3);
  yb(5);
```

```
   ya(6);
   yb(6)-ya(2)/(s-a)*a;
   yb(8);
   yb(9);
   ya(8);
   ya(9)-ya(2)/(s-a)*l];
%
```

C.3 Release

1. release.m

```
function [V]=release(b)
clear all
close all
clc
%  This program finds the release voltage of a given membrane with radius
global epsilon epsilon_ox g g_eq a c t h l A D Df E nu beta g_ansys
%----------------------------------
% Enter design parameters:
Actuator_inner_radius=500;     %um
Actuator_outer_radius=1750;    %um
Top_Plate_thickness=17;        %um
Fulcrum_thickness=50;          %um
Gap=10;                        %um
Capacitor_diameter=400;        %um
Oxide_thickness=0.27;          %um
Fulcrum_height=340;            %um
Capacitor_initial_gap=0;       %um
%----------------------------------
%----------------------------------
% Dimensions of the plate
a=Actuator_inner_radius+Fulcrum_thickness;      %um
b=Actuator_outer_radius;       %um
h=Top_Plate_thickness;         %um
t=Fulcrum_thickness;           %um
g=Gap;                         %um
cd=Capacitor_diameter;         %um
c=Oxide_thickness;             %um
d=Fulcrum_height;              %um
go=Capacitor_initial_gap;      %um
l=Fulcrum_height;              %um
%----------------------------------
% Material properties of the plate, uMKS units
nu=0.25;
E=169*10^3;
```

```
D=E*h^3/(12*(1-nu^2));
Df=E*t^3/(12*(1-nu^2));
epsilon=8.85*10^-6;
epsilon_ox=3.9;
g_eq=g+c/epsilon_ox;
g_ansys=g_eq-0.8;
%---------------------------------
% Derived values
beta=(E*t/(4*a^2*Df))^.25;
A=a/(b-a);
%---------------------------------
%*********************************************************************************
%call the function
   [xint,sxint,V]=release_fun(b);
   W=sxint(1,:);
   dW=sxint(2,:); %rotation
   ddW=sxint(3,:);
   dddW=sxint(4,:);
   r=xint*(b-a)+a;;
   w=W*g;
   dw=dW*g/(b-a);
   ddw=ddW*g/(b-a)^2;
%resulted (internal) moment at r=a
   M1=-D*(ddw(1)+nu/a*dw(1))*2*pi*a
%the outer deflectioin
   rotation_at_a_outerplate=dw(1)
%total force
   F=force_intg(r,w,V);
%vertical deflection of fulcrum
   axial_defl=F*l/2/pi/a/t/E;
%center plate
   W3=sxint(5,:);
   dW3=sxint(6,:);
   r3=xint*a;
   w3=W3*g;
   dw3=dW3/a*g;
   center_defl=w3(1)
   %center translation
   center_translation=w3(955);
   center_defl_comp=center_defl-axial_defl-center_translation
   rotation_at_a_centerplate=dw3(1001);
%fulcrum
   W2=sxint(8,:);
   dW2=sxint(9,:);
   x=xint*l;
   y=W2*g;
```

```
   dy=dW2/l*g;
   rotation_at_a_fulcrum=dy(1);
%*************************************************************************
%
figure
%plot the deflection
subplot(2,2,1)
plot(r,w,r3,w3)
title('Plate Displacement vs. Radius')
xlabel('Radius (um)')
ylabel('Plate Displacement (um)')
%
%plot the rotation
subplot(2,2,2)
plot(r,dw,r3,dw3)
title('Plate rotation vs. Radius')
xlabel('Radius (um)')
ylabel('Rotation')
%
%plot the deflection of the fulcrum
subplot(2,2,3)
plot(x,y)
title('Fulcrum Deflection vs. Length')
xlabel('Fulcrum Length (um)')
ylabel('Fulcrum Deflection (um)')
%
%plot the rotation of the fulcrum
subplot(2,2,4)
plot(x,dy)
title('Fulcrum Rotation vs. Length')
xlabel('Fulcrum Length (um)')
ylabel('Fulcrum Rotation')
%
%*************************************************************************
%function to find the total electrostatic foce
% ------------------------------------------------------------------
function force=force_intg(r,w,v)
%
global epsilon g epsilon_ox c A b g_ansys
force=0;
for j=1:1:(size(r,2)-1)
   force=1/2*epsilon*v^2/(g+w(j)+c/epsilon_ox)^2*2*pi*r(j)*(r(j+1)-r(j))+force;
end
%*************************************************************************
```

2. release_fun.m

```
function [xint,sxint,V]=release_fun(b)
%
%  Solve del^4 W = B / (g_eq - W)^2
%  subject to W(a)=0          assume zero fulcrum end deflection
%          W'(a)=-phi         rotation at fulcrum end
%          M(b)=0;            zero shear force at outer edge
%          V(b)=0;            zero moment at outer edge
global epsilon epsilon_ox g g_eq a b c t h l A D Df E nu beta g_ansys
%*************************************************************************
   solinit = bvpinit(linspace(0,1,1000),@allinit,0.72);    %define range of integration
   sol = bvp4c(@allode,@allbc,solinit);
   xint = [0:0.001:1];
   sxint = bvpval(sol,xint);
   zeta=sol.parameters;
   V=zeta*sqrt(2*D*g^3/(b-a)^4/epsilon);
%*************************************************************************
%define the function elements of the radial outerplate
%*************************************************************************
%first, need to supply a guess function
% ------------------------------------------------------------------------------
function v = allinit(x);
%
global g g_ansys g_eq nu A
rotation=-0.001;
p=[ 1 1 1 1; 1 0 0 0; nu/(1+A) 2*nu/(1+A)+2 3*nu/(1+A)+6 4*nu/(1+A)+12; -1/(1+A)^2 2/
(1+A)-2/(1+A)^2 6+6/(1+A)-3/(1+A)^2 24+12/(1+A)-4/(1+A)^2]^(-1)*[-g_ansys/g; rotation; 0; 0
];
v =[ p(1)*x+p(2)*x^2+p(3)*x^3+p(4)*x^4;
     p(1)+2*p(2)*x+3*p(3)*x^2+4*p(4)*x^3;
     2*p(2)+6*p(3)*x+12*p(4)*x^2;
     6*p(3)+24*p(4)*x;
     0;
     0;
     0;
     0;
     0;
     0;
     0];
   %x=[0:0.01:1];
   %y=p(1)*x+p(2)*x.^2+p(3)*x.^3+p(4)*x.^4;
   %figure
   %plot(x,y)
%
%*************************************************************************
%next, set up odes for the problem
% ------------------------------------------------------------------------------
```

```
function dydx = allode(x,y,zeta)
%
global epsilon g_eq A g beta l
%
dydx = [y(2);
   y(3);
   y(4);
   -zeta^4/(g_eq/g+y(1))^2-2*y(4)/(x+A)+y(3)/((x+A)^2)-y(2)/((x+A)^3);
   y(6);
   y(7);
   0;
   y(9);
   y(10);
   y(11);
   -4*beta^4*l^4*y(8)];
if x==0
   dydx(7)=0;
else
   dydx(7)=-y(7)/x+y(6)/x^2;
end
%
%*************************************************************************
%enforce boundary conditions
% -------------------------------------------------------------------------
function res = allbc(ya,yb,zeta)
%
global epsilon g epsilon_ox a b nu A D Df l g_ansys
res = [ya(1); %deflection at r=a is zero
   yb(1)+g_ansys/g;
   yb(3)+nu/(1+A)*yb(2);
   D*(ya(3)+nu/A*ya(2))-(D*(yb(7)+nu*yb(6))/a^2-Df*ya(10)/l^2)*(b-a)^2;
   yb(4)+1/(1+A)*yb(3)-1/(1+A)^2*yb(2);
   yb(5);
   ya(6);
   yb(6)-ya(2)/(b-a)*a;
   yb(8);
   yb(9);
   ya(8);
   ya(9)-ya(2)/(b-a)*l];
%
```

C.4 MOS structure analysis for actuator

```
%This code calculates the threshold voltage of the actuator and returns
%the depletion thickness as function of actuation voltage. The goal is
```

```
%to find out whether the depletion layer is significantly large as to
%affect the calculation of the pull-in voltage characteristics

clear all
close all

k=1.38e-23;        %J/K, Boltzman constant
T=300;  %K, room temperature
q=1.6e-19;         %Coulomb, charge of an electron
Nv=3.1e19*1e6;     %m^(-3),
NA=7e18*1e6;       %m^(-3), Acceptor concentration
ni=10e10*1e6;      %m^(-3),
Wm=4.7             %eV, metal work function for Gold

epsilon_ox=3.9;    %relative permittivity of oxide
epsilon_si=11.9;   %relative permittivity of silicon
e=8.85e-12;        %F/m, vacumm permittivity

%calculate built-in voltage
Ws=4.04+1.1+k*T*log(NA/Nv);    %eV, work function for silicon
Phi_Bi=Ws-Wm                   %eV, built-in voltage

Phi_sth=2*k*T/q*log(NA/ni)     %surface potential threshold of silicon

g_ox=.27e-6;                   %m; thickness of oxide insulation
g_air=0e-6;                    %m; air gap
g_ox_eq=g_ox+g_air/3.9         %m; equivalent oxide thickness
C_ox=1/(g_ox/(epsilon_ox*e)+(g_air/e))     %F/m^2; capacitance per unit area

gamma=1/C_ox*sqrt(2*e*epsilon_si*q*NA)     %body factor coefficient

%calculate threshold voltage
Vth=-Phi_Bi+Phi_sth+gamma*sqrt(Phi_sth)    %V, threshold voltage

Max_xd=sqrt(2*epsilon_si*e*Phi_sth/q/NA)   %m, maximum depletion layer thicknness

%in depletion
V=[1:1:100];                               %V, applied voltage
x_d=epsilon_si*e/C_ox*(sqrt(1+4*(Phi_Bi+V)/gamma^2)-1);    %m, depletion thickness

plot(V,x_d)                    %plot depletion thickness as function of voltage
xlabel('Voltage (V)')
ylabel('Depletion layer thickness (m)')
title('Thickness of Depletion Layer vs. Applied Voltage')

Ld=sqrt(epsilon_si*e*k*T/q^2/NA)           %m, Debye length
```

```
x_inv=sqrt(2)*Ld                    %m, inversion layer thickness

Phi_s=gamma^2/4*(sqrt(1+4*(Phi_Bi+V)/gamma^2)-1).^2;      %V, surface potential of sili-
con
figure
plot(V,Phi_s)                       % plot surface potential as function of voltage
xlabel('Voltage (V)')
ylabel('Surface Potential (V)')
title('Surface Potential of Silicon vs. Applied Voltage')
```

C.5 MOS structure analysis for capacitor and Metal-Semiconductor interface for electrode contact

```
%This code analyzes the MOS structure of the capacitor

clear all;
close all;

k=1.38e-23;          %J/K, Boltzman constant
T=300;               %K, room temperature
q=1.6e-19;           %Coulomb, charge of an electron
NA=7e18*1e6;         %m^(-3), Acceptor concentration
Phi_Bi=0.44;         %V, built-in voltage as calculated from the actuator case
ni=10e10*1e6;
Phi_sth=2*k*T/q*log(NA/ni)  %V, surface potential threshold of silicon

epsilon_ox=3.9;      %relative permittivity of oxide
epsilon_si=11.9;     %relative permittivity of silicon
epsilon=8.85e-12;    %F/m, vacuum permittivity
r=200e-6;            %m, radius of the capacitor
A=pi*r^2;            %m^2, area of the capacitor

g_ox=.27e-6;         %m, thickness of oxide insulation
g_air=500e-9;        %m, air gap
C_air=epsilon*A/g_air   %m, equivalent oxide thickness
C_ox=epsilon*epsilon_ox*A/g_ox     %F, capacitance of oxide
C_total=1/(1/C_air+1/C_ox)         %F, total capacitance

gamma=1/C_total/A*sqrt(2*epsilon*epsilon_si*q*NA)    %body factor coefficient

Vth=-Phi_Bi+Phi_sth+gamma*sqrt(Phi_sth)       %V, threshold voltage

V=0.5;               %V, voltage signal used in measurement
```

```
C_corrected=C_total/sqrt(1+4*(V+Phi_Bi)/gamma^2)    %F, capacitance after MOS correction


%Calculation of metal-semiconductor interface for the electrode contact
depletion_thickness=sqrt(2*epsilon*epsilon_si*Phi_Bi/q/NA)
depletion_capacitance=epsilon*epsilon_si*pi*(1.5e-3)^2/depletion_thickness
```

C.6 Design Studies

1. pullin_study.m

```
function [V, center_deflection,center_deflection_com]=pullin_study(g,t)
clear all
close all
clc
%This script finds the pull-in voltage as function of fulcrum thickness and gap thickness
%
global epsilon epsilon_ox g g_eq a b c t h l A D Df E V nu beta zeta_guess g_ansys s
%----------------------------------
% Enter design parameters:
Fulcrum_inner_radius=500;      %um
Actuator_outer_radius=1750;    %um
Capacitor_diameter=400;        %um
Oxide_thickness=0.27;          %um
Fulcrum_height=340;            %um
Capacitor_initial_gap=0.1;     %um
s=1750;
%----------------------------------
%----------------------------------
% Dimensions of the plate
b=Actuator_outer_radius;       %um
cd=Capacitor_diameter;         %um
c=Oxide_thickness;             %um
d=Fulcrum_height;              %um
go=Capacitor_initial_gap;      %um
l=Fulcrum_height;              %um
%----------------------------------
% Material properties of the plate, uMKS units
nu=0.25;
E=169*10^3;
epsilon=8.85*10^-6;
epsilon_ox=3.9;
%*************************************************************************
h=20;                    %plate thickness
```

```
V0=110;                    %initial guess for the pull-in voltage
for k=1:2
  D=E*h^3/(12*(1-nu^2));     %flexural regidity of plate
  t=50;                    %initial fulcrum thickness
for i=1:10
  T(i)=t;
  a=Fulcrum_inner_radius+t;  %actuator inner radius
  Df=E*t^3/(12*(1-nu^2));    %flexural regidity of fulcrum
  beta=(E*t/(4*a^2*Df))^.25; %constant
  A=a/(s-a);           %normalization factor
  g=10;
  for j=1:8
    G(j)=g;
    g_eq=g+c/epsilon_ox;    %equivalent air gap thickness
    g_ansys=g+c/epsilon_ox-0.8;    %maximum displacement from ANSYS
    zeta_guess=sqrt((s-a)^4*epsilon*V0^2/(2*D*g^3));  %guess for the unknown zeta
%call the function
    [xint,sxint,V]=pullin_study_fun(g,t);
    V0=V;
    U(i,j)=V
    W=sxint(1,:);
    dW=sxint(2,:);
    ddW=sxint(3,:);
    dddW=sxint(4,:);
    r=xint*(s-a)+a;
    w=W*g;
    dw=dW*g/(s-a);
    ddw=ddW*g/(s-a)^2;
    dddw=dddW*g/(s-a)^3;
%resulted (internal) moment at r=a
    M1(i,j)=-D*(ddw(1)+nu/a*dw(1))*2*pi*a;
%total force
    F(i,j)=force_intg(r,w,V);
%vertical deflection of fulcrum
    axial_defl(i,j)=F(i,j)*l/2/pi/a/t/E;
%center plate
    W3=sxint(5,:);
    dW3=sxint(6,:);
    ddW3=sxint(7,:);
    r3=xint*a;
    w3=W3*g;
    dw3=dW3*g/a;
    ddw3=ddW3*g/a^2;
    center_deflection(i,j)=w3(1);
    center_deflection_comp(i,j)=w3(1)-axial_defl(i,j)
    M3(i,j)=-D*(ddw3(101)+nu/a*dw3(101))*2*pi*a;
```

```
      M_ratio(i,j)=M3(i,j)/M1(i);
%fulcrum
      W2=sxint(8,:);
      dW2=sxint(9,:);
      ddW2=sxint(10,:);
      x=xint*l;
      y=W2*g;
      dy=dW2*g/l;
      ddy=ddW2*g/l^2;
      rotation_at_a_fulcrum=dy(1);
      M2(i,j)=-Df*(ddy(1))*2*pi*a;
      g=g-1;
%
   end
    t=t-5;
    V0=U(i,1);
end
%
%plot pull-in voltage and center deflection
   figure(1)
   subplot(2,1,1)
   mesh(G,T,U)
   title('a)')
   xlabel('Air Gap Thickness (um)')
   ylabel('Fulcrum Thickness (um)')
   zlabel('Pull-In voltage (V)')
   hold on

   subplot(2,1,2)
   mesh(G,T,center_deflection_comp)
   title('b)')
   xlabel('Air Gap Thickness (um)')
   ylabel('Fulcrum Thickness (um)')
   zlabel('Center Deflection at Pull-In (um)')
   hold on
%
h=10;
V0=50;  %guess pull-in voltage for h=10, t=50 and g=10
end
%save the pull-in voltage and center deflection in a text file
   defl=[U;center_deflection_comp];
   fid=fopen('defl.txt','w');
   fprintf(fid,'8(%12.5f) 8(%12.5f)\r',defl);
   fclose(fid);
%*************************************************************************
%function to find the total foce
```

```
% ------------------------------------------------------------------------------
function force=force_intg(r,w,v)
%
global epsilon g epsilon_ox c A
force=0;
for j=1:1:(size(r,2)-1)
   force=1/2*epsilon*v^2/(g+w(j)+c/epsilon_ox)^2*2*pi*r(j)*(r(j+1)-r(j))+force;
end
%*******************************************************************************
```

2. pullin_study_fun.m

```
function [xint,Sxint,V]=pullin_study_fun(t)
%
%  Solve del^4 W = B / (g_eq - W)^2
%  subject to W(a)=0          assume zero fulcrum end deflection
%           W'(a)=-phi        rotation at fulcrum end
%           M(b)=0;           zero shear force at outer edge
%           V(b)=0;           zero moment at outer edge
%  here B=epsilon*V^2/(2*D)--D is bending stiffness
%
global epsilon epsilon_ox g g_eq a b c t h l A D Df V nu zeta_guess g_ansys s
%*******************************************************************************
   solinit = bvpinit([0:0.01:1],@allinit,zeta_guess);
   sol = bvp4c(@allode,@allbc,solinit);
   xint = [0:0.01:1];
   Sxint = bvpval(sol,xint);
   zeta=sol.parameters
   V=zeta*sqrt(2*D*g^3/(s-a)^4/epsilon);
%*******************************************************************************
%define the function elements of the radial outerplate
%*******************************************************************************
%first, need to supply a guess function
% ------------------------------------------------------------------------------
function yinit = allinit(x);
%
global g g_ansys g_eq
rotation=-0.001;
p=[ 1 1 1 1; 1 0 0 0; 1 2 3 4; 0 2 6 12]^(-1)*[-g_ansys/g; rotation; 0; 0 ];
yinit =[ p(1)*x+p(2)*x^2+p(3)*x^3+p(4)*x^4;
      p(1)+2*p(2)*x+3*p(3)*x^2+4*p(4)*x^3;
      2*p(2)+6*p(3)*x+12*p(4)*x^2;
      6*p(3)+24*p(4)*x;
      0;
      0;
      0;
```

```
      0;
      0;
      0;
      0];
%
%*************************************************************************
%next, set up odes for the problem
% -------------------------------------------------------------------------
function dydx = allode(x,y,zeta)
%
global epsilon g_eq g beta l D A s a t
%
dydx = [y(2);
   y(3);
   y(4);
   -zeta^2/(g_eq/g+y(1))^2-2*y(4)/(x+A)+y(3)/((x+A)^2)-y(2)/((x+A)^3);
   y(6);
   y(7);
   0;
   y(9);
   y(10);
   y(11);
   -4*beta^4*l^4*y(8)];
if x==0
   dydx(7)=0;
else
   dydx(7)=-y(7)/x+y(6)/x^2;
end
%
%*************************************************************************
%enforce boundary conditions
% -------------------------------------------------------------------------
function res = allbc(ya,yb,zeta)
%
global epsilon g epsilon_ox phi a nu D Df l c a b g_ansys s A
%H=sqrt(epsilon*epsilon_ox/(2*D*c));
%V=zeta*sqrt(2*D*g^3/((b-a)^4*epsilon));
res = [ya(1);
   D*(ya(3)+nu/A*ya(2))-(D*(yb(7)+nu*yb(6))/a^2-Df*ya(10)/l^2)*(s-a)^2;
   yb(1)+g_ansys/g;
   yb(2);
   yb(3);
   yb(5);
   ya(6);
   yb(6)-ya(2)/(s-a)*a;
   yb(8);
```

```
    yb(9);
    ya(8);
    ya(9)-ya(2)/(s-a)*l];
%
```

C.7 Simulation of LC resonator

```
close all;
clear all;
clc
%
% Geometry of LC tank
R2=550e-6;
R1=200e-6;
d=300e-6;
c=50e-9; %oxide dielectric thickness
% Properties
sigmaAu=1/2.44e-8;
sigmaSi=10;
% Skin depth of Au at 5 GHz
dAu=sqrt(2/2/pi/5e9/(4*pi*1e-7)/sigmaAu);
fprintf('Skin depth in gold: %.3f um\n',dAu*1e6);
%
h=10e-9;
fo=3e9;
for i=1:2
% Calculate inductance
   L=(4*pi*1e-7)*d/2/pi*log(R2/R1);
   fprintf('Inductance = %.3f pH\n',L*1e12);
% Calculate capacitance
   C=3.9*8.854e-12*pi*R1^2./(c+3.9*h);
   fprintf('Capacitance = %.3f pF\n',C*1e12);
% Resonant frequency
   f=1/2/pi./sqrt(L*C);
   fprintf('Frequency = %.3f GHz\n',f/1e9);
% Losses in Au
   dAu=sqrt(2/2/pi/fo/(4*pi*1e-7)/sigmaAu);
   Rr1=d/sigmaAu/2/pi/R1/dAu;
   Rr2=d/sigmaAu/2/pi/R2/dAu;
   Rtop=log(R2/R1)/sigmaAu/dAu/2/pi;
   RL=Rr1+Rr2+2*Rtop;
   RC=c/sigmaSi/pi/R1^2;
   fprintf('Resistance of L = %.3f mOhm\n',RL*1e3);
   fprintf('Resistance of C = %.3f mOhm\n',RC*1e3);
%
```

```
    figure(1)
    Num=[RC*L (RL*RC+L/C) RL/C];
    Den=[L (RL+RC) 1/C];
    sys=tf(Num,Den)
    f=[5e8:1e8:10e10];
    w=2*pi*f;
    [mag,phase] = BODE(sys,w);
    semilogx(f,squeeze(mag(1,1,:)));
    xlabel('Frequency (Hz)')
    ylabel('Magnitude (Ohm)')
    grid on;
    hold on;
%
    figure(2)
Q=abs((L.*(RC^2+1/C^2./(2*pi*f).^2)-1/C./(2*pi*f).*(RL^2+L^2.*(2*pi*f).^2))./
(RL.*(RC^2+1/C^2./(2*pi*f).^2)+RC.*(RL^2+L^2.*(2*pi*f).^2)));
    semilogx(f,Q)
    xlabel('Frequency (Hz)')
    ylabel('Quality Factor')
    grid on;
    hold on;
h=700e-9;
fo=16e9;
end
```

Appendix D

ANSYS Codes

D.1 Single Voltage Input

```
/batch,list
/prep7, Silicon plate deflection from an applied voltage

! Define element types
et,1,121,,,1
et,2,82,,,1            ! PLANE82 element for membrane (axisymmetric)
et,3,172,,1,,,,,,,,,4! Conta172 element for contact surface, with no seperation (always)
et,4,169! Targe169 element for target surface

! Specify material properties
emunit,epzro,8.854e-6    ! Free-space permittivity, μMKSV units
mp,perx,1,1              ! Relative permittivity for air

! Define the constants
lambda=1750              ! plate radius (μm)
a=500                    ! fulcrum radius (μm)
t=50                     ! thickness of fulcrum (μm)
h=17                     ! thickness of plate (μm)
l=340! height of the fulcrum (μm)
bpt=10                   ! Grounded bottom plate thickness (μm)

epsilon=3.9! Enter relative permitivity of insulator used
c=0.27! thickness of insulator

g=10                     ! Air gap (μm)
vltg=60                  ! Applied voltage (V)
taroff=0.8! offset of target surface from the grounded bottom plate
g_eq=g+c/epsilon
```

```
! Draw the geometry! The equivalent height of the air gap
rectng,0,lambda,g_eq,h+g_eq    ! Create the membrane area
rectng,a,a+t,h+g_eq,h+g_eq+l! Create the fulcrum area
rectng, a+t, lambda,0, -bpt! Create the ground plate
rectng,20,2000,-100,400! Create the air area
k,0,lambda,taroff! Create keypoint for the target
k,0,a+t,taroff! Create another keypoint for the target
l,17,18! Create line for the target surface

aovlap,all
aadd,5,6,2! Add areas 2 and 5 to form the plate and fulcrum area: becomes area 1

! Associate attributes
asel,s,area,,7          ! Area for air elements
cm,air,area             ! Group air area into component
aatt,1,,1

asel,s,area,,1          ! Area for plate
aatt,2,,2! Material number is 2, type number is 2

asel,s,area,,3! Area for ground plate
aatt,2,,2

lsel,s,line,,21! Line for contact surface
lsel,a,line,,18
cm,contact,line

lsel,s,line,,17! Line for target surface
latt,3,1,4! Material number is 3, real constant number is 1, type number is 4

! Create mesh
allsel,all
smrtsiz,2
amesh,1                 ! Mesh membrane and fulcrum area
amesh,3! Mesh ground plate
lmesh,17! Mesh target surface

cmsel,s,contact! Select all the nodes attached to the contact surface
nsll,s
!nsel,r,loc,x,a+t,lambda
esln,s! Select elements attached to those nodes
type,3! Assign element type to be 3
mat,3! Assign material type to be 3
real,1! Assign real constant number to be 1
esurf! Automatically generate contact elements
```

```
mshape,1
amesh,7                ! Mesh air with triangles

! Apply voltage to top electrode and bottom electrode
asel,s,area,,1
lsla,s
dl,all,,volt,0         ! Apply voltage to beam

asel,s,area,,3
lsla,s
dl,all,,volt,vltg          ! Ground conductor (not meshed)

! Create electrostatic physics file
allsel,all
et,1,121,,,1
et,2,0                 ! Set structure to null element type
et,3,0
et,4,0

! Write electrostatic physics file
allsel,all
physics,write,ELECT    ! Write electrostatic physics file
physics,clear          ! Clear Physics

et,1,0
et,2,82,,,1            ! PLANE82 element for membrane (axisymmetric)
et,3,172,,1,,,,,,,,,4! Conta172 element for contact surface
et,4,169! Targe169 element for target surface

! Define material properties
mp,ex,2,169e3          ! Set Modulus μN/(μm)**2
mp,prxy,2,0.25
mp,mu,3,0
r,1,,,0.05

! Apply boundary conditions
dl,7,1,ux,0
dl,7,1,uy,0
dl,7,1,symm

da,3,ux,0
da,3,uy,0
da,3,symm

! Set solution options
nlgeom,on! Set analysis option to "Large Displacement Static"
```

```
outres,all,all! Choose "All solution items" for "write items to results file"
eqslv,sparse! Set equation solver to sparse direct
/gst,off! set "tracking" to off

! Write and clear structural physics file
allsel,all
physics,write,STRUCT    ! Write structural physics file

! Issue Essolv macro
ESSOLV,'ELECT','STRUCT',2,0,'air',,,,50  ! Solve coupled-field problem

finish

! Show the displaced shape of the beam
/prep7
physics,read,struct
upcoord,-1
/dscale,,1
/post1
set,last
pldisp


! Plot the fulcrum depflection
path,fulcrum,2
ppath,1,,a+t,g_eq+h,0
ppath,2,,a+t,g_eq+h+l,0
PDEF,fulcrum,u,x
plpath,fulcrum

! Plot the membrane depflection
path,defl,2,,100
ppath,1,,0,g_eq,0
ppath,2,,lambda,g_eq,0
PDEF,defl,u,y
plpath,defl

! Plot the equivalent stress
path,strs,2
ppath,1,,0,g_eq,0
ppath,2,,lambda,g_eq,0
pdef,strs,s,x
plpath,strs
```

D.2 Voltage Sweep

```
/batch,list
/prep7, Silicon plate deflection from a voltage sweep

! Define input array
n_loops=33
*dim,vinp,array,n_loops
*dim,defl,table,151,n_loops
*dim,xloc,table,151,1

! Define input voltages
vmax=180
vinp(1)=20
vinp(2)=40
vinp(3)=60
vinp(4)=80
vinp(5)=100
vinp(6)=101
vinp(7)=102
vinp(8)=103
vinp(9)=104
vinp(10)=105
vinp(11)=106
vinp(12)=107
vinp(13)=108
vinp(14)=109
vinp(15)=110
vinp(16)=120
vinp(17)=140
vinp(18)=160
vinp(19)=180
vinp(20)=160
vinp(21)=140
vinp(22)=120
vinp(23)=100
vinp(24)=90
vinp(25)=80
vinp(26)=70
vinp(27)=60
vinp(28)=55
vinp(29)=50
vinp(30)=45
vinp(31)=40
vinp(32)=30
vinp(33)=20
```

```
! Define arrays for reults representation
! Input voltage = vinp
! Deflection at the membrane end = end_defl
! Deflection at the center = cen_defl
*dim,end_defl,array,n_loops! Resulting displacement
*dim,cen_defl,array,n_loops
*dim,res,table,n_loops,3! Table of results

! Input geometry and mesh and create structural and electric physics files

! Define element types
et,1,121,,,1   ! PLANE121 element for air (axisymmetric)
et,2,82,,,1          ! PLANE82 element for membrane (axisymmetric)
et,3,172,,1,,,,,,,,,4! Conta172 element for contact surface, with no seperation (always)
et,4,169! Targe169 element for target surface

! Specify material properties
emunit,epzro,8.854e-6    ! Free-space permittivity, μMKSV units
mp,perx,1,1          ! Relative permittivity for air

! Define the constants
lambda=1750          ! plate radius (μm)
a=500                ! fulcrum radius (μm)
t=50                 ! thickness of fulcrum (μm)
h=17                 ! thickness of plate (μm)
l=340! height of the fulcrum (μm)
bpt=10               ! Grounded bottom plate thickness (μm)

epsilon=3.9! Enter relative permitivity of insulator used
c=0.27! thickness of insulator

g=10                 ! Air gap (μm)
taroff=0.8! offset of target surface from the grounded bottom plate
g_eq=g+c/epsilon

! Draw the geometry! The equivalent height of the air gap
rectng,0,lambda,g_eq,h+g_eq    ! Create the membrane area
rectng,a,a+t,h+g_eq,h+g_eq+l! Create the fulcrum area
rectng, a+t, lambda,0, -bpt! Create the ground plate
rectng,20,2000,-100,400! Create the air area
k,0,lambda,taroff! Create keypoint for the target
k,0,a,taroff! Create another keypoint for the target
l,17,18! Create line for the target surface

aovlap,all
```

```
aadd,5,6,2! Add areas 2 and 5 and 6 to form the plate and fulcrum area: becomes area 1

! Associate attributes
asel,s,area,,7          ! Area for air elements
cm,air,area             ! Group air area into component
aatt,1,,1

asel,s,area,,1          ! Area for plate
aatt,2,,2! Material number is 2, type number is 2

asel,s,area,,3! Area for ground plate
aatt,2,,2

lsel,s,line,,21! Line for contact surface
cm,contact,line

lsel,s,line,,17! Line for target surface
latt,3,1,4! Material number is 3, real constant number is 1, type number is 4

! Create mesh
allsel,all
smrtsiz,1
amesh,1                 ! Mesh membrane and fulcrum area
amesh,3! Mesh ground plate
lmesh,17! Mesh target surface

cmsel,s,contact! Select all the nodes attached to the contact surface
nsll,s
nsel,r,loc,x,a+t,lambda
esln,s! Select elements attached to those nodes
type,3! Assign element type to be 3
mat,3! Assign material type to be 3
real,1! Assign real constant number to be 1
esurf! Automatically generate contact elements

mshape,1
amesh,7                 ! Mesh air with triangles

! Apply voltage to top electrode and bottom electrode
asel,s,area,,1
lsla,s
dl,all,,volt,0          ! Apply voltage to beam

asel,s,area,,3
lsla,s
dl,all,,volt,vinp(1)            ! Ground conductor (not meshed)
```

```
! Create electrostatic physics file
allsel,all
et,1,121,,,1
et,2,0                  ! Set structure to null element type
et,3,0
et,4,0

! Write electrostatic physics file
allsel,all
physics,write,ELECT     ! Write electrostatic physics file
physics,clear           ! Clear Physics

et,1,0
et,2,82,,,1             ! PLANE82 element for membrane (axisymmetric)
et,3,172,,1,,,,,,,,,4! Conta172 element for contact surface
et,4,169! Targe169 element for target surface

! Define material properties
mp,ex,2,169e3           ! Set Modulus  μN/(μm)**2
mp,prxy,2,0.25
mp,mu,3,0
r,1,,,0.05

! Apply boundary conditions
dl,7,1,ux,0
dl,7,1,uy,0
dl,7,1,symm

! Set solution options
nlgeom,on! Set analysis option to "Large Displacement Static"
outres,all,all! Choose "All solution items" for "write items to results file"
eqslv,sparse! Set equation solver to sparse direct
/gst,off! set "tracking" to off

! Write and clear structural physics file
allsel,all
physics,write,STRUCT    ! Write structural physics file

! Enter do loop
*do,i,1,n_loops

! Issue Essolv macro
ESSOLV,'ELECT','STRUCT',2,0,'air',,,,50,,i,1  ! Solve coupled-field problem

! Store displacement results for each voltage in arrays
```

```
physics,read,struct
/post1
set,last
! Read the deflection at end of plate
cmsel,s,contact
nsll,s,1
nsort,u,sum,1,1
*get,end_defl(i),sort,0,max
! Read the deflection at center of plate
cmsel,s,contact
nsll,s,1
nsort,u,y,1,1
*get,cen_defl(i),sort,0,max
! Assign the values to table
res(i,1)=vinp(i)
res(i,2)=end_defl(i)
res(i,3)=cen_defl(i)

! Store nodal results of node # 1,4,9,57-204
*VGET,defl(1,i),NODE,1,U,Y, , ,2
*VGET,defl(2,i),NODE,4,U,Y, , ,2
*VGET,defl(3,i),NODE,9,U,Y, , ,2
*do,ICOUNT,57,204,1
  *VGET,defl((ICOUNT-53),i),NODE,ICOUNT,U,Y, , ,2
*enddo

! Store xloc of node # 1,4,9,57-204
*VGET,xloc(1,1),NODE,1,LOC,X, , ,2
*VGET,xloc(2,1),NODE,4,LOC,X, , ,2
*VGET,xloc(3,1),NODE,9,LOC,X, , ,2
*do,ICOUNT,57,204,1
  *VGET,xloc((ICOUNT-53),1),NODE,ICOUNT,LOC,X, , ,2
*enddo

*if,i,eq,n_loops,exit

! Update electric physics file
physics,read,elect
/prep7
asel,s,area,,3
lsla,s
dl,all,,volt,vinp(i+1)
alls
physics,write,elect

! End the do loop
```

```
*enddo

! Write parameters in a file
! First column is the x-location
! Other columns are the deflection
*CFOPEN,'deflection','txt',' '
*VWRITE,xloc(1),defl(1,1),defl(1,2),defl(1,3),defl(1,4),defl(1,5),defl(1,6),defl(1,7),defl(1,8),
defl(1,9),defl(1,10),defl(1,11),defl(1,12),defl(1,13),defl(1,14),defl(1,15),defl(1,16),defl(1,17),defl
(1,18),defl(1,19),defl(1,20),defl(1,21),defl(1,22),defl(1,23),defl(1,24),defl(1,25),defl(1,26),defl(1,
27),defl(1,28),defl(1,29),defl(1,30),defl(1,31),defl(1,32),defl(1,33)
(f17.12,',',34(f18.15,','))
*CFCLOS


! Write the results paramter in a file
!*CFOPEN,'results','txt',' '
!*VWRITE,res(1,1),res(1,2),res(1,3)
!(3(f18.5,','))
!*CFCLOS

! Plot maximum displacement vs. voltage
/axlab,x,Applied Voltage (Volts)
/axlab,y,Maximum Displacement (micron)
/xrange,0,vmax
/yrange,0,g_eq
*vplot,res(1,1),res(1,2)

save
```

D.3 Self and Mutual Capacitances

```
/batch, list
/prep7, self and mutual capacitances of the device

! Define element types
et,1,121,,,,1    ! Air element

! Specify material properties
emunit,epzro,8.854e-6     ! Free-space permittivity, μMKSV units
mp,perx,1,1               ! Relative permittivity of air
mp,perx,2,4.6! Relative permittivity of Pyrex

! Define the constants
lambda=1750               ! plate radius (μm)
a=550                     ! fulcrum radius (μm)
```

```
t=50                ! thickness of fulcrum (μm)
h=17                ! thickness of plate (μm)
l=340! height of the fulcrum (μm)
bpt=0.5             ! Grounded bottom plate thickness (μm)
r=200! radius of the capacitor
h_c=0.5! thickness of the capacitor

epsilon=3.9! Enter equivalent relative permitivity of insulator used
c=0.27! thickness of insulator

g=10+c/epsilon          ! Equivalent air gap (μm)
g_cap=c/epsilon! air gap for the capacitor

! Draw the geometry
rectng,0,lambda,0,h     ! Create the plate area
rectng,a,a+t,h,h+l! Create the fulcrum area
rectng,a,lambda,-g,-g-bpt! Create the ground plate
rectng,0,r,-g_cap,-g_cap-h_c! Create the capacitor
rectng,0,2000,-500,500! Create the air area

aovlap,all
aadd,2,6! Add areas to form the plate and fulcrum area: becomes area 1

rectng,0,r,-g_cap-h_c,-g-bpt
rectng,0,2000,-500,-g-bpt
aadd,2,5
aovlap,all

! Associate attributes
asel,s,area,,5          ! Area for air elements
cm,air,area             ! Group air area into component
aatt,1,,1

asel,s,area,,2          ! Area for air elements
cm,pyrex,area           ! Group air area into component
aatt,2,,1

asel,s,area,,1          ! Area for plate
aatt,2,,2! Material number is 2, type number is 2

! Create mesh
allsel,all
smrtsiz,1
mshape,1
amesh,5                 ! Mesh air with triangles
amesh,2
```

```
nsel,s,loc,y,-g
nsel,r,loc,x,a,lambda
cm,cond1,node

nsel,s,loc,y,-g_cap
nsel,r,loc,x,0,r
cm,cond2,node

nsel,s,loc,y,0
cm,cond3,node

alls
finish
/solu
eqslv,jcg

cmatrix,,'cond',3,0

finish
```

D.4 ANSYS Model for Device 9_1

```
/batch,list
/prep7, compare ANSYS with experiments for device 9_1


! Define element types
et,1,121,,,1     ! PLANE121 element for air (axisymmetric)
et,2,183,,,1          ! PLANE183 element for membrane (axisymmetric)
et,3,172,,1,,,,,,,,,4! Conta172 element for contact surface, with no seperation (always)
et,4,169! Targe169 element for target surface

! Specify material properties
emunit,epzro,8.854e-6     ! Free-space permittivity, μMKSV units
mp,perx,2,1          ! Relative permittivity for air

! Define the constants
lambda=1750          ! plate radius (μm)
a=500                ! fulcrum radius (μm)
ttop=46              ! thickness of fulcrum on top (μm)
tbot=12! thickness of fulcrum at bottom (μm)
h=20                 ! thickness of plate (μm)
l=340! height of the fulcrum (μm)
bpt=10               ! Grounded bottom plate thickness (μm)
```

```
epsilon=3.9! Enter relative permitivity of insulator used
c=0.27! thickness of insulator

g=9.3                ! air gap (μm)
!g=10.1
vltg=0               ! Applied voltage (V)
taroff=g-8.3+c/epsilon! offset of target surface from the grounded bottom plate
g_eq=g+c/epsilon! The equivalent height of the air gap
bond=50! The bonded length (μm)

! Draw the geometry
rectng,0,lambda-bond,g_eq,h+g_eq    ! Create the membrane area
rectng,lambda-bond,lambda,g_eq,h+g_eq! Create the bonded area
k,0,a+(ttop-tbot)/2,h+g_eq,0! Create keypoints for the fulcrum area
k,0,a+ttop-(ttop-tbot)/2,h+g_eq,0
k,0,a+ttop,h+g_eq+l,0
k,0,a,h+g_eq+l,0
a,9,10,11,12! Create fulcrum area
rectng, a+t, lambda-50,0, -bpt! Create the ground plate
rectng,20,2000,-100,400! Create the air area
k,0,lambda,taroff! Create keypoint for the target
k,0,a+t,taroff! Create another keypoint for the target
l,21,22! Create line for the target surface

aovlap,all
aadd,3,7,8! Add areas 3, 7 and 8 to form the plate and fulcrum area

! Associate attributes
asel,s,area,,9          ! Area for air elements
cm,air,area             ! Group air area into component
aatt,2,,1

asel,s,area,,1          ! Area for plate
aatt,1,,2! Material number is 2, type number is 2

asel,s,area,,6! Area for bonded plate
aatt,1,,2

lsel,s,line,,27! Line for contact surface
lsel,a,line,,22
cm,contact,line

lsel,s,line,,21! Line for target surface
latt,3,1,4! Material number is 3, real constant number is 1, type number is 4
```

```
! Create mesh
allsel,all
smrtsiz,1
amesh,1                ! Mesh membrane and fulcrum area
amesh,6
lmesh,21! Mesh target surface
nummrg,all

cmsel,s,contact! Select all the nodes attached to the contact surface
nsll,s
nsel,r,loc,x,a+t,lambda
esln,s! Select elements attached to those nodes
type,3! Assign element type to be 3
mat,3! Assign material type to be 3
real,1! Assign real constant number to be 1
esurf! Automatically generate contact elements

mshape,1
amesh,9                ! Mesh air with triangles

! Apply voltage to top electrode and bottom electrode
asel,s,area,,1
lsla,s
dl,all,,volt,0         ! Apply voltage to beam

asel,s,area,,4
lsla,s
dl,all,,volt,vltg          ! Ground conductor (not meshed)

! Create electrostatic physics file
allsel,all
et,1,121,,,1
et,2,0                 ! Set structure to null element type
et,3,0
et,4,0

! Write electrostatic physics file
allsel,all
physics,write,ELECT    ! Write electrostatic physics file
physics,clear          ! Clear Physics

et,1,0
et,2,183,,,1           ! PLANE82 element for membrane (axisymmetric)
et,3,172,,1,,,,,,,,4! Conta172 element for contact surface
et,4,169! Targe169 element for target surface
```

```
! Define material properties
mp,prxy,1,0.25
tb,anel,,,,0            ! Set Modulus  μN/(μm)**2
tbdata,1,166e3,64e3,64e3,0,0,0
tbdata,7,166e3,64e3,0,0,0,166e3
tbdata,13,0,0,0,80e3,0,0
tbdata,19,80e3,0,80e3
mp,mu,3,0
r,1,,,0.05


! Apply boundary conditions
alls
dl,11,1,ux,0
dl,11,1,uy,0

da,6,uy,-g_eq+taroff! Edge bonded down
!dk,7,uy,-g_eq+taroff! Edge touched down

! Apply uniform pressure load to center plate
sfl,29,pres,-0.101325/2! Pressure from bonding process for edge touched-down case
!sfl,29,pres,-0.101325/1.6! Pressure from bonding process for edge zipped-in case
sfl,28,pres,0.101325/500! Equivalent pressure for residual stress
sfl,23,pres,0.101325/500

! Set solution options
nlgeom,on! Set analysis option to "Large Displacement Static"
outres,all,all! Choose "All solution items" for "write items to results file"
eqslv,sparse! Set equation solver to sparse direct
/gst,off! set "tracking" to off

! Write and clear structural physics file
allsel,all
physics,write,STRUCT     ! Write structural physics file

! Issue Essolv macro
ESSOLV,'ELECT','STRUCT',2,0,'air',,,,50  ! Solve coupled-field problem

finish

! Show the displaced shape of the beam
/prep7
physics,read,struct
upcoord,-1
/dscale,,1
/post1
```

```
set,last

path,defl,2,,200
ppath,1,,0,g_eq+10,0
ppath,2,,lambda,g_eq,0
PDEF,defl,u,y
plpath,defl
```

D.5 New Actuator Design

```
/batch,list
/prep7


! Define element types
et,1,121,,,1
et,2,82,,,1            ! PLANE82 element for membrane (axisymmetric)

! Specify material properties
emunit,epzro,8.854e-6     ! Free-space permittivity, μMKSV units
mp,perx,1,1               ! Relative permittivity for air

! Define the constants
a=550                     ! plate radius (μm)
act_in=0! actuator inner radius (um)
act_out=500! actuator outer radius (um)
h=10                      ! thickness of plate (μm)
h_b=1! bridge thickness
bpt=10                    ! Grounded bottom plate thickness (μm)

epsilon=3.9! Enter relative permitivity of insulator used
c=0.27! thickness of insulator

g=2.5                     ! Air gap (μm)
vltg=40                   ! Applied voltage (V)
g_eq=g+c/epsilon

! Draw the geometry! The equivalent height of the air gap
rectng,0,act_out,g_eq,h+g_eq! Create the plate area
rectng,act_out,a,g_eq,h_b+g_eq! Create the bridge area
rectng, act_in, act_out,0, -bpt! Create the ground plate
rectng,0,800,-100,200! Create the air area

aovlap,all
aadd, 6,5
```

```
! Associate attributes
asel,s,area,,7          ! Area for air elements
cm,air,area             ! Group air area into component
aatt,1,,1

asel,s,area,,1          ! Area for plate
aatt,2,,2! Material number is 2, type number is 2

asel,s,area,,3! Area for ground plate
aatt,2,,2


! Create mesh
allsel,all
smrtsiz,2
amesh,1                 ! Mesh membrane area

mshape,1
amesh,7                 ! Mesh air with triangles

! Apply voltage to top electrode and bottom electrode
asel,s,area,,1
lsla,s
dl,all,,volt,0          ! Apply voltage to beam

asel,s,area,,3
lsla,s
dl,all,,volt,vltg           ! Ground conductor (not meshed)

! Create electrostatic physics file
allsel,all
et,1,121,,,1
et,2,0                  ! Set structure to null element type
et,3,0
et,4,0

! Write electrostatic physics file
allsel,all
physics,write,ELECT     ! Write electrostatic physics file
physics,clear           ! Clear Physics

et,1,0
et,2,82,,,1             ! PLANE82 element for membrane (axisymmetric)

! Define material properties
```

```
mp,ex,2,169e3          ! Set Modulus μN/(μm)**2
mp,prxy,2,0.25
mp,mu,3,0
r,1,,,0.05

! Apply boundary conditions
dl,6,1,ux,0
dl,6,1,uy,0
dl,6,1,symm

! Set solution options
nlgeom,on! Set analysis option to "Large Displacement Static"
outres,all,all! Choose "All solution items" for "write items to results file"
eqslv,sparse! Set equation solver to sparse direct
/gst,off! set "tracking" to off

! Write and clear structural physics file
allsel,all
physics,write,STRUCT    ! Write structural physics file

! Issue Essolv macro
ESSOLV,'ELECT','STRUCT',2,0,'air',,,,50  ! Solve coupled-field problem

finish

! Show the displaced shape of the beam
/prep7
physics,read,struct
upcoord,-1
/dscale,,1
/post1
set,last
pldisp

path,defl,2,,100
ppath,1,,0,g_eq,0
ppath,2,,a,g_eq,0
PDEF,defl,u,y
plpath,defl
```