InAlAs/InGaAs/InP HEMTs with
Pseudomorphic Schottky Barriers

by

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Submitted to the

DEPARTMENT OF ELECTRICAL ENGINEERING
AND COMPUTER SCIENCE

in partial fulfillment of the requirements

for the degrees of

BACHELOR OF SCIENCE

and

MASTER OF SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1994

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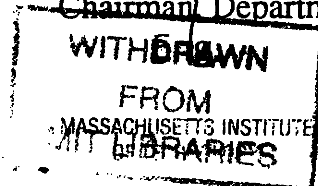
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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degrees of Bachelor of Science and Master of Science at Massachusetts Institute of Technology

ABSTRACT

Higher gain and current density than even the best GaAs-based pseudomorphic high electron mobility transistors (PHEMTs) have been reported for InAlAs/InGaAs/InP HEMTs operating at microwave and millimeter-wave frequencies by several authors. However, the power performance potential of these devices has not yet been fully exploited due to their low breakdown voltage and Schottky barrier height. In this study, AlAs mole fraction of the $In_xAl_{1-x}As$ Schottky barrier was enhanced (x = 0.45, 0.40, 0.35) over the lattice-matched value (x = 0.52) in an effort to overcome these deficiencies. We found that AlAs-rich insulator HEMTs showed an increase in 2-terminal breakdown voltage and forward turn-on voltage. No apparent degradation in transconductance or parasitic element values were observed. All InP-based HEMTs studied in this work had higher f_T and G_{max} (at 18 GHz) than even the state-of-the-art GaAs-based power PHEMTs. However, in this experiment, the saturated drain current decreased for HEMTs with AlAs-rich Schottky barriers. This may have arisen from an observed decrease in sheet electron concentration probably as a result of segregation and inactivation of silicon dopants in AlAs-rich Schottky barriers. Growth parameters of pseudomorphic layers must be optimized in order to realize the full power performance potential of InAlAs/InGaAs/InP HEMTs and PHEMTs.

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ACKNOWLEDGMENT

I would like to thank Dr. John C. Huang, who has served as my interviewer, mentor, and supervisor during the 6-A program. Without his efforts, it would not have been possible for me to perform my thesis work at Raytheon.

Professor Jesús A. del Alamo of MIT is deeply appreciated for his guidance as my thesis supervisor. Dr. Noren Pan is thanked for the growth and the characterizations of epitaxial materials. Rebecca McTaggart, Alicia Bertrand, and Pam Saledas are thanked for their assistance with processing. Lisa Aucoin and Dr. Katerina Hur are appreciated for their helpful suggestions and comments. Alan Miller and Mike Cobb are thanked for their help with device testing and characterization. I would also like to thank Dr. James Oakes for his critical review of the manuscript. Dr. Stanley Shanfield and Raytheon Company are acknowledged for giving me the opportunity to pursue my interests during this thesis work.

Most of all, I would like to thank my family for all their patience and support throughout my undergraduate and graduate studies.

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Chapter 1. Introduction

1.1 Motivations for the Study

As the operations of many electronic systems, including military and commercial communication and radar systems, extend toward higher frequencies into the millimeter-wave range, the need for low cost solid-state devices capable of operating at these frequencies with high gain and output power has become imperative. These needs have begun to be met by the development of high electron mobility transistors (HEMTs).

Since the first demonstration of carrier mobility enhancement in modulation-doped heterostructures by Dingle *et al.* [1], HEMTs have achieved unsurpassed gain and noise performances at frequencies up to 100 GHz [2]-[6]. In fact, noise figures as low as 0.3 dB at 18 GHz [5] and 1.4 dB at 94 GHz [6] have been achieved. Advantages over more mature metal-semiconductor transistor (MESFET) technology, which has dominated the low noise and high power microwave transistor market, are numerous, including higher electron mobility and peak velocity in two-dimensional electron gas (2-DEG), and more flexibility on the choice of channel material [7]. As described in Section 1.3, these advantages are being utilized to optimize HEMTs and pseudomorphic HEMTs (PHEMTs) for high power applications [8], [9].

1.2 Fundamental Limits for Power Performance of an FET

Power performance of an FET at millimeter-wave frequencies is usually characterized in terms of its 1) maximum RF output power P_0, 2) power gain G, and 3) maximum power-added-efficiency PAE. To derive the maximum RF output power in class A operation, one may start with the most general expression for AC power:

$$P_o = V_{rms} I_{rms} \quad (1.1)$$

where V_{rms} and I_{rms} are the root-mean-square values defined for an FET as

$$I_{rms} = \frac{I_{D\max} - I_{D\min}}{2\sqrt{2}} \quad (1.2)$$

and

$$V_{rms} = \frac{V_{DS\max} - V_{DS\min}}{2\sqrt{2}}. \quad (1.3)$$

Substituting Equations (1.2) and (1.3) into Equation (1.1), P_0 becomes

$$P_o = \frac{(V_{DSmax} - V_{DSmin})(I_{Dmax} - I_{Dmin})}{8}. \quad (1.4)$$

This simple approximation is graphically presented in Figure 1.1, in which the FET operates along its ideal load line, $R_L = R_{opt} = (BV_{DS} - V_k)(I_{D\max} - I_{D\min})$. Using the parameters shown in Figure 1.1, Equation (1.4) now becomes

$$P_o = \frac{(BV_{DS} - V_k)(I_{D\max} - I_{D\min})}{8}. \quad (1.5)$$

Here, the importance of having a large source-drain breakdown voltage (BV_{DS}) and a large maximum channel current (I_{Dmax}) in order to produce a high RF output power is evident.

In terms of the equivalent circuit model discussed in Chapter 3, the maximum available gain (G_{max}) of a HEMT, which is closely related to G, is given by the following approximate expression:

$$\begin{aligned} G_{max} &= \frac{(f_T / f)^2}{4g_o(R_g + R_i + R_s + \pi f_T L_s) + 4\pi f_T C_{gd}(2R_g + R_i + R_s + 2\pi f_T L_s)} \\ &= \left(\frac{g_m}{2\pi C_{gs} f}\right)^2 \frac{1}{4g_o(R_g + R_i + R_s + \pi f_T L_s) + 4\pi f_T C_{gd}(2R_g + R_i + R_s + 2\pi f_T L_s)} \end{aligned} \quad (1.6)$$

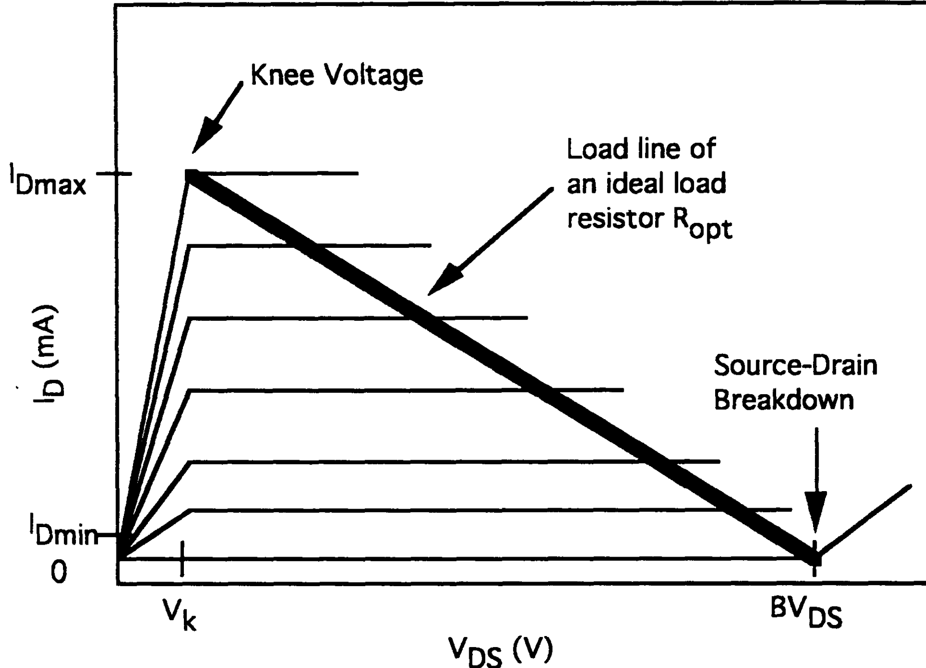

Figure 1.1: Load line for an ideal class A operation of an FET.

where f_T is the current gain cutoff frequency, f is the operating frequency, g_m is the extrinsic transconductance, g_o is the output conductance, R_g is the gate resistance, R_i is the intrinsic resistance, R_s is the source resistance C_{gd} is the gate-to-drain capacitance, C_{gs} is the gate-to-source capacitance, and L_s is the source inductance of the device. As Equation 1.6 indicates, for a large gain, it is necessary to have a high transconductance.

The transconductance of a HEMT is defined as

$$g_m \equiv \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}=\text{constant}} . \qquad (1.7)$$

The transconductance represents the incremental change of the (output) drain current induced by the (input) gate voltage increment. For the reason noted in Section 2.3.3, microwave and millimeter-wave HEMTs have very short gate lengths (0.25 μm and below) and thus operate in the saturation regime of electron velocity. The intrinsic transconductance is then given by

$$g_{m0} = \frac{\varepsilon v_{sat} W}{t} \tag{1.8}$$

where W is the device width, v_{sat} is the saturated electron velocity, t is the Schottky barrier thickness, and ε is the permittivity of the Schottky barrier. In order to achieve a high gain and efficiency, the channel material must have a high v_{sat}.

Another important parameter in determining power performance is the power-added-efficiency. *PAE* is defined as

$$PAE = \frac{P_o - P_i}{P_{dc}} = \frac{P_o(1-1/G)}{P_{dc}} \tag{1.9}$$

where P_o is the RF output power, P_i is the RF input power, and P_{dc} is the DC power used to bias the FET and is given by

$$P_{dc} = \frac{(I_{Dmax} + I_{Dmin})(BV_{DS} + V_k)}{4}. \tag{1.10}$$

For I_{Dmin} and $V_k \approx 0$, Equation (1.9) becomes

$$PAE = \frac{1-1/G}{2}. \tag{1.11}$$

As $1/G$ approaches 0, *PAE* approaches the theoretical maximum of 1/2. Hence, in order to have high overall power-added-efficiency, high gain is necessary for a wide range of operating conditions.

1.3 InP-Based HEMTs

1.3.1 Advantages Over Other Material Systems

AlGaAs/GaAs was the first material system used to demonstrate the enhancement of carrier mobility in heterostructures [1]. In an attempt to increase device performance, feasibility of several different material systems have been studied. The first PHEMTs utilizing $In_{0.15}Ga_{0.85}As$ channel on GaAs substrate were demonstrated in 1986 [8]. PHEMTs using this type of structure have shown

far superior performance than conventional AlGaAs/GaAs-based HEMTs [3], [8], [9]. However, in recent years InP-based HEMTs have demonstrated even better noise figure and gain at frequencies up to 100 GHz [6], [10], [11].

InAlAs/InGaAs/InP material system has many inherent advantages over AlGaAs/GaAs and pseudomorphic AlGaAs/InGaAs/GaAs material systems. Figure 1.2 shows the bandgap energies and the lattice constants of materials included in this discussion. The following are some of the properties of InAlAs/InGaAs/InP material system that enhance the device performance:

1. The conduction band discontinuity (ΔE_C) for $In_{0.52}Al_{0.48}As$/ $In_{0.53}Ga_{0.47}As$ (lattice matched to InP) is greater than 0.50 eV while that for pseudomorphic $Al_{0.2}Ga_{0.8}As/In_{0.15}Ga_{0.85}As$ heterostructure on GaAs is 0.30 eV, and that for $Al_{0.30}Ga_{0.70}As$/GaAs is only 0.24 eV. A larger ΔE_C translates into better electron confinement and thus higher sheet electron concentrations [12], [13].

2. $In_{0.53}Ga_{0.47}As$ has an electron effective mass around half that of GaAs, resulting in 50% higher mobility [14].

3. Since the separation between Γ_L and Γ_X valleys is much larger in $In_{0.53}Ga_{0.47}As$ than in GaAs, higher electric fields can be tolerated without the onset of electron velocity saturation. As a result, peak electron velocity in $In_{0.53}Ga_{0.47}As$ ($v_p > 3x10^7$ cm/s) is much higher than in GaAs ($v_p > 2x10^7$ cm/s) [15], [16].

4. Since InP has 50% higher thermal conductivity than GaAs, InAlAs/InGaAs HEMTs on InP substrate can work at a lower operating temperature for the same power dissipation than either AlGaAs/GaAs HEMTs or AlGaAs/InGaAs PHEMTs on GaAs substrate [17].

By increasing the InAs mole fraction of InGaAs, further enhancement in electron mobility and velocity over GaAs have been demonstrated [12], [18]. However, it is not possible to grow $In_xGa_{1-x}As$ layer with x larger than ~0.35 on a GaAs substrate without introducing defects due to the large differences in lattice constants (see Figure 1.2) [12], [18]. InP, on the other hand, has a larger lattice constant than GaAs and can accommodate InGaAs with InAs mole fraction

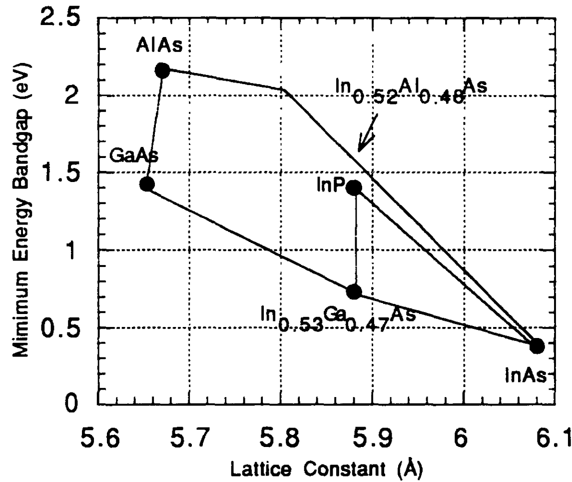

Figure 1.2: Compilation of minimum energy bandgap versus lattice constant for the materials of interest. Connecting lines give information for alloys of the materials at the endpoints of a given line segment [16].

much higher than 35%. The enhanced transport characteristics of InGaAs with InAs mole fraction as high as 65% have resulted in HEMTs with better performance than any GaAs-based HEMTs or PHEMTs [2], [6], [10], [11].

1.3.2 Problems

There are several problems that have limited the use of InP-based HEMTs to low noise, low voltage applications despite proven potential for high output power at millimeter-wave frequencies [2], [6], [10]. InP-based HEMTs suffer from high gate leakage current, low Schottky barrier height (ϕ_B), and low breakdown voltage (BV). High gate leakage current and low ϕ_B have been attributed to the poor quality of the Schottky barrier on $In_{0.52}Al_{0.48}As$ while low breakdown voltage has been attributed to the low bandgap energy (E_G) of the $In_{0.53}Ga_{0.47}As$ channel and the low Schottky barrier height of $In_{0.52}Al_{0.48}As$ layer [19]-[22].

$In_{0.53}Ga_{0.47}As$ has $E_G = 0.73$ eV [23], which is only about half as large as that of GaAs ($E_G = 1.42$ eV) [24]. Low E_G fundamentally limits the breakdown

voltage of $In_xGa_{1-x}As$ to be much smaller than GaAs [22]. As shown in Figure 1.2, decreasing the InAs mole fraction of InGaAs increases the bandgap energy, but this is accompanied by a degradation in electron transport properties as discussed in Section 1.3.1.

Low ϕ_B of the $In_{0.52}Al_{0.48}As$ layer is the cause of relatively large gate leakage current. The current is the result of tunneling and thermionic emission across the metal-semiconductor junction. Since thermionic emission and tunneling rate are exponential functions of ϕ_B, the increase in gate current is dramatic for low Schottky barrier heights. For more detailed information, see Appendix B.

The above problems have been observed frequently in InP-based HEMTs. Drain-gate breakdown voltages (BV_{DG}) have been limited to about 4 to 6 V while drain-source breakdown voltages (BV_{DS}) have been around 3 to 5 V [6], [19]. As already shown in Section 1.2, high breakdown voltage is necessary in order to produce high output power. Because of these weaknesses, even though the potential for high power operation of InAlAs/InGaAs/InP HEMTs at millimeter-wave frequencies have been demonstrated [19], [25], it has yet to be exploited.

1.4 Objectives of This Work

There is an increasing amount of effort to develop solid-state devices for high power applications at frequencies of 60 GHz and beyond. Only InP-based HEMTs and PHEMTs have demonstrated appreciable gains at these frequencies due to their high electron velocities. In an attempt to address the problems stated in Section 1.3.2, AlAs mole fraction of the $In_xAl_{1-x}As$ Schottky barrier of an InP-based HEMT is enhanced beyond the lattice matched value. Higher Schottky barrier heights have been measured on such structures with high AlAs mole fractions [26]-[29]. Higher gate-drain breakdown voltages (BV_{DG}) and source-

drain breakdown voltages also have been reported on HEMTs with such pseudomorphic Schottky barriers [20], [30]. This composition change in the $In_xAl_{1-x}As$ Schottky barrier will form the foundation for an exploratory study to determine whether HEMTs with such pseudomorphic Schottky barriers are suitable for millimeter-wave power applications. In order to accomplish this task, HEMTs with varying AlAs mole fraction Schottky barriers will be fabricated, and several DC and RF performance figures of merit will be compared and contrasted.

Chapter 2. Device Background

This chapter contains the qualitative description of HEMT operation as well as the possible effects of varying the AlAs mole fraction of the InAlAs Schottky barrier on device performance. The geometry of active devices and test structures used in this work is also described. Finally, the fabrication process for the above devices is outlined.

2.1 Qualitative Description of HEMT Operation

When two semiconductor materials with different bandgaps are joined together, they form a heterojunction with discontinuities in both the conduction-band and the valence-band as shown in Figure 2.1. By doping the wide-bandgap material, $In_{0.52}Al_{0.48}As$ in Figure 2.1, free electrons are introduced. Electrons accumulate in the potential well created at the heterojunction and form a sheet of charge called two-dimensional electron gas (2-DEG). The narrow-bandgap material, $In_{0.53}Ga_{0.47}As$ in Figure 2.1, remains undoped. A spacer layer separates the $In_{0.53}Ga_{0.47}As$ channel from the donor impurities in the wide-bandgap material. Thus, impurity scattering is much reduced, enhancing both electron mobility and electron velocity. The gate metal is placed on $In_{0.52}Al_{0.48}As$ to form a Schottky barrier and modulate the charge in the 2-DEG.

2.2 Implications of Pseudomorphic Schottky Barriers

Increasing the AlAs mole fraction of the InAlAs Schottky barrier changes many different parameters that directly affect the performance of a HEMT. Some of the implications of having a pseudomorphic Schottky barrier are discussed in this section.

As briefly mentioned in Section 1.4, larger Schottky barrier heights and breakdown voltages have been observed by increasing the AlAs mole fraction of

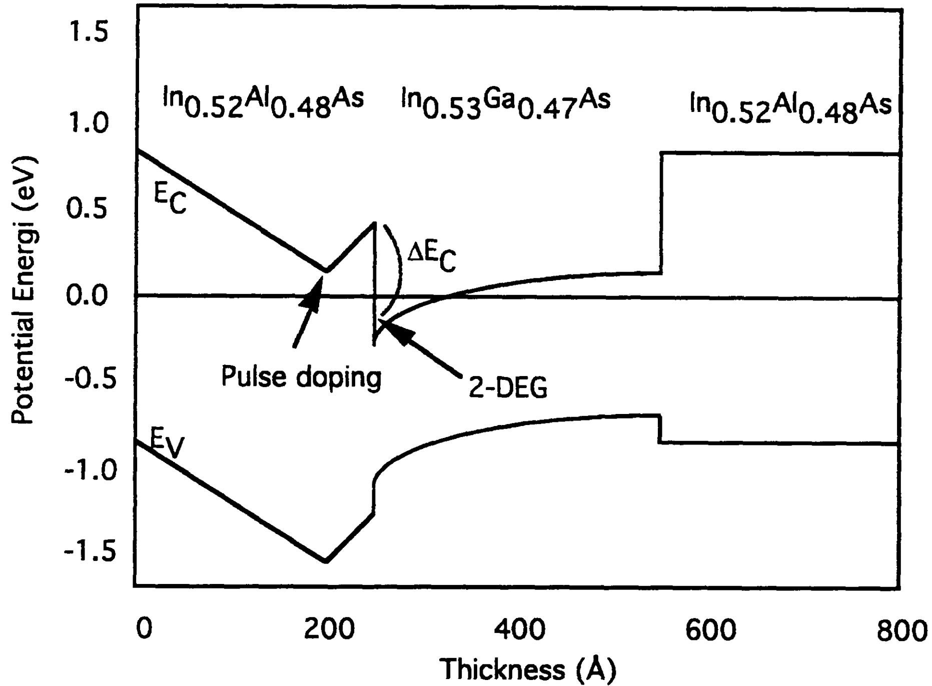

Figure 2.1: Band diagram of a typical lattice-matched InP-based HEMT in thermal equilibrium.

the InAlAs Schottky layer beyond the typical 48% [26]-[30]. However, nearly no work has been published on a systematic investigation to determine the quality of the Schottky barrier as the AlAs mole fraction is varied [29]. Presence of aluminum oxide between the metal and the $In_{0.52}Al_{0.48}As$ has been reported [31]. Because of the reactive nature of aluminum, formation of oxides at the metal-semiconductor interface may become more prevalent as the AlAs mole fraction is increased. Quality of the Schottky barrier greatly affects the device behavior, so the possible presence of oxides should be considered carefully in evaluating the performance among HEMTs with different AlAs mole fraction Schottky barriers.

The maximum amount of current in the channel is largely determined by the sheet electron concentration in the 2-DEG, which in turn is largely determined by ΔE_C shown in Figure 2.1. Since the $In_{0.52}Al_{0.48}As$ spacer was not varied for

different Schottky barriers, to the first order, ΔE_C and hence the maximum channel current should not change. However, different energy bandgaps of different Schottky barriers may affect the band diagram shown in Figure 2.1. Determining accurate band diagram requires solving Poisson's equation using numerical methods, but necessary resources were not available to accomplish this task.

As the AlAs mole fraction of InAlAs is increased, the lattice constant of the material begins to deviate from that of InP and $In_{0.53}Ga_{0.47}As$. Epitaxial growth techniques, such as molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD), have allowed growth of such lattice-mismatched structures. Since single layers of atoms are grown sequentially, the normal geometry of the crystal lattice bonds can elastically deform over the first few monolayers and accommodate the lattice constant mismatch while forming one-to-one bonds. However, the layer is necessarily strained in order to sustain such a pseudomorphic structure.

Due to this strain, thickness of the pseudomorphic layer must be kept below a value called the critical thickness. If the pseudomorphic layer exceeds this thickness, dislocations suddenly form and relieve the strain. Dislocations severely degrade carrier transport properties and device performance. Several competing theories have been proposed to determine the critical thickness for pseudomorphic structures [32]-[34]. The results are shown in Figure 2.2. Using the information from Figure 1.1, as well as [16] and [32]-[34], misfit percentages were calculated for varying AlAs mole fractions. The results are summarized in Table 2.1.

As shown by Figure 2.2 and Table 2.1, different theories give conflicting information about the critical thickness of InAlAs alloys listed in Table 2.1. However, Bennet *et al.* have shown that up to ~250 Å of high crystalline quality

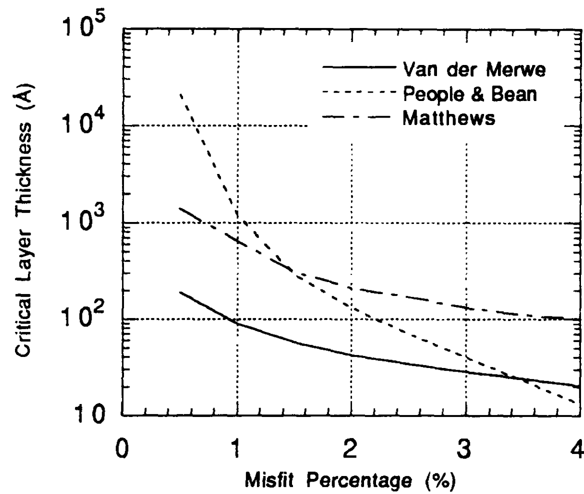

Figure 2.2: Calculated critical layer thickness as a function of the misfit percentage with respect to InP [32]-[34].

Table 2.1: Misfit of $In_xAl_{1-x}As$ with respect to InP

	InP	$In_{0.45}Al_{0.55}As$	$In_{0.40}Al_{0.60}As$	$In_{0.35}Al_{0.65}As$
a_0 (Å)	5.869	5.815	5.800	5.785
Misfit (%)	0	0.85	1.17	1.36

$In_{0.35}Al_{0.65}As$ can be grown on InP substrates [35]. Also, past reports of fabricating reasonably good devices with similar Schottky layers suggest that excellent material can indeed be grown [20], [30], [36].

2.3 Fabrication of InP-Based HEMTs

2.3.1 Epitaxy

Performance of HEMTs depends greatly on the precise control of doping densities and layer thicknesses. Advancement of epitaxial growth techniques such as molecular beam epitaxy and metal-organic chemical vapor deposition has enabled rapid advances in HEMT technology. State-of-the-art performance has been demonstrated by both MBE- and MOCVD-grown materials [37], [38].

Four 2-inch diameter InP semi-insulating (SI) substrates were processed for this study. Each wafer had MOCVD-grown active layers. As shown in Figure 2.3, the epitaxial layer structure for the HEMTs used in this work consists of an $In_{0.52}Al_{0.48}As$ buffer layer, an $In_{0.53}Ga_{0.47}As$ channel layer, an $In_{0.52}Al_{0.48}As$ spacer layer, a delta-doped plane of silicon, an $In_xAl_{1-x}As$ Schottky layer, and an $In_{0.53}Ga_{0.47}As$ cap layer, all grown sequentially using an MOCVD system.

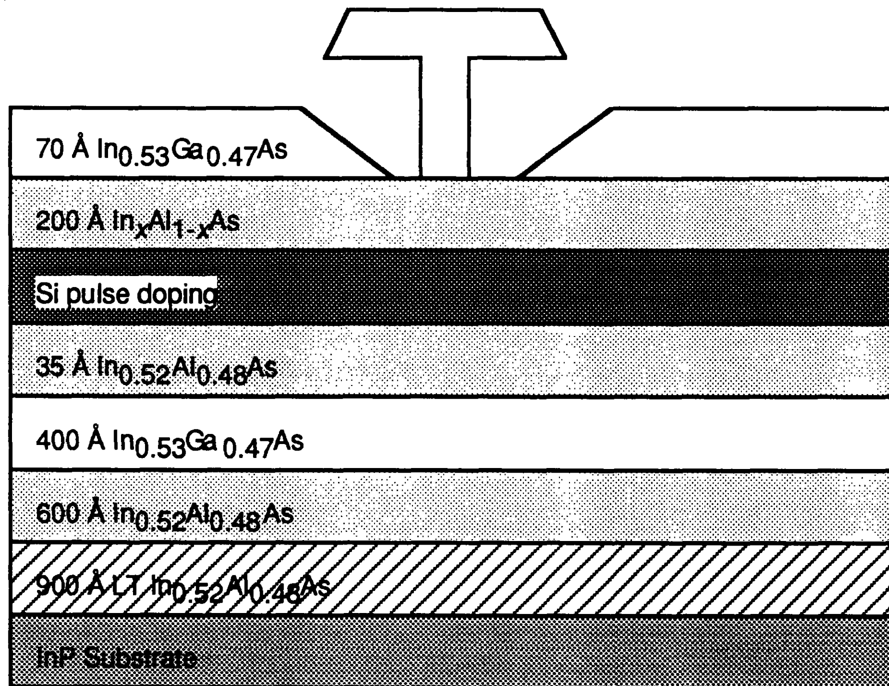

Figure 2.3: Cross-section of device structure.

The $In_{0.52}Al_{0.48}As$ buffer layer is used to prevent defects that may be present on the surface of the InP substrate from adversely influencing the transport properties of the active layers. Also, high resistivity of this layer virtually eliminates any leakage current that may flow through the substrate. The $In_{0.53}Ga_{0.47}As$ layer is the conduction channel, and the delta-doped plane of silicon above provides the carriers for current conduction. The $In_{0.52}Al_{0.48}As$ spacer layer separates the donors from the channel to minimize impurity scattering. The $In_{0.53}Ga_{0.47}As$ cap layer prevents the underlying $In_xAl_{1-x}As$

Schottky layer from oxidizing and also facilitates ohmic contact to the channel. All layers, except the delta-doped plane of silicon, were undoped. The only variable among the four wafers was the AlAs mole fraction of the Schottky barrier ($In_xAl_{1-x}As$) as shown in Table 2.2.

Table 2.2: Variability of the wafers used in this work.

Wafer Number	AlAs Mole Fraction
Q54-1	48%
Q54-2	55%
Q54-3	60%
Q54-4	65%

The $In_{0.52}Al_{0.48}As$ buffer layer consisted of 900 Å of low temperature (LT) layer and 600 Å of standard temperature layer. The LT $In_{0.52}Al_{0.48}As$ layer was grown at 475°C to increase the resistivity and to enhance the surface morphology of the epitaxial/substrate interface [39], [40]. All other layers were grown at 650°C. Trimethylindium (TMI), trimethylaluminum (TMA), trimethylarsenic (TMAs), and pure arsine were used as source materials for the $In_xAl_{1-x}As$ layers. TMI, trimethylgallium (TMG), and arsine were used to grow $In_{0.53}Ga_{0.47}As$ layers. The TMG, TMAs, TMA, and TMI bubbler temperatures were maintained at -10°C, 10.0°C, 18.1°C, and 19.9°C, respectively. The structures were grown in an atmospheric pressure MOCVD reactor.

2.3.2 Ohmic Metal

Ohmic metal patterns were formed using standard contact ultraviolet (UV) photolithography and lift-off techniques. A stack of Pd-Ge-Au was evaporated and alloyed at 440°C for 40 seconds to form ohmic contacts. The characteristics of ohmic contacts can be found in Sections 3.4.1 and 3.4.2.

2.3.3 T-Gate Fabrication

The gate length of an FET is a very important physical parameter since it is inversely proportional to the intrinsic speed of the device. However, as the gate length of an FET gets smaller, parasitic effects, such as gate resistance along the width of the gate metal, begin to degrade the performance. A tri-layer T-gate process was developed to resolve the problem by increasing the gate cross-sectional area to reduce the resistance along the gate metal, yet allowing the "footprint" of the gate to remain small to optimize performance.

After the gate openings were defined using electron-beam (E-beam) lithography, the $In_{0.53}Ga_{0.47}As$ cap was etched using a non-selective wet chemical etchant (H_3PO_4:H_2O_2:H_2O). The gate metal, Ti-Pt-Au, was then evaporated and lifted-off.

2.3.4 Isolation

Device isolation was performed by chemically etching a mesa down to the InP substrate using H_2SO_4:H_2O_2:H_2O etch. There was no parasitic gate-leakage path at the mesa sidewall since the mesa etch was performed after the evaporation of the gate metal. Typical device-to-device isolation was greater than 5 MΩ.

2.3.5 Passivation

All wafers were passivated with 700 Å of Si_3N_4 using silane and ammonia reactants. A plasma-enhanced chemical vapor deposition (PECVD) system was used to deposit the nitride at 250°C. The pressure inside the chamber was maintained at 650 µtorr, and the RF power during the deposition was 35 W. This passivation procedure is still experimental for InP-based HEMTs. The results of related experiments are described in Section 3.5.

2.3.6 Air Bridge

Source pads of multi-finger devices were connected with air bridges. Air bridges were formed by patterning insulating pads of thick resist over gate and drain fingers. The source pads were then connected by evaporating gold over these pads. The insulating pads keep the metal from "shorting-out" the gate and the drain contacts. All interconnects as well as gate and drain bonding pads were thickened in the process.

Although a great care was given to ensure identical fabrication processes for different wafers, certain steps differed from wafer to wafer. For example, during the gate recess step described in Section 2.3.3, the wafers were etched one at a time. Immediate feedback on the effects of the etch was received for each wafer thereby allowing the opportunity to adjust the etch process to obtain the optimal results for the remaining wafers. Unfortunately, this had the effect of varying some device figures of merit among different wafers, but attempts have been made to appropriately compensate for the variance during data analysis.

2.4 Geometry of Devices and Test Structures

2.4.1 Coplanar HEMTs

Coplanar HEMTs were characterized. An impedance-matched RF probe station was used to measure these devices without unwanted oscillations that are frequently observed in InP-based HEMTs. The vast majority of the characterized devices had 2 gate fingers, each 100 μm wide, for the total gate width of 200 μm as shown in Figure 2.4. Source-drain spacing (L_{sd}) varied from 1.6 μm to 2.6 μm with T-gates located nominally in the center of the spacing. Since gates were centered, one may calculate the gate-drain spacing (L_{gd}) by using $L_{gd} = \frac{L_{sd}}{2} - \frac{1}{2}L_g$. A few devices with 4 gate fingers were measured. For these

devices, source pads were connected with an air bridge as described in Section 2.3.6.

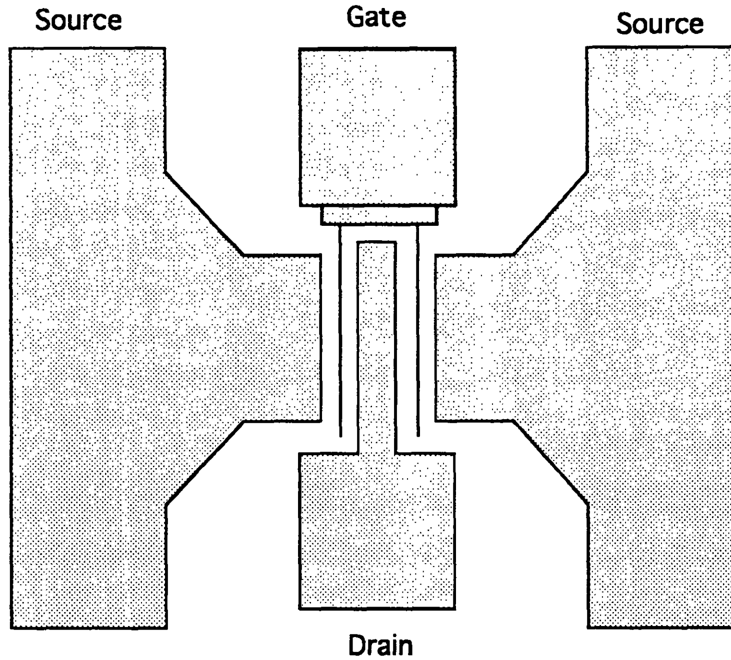

Figure 2.4: Schematic of a coplanar HEMT with 100 μm unit gate width and 2 fingers.

2.4.2 TLM Test Structures

Transmission-line model (TLM) structures were used to measure channel sheet resistance and ohmic contact resistance [41]. As shown in Figure 2.5, TLM structure consists of several alloyed ohmic contacts of similar dimension fabricated over the same channel but spaced unequally apart. The ohmic-to-ohmic resistance R_j measured at spacing j is given by

$$R_j = 2R_C + R_{SH}\frac{L_j}{W} \tag{2.1}$$

where R_C is the ohmic contact resistance, R_{SH} is the channel sheet resistance, L_j is the ohmic-to-ohmic spacing, and W is the channel width. If R_j is measured at several spacing j and plotted as a function of L_j, the Y-intercept gives twice the ohmic contact resistance ($2R_C$), and the slope gives the channel sheet resistance R_{SH}.

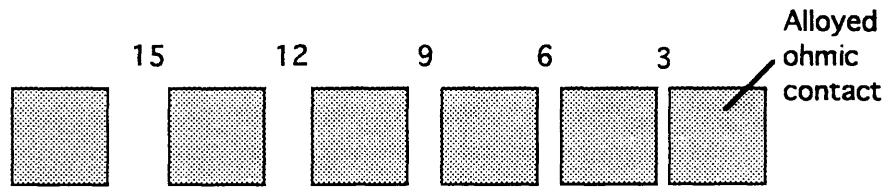

Figure 2.5: TLM structure. Numbers above the contacts represent the spacing in μm.

2.4.3 Gate Resistance Measurement Structures

As described in Section 2.3.3, parasitic effects of gate resistance along the width of the gate metal begins to dominate and degrade HEMT performance as the gate length decreases below 1 μm. Development of a T-gate process, however, has partly alleviated the problem. The test structure shown in Figure 2.6 was used to measure the gate resistance. A range of current is forced through metal pads A and D while resulting voltages are measured in pads B and C. By plotting the voltage versus the current, resistance can be calculated from the slope of the curve. Since the resistance is inversely proportional to the gate length, information about the gate length can also be obtained using this measurement.

2.5 Conclusion

Chapter 2 has described the possible effects of varying the AlAs mole fraction of the InAlAs Schottky barrier on the performance of HEMTs. The fabrication process has also been described, as well as the geometry of active devices and test structures.

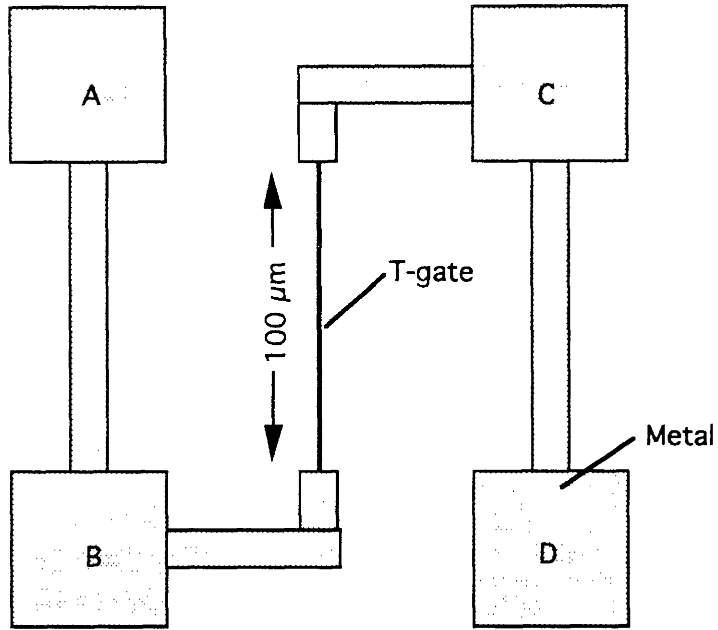

Figure 2.6: Gate resistance measurement structure.

Chapter 3. Results and Discussion

In this chapter, results from the Hall effect measurement of HEMT structures with varying AlAs mole fraction Schottky barriers are presented. DC and RF characteristics of HEMTs fabricated using these structures are also presented and compared. In addition, effects of parasitic elements and passivation on device performance are discussed.

3.1 Material Characteristics

Sheet electron concentrations (n_s) and electron mobilities (μ_e) were measured utilizing the Hall effect. Results of the measurements are shown in Table 3.1. Typical values from a GaAs-based PHEMT structure ($Al_{0.24}Ga_{0.76}As$/ $In_{0.16}Ga_{0.84}As$) are included for comparison.

Table 3.1: Hall effect measurements.

AlAs Mole Fraction	48% (Q54-1)	55% (Q54-2)	60% (Q54-3)	65% (Q54-4)	AlGaAs/ InGaAs
μ_e @ T = 300 K ($cm^2 V^{-1} s^{-1}$)	7,131	5,000	7,236	7,559	6,820
μ_e @ T = 77 K	16,351	9,100	18,457	18,212	19,236
n_s @ T = 300 K (cm^{-2})	3.7E12	4.1E12	3.5E12	2.9E12	3.3E12
n_s @ T = 77 K	3.6E12	4.3E12	3.4E12	2.8E12	3.2E12

Growth conditions outlined in Section 2.3.1 were used for all four wafers. Obviously, growth conditions for $In_xAl_{1-x}As$ Schottky layers were different for each wafer in order to vary the AlAs mole fraction. The doping level was kept constant. Since the $In_{0.52}Al_{0.48}As$ spacer layer was lattice matched to the $In_{0.53}Ga_{0.47}As$ channel on all four wafers, the conduction bandgap discontinuities should be the same in all four, and the sheet electron concentrations should not change very much as the AlAs mole fraction varied. Since sheet carrier

concentration is directly proportional to maximum channel current, it is important to have high n_s, especially for power applications (see Section 1.2). However, there existed a reduction in sheet electron concentration as the AlAs mole fraction increased from 55% to 60% and 65%.

Brown *et al.* studied the characteristics of Al-rich InAlAs Schottky barriers for InP-based HEMT structures. They observed a decrease in silicon activation and an increase in silicon segregation for higher AlAs mole fraction InAlAs layers [42]. Their findings are consistent with the measurements made in this work where the decrease in electron sheet concentration for higher AlAs mole fraction Schottky barriers may be due to such dopant-related effects. However, the above explanation does not resolve the pattern between wafers Q54-1 and Q54-2. Relying on the observations made by Brown *et al.*, one would have expected the highest sheet electron concentration from wafer Q54-1, not Q54-2. The reason for this anomaly is not yet known.

Silicon segregation from the pulse doping layer has been found to exhibit a large dependence on the growth temperature of the InAlAs Schottky layer. Reduction in growth temperature from 500 °C to 420 °C dramatically reduced the extent of silicon segregation in InAlAs [42]. As described in Section 2.3.1, active layers for devices used in this work were grown at 650 °C, establishing the possibility that the same performance-degrading phenomena may have affected the materials studied in this work.

As expected, even with dopant-related phenomena, larger conduction band discontinuity of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterojunction resulted in a higher sheet electron density than $Al_{0.24}Ga_{0.76}As/In_{0.16}Ga_{0.84}As$ junction of GaAs-based PHEMTs.

3.2 DC Results

To assess the power performance potential of InP-based HEMTs with pseudomorphic Schottky barriers at millimeter-wave frequencies, an extensive amount of testing was done throughout the fabrication process to evaluate the quality of materials, processes, and devices. Characteristics of these devices were then compared with each other and with Raytheon's GaAs-based PHEMTs, which have demonstrated record power performances at *Q*-band [43].

3.2.1 Threshold Voltage

One of the most crucial steps in HEMT fabrication process is the recessing of the cap layer. Although there have been reports of obtaining very uniform threshold voltages ($\overline{V_t} = -234$ mV, $\sigma V_t = 15$ mV) of InAlAs/InGaAs/InP HEMTs across a 2-inch wafer using a 1:1 citric acid:H_2O_2 solution [44], the same process was not used in this work (see Section 2.3.3). Figures 3.1 shows the threshold voltage values from different wafers. Threshold voltage was defined as V_{GS} at which the resulting saturated drain current (at V_{DS} = 1 V) equals 2% of the drain current at V_{GS} = 0.3 V and V_{DS} = 1 V. The box shown in Figure 3.1 represents the middle 50% of the data distribution with the middle line being the median value. The lines extending from the top and bottom of each box mark the maximum and minimum for each variable.

Thickness of the InAlAs Schottky barrier, controlled by the etch depth, is a very important physical parameter because it affects many key device figures of merit. Thinner Schottky barriers correspond to less negative threshold voltages because of the proximity of the gate to the 2-DEG. For this reason, comparison of devices with relatively large differences in threshold voltages makes the process of evaluating the intrinsic device performance difficult. For example, as shown in Equation (1.8), intrinsic transconductance of an FET is inversely proportional to

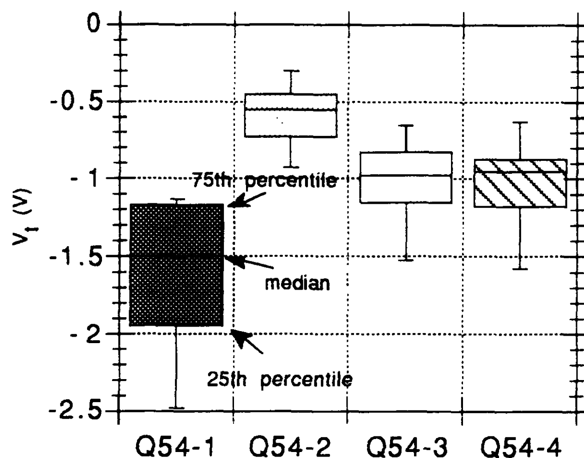

Figure 3.1: Threshold voltage distribution (post-passivation).

the thickness of the insulating layer. Since a non-selective etchant was used to recess the cap layer, it is quite possible that different thicknesses of $In_xAl_{1-x}As$ remained for different devices after the etch. Etching into the $In_xAl_{1-x}As$ layer decreases the thickness, thereby increasing the transconductance. Thinner Schottky barriers decrease the saturated channel current because of the reduced V_{GS} swing that results from a more positive threshold voltage. These features are indeed present in the data shown in Figures 3.2 and 3.3.

Figure 3.2 shows the decrease in saturated drain current for less negative threshold voltages. Saturated drain current was measured at V_{GS} = 0 V and V_{DS} = 1 V. Figure 3.3 shows that less negative threshold voltages correspond to higher peak transconductances. Devices were biased at V_{DS} = 1 V while V_{GS} was swept from below the threshold voltage to +0.3 V. The reported value is the maximum value for any V_{GS}.

Because of the non-uniformity of threshold voltages, it was difficult to reach definite conclusions about the effects of different AlAs composition in the Schottky barriers. In order to remove the possibility of the etch depth affecting

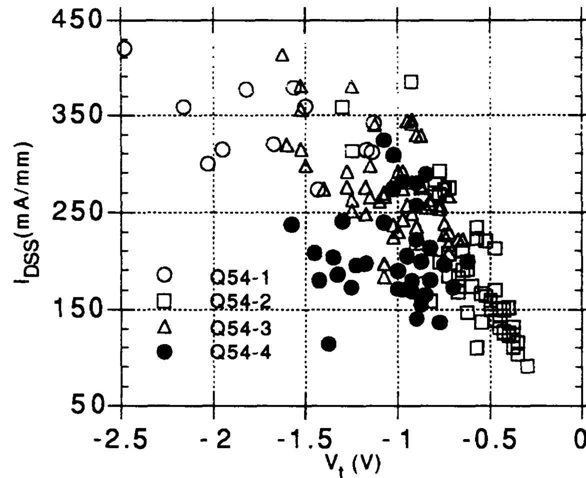

Figure 3.2: Saturated drain current versus threshold voltage (post-passivation).

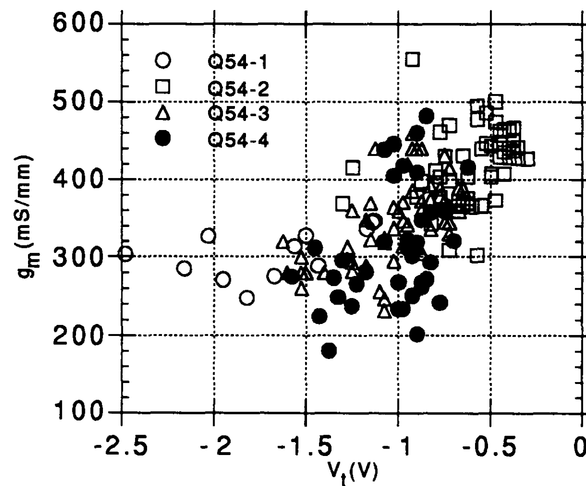

Figure 3.3: Peak extrinsic transconductance versus threshold voltage (post-passivation).

the behavior of devices from different wafers, a group of devices were selected from each wafer based solely on the threshold voltage. The chosen devices each had the threshold voltage in the range -0.8 V > V_t > -1.2 V. Results and discussions in Sections 3.2.2-3.2.4 are limited to the devices included in this group. I-V plot of a typical device in this group is shown in Figure 3.4.

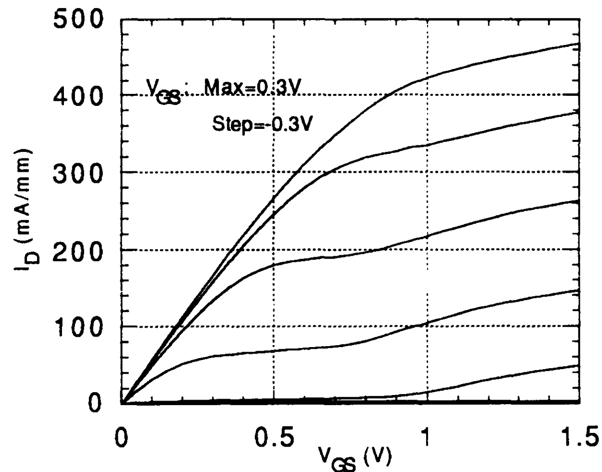

Figure 3.4: I-V plot of a typical device from wafer Q54-3.

The I-V plot in Figure 3.4 shows the characteristic "kink" found in most InP-based HEMTs. The origin of the "kink" has been attributed to traps in the InAlAs buffer or Schottky layer [45], [46].

3.2.2 Saturated Drain Current

As shown by Figure 3.5, there was a systematic decrease in saturated drain current as the AlAs mole fraction of the InAlAs Schottky barrier increased. This behavior was expected from the Hall effect measurement presented in Section 3.1 where the sheet electron concentration decreased as the AlAs mole fraction increased. Devices from wafer Q54-1 had higher than expected current level, but the validity of the data is questionable because the wafer had only 3 devices with threshold voltages in the selected range described in the previous section.

3.2.3 Transconductance

Figure 3.6 shows that the peak extrinsic transconductance of devices do not change very much as a function of AlAs mole fraction of the Schottky barrier. (The wide spread in data masked the presence of any clear trends.) As shown

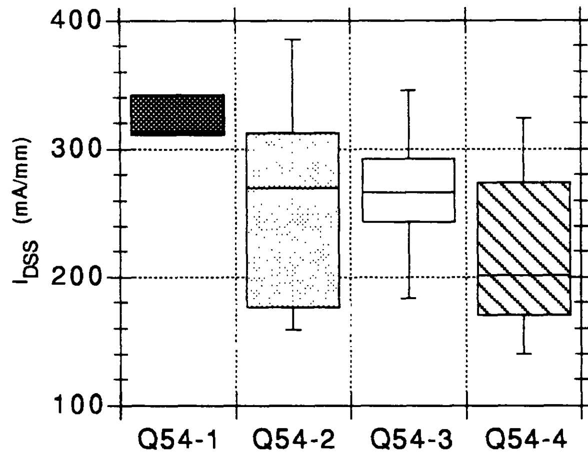

Figure 3.5: Saturated drain current of devices with threshold voltages between -0.8 and -1.2 V (post-passivation)

later in Section 3.3.2, this is in agreement with Equation (1.8), which predicted $g_{m0} \propto v_{sat}$ behavior, for calculated values of v_{sat} were very similar for devices from different wafers.

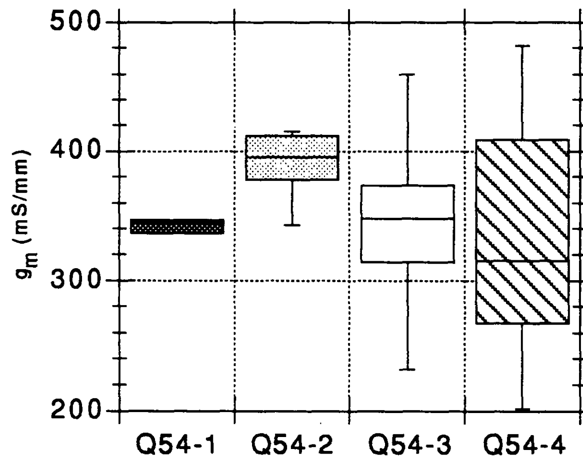

Figure 3.6: Peak transconductance of device with threshold voltages between -0.8 and -1.2 V (post-passivation).

Figure 3.7 shows g_m vs. V_{GS} characteristics of typical devices from each wafer. Devices from wafers Q54-2, Q54-3, and Q54-4 exhibited very similar

characteristics while the device from wafer Q54-1 exhibited a plateau not seen in devices from other wafers. The origin of this is not yet determined. Figure 3.8 shows g_m vs. I_D plot of the same devices.

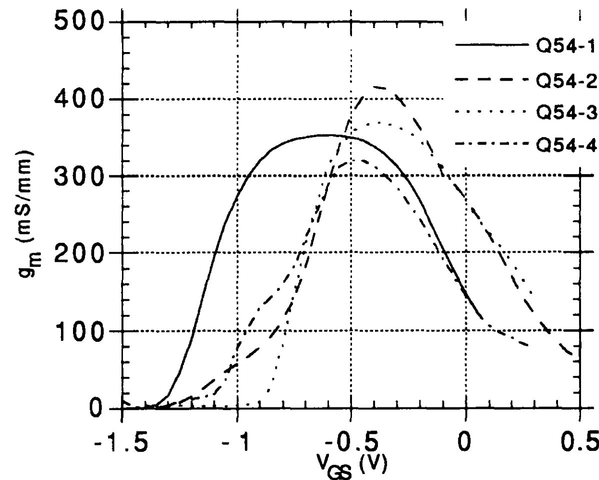

Figure 3.7: Transconductance versus gate-source voltage of typical devices from each wafer.

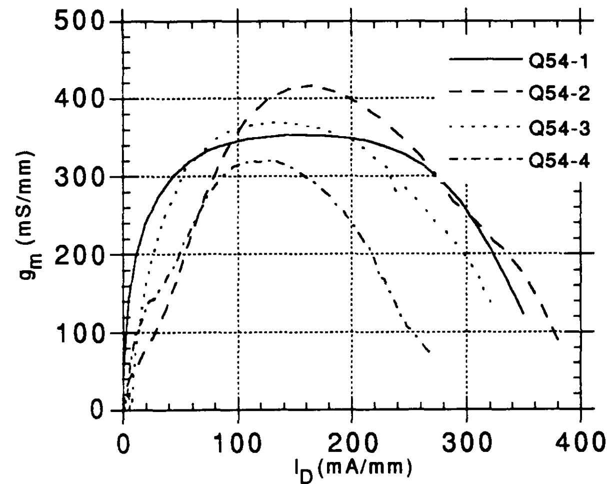

Figure 3.8: Transconductance versus drain current of typical devices from each wafer.

3.2.4 Forward Turn-on Voltage

Low Schottky barrier height of $In_{0.52}Al_{0.48}As$ has prevented applying V_{GS} greater than ~0.4 V due to the large gate current that is produced at high positive V_{GS}. An FET may be able to carry more current in the channel if the gate is forward biased, but the increase in gate current makes this mode of operation for InP-based HEMTs impractical. In addition, if a device is able to achieve optimal performance at positive V_{DS} and V_{GS} bias conditions, there would be no need for a bipolar power supply, greatly relaxing the system design constraints.

It has already been shown that the increase in the AlAs mole fraction of InAlAs increases the Schottky barrier height [26]-[29], and as shown in Appendix B, an increase in Schottky barrier height reduces both forward and reverse current. Devices with similar threshold voltages were compared. In order to measure the forward turn-on voltage (V_{on}), both drain and source terminals were grounded while I_G was increased from 0 to 1 mA/mm. As shown in Figure 3.9, V_{on} is defined as V_{GS} at which a linear interpolation of high current values intercepts the x-axis.

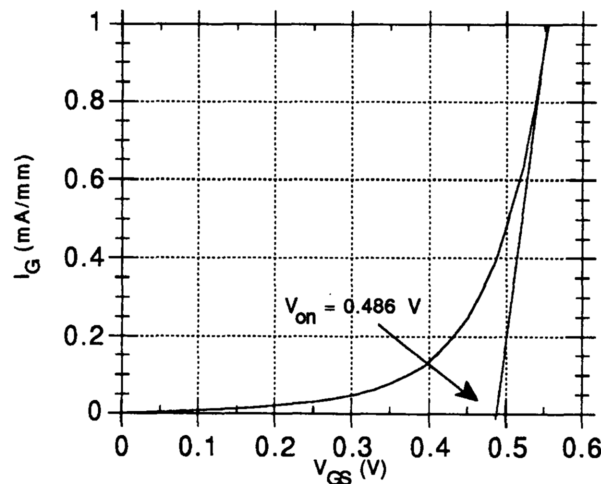

Figure 3.9: An example of V_{on} measurement of a typical device from wafer Q54-3 ($V_{DS} = 0$).

Figure 3.10 shows the values of forward turn-on voltages for each wafer. Once again, data from wafer Q54-1 may be misleading because only 3 devices were measured from this wafer. For other wafers, which had significantly larger number of devices, V_{on} expectedly increased as the AlAs mole fraction of the Schottky barrier increased.

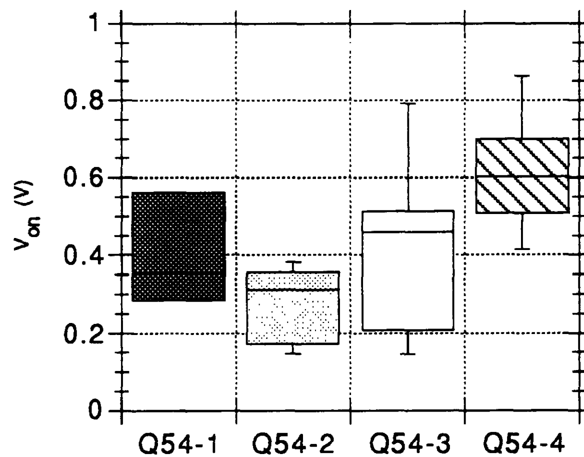

Figure 3.10: Forward turn-on voltages of devices with threshold voltages between -0.8 and -1.2 V (post-passivation).

3.2.5 Breakdown Voltage

As discussed in Sections 1.2 and 1.3.2, InAlAs/InGaAs/InP HEMTs suffer from low breakdown voltages that make them unable to produce high output power. Only a limited amount of work has been done on the physics of breakdown of InP-based HEMTs [47], [48], while significantly more work has been done on GaAs-based HEMTs and MESFETs [49]-[55]. The majority of these studies has indicated that the source-drain breakdown voltage of a HEMT is limited by gate-drain breakdown. Electrons are injected into the channel from the gate by a combination of thermionic emission and tunneling, and the high electric field of the region between the gate and the drain starts an impact-

ionization process producing both holes and electrons. Some holes are swept into the gate while the rest flow to the source where they recombine with electrons. The electrons are swept into the drain causing a rise in drain current and thus limiting the source-drain breakdown voltage. A schematic of this process is shown in Figure 3.11.

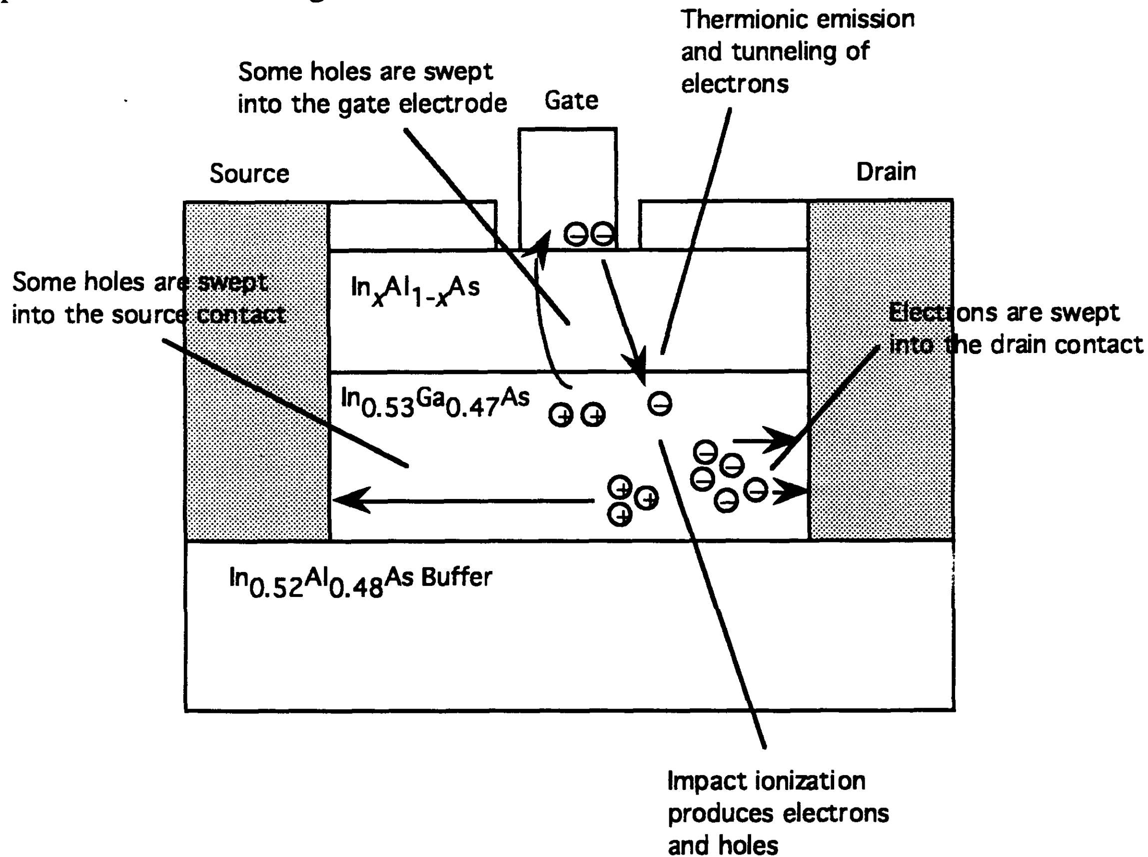

Figure 3.11: Schematic of breakdown in an InP-based HEMT.

3.2.5.1 Gate-Drain Breakdown

While source-drain breakdown voltage determines the maximum operating drain voltage of a HEMT, higher gate-drain breakdown voltage is also needed for better power performance since, as described later in this section and also in Section 3.2.5.2, BV_{DS} of a HEMT is ultimately limited by the gate-drain breakdown. Two-terminal BV_{DG} was measured as a function of source-drain spacing and AlAs mole fraction of the Schottky barrier. The device-under-test

had the source floating, and the drain grounded, while a negative current was forced through the gate. The current was increased from 0 mA/mm to -1 mA/mm, at which point the voltage developed across the gate terminal and the drain terminal was defined as BV_{DG}. A typical breakdown voltage measurement is shown in Figure 3.12. Figures 3.13 and 3.14 show the effects of source-drain spacing and AlAs mole fraction of the insulator on gate-drain breakdown voltage, respectively. These measurements are from the pre-passivation stage of the fabrication process since changes in breakdown voltage were observed after passivation (see Section 3.5); the changes due to passivation may have influenced the effects of L_{sd} on BV_{DG}.

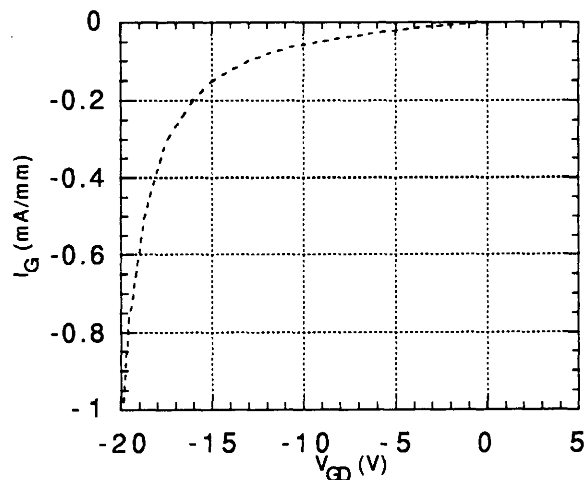

Figure 3.12: Gate-drain breakdown voltage measurement of a typical device from wafer Q54-2 (pre-passivation). Source terminal was left floating.

Figures 3.13 and 3.14 show improved BV_{DG} for larger L_{sd} and higher AlAs mole fraction Schottky barriers. These dependencies may be explained by the following mechanisms of breakdown. Gate-drain breakdown of a HEMT has been attributed to a combination of thermionic emission and tunneling of electrons across the Schottky barrier and avalanche breakdown. As the bias on the gate becomes stronger, the electric field can become sufficiently large so that

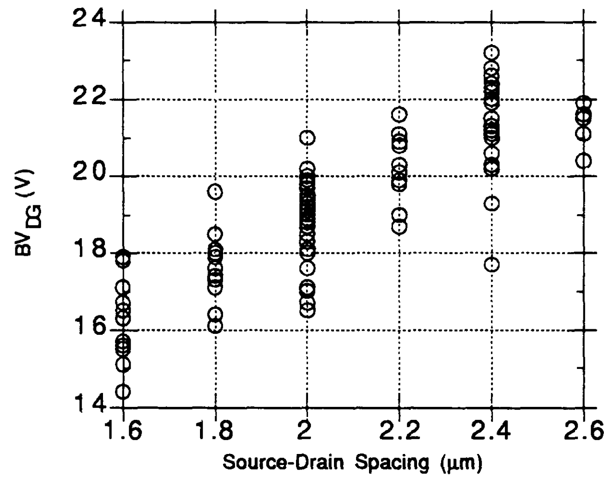

Figure 3.13: Gate-drain breakdown voltage versus source-drain spacing of all HEMTs from wafer Q54-2 (pre-passivation).

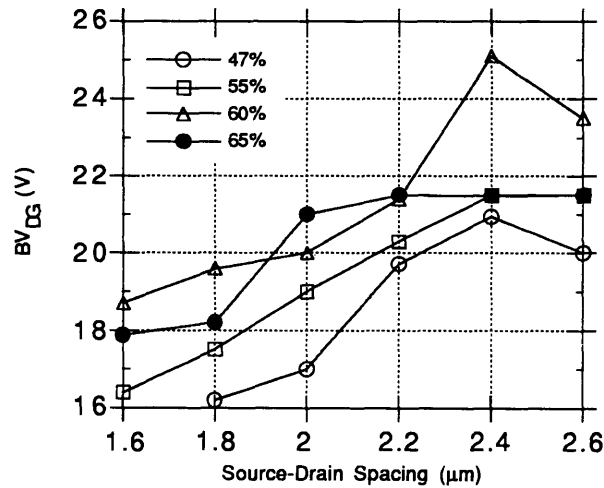

Figure 3.14: Median values of gate-drain breakdown voltage versus source-drain spacing of HEMTs with different AlAs mole fraction Schottky barriers (pre-passivation).

thermionic emission and tunneling of electrons take place. These electrons then flow to the drain and provide a leakage current [50]. The rate of tunneling and thermionic emission decrease exponentially for larger ϕ_B, reducing the gate leakage current and thus increasing the gate-drain breakdown voltage [56].

As drain-gate potential increases, the depletion region under the gate begins to widen from the gate edge toward the drain. Extra potential is supported by this lateral spreading of the depletion region. The electric field can become sufficiently high in the depletion region for impact ionization to occur in the channel. As shown in Figure 3.12, the breakdown characteristic was rather "soft" in most devices, indicating that avalanche breakdown does not take place. Hence, it is likely that breakdown consists of tunneling, thermionic emission, and impact ionization.

In order to accurately predict the effects of different device parameters, a 2-dimensional model is necessary. The model needs to calculate the electric field distribution inside the device as well as the ionization coefficient of carriers in the field. No such models have been published for InP-based HEMTs. However, models based on GaAs MESFETs and HEMTs suggest that gate-drain breakdown indeed does occur at the drain side of the gate metal due to high electric field, and larger L_{gd} reduces the peak electric field and delays the onset of breakdown due to thermionic emission, tunneling and impact ionization [49]-[55]. The agreement between the data compiled in this work and the past simulations of GaAs-based FETs [49]-[55] suggests that the breakdown processes outlined above do indeed occur in InP-based HEMTs.

It should be noted that as the AlAs mole fraction of the Schottky barrier reached 65%, the BV_{DG} decreased in contrast to explanations given above. The reasons for this unexpected behavior is not clear. However, one might suspect that due to the high Al content of $In_{0.35}Al_{0.65}As$, a thick layer of aluminum oxide may exist between the gate metal and the semiconductor. Formation of aluminum oxide has been observed on $In_{0.52}Al_{0.48}As$ [31]. This aluminum oxide layer may have been responsible for the deviation from expected Schottky characteristics [29], [31].

Devices fabricated in this work exhibited much higher BV_{DG} than any other previous reports of InP-based HEMTs with single recess [6], [19]. The reasons for this vast improvement is not yet known.

3.2.5.2 Source-Drain Breakdown

Source-drain breakdown voltage of a HEMT must be increased in order to produce higher output power as discussed in Section 1.2. Bahl *et al.* have reported a novel and simple way of measuring the off-state 3-terminal breakdown voltage of FETs [57]. Results obtained using this method are equivalent to the source-drain breakdown voltages that may be measured by first biasing the gate terminal to pinch-off the channel, then increasing V_{DS} until the drain current reaches a specified value, usually 1 mA/mm. Unfortunately, BV_{DS} could not be measured on all devices due to the fact that attempts to measure BV_{DS} often resulted in catastrophic failures of devices. There were, however, a limited number of devices that could be measured, but the small sample size prevented any meaningful conclusions about the effects of AlAs mole fraction of the Schottky barrier or L_{gd} on the source-drain breakdown voltage. Still, some information about physics of breakdown may be obtained by studying the breakdown characteristics.

Figure 3.15 displays the three-terminal breakdown voltage measurement of a typical device. The peak of V_{DS} corresponds to a large increase in gate current. Also, V_{DG} is nearly constant for $V_{GS} \ll 0$. These facts suggest that the source-drain breakdown voltage is indeed limited by the gate-drain breakdown, similar to GaAs-based HEMTs and MESFETs [47]-[55]. Based on this result, it is plausible to conclude that BV_{DS} of an InP-based HEMT will improve if one can increase BV_{DG}.

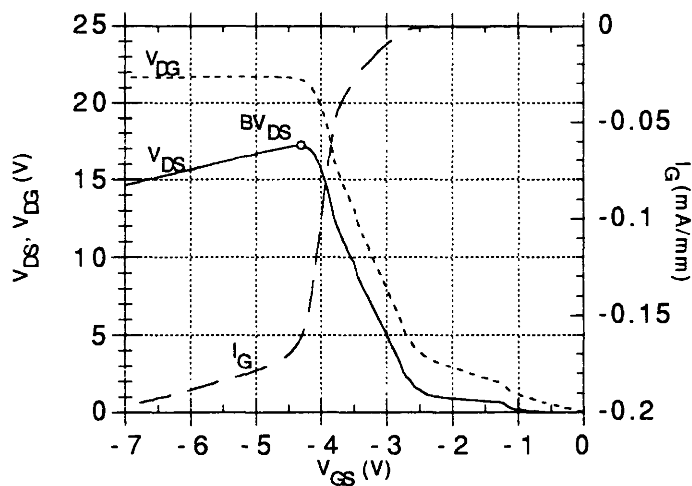

Figure 3.15: Drain-current injection scan of a PHEMT from wafer Q54-4 (I_D = 0.25 mA/mm). BV_{DG} is not shown on this scale. The device failed after the measurement.

Causes for the catastrophic failures of devices during and after source-drain breakdown voltage measurement remain unclear. As shown in Figure 3.16, failures often occurred between the gate metal and the drain contact. It was not possible to determine whether the failure was initiated from the gate metal edge or the drain contact edge. One source of the problem may be the roughness of the gate recess and the gate metal as shown in Figure 3.17. For a fixed applied voltage, electric field is proportional to the radius of curvature of the local metal. Rough edges of the gate recess, such as the ones shown in Figure 3.17, may have been subjected to anomaly high electric fields and induced premature and catastrophic avalanche breakdown.

Similar burnout problems were reported in late 1970's and early 1980's by workers in the field of GaAs MESFETs [58]-[60], who attributed the problem to the drain ohmic contact. They reported the presence of molten eruptions of GaAs-ohmic metal mixture near the edge of the contact, similar to those shown in

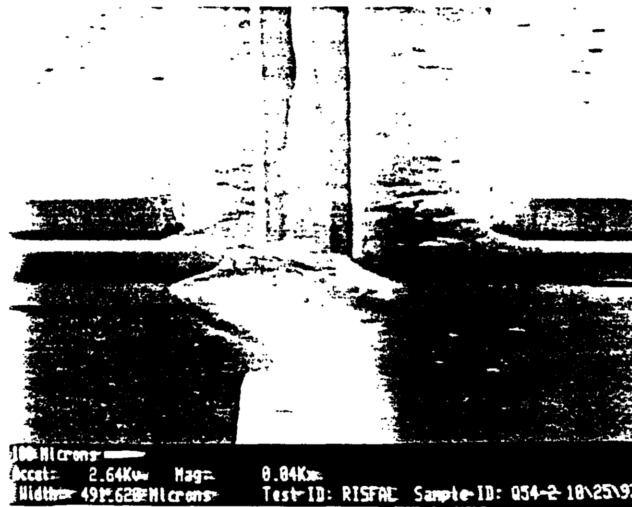

Figure 3.16: Picture of a failed device. Left pad is the drain contact, and the center metal is the T-gate.

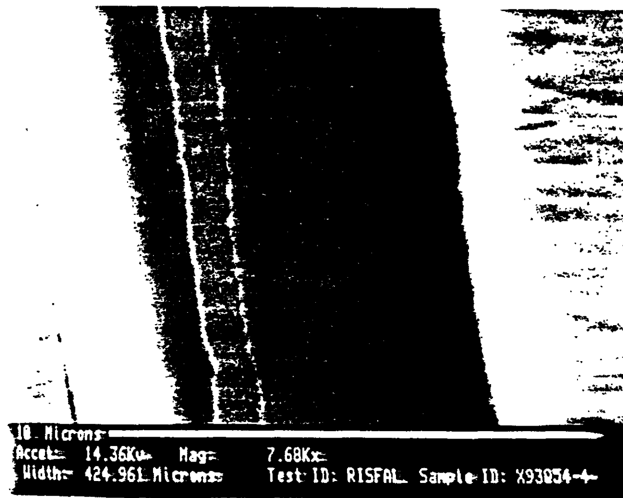

Figure 3.17: Picture of the gate trench after the etch. Left pad is the drain contact, and the right pad is the source contact. Notice the rough edges of the trench.

Figure 3.16. They resolved the problem by employing an n^+ contact layer under the ohmic drain to smooth the high electric field. The $In_{0.53}Ga_{0.47}As$ cap layer employed in this work was undoped and may have contributed to the problem of catastrophic burnout.

3.2.6 Presence of Impact Ionization

Electron ionization rate of $In_{0.53}Ga_{0.47}As$ has been found to be significantly larger than that of GaAs [61]. Electron ionization rate is defined as the number of electron-hole pairs generated by an electron per unit distance traveled. As suggested by [47] and [48], this fact promotes the multiplication process that increases the channel current and initiates the source-drain breakdown of an InAlAs/InGaAs/InP HEMT. The presence of impact ionization in the channel has been observed by monitoring the holes that are created by the impact ionization in the channel. Heedt *et al.* have observed an increase in gate leakage current due to holes in lattice-matched $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ HEMTs [62]. Figure 3.18 shows the gate leakage current measurement from a typical device processed in this work.

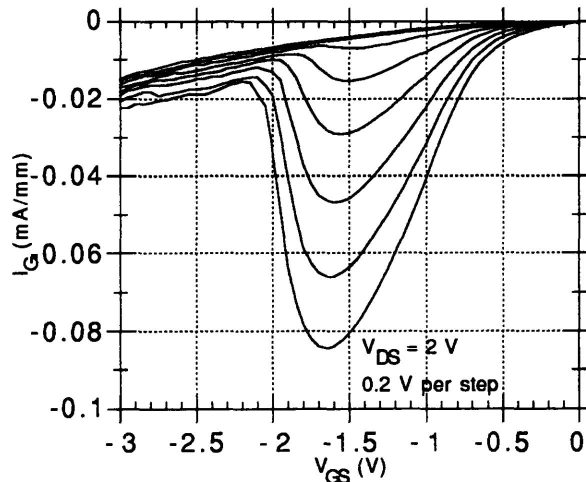

Figure 3.18: Gate leakage current of a typical device from wafer Q54-4.

At a low V_{DS}, the gate leakage current is mostly due to electrons tunneling through the Schottky barrier. However, as V_{DS} is increased beyond 1 V, impact ionization starts in the $In_{0.53}Ga_{0.47}As$ channel. For $V_{GS} < -2$, the device is off and no impact ionization occurs. However, as the device turns on around V_{GS} = -2 V,

impact ionization starts in the channel, and the holes created by the process are swept to the most negatively biased terminal, the gate, thus increasing the negative gate current (see Figure 3.11 for a schematic diagram of this process). Subsequent peak and decline of the gate current due to the generation of holes depend on the gate bias and the resulting valence band structure. As shown in Figure 2.1, the valence band forms a "hole barrier" in thermal equilibrium. As the voltage on the gate is swept from beyond the threshold voltage to 0 V, the magnitude of the valence band discontinuity begins to change. Exact magnitude cannot be known without resorting to numerical methods. Devices with larger AlAs mole fraction in the Schottky barrier should have higher "hole barrier" due to their larger bandgap energies, and hence smaller "hump" in the gate leakage currents. However, the difference in valence band discontinuities are very small for differing AlAs mole fractions, and no significant difference was observed in devices from different wafers.

3.2.7 Comparison of Key DC Parameters

Table 3.2 lists some key DC parameters of typical devices fabricated in this work ($L_g \approx 0.15$ μm) as well as those of a typical GaAs-based power PHEMT fabricated at Raytheon ($L_g \approx 0.2$ μm) [43]. Relatively low maximum drain current and peak transconductance of InP-based HEMTs fabricated in this work are probably due to poor quality of epitaxial material as discussed in Section 3.1. Much higher current densities and transconductances have been reported previously for InP-based HEMTs [2]-[4], [6], [10]-[12]. The breakdown voltage and forward turn-on voltage were comparable to the GaAs-based PHEMT. As higher levels of current and transconductance are attained through growing better quality material, InP-based HEMTs with pseudomorphic Schottky barriers should have better DC characteristics than GaAs-based PHEMTs.

Table 3.2: Some key DC parameters of GaAs-based power PHEMTs [43] and of InP-based HEMTs fabricated in this work.

	Q54-1	Q54-2	Q54-3	Q54-4	GaAs-based PHEMT
I_{Dmax} (mA/mm)	373	405	355	306	580
I_{DSS} (mA/mm)	321	297	262	205	250
g_m (mS/mm)	363	426	371	325	545
BV_{DG} (V)	17.5	19.1	20.6	21.1	12.5
BV_{DS} (V)	-	-	-	-	11.9
V_{on} (V)	0.35	0.3	0.47	0.65	0.78
V_k (V)	0.7	0.6	0.62	0.55	0.5

3.3 RF Results

3.3.1 Test Setup

Valuable information about performance of HEMTs at high frequencies can be obtained by studying their RF characteristics. The simplest way to model the high frequency behavior is to derive a small-signal equivalent circuit model. To derive such a model, S-parameter measurements were made. Parasitic capacitances and inductances, arising mostly from fringing electric field around metal pads, were subtracted out, but parasitic resistances, including R_s, R_d, and R_g, were assimilated into the equivalent circuit, for exact values of these elements could not be measured. Hence, the extracted model may not be the unique representation of the device. However, since all measured devices had the same layout, the parasitic elements are equivalent for each device, and the relative values can still provide valuable information.

S-parameter measurements were made on-wafer with impedance matched coplanar probes. The S-parameters of the devices at frequencies from 1 GHz to 18

GHz were made for several V_{GS} and V_{DS} values to determine the bias dependence of the model. The measured S-parameters were converted to Y-parameters, and the Y-parameters were then solved to obtain the small-signal equivalent circuit model shown in Figure 3.19.

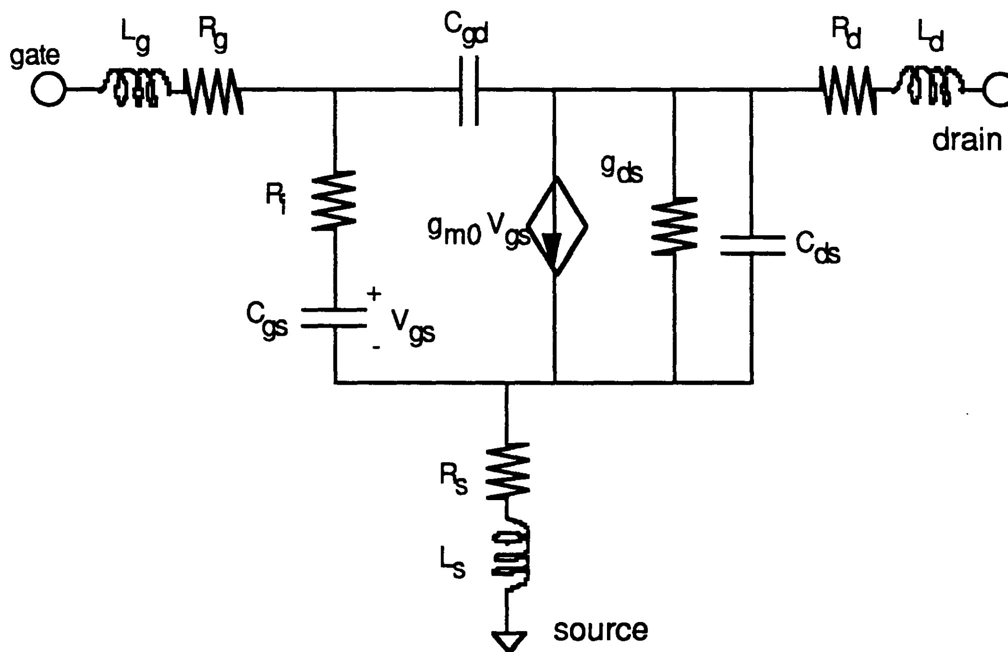

Figure 3.19: Small-signal equivalent circuit model neglecting parasitic elements.

3.3.2 Results and Discussions

Representative devices from each wafer were measured. The results are summarized in the Table 3.3 along with the results from a typical GaAs-based power PHEMT fabricated at Raytheon. Several key small-signal parameters, including C_{gs}, C_{gd}, g_{ds}, and f_T, did not vary much for different AlAs compositions in the insulator. All InP-based HEMTs fabricated in this work had higher maximum available gain at 18 GHz than a record-setting GaAs-based power PHEMT [43]. This result is very promising for RF power amplification.

Table 3.3: RF characteristics and small-signal equivalent circuit model element values for typical HEMTs. Devices were biased at V_{DS} = 1.5 V. V_{GS} varied for each parameter to give the "best" or "saturated" values.

	Q54-1	Q54-2	Q54-3	Q54-4	GaAs-based PHEMT
g_{m0} (mS/mm)	426	565	535	549	673
C_{gs} (pF/mm)	0.65	0.68	0.74	0.66	1.6
C_{gd} (fF/mm)	63.5	51.5	71.5	58.5	139
R_i (Ω mm)	2.38	2.4	1.58	2.26	1.38
g_{ds} (mS/mm)	38.6	25.6	40.0	29.5	6.35
f_T (GHz)	96.6	110.1	98.1	108.4	58.59
f_{max} (GHz)	290.8	283	250.5	271.7	203.6
G_{max} @ 18 GHz (dB)	17.67	19.83	18.24	19.22	15.72

Neglecting parasitic gate capacitance C_{gp}, current gain cutoff frequency for a short-gate HEMT is commonly given by

$$f_T = \frac{v_{sat}}{2\pi L_g}. \tag{3.1}$$

Using Equation (3.1), f_T = 110.1 GHz and L_g = 0.15 µm correspond to v_{sat} of 1.04E7 cm/s, a value very close to the measured value in bulk $In_{0.53}Ga_{0.47}As$ [16]. However, values twice as high have been reported in the literature [63]. Relative closeness of f_T's among devices implies that v_{sat} has not degraded for high AlAs mole fraction Schottky barriers. The spacer-channel heterojunction seems relatively unaffected by the strain caused by the pseudomorphic Schottky barrier. f_T vs. V_{GS} characteristics of typical devices from each wafer are plotted in Figure 3.20.

Transconductances reported in Table 3.3 are higher than those measured under DC (low frequency) condition. Ketterson *et al.* had attributed these

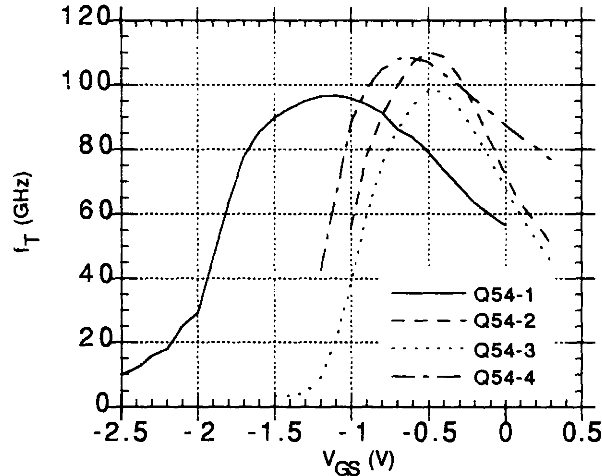

Figure 3.20: f_T versus gate-source voltage of typical devices.

discrepancies to frequency-dependent parasitic charge fluctuation in the InAlAs Schottky layer [64]. Charge fluctuations due to deep traps, free-electron generation, and neutralization of donors are all mechanisms that degrade the DC transconductance but not RF transconductance. At microwave frequencies, these traps lack sufficient time to react to change in gate voltage and are not modulated with the result that g_m is not reduced [64], [65]. A more detailed study of the material is necessary in order to control these traps and eliminate any degrading effects.

3.4 Parasitic Elements

3.4.1 TLM Measurements

TLM measurements were made using the structure shown in Figure 2.5. The results are summarized in Table 3.4 and Figures 3.21 and 3.22. Contact resistances were comparable to the best reported values for InP-based HEMTs and GaAs-based PHEMTs. Even though higher AlAs mole fraction of the $In_xAl_{1-x}As$ Schottky layer presents a larger barrier to the formation of ohmic

contacts, the metalization and the alloying process employed in this work seem immune to such increase in difficulty.

Table 3.4: Median values of contact and sheet channel resistances.

Wafer	Q54-1	Q54-2	Q54-3	Q54-4
R_C (Ω mm)	0.172	0.163	0.181	0.168
R_{SH} (Ω/sq)	381	296	452	348

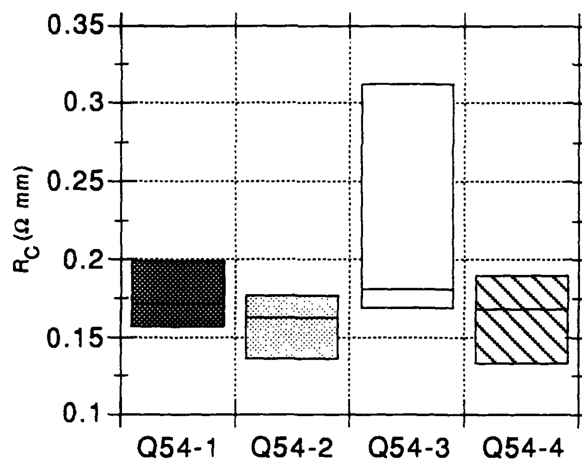

Figure 3.21: Contact resistance.

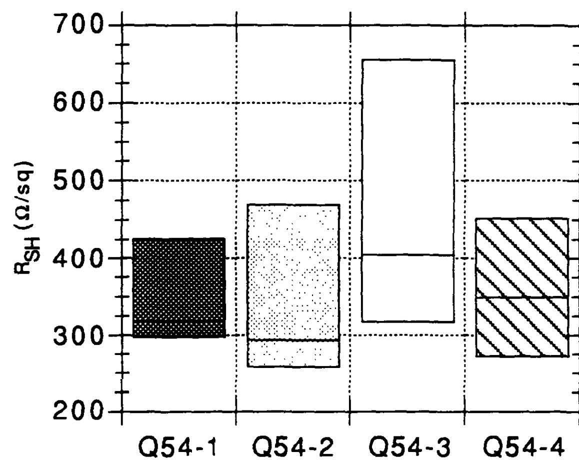

Figure 3.22: Channel sheet resistance.

Channel sheet resistance values were consistent with values that may be calculated using $R_{SH} = \frac{1}{q\mu_e n_s}$. However, one should note that this R_{SH} represents the value of the region underneath the cap and does not correspond to the value underneath the gate. Calculated values are 237, 305, 247, and 285 Ω/sq for wafers Q54-1, Q54-2, Q54-3 and Q54-4, respectively. There was no systematic degradation of the channel quality as the AlAs mole fraction of the insulator increased. Since the pseudomorphic interface was separated from the channel by the lattice-matched spacer layer, this insensitivity is not surprising.

As evident from Figures 3.21 and 3.22, the uniformity of measured values of R_C and R_{SH} over 2-inch wafers was poor. The exact cause of this non-uniformity is yet to be determined. However, Figure 3.23 provides some clues about factors that may be responsible.

Figure 3.23 shows the spatial distribution of contact resistance and channel sheet resistance. Bold dots representing position on the wafer correspond to the dark bars in the histograms of measured values. The center eight locations on the wafer all had channel sheet resistance between 200 and 300 Ω/sq, while the outer parts of the wafer had significantly higher resistances. This non-uniformity seems to indicate the existence of a circular pattern in measured values. Such distribution across a wafer may suggest problems with material growth. Since the wafers were continuously rotated during epitaxial layer growth, this may have resulted in the radial distribution observed in Figure 3.23.

Alloying process may also be responsible for the non-uniformity. There may have been an uneven distribution of heat over a wafer. Although InP substrate itself is a reasonably good heat conductor, the quartz succeptor used to hold the wafer in the furnace is not. Hence, the outer parts of the wafer may have reached a higher temperature than the center of the wafer. This difference in

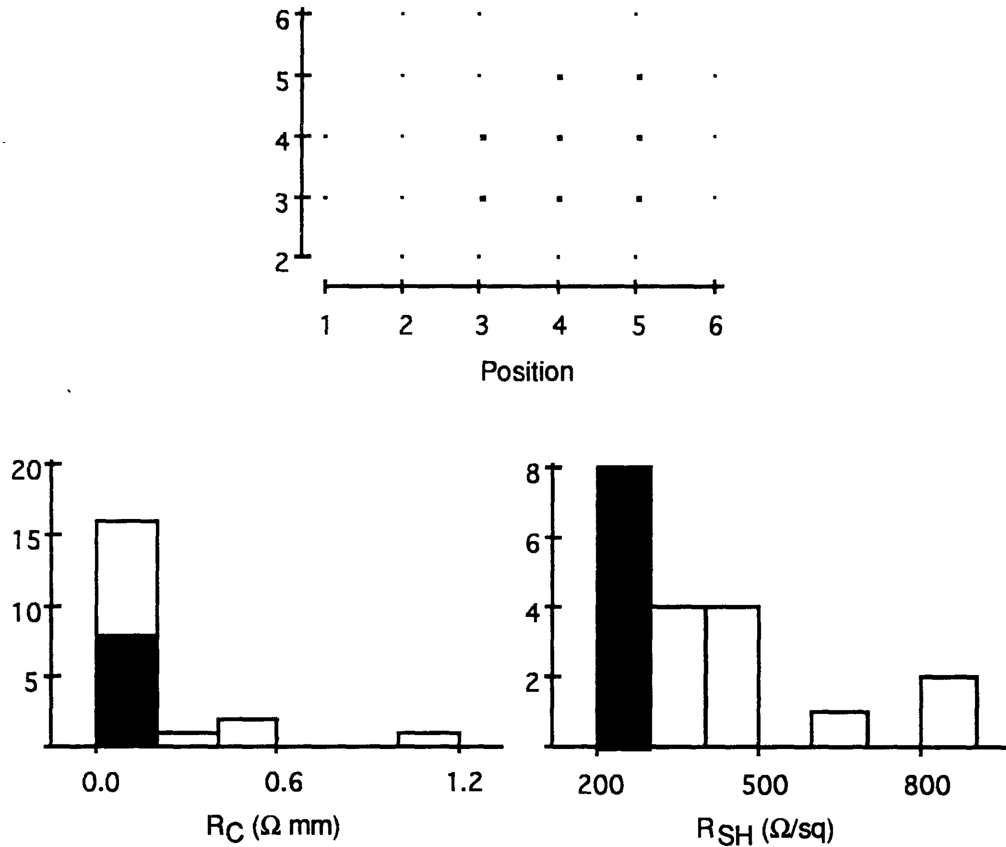

Figure 3.23: Spatial distribution of contact resistance and channel sheet resistance of wafer Q54-4.

temperature may have caused the spread in ohmic contact resistance and channel sheet resistance.

As already discussed in Section 3.2.1, non-uniformity of the data proved to be a big obstacle in reaching statistically significant conclusions due to the uncertainties about the data. Uniformity must be controlled in order to ensure future manufacturability of these devices. Temperature variation across the wafer during the alloying process may be resolved by using a succeptor made of a better heat conducting material, such as carbon. However, if the non-uniformity arises from material growth, more elaborate solutions may be needed.

3.4.2 Source Resistance

Source resistance is a very significant parasitic element that must be minimized in a high performance HEMT. For a fixed V_{GS}, larger source resistance increases the total on-resistance (R_{on}), decreases the channel current, and decreases the extrinsic transconductance. The last two items are especially important for power performance of a HEMT as shown in Section 1.2.

Unlike GaAs-based PHEMTs, formation of ohmic contacts on InP-based HEMTs presents a great challenge because the metal must make a direct contact to the channel through the large bandgap energy barrier of $In_xAl_{1-x}As$. In a GaAs-based PHEMT, this is not necessary since the GaAs contact layer forms parallel conduction paths from the source metal to the channel, lowering the access resistance [66].

The detrimental effects of source resistance on extrinsic transconductance of a HEMT is given by the following equation:

$$g_m = \frac{g_{m0}}{1 + g_{m0} R_s}. \tag{3.2}$$

This effect becomes even more significant as g_{m0} is increased through optimization of material growth and device fabrication process.

Although it is possible to extract the value of source resistance by using channel sheet resistance and contact resistance obtained from the TLM structure, this method requires precise knowledge of other parameters including the extrinsic source-gate (L_{sg}) spacing. A more accurate and direct method, called floating-drain technique, was used in this work. As shown in Figure 3.24, a positive gate current I_G is injected into the gate terminal with the drain terminal floating and the source terminal grounded, while measuring the resulting V_{DS}. The current passes through the channel and out of the source causing a resistive voltage drop $\frac{V_{DS}}{I_G}$. This value is the sum of R_s and an effective channel

resistance, R_{ch}. However, in a short gate device, R_{ch} can be decreased to a negligible fraction of R_s by increasing the channel charge with large forward V_{GS}, virtually equating $\frac{V_{DS}}{I_G}$ and R_s. There is one drawback to this technique, however. In order to get high enough signal-to-noise ratio in the measurement, a very large amount of current must be passed through the gate (typically around 100 mA/mm). Because of the low Schottky barrier height of $In_xAl_{1-x}As$, injection of that much current destroyed many gate structures. Due to this fact, source resistance could not be measured safely on all devices. Results summarized in Table 3.5 represent typical devices from each wafer with source-drain spacing of 2 μm. As was the case for contact resistance, source resistance did not seem to degrade for HEMT structures with higher AlAs mole fraction in the insulator.

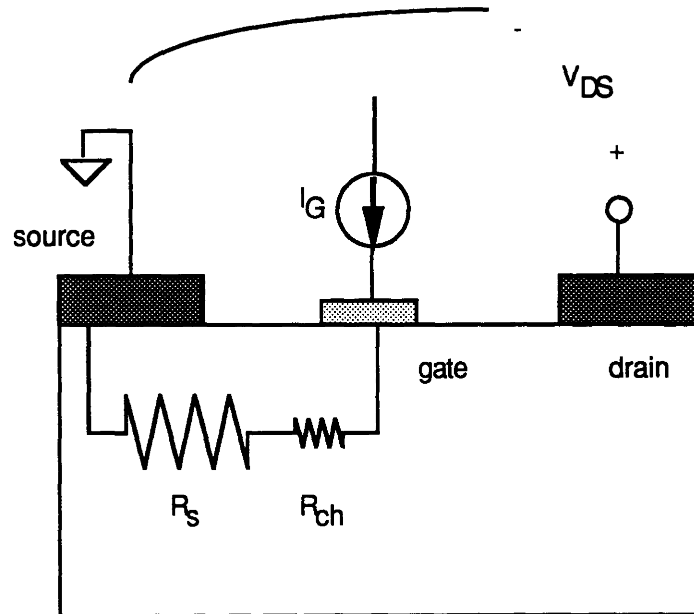

Figure 3.24: Schematic for source resistance measurement using floating-drain technique.

Table 3.5: Median values of source resistance.

	Q54-1	Q54-2	Q54-3	Q54-4
R_s (Ω mm)	0.45	0.52	0.43	0.43

Due to the problem mentioned above with floating-drain technique, source resistance was not measured for all devices. However, on-resistance was safe enough to measure on all devices. R_{on} was measured by calculating

$$R_{on} = \frac{V_{DS}}{I_D} \tag{3.3}$$

at $V_{DS} = 0.5$ V and $V_{GS} = 0.3$ V. Hence, on-resistance of a HEMT may be defined in the following manner:

$$R_{on} = R_s + R_d + 2R_{ch}. \tag{3.4}$$

Since R_{ch} is small compared to R_s, and R_d nominally equals R_s, R_{on} should have a similar functional dependence on L_{sd} as R_s.

Figure 3.25 shows that as the source-drain spacing increases, R_{on} increases as well. From this we may deduce that R_s is also proportional to the source-drain spacing. However, when transconductance is plotted against source-drain spacing in Figure 3.26, no clear degradation of g_m exists as the source-drain spacing increases. This apparent conflict with Equation (3.2) can be resolved by realizing that $R_s g_{m0}$ product is relatively small, around 0.18 for a typical device, so the source resistance does not exert much influence on the extrinsic transconductance. g_m of HEMTs studied in this work is limited by inefficient charge control, not by parasitic source resistance. For devices with higher intrinsic transconductance, however, one must be more concerned with source resistance and minimize its parasitic effect as much as possible.

3.4.3 Gate Resistance

As already explained in Section 2.3.3, gate length must be decreased in order to increase the high frequency performance of a HEMT. However, the decrease in gate length is necessarily accompanied by an increase in resistance along the width of the gate metal. T-gate process alleviates some of the

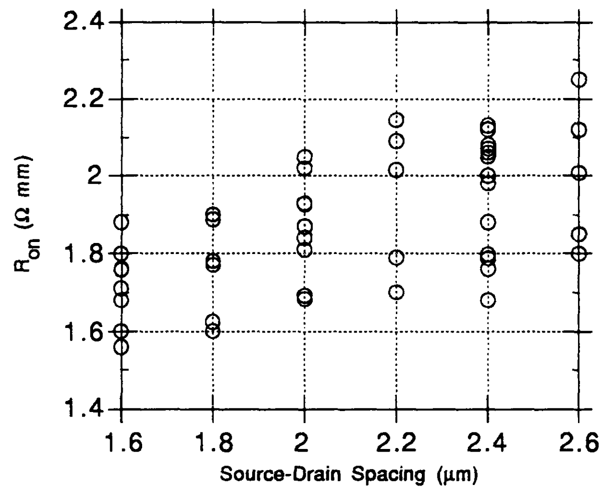

Figure 3.25: On-resistance of typical devices from all wafers versus source-drain spacing (post-passivation).

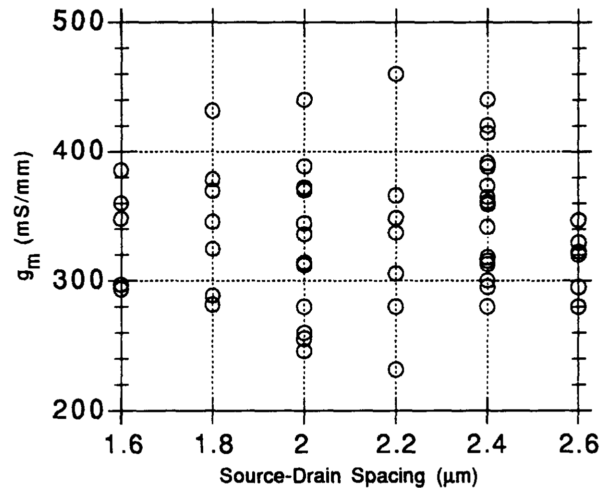

Figure 3.26: Peak transconductance of passivate devices versus source-drain spacing on wafer Q54-3.

detrimental effects of high resistance by increasing the cross-sectional area of the gate metal.

Gate resistance measurement can also be used to determine the gate length. Although the gate lengths of devices were processed to be the same for all wafers used in this work, a certain amount of uncertainty existed as the target

gate length approached 0.15 μm. Visual inspection was difficult due to top of the T-gate covering the footprint. Results in Table 3.6 revealed that the resistances were comparable, implying similar gate lengths for various devices across different wafers.

Table 3.6: Median values of R_g

	Q54-1	Q54-2	Q54-3	Q54-4
R_g (Ω/mm)	435	545	450	530

3.5 Effects of Passivation

Deposition of a dielectric passivation layer to encapsulate the surface of a HEMT is desirable for the following reasons:

1. A passivation layer protects delicate structures, especially the T-gate, from the environment.
2. A passivation layer may serve as a moisture barrier to repel water vapor and inhibit oxide formation on the surface.
3. A passivation layer may neutralize electronic states that may be present on the surface of a device thereby stabilizing the electrical properties of the device.
4. Previous experiments with passivation on MESFETs have shown that suitable passivation layer increases the long term reliability of devices especially during RF operations [67].

Based on the past success with Si_3N_4 passivation layer for GaAs-based PHEMTs, a similar process was used to study the effect of passivation on InP-based HEMTs. As described in Section 2.3.5, the wafers were coated with 700 Å of Si_3N_4 and were patterned to etch away the nitride from metal pads. Each of the four wafers exhibited very similar changes in device characteristics pre- and post-passivation. Therefore, data from only one wafer, a calibration wafer which had the same layer structure as wafer Q54-2, was used to study the effects of passivation.

As clearly seen in Figures 3.27-3.30, a large change in electrical characteristics of devices were observed after passivation. The median change of threshold voltage (ΔV_t) was +0.9 V or 34%. The saturated drain current was largely unchanged while peak transconductance increased about 11%, and BV_{DG} increased about 15%. Similar changes were observed in MESFETs and in GaAs-based HEMTs by Chang *et al.* although the magnitudes of changes were not as large [68], [69].

A major concern with any type of passivation process is the possible degradation of important FET parameters after deposition of the dielectric layer. While none of the four measured parameters degraded in this experiment, large changes, especially in threshold voltage, should generate question about the origins of these effects and about the ways to control them. Chang *et al.* concluded, at least for GaAs-based MESFETs and HEMTs, that changes in electrical characteristics are due to stress-induced piezoelectric charge distribution in the channel [68], [69]. The stress was attributed to the lattice constant difference between Si_3N_4 and the semiconductor. Using a very thin layer of Si_3N_4 may lessen the amount of stress, but nitride layers thinner than 500 Å have shown tendencies to develop pinholes through the layer, largely negating the benefits of passivation [70].

The physics at the surface has a large influence on the behavior of HEMTs. Surface atoms may have dangling bonds and form surface energy states which may act as hole or electron traps. Several studies have shown the presence of such surface states and traps in InP-based HEMTs [71], [72]. These surface states are responsible for Fermi level pinning which fixes the built-in surface potential, ψ_s, of a semiconductor. Other factors, including doping type and density, may also contribute to the effect. ψ_s is responsible for the depletion region that forms underneath the surface at zero bias.

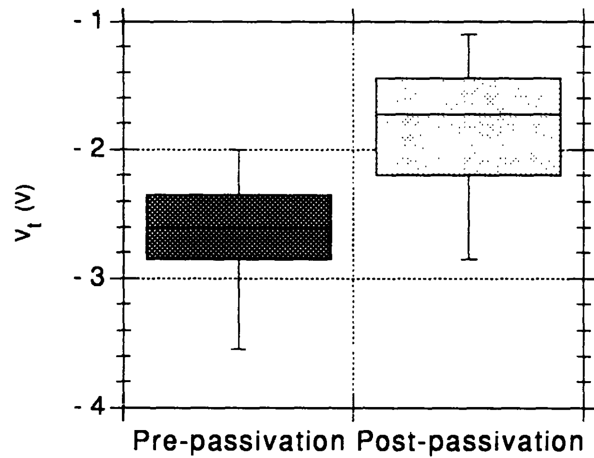

Figure 3.27: Comparison of threshold voltage.

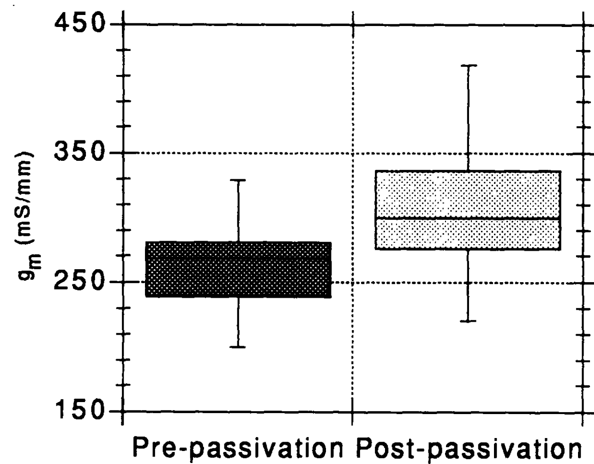

Figure 3.28: Comparison of peak transconductance.

A plausible argument for the positive shift in threshold voltage may be the following: deposition of Si_3N_4 may introduce more negative surface states to the surface of the $In_{0.53}Ga_{0.47}As$ cap layer, hence repelling away more electrons underneath the gate metal to form a larger depletion region. A less negative voltage at the gate electrode is then needed in order to fully deplete the channel

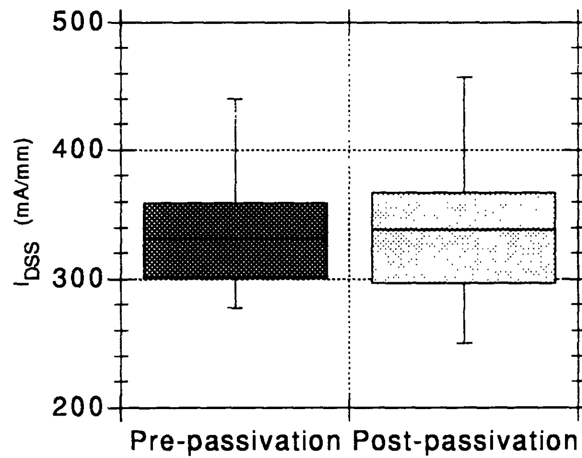

Figure 3.29: Comparison of saturated drain current.

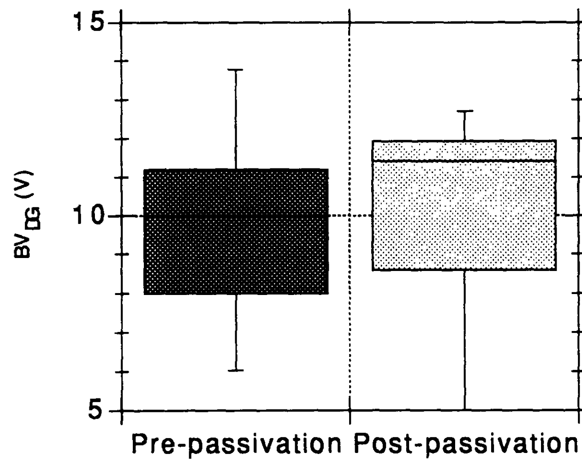

Figure 3.30: Comparison of two-terminal breakdown voltage.

and turn off the device. This process is plausible, but not enough information exists to conclusively prove this hypothesis.

In [68], the authors discovered that the positive change in threshold voltage increased dramatically as the gate length decreased. This effect can also be explained by the hypothesis above. Assuming that a fixed number of surface states exists, a larger percentage of the region underneath the gate is affected by

the surface states for a device with smaller gate length. Hence, surface states have more of an effect on the device and can cause a larger shift in the threshold voltage. The above reasoning may explain why ΔV_t in this work was so much larger than in [68], in which the shortest gate length studied was 0.5 μm.

Large influence of surface states on the device behavior may be explained by realizing that an undoped $In_{0.53}Ga_{0.47}As$ cap layer was used in this work. The phenomènon of "parasitic gating" has been observed in GaAs-based PHEMTs, in which surface states have a direct control over the channel region of the device due to the lack of electrons in the undoped cap layer [9]. Similar effects may have influenced the devices studied in this work.

3.6 Conclusions

Hall effect measurements revealed a decrease in sheet electron concentration for HEMT structures with high AlAs mole fraction Schottky barriers. This decrease in charge resulted in lower saturated channel current. However, peak transconductance did not change for different AlAs mole fraction insulators. The decrease in sheet electron concentration has been attributed to non-ideal conditions under which the pseudomorphic layers were grown. Neither temperature nor doping density was optimized for Al-rich InAlAs layers. As reported by Brown *et al.*, performance degrading effects due to dopant segregation and inactivation are expected to dramatically decrease as growth conditions are optimized for $In_xAl_{1-x}As$ layers with x less than 0.52 [42].

Forward turn-on voltage increased for HEMTs with high AlAs mole fraction Schottky barriers. This result is very promising because the gate terminal can be forward biased up to ~0.6 V without drawing a significant amount of gate current. This mode of operation may allow an optimized device to a carry greater amount of current in the channel.

Two-terminal gate-drain breakdown voltage increased for HEMTs with larger Schottky barrier heights and larger gate-drain spacings. Larger Schottky barrier height decreased the gate leakage current, and larger L_{gd} reduced the peak electric field near the gate contact, thus decreasing tunneling, thermionic emission, and impact ionization. Three-terminal breakdown voltages were not measured on most devices. However, improvement in BV_{DG} would likely enhance BV_{DS} as well.

The presence of impact ionization in the channel was verified by studying the gate leakage current. Both holes and electrons are created during impact ionization, but only holes are attracted to the gate terminal when it is negatively biased. The flow of holes to the gate terminal resulted in a "hump" in the gate current. The onset of impact ionization is widely believed to be the cause of source-drain breakdown, hence the process must be delayed in order to improve the breakdown voltage and thus the power performance of a HEMT.

RF characteristics of HEMTs with high AlAs mole fraction Schottky barriers were very encouraging. There were no significant degradation of important parameters as the AlAs mole fraction was increased. G_{max} at 18 GHz of all InP-based HEMTs fabricated in this work was higher than that of a state-of-the-art GaAs-based PHEMT. This confirms the potential for Q-, V-, and W-band operations of InP-based HEMTs.

Performance degrading effects of parasitic elements, including R_{SH}, R_C, and R_s, showed no sign of increase for devices with high AlAs mole fraction Schottky barriers. The focus of further research may be concentrated on improving the intrinsic performance of these devices rather than on minimizing the effects of parasitic elements.

Effects of Si_3N_4 passivation on InP-based HEMTs were studied. Changes in device parameters after passivation were very large. These changes were

partially attributed to stress cause by the dielectric film. Much more work is needed in order to develop a suitable passivation layer for InP-based HEMTs.

Chapter 4. Conclusions

4.1 Summary

$In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As/InP$ HEMTs with x ranging from 0.52 to 0.35 have been fabricated and characterized. The main motivation was to evaluate the power performance potential of InP-based HEMTs with pseudomorphic Schottky barriers. Improvements in BV_{DG} and V_{on} were observed for devices with higher AlAs mole fraction Schottky barriers. BV_{DS}, however, could not be measured on most devices due to the initiation of catastrophic burnouts.

RF measurements revealed the excellent potential for high frequency operation of InP-based HEMTs. Many key parameters, including f_T, f_{max}, C_{gs}, and C_{gd}, surpassed those of even the best GaAs-based PHEMTs. G_{max} at 18 GHz, in particular, was higher for all InP-based HEMTs fabricated in this work than for even the state-of-the-art GaAs-based power PHEMTs.

Evidence of impact ionization in the $In_{0.53}Ga_{0.47}As$ channel has been observed by monitoring the gate leakage current. This physical mechanism limits the source-drain breakdown voltage of InP-based HEMTs, hence it must be controlled.

Performance degradation due to parasitic elements did not change as the AlAs mole fraction of the Schottky barrier increased. However, saturated drain current decreased as the AlAs mole fraction increased. This behavior has been attributed to low sheet electron densities caused by silicon segregation and inactivation in HEMT structures with high AlAs mole fraction Schottky barriers.

4.2 Suggestions for Future Work

The following suggestions represent tasks which, for either lack of time or equipment, have not been accomplished in this work. They are not necessarily

the "correct" approaches to resolve all difficulties that exists in this field. Rather, they represent the author's understanding of the problems encountered during this study and possible solutions that may be utilized to overcome these problems.

Growth conditions must be optimized for pseudomorphic structures. The observed reduction in sheet electron concentration largely negates any benefits that may arise from having a larger Schottky barrier height. The conduction band discontinuity and sheet electron concentration may be increased without changing the $In_{0.53}Ga_{0.47}As$ channel by using a spacer layer also rich in Al.

Catastrophic burnout of devices must be controlled. As discussed in Section 3.2.5.2, improvements in E-beam lithography is needed to eliminate the jagged lines in the exposure pattern. Use of highly doped region beneath ohmic contacts may also help control the burnout.

Impact ionization in the channel must be reduced. Reducing the InAs mole fraction of $In_{0.53}Ga_{0.47}As$ may accomplish this feat, but it also degrades the transport characteristics. Enhancement in effective energy gap and breakdown voltage have been observed by introducing energy quantization by reducing the channel thickness to dimensions comparable to the electron wavelength [73]. However, increase in source resistance and contact resistance have been observed for thinner channels [73], [74]. Further work on ohmic contact technology is needed in order to solve this problem.

Better passivation process is needed in order to stabilize and protect the HEMTs. Stress induced by the dielectric layer may be responsible for large changes in device parameters. Much work is in progress here and elsewhere to reduce the induced stress.

APPENDIX A - LIST OF SYMBOLS

Symbol	Description
A^*	Effective Richardson constant [A cm^{-2} K^{-2}]
BV	Breakdown voltage [V]
BV_{DG}	Drain-gate breakdown voltage [V]
BV_{DS}	Drain-source breakdown voltage [V]
C_{gd}	Gate-to-drain capacitance [fF/mm]
C_{gs}	Gate-to-source capacitance [pF/mm]
E	Electric field [V/cm]
E_C	Conduction band [eV]
E_F	Fermi energy or Fermi level [eV]
E_G	Energy bandgap [eV]
E_V	Valence band [eV]
f	Frequency [GHz]
f_{max}	Unilateral power gain cutoff frequency [GHz]
f_T	Current gain cutoff frequency [GHz]
G	Power gain [dB]
g_m	Transconductance [mS/mm]
g_{m0}	Intrinsic transconductance [mS/mm]
G_{max}	Maximum available gain [dB]
g_o	Output conductance [mS/mm]
I_D	Drain current [mA/mm]
I_{Dmax}	Maximum drain current [mA/mm]
I_{Dmin}	Minimum drain current [mA/mm]
I_{DSS}	Saturated drain current [mA/mm]
I_G	Gate current [mA/mm]
I_{rms}	Root-mean-square current [mA/mm]
K	Boltzmann constant [eV/K]
L_g	Gate length [μm]
L_{gd}	Gate-drain spacing [μm]
L_s	Source inductance [pH/mm]
L_{sd}	Source-drain spacing [μm]
m^*	Carrier effective mass [kg]
n_S	Sheet carrier concentration [cm^{-2}]
P_{dc}	DC power [W/mm]
P_i	Input power [W/mm]
P_o	Output power [W/mm]
q	Electric charge [C]
R_C	Ohmic contact resistance [Ω mm]
R_{ch}	Channel resistance [Ω mm]
R_d	Drain resistance [Ω mm]
R_g	Gate resistance [Ω/mm]
R_i	Intrinsic resistance [Ω/mm]

R_L	Load resistor [Ω]
R_{on}	On resistance of an FET [Ω mm]
R_{opt}	Ideal (optimal) load resistor [Ω]
R_s	Source resistance [Ω mm]
R_{SH}	Channel sheet resistance [Ω/sq]
T	Temperature [K]
v	Carrier group velocity [cm/s]
V_{bi}	Built-in junction voltage [V]
v_d	Drift velocity [cm/s]
V_{DS}	Drain-to-source voltage [V]
V_{GS}	Gate-to-source voltage [V]
V_k	Knee voltage [V]
V_{on}	Schottky barrier forward turn-on voltage [V]
v_p	Peak velocity [cm/s]
V_{rms}	Root-mean-square voltage [V]
v_{sat}	Saturated velocity [cm/s]
V_t	Threshold voltage [V]
W	Device width [mm]
ε	Permittivity [F/cm]
ε_0	Free space permittivity [F/cm]
ϕ_B	Schottky barrier height [V]
Γ	Center of the Brillouin zone
μ_e	Electron mobility [$cm^2\ V^{-1}\ s^{-1}$]
ρ	Resistivity of the material [Ω cm]
σ	Conductivity [$\Omega^{-1}\ cm^{-1}$]
ψ_s	Built-in surface potential of semiconductor [eV]

APPENDIX B - THEORY OF THERMIONIC EMISSION

The following derivation of thermionic emission at metal-semiconductor junction is mainly from the work of Sze [75] who relied on the theory first proposed by Bethe [76]. Bethe's theory assumes that (1) the barrier height ϕ_B is much larger than kT/q, (2) thermal equilibrium is established at the metal-semiconductor junction, and (3) the existence of a net current flow does not affect this equilibrium. Because of these assumptions, the shape of the barrier is immaterial, and only the barrier height determines the current flow. The current density $J_{s \to m}$ from the semiconductor to metal is given by the concentration of electrons traversing in the x direction with sufficient energy to overcome the potential barrier:

$$J_{s \to m} = \int_{E_F + q\phi_B}^{\infty} q v_x \, dn \tag{B1}$$

where $E_F + q\phi_B$ is the minimum energy required for thermionic emission into the metal, and v_x is the electron velocity in the direction of transport. The incremental electron density is given by

$$\begin{aligned} dn &= N(E)F(E)dE \\ &= \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E - E_C}\,\exp[-(E - E_C + qV_n)/kT]dE \end{aligned} \tag{B2}$$

where $N(E)$ is the density of states, $F(E)$ is the distribution function, m^* is the effective mass, and qV_n equals $(E_C - E_F)$.

Assuming that all the energy of an electron in the conduction band is in the form of kinetic energy, one may then write

$$E - E_C = \frac{1}{2} m^* v^2 \tag{B3}$$

$$dE = m^* v dv \tag{B4}$$

$$\sqrt{E - E_C} = v\sqrt{m^*/2}. \tag{B5}$$

Substituting Equations (B3)-(B5) into Equation (B2) gives

$$dn = 2\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{qV_n}{kT}\right) \exp\left(-\frac{m^* v^2}{2kT}\right)(4\pi v^2 dv). \tag{B6}$$

Equation (B6) gives the number of electrons per unit volume that have speeds between v and $v+dv$ distributed in all directions. Resolving the speed into different directions, one gets the vector sum

$$v^2 = v_x^2 + v_y^2 + v_z^2. \tag{B7}$$

With the transformation $4\pi v^2 dv = dv_x dv_y dv_z$, Equations (B1), (B6), and (B7) become

$$J_{s \to m} = 2q\left(\frac{m^*}{h}\right)^3 \exp(-qV_n / kT)$$

$$\int_{v_{0x}}^{\infty} v_x \exp(-m^* v_x^2 / 2kT) dv_x \int_{-\infty}^{\infty} \exp(-m^* v_y^2 / 2kT) dv_y$$

$$\int_{-\infty}^{\infty} \exp(-m^* v_z^2 / 2kT) dv_z$$

$$= \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp(-qV_n / kT) \exp\left(-\frac{m^* v_{0x}^2}{2kT}\right). \tag{B8}$$

v_{0x} is the minimum velocity required in the x direction to overcome the barrier and is given by

$$\frac{1}{2} m^* v_{0x}^2 = q(V_{bi} - V_A) \tag{B9}$$

where V_{bi} is the built-in potential at zero bias, and V_A is the applied voltage. Substituting Equation (B9) into Equation (B8) yields

$$J_{s\to m} = \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp\left[-\frac{q(V_n + V_{bi})}{kT}\right] \exp\left(\frac{qV_A}{kT}\right)$$

$$= A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \exp\left(\frac{qV_A}{kT}\right) \qquad \text{(B10)}$$

where ϕ_B equals the sum of V_n and V_{bi}, and

$$A^* = \frac{4\pi q m^* k^2}{h^3} \qquad \text{(B11)}$$

is the effective Richardson constant for thermionic emission, neglecting the effects of optical phonon scattering and quantum mechanical reflection. When the image force lowering is considered, the barrier height ϕ_B in Equation (B10) is reduced by $\Delta\phi_B$.

Since the barrier height for electrons moving from the metal into the semiconductor remains the same, the current flowing into the semiconductor is thus unaffected by the applied voltage. It must therefore be equal to the current flowing from the semiconductor into the metal when $V_A = 0$. Hence,

$$J_{m\to s} = -A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right). \qquad \text{(B12)}$$

The total current density is then given by the sum of Equations (B10) and (B12).

$$J_n = \left[A^* T^2 \exp\left(\frac{q\phi_B}{kT}\right)\right]\left[\exp\left(\frac{qV_A}{kT}\right) - 1\right]$$

$$= J_{ST}\left[\exp\left(\frac{qV_A}{kT}\right) - 1\right] \qquad \text{(B13)}$$

where

$$J_{ST} \equiv A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right). \qquad \text{(B14)}$$

The amount of current flowing across a metal-semiconductor junction due to thermionic emission is an exponential function of both the applied voltage and the Schottky barrier height.

REFERENCES

[1] R. Dingle, H. L. Stormer, A. C. Gossard, and W. Wiegmann, "Electron mobilities in modulation-doped semiconductor heterojunction superlattices," *Applied Physics Letters*, 33 (7), pp. 665-667, July 1978.

[2] K. L. Tan, R. M. Dia, D. C. Streit, T. Lin, T. Q. Trinh, A. C. Han, P. M. D. Chow, and H. C. Yen, "94 GHz 0.1-μm T-gate low-noise pseudomorphic InGaAs HEMT's," *IEEE Electron Device Letters*, vol. 11, pp. 585-587, Dec. 1990.

[3] K. L. Tan, R. M. Dia, D. C. Streit, L. K. Shaw, A. C. Han, M. D. Sholley, P. H. Liu, T. Q. Trinh, T. Lin, and H. C. Yen, "60-GHz pseudomorphic $Al_{0.25}Ga_{0.75}As$/ $In_{0.28}Ga_{0.72}As$ low-noise HEMT's," *IEEE Trans. Electron Devices*, vol. 12, pp. 23-25, Jan. 1991.

[4] K. H. G. Duh, P. C. Chao, P. Ho, A. Tessmer, S. M. J. Liu, M. Y. Kao, P. M. Smith, and J. M. Ballingall, "W-band InGaAs HEMT low noise amplifier," in *IEEE MTT-S Symp. Digest*, p. 595, 1990.

[5] A. W. Swanson, P. M. Smith, P. C. Chao, K. H. Duh, and Ballingall, "mm-wave HEMT technology," in *IEEE MILCOM Conference Digest*, pp. 745-748, Oct. 1989.

[6] P. C. Chao, A. J. Tessmer, K. H. G. Duh, P. Ho, M. Y. Kao, P. M. Smith, J. M. Ballingall, S. M. J. Liu, and A. A. Jabra, "W-band low noise InAlAs/InGaAs lattice-matched HEMTs," *IEEE Electron Device Letters*, vol. 11, no. 1, pp. 59-62, Jan. 1990.

[7] N. Moll, "HFETs: A study in developmental device physics," in *Compound Semiconductor Transistors: Physics and Technology*, Sandip Tiwari, Ed. Piscataway, NJ: IEEE Press, pp. 3-20, 1993.

[8] T. Henderson, M. Aksun, C. Peng, H. Morkoç, P. C. Chao, P. M. Smith, K. H. G. Duh, and L. Lester, "Power and noise performance of the pseudomorphic MODFET at 60 GHz," in *1986 IEDM Tech. Digest*, pp. 464-466, 1986.

[9] J. C. Huang, G. Jackson, S. Shanfield, W. Hoke, P. Lyman, D. Atwood, P. Saledas, M. Schindler, Y. Tajima, A. Platzker, D. Massé, and H. Statz, "An AlGaAs/ InGaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) For *X*- and *Ku*-band Power Applications," in *IEEE MTT-S Symp. Digest*, pp. 713-716, 1991.

[10] U. K. Mishra, A. S. Brown, L. M. Jelloian, M. Thompson, L. D. Nguyen, and S. E. Rosenbaum, "Novel high performance self-aligned 0.15 micron long T-gate AlInAs-GaInAs HEMTs," in *IEDM Tech. Digest*, pp. 101-104, 1989.

[11] P. Ho, M. Y. Kao, P. C. Chao, K. H. G. Duh, J. M. Ballingall, S. T. Allen, A. J. Tessmer, and P. M. Smith, "Extremely high gain 0.15 μm gate-length InAlAs/

InGaAs/InP HEMTs," *Electronics Letters*, vol. 27, no. 4, pp. 325-327, 14th Feb. 1991.

[12] G. I. Ng, D. Pavlidis, M. Jaffe, J. Singh, and H. F. Chau, "Design and experimental characteristics of strained $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x > 0.53$) HEMTs," *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2249-2259, Oct. 1989.

[13] L. D. Nguyen, L. E. Larson, and U. K. Mishra, "Ultra-high-speed modulation-doped field-effect transistors: a tutorial review," *Proc. of the IEEE*, vol. 80, no. 4, pp. 494-518, Apr. 1992.

[14] H. Ohno and J. Barnard, "Field-effect transistors," in *GaInAsP Alloy Semiconductors*, T. P. Pearsall, Ed. New York: Wiley, ch 17, 1982.

[15] W. Kowalski and A. Schlachetzki, "Transferred-Electron Effects in InGaAsP Alloys Lattice-Matched to InP," *Solid-State Electronics 28*, pp. 299-305, 1985.

[16] J. C. Bean, "Materials and Technologies," in *High-Speed Semiconductor Devices*, S. M. Sze, Ed. New York: John Wiley & Sons, Inc., ch 1, 1990.

[17] W. Both, V. Gottschalch, and G. Wagner, *Crystal Res. Technol.* 21, p. K85, 1986.

[18] C. K. Peng, S. Sinha, and H. Morkoç, "Characterization of graded interface $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ ($0.53 < x < 0.70$) structures grown by molecular-beam epitaxy," *Journal of Applied Physics*, 62 (7), pp. 2880-2884, Oct. 1987.

[19] M. Y. Kao, P. M. Smith, P. C. Chao, and P. Ho, "Millimeter wave power performance of InAlAs/InGaAs/InP HEMTs," in *Proc. IEEE/Cornell Conf. on High Speed Semiconductor Devices and Circuits*, pp. 469-477, 1991.

[20] J. J. Brown, A. S. Brown, S. E. Rosenbaum, A. S. Schmitz, M. Matloubian, L. E. Larson, M. A. Melendes, and M. A. Thompson, "Study of the Dependence of $Ga_{0.47}In_{0.53}As/Al_xIn_{1-x}As$ Power HEMT Breakdown Voltage on Schottky Layer Design and Device Layout," in *Device Research Conference Digest*, 1993.

[21] J. Dickmann, K. Riepe, H. Daembkes, and H. Künzel, "AlInAs/GaInAs Pseudomorphic HEMTs: Design and Performances," in *Fifth International Conference on InP and Related Materials*, pp. 461-464, 1993.

[22] S. R. Bahl and J. A. del Alamo, "Physics of breakdown in InAlAs/n^+-InGaAs Heterostructure Field-Effect Transistors," in *Fifth International Conference on InP and Related Materials*, pp. 243-246, 1993.

[23] D. K. Gaskill, N. Bottka, L Aina, and M. Mattingly, "Band-gap determination by photoreflectance of InGaAs and InAlAs lattice matched to InP," *Applied Physics Letters*, 56 (13), pp. 1269-1271, 26 Mar. 1990.

[24] S. Adachi, "Material parameters of $In_{1-x}Ga_xAs_yP_{1-y}$ and related binaries," *Journal of Applied Physics*, 53, pp. 8775-8792, 1982.

[25] M. Matloubian, L. D. Nguyen, A. S. Brown, L. E. Larson, M. A. Melendes, and M. A. Thompson, "High power and high efficiency AlInAs/GaInAs on InP HEMTs," in *IEEE MTT-S Symp. Digest*, pp. 721-724, 1991.

[26] P. Chu, C. L. Lin, H. H. Wieder, "Schottky-Barrier Height of $In_{0.43}Al_{0.57}As$," *Electronics Letters*, vol. 22, no. 17, pp. 890-892, 14th Aug. 1986.

[27] K. Imanish, *et al., Inst. Phys. Conf. Ser. No. 106*, pp. 637-640, 1990,

[28] C. L. Lin, P. Chu, A. L. Kellner, and H. H. Wieder, "Composition dependence of $Au/In_xAl_{1-x}As$ Schottky barrier heights," *Applied Physics Letters*, 49 (23), 8 Dec. 1986.

[29] K. Imanishi, T. Nishikawa, and K. Kondo, "$N\text{-}In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ pseudomorphic selectively doped heterostructures with improved Schottky characteristics," in *GaAs and Related Compounds*, pp. 637-640, 1989.

[30] P. C. Chao, A. J. Tessmer, M. Y. Kao, K. H. G. Duh, P. Ho, H. M. Smith, J. M. Ballingall, S. M. J. Liu, and A. A. Jabra, "V- and W-band low-noise InAlAs/InGaAs/InP HEMTs and amplifiers," *SPIE Vol. 1288 High-Speed Electronics and Device Scaling*, pp. 2-8, 1990.

[31] S. Fujita, S. Naritsuka, T. Noda, A. Wagai, and Y. Ashizawa, "Barrier Height Lowering of Schottky Contacts on AlInAs Layers Grown by Metal-Organic Chemical-Vapor Deposition," *Journal of Applied Physics*, 73 (3), pp. 1284-1287, 1 Feb. 1993.

[32] J. H. Van der Merwe, "Crystal interfaces: Part I, Semi-infinite crystals," *Journal of Applied Physics*, 34 (1), pp. 1117-112, 1963.

[33] J. W. Matthews, "Misfit dislocations," in *Dislocations in Solids*, vol. 2, F. R. N. Nabarro, Ed. Amsterdam: North Holland, pp. 461-545, ch. 7, 1979.

[34] F. N. R. Nabarro, *Theory of Crystal Dislocations*. New York: Clarendon, 1967.

[35] B. R. Bennet and J. A. del Alamo, "Mismatched InGaAs/InP and InAlAs/InP heterostructures with high crystalline quality," *Journal of Applied Physics*, 73 (7), pp. 3195-3202, 1 Apr. 1993.

[36] S. R. Bahl, W. J. Azzam, and J. A. del Alamo, "Strained-Insulator $In_xAl_{1-x}As/n^+\text{-}In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 38, no. 9, pp. 1986-1992, Sep. 1991.

[37] L. D. Nguyen, A. S. Brown, M. A. Thompson, L. M. Jelloian, L. E. Larson, and M. Matloubian, "650 Å Self-Aligned-Gate Pseudomorphic $Al_{0.48}In_{0.52}As$/ $Ga_{0.20}In_{0.80}As$ High Electron Mobility Transistors," *IEEE Electron Device Letters*, vol. 13, no. 3, pp. 143-145, Mar. 1993.

[38] K. B. Chough, W. P. Hong, P. S. D. Lin, C. Caneau, and J. I. Song, "MOCVD-Grown InAlAs/InGaAs HEMTs with $f_T = 200$ GHz," *Electronics Letters*, vol. 29, no. 15, pp. 1361-1363, 22nd July 1993.

[39] N. Pan, J. Carter, J. Elliot, H. Hendriks, S. Brierley, and K. C. Hsieh, "Low Temperature InAlAs Buffer Layers using Trimethylarsenic and Arsine by Metalorganic Chemical Vapor Deposition," *Applied Physics Letters*, 63 (220), pp. 3029-3031, 29 Nov. 1993.

[40] N. Pan, J. Elliot, J. Carter, H. Hendriks, and L. Aucoin, "Growth of InAlAs/ InGaAs Modulation Doped Structures on Low Temperature InAlAs Buffer Layers using Trimethylarsenic and Arsine by Metalorganic Chemical Vapor Deposition," in *GaAs and Related Compounds*, 1993.

[41] W. Shockley, "Research and Investigation of Inverse Epitaxial UHF Power Transistors," *Report No. Al-TOR-64-207*, Air Force Atomic Laboratory, Wright-Patterson Air Force Base, Ohio, Sep. 1964.

[42] A. S. Brown, J. Brown, J. A. Henige, R. G. Wilson, R. A. Metzger, M. A. Melendes, M. Matloubian, L. Jelloian, and L. E. Larson, "The Growth of High Performance GaInAs-$Al_xIn_{1-x}As$ Power HEMT Devices by MBE: Si Segregation and Activation, and Strained Layer Structural Quality," in *Electronic Materials Conference*, 1993.

[43] J. C. Huang, P. Saledas, J. Wendler, A. Platzker, W. Boulais, S. Shanfield, W. Hoke, P. Lyman, L. Aucoin, A. Miquelarena, C. Bedard, and D. Atwood, "A Double-Recessed $Al_{0.24}GaAs/In_{0.16}GaAs$ Pseudomorphic HEMT for *Ka*- and *Q*-Band Power Applications," *IEEE Electron Device Letters*, vol. 14, no. 9, pp. 456-458, Sep. 1993.

[44] M. Tong, K. Nummila, A. Ketterson, I. Adesida, C. Caneau, and R. Bhat, "InAlAs/InGaAs/InP MODFET's with Uniform Threshold Voltage Obtained by Selective Wet Gate Recess," *IEEE Electron Device Letters*, vol. 13, no. 10, pp. 525-527, Oct. 1992.

[45] A. S. Brown, U. K. Mishra, L. E. Larson, and S. E. Rosenbaum, "The elimination of dc I-V anomalies in $Ga_{0.47}In_{0.53}As$-$Al_{0.48}In_{0.52}As$ HEMTs," in *GaAs and Related Compounds*, pp. 445-448, 1988.

[46] L. F. Palmateer, P. J. Tasker, W. J. Schaff, L. D. Nguyen, and L. F. Eastman, "dc and rf measurements of the kink effect in 0.2 μm gate length AlInAs/GaInAs/ InP modulation-doped field-effect transistors," *Applied Physics Letters*, 54 (21), 22, pp. 2139-2141, May 1989.

[47] S. R. Bahl, J. A. del Alamo, J. Dickmann, and S. Schildberg, "Physics of Breakdown in InAlAs/InGaAs MODFETs," in *Device Research Conference Digest*, 1993.

[48] J. B. Shealy, M. M. Hashemi, S. P. DenBaars, U. K. Mishra, T. K. Liu, J. J. Brown, and M. Lui, "Breakdown Characterization of AlInAs/GaInAs Junction Modulated HEMTs (JHEMTs) with Regrown Ohmic Contacts by MOCVD," in *Proc. IEEE/Cornell Conf. on High Speed Semiconductor Devices and Circuits*, pp. 548-556, 1993.

[49] K. Hikosaka, Y. Hirachi, and M. Abe, "Microwave power double-heterojunction HEMTs," *IEEE Trans. Electron Devices*, vol. ED-33, no. 5, pp. 583-589, 1986.

[50] R. J. Trew and U. K. Mishra, "Gate breakdown in MESFETs and HEMTs," *IEEE Electron Device Letters*, vol. 12, no. 10, pp. 524-526, Oct. 1991.

[51] S. H. Wemple, W. C. Niehaus, H. M. Cox, J. V. Dilorenzo, and W. O. Schlosser, "Control of Gate-Drain Avalanche in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-27, no. 6, pp. 1013-1018, June 1980.

[52] Y. Wada and M. Tomizawa, "Drain Avalanche Breakdown in Gallium Arsenide MESFET's," *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1765-1770, Nov. 1988.

[53] R. Wroblewski, G. Salmer, and Uves Crosnier, "Theoretical Analysis of the DC Avalanche Breakdown in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-30, no. 2, pp. 154-159, Feb. 1983.

[54] W. R. Frensley, "Power-Limiting Breakdown Effects in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-38, no. 8, pp. 962-970, Aug. 1981.

[55] H. Chau, D. Pavlidis, and K. Tomizawa, "Theoretical Analysis of HEMT Breakdown Dependence on Device Design Parameters," IEEE Trans. Electron Devices, vol. 38, no. 2, pp. 213-221, Feb. 1991.

[56] S. M. Sze, "Physics of Semiconductor Devices," New York: John Wiley & Sons, Inc., ch 7, 1981.

[57] S. R. Bahl and J. A. del Alamo, "A New Drain-Current Injection Technique for the Measurement of Off-State Breakdown Voltage in FET's," *IEEE Trans. Electron Devices*, vol. 40, no. 8, pp. 1558-1560, Aug. 1993.

[58] T. Furutsuka, T. Tsuji, and F. Hasegawa, "Improvement of the Drain Breakdown Voltage of GaAs Power MESFET's by a Simple Recess Structure," *IEEE Trans. Electron Devices*, vol. ED-25, no. 6, pp. 563-567, June 1978.

[59] S. H. Wemple and W. C. Niehaus, "Source-Drain Burn-out in GaAs MESFETs," *Inst. Physics Conference Series*, no. 33b, pp. 262-270, 1977.

[60] S. H. Wemple, W. C. Niehaus, H. Fukui, J. C. Irvin, H. M. Cox, J. C. M. Hwang, J. V. DiLorenzo, and W. O. Schlosser, "Long-Term and Instantaneous Burnout in GaAs Power FET's: Mechanisms and Solutions," *IEEE Trans. Electron Devices*, vol. ED-28, no. 7, July 1981.

[61] S. M. Sze, "Physics of Semiconductor Devices," New York: John Wiley & Sons, Inc., ch 1, 1981.

[62] C. Heedt, F. Buchali, W. Prost, D. Fritsche, H. Nickel, and F. J. Tegude, "Characterization of Impact-Ionization in InAlAs/InGaAs/InP HEMT Structures Using a Novel Photocurrent-Measurement Technique," in *Fifth International Conference on InP and Related Materials*, pp. 247-250, 1993.

[63] L. D. Nguyen, L. M. Jollian, M. Thompson, and M. Lui, "Fabrication of a 80-nm self-aligned T-gate AlInAs/GaInAs HEMT," in *IEDM Tech. Digest*, Dec. 1990.

[64] A. A. Ketterson, J. Laskar, T. L. Brock, I. Adesida, J. Kolodzey, O. A. Aina, and H. Hier, "DC and RF Characterizations of Short-Gate-Length InGaAs/InAlAs MODFET's," *IEEE Trans. Electron Devices*, vol. 36, no. 10, Oct. 1989.

[65] F. Ponse, W. T. Masselink, and H. Morkoç, "Quasi-Fermi Level Bending in MODFET's and Its Effect on FET Transfer Characteristics," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1017-1023, June 1985.

[66] J. C. Huang, G. S. Jackson, S. Shanfield, A. Platzker, P. K. Saledas, and C. Weichert, "An AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistor With Improved Breakdown Voltage for *X*- and *Ku*-Band Power Applications," *IEEE Trans. MTT*, vol. 41, no. 5, May 1993.

[67] J. G. Tenedorio and P. A. Terizian, "Effects of Si_3N_4, SiO, and Polyimide Surface Passivation on GaAs MESFET Amplifier RF Stability," *IEEE Electron Device Letters*, vol. 5, no. 6, pp. 199-202, 1984.

[68] E. Y. Chang, G. T. Cibuzar, J. M. Vanhove, R. M. Nagarajan, and K. P. Pande, "GaAs Device Passivation Using Sputtered Silicon Nitride," *Applied Physics Letters*, 53 (17), pp. 1638-1640, 24 Oct. 1988.

[69] E. Y. Chang, G. T. Cibuzar, and K. P. Pande, "Passivation of GaAs FET's with PECVD Silicon Nitride Films of Different Stress States," *IEEE Trans. Electron Devices*, vol. 35, no. 9, Sep. 1988.

[70] L. Aucoin, private communication, Oct. 1993.

[71] G. I. Ng and D. Pavlidis, "Frequency-Dependent Characteristics and Trap Studies of Lattice-Matched (x = 0.53) and Strained (x > 0.53) $In_{0.52}Al_{0.48}As$/

$In_xGa_{1-x}As$ HEMTs," *IEEE Trans. Electron Devices*, vol. ED-38, no. 4, pp. 826-870. Apr. 1991.

[72] W. Kruppa and J. B. Boos, "Sinusoidal and Transient Response of Traps in Double-Recessed InAlAs/InGaAs/InP HEMTs," in *Fifth International Conference on InP and Related Materials*, pp. 251-254, 1993.

[73] S. R. Bahl and J. A. del Alamo, "Breakdown Voltage Enhancement from Channel Quantization in InAlAs/n^+-InGaAs HFET's," *IEEE Electron Device Letters*, vol. 13, no. 2, pp. 123-125, Feb. 1992.

[74] K. Hur, private communication, Jan. 1994.

[75] S. M. Sze, "Physics of Semiconductor Devices," New York: John Wiley & Sons, Inc., ch 5, 1981.

[76] H. A. Bethe, "Theory of the Boundary Layer of Crystal Rectifiers," *MIT Radiation Laboratory Report 433-12*, 1942.