Modeling for Hot-Electron Reliability Simulation

by

Jeffery Seokwon Kim

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degrees of

Bachelor of Science in Electrical Science and Engineering

and

Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 1995

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Abstract

In order to study the hot-electron degradation parameters **n**, **m**, and **H**, whose accurate extraction is critical in simulating circuit-level hot-electron degradation, both N-MOSFETs and P-MOSFETs have been fabricated with the shortest channel length of 0.25 μm. Processing techniques, such as an over-exposure and a short drive-in at high temperature, are used in order to fabricate short channel devices with shallow junctions, using a standard ultraviolet lithography system. A thorough characterization of hot-electron degradation parameters is presented, and physical explanations are given for the degradation parameters' dependencies on various MOSFET parameters, such as T_{ox} and N_{sub}, stressing conditions, such as E_{ox} and V_{sub}, and degradation mechanisms, such as interface-state generation and charge trapping. Several existing physical theories are explored and explained in further detail. Future research plans are presented in order to accomplish the goal of developing an optimal degradation parameter extraction guideline for hot-electron circuit performance degradation simulation.

Thesis Supervisor: James E. Chung
Title : Assistant Professor of Electrical Engineering

Acknowledgment

My Lord, I give my sincere thanks and praise to you from the most bottom of my heart for having lead my study and life for the past five and a half years here at M.I.T. I bring all the glory to you alone. Although my life has been hard and frustrating at times from both my academic and personal problems, you have been always present with me with constant inspiration and encouragement. I am very grateful for your help and grace and also for an opportunity to study and research at one of the finest universities in the world.

Lord, I am most thankful for my wonderful family, who has helped me physically and spiritually through constant prayer. My mother Jong-Rea Eun and my father Sam-Kyun Kim have encouraged and helped me all the time whether I was well or not well. Without their support, my study would not have been possible. My Lord, I ask you for your special blessings on them. I also give my sincere thanks to my brother Seok-Young Kim and my sister Jin Kim who have provided me with their valuable opinions in making numerous important decisions in both my academic and personal life. Again, I ask for your blessings on them.

Heavenly Father, my sincere gratitude also goes to my thesis supervisor Professor James E. Chung, who has been patiently teaching and guiding me through my research. He was more encouraging than scolding when I could not deliver the research results well. I sincerely thank him for his patience and help, and, again, I ask you Lord to be with him all the time so that he can feel and realize your presence with him and thank you for your graceful salvation.

My God, I am also grateful to many of my fellow students and friends: Vei-han Chan, who has helped and advised me with his technical knowledge, Lisa Su, who has lent me her lithography masks to fabricate my devices, Jee-hoon Yap, Tinaung Daniel Maung, Eric Chang, Huy Le, Jocelyn Nee, Wenjie Jiang, Jung-Wook Yoon, and Andy Tang who have made my study here more pleasant. Lord, I pray to you to reveal yourself and personally meet those who do not know you so that they can also accept your wonderful salvation and can live in constant joy.

My special thanks go to some of my brothers and sisters in Christ: Folusho Oyerokun, who has inspired and prayed with me by sharing his faith, hope, and love, Jeom-Nye Yee, who has been to me like my real sister since I have known her, Pyoung-Won Yim, Kyoung-Chae Kye, Ko-Woon Yang and In-Kye Lee, who have been my true comfort. Lord, please bless them as much as you have blessed me.

My Heavenly Father, I thank you again for everything you have done for me, and pray all of the above in the name of our victorious Savior Jesus Christ. Amen.

Twenty-fifth day of January in year nineteen hundred ninety-five

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Introduction

1.1 Hot-electron Phenomenon

1.1.1 Overview

Hot-electrons are produced in the MOSFET by a high lateral electric field near the drain. Recently, as the channel length of the MOSFET is reduced to the submicron level while keeping the power supply voltage the same, the lateral electric field along the channel of the MOSFET has increased. This increased electric field accelerates the channel electrons, increasing their energy, and the accelerated electrons' effective temperature becomes higher than that of the surrounding silicon lattice. Thus, these electrons are called **hot-electrons**. The generation of hot-electrons is shown in Figure 1.1.

There are numerous problems that are direct results of hot-electrons. As the hot-electrons' effective temperature becomes high, they gain high enough energy to cross over the energy barrier between the Si and SiO_2. When the hot-electrons cross over the Si-SiO_2 interface, they break the Si-H bonds at the interface and create interface-traps. This phenomenon is shown in Figure 1.2. As a result of these interface-traps, the MOSFET's characteristics change. For example, in the case of an N-MOSFET, the threshold

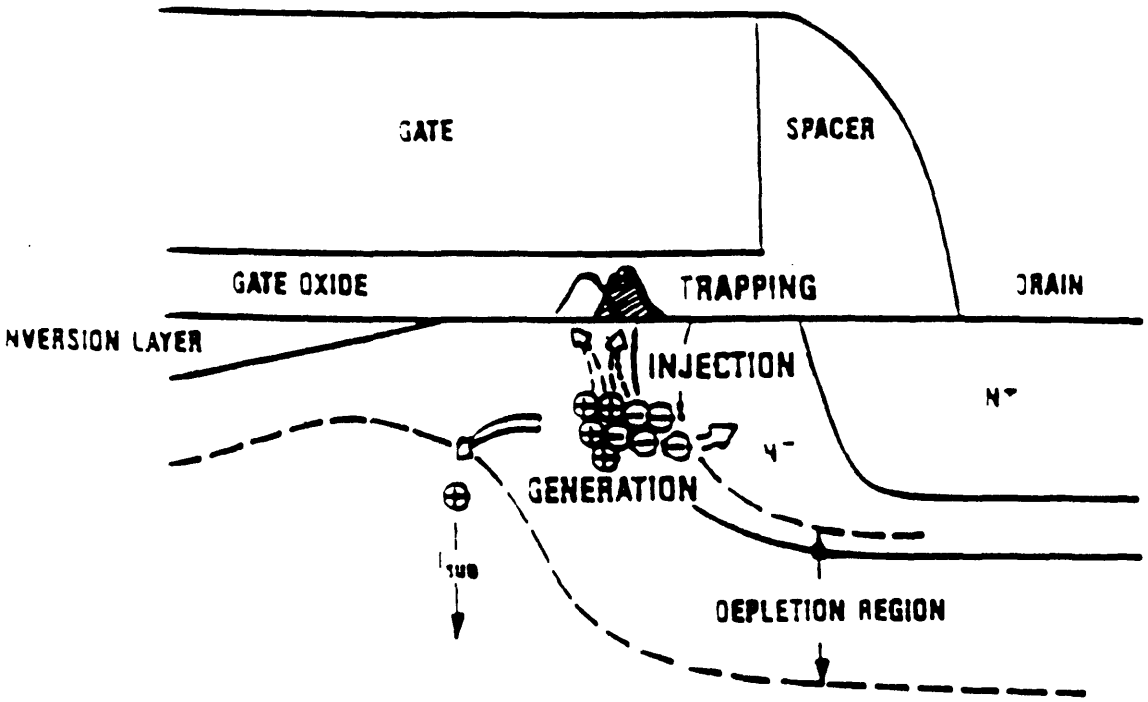

Figure 1.1 Hot-electron generation [1]

voltage(V_T) increases due to the negative charge at the Si-SiO_2. As the V_T increases, the drain current (I_D) decreases, and the transconductance(G_m) also decreases. In general, the performance of the MOSFET degrades. This effect is called **hot-electron degradation.**

1.1.2 Background

The fabrication technology of MOSFETs has been improving rapidly since the introduction of the first working device about 30 years ago[2]. Today, integrating more than 64 million MOSFETs on a silicon substrate as small as 1 $inch^2$ has become successful. The feature sizes of ULSI MOSFETs have been continuously scaled down to produce higher yields at lower costs, allow more circuit functions per chip, and improve device and circuit performance through higher speed and lower power consumption. At

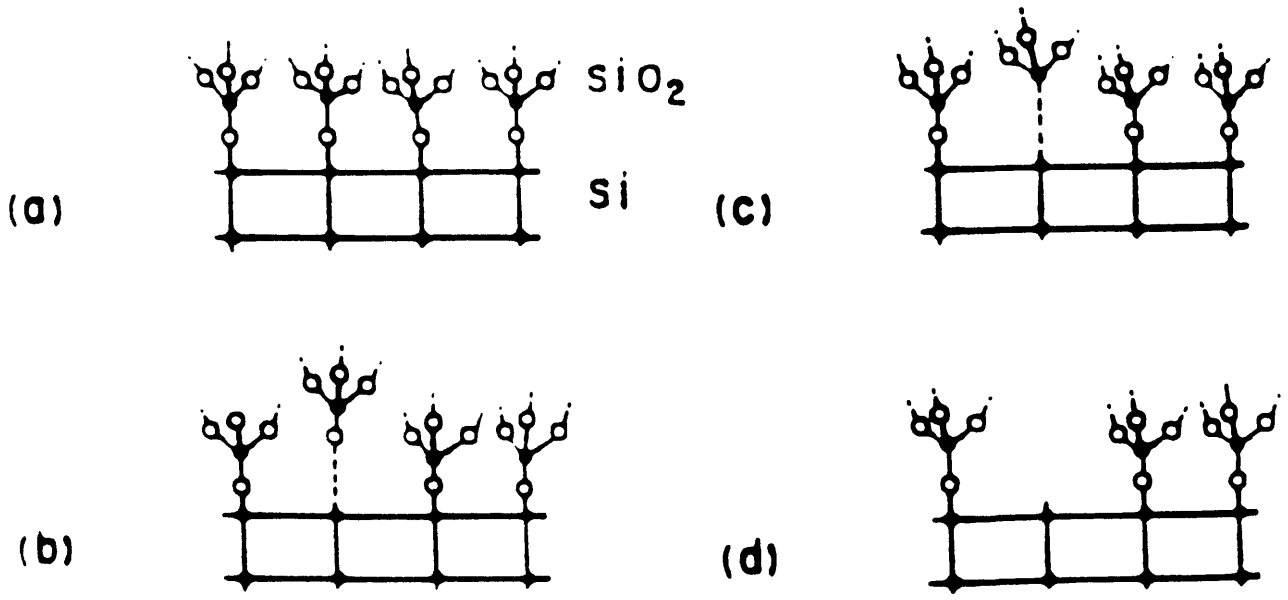

Figure 1.2 Possible interface-traps: (a) silicon lattice and perfect SiO2 overlayer; (b) stretched Si-O2 bond; (c) stretched Si-Si bond or oxygen vacancy; (d) silicon dangling bond [3]

the same time, there have been efforts to maintain the same power supply voltage for system compatibility with other existing integrated circuits.

Scaled-down devices have shorter channel lengths, shallower junction depths, and thinner gate oxides. Currently, the channel length goes down to as small as 0.1 μm, the junction depth to 50 nm, and the gate oxide thickness to 5 nm, using SOI(silicon-on-insulator) technology[4].

It is projected that commercially productive MOSFET's feature sizes for memory circuits will go down to as small as 0.09 μm in channel length, 70 nm in junction depth, and 4 nm in the gate oxide thickness by year 2007, using conventional bulk technology[5].

These scalings are necessary to provide more current drive while maintaining the correct device threshold voltage and off-state current. But since the power supply voltage

remains the same due to system requirements, the same voltage is now applied across a shorter channel, hence the resultant electric field is much higher. In addition, the shallower junction and thinner gate oxide also increase the electric field at the drain junction.

In N-MOSFETs, the channel electrons are accelerated by the high drain electric field and become hot-electrons. The maximum channel electric field E_m, which occurs at the drain end of the channel, has the greatest impact on the hot-electron degradation[6]. It has been recognized for a long time that the hot-electron degradation imposes major constraints on device scaling[7-8]. Therefore, the physical mechanisms of the hot-electron degradation and solutions to suppress its effects have been extensively researched[9-13].

1.1.3 Theory

While device degradation may be the most discussed hot-electron effect as explained above, there are other manifestations of hot-electrons. Figure 1.3 gives a bigger conceptual view of the hot-electron problem. As shown in Figure 1.3, all the hot-electron effects are driven by a common driving force- the channel electric field, or more specifically the maximum channel electric field E_m, which occurs at the drain end of the channel. The maximum channel electric field can be modeled as follows [7]:

$$E_m = \frac{V_{DS} - V_{Dsat}}{0.22 * T_{ox}^{\frac{1}{3}} * X_j^{\frac{1}{2}}} \quad V/cm \qquad (1.1)$$

When the channel electrons are accelerated by this maximum electric field, they become so energetic that they collide with the silicon lattice, and, as a consequence, electron/hole pairs are generated. This phenomenon is called **impact ionization**. Most of the electrons

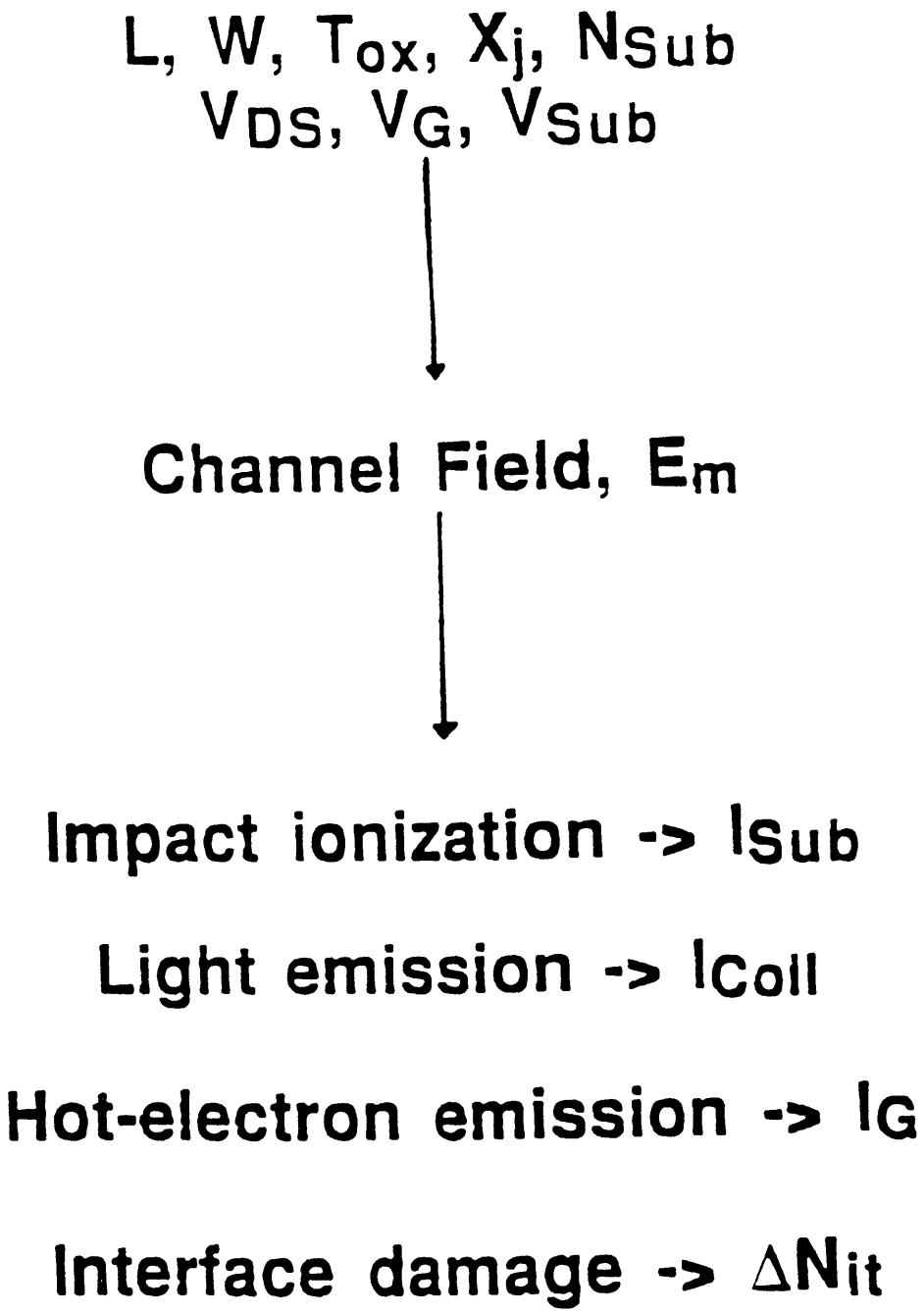

Figure 1.3 Conceptual view of the hot-electron problems[6]

generated by the impact ionization flow into the drain due to the channel electric field. Some generated holes flow into the substrate and appear as substrate current[14-15]. Thus, the substrate current I_{sub} is often used as a monitor for hot-electron degradation.

Some of the hot-electrons may be injected into the gate oxide of the MOSFET, where they become trapped and can damage the oxide and Si-SiO_2 interface. This injection is made possible because these hot-electrons have gained sufficient energy to surmount the Si-SiO_2 energy barrier(Φ_B = 2.7 - 3.2 eV, depending on the amount of barrier lowering)[10]. When crossing over the Si-SiO_2 interface, the hot-electrons break the Si-H bonds, leaving behind silicon dangling bonds that result in the formation of acceptor-type interface states[6, 13].

Conflicting views exist on whether the hot-electron degradation in N-MOSFETs, such as V_T shift and I_D reduction, is due to the charge traps in the gate oxide or the interface traps. Recent studies, however, show that for low V_{gs}($V_{gs} \approx V_T$) , the hole traps dominate the degradation mechanism, for high V_{gs}($V_{gs} \approx V_{ds}$), the electron traps dominate the degradation mechanism, and for peak I_{sub} conditions($V_{gs} \approx \frac{V_{ds}}{2}$), which has been believed to be the worst hot-electron degradation condition, the interface traps dominate the degradation mechanism[16-17]. In circuits, the MOSFETs constantly go through transients and, thus, the medium V_{gs} condition ($V_{gs} \approx \frac{V_{ds}}{2}$) best simulates the circuit operation.

There is additional evidence supporting the dominant interface traps theory. It has been shown that after long-term operation or accelerated stressing, the current-voltage characteristics of MOSFETs change. A linear relationship has been observed between the V_T shift, I_D reduction, and G_m degradation[6]. This linear relationship suggests that interface-state generation is the dominant degradation mechanism[18]. Charge pumping measurement experiments have given further evidence to support the role of ΔN_{it}[19]. Based on the above theories, the current hot-electron degradation model has been

developed under the assumption that the main degradation mechanism is interface traps[6].

Hot-electron-induced interface state can have significant impact on the performance of the MOSFET. In general, the interface state shifts the V_T and degrades the mobility of the carriers[20]. Thus, the current is continually reduced as more and more hot-electrons are injected into the gate oxide. This presents a potential reliability problem in circuits. It has been shown that both analog and digital circuit's performance degrade due to the hot-electrons[1, 21-22]. Another potential problem is CMOS latchup[23]. This can be caused by excessive substrate current which is generated by impact ionization, which, in turn, is caused by the hot-electrons.

In the N-MOSFET, the acceptor-type interface states become negatively charged when filled with electrons and reduce the number of channel electrons present at a given gate bias[12-13]. The amount of interface states that are generated due to the hot-electrons has been modeled as follows[6]:

$$\Delta N_{it} \propto [\frac{I_D}{W} e^{-\frac{\Phi_{it}}{q\lambda E_m}} * t_{stress}]^n \qquad (1.2)$$

where I_D is the drain current, W is the width of the device, Φ_{it} is the critical energy to create the interface state, λ is the electron mean-free path, E_m is the maximum electric field, t_{stress} is the time for which the device has been stressed, and n is the degradation rate coefficient which needs to be empirically extracted. Physically, the model says the following: the number of interface state generated is proportional to the drain current and the stress time, exponentially proportional to the maximum electric field, and exponentially inversely proportional to the critical energy required to create the interface state. In other words, the number of interface states generated decreases exponentially as the critical energy to create the interface states increases.

Hot-electron-induced substrate current has been modeled as follows[14]:

$$I_{sub} \propto I_D * e^{-\frac{\Phi_i}{q\lambda E_m}} \qquad (1.3)$$

where Φ_i is the critical energy for impact ionization. Again, it can be interpreted that I_{sub} is proportional to I_D, exponentially proportional to E_m, and exponentially inversely proportional to Φ_i. In other words, the substrate current decreases exponentially as the critical energy for impact ionization increases.

Combining the expressions (1.2) and (1.3) in order to eliminate the E_m term, the following equation is derived:

$$\Delta N_{it} = [\frac{I_D}{W * H} * (\frac{I_{sub}}{I_D})^m * t_{stress}]^n \qquad (1.4)$$

where $m = \frac{\Phi_{it}}{\Phi_i}$, and H is a technology-dependent constant in order to account for different technologies and device variations. It is important to notice that one needs to extract three degradation parameters, namely **n**, **m**, and **H**, experimentally, in order to use the above model to predict the amount of the hot-electron degradation in MOSFETs. This parameter extraction procedure will be explained in detail in the next chapter, and modeling these parameters to extract their values accurately forms the core study of this thesis.

In order to simplify the notation in Equation (1.4), we define the "**Age**" as follows:

$$\text{Age} \equiv \frac{I_D}{W * H} * (\frac{I_{sub}}{I_D})^m * t_{stress} \qquad (1.5)$$

When the I_D and I_{sub} are time-dependent and periodic, as in the case of AC stressing, the "Age" is modeled as follows:

$$Age = \int_0^T \frac{I_{sub}(t)^m I_D(t)^{1-m}}{W_{eff} H} dt \qquad (1.6)$$

where T is the wave form period.

Then, combining Equation (1.4) and (1.5) or (1.6),

$$\Delta N_{it} = [\text{Age}]^n \qquad (1.7)$$

We observe from equation (1.7) that the hot-electron degradation ΔN_{it} has a power law dependence on the Age.

Whereas ΔN_{it} is the dominant degradation mechanism for N-MOSFETs, it has been shown that electron traps are the dominant degradation mechanism for P-MOSFETs[24]. It has been also observed that gate current(I_g) is a better monitor for P-MOSFET hot-electron degradation than substrate current(I_{sub}), unlike in the case of N-MOSFETs. Hot-electron degradation in P-MOSFETs introduces a new problem in addition to the aforementioned problems in N-MOSFETs: a channel-length shortening phenomenon[25]. When the hot-electrons are trapped in the gate oxide near the drain, they invert the N-type Si near the drain to the P-type Si, and, thus, the effective channel length through which the carriers(holes) flow is reduced. This problem becomes more serious as the dimensions of MOSFETs reach the submicron regime. There has been less research on P-MOSFET hot-electron degradation because N-MOSFETs have caused more serious problems in the circuit operations so far. However, as device dimensions decrease, the effects of P-MOSFETs are increasing, and, thus, it is likely that the P-MOSFETs will draw more attention and research in the near future.

1.1.4 Solutions

Since hot-electron degradation has caused much concern over the years, there has been much effort to develop possible solutions to reduce hot-electron degradation effects on MOSFETs. There are two categories of solutions: (1) gate-oxide engineering to make the gate oxide more resistant to hot-electrons, and (2) drain engineering to reduce the maximum electric field.

First, gate oxide engineering seems to be a very reasonable solution because, after all, the hot-electron degradation effects(i.e changes in current-voltage characteristics) are due to the trapped hot-electrons either at the Si-SiO_2 interface or in the gate oxide. Thus, if the gate oxide becomes more hot-electron resistant, it seems that there will be less hot-electrons trapped both at the interface and in the gate oxide, and, as a result, the characteristics of MOSFETs will change less.

Fluorination and nitridation of the gate oxide are two different methods of making the oxide more hot-electron resistant. Both methods make it more difficult for hot-electrons to generate interface states[26-28]. It has been shown that significant improvement in hot-electron "hardness" is observed due to the reduced generation rate of interface traps by properly incorporating fluorine into the gate oxide[26]. Nitridation of the gate oxide has also improved the resistance to hot-electron degradation. Nitridation introduces both nitrogen and hydrogen related species into the gate oxide and demonstrates smaller charge-trapping characteristics[27-28]. A drawback of this solution, however, is that the mobility of the carriers is reduced.

As shown in equation (1.2), ΔN_{it} is exponentially proportional to the maximum electric field E_m. Thus, if E_m is reduced, ΔN_{it} would decrease exponentially. This motivates drain engineering as one of the possible solutions to hot-electron degradation. It has been shown that E_m at the drain end decreases when the lightly-doped drains(LDD) are formed by As or P implantation[29]. The LDD structure lowers the electric field by spreading the drain-to-source potential across the lightly-doped region adjacent to the drain junction. Its cross-section is compared with that of the conventional device in Figure 1.4. Apart from reducing the maximum electric field, and, hence, resulting in higher breakdown voltage, lower substrate current, and improved reliability, the LDD device also reduces short channel effects and the punchthrough voltage due to the shallower junction of the drain extension[1]. However, there are several drawbacks to this solution. First, the series resistance increases because the n^- region adds to the device on-resistance. This, in turn, reduces the current drivability. Second, the mobility of the device also degrades. The mobility reduction is a direct result of the damage in the subdiffusion and channel regions(under the gate-electrode control), which induces Coulomb scattering, which, in turn, reduces the mobility[30]. When the series resistance increases very much, ΔN_{it} does not exhibit power law dependence on Age any more as in equation (1.4).

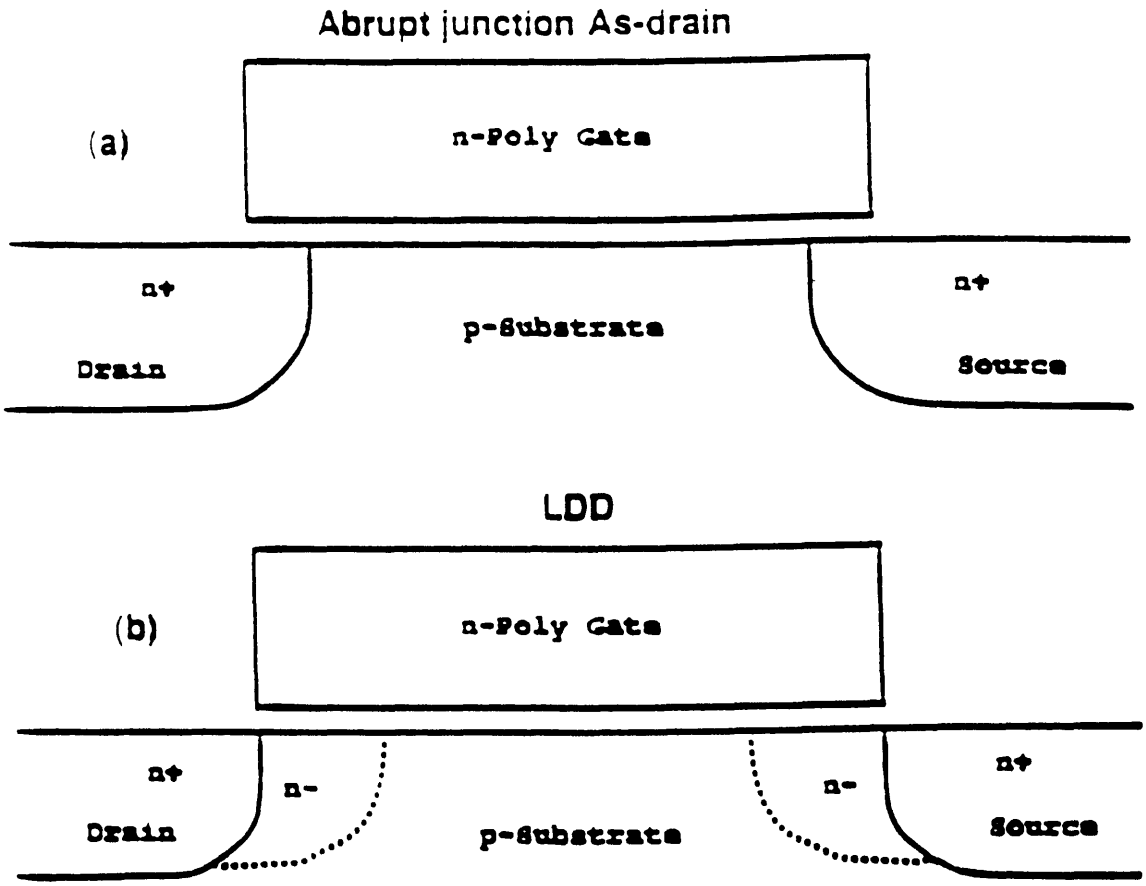

Figure 1.4 (a) the cross section of the conventional N-MOSFET; (b) the cross section of the LDD N-MOSFET

Rather, the degradation saturates with time. An astute technique can be used to calibrate the parameter extraction procedure in order to use Equation (1.4) to predict hot-electron degradation[31].

There are several possible solutions to remedy some of the hot-electron degradation effects, but there is a trade-off between device performance and reliability. This trade-off needs to be taken into account when one designs solutions for hot-electron degradation.

Chapter II

Motivation

2.1 Circuit Level Hot-electron Reliability Simulation

System and circuit performance requirements should be the primary basis for hot-electron reliability criteria because, from the customer's point of view, reliable devices are meaningless unless the end product, circuit or system, is reliable. Unfortunately, however, although there have been some extensive studies on hot-electron degradation on MOSFET devices, it still remains unclear how the hot-electron affects the overall circuit or system performance[32].

Because of uncertainty about the overall impact of hot-electron degradation, extremely conservative circuit design guidelines have been employed. The maximum allowable MOSFET V_{ds} is usually tightly limited. In addition, cascode design techniques are used to reduce the voltage drop across individual devices[33]. At the device level, the uncertainty has resulted in the widespread adoption of relatively conservative hot-electron technologies, such as LDD and fluorinated or nitrided gate oxide as explained in chapter 1. The conservative design guidelines both at the circuit and the device level sacrifice the system performance for reliability.

The uncertainty about the overall impact of hot-electron degradation on circuit performance has motivated to develop a circuit level hot-electron reliability simulation

program called the Circuit-Aging Simulator (CAS)[34]. CAS can predict the hot-electron degradation of MOSFET devices undergoing dynamic operation in circuits and, thus, can predict the degraded behavior that the circuits would have after operating a user specified operating time. In order to predict the amount of hot-electron degradation on MOSFET devices in circuits, CAS uses Equation (1.4). The three degradation parameter values in the model, **n**, **m**, and **H**, must be extracted by stressing and measuring the MOSFETs. For I_D in Equation (1.4), the SPICE model is used. For I_{sub}, the following model is used[34].

$$I_{sub} = \frac{A_i}{B_i} I_D (V_{ds} - V_{dsat}) e^{(-\frac{B_i l_c}{V_{ds} - V_{dsat}})} \tag{2.1}$$

where A_i and B_i are set to 200 and 170 for N-MOSFET and 1000 and 370 for P-MOSFET, respectively, and V_{dsat} is modeled as

$$V_{dsat} = \frac{E_{crit} L (V_{gs} - V_T)}{E_{crit} L + (V_{gs} - V_T)} \tag{2.2}$$

The l_c parameter in Equation (2.1) and E_{crit} parameter in Equation (2.2) are extracted by measuring the MOSFETs. The A_i and B_i above are empirically determined values through extensive measurements of MOSFETs to fit the model. The circuit simulator SPICE is built into CAS in order to simulate the behavior of circuits.

The following steps are taken in order to predict the hot-electron degraded behavior of circuits in CAS:

(1) A fresh circuit with no stressing is simulated by SPICE, using fresh MOSFET parameters. The MOSFET parameters, such as the flat band voltage(V_{FB}), the surface potential(ϕ_S), and the mobility constant(μ), etc., are extracted using BSIM2 parameter extraction program[35]. The output is the behavior of the fresh circuit.

(2) The user stresses a MOSFET for a certain length of time, t_1, by applying constant DC voltages(V_{ds}, V_{gs}, and V_{bs}). A proper stressing condition will be explained in section 2.2. Then, the user runs the BSIM2 parameter extraction program, with the stressed device for the period of t_1, in order to obtain degraded MOSFET

parameter values. Then, the user calculates the Age at t_1(Age_1), using Equation (1.5). This is relatively a straightforward process since all the stressing conditions are known(i.e. I_D, I_{sub}, and t_{stress} are known). The **n**, **m**, and **H** values need to be extracted in order to calculate the Age before using Equation (1.5). Extraction procedure of these three degradation parameters will be explained in detail in section 2.2. Notice that extracting these degradation parameters accurately is a critical step since the number of interface states generated(ΔN_{it}) or the changes in the I-V characteristics of MOSFETs are a strong function of these degradation parameters.

(3) The user stresses the above MOSFET for a longer period of time, t_2, by applying the same stressing conditions as above. Then, he repeats the rest of the steps taken in (2). Now, the Age_2 is calculated, and a set of degraded MOSFET parameters corresponding to the Age_2 is obtained. The user repeats this process until he obtains the Age_N. Then, N sets of degraded MOSFET parameters corresponding to Age_1 to Age_N are obtained.

(4) CAS simulates the desired circuit and calculates the Age that each device in the circuit would have if the SPICE analysis is repeated up to the user-specified future time point.

(5) CAS compares the Age of each device in the circuit with that of the stressed model parameter files that were taken in step (2) and (3), and calculates the new aged model parameters for each device in the circuit by interpolation or regression. This step is shown in Figure 2.1

(6) Once the degraded parameters for each device in the circuit is obtained from step (5), then the SPICE circuit simulation is run again with the degraded parameters. The output of this simulation is the hot-electron degraded behavior of the circuit after the user-specified future time. This can be compared with the fresh output taken in step (1).

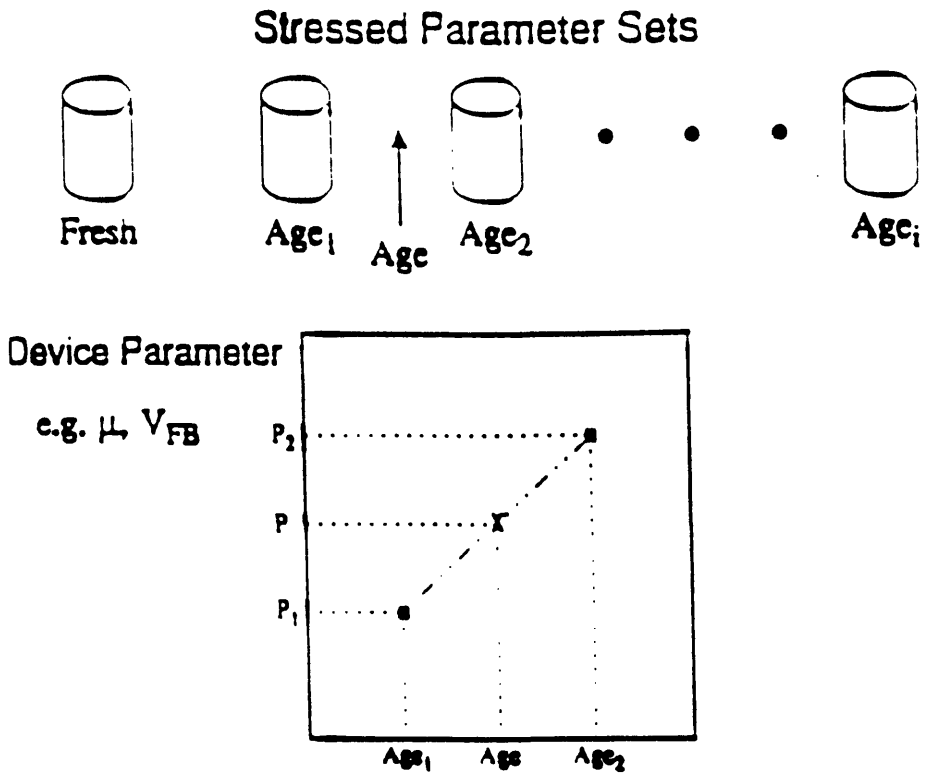

Figure 2.1 Calculation of the aged MOSFET parameters from pre-DC-stressed model parameter sets. The barrels represent the various model parameter sets with different ages Age_1, Age_2, etc., while the MOSFET's age in the circuit is represented by Age[34].

In Figure 2.1, the barrels represent the fresh and pre-DC-stressed model parameter files with Age_1, Age_2, and, etc. The Age of the device in the circuit is being compared with each Age_i. Typically, the Age of the device in the circuit will lie between two of the pre-DC-stressed model parameter sets. The user has a choice to specify whether interpolation is used as in Figure 2.1 or whether regression is desired in order to obtain the degraded parameters for each MOSFET in the simulated circuit.

The following procedure is taken in order to calculate the total ΔN_{it} that each device ,which undergoes dynamic operation in the circuit, would have(i.e. the following is

an elaboration of step (4) above). For the discussion below, the following constant is defined:

$$A = [\frac{I_D}{W * H}(\frac{I_{sub}}{I_D})^m]^n \qquad (2.3)$$

Then,

$$\Delta N_{it} = A * t^n \qquad (2.4)$$

To calculate the total ΔN_{it} that occurs in the SPICE analysis, ΔN_{it} during each time step Δt is first calculated. All the MOSFET parameters and currents(I_D and I_{sub} for each MOSFET) are assumed to be constant and are equal to their values at the beginning of the time step. Now, let us number each time period t_1, t_2, ... with differing A coefficients A_1, A_2, ... and **n** values $\mathbf{n_1}$, $\mathbf{n_2}$, ... because of the variations of the degradation parameters and currents that occur for different times.

Starting from the beginning of the analysis, ΔN_{it} occurring in the first time step is $\Delta N_{it}(t_1) = A_1 * \Delta t^{n_1}$, since no degradation has occurred before this time step. To calculate ΔN_{it} in the next time step, however, we need to consider the amount of degradation that occurred before it(i.e. $\Delta N_{it}(t_1)$), in this case equal to $A_1 * \Delta t^{n_1}$. Since ΔN_{it} of the present time step, t_2, depends only on the magnitude of the previous current degradation(i.e. ΔI_D and ΔI_{sub}), not on the stressing history, we can introduce another variable t' which represents the time it would take the device to obtain this previous degradation but at the present current level(i.e. new I_D and I_{sub}) and parameter values. In other words, in this example, we can introduce t' such that

$$\Delta N_{it}(t_1) = A_1 * \Delta t^{n_1} = A_2 * t'^{n_2} \qquad (2.5)$$

Then, we can directly add the times to compute the total degradation up to the present time step t_2.

$$\Delta N_{it}(t_2) = A_2(t' + \Delta t)^{n_2} \qquad (2.6)$$

Note that we cannot directly add the degradation of the two time steps together without normalizing the time as t' as in Equation (2.6) because Equation (2.4) only applies to DC stressing where all the currents (I_D and I_{sub}) and **n** value are constant. In other words,

$$\Delta N_{it}(t_2) \neq A_1 * \Delta t^{n1} + A_2 * \Delta t^{n2} \qquad (2.7)$$

Now, we solve Equation (2.5) for t' and substitute it into Equation (2.6) and obtain

$$\Delta N_{it}(t_2) = A_2 * [\frac{\Delta N_{it}(t_1)^{\frac{1}{n2}}}{A_2} + \Delta t]^{n2} \qquad (2.8)$$

$$= [\Delta N_{it}(t_1)^{\frac{1}{n2}} + A_2^{\frac{1}{n2}} * \Delta t]^{n2} \qquad (2.9)$$

Equation (2.9) states that the total ΔN_{it} up to the present time step can be found from that of the previous time step and from the present currents(I_D and I_{sub}) and degradation parameter **n**. In CAS, Equation (2.9) is applied successively to each time step t_i to find the total ΔN_{it} of each MOSFET in the simulated circuit[34].

2.2 Parameter Extraction Procedure

As discussed in section 2.1, CAS is used to predict the hot-electron degraded behavior of circuits. In order to use CAS successfully, the three degradation parameters, **n**, **m**, and **H**, need to be accurately extracted and fed into CAS since the degradation ΔN_{it} is a function of these parameters. A small inaccuracy in these parameter values may result in huge error of the simulation since the degradation has the power law functional dependence on these parameters as shown in Equation (1.4). This section describes the parameter extraction procedure and discusses the general issues that are associated with accurately extracting these parameters.

2.2.1 Parameter *n* Extraction

Assuming that the changes of MOSFET characteristics, such as $\frac{\Delta I_D}{I_D}$, $\frac{\Delta G_m}{G_m}$, and ΔV_T, are mainly due to the interface states as discussed in chapter 1, Equation (1.4) can be written as

$$\frac{\Delta I_D}{I_D} = [\frac{I_D}{W * H} * (\frac{I_{sub}}{I_D})^m * t_{stress}]^n \qquad (2.10)$$

Then, when plotting $\log(\frac{\Delta I_D}{I_D})$ vs. $\log(t_{stress})$ in the x-y graph, the slope of the line becomes the parameter **n**. This is shown in Figure 2.2. The data in Figure 2.2 are obtained by applying constant DC voltages V_{ds}, V_{gs}, and V_{bs}, to a N-MOSFET for 100 minutes. Intermittently, $\frac{\Delta I_D}{I_D}$ is measured and recorded. In Figure 2.2, it is measured at 1, 2, 5, 10, 20, 50 and 100 minutes so that the spacing in the log-log plot is equi-distant.

Choosing a stressing condition to obtain such a plot is important since the degradation parameter values can be a function of the stressing conditions. Traditionally, in order to account for the worst hot-electron degradation scenario, the stressing condition has been chosen such that I_{sub} is the maximum. It has long been believed that the MOSFET undergoes the most hot-electron degradation under the peak I_{sub} condition because I_{sub} is produced as a result of impact ionization, which also creates the hot-electrons[6]. The peak I_{sub} condition implies that V_{bs} = 0V for a set of V_{ds} and V_{gs}. The V_{ds} is chosen around the avalanche break-down voltage so that the degradation of the MOSFET is accelerated. Then, at $V_{ds} \approx$ break-down V_{ds} and V_{bs} = 0V, V_{gs} is swept from 0V to 5V to find the maximum I_{sub} condition. Typically, the V_{gs} for the maximum I_{sub} condition lies between 0V and 5V. Once these stressing conditions are determined, they are applied to a MOSFET for a long enough period of time to observe a considerable of amount of hot-electron degradation, such as 10% reduction of I_D in the linear region. There are other methods of choosing stressing conditions. For example, as will be shown later, the parameter **m** has a functional dependence on the electric field across the $SiO_2(E_{ox})$. Since E_{ox} at the drain end of the channel is modeled as

$$E_{ox} \cong \frac{V_{gs} - V_{ds} - V_{FB}}{T_{ox}} \qquad (2.11)$$

the V_{gs} is varied for a fixed value of V_{ds} to observe the effect of E_{ox} on the parameter values **n**, **m**, and **H**.

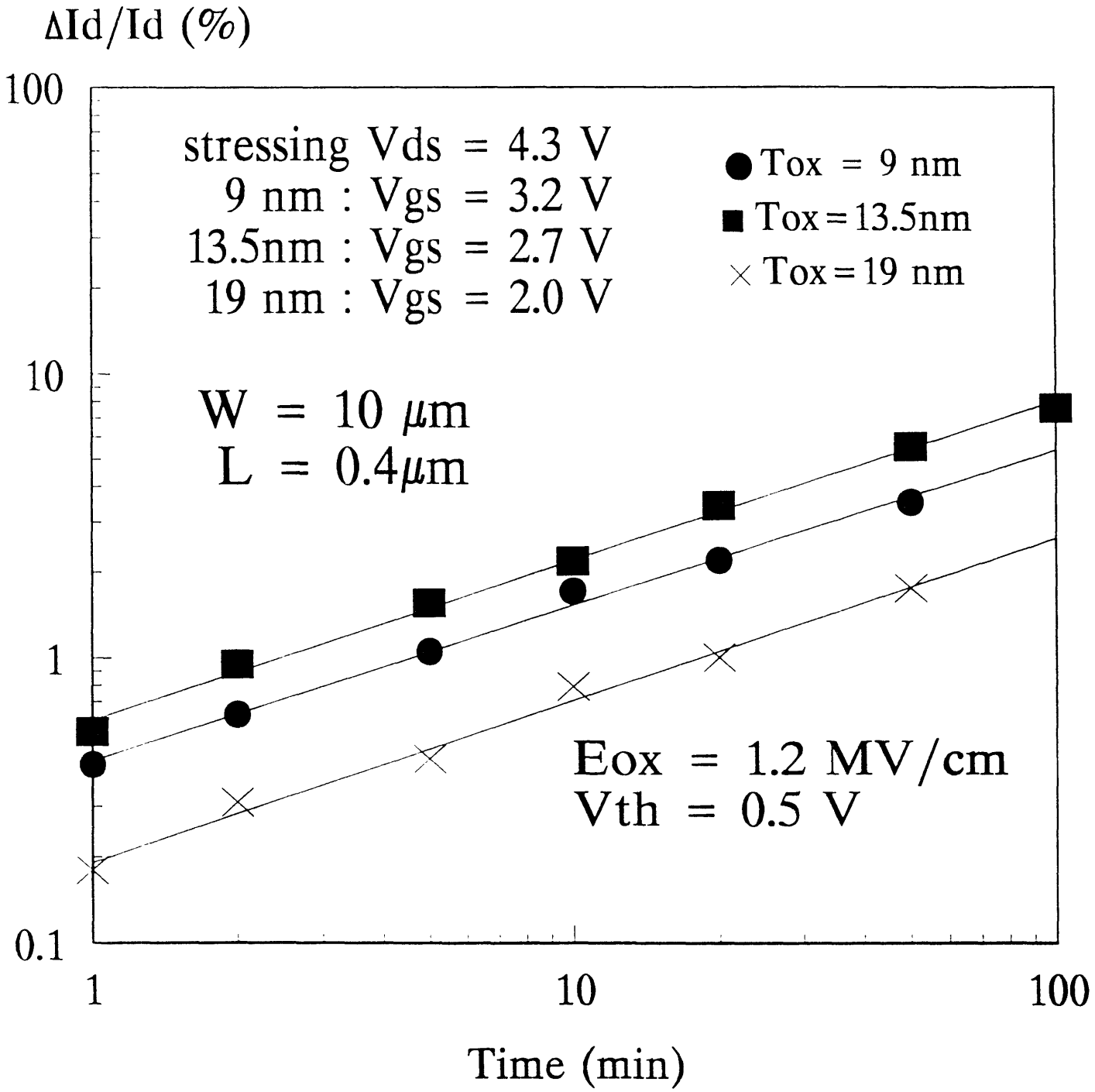

Figure 2.2 Parameter **n** extraction. The slope of the fitted lines is **n**.

In Figure 2.2, the stressing V_{ds} was chosen 4.3V, and V_{gs} was chosen for each oxide thickness(T_{ox}) so that the E_{ox} remains constant for all three T_{ox}'s. V_{bs} was set to 0 to maximize the I_{sub} as discussed above. It is found that $n \cong 0.5$ and the value is independent of the T_{ox} of MOSFETs.

2.2.2 Parameter *m* and *H* Extraction

In order to calculate the lifetime of a MOSFET due to hot-electron degradation, a lifetime criterion first needs to be formulated. A typical lifetime criterion is 10% reduction of I_D in the linear region(i.e. the time it would take the device to degrade 10% of the linear I_D under a normal operating condition). The I_D in the linear region is used most frequently as the principal degradation monitor because of its direct relation to the hot-electron-generated interface state density[20] and ease of measurements. The lifetime criterion above, however, is completely arbitrary. In fact, it has been shown through numerous studies[21, 36-37] that 10% reduction of the linear region I_D do not contribute much to the overall circuit performance degradation. For example, it has been reported that 10% degradation of I_D correspond to approximately 2.5% degradation of the propagation delay in a ring oscillator[36]. Once the lifetime criterion is formulated, Equation (1.5) can be rearranged as following:

$$\frac{\tau * I_D}{W} = H * \left(\frac{I_{sub}}{I_D}\right)^{-m} \qquad (2.12)$$

Based on Equation (2.12), the parameter **m** and **H** can be extracted from the lifetime correlation plot of $\frac{\tau * I_D}{W}$ vs. $\frac{I_{sub}}{I_D}$ in a log-log scale. By stressing the MOSFETs with different $\frac{I_{sub}}{I_D}$ ratios, the data can be fitted to the model (2.12). The negative slope and y-intercept of the fitted line correspond to the parameter **m** and log(**H**), respectively. Extraction of these parameters are shown in Figure 2.3. N-MOSFETs with feature sizes L_{eff} = 0.8μm, W= 20μm, and T_{ox}=16.5nm were stressed for 50 minutes for several different ratios of $\frac{I_{sub}}{I_D}$. Each fitted line in Figure 2.3 represents different stressing E_{ox} as

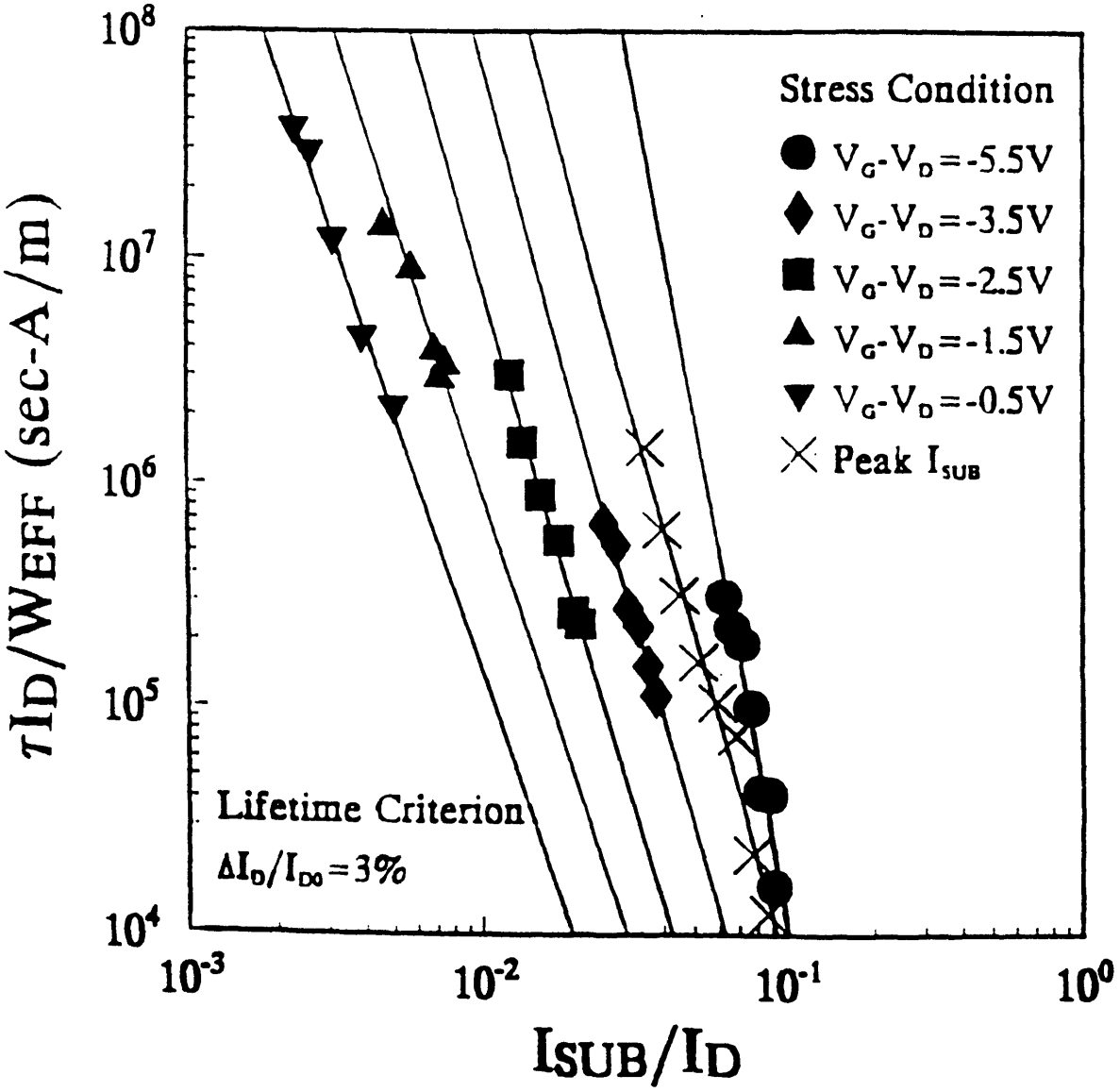

Figure 2.3 Parameter **m** extraction. The slopes of the fitted lines are **m**.

shown in Equation (2.11). It is clear from this figure that the parameters **m** and **H** have functional dependencies on E_{ox}. Its dependence is shown in Figure 2.4. A natural question that arises, then, is that which value of **m** and **H** should be fed into CAS in order to accurately simulate the hot-electron degraded behavior of circuits. It also leads to a question that whether these parameters have functional dependencies on other stressing conditions, such as V_{bs}, and MOSFET processing parameters, such as T_{ox}, X_j, and N_{sub}.

A main driving force for these questions about the **n**, **m**, and **H** parameter extraction is the lack of physical understanding of these parameters. The model (1.4) was semi-empirically developed based on extensive measurements of N-MOSFETs and a hand-waving physical theory, and, these parameters were introduced to fit the model (1.4). For example, it has been observed that the degradation has a power-law relationship with stressed time(i.e. $\Delta N_{it} = Kt^n$), but its physical reason is still unknown. The parameter **m** $= \frac{\phi_{it}}{\phi_i}$ has a physical meaning of the ratio of the critical energy for the interface traps over the impact ionization energy. However, its dependence on E_{ox}, as shown in Figure 2.3, is only qualitatively known[38]. The parameter **H** was introduced in order to account for different processing technologies and to fit the model (1.4). It has no physical meaning. Another problem that arises is how to select a correct stressing condition to extract these parameters. Since these parameters are functions of the stressing conditions, we need to find an optimal stressing condition to accurately simulate the hot-electron degraded performance of circuits.

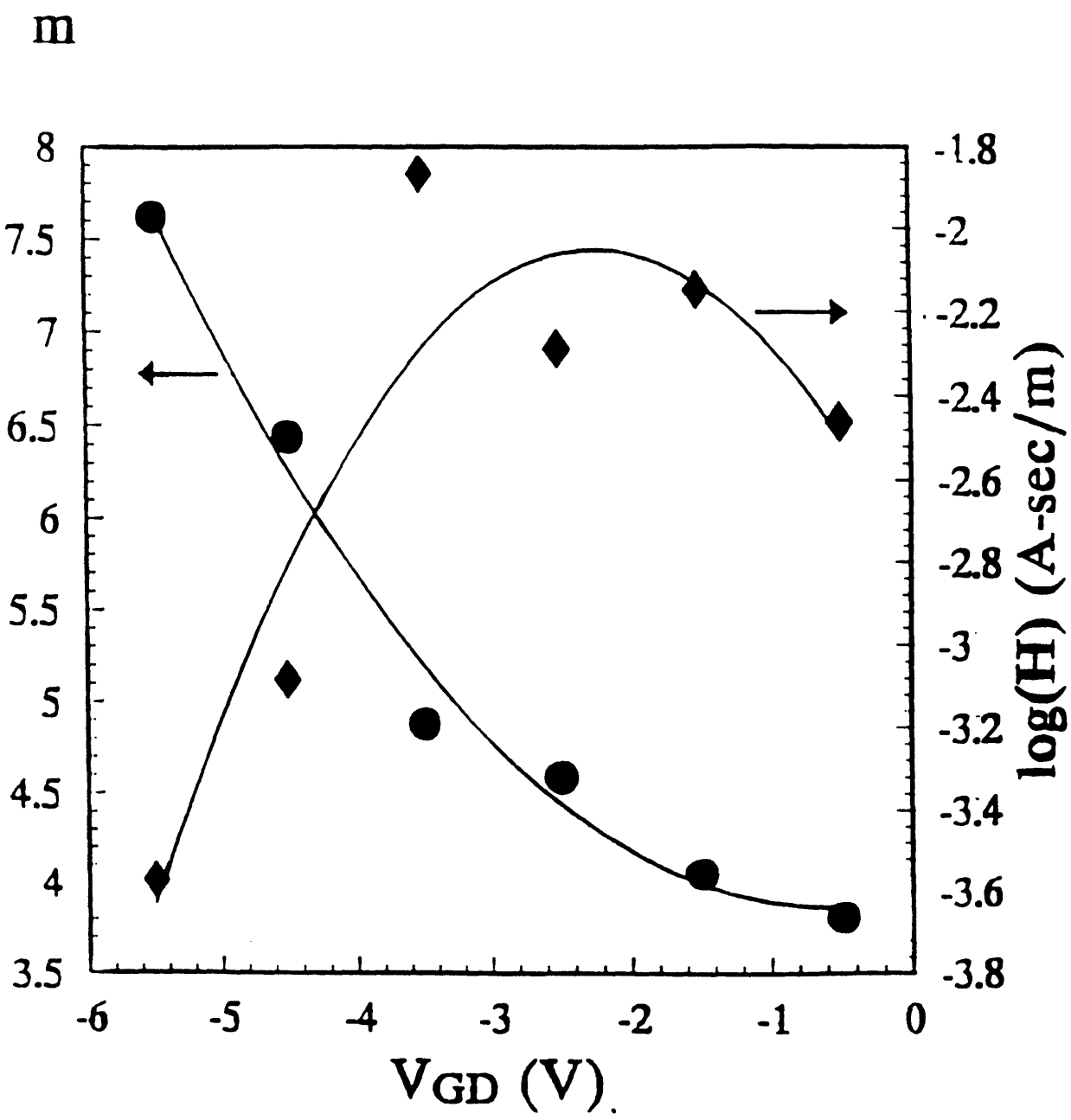

Figure 2.4 Parameter **m**'s dependence on gate-oxide electric field

Chapter III

Research Plan

3.1 Research Objective

Although there have been several experimental hot-electron degradation studies on different classes of circuits ranging from digital circuits, such as ring oscillators, different logic gates(NAND, NOR, etc) to analog circuits, such as differential amplifiers and sense amplifiers[21-22, 36-41], there has been less research on the circuit-level simulation because of numerous unanswered questions and issues that are described in section 2.2. Even some simulation studies do not address the issues that are involved in the parameter extraction procedure since these studies assume the correct parameter values[42-43]. However, it is discussed in chapter 2 that without careful calibrations, the simulation tools such as CAS and RELY[44] would not be very accurate, thus, limit their overall impacts and usefulness.

This research focuses on the parameter extraction procedure for the circuit-level hot-electron reliability simulation. More specifically, the three degradation parameters in the model (1.4), namely, **n**, **m**, and **H**, are studied. It was shown that an accurate extraction of these three parameter values is critical in simulating the performance degradation of circuits. As explained in section 2.2.2, however, the lack of physical

understanding of these parameters has caused the bottleneck in calibrating the simulation tool to a particular process.

Through extensive MOSFET measurements and stressings, these parameters' dependencies on stressing conditions(E_{ox}, E_m, V_{bs}, V_{gs}, and V_{ds}) and MOSFET processing parameters(L_{eff}, N_{sub}, T_{ox}, etc.) will be shown. As mentioned above, this issue has not been addressed in detail thus far. First, the functional dependence of the degradation parameters on stressing conditions and MOSFET processing parameters is interesting by itself to observe since this phenomenon was never completely characterized. Second, a complete result of such a functional dependence will help to summarize all the existing, hand-waving physical theories, such as the parameter **m**'s dependence on E_{ox}, and will lead to more concrete physical understanding and explanation of the degradation parameters.

Once we develop the physical intuition of these degradation parameters, we can develop an optimal stressing condition which is necessary to accurately extract these parameters. Then, we can also develop a standardized parameter extraction guideline, which explains how to calibrate the simulation tool to a particular process to simulate the hot-electron degraded performance of circuits. This will be an invaluable tool for a device engineer or circuit designer who needs the reliability criteria before the actual design and implementation stage.

3.2 Experimental Setup

The equipments used for the hot-electron stressing and measurement are shown in Figure 3.1. The setup consists of a probe station, which probes MOSFETs individually, a semi-conductor parameter analyzer(HP4145), which measures the I-V characteristics of MOSFETs, a personal computer, which controls all the stressing and measurement of MOSFETs, and a plotter, which prints out the data and figures on paper for analysis.

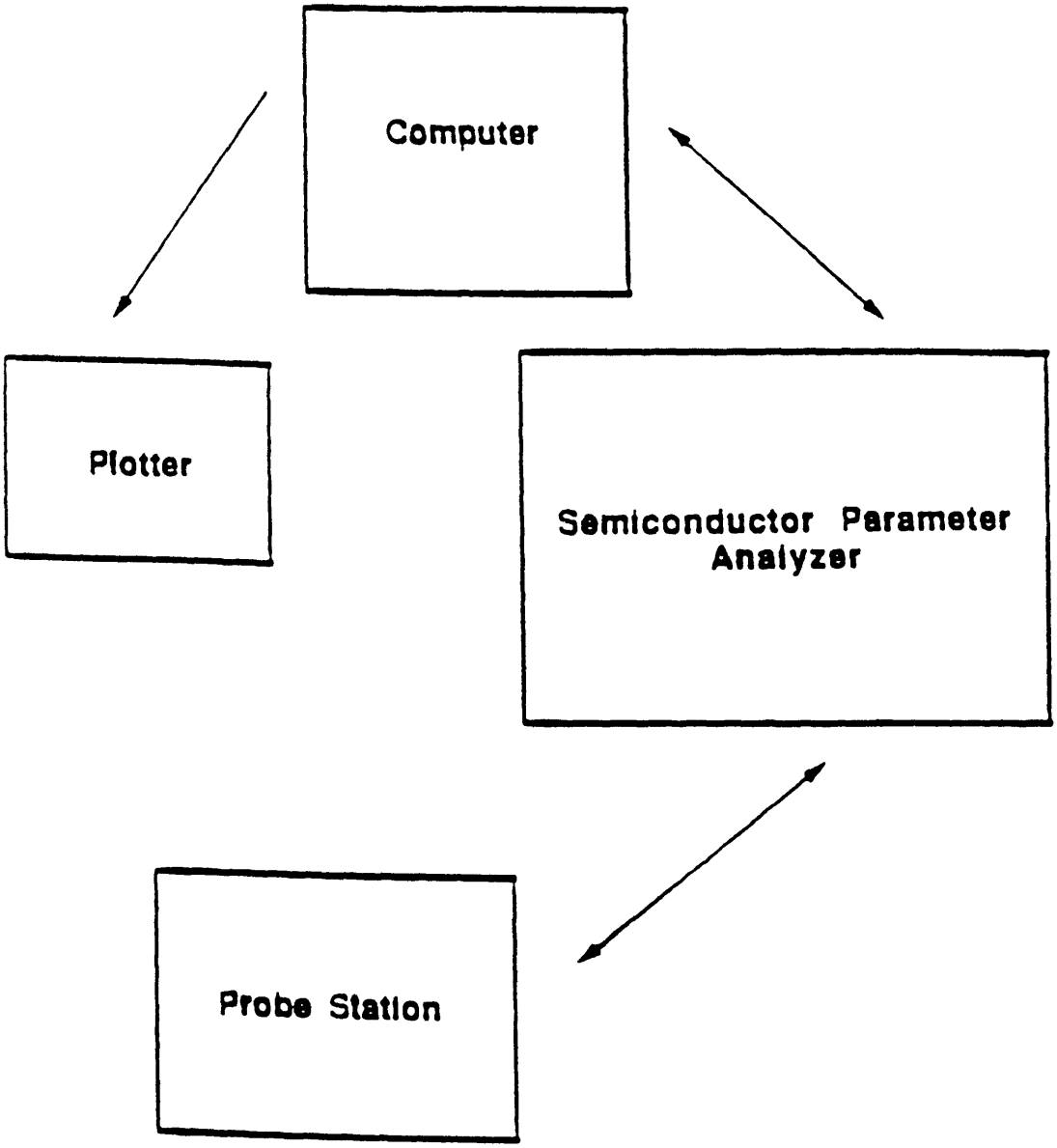

Figure 3.1 Experimental setup for automated stressing and measuring MOSFETs

There are several software programs that are used to automate the stressing procedure and analyze the data to calculate the current degradation, threshold voltage shifts, and etc.

Chapter IV

Device Fabrication

4.1 MOSFET Splits

As explained in Chapter 3, an extensive number of MOSFET devices with different processing parameters are needed in order to observe functional dependencies of the hot-electron degradation parameters(**n**, **m**, and **H**) on the MOSFET processing parameters, such as the gate-oxide thickness(T_{OX}) and the channel substrate doping(N_{sub}). Therefore, both the N-MOSFETs and P-MOSFETs have been fabricated with varying T_{OX}'s and N_{sub}'s. Table 4.1 summarizes all the splits for the N-MOSFETs, and Table 4.2 summarizes all the splits for the P-MOSFETs that were fabricated.

For the N-MOSFETs, the starting wafer is a conventional boron-doped bulk wafer with the resistivity of 10-20 ohm-cm. For each T_{OX}, three wafers through identical processing conditions are fabricated in order to model the device variations. For the P-MOSFETs, the starting wafer is a conventional phosphorous-doped bulk wafer with the resistivity of 10-20 ohm-cm. For each T_{OX}, two wafers through identical processing conditions are fabricated. For both the N-MOSFETs and P-MOSFETs, there are a total of five T_{OX}'s splits, ranging from 7 nm to 33 nm. Thus, there are a total of 15 wafers of N-MOSFETs and 10 wafers of P-MOSFETs.

N-MOSFETs

Wafer ID	T_{ox}	BF_2 dose	V_T
G7, E7, B4	9 nm	High: 1.0 x $10^{13}cm^{-2}$ Med: 5.5 x 10^{12} Low: 3.1 x 10^{12}	1.05 V 0.67 V 0.50 V
A1, B0, D4	13.5 nm	High: 5.0 x 10^{12} Med: 3.1 x 10^{12} Low: 2.0 x 10^{12}	0.80 V 0.55 V 0.35 V
D3, F5, G6	19 nm	High: 3.5 x 10^{12} Med: 2.4 x 10^{12} Low: 1.7 x 10^{12}	0.35 V 0.22 V 0.05 V
G4, F7, A4	24 nm	High: 2.9 x 10^{12} Med: 2.1 x 10^{12} Low: 1.5 x 10^{12}	0.65 V 0.42 V 0.27 V
A2, E3, B5	33 nm	High: 2.7 x 10^{12} Med: 1.9 x 10^{12} Low: 1.4 x 10^{12}	0.45 V 0.27 V 0.15 V

Table 4.1 Processing parameter splits for N-MOSFETs

P-MOSFETs

Wafer ID	T_{ox}	Phosphorous dose	V_T
G1, H1	9 nm	High: 7.5 x $10^{12}cm^{-2}$	- 1.05 V
		Med: 5.0 x 10^{12}	- 0.81 V
		Low: 2.5 x 10^{12}	- 0.55 V
E6, D6	13.5 nm	High: 4.0 x 10^{12}	- 0.95 V
		Med: 2.7 x 10^{12}	- 0.75 V
		Low: 1.1 x 10^{12}	- 0.30 V
C4, C0	19 nm	High: 2.5 x 10^{12}	- 0.50 V
		Med: 1.4 x 10^{12}	- 0.22 V
		Low: 9.0 x 10^{11}	- 0.15 V
G2, F2	24 nm	High:1.7 x 10^{12}	- 1.15 V
		Med:1.1 x 10^{12}	- 0.70 V
		Low:8.0 x 10^{11}	- 0.45 V
C7, B5	33 nm	High:1.1 x 10^{11}	- 0.95 V
		Med:9.0 x 10^{11}	- 0.62 V
		Low:7.0 x 10^{11}	- 0.55 V

Table 4.2 Processing parameter splits for P-MOSFETs

Within a wafer for each T_{ox}, three different channel dopings(N_{sub}) are implanted. Instead of having different N_{sub}'s on different wafers, which would have been much easier and simpler process, the N_{sub} splits are done on the same wafer in order to minimize the effects of device variations on the N_{sub} splits. Rows 2, 5, and 8 are chosen for the highest doping concentration, rows 1,4, and 7 for the medium doping concentration, and rows 3 and 6 for the lowest doping concentration for all the wafers. The rows that are not being implanted are covered by photoresist. For example, when rows 2, 5, and 8 are to be implanted with the highest dose, all the remaining rows are covered by photoresist. This procedure is repeated for all three doping concentrations.

The splits in T_{ox} can be used to test the parameter **n** and **m**'s dependence on T_{ox} and also on E_{ox}. Since T_{ox} is different, applying the same bias V_{gs} and V_{ds} would stress MOSFETs at different E_{ox}'s, and, thus, the parameters' dependence on E_{ox} can be characterized. The splits in N_{sub} are also used in a similar way to determine the parameters' functional dependence on N_{sub}. This is especially interesting because the energy band, in the channel near the drain, bends by different amount for different doping concentrations, and, would change the Φ_{it}, the critical energy to create the interface-traps, thus, change the parameter $\mathbf{m}(=\frac{\Phi_{it}}{\Phi_i})$. This test can illuminate on the existing, physical hand-waving theory regarding the parameter **m**'s dependence on E_{ox} as explained before.

4.2 Process Flow and Fabrication

Four masks are used in building both the N-MOS and P-MOS devices: active-area pattern, gate definition, contacts, and metal mask. SUPREM III is used in order to simulate the entire process. Since there are five different oxide thicknesses and fifteen different doses for channel implant for both N-MOS and P-MOS, the simulation is repeated with different parameter values, such as different temperatures and time lengths for the gate-oxidation, and different values of implant doses in order to design the

MOSFETs according to the desired specification. For example, for all the gate oxide thicknesses, it is aimed that the highest V_T is 1V, the medium one is 0.75V, and the lowest one is 0.5V(in absolute magnitude for P-MOS devices). An example input and output file of the SUPREM simulation are shown in Figure 4.1 and 4.2. However, as shown in Table 4.1 and 4.2, the actual measured values are a bit different from the simulated ones. This shows the limit on the accuracy of the SUPREM III simulator.

There are some noticeable characteristics of this process. First, all the gate oxidations are carried out at the same temperature 950 C in order to keep the oxide quality about the same. The aimed oxide thicknesses from the simulation are 7, 12, 18, 24, and 30 nm. There is again a small discrepancy between the simulated and the measured values as shown in Table 4.1. Although the simulator yields 16 minutes for 7 nm of the gate oxide at 950 C, the actual thickness measured by ellipsometer is approximately 9 nm after the specified time period of the oxidation. This difference is due to the rapid dry oxidation at relatively high temperature 950 C.

Second, an over-exposure technique is employed in order to yield the MOSFETs for the channel length as short as 0.25 μm. The photo-lithography system which is used for this process uses the ultraviolet(UV) G-line light whose wavelength is too long to fabricate very short channel devices. Using this lithography system, the minimum feature size that can be reliably fabricated is about 1 μm. Thus, an astute fabrication technique called the over-exposure is used in order to make short channel devices using this lithography system. The gate-definition mask is designed such that the smallest channel length goes down to as small as 0.5 μm, and the channel length of the device increases every 0.1 μm until 1.2 μm. In order to make very short channel devices, we purposely increase the light exposure time in order to barely expose away the smallest channel length, in this case, 0.5 μm. Then, starting from 0.6 μm, we have a very short channel, which is on the verge of being exposed away. Usually, the first few smallest dimensions, in this case, up to 0.8 μm do not form a well-defined channel. For my devices, starting

```
TITLE       N-MOSFET SIMULATION
COMMENT     This simulation is just on the active area.
COMMENT     HI Vt IMPLANT SPLIT with gate oxide = 70A

INITIALIZE SILICON <100>, CONCENTR=2.5E14 BORON, THICKNESS=2

COMMENT STEP 1
DIFFUSION    TIME=30  TEMPERAT=900 DRYO2
PRINT        LAYERS

COMMENT STEP 2
IMPLANT      DOSE=1E13    ENERGY=40  BF2
PLOT         CHEMICAL ACTIVE BORON


COMMENT STEP 3
ETCH         OXIDE ALL
PRINT        LAYERS

COMMENT STEP 4 : GATE OXIDATION FOR 70A
DIFFUSION    TIME=16  TEMPERAT=900 DRYO2
PRINT        LAYERS

COMMENT STEP 5 : POLYSILICON DEPOSITION
DEPOSITION   THICKNESS=0.3 POLYSILI TEMPERAT=625 CONCENTR=1E19 AS
PRINT        LAYERS
PLOT          ACTIVE BORON

COMMENT STEP 6 : POLYSI GATE IMPLANT
IMPLANT      DOSE=4E15  ENERGY=25  AS
comment PRINT        LAYERS
PLOT         ACTIVE AS

COMMENT STEP 7 : DIFFUSION OF IMPLANTED AS
DIFFUSION    TIME=18  TEMPERAT=950  DRYO2


COMMENT STEP 8 : ETCH OXIDE
ETCH         OXIDE  ALL
PRINT        LAYERS
PLOT         ACTIVE AS

COMMENT STEP 9 : METALIZATION
DEPOSITION   THICKNESS=1.0 ALUMINUM
PRINT        LAYERS


COMMENT STEP 9 : Vth
V.THRESHOLD   SURFACE

SAVEFILE FILENAME = siml-h STRUCTUR
```

Figure 4.1 An example input file to SUPREME III. The corresponding output is shown in Figure 4.2

```
                    Thu Apr 14 18:27:06 1994

*******************************************************************************

    Simulation commands input from siml-h.sup

Layer    material type       thickness   dx     dxmin top  bottom  orientation
 no.                         (microns)   (microns)   node  node  or grain size
  2    OXIDE                   0.0110 0.0100 0.0010  298   299
  1    SILICON                 1.9952 0.0100 0.0010  300   500       <100>

                        Integrated Dopant
Layer            Net                          Total
 no.      active       chemical       active       chemical
  2    -3.1369E+08  -3.1369E+08   3.1369E+08   3.1369E+08
  1    -4.9434E+10  -4.9434E+10   4.9434E+10   4.9434E+10
 sum   -4.9748E+10  -4.9748E+10   4.9748E+10   4.9748E+10

                        Integrated Dopant
Layer            BORON
 no.      active       chemical
  2     3.1369E+08   3.1369E+08
  1     4.9434E+10   4.9434E+10
 sum    4.9748E+10   4.9748E+10

Chemical BORON Impurity Profile
      14         15         16         17         18         19         20         21
  0.00 ==========================================*==================================
  0.01 ==========================================*==================================
       !          !          !          !          ! *        !          !          !
       !          !          !          !*         !          !          !          !
       !          !          *          !          !          !          !          !
       !          ! *        !          !          !          !          !          !
       !        * !          !          !          !          !          !          !
       !      *   !          !          !          !          !          !          !
  0.25 +-----*----+----------+----------+----------+----------+----------+----------+
       !    *     !          !          !          !          !          !          !
       !    *     !          !          !          !          !          !          !
       !    *     !          !          !          !          !          !          !
       !    *     !          !          !          !          !          !          !
       !    *     !          !          !          !          !          !          !

 STEP 4 : GATE OXIDATION FOR 70A
000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\(
0\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\00(
000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\000\(
0\000\000\000\000\000\000\000\000\000\000
1

Layer    material type       thickness   dx     dxmin top  bottom  orientation
 no.                         (microns)   (microns)   node  node  or grain size
  2    OXIDE                   0.0070 0.0100 0.0010  298   299
  1    SILICON                 1.9921 0.0100 0.0010  300   500       <100>
```

Figure 4.2 The simulated result of the input file shown in Figure 4.1. The simulated T_{ox} = 12 nm and V_T = 1V.

Layer no.	material type	thickness (microns)	dx (microns)	dxmin	top node	bottom node	orientation or grain size
4	ALUMINUM	1.0000	0.0100	0.0010	267	267	
3	POLYSILICON	0.2870	0.0100	0.0010	268	297	0.4138
2	OXIDE	0.0070	0.0100	0.0010	298	299	
1	SILICON	1.9921	0.0100	0.0010	300	500	<100>

STEP 9 : Vth

Threshold Voltage Calculation.

Device Temperature: 27. degrees C.
Fixed Oxide Charge Density: 0.0000E+00 per unit area
Bulk Contact Concentration: 7.8894E+17 per cm-3, p-type
Oxide Capacitance: 4.9036E-07 F/cm

Vsub	Vth	Vpnch	Xdpl
0.000	1.061	1.043	0.047
0.500	1.303	1.281	0.057
1.000	1.497	1.472	0.067
1.500	1.659	1.631	0.077
2.000	1.794	1.773	0.097
2.500	1.907	1.878	0.107
3.000	1.990	1.956	0.137
3.500	1.963	1.928	1.037
4.000	1.957	1.919	1.897
4.500	1.957	1.917	2.542
5.000	1.958	1.916	3.042

Figure 4.2 continued from the previous page

from approximately 0.9 μm drawn dimension, the MOSFET starts to have good characteristics. This technique is called the over-exposure technique, and it requires a very careful calibration of the lithography tool and inspection of the lithography result. A typical light exposure time is about 0.18 seconds as opposed to 0.12-0.14 seconds for a normal process.

Third, short channel devices have shallow junction depth. As mentioned in Chapter 1, the scaling for the junction depth is necessary as well as for the channel length. In order to achieve a shallow junction depth, a short drive-in is carried out at high temperature. For this process, the drive-in is carried out for 13 minutes at 900 C. The simulated junction depth is 0.12 μm.

The entire process flow is designed and implemented using the Process Flow Representation (PFR), a research project to computerize the processing steps in the Microsystems Technology Laboratory(MTL) at M.I.T. Although it takes some initial effort and time to learn to program in PFR, it facilitates the processing steps in fabrication later since all the procedures are computerized. The PFR can be especially useful if the wafers are fabricated by a group of people since the computer program provides a clear communication between fabricators. The complete flow for my process in the PFR program is attached in the Appendix for more detailed process steps that are not discussed above.

4.3 Device Characterization

Once the MOSFETs are fabricated, their I-V characteristics need to be verified before being stressed in order to model the hot-electron degradation parameters. Figure 4.3 shows drain current(I_D) characteristics as a function of V_{gs} and V_{ds}. The wafer ID is G7 and T_{ox} = 9 nm. The measured device is in row 5 on the wafer G7, and, as shown in Table 4.1, the extrapolated V_T at V_{bs} = 0V is 1V. The extracted channel length, using the R_{meas} algorithm[44], is 0.3 μm, and the width is 10 μm. Figure 4.4 shows substrate

current(I_{sub}) characteristics as a function of V_{gs} and V_{ds}. The I_{sub} is plotted on the log scale since the order of magnitude varies by about 10^6 from the lowest to the highest value. Both I_D and I_{sub} show clean, nice device characteristics.

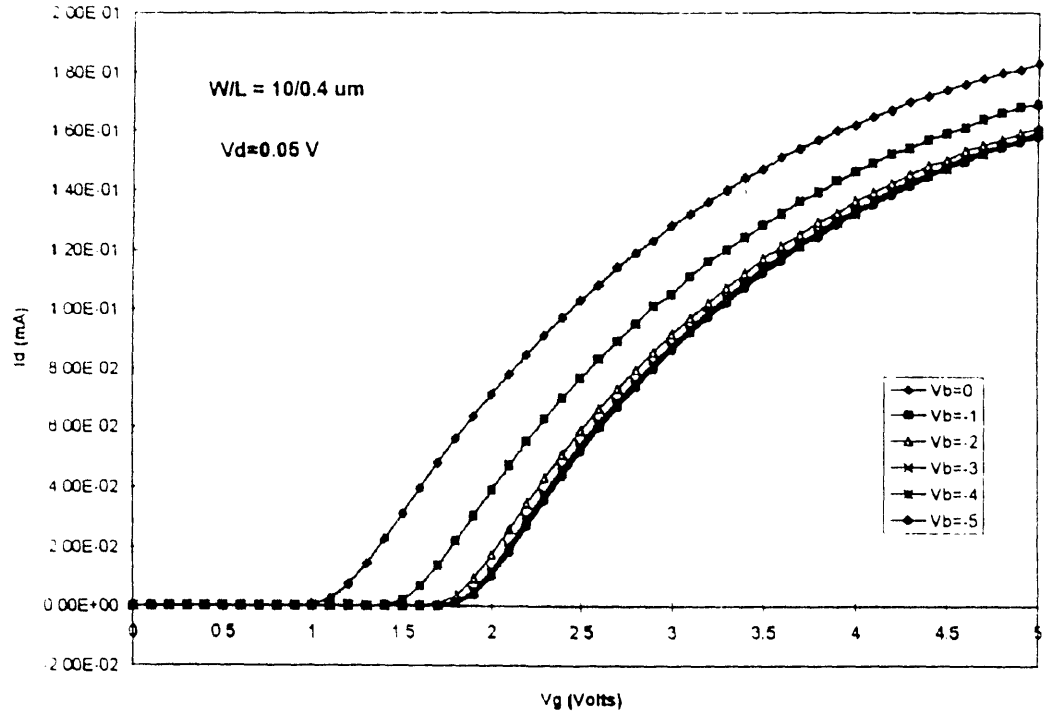

Figure 4.3 (a) I_D vs. V_{gs} for several V_{bs} biases.

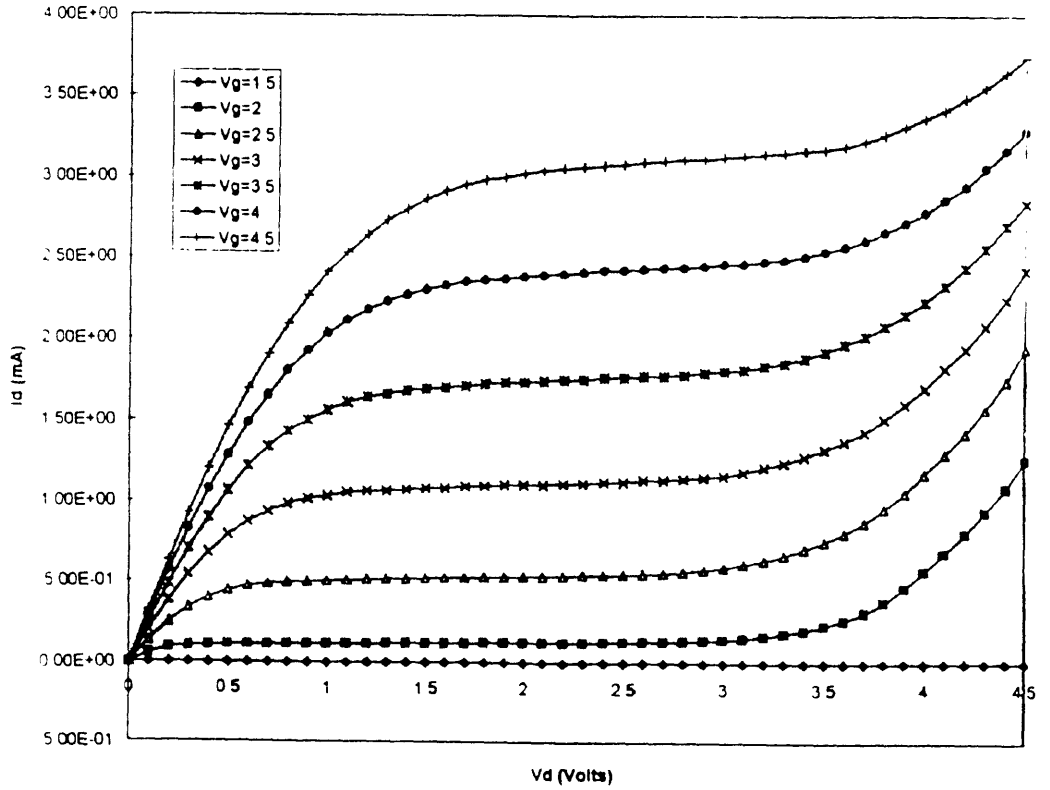

Figure 4.3 (b) I_D vs. V_{ds} for several V_{gs} biases.

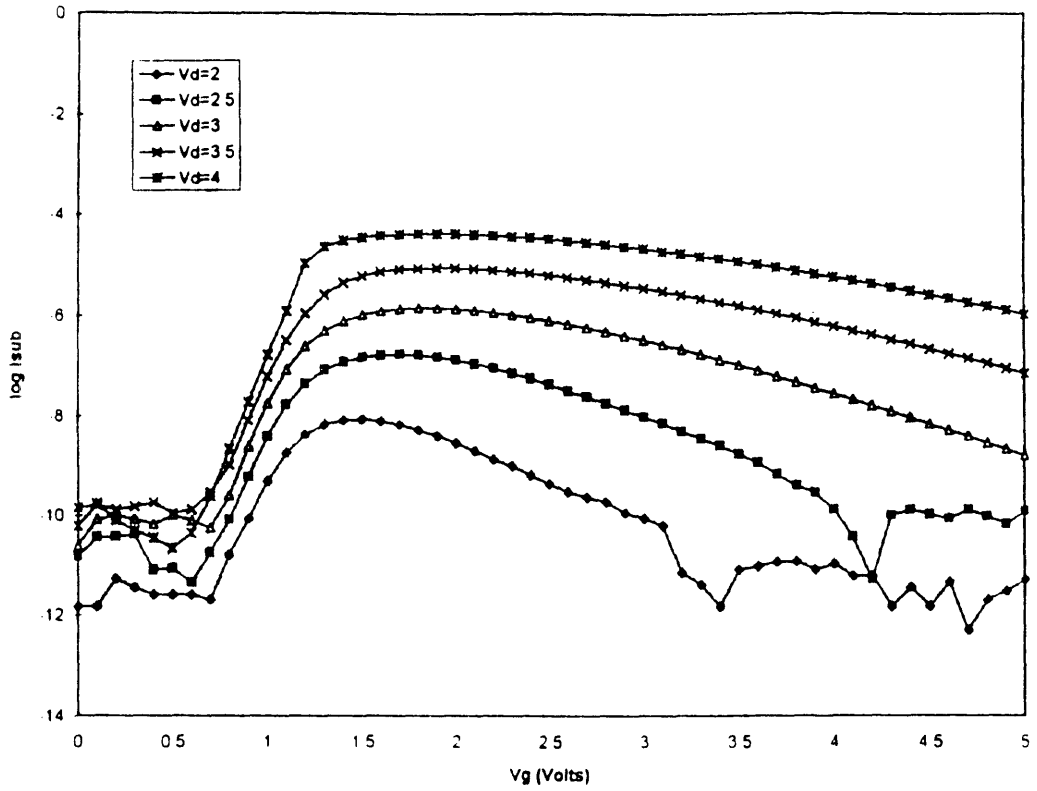

Figure 4.4 (a) I_{sub} vs. V_{gs} for several V_{ds} biases.

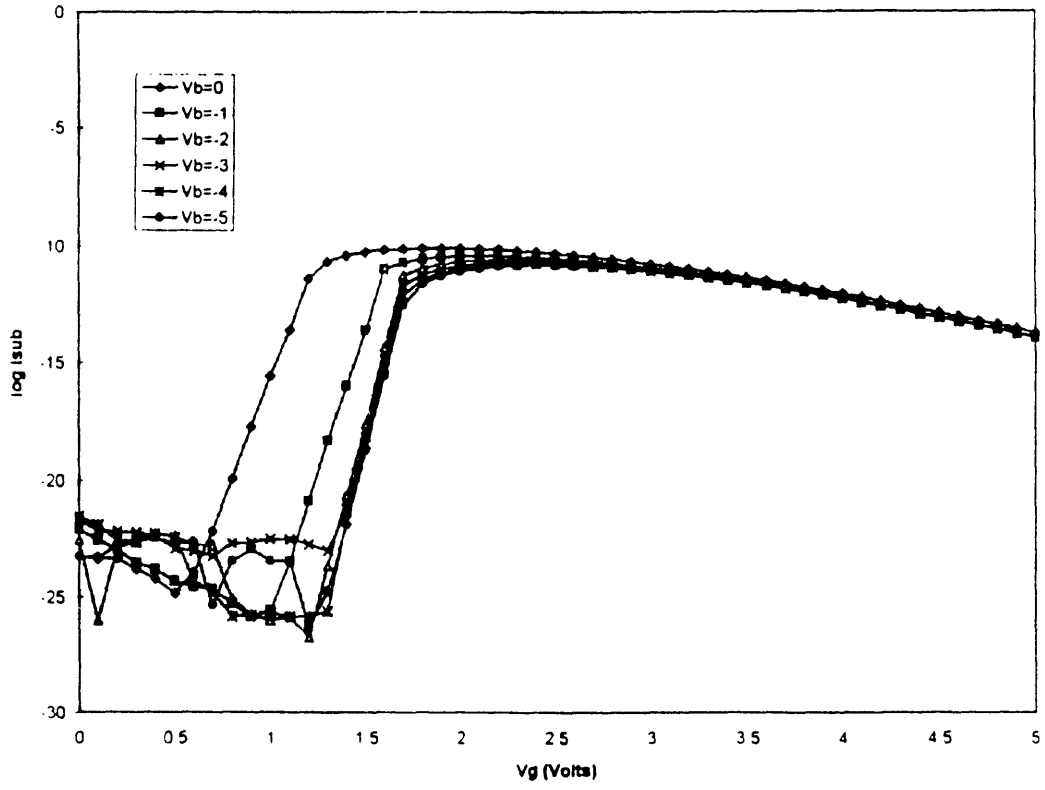

Figure 4.4 (b) I_{sub} vs. V_{gs} for several V_{bs} biases

Chapter V

Hot-electron Degradation Model & Its Parameter Extraction

5.1 Overview

Fabricated MOSFET devices have been stressed at various stressing conditions in order to determine the hot-electron degradation parameters' dependence on the MOSFET processing parameters(from the MOSFET splits) and stressing conditions. For a review of the degradation parameters, the degradation model is shown below.

$$\Delta N_{it} = \left[\frac{I_D}{W * H} * \left(\frac{I_{sub}}{I_D}\right)^m * t_{stress}\right]^n \qquad (5.1)$$

In order to predict the number of interface states generated, or the amount of corresponding change in the I-V characteristics of MOSFETs after the MOSFETs undergo the hot-electron degradation, Equation (5.1) is used in the circuit aging simulator(CAS). In order to use the simulation program, however, the degradation parameters **n**, **m**, and **H** must be extracted by stressing and measuring the MOSFETs. The physical meanings of the degradation parameters and their extraction technique are explained in detail in Chapter 2.

An accurate extraction of these parameter values is very critical in simulating the hot-electron degraded behavior of circuits after the circuits operate for a user-specified period of time.

A small amount of inaccuracy in the degradation parameter values may result in a huge amount of error in the simulation because the calculated ΔN_{it} for one cycle is extrapolated to a ΔN_{it} value that each MOSFET device in circuits would have after being operated for a user-specified period of time. An example for an error in extracted parameter **n** is shown in Figure 5.1. It is shown that as deviation of the extracted parameter **n** value is further away from the true **n** value, the extrapolation error increases by large amount as the number of extrapolated cycles increases.

The importance of accurately extracting the degradation parameters **n**, **m**, and **H** has motivated to study their extraction method(for example, choosing an optimal stressing condition) and their physical meanings. As an initial step, the degradation parameters' dependence on MOSFET processing parameters, such as T_{ox} and N_{sub}, and stressing conditions, such as different biases of V_{gs}, V_{ds}, and V_{bs}, has been characterized. Its result is also analyzed in order to illuminate on the existing physical mechanisms, and to further the understanding of and build up on the current theories.

5.2 Degradation Parameters' Characterization

5.2.1 Parameter *n*

5.2.1.1 Oxide Thickness(T_{ox})

The extraction method of the parameter **n** was shown in Figure 2.3 in Chapter 2. $\frac{\Delta I_D}{I_D}$ is plotted against the stressed time in log-log scale, and the slope of the fitted lines corresponds to the parameter **n**. Figure 5.2 shows the parameter **n**'s dependence on T_{ox}. MOSFETs with different T_{ox}'s, which are stressed, have the same amount of doping

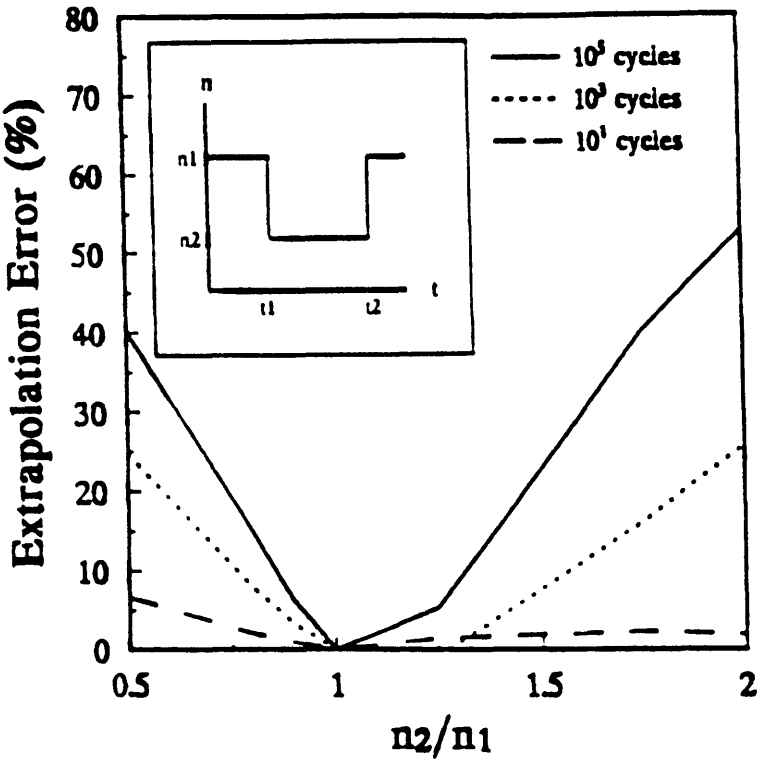

Figure 5.1 Extrapolated error as a function of deviation of the measured **n** value from the true **n** value

concentration(N_{sub}). The stressing condition for each T_{ox} is chosen such that the strength of the electric field across the gate-oxide at the drain end(E_{ox}) remains equal for all the oxide thicknesses. Equation (2.11) is used in order to model the E_{ox}. The V_{gs} and V_{ds} bias are chosen such that the degradation mechanism for all the T_{ox}'s is in the same regime, namely the interface-trap dominant regime[17]. The chosen stressing condition and the MOSFET splits ensure to decouple the effect of T_{ox} on the parameter **n** from all the other MOSFET processing parameters, stressing conditions, and the degradation mechanisms. As one can see, the slopes of the fitted lines are approximately equal to one another for the range of T_{ox}'s from 13.5 nm to 24 nm. As a matter of fact, the data compared with those of Figure 2.3 are very similar. In all cases, the parameter **n** value is about 0.5 from the oxide thickness of 9 nm to 24 nm. T_{ox} 33 nm is not used since the E_{ox} cannot be normalized to have the same strength because its source-drain break-down voltage is not high enough to support large V_{gd} for the same strength of E_{ox}. From these

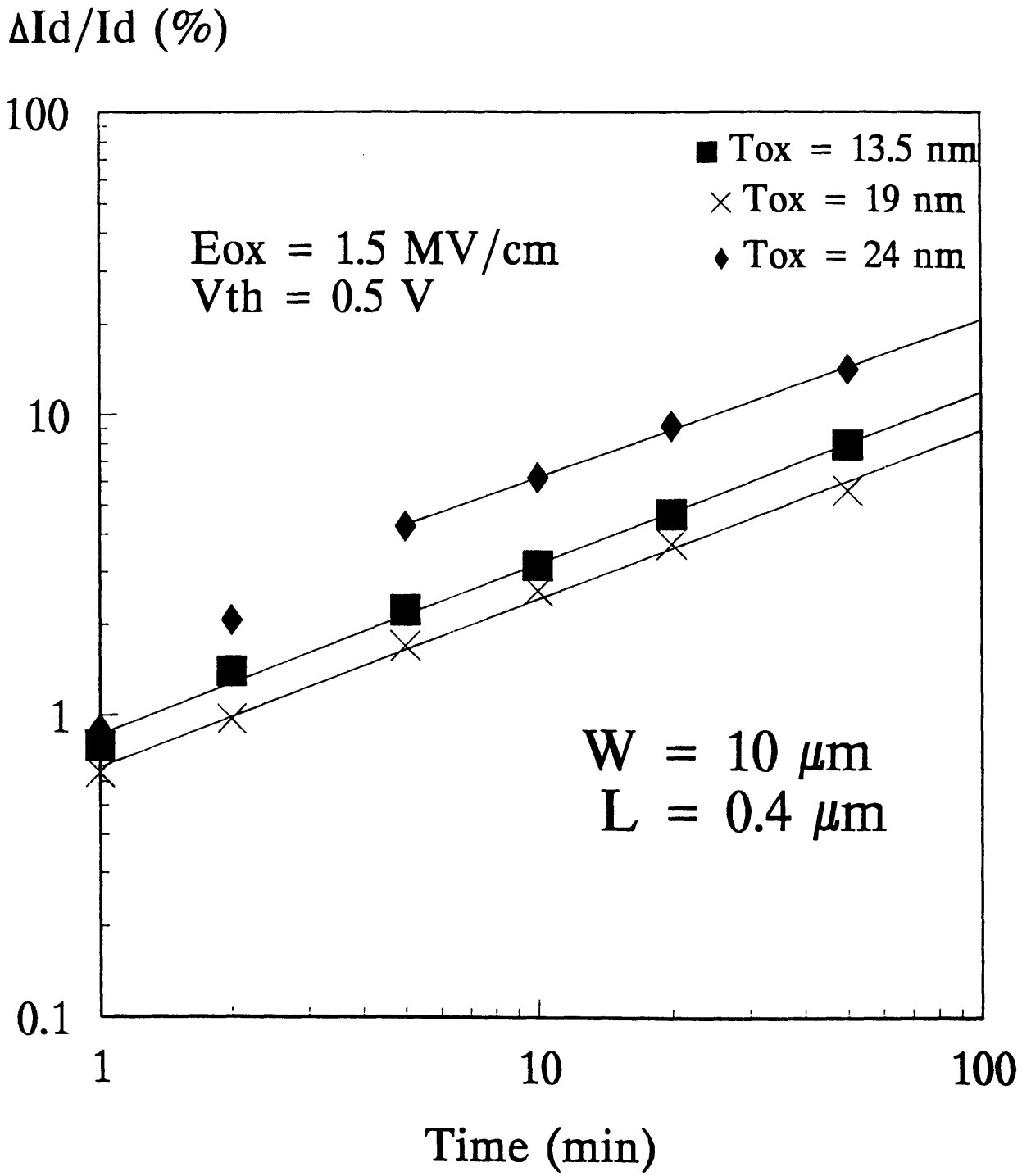

Figure 5.2 The degradation rate coefficient **n**'s dependence on T_{ox}

data, we conclude that the degradation rate coefficient **n** is independent of the gate-oxide thickness.

5.2.1.2 Channel Doping Concentration(N_{sub})

Figure 5.3 shows the parameter **n**'s dependence on N_{sub}. T_{ox} of the used MOSFETs is 13.5 nm. Again, all the stressing conditions are chosen such that the effect of N_{sub} is decoupled from all the other parameters, such as E_{ox} and degradation mechanisms. As one can see, the degradation rate coefficient **n** is independent of the channel doping concentration. This is interesting because the amount of energy band bending in the channel is different for different N_{sub}'s. Physically , it says that the time acceleration factor **n** in the hot-electron degradation is not influenced by the band bending in the channel(i.e. the vertical electric field in the channel).

5.2.1.3 Electric Field Across the Gate-oxide at the Drain(E_{ox})

The rate coefficient **n**'s dependence on E_{ox} is shown in Figure 5.4. In part (a), T_{ox} of the stressed MOSFETs is 9 nm. The stressing V_{ds} is set at 4.5V, and the V_{gs} is swept from 2.1V to 3.6V. These stressing conditions vary the E_{ox}, but the dominant degradation mechanism is still under the interface-traps regime[17]. The channel doping concentration is kept the same at $5x10^{17}$ cm^{-3} for all the E_{ox}'s. The stressing V_{bs} is set to 0V. It is shown that **n** is the same for all the stressing E_{ox}'s. This is verified by using another set of devices in part (b). T_{ox} of the stressed MOSFETs is 13.5 nm. The stressing conditions are similar to those in part (a) so that the effect of E_{ox} is separated from all the other MOSFET processing parameters, stressing conditions, and degradation mechanisms. As in part (a), **n** is independent of the stressing E_{ox}.

5.2.1.4 Hot-electron Degradation Mechanism

Thus far, the degradation rate coefficient **n** has been shown independent of the MOSFET processing parameter T_{ox} and N_{sub} and the stressing condition E_{ox}. However, as explained in Section 1.1.3, the MOSFETs undergo the hot-electron degradation by various degradation mechanisms. It has been shown in [16-17] that the

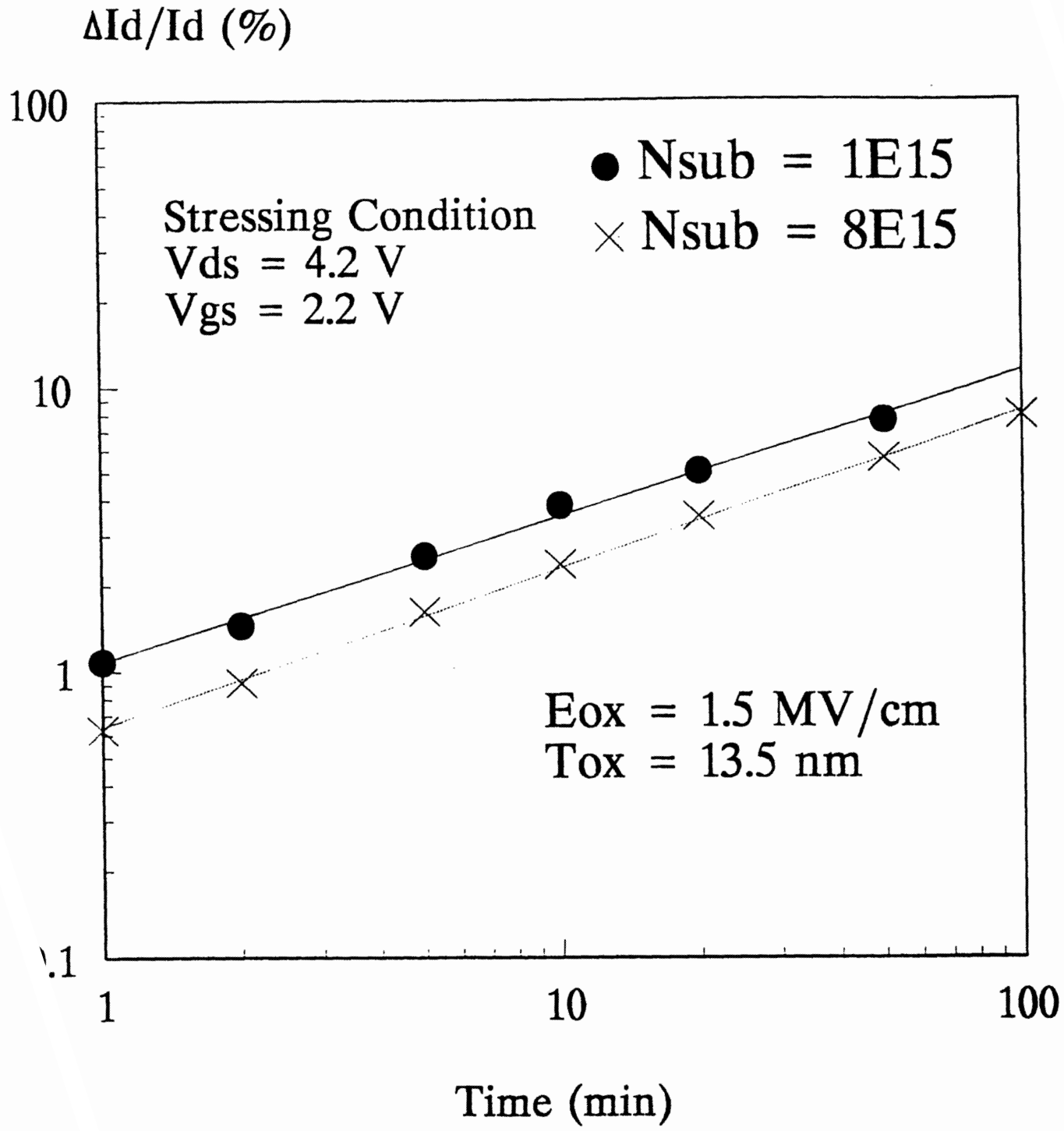

Figure 5.3 The degradation rate coefficient **n**'s dependence on N_{sub}

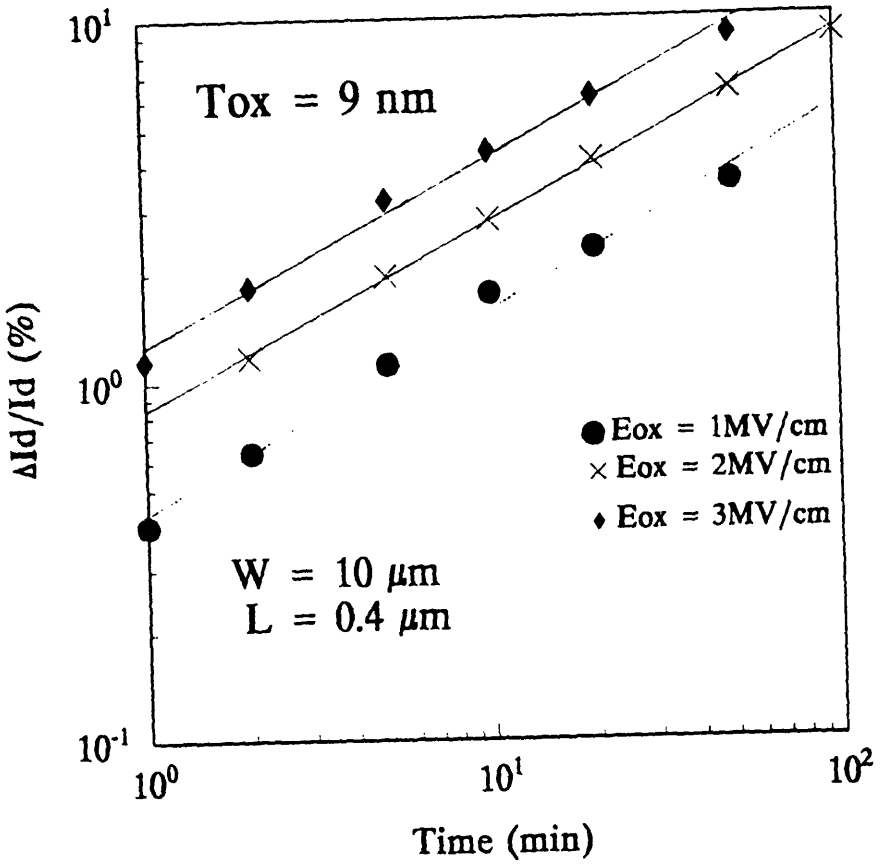

Figure 5.4 (a) The degradation rate coefficient **n**'s dependence on E_{ox} for T_{ox} = 9 nm

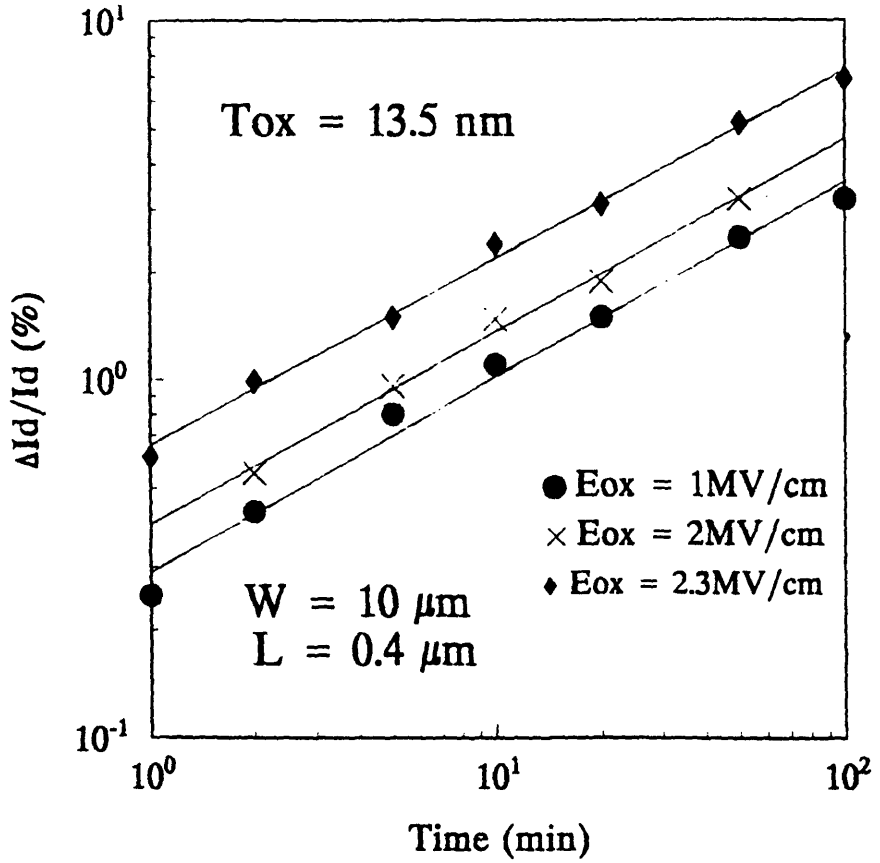

Figure 5.4 (b) The degradation rate coefficient **n**'s dependence on E_{ox} for T_{ox} = 13.5 nm

hole-traps dominate the degradation mechanisms at low V_{gs}, the interface-traps at medium V_{gs}, and the electron-traps at high V_{gs} for a fixed value of V_{ds}. The rate coefficient **n**'s dependence on the degradation mechanisms is shown in Figure 5.5. In part (a), for a fixed stressing V_{ds} = 3.9V, the V_{gs} is swept from near the V_T up to V_{ds} so that all the degradation regimes are covered. In part (b), MOSFETs with different T_{ox} is stressed. In this figure, the stressing V_{ds} = 4.5V, and, the V_{gs} swept again from low V_T up to V_{ds} value. In both figures, the rate coefficient **n** has a clear dependence on the degradation mechanism. More specifically, **n** is the highest under the interface-traps regime and is about the same for both the electron- and hole-traps regimes. The extracted **n** values for both Figure 5.5(a) and (b) are shown in Figure 5.6(a) and (b), respectively. Although its physical reason is still to be explored and researched, this dependence raises a question which value should be used in simulating the hot-electron degraded performance of circuits. The true **n** value would lie between these values because each MOSFET in the simulated circuits undergoes the hot-electron degradation by convolution of these various degradation mechanisms. Since a small inaccuracy can compound the extrapolation error as shown in Figure 5.1, a reliability engineer should be aware of the confidence limits on the lifetime prediction when extracting the degradation parameter **n** in order to simulate the hot-electron performance degradation with CAS. It is suggested, however, that the **n** value closer to the one in the interface-traps regime is used since it simulates the worst hot-electron degradation performance.

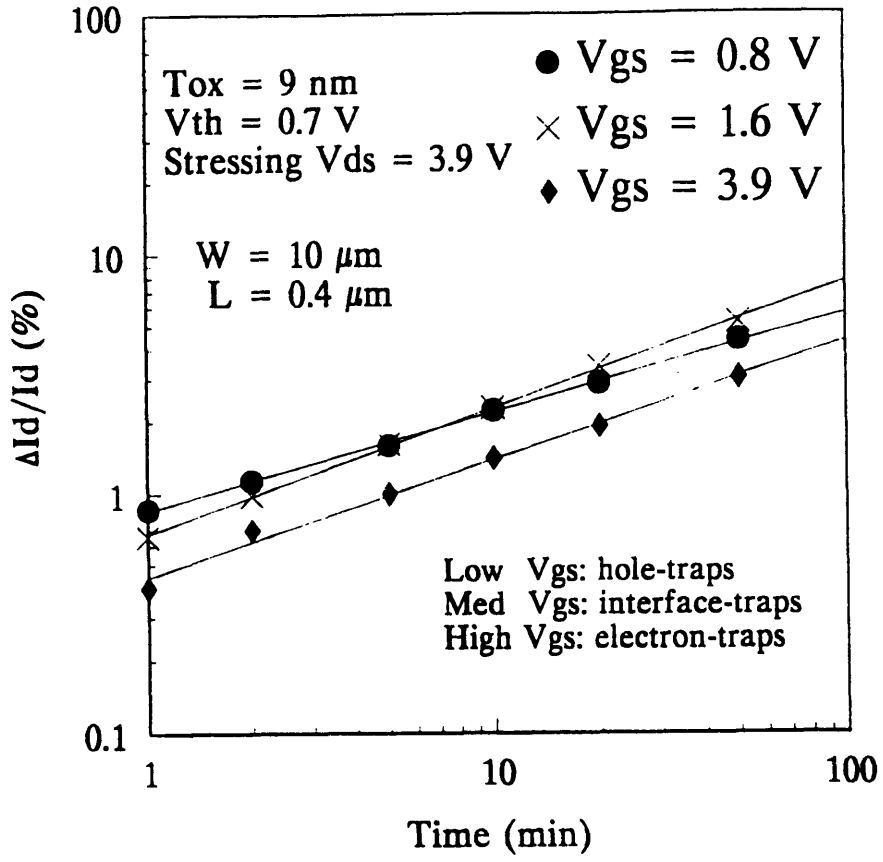

Figure 5.5 (a) n's dependence on degradation mechanisms for T_{OX} = 9 nm

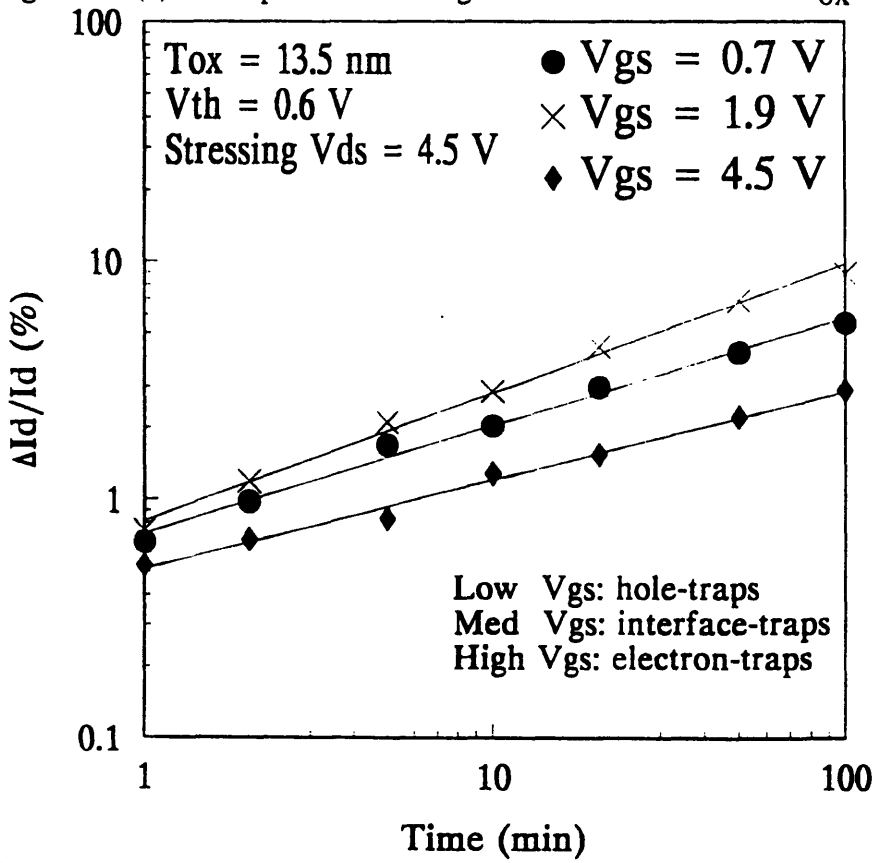

Figure 5.5 (b) n's dependence on degradation mechanisms for T_{OX} = 13.5 nm

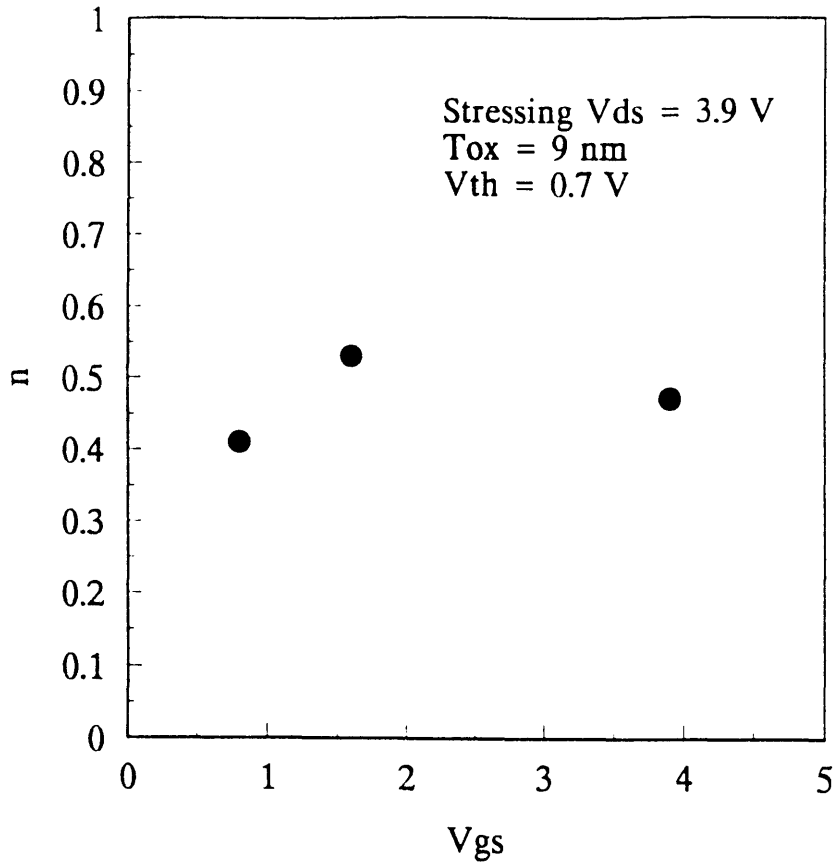

Figure 5.6 (a) Extracted **n** values in Figure 5.5 (a)

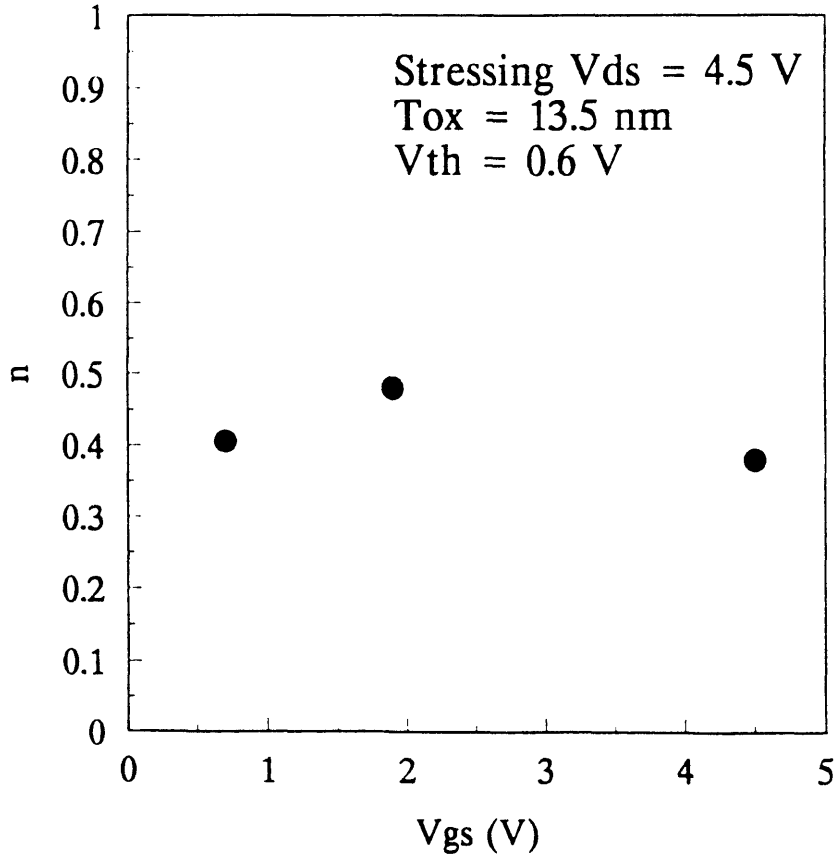

Figure 5.6 (b) Extracted **n** values in Figure 5.5 (b)

5.2.2 Parameter *m*

5.2.2.1 Oxide Thickness(T_{ox})

The extraction method of the parameter **m** was shown in Figure 2.4. Once MOSFETs are stressed at a wide enough range of $\frac{I_{sub}}{I_D}$ ratios, $\frac{\tau * I_D}{W}$ is plotted against the $\frac{I_{sub}}{I_D}$ in log-log scale, and the slope in absolute magnitude of the fitted lines corresponds to the parameter **m**. This was shown in Equation (2.12). As shown in deriving Equation (1.4), **m** is physically the ratio of the critical energy required to create the interface-traps over the critical energy to cause the impact ionization(i.e. $\mathbf{m}=\frac{\Phi_{it}}{\Phi_i}$). Since the impact ionization energy Φ_i remains constant at 1.1eV for Si, plotting the degradation parameter **m** against various MOSFET processing parameters and stressing conditions would show the Φ_{it}'s functional dependence on the MOSFET processing parameters and stressing conditions.

The Φ_{it}'s dependence on T_{ox} is shown in Figure 5.7. For all the MOSFETs that were stressed with various T_{ox}'s, the same N_{sub} is used and the E_{ox} is normalized so that the hot-electrons in the MOSFETs face the same strength of E_{ox}. In Figure 5.7(a), the lifetime correlation plot is shown to extract the parameter **m**, and in 5.7(b), the extracted **m** value is shown for each T_{ox}. The line fitting to the data is done using the least square error approximation. Although the **m** seems to be a bit lower for T_{ox} = 24 nm than for the other two T_{ox}'s, this is not statistically significant. The error is due to the scattered data points. Figure 5.7 suggests Φ_{it}'s independence on T_{ox}. The transit time for the hot-electron to travel through the gate-oxide after it crosses over the Si-SiO_2 energy barrier height is longer for the thicker T_{ox}. Therefore, the parameter **m**'s independence on T_{ox} suggests that the critical energy to create the interface-traps is not correlated with the hot-electron transit time through the gate-oxide. Physically, it seems

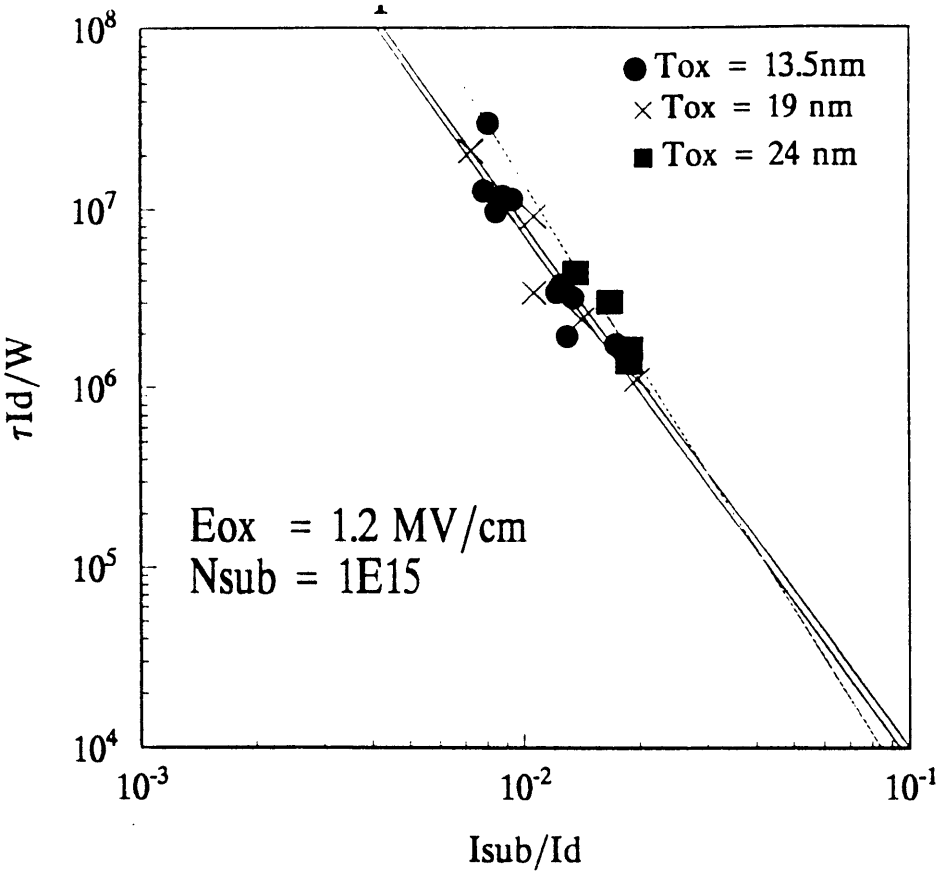

Figure 5.7(a) The parameter **m**'s dependence on T_{ox}

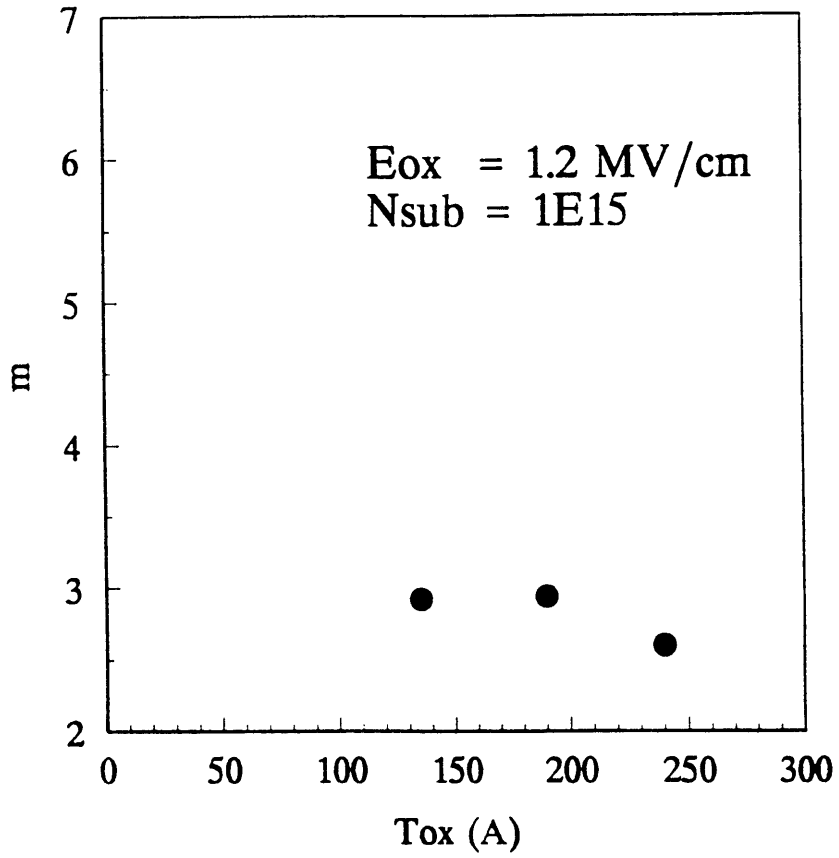

Figure 5.7(b) Extracted **m** value for each T_{ox}

to be coherent since the amount of Si-SiO2 interface damage should not be related with how long the hot-electron stays in the gate-oxide after it passes the interface.

5.2.2.2 Channel Doping Concentration(N_{sub})

The lifetime correlation plot is shown in Figure 5.8 in order to observe the degradation parameter **m**'s dependence on N_{sub}. Constant E_{ox} of 1.5 MV/cm is applied to all the stressed MOSFETs whose T_{ox}=13.5 nm in Figure 5.8(a). The slope **m** has a clear dependence on N_{sub}. Since it was found that the **m** is independent of T_{ox} in the above discussion, the data on another T_{ox} are compared in Figure 5.8(b). In Figure 5.8(b), E_{ox} is kept the same 1.5 MV/cm as in Figure 5.8(a), and T_{ox}=19 nm. In both figures, it is shown that the **m** has higher values for higher doping concentrations. The extracted **m** values in Figure 5.8(a) and (b) are plotted against the N_{sub} in Figure 5.9.

The Φ_{it}'s dependence on N_{sub} is expected because the energy band bends by different amount in the channel when the channel doping concentration is different. As the energy band, which shows the vertical electric field in the channel, bends more, the current path would be located deeper into the Si, away from the Si-SiO_2 interface, thus, making it more difficult for the hot-electrons to cross over the energy barrier at Si-SiO_2 interface. However, this is only a possible explanation since the physical reason why the energy band bends more for the heavier channel doping concentration is not explained yet. It is also possible that the Φ_{it} is greater for the higher N_{sub}, not because of the energy band bending, but because of different hot-electron degradation mechanisms. For example, it has been reported that the hot-hole-induced-interface traps are favored for the higher N_{sub}[45], and the parameter **m** is modeled as follows:

$$m = -(1 + \frac{\Phi_{it,h} * \lambda_e}{\Phi_i * \lambda_h}) \qquad (5.2)$$

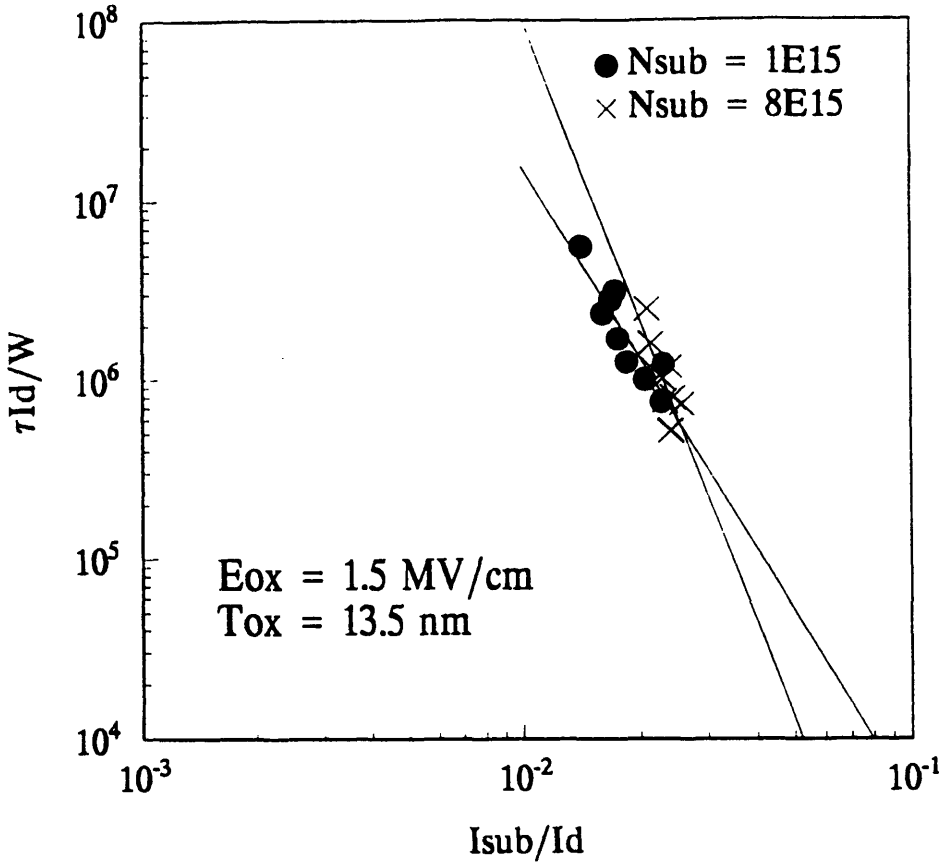

Figure 5.8(a) The parameter **m**'s dependence on N_{sub} at constant E_{ox} for T_{ox}=13.5 nm

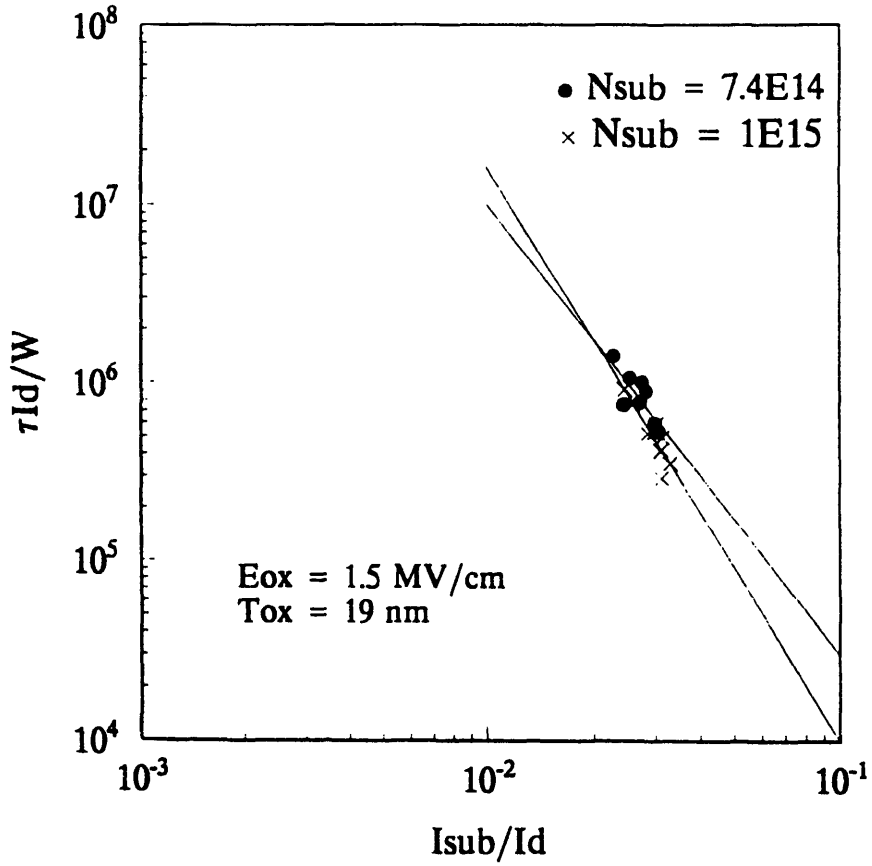

Figure 5.8(b) The parameter **m**'s dependence on N_{sub} at constant E_{ox} for T_{ox}=19 nm

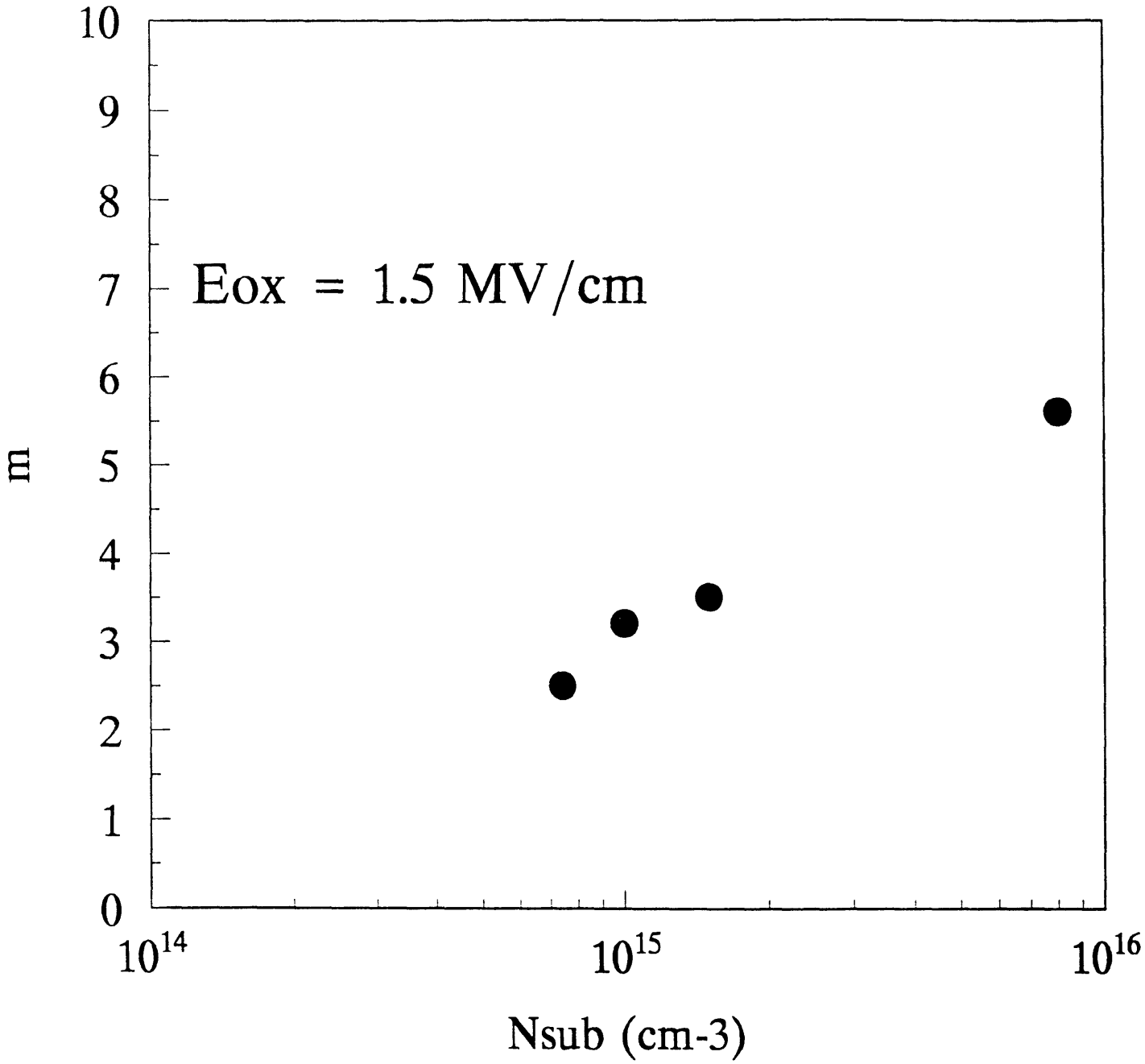

Figure 5.9 Extracted **m** values in Figure 5.8(a) and (b)

Using the model (5.2), the reported extracted **m** values are between 5 and 6, which are generally higher than those for the hot-electron-induced-interface-traps. In order to observe the carriers, electric field, and potential distributions in the stressed MOSFETs, a device simulation needs to be run with a semi-conductor device simulator, such as MINIMOS and Medici. This will help us to picture the hot-electron/hot-holes distributions and summarize the existing theories in more unified and consistent way.

5.2.2.3 Electric Field Across the Gate-oxide at the Drain(E_{ox})

In a stressing condition where $V_{gs} < V_{ds}$, which is usually the case in a circuit operation, the vertical electric field across the gate-oxide(E_{ox}) acts against the hot-electrons because the field points toward the gate terminal from the drain terminal. The stronger the E_{ox} is, the more difficult it is for the hot-electrons to cross over the energy barrier at the Si-SiO_2 interface, the more energy needed to create the interface-traps, thus, the Φ_{it} is greater. This is shown by the energy band diagram in Figure 5.10. The band diagram is drawn across the MOS structure at the drain end of the channel. As the E_{ox} becomes larger, the band bending across the oxide becomes larger. The band bending in

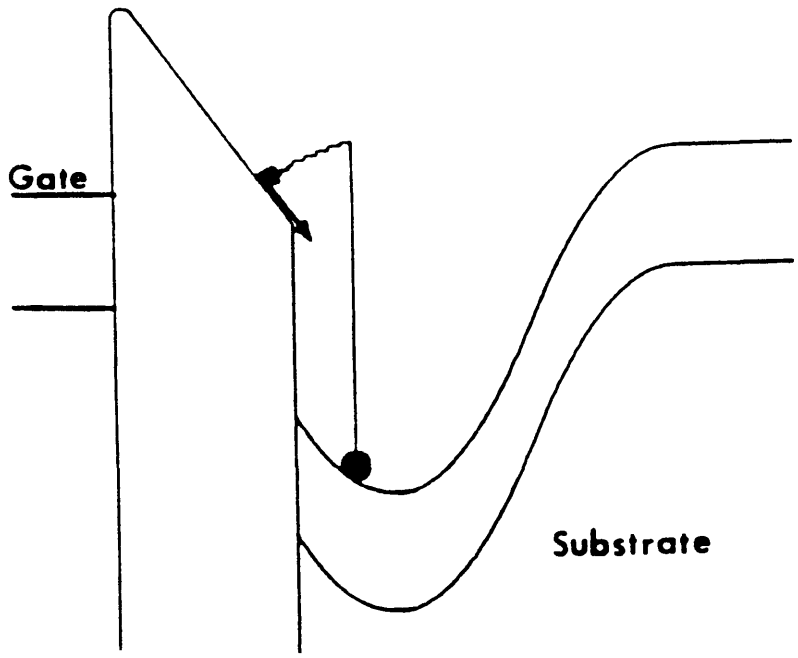

Figure 5.10 Energy band diagram across the MOS structure drawn at the drain end of the channel

the channel becomes also larger, and, as a result, the current path is further into the Si, away from the Si-SiO_2 interface. Thus, additional energy is required for the hot-electrons to approach the Si-SiO_2 interface first, and, then, to cross over the energy barrier height to create the interface-traps. This hypothesis is verified in Figure 5.11. In Figure 5.11(a), all the stressed MOSFETs are located on the same row of the same wafer, thus, having the same T_{ox} and N_{sub}. Only the stressing E_{ox} is changed. As one can see, the Φ_{it} is greater for the stronger E_{ox}. In order to verify its universality, the same test is performed on MOSFETs with different T_{ox} and N_{sub}, and with a wider range of E_{ox}. Its result is shown in Figure 5.11(b). As before, the Φ_{it} is greater for the stronger E_{ox}.

It is interesting to notice, however, that the above explanation in terms of the energy band diagram may not be complete. The Φ_{it} in Figure 5.11(b) varies more than by 2eV. It has also been reported that in LDD devices, the dependence of Φ_{it} on E_{ox} has even larger variations[31]. Although an accurate device simulation needs to be done before predicting the amount of energy band bending, it is very unlikely that the energy band will bend by more than 2eV in Si. In other words, it is strongly believed that there are some other unknown mechanisms or factors that are involved in contributing to the Φ_{it} dependence on E_{ox} besides the band bending.

In order to verify the universality of the Φ_{it} dependence on N_{sub} and E_{ox}, MOSFETs are stressed at higher E_{ox} with varying N_{sub}'s in Figure 5.12(a). T_{ox} of the chosen devices is 9 nm. Notice that the Φ_{it} is independent of T_{ox} from Section 5.2.2.1. As before, the Φ_{it} is higher for the higher N_{sub}. This result is overlaid on Figure 5.9 with previous data, and it is shown in Figure 5.12(b). It is clear that the Φ_{it} is higher for the higher N_{sub} and E_{ox}.

Although there are possible theories to explain such dependencies, it still lacks clear physical explanations. As an example, an energy band bending theory has been suggested. For another example, different degradation mechanism, namely the hot-hole-

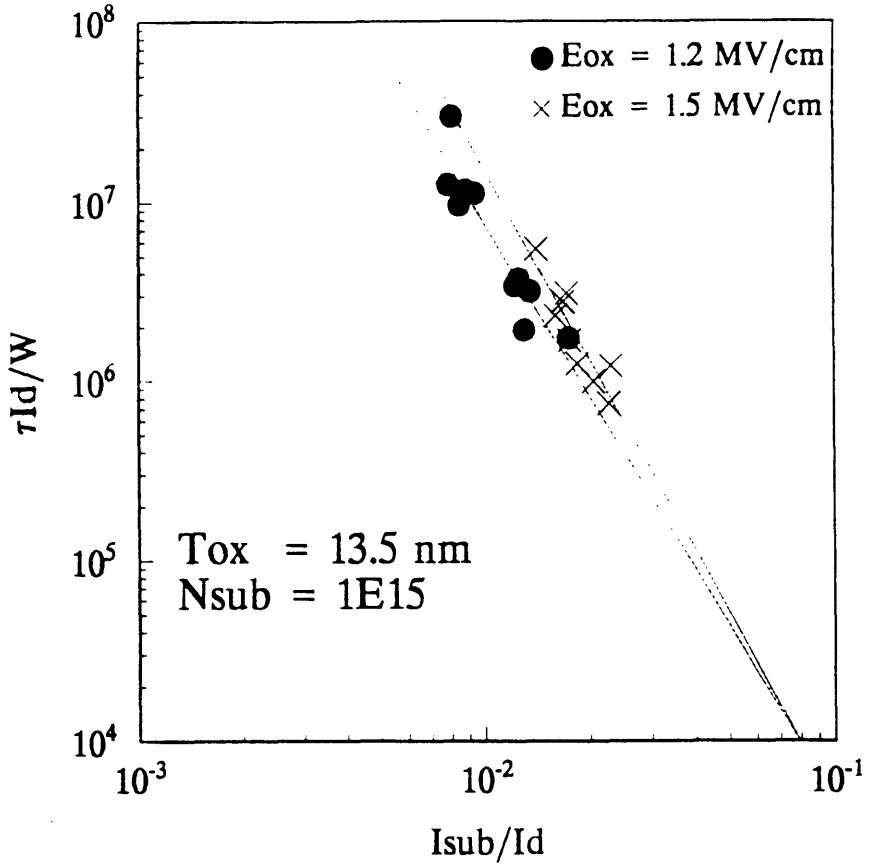

Figure 5.11(a) The parameter **m**'s dependence on E_{ox} for T_{ox}=13.5 nm

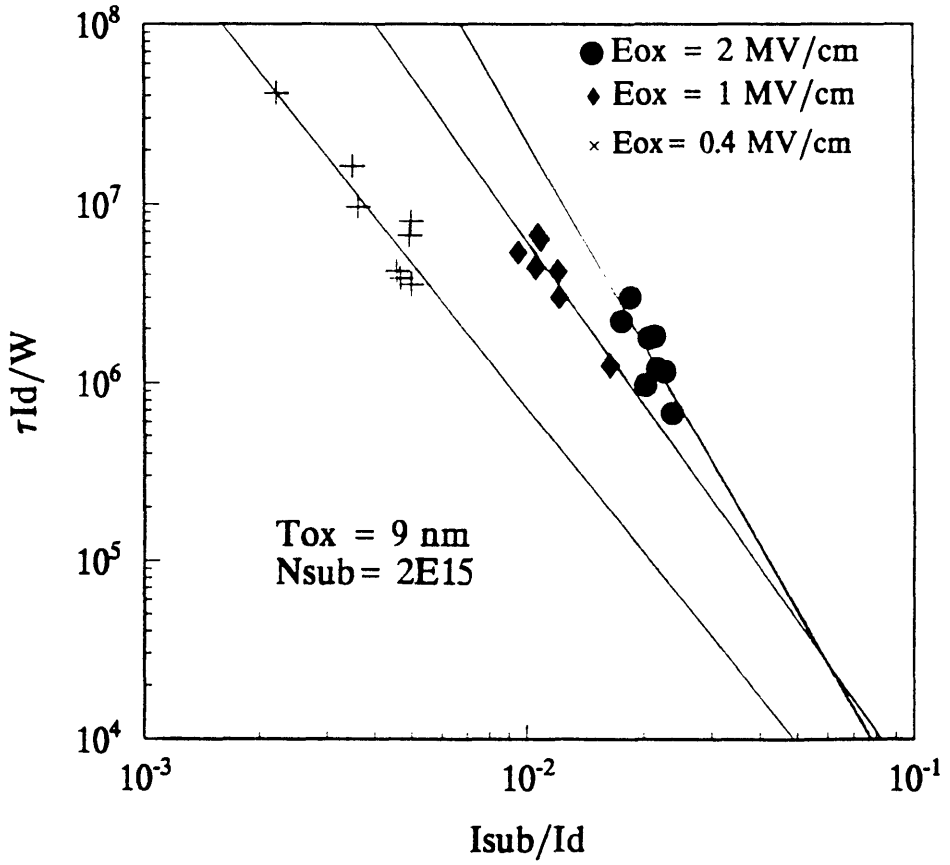

Figure 5.11(b) The parameter **m**'s dependence on E_{ox} for T_{ox}=9nm

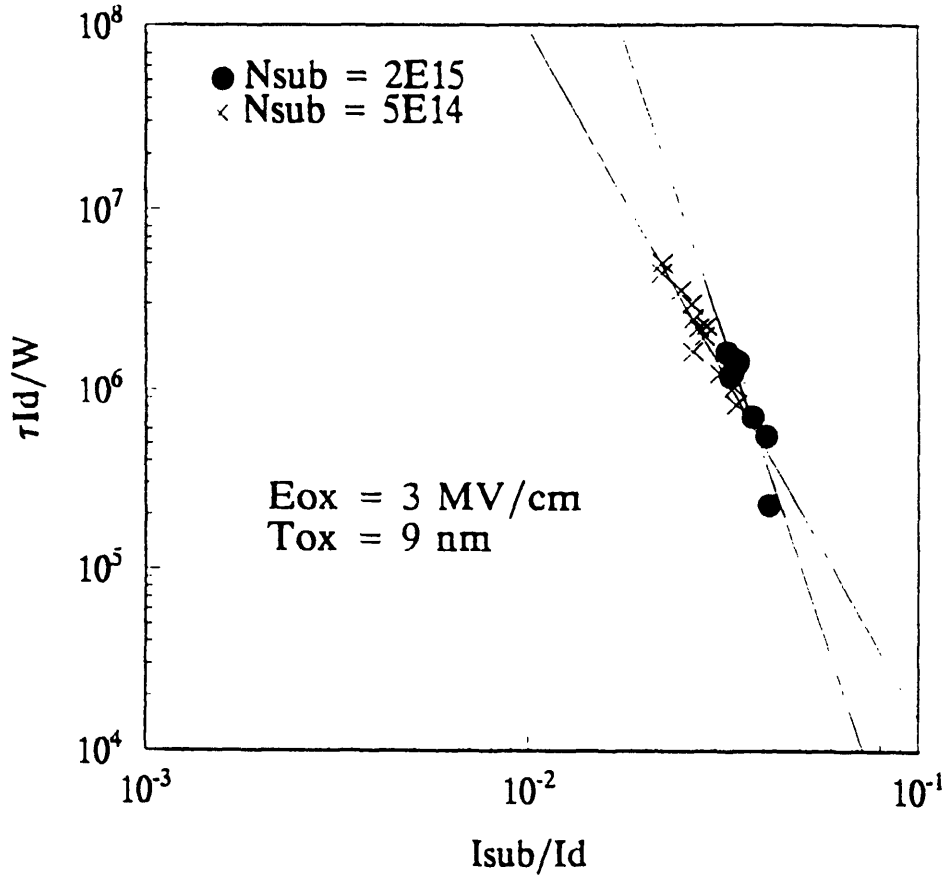

Figure 5.12(a) The parameter **m**'s dependence on N_{sub} for E_{ox}=3MV/cm

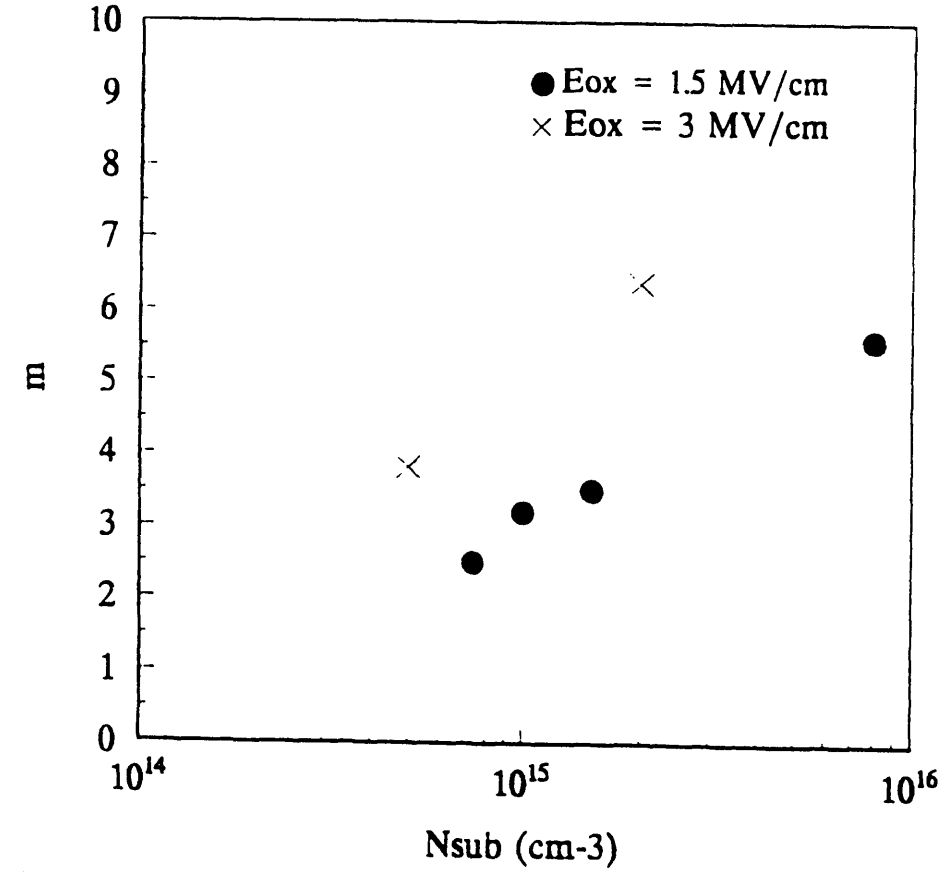

Figure 5.12(b) Extracted **m** values against N_{sub} for various values of E_{ox}

induced-interface-traps, has been suggested. However, both theories are not still clearly verified.

5.2.2.4 Substrate Bias(V_{bs})

Thus far, all the MOSFETs have been stressed with no substrate bias(V_{bs}=0V) because the maximum substrate current I_{sub} occurs at V_{bs}=0V for a given set of V_{gs} and V_{ds}. Now, in order to understand the variations of Φ_{it} physically, different V_{bs}'s have been applied. First, in order to check the Φ_{it}'s dependence on E_{ox}, the stressing E_{ox} is used as a variable and a constant V_{bs}=5V is applied. As in no substrate bias case, the Φ_{it} is larger for the higher E_{ox}. This is shown in Figure 5.13(a). In Figure 5.13(b), the Φ_{it} is compared between the stressing condition V_{bs}=0V and V_{bs}=5V. For both V_{bs}'s, the V_{gs} and V_{ds} remain the same. It is clear that the Φ_{it} is larger for the substrate bias V_{bs}=5V. The same test is performed on MOSFETs at different E_{ox}, and its result is shown in Figure 5.13(c). As in Figure 5.13(b), the Φ_{it} is larger when there is a substrate bias.

Smaller values of V_{bs} have not been tested because the V_T dependence of MOSFETs on the substrate bias is not much big as shown in the device characterization in Figure 4.3(a). In other words, the V_T for V_{bs}=3V, for example, is not much different from the V_T for V_{bs}=5V. The physical reason for such a dependence is speculated that the hot-holes are favored into the gate-oxide as V_{bs} is increased. In Figure 4.4(b), the data show that the peak of the I_{sub} curve shifts to the right as V_{bs} increases. As it moves to the right, it becomes more favorable for the hole-traps to occur[45]. If the hot-hole-induced-interface-traps are the dominant degradation mechanism, then the Φ_{it} is modeled by Equation (5.2), which generally yields higher value than $\frac{\Phi_{it}}{\Phi_i}$.

Many physical reasons for the degradation parameters **n** and **m**, which have given thus far have not been experimentally verified. The most formidable task about the experimental verification of the given theories is the difficulty of separating the numerous hot-electron degradation mechanisms from one another. MOSFETs go through the

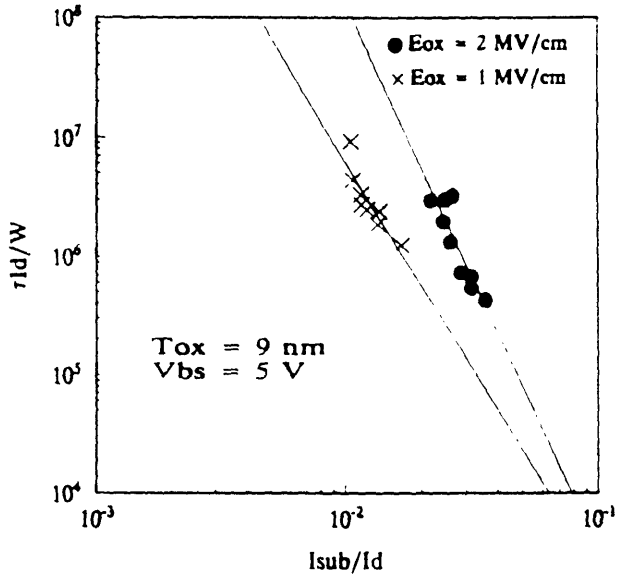

Figure 5.13(a) The parameter **m**'s dependence on E_{ox} for V_{bs}=5V

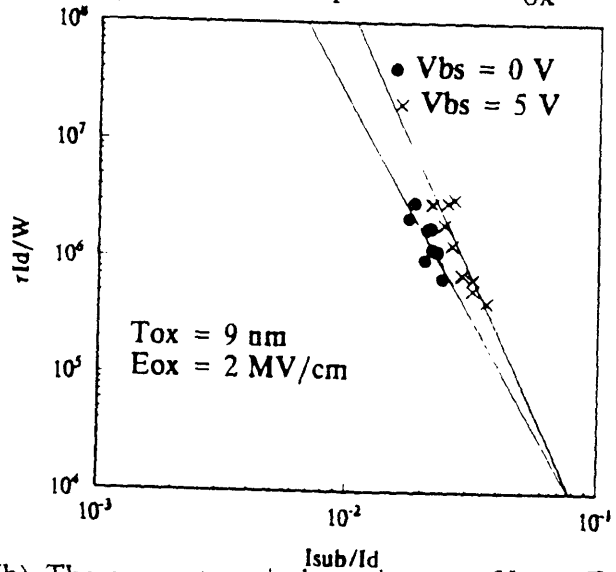

Figure 5.13(b) The parameter **m**'s dependence on V_{bs} at E_{ox}=2MV/cm

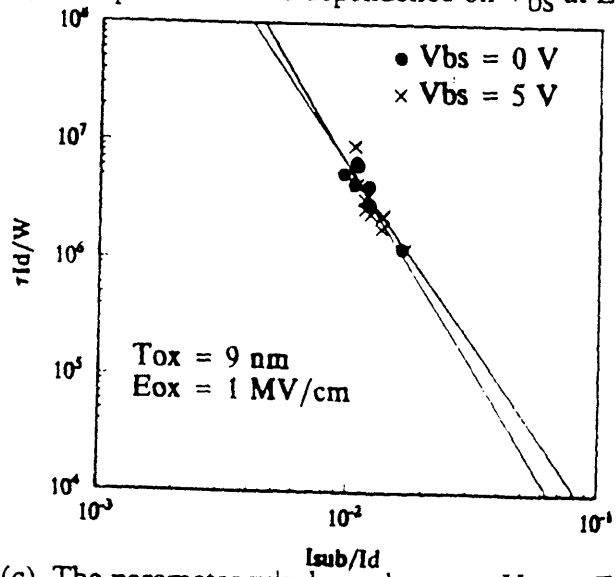

Figure 5.13(c) The parameter **m**'s dependence on V_{bs} at E_{ox}=1MV/cm

degradation dynamically through the convolution of these degradation mechanisms, and, it is unclear how to decouple the effect of each degradation mechanism to clearly understand the degradation parameters.

5.3 Summary

The hot-electron degradation parameter **n** and **m**'s dependencies on various MOSFET processing parameters, stressing conditions, and the degradation mechanisms are summarized in Table 5.1. The "yes" indicates that the degradation parameter is a function of the corresponding item, and the "no" indicates that it is not.

It has been shown that the hot-electron degradation rate coefficient **n** is not affected by any MOSFET processing parameters, such as T_{ox} and N_{sub}, and stressing conditions, such as E_{ox} and V_{bs}. Physically, it means that the degradation time acceleration factor **n** is not influenced by the hot-electron transit time through the gate-oxide, the vertical electric field in the channel, the vertical electric field across the gate-oxide, and the vertical electric field across the substrate. However, the physical reason why the time acceleration factor **n** is related by a power-law function with the device degradation(i.e. $\Delta N_{it} = A * t^n$) is further to be investigated.

It has been also shown that the degradation coefficient **m** is not affected by T_{ox} but is affected by N_{sub}, E_{ox}, V_{bs}, and degradation mechanisms. For the hot-hole-induced-interface-traps, Equation (5.2) should be used although it was not done in this thesis. Physically, it means that the critical energy to create the interface-traps(i.e. the Φ_{it}) is not influenced by the hot-electron transit time, but is influenced by the vertical electric field across the channel, the vertical electric field across the gate-oxide, and the vertical electric field across the substrate. Although the degradation parameter **H** is as important as the other two in simulating the hot-electron degraded performance of circuits, it has not been characterized for this thesis because it has no physical meaning. As mentioned before, the parameter **H** was introduced in Equation (1.4) in order to account for different processing

Parameter	T_{ox}	N_{sub}	E_{ox}	V_{bs}	Degr. Mech.
n	no	no	no	no	yes
m	no	yes	yes	yes	yes

Table 5.1 The hot-electron degradation parameter **n** and **m**'s functional dependencies on various MOSFET processing parameters, stressing conditions, and degradation mechanisms

variations so that the model can be fitted to the data. However, since the **H** is the last variable in Equation (1.4), if the correct values of the **n** and **m** are extracted, then the extracted **H** should be correct as well.

Chapter VI

Conclusion & Future Research Plan

A thorough characterization of the hot-electron degradation parameters **n** and **m** has been done for various MOSFET processing parameters, stressing conditions, and the degradation mechanisms. The goal is to develop more physical understanding of these degradation parameters so that their accurate values can be extracted for the circuit-level hot-electron degradation simulation. The third degradation parameter **H** has not been characterized since it has no physical meaning, and extracting the other two parameters accurately would lead to an accurate extraction of this parameter because it is the last variable once the **n** and **m** are acquired.

As mentioned intermittently in each section for the parameter **n** and **m**'s dependence, only partial explanation for the physical understanding is presented. The complete analysis requires device simulations, using the semi-conductor device simulator MINIMOS or Medici. This simulation will show us the carriers, electric field, and potential distributions in the MOSFET, from which the hot-electrons' distribution may be obtained. This can support more strongly only partially explained theories before. Thus, this is an immediate research plan for the upcoming semester.

Besides the device simulation, an experimental verification is necessary to complete the physical understanding. The most difficult part is to decouple the effect of each degradation mechanism on the degradation parameters. It has been reported that the technique of charge pumping current(I_{cp}) measurement can separate ΔN_{it} from charge trappings[19] to a certain extent. However, it still remains unclear how the effect of the hot-hole-induced-interface-traps on the degradation parameters can be separated from that of the hot-electron-induced-interface-traps.

The eventual goal of the research is to develop a standardized guideline to extract the hot-electron degradation parameters accurately from MOSFETs fabricated by various technologies. This will include an optimal stressing condition in order to best simulate the degradation at the circuit-level. The goal can be accomplished only after having a thorough physical understanding of the degradation parameters, and, as an initial step, their characterization has been done through extensive MOSFET stresses and measurements.

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Appendix: Process Flow for N-MOSFETs & P-MOSFETs

%% This file contains the process traveller for the 1st bulk
%% NMOS devices to be fabricated by J. Seokwon Kim.
%% There should be 5 oxide splits: 70A, 120A, 180A, 240A,
%% 300A. For each oxide thickness, there are also 3 Vt splits
%% (1V, 0.75V, 0.5V).On each wafer, there are 3 Vt splits as
%% follows
%% 1V : rows 2, 5, 8
%% 0.75V : rows 1, 4, 7
%% 0.5V : rows 3, 6
%% The oxides will be grown at the same temperature 950C

PROCESS NAME : MITICL1
LOT NAME : KIMNMOS1
OWNER : JEFFERY SEOKWON KIM

STARTING BULK WAFER : P SUBSTRATE (Boron doped, 2.5E14 cm^-3)
RESISTIVITY : 10-20 ohm-cm
Total number of wafers : 2 for each gate oxide thickness(= 10)

WAFER NAMES
70A : G7, E7, B4
120A : A1, B0, D4
180A : D3, F5, G6
240A : G4, F7, A4
300A : A2, E3, B5

* indicates a step which needs to be modified from the NMOS baseline opset

STEP #	STEP DESCRIPTION	OPSET	INFORMATION
1*	Stress Relief Oxide dsro220.set (recipe 230/A1) (950C, 38.75min in DryO2 950C, 30min in N2) Dummy #1 in for SRO monitoring, out Dummies #2,3 in; dummy #4 in, out	dsro220	standard baseline gate oxidation
2	LPCVD Silicon Nitride dnit1.5k.set (recipe 410/A5) (800C, 2hr) Dummies #2,3 for Nitride monitoring,out	dnit1-5k	standard baseline nitride deposition
3	Active Area Pattern phfieldsor.set (Mask: SOI CD Job: ICL CWR1)	phactive	standard baseline active area pattern under ../baseline directory
4	Nitride Plasma Etch plnit1.5k.set Dummy #2 in, for etch monitoring, out	plnit1-5k	standard baseline plasma nitride etch
5*	P-Field Implant (p-bulk) ipfieldlsu.set (Boron, 3E13, 25 keV) dummy #4 and its twin in, out	ipfieldkim	dose is changed from the baseline

```
6   Resist Ash                          phash
    ash.set


7   Field Oxide                         dfield5-1k      standard baseline
    Tox = 5000A                                         field oxidation
    Dummy #4 in for fox monitoring, out

8   Nitride Wet Etch                    wnit1-5k        standard baseline
    wnit1.5k.set                                        nitride wet etch
    Dummy #3 in for etch monitoring, out


9       Stress Relief Oxide Wet Etch                    Number wafers _______
        wsro220.set                                     Opset start   _______
                                                        Opset finish  _______
        Dummy #1 in for SRO etch monitoring, out

10*     Dummy Gate Oxide Growth                         Number wafers _______
        dgate120.set (recipe 112/A2)                    Opset start   _______
        (900C, 25min in DryO2                           Opset finish  _______
         900C, 25min in N2)
        Dummy #5 in for oxide monitoring, out
        Dummies #6 & #7 in, out

****************(repeat 11,12,13 for implant splits)******************
11*     Channel Implant Pattern                         Number wafers _______
        phchannel.set                                   Opset start   _______
        (Mask: no mask                                  Opset finish  _______
         Job: LSU,4 for HI  vt)
              LSU,9 for MED vt)
        Decide channel implant dose now using known dummy oxide thick-
        ness and SUPREM, so as to have non-fully depleted mode for
        higher dose implants, lower dose implant and intrinsic are
        fully depleted modes.

12*     Channel Implant                                 Number wafers _______
        ipvtlsu.set                                     Opset start   _______
        (BF2, 40keV, 3E12 for HI vt)                    Opset finish  _______
        (BF2, 40keV, 1E12 for MED vt)
        (no implants for low vt)
        Dummies #6 & #7 in, out

13      Resist Ash                                      Number wafers _______
        ash.set                                         Opset start   _______
                                                        Opset finish  _______

****************(repeat 11,12,13 for implant splits)******************

14      Dummy Gate Wet Etch                             Number wafers _______
        wgate120.set                                    Opset start   _______
        Dummy #5 in for etch monitoring, out            Opset finish  _______
        Dummies #6 & #7 in
****************(repeat 15 for gate-oxide splits)**********************
15*     Gate Oxide                                      Number wafers _______
        dgate109.set (recipe 112/A2)                    Opset start   _______
        (900C, 25min in DryO2                           Opset finish  _______
         900C, 25min in N2)
        Dummies #6 & #7 out
        Dummies #8 & #9 in for oxide monitoring
        Dummy #10 in, out
****************(repeat 15 for gate-oxide splits)**********************
```

16* LPCVD Polysilicon — Number wafers _____
poly3k.set (recipe 428/A6) — Opset start _____
(625C) — Opset finish _____
Dummies #8 & #9 for poly monitoring, out
Dummy #11 in, out

17 Poly Gate Pattern — Number wafers _____
phpolylsu.set — Opset start _____
(Mask: SOI CP — Opset finish _____
Job: ICL CD1)

18 Plasma Poly Etch — Number wafers _____
plpoly3k.set — Opset start _____
Dummy #8 in for etch monitoring, out — Opset finish _____

19 Resist Ash — Number wafers _____
ash.set — Opset start _____
Opset finish _____

20 N+ Poly/S/D Pattern — Number wafers _____
phn+lsu.set — Opset start _____
(Mask: SOI CN+ — Opset finish _____
Job: ICL CP1)

21* Poly And S/D Implant — Number wafers _____
inpsdhao.set — Opset start _____
(As: 25kev,4e15) — Opset finish _____
Dummies #10 & #11 in, out

22 Resist Ash — Number wafers _____
ash.set — Opset start _____
Opset finish _____

23 P+ Poly/S/D Pattern — Number wafers _____
pp+lsu.set — Opset start _____
(Mask: SOI CP+ — Opset finish _____
Job: ICL CD1)

24* P+ Sub Contact Implant — Number wafers _____
innsdlsu.set — Opset start _____
(BF2: 25kev,4e15) — Opset finish _____
Dummy #9 in, out

25 Resist Ash — Number wafers _____
ash.set — Opset start _____
Opset finish _____

26* Poly And S/D Diffusion — Number wafers _____
ddrivehao.set (recipe 113/B5) — Opset start _____
(900C, 15min in Dry O2) — Opset finish _____
(900C, 5 min in N2)
Dummies #6,#7,#9,#10 & #11 in,out
Dummy #10 for oxide increase (beyond gate oxide) monitoring

27* LTO Deposition — Number wafers _____
dlto4k.set (recipe 437/A7, 400C) — Opset start _____
Dummies #12 &#13 in for LTO monitoring — Opset finish _____

28 LTO densification
dann.set (recipe 806/B5) — Number wafers _____
(950C, 30min in N2) — Opset start _____
Dummies #12 & #13 out — Opset finish _____
Dummies #6,#7,#9,#10 & #11 in,out

29 Resist Coat
phcoat.set

Number wafers _____
Opset start _____
Opset finish _____

30 Backside LTO Wet Etch
wlto4k.set

Number wafers _____
Opset start _____
Opset finish _____

Dummies #6 & #7 in for channel doping monitoring, out
Dummy #9 in for P + sub contact doping monitoring, out
Dummy #10 in for S/D doping monitoring, out
Dummy #11 in for poly doping monitoring, out

31 Backside Poly Plasma Etch
plpoly3k.set
(CCL4, 45sec/8sec)

Number wafers _____
Opset start _____
Opset finish _____

32 Backside Oxide Wet Etch
wox5k.set

Number wafers _____
Opset start _____
Opset finish _____

33 Resist Ash
ash.set

Number wafers _____
Opset start _____
Opset finish _____

34 Contact Pattern
phconthao.set
(Mask: SOI CC
Job: ICL CP1)

Number wafers _____
Opset start _____
Opset finish _____

35 LTO Plasma Etch
pllto4k.set
(CF4)

Number wafers _____
Opset start _____
Opset finish _____

Dummies #12 & #13 in for etch monitoring

36 LTO Wet Etch
wlto4k.set

Number wafers _____
Opset start _____
Opset finish _____

Dummies #12 & #13 for etch monitoring, out

37 Resist Ash
ash.set

Number wafers _____
Opset start _____
Opset finish _____

38 Metal Deposition (Al)
cvclugc.set
(Use Varian.set)

Number wafers _____
Opset start _____
Opset finish _____

Dummy #14 in for metal monitoring, out

39 Metal Pattern
phmetlsu.set
(Mask: SOI CM1
Job: ICL CC)

Number wafers _____
Opset start _____
Opset finish _____

40 Metal Plasma Etch
plmetal.set

Number wafers _____
Opset start _____
Opset finish _____

41 Resist Ash
ash.set

Number wafers _____
Opset start _____
Opset finish _____

42 Sinter Metal
dsinter.set (recipe 710/B8)
(400C, 40min in H2+N2)

Number wafers _____
Opset start _____
Opset finish _____

PROCESS NAME : MITICL2
LOT NAME : KIMPMOS1
OWNER : JEFFERY SEOKWON KIM

STARTING BULK WAFER : N SUBSTRATE (P DOPED, 2.5E14 cm-3)
RESISTIVITY : 10-20 ohms

WAFER NAMES
70A : G1, H1
120A : E6, D6
180A : C4, C0
240A : G2, F2
300A ; C7, B5

* indicates a step which needs to be modified from the PMOS baseline opset

STEP #	STEP DESCRIPTION	STATUS
1*	Stress Relief Oxide dsro220.set (recipe 230/A1) (950C, 38.75min in DryO2 950C, 30min in N2) Dummy #1 in for SRO monitoring, out Dummies #2,3 in; dummy #4 in, out	Number wafers _____ Opset start _____ Opset finish _____
2	LPCVD Silicon Nitride dnit1.5k.set (recipe 410/A5) (800C, 2hr) Dummies #2,3 for Nitride monitoring,out	Number wafers _____ Opset start _____ Opset finish _____
3	Active Area Pattern phfieldsor.set (Mask: SOI CD Job: ICL CWR1)	Number wafers _____ Opset start _____ Opset finish _____
4	Nitride Plasma Etch plnit1.5k.set Dummy #2 in, for etch monitoring, out	Number wafers _____ Opset start _____ Opset finish _____
5	N-Field Implant (N-bulk) infieldpkt.set (Phos, 3E12, 40 keV)	Number wafers _____ Opset start _____ Opset finish _____
6	Resist Ash ash.set	Number wafers _____ Opset start _____ Opset finish _____
7*	Field Oxide (fox+SRO:3500A SiO2 for 1st thining)	Number wafers _____

```
8       Nitride Wet Etch                          Number wafers _____
        wnit1.5k.set                              Opset start   _____
        Dummy #3 in for etch monitoring, out      Opset finish  _____


9       Stress Relief Oxide Wet Etch              Number wafers _____
        wsro220.set                               Opset start   _____
                                                  Opset finish  _____
        Dummy #1 in for SRO etch monitoring, out

10*     Dummy Gate Oxide Growth                   Number wafers _____
        dgate120.set (recipe 112/A2)              Opset start   _____
        (900C, 25min in DryO2                     Opset finish  _____
         900C, 25min in N2)
        Dummy #5 in for oxide monitoring, out
        Dummies #6 & #7 in, out

****************(repeat 13,14,15 for implant splits)******************
11*     Channel Implant Pattern                   Number wafers _____
        phchannel.set                             Opset start   _____
        (Mask: no mask                            Opset finish  _____
         Job: LSU,4 for HI  vt)
              LSU,9 for MED vt)
              LSU,1 for LOW vt)

12*     Channel Implant                           Number wafers _____
        ipvtlsu.set                               Opset start   _____
        (Phos, 40keV, 3e12 for HI vt)             Opset finish  _____
        (Phos, 40keV, 1.5e12 for MED vt)
        (Phos, 40keV, 9e11  for LOW vt)
        Dummies #6 & #7 in, out

13      Resist Ash                                Number wafers _____
        ash.set                                   Opset start   _____
                                                  Opset finish  _____

****************(repeat 13,14,15 for implant splits)******************

14      Dummy Gate Wet Etch                       Number wafers _____
        wgate120.set                              Opset start   _____
        Dummy #5 in for etch monitoring, out      Opset finish  _____
        Dummies #6 & #7 in


***************(repeat 15 for gate-oxide split)************************

15*     Gate Oxide                                Number wafers _____
        [ dgate45.set (recipe 226/A2) (45A)       Opset start   _____
            (800C, 30min in DryO2                 Opset finish  _____
             800C, 15min in N2)
          dgate100.set (recipe 236/A2)(100A)
            (950C, 12min in DryO2
             950C, 12min in N2)
          dgate235.set (for 150A)
          dgate230.set (for 230A)
          dgate238.set (for 300A)]

        Dummies #6 & #7 out
```

16* LPCVD Polysilicon — Number wafers _____
poly3k.set (recipe 428/A6) — Opset start _____
(625C) — Opset finish _____
Dummies #8 & #9 for poly monitoring, out
Dummy #11 in, out

17 Poly Gate Pattern — Number wafers _____
phpolylsu.set — Opset start _____
(Mask: SOI CP — Opset finish _____
Job: ICL CD1)

18 Plasma Poly Etch — Number wafers _____
plpoly3k.set — Opset start _____
Dummy #8 in for etch monitoring, out — Opset finish _____

19 Resist Ash — Number wafers _____
ash.set — Opset start _____
Opset finish _____

20* Poly And S/D Implant — Number wafers _____
inpsdhao.set — Opset start _____
(BF2: 25kev,4e15) — Opset finish _____
Dummies #10 & #11 in, out

21* Poly And S/D Diffusion — Number wafers _____
ddrivehao.set (recipe 113/B5) — Opset start _____
(900C, 15min in Dry O2) — Opset finish _____
(900C, 5 min in N2)
Dummies #6,#7,#9,#10 & #11 in,out
Dummy #10 for oxide increase (beyond gate oxide) monitoring

22* LTO Deposition — Number wafers _____
dlto4k.set (recipe 437/A7, 400C) — Opset start _____
Dummies #12 &#13 in for LTO monitoring — Opset finish _____

23 LTO densification
dann.set (recipe 806/B5) — Number wafers _____
(950C, 30min in N2) — Opset start _____
Dummies #12 & #13 out — Opset finish _____
Dummies #6,#7,#9,#10 & #11 in,out

24 Resist Coat — Number wafers _____
phcoat.set — Opset start _____
Opset finish _____

25 Backside LTO Wet Etch — Number wafers _____
wlto4k.set — Opset start _____
Opset finish _____
Dummies #6 & #7 in for channel doping monitoring, out
Dummy #9 in for N+ sub contact doping monitoring, out
Dummy #10 in for S/D doping monitoring, out
Dummy #11 in for poly doping monitoring, out

26 Backside Poly Plasma Etch — Number wafers _____
plpoly3k.set — Opset start _____
(CCL4, 45sec/8sec) — Opset finish _____

27 Backside Oxide Wet Etch — Number wafers _____
wox5k.set — Opset start _____

```
;;; This lot contains 5 oxide splits(70A, 120A, 180A, 240A, 300A)
;;; On each wafer, there are three Vt splits.
;;;  Vt = 1V    on rows 2, 5, 8
;;;  Vt = 0.75V on rows 1, 4, 7
;;;  Vt = 0.5V  on rows 3, 6

(fl-load "/homes/jskim/MOSFET/NMOS/PFR/lib-loc.fl")
(fl-library :database)
(fl-load "constants.fl")
(fl-load "utils.fl")
(fl-load "masks.fl")

(define MITICL1
  (flow
    (:doc "MITICL1 - NMOS lot with 5 oxide splits")
    (:version
       (:modified  :number 1.0 :by "Jeffery Seokwon Kim"  :date "Jan. 31,1994"
                   :what "NMOS lot"))
    (:body
      (flow
         dsro220
         LPCVD-SILICON-NITRIDE
         (phactive :mask SOI_CD :mask-id "SOI_CD"  :dswjob "ICL_CWR1")
         NITRIDE-PLASMA-ETCH
         ipfieldkim
         RESIST-ASH
         FIELD-OXIDE
         NITRIDE-WET-ETCH
         wsro220
         dgate120
         (flow
           (:wafers ("G7" "E7" "B4"))
           (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-4")
           chan1h
           RESIST-ASH
           (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-9")
           chan1m
           RESIST-ASH
           (phjoblsu : mask EMPTY ;mask-id "EMPTY"  ;dswjob "LSU-7")
           chan1l)
         (flow
           (:wafers ("A1" "B0" "D4"))
           (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-4")
           chan2h
           RESIST-ASH
           (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-9")
           chan2m
           RESIST-ASH
           (phjoblsu : mask EMPTY ;mask-id "EMPTY"  ;dswjob "LSU-7")
           chan2l)
         (flow
           (:wafers ("D3" "F5" "G6"))
           (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-4")
           chan3h
           RESIST-ASH
           (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-9")
```

```
  chan3m
  RESIST-ASH
  (phjoblsu : mask EMPTY ;mask-id "EMPTY"  ;dswjob "LSU-7")
  chan3l)
(flow
  (:wafers ("G4" "F7" "A4"))
  (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-4")
  chan4h
  RESIST-ASH
  (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-9")
  chan4m
  RESIST-ASH
  (phjoblsu : mask EMPTY ;mask-id "EMPTY"  ;dswjob "LSU-7")
  chan4l)
(flow
  (:wafers ("A2" "E3" "B5"))
  (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-4")
  chan5h
  RESIST-ASH
  (phjoblsu : mask EMPTY :mask-id "EMPTY"  :dswjob "LSU-9")
  chan5m
  RESIST-ASH
  (phjoblsu : mask EMPTY ;mask-id "EMPTY"  ;dswjob "LSU-7")
  chan5l)
RESIST-ASH
wgate120
(flow
  (:wafers ("G7" "E7" "B4"))
  gate70)
(flow
  (:wafers ("A1" "B0" "D4"))
  gate120)
(flow
  (:wafers ("D3" "F5" "G6"))
  gate180)
(flow
  (:wafers ("G4" "F7" "A4"))
  gate240)
(flow
  (:wafers ("A2" "E3" "B5"))
  gate300)
poly3k
(phpoly :mask SOI_CP :mask-id "SOI_CP" :dswjob "ICL_CD1")
plpoly3k
RESIST-ASH
innsdkim
drivekim
lto4k
TOP-RESIST-COAT
wlto4k
plpolybk
wbkox
RESIST-ASH
(phcont :mask SOI_CC :mask-id "SOI_CC" :dswjob "ICL_CP1")
pllto4k
wlto
RESIST-ASH
METAL-DEPOSITION
(phmetal :mask SOI_CM1 :mask-id "SOI_CM1" :dswjob "ICL_CC")
METAL-PLASMA-ETCH
RESIST-ASH
SINTER))))
```