A Mechanical Model for Erosion in Copper Chemical-Mechanical Polishing

Kyungyoon Noh, Nannaji Saka and Jung-Hoon Chun
Laboratory for Manufacturing and Productivity
Massachusetts Institute of Technology

Abstract—**The Chemical-mechanical polishing (CMP) process is now widely employed in the ultralarge scale integration chip fabrication. Due to the continuous advances in semiconductor fabrication technology and decreasing sub-micron feature size, the characterization of erosion, which affects circuit performance and manufacturing throughput, has been an important issue in Cu CMP. In this paper, the erosion in Cu CMP is divided into two levels. The wafer-level and die-level erosion models were developed based on the material removal rates and the geometry of incoming wafers to the Cu CMP process, including the Cu interconnect area fraction, linewidth and Cu deposition thickness. Experiments were conducted to obtain the selectivity values between the Cu, barrier layer and dielectric, and the values of within-wafer material removal rate ratio, β, for the validation of the new erosion model. It was compared with the existing models and was found to agree better with the experimental data.**

Index Terms— **Chemical Mechanical Polishing, Erosion, Semiconductor Manufacturing**

I. INTRODUCTION

CONTINUING advances in ultra-large-scale integration technology necessitate the design and fabrication of extremely small features of higher resolution, denser packing and multi-layer interconnects. Recently, copper has emerged as the optimal interconnect material because of its low electrical resistivity and great resistance to electromigration. Patterned Cu lines are produced by a damascene scheme involving oxide trench patterning and Cu deposition followed by chemical-mechanical polishing (CMP). The current success in producing high resolution interconnects is due to the excellent local and global planarization capabilities of the Cu CMP process.

Fig. 1 schematically shows a single Cu interconnect layer structure before and after CMP. A diffusion barrier layer and Cu are deposited on the etched dielectric trenches as shown in Fig. 1(a). Then the Cu CMP process is employed to remove excess Cu and the diffusion barrier layer without excessive loss of interconnect lines and the dielectric. It has been reported in the literature that the material removal rate in the Cu CMP process is related to the local pattern geometry and material being polished [1-5]. Although the ideal Cu CMP process finishes polishing the excess Cu and barrier layer at the same time over the entire wafer as shown in Fig. 1(b), there often exists a non-uniformity in the real case, as shown in Fig. 1(c), caused by different material removal rate for each layer material and the underlying pattern geometry. Since the end-point of the Cu CMP process occurs when the excess Cu and barrier layer is removed completely, there are overpolished dielectric areas, and resulting dielectric thinning or so-called erosion. Moreover, because the soft interconnect Cu is polished faster than the hard dielectric material, the Cu line is dished, i.e., there exists a relative height difference between Cu interconnect line and the adjacent dielectric material as shown in Fig. 1(c).

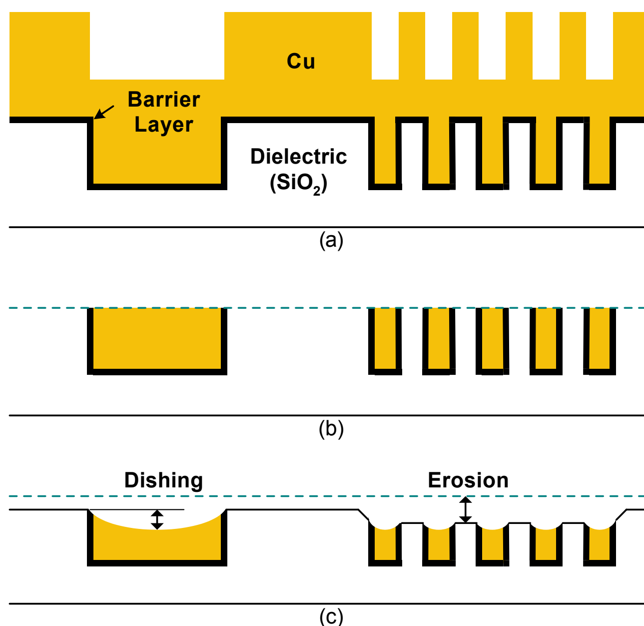

Fig. 1. Schematics of a single Cu interconnect layer of (a) before polishing and after polishing (b) ideal case (c) real case (there exist non-uniformities due to the different material and pattern geometries)

The dishing and erosion in Cu CMP reduce the thickness of both dielectric and Cu interconnects and results in surface non-planarity, which can significantly affect the chip performance. Thus, the mechanisms of dishing and erosion must be determined and their impact on process yield must be addressed.

The material removal rate in CMP is expressed by the Preston equation [6], which can be written as:

Kyungyoon Noh is a Ph.D. candidate in the Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A. (phone: 617-253-2108; fax: 617-253-2123; e-mail: kyno@mit.edu)

Dr. Nannaji Saka is a principal research scientist in the Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A. (e-mail: nsaka@mit.edu)

Prof. Jung-Hoon Chun is a professor in the Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A. (e-mail: jchun@mit.edu)

$$\left|\frac{dh}{dt}\right| = k_p \cdot p \cdot v_R \quad (1)$$

where h is the thickness of the layer removed, t the polishing time, p the nominal pressure, v_R the relative velocity, and k_p a constant known as the Preston constant. In recent years, it has been demonstrated that the above relation is also valid for metals [1, 5, 7] as well as ceramics [8]. The Preston equation describes the local material removal rate for each point on a wafer. Thus, the Preston constant can be different for each point on a wafer, and is affected by the hardness of the material being polished, abrasive size, slurry chemicals and slurry transport. Also, the local pressure and relative velocity distribution must be known.

Dishing and erosion problems in Cu CMP have been addressed in several studies [2, 3]. It has been reported that erosion is more significant than dishing in the small Cu interconnect linewidth regions, such as device level features, and that dishing is more important than erosion in the large Cu linewidth region of top layers of a multi-level Cu damascene structure. The continuous advances in semiconductor fabrication technology and decreasing sub-micron feature size make it more important to characterize the erosion in Cu CMP.

Due to the complexity of material removal by mechanical, chemical and chemomechanical interactions in the CMP process, previous efforts to characterize the relationship between erosion and process parameters are confined to experimental characterizations and parametric studies on such pattern parameters as area fraction and linewidth [4, 7, 9, 10]. Though a few semi-quantitative models have been proposed [2, 3], the fundamentals of erosion and its relation to pattern geometry and material properties in the Cu CMP process are still not fully understood.

In this study, a systematic way of characterizing and modeling erosion in Cu CMP is presented. An erosion prediction scheme based on the local pressure distribution to focus on the mechanical aspects of the polishing process is suggested. Moreover, a theoretical framework for relating the process parameters to wafer-level and die-level erosion is established.

II. Theory

A. Definition of erosion

Every point on a wafer has a different material removal rate due to different chemical effects, pressure, relative velocity, slurry transportation and initial topography. The material removal rate in the Preston equation contains the local information for the Preston constant, pressure and relative velocity rather than wafer-level mean values. This means that the local information should be addressed first when the material removal rate in Cu CMP is considered.

The ideal Cu CMP process completely removes the excess Cu and the barrier layer at the same time over the entire wafer, and ends before removing the dielectric pattern as shown in Fig. 1(b). But it is well known that material removal rates differ between any two points on a wafer because of the non-uniform process parameters. Because the end-point of the Cu CMP process should be the time when all of the excess copper and barrier layer are completely removed, there are always other overpolished regions. Erosion in Cu CMP is defined as the amount of overpolished dielectric thickness with respect to the original dielectric film thickness as shown in Fig. 2.

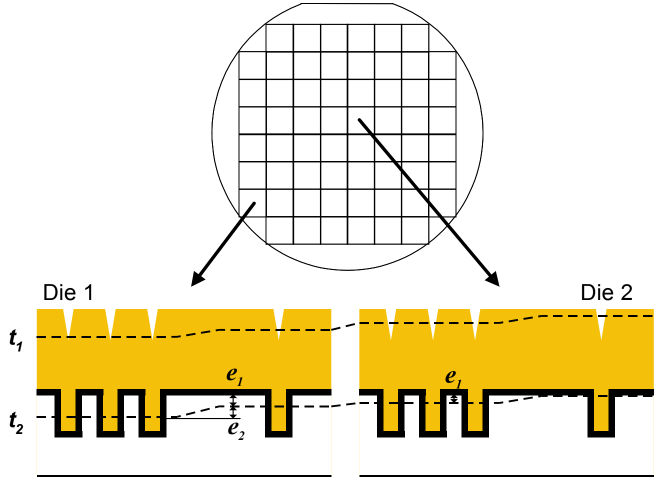

Fig. 2. Time evolution of a polishing surface at two different dies in a wafer during CMP process, which accounts for wafer-level erosion, e_1, and die-level erosion, e_2: material removal rate in die 1 is higher than that of die 2.

Because the erosion in Cu CMP is due to the different material removal rates between two points on a wafer, it is essential to consider the thickness change of any two points on a wafer for the erosion characterization. Fig. 2 shows time evolution of polishing surface at two different dies on a wafer during the Cu CMP process. The material removal difference causes non-uniformities at two levels: wafer-level and die-level. To characterize wafer-level non-uniformity, two points, which are located on the different dies but have the same feature pattern geometries are considered. Whenever each feature of same pattern geometry on Die 1 and Die 2 are compared, Die 1 will always be polished faster than Die 2 because of its higher material removal rate. To characterize die-level non-uniformity, two different feature pattern geometries on the same die are considered. At a certain time, two different features on a die will have different material removal rates. Generally, a feature with a large area fraction of Cu interconnect lines will be polished faster than a feature with a small area fraction.

In this study, based on the schematics in Fig. 2, wafer and die-level erosion are defined as e_1 and e_2, respectively. e_1 is defined as the amount of overpolishing from the original dielectric thickness with respect to a local reference point. The local reference point can be any point which has same pattern feature in each die. e_2 is defined as the dielectric layer thickness difference with respect to each local reference point, which is mainly dependent on the pattern geometry. The blanket area of each die is considered as a local reference point.

B. Effect of relative velocity

To consider the kinematics of the Cu CMP process, a coordinate system for a rotary polisher is shown in Fig. 3. The rotational centers of the wafer and the platen are $O_w$and O_p, and the angular velocities are ω_w and ω_p, respectively. The two

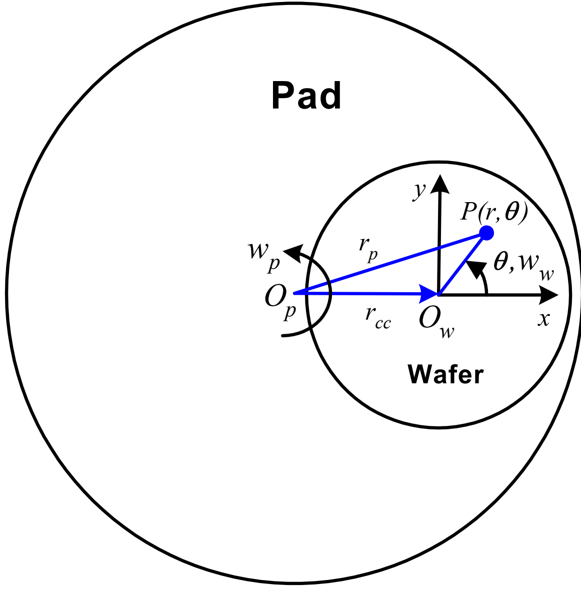

Fig. 3. Schematic of the coordinate system for a rotary CMP process

rotational axes are normal to the polishing plane with an offset, r_{cc}.

The magnitude of relative velocity at point $P(r, \theta)$ in the wafer can be expressed as:

$$v_R = \sqrt{\omega_p^2 r_{cc}^2 + (\omega_w - \omega_p)^2 r^2 - 2\omega_p(\omega_w - \omega_p) r_{cc} r \cos\theta} \tag{2}$$

The material removal rate at position $P(r, \theta)$ is compared to the material removal rate at the center of the wafer. To investigate the effect of relative velocity only, the Preston constant, k_p, and pressure, p, are assumed uniform over the wafer. Also, a new variable η is introduced as $\eta \equiv (\omega_w - \omega_p)/\omega_p$ to represent this material removal rate ratio in a dimensionless form. Eq. 2 shows that the relative velocity is a function of position coordinate (r, θ) if other operating conditions such as ω_w, ω_p are fixed during polishing. Because v_R is periodic with θ, the material removal rate can be integrated for each revolution of the wafer and expressed as a function of r only. Finally, the material removal rate ratio between any position $P(r)$ and the center of the wafer can be represented as:

$$\frac{MRR(r)}{MRR(r=0)} = \frac{v_R(r)}{\omega_p r_{cc}} = \sqrt{1 + \left(\eta \frac{r}{r_{cc}}\right)^2 - 2\eta \frac{r}{r_{cc}} \cos\theta} \tag{3}$$

Fig. 4 shows the result of the material removal rate ratio for different η and this result suggests some important points about wafer-level non-uniformity. When $\eta = 0$ ($\omega_w = \omega_p$), the wafer-level non-uniformity due to relative velocity disappears, which can be an optimal operating condition for the rotary CMP machine. Although the wafer-level non-uniformity due to relative velocity increases as η increases, the effect of this variation can be considered small compared to other sources of variation for wafer-level non-uniformity. For example, when the angular velocity of platen is as much as 50% greater than

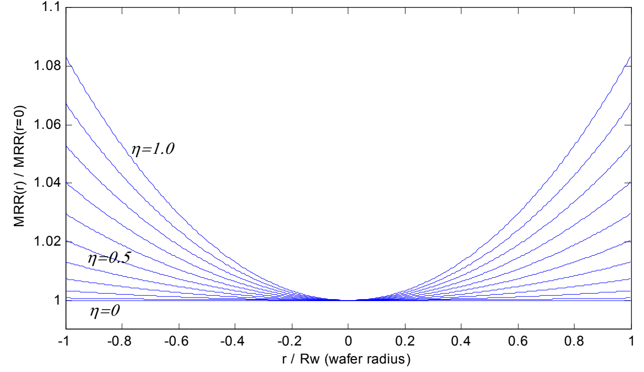

Fig. 4. Material removal rate ratio distribution for various η, where $\eta \equiv (\omega_w - \omega_p)/\omega_p$.

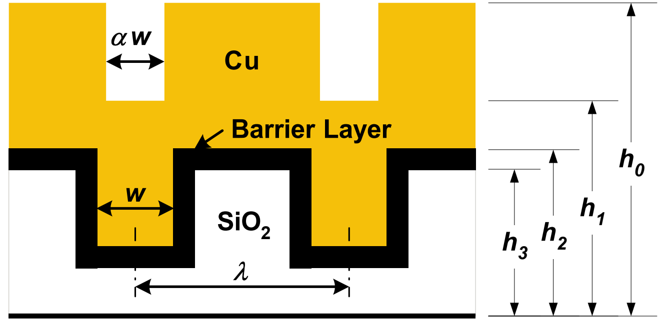

Fig. 5. Definition of basic terms used in the erosion model.

that of the wafer ($\eta = 0.5$), the variation of wafer level non-uniformity due to relative velocity is only 2%, which is within current semiconductor industry specifications [11].

Based on this simulation, two important statements can be made. First, a direct effect of the relative velocity variation on the wafer-level non-uniformity is *not* a significant factor in the CMP process as it has been considered. This means that the relative velocity, v_R, in the Preston equation can be separated as an independent value and considered as a constant. Yet it can still be considered as one of the factors which affect the Preston constant as shown in the slurry transportation analysis and the polishing. Second, there may exist a slip between the wafer and the wafer carrier pad, but the amount of slip is small enough to be neglected.

C. Basic material removal rate prediction scheme

Fig. 5 shows basic terms for the general material removal rate prediction in the Cu CMP process. There are several factors which should be considered as main parameters for erosion calculation.

Although the Preston equation represents a local material removal rate at any point on a wafer, it is often used as an average material removal rate on the wafer level in the case of a blanket wafer polishing. In this case, the Preston constant, pressure and relative velocity are considered as uniform over the entire wafer. Also, it is shown that the relative velocity can be separated from the Preston equation because the local distribution of relative velocity does not have a significant effect on the wafer-level non-uniformity. Finally, a new dimensionless term χ is

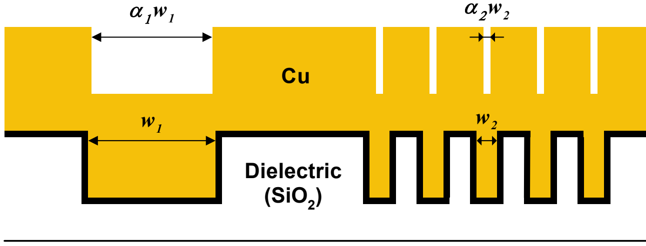

Fig. 6. Definition of Cu interconnect deposition factor α, α is strongly related with the original Cu linewidth. Here, $w_1 = 5\mu m, \alpha_1 = 0.9, w_2 = 0.5\mu m, \alpha_2 = 0.1$.

introduced as the product of the Preston constant and the average pressure, which represents a normalized material removal rate of a blanket wafer.

$$\chi \equiv k_p \cdot p_{av} \tag{4}$$

The normalized material removal rates of blanket Cu, barrier layer material and oxide wafer are represented as χ_{Cu}, χ_b and χ_{ox}. Additionally, the selectivity can be defined as the blanket wafer material removal rate ratio of two different materials. For instance, the selectivity of the Cu and the oxide can be represented as $\frac{\chi_{Cu}}{\chi_{ox}}$.

Pattern geometry in Cu CMP can be represented by two parameters: area fraction and linewidth of Cu interconnect lines. Both parameters can be measured by the original mask pattern, and define the pattern geometry of the Cu damascene structure. A_f is defined as the mask pattern area ratio of the Cu interconnect line.

$$A_f \equiv \frac{A_{Cu}}{A_{total}} \quad (0 < A_f < 1) \tag{5}$$

Much of the past research about the effects of pattern geometry on the material removal rate has focused on the interlevel dielectric (ILD) layer, and it is well known that the material removal rate during polishing is mainly proportional to the $\frac{1}{1-A_f}$ [12].

Although the underlying pattern geometry of Cu damascene structure can be represented by A_f and w, there is another factor which should be included. Most of the polishing time in the Cu CMP process is for the excess Cu removal stage. Due to the characteristics of the Cu deposition process such as physical vapor deposition (PVD) and electroplating, the initial Cu pattern is quite different from the original mask pattern. It is observed that the initial Cu pattern linewidth is smaller than the original Cu interconnect linewidth in the PVD Cu patterned wafer and that the ratio of these two linewidths is mainly dependent on the original Cu interconnect linewidth as shown in Fig. 6. To characterize this ratio, α is defined as:

$$\alpha \equiv \frac{w_{up}}{w_{original}} , \quad w_{up} = \alpha\, w_{original} \quad (0 < \alpha < 1) \tag{6}$$

When $\alpha = 0$, the top surface can be treated as a blanket region regardless of the initial pattern geometry. When $\alpha = 1$, the deposition pattern reflects the initial pattern with the same area fraction and linewidth.

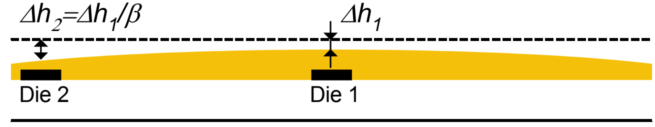

Fig. 7. Definition of wafer-level non-uniformity factor β: Material removal rate ratio between two dies in a wafer, here, material removal rate at Die 1 is larger than that of Die 2.

To include the wafer-level non-uniformity in the erosion model, a new parameter β is introduced, which represents the material removal ratio between two points having the same pattern geometry on different dies in a wafer as shown in Fig. 7. Due to the different material removal rate on these two points, β can be any positive value. In this study, β is set to be in the range of $0 < \beta < 1$, in order to make it consistent with other variables. Following the definition of β, the wafer is perfectly flat when $\beta = 1$ and the wafer-level non-uniformity decreases as β increases.

$$\beta \equiv \frac{|\frac{dh}{dt}|_{die1}}{|\frac{dh}{dt}|_{die2}} = \frac{\chi_{die1}}{\chi_{die2}} \quad (0 < \beta < 1) \tag{7}$$

Another factor to be considered is the local pressure distribution parameter, γ, which is defined as a ratio of Cu interconnect line pressure and average pressure. When polishing starts, the pad contacts the top surface of a wafer, which is affected by the Cu deposition pattern. In this period, the value of γ can be set at zero because the deposited pattern line is empty and the pad deformation is restricted. As the pattern is polished, the whole wafer surface starts holding pressure and the γ value is changed to one. As soon as the pad starts contacting the diffusion barrier layer, γ value starts decreasing from one to zero since the material removal rate of the barrier layer or the dielectric region and the Cu interconnect is different. This γ parameter is closely related to dishing. In this study, the effect of γ on the erosion problem is considered as the local pressure change.

$$\gamma \equiv \frac{p_{Cu}}{p_{av}} \quad (0 < \gamma < 1) \tag{8}$$

The basic material removal rate prediction scheme at each height stage in Fig. 5 can be represented based on the local pressure distribution analysis. Initially, the pad starts contacting the top of the wafer surface, which is filled with Cu with a deposition pattern geometry. The local pressure in this stage can be represented as $\frac{p_{av}}{1-\alpha A_f}$ and the material removal rate becomes $\frac{\chi_{Cu} v_R}{1-\alpha A_f}$. After the pattern is polished, the material removal rate becomes the same as that of the Cu blanket material removal rate until the pad contacts the barrier layer. When it starts polishing the barrier layer or the oxide layer, the γ affects the local pressure distribution as $p_{av}\left(\frac{1-\gamma A_f}{1-A_f}\right)$ and the material removal rate is changed to $\chi_b v_R \left(\frac{1-\gamma A_f}{1-A_f}\right)$ and $\chi_{ox} v_R \left(\frac{1-\gamma A_f}{1-A_f}\right)$, respectively.

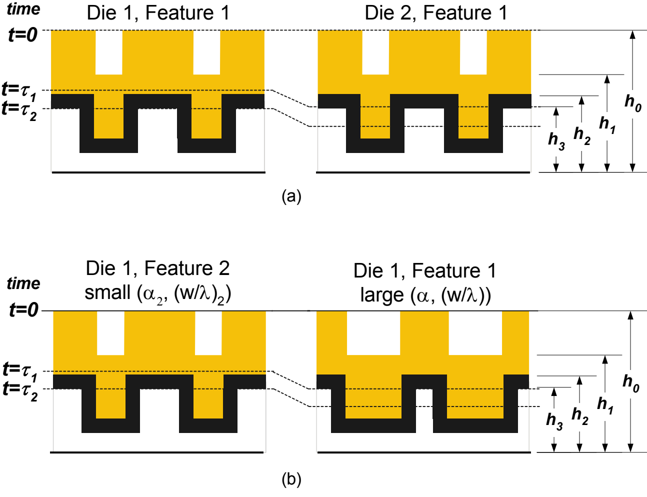

Fig. 8. Schematics of time-based erosion calculation for (a) wafer-level erosion (e_1): compared between same feature points on the different dies and (b) die-level erosion (e_2): compared between two points on the same die.

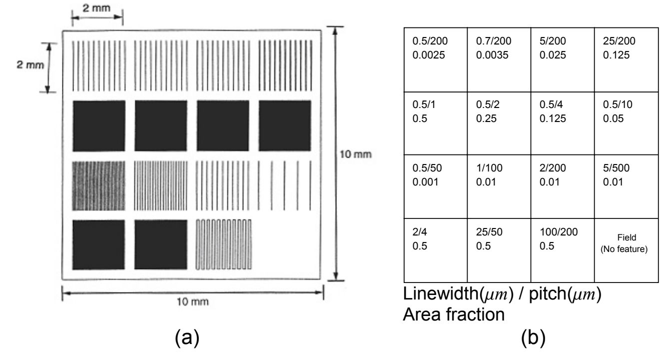

Fig. 9. Schematics of the CMP mask: (a) mask layout and (b) pattern geometry layout

$$h_0 < h < h_1 \qquad \left|\frac{dh}{dt}\right| = \frac{\chi_{Cu} v_R}{1-\alpha A_f} \tag{9}$$

$$h_1 < h < h_2 \qquad \left|\frac{dh}{dt}\right| = \chi_{Cu} v_R \tag{10}$$

$$h_2 < h < h_3 \qquad \left|\frac{dh}{dt}\right| = \chi_b v_R \left(\frac{1-\gamma A_f}{1-A_f}\right) \tag{11}$$

$$h_3 < h < h_4 \qquad \left|\frac{dh}{dt}\right| = \chi_{ox} v_R \left(\frac{1-\gamma A_f}{1-A_f}\right) \tag{12}$$

D. Wafer level erosion

The erosion at each stage can be derived by applying the basic material removal rate calculation scheme for corresponding pattern geometry. Fig. 8 shows a schematic of a time-based erosion calculation model.

Wafer-level erosion e_1 can be modeled by comparing two points with the same features on different dies, as shown in Fig. 8(a). If Die 2 has a higher material removal rate than Die 1, the time that the oxide layer of Die 1 is exposed to the polishing pad, τ_2, will be longer than the time for the Die 2 case, τ_1. τ_1 can be calculated by using the basic material removal calculation scheme as:

$$\tau_1 = \frac{h_0 - h_1}{\frac{\chi_{Cu} v_R}{1-\alpha A_f}} + \frac{h_1 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R \left(\frac{1-\gamma A_f}{1-A_f}\right)} \tag{13}$$

By applying the wafer-level non-uniformity factor β, τ_2 can be simply expressed as:

$$\tau_2 = \frac{1}{\beta}\tau_1 \tag{14}$$

After the oxide layer of Die 1 is exposed to the polishing surface, the polishing still continues until the time becomes τ_2, which means that all excess Cu and barrier material on the both dies are removed. Because the oxide layer of Die 2 will be thinned by overpolishing during this period, the erosion time $\Delta\tau$ can be determined as:

$$\Delta\tau = \tau_2 - \tau_1 \tag{15}$$

Wafer-level erosion, e_1, can be obtained by considering the oxide removal at Die 2 during erosion time interval $\Delta\tau$.

$$\begin{aligned} e_1 &= \chi_{ox} v_R \left(\frac{1-\gamma A_f}{1-A_f}\right) \cdot \Delta\tau \\ &= \left(\frac{1}{\beta} - 1\right) \left[\frac{\chi_{ox}}{\chi_{Cu}} \left(\frac{1-\gamma A_f}{1-A_f}\right) \left[(1-\alpha A_f)(h_0 - h_1) \right.\right. \\ &\quad \left.\left. + (h_1 - h_2)\right] + \frac{\chi_{ox}}{\chi_b}(h_2 - h_3)\right] \end{aligned} \tag{16}$$

To consider the wafer-level erosion specifically, a local reference point for each die needs to be selected in order for the pattern effect to be disregarded. In this study, a test mask set has 15 different pattern features and 1 field (no pattern) region per each die as shown in Fig. 9. The field region with no feature is chosen as a local reference point for the current erosion model. Thus, wafer-level erosion e_1 for the local reference points for each die can be rewritten as:

$$e_1 = \left(\frac{1}{\beta} - 1\right) \left[\frac{\chi_{ox}}{\chi_{Cu}}(h_0 - h_2) + \frac{\chi_{ox}}{\chi_b}(h_2 - h_3)\right] \tag{17}$$

Eq. 17 shows that there are two parameters that significantly determine the amount of the wafer-level erosion in the Cu CMP process. One is the wafer-level non-uniformity factor β and the other is the blanket material removal rate ratio among the Cu, barrier layer and dielectric.

E. Die level erosion

To specify the amount of die-level erosion, e_2, two points with different features on the same die are considered as shown in Fig. 8(b). According to the basic material removal rate calculation scheme, Feature 1 with a larger area fraction of Cu interconnects is polished faster than Feature 2 with a smaller area fraction. The time that the oxide layer of Feature 1 and

Feature 2 are on the polishing surface can be obtained as τ_1 and τ_2, respectively, by using the basic material removal calculation scheme.

$$\tau_1 = \frac{h_0 - h_1}{\frac{\chi_{Cu} v_R}{1-\alpha A_f}} + \frac{h_1 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R \left(\frac{1-\gamma A_f}{1-A_f}\right)} \quad (18)$$

$$\tau_2 = \frac{h_0 - h_1}{\frac{\chi_{Cu} v_R}{1-\alpha_2 A_{f_2}}} + \frac{h_1 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R \left(\frac{1-\gamma_2 A_{f_2}}{1-A_{f_2}}\right)} \quad (19)$$

After the polishing surface reaches the top of the oxide material on Feature 1, the polishing still continues until the time becomes τ_2 at which time the oxide layer on Feature 2 starts being polished. Because the oxide layer on Feature 1 will be thinned by overpolishing during this period, the erosion time, $\Delta\tau$, can be represented as:

$$\Delta\tau = \tau_2 - \tau_1 \quad (20)$$

General die-level erosion e_2 can be calculated by considering oxide material removal in Feature 1 during the time gap $\Delta\tau$.

$$\begin{aligned} e_2 &= \chi_{ox} v_R \left(\frac{1-\gamma_1 A_{f_1}}{1-A_{f_1}}\right) \cdot \Delta\tau \quad (21) \\ &= \frac{\chi_{ox}}{\chi_{Cu}} \left[\frac{(1-\gamma_1 A_{f_1})(\alpha_1 A_{f_1} - \alpha_2 A_{f_2})}{1-A_{f_1}}\right](h_0 - h_1) \\ &\quad + \frac{\chi_{ox}}{\chi_b}\left[\left(\frac{1-\gamma_1 A_{f_1}}{1-A_{f_1}}\right)\left(\frac{1-A_{f_2}}{1-\gamma_2 A_{f_2}}\right) - 1\right](h_2 - h_3) \end{aligned}$$

Again, the same local reference point from the wafer-level erosion calculation will be needed to be able to separate the die-level erosion with wafer-level erosion. Thus, e_2 is defined as the relative oxide thickness of each feature in a die with respect to the oxide thickness of the local reference point in the same die.

$$\begin{aligned} e_2 &= \left(\frac{A_{f_1}}{1-A_{f_1}}\right)\left[\frac{\chi_{ox}}{\chi_{Cu}}(1-\gamma_1 A_{f_1})\alpha_1(h_0 - h_1) \right. \\ &\quad \left. + \frac{\chi_{ox}}{\chi_b}(1-\gamma_1)(h_2 - h_3)\right] \quad (22) \end{aligned}$$

Eq. 22 shows that there are several parameters which affect the amount of the die-level erosion in the Cu CMP process such as the area fraction of a feature A_f, the local pressure distribution factor γ, the interconnect deposition factor α and the blanket material removal rates of the Cu, barrier layer and dielectric, χ_{Cu}, χ_b and χ_{ox}.

III. Experiments

A Cu damascene structure has been designed to study the effects of the various parameters on wafer-level and die-level erosion and to verify the current model. Fig. 9 shows the physical layout of the pattern on the mask. The pattern for each die (10x10 mm) consists of a matrix of 2.5 x 2.5 mm blocks (subdie). These blocks consist of line-space features, with a minimum linewidth of 0.5 μm and a maximum linewidth of 100 μm. The area fraction of Cu interconnects in the experimental mask has ranges from 0.01, representing isolated lines, to 0.5, representing a dense packing case. This pattern was transferred onto a 2 μm thick SiO_2 coating by lithography on a 100 mm, (100) orientation silicon wafer. After oxide trenches are etched to a depth of 1 μm, a 20 nm thick Ta barrier layer was deposited, followed by a 1.5 μm thick Cu film, by physical vapor deposition (PVD).

TABLE I

Experimental conditions

Parameters	Value
Diameter of Wafer (m)	0.1
Normal Load (N)	391
Normal Pressure (kPa)	48
Rotational Speed (rad/s)	7.8
Linear Velocity (m/s)	0.70
Duration (sec)	60-360
Slurry Flow Rate (ml/sec)	2.5

TABLE II

Blanket Material Removal Rate

Abrasive Material	Al_2O_3	Al_2O_3	SiO_2	CeO_2
Abrasive Particle Size (nm)	1000	300	1000	1000
Cu	489	213	372	49
Ta	27	13	128	149
TaN	25	12	72	74
SiO_2	34	14	383	123

Unit of MRR = nm/min

Experiments were conducted on a rotary CMP machine with the experimental conditions listed in Table 1. The normal pressure was maintained at 48 kPa and the relative velocity was maintained at 0.7 m/s over the wafer by setting the rotational velocity of the wafer and the platen at the same value. The polishing duration was varied from 1 to 6 min to cover a different set of blanket material removal rates of Cu, oxide and diffusion barrier layer.

Four types of slurries were used to get blanket material removal rates for each layer material as listed in Table 2. Hydrogen peroxide was used in the commercial Al_2O_3 slurry with 1 μm mean particle size to prevent particle agglomeration and to get the specified material removal rate. All other slurries were mixed immediately before use and were stirred to prevent particle settling during polishing. In contrast to the acidic or basic solutions which have been used in commercial Cu CMP, pH of each slurry was maintained at 7$\sim$7.5 to focus only on the mechanical aspects of polishing. The Rodel IC-1400 was used to polish the wafer and the pad was conditioned before polishing each wafer.

IV. Results

A. Blanket material removal rate

The developed wafer and die-level erosion models show that one of the major factors in deciding the amount of erosion is

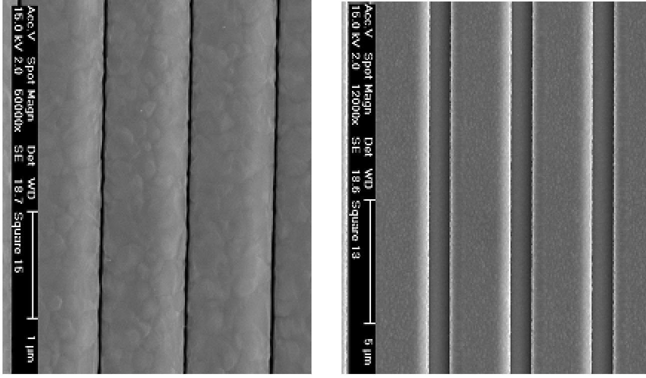

Fig. 10. SEM micrographs for the effect of interconnect deposition factor, α, (a) $A_f = 0.5, w = 0.5\mu m, \alpha = 0.1$ and (b) $A_f = 0.5, w = 2\mu m, \alpha = 0.8$.

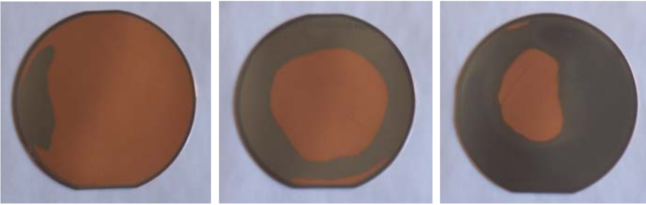

Fig. 11. Observation of the effect of wafer-level non-uniformity factor, β in Cu blanket wafer polishing at (a) t=2min, (b) t=3min and (c) t=4min.

selectivity, which represents the ratio of blanket material removal rates between the Cu, dielectric and diffusion barrier layer. Therefore, it is necessary to get a blanket material rate of each material for different slurries. Four different slurries are used for three different blanket material coatings and the results are listed at Table 2.

B. Measurement of Cu interconnect line deposition factor α

The interconnect deposition factor α can be easily obtained by measuring the deposited top surface of a patterned wafer by Scanning Electron Microscopy (SEM). Fig. 10 shows the results of the SEM measurement of two points with the same area fraction (0.5) and different linewidths (0.5 μm and 2 μm). PVD Cu patterned wafers were used for SEM measurements. The results show that the value of α is closely related to the Cu interconnect linewidth w. If the linewidth is larger than 5 μm, α is about 0.9, which means that the deposited pattern reflects the original mask pattern very well. If the linewidth is smaller than 1 μm, α is under 0.1 and the top surface deposited pattern could be considered as blanket area. In the range between these two ($1\mu m < w < 5\mu m$), the α value increases as the linewidth w increases.

C. The wafer-level non-uniformity factor β

The wafer-level non-uniformity factor β can be quantified by observing the blanket wafer polishing material removal rate at two points on the same wafer through time evolution. Fig. 11 shows the Cu blanket wafers at 2 min, 3 min and 4 min of polishing time during CMP process. The figure shows that the edge of the wafer is being polished faster than the center area

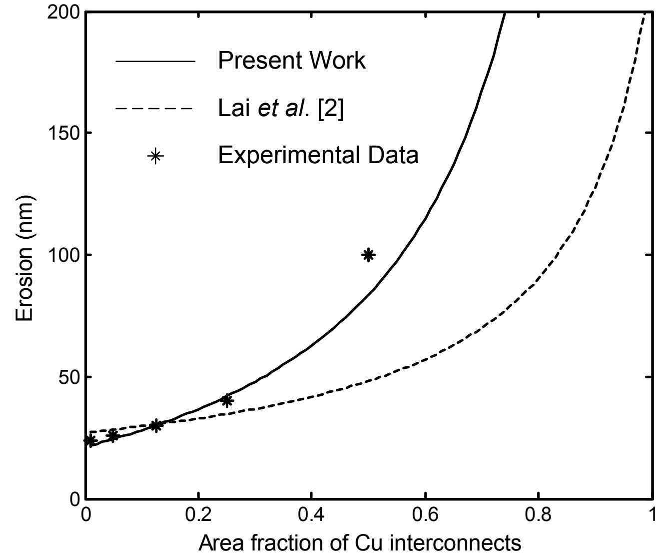

Fig. 12. Model verification for experimental results and comparison with the model of Lai *et al.* [2]: mainly addressed for small A_f.

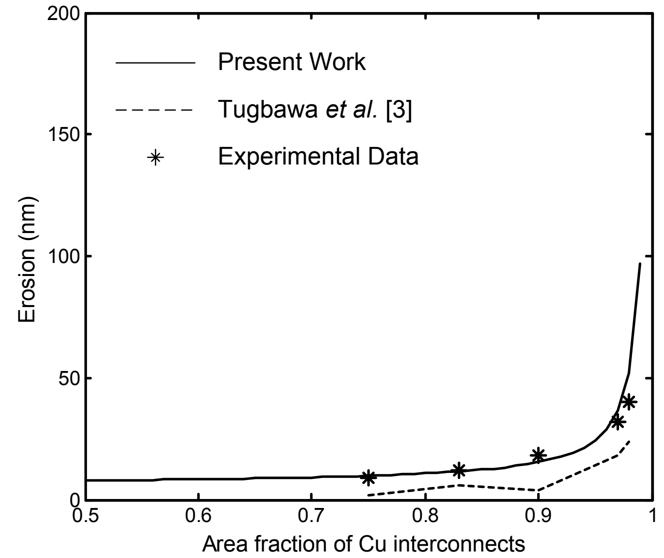

Fig. 13. Model verification for experimental results and comparison with the model of Tugbawa *et al.* [3]: mainly addressed for large A_f.

as polishing time increases, and that the maximum ratio of material removal rate is close to 0.8. Each CMP machine can have different β values. Also, it is important to point out that the β is not the exact wafer-level non-uniformity value of polished wafer after the Cu CMP process but only the material removal rate ratio between two points on a wafer which is strongly related to the final wafer-level non-uniformity value.

D. Model verification

After all of the parameter values from the previous section such as selectivity, α and β are determined, these values can be used for calculating the amount of wafer-level and die-level erosion based on the proposed model. In this study, two different sets of previous data are used to verify the current erosion

model. Fig. 12 shows the experimental data and an erosion model by Lai *et al.* [2] and the current model. When the area fraction is under 0.2, both models predict the experimental data well but, as area fraction increases over 0.3, there is a significant deviation between the Lai *et al.* model and the real data. As shown in Fig. 12, the current model can predict the real data more closely in the middle value of the Cu interconnect area fraction as well as the small value of area fraction than the Lai *et al.* model. These data show that the current erosion model can predict the erosion well in the less packed pattern geometry with the area fraction under 0.5.

Fig. 13 shows the data and an erosion model by Tugbawa *et al.* [3] and the current model. Most of the data in these experiments are distributed throughout the high packed pattern geometry region with an area fraction over 0.7. There exists a gap similar to shifting between the Tugbawa *et al.* model and the actual data, but the current model still matches the experimental data well.

In each case of model verification, wafer-level erosion can be easily represented by choosing a local reference point, which has a special pattern geometry with a zero area fraction of the Cu interconnect on each die. This results in the shifting effect of die-level erosion in total erosion calculation because wafer-level erosion is constant over the same die.

V. Conclusions

Both analytical and experimental studies on the erosion in the Cu CMP process are presented in this paper and the following conclusions can be drawn.

1. The erosion in the Cu damascene structure is defined by the oxide thinning with respect to the original oxide thickness. To identify the source of erosion systematically, wafer-level and die-level erosion are defined separately. The possible sources of erosion at each level are identified, such as Cu interconnect deposition factor α, wafer-level non-uniformity factor β, local pressure distribution factor γ and blanket wafer material removal rate, χ. Redefining the erosion as wafer-level and die-level makes it possible to get clear sources of erosion and their effects. For example, the wafer-level non-uniformity factor and the pattern geometry factor effects on erosion could be considered separately in the current model, if a suitable local reference point is considered.

2. Based on the kinematics of a rotary CMP machine, the material removal rate ratio distribution for various angular velocities of wafer and platen was described. It is shown that a direct effect of the relative velocity variation on the wafer-level non-uniformity is not as significant in the CMP process as it has been considered. This means that the relative velocity, v_R, in the Preston equation can be separated as an independent value and considered as a constant.

3. The basic material removal rate calculation scheme was developed by using the local pressure distribution analysis in the Cu damascene structure. Pattern geometries on each stage were defined by using the area fraction, A_f, linewidth, w, of the Cu interconnects and the local pressure was calculated at each height stage. Other local effects during the polishing except pressure, were included in the normalized blanket material removal rate.

4. Experiments were conducted to determine the values of each parameter. The blanket wafer material removal rates for each layer materials could be acquired for different types of slurries. For a given mask pattern geometry, the Cu interconnect deposition factor α was measured in SEM and it could be shown that α is strongly related to Cu linewidth and deposition method. The wafer-level non-uniformity factor β was also observed through the blanket Cu wafer polishing experiments. By considering the significance of each parameter on the developed erosion model, the optimized erosion minimization scheme can be suggested.

5. The developed erosion model was verified through the existing erosion models and data. It has been shown that the current model can reflect the real erosion data very well in the low area fraction region ($A_f < 0.5$) as well as in the packed interconnect pattern geometry region ($A_f > 0.5$). Also, it was addressed that total erosion can have a shifting effect of die-level erosion if the wafer-level erosion is independent of pattern geometry, as shown in Fig. 13.

Acknowledgment

This work was supported by The Singapore-MIT Alliance program.

References

[1] J.-Y. Lai, N. Saka and J. H. Chun, *Evolution of Copper-Oxide Damascene Structures in Chemical Mechanical Polishing, - Contact Mechanics Modeling,* J. Electrochem. Soc., Vol 149, G31-G40,2002.

[2] J.-Y. Lai, N. Saka and J. H. Chun, *Evolution of Coppe-Oxide Damascene Structures in Chemical Mechanical Polishing, - Copper Dishing and Exide Erosion,* J. Electrochem. Soc., Vol 149, G41-G50, 2002.

[3] Tamba E. Gbondo-Tugbawa, *Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing Process,* Ph.D. thesis, M.I.T., 2002.

[4] D.-Z. Chen and B.-S. Lee, *Pattern Planarization Model of Chemical Mechanical Polishing,* J. Electrochem. Soc., Vol. 146, pp. 744-748., 1999.

[5] J.M. Steigerwald, R. Zirpoli, S.P. Murarka, D. Price and R.J. Gutmann, *Pattern Geometry Effects in the Chemical-Mechanical Polishing of Inlaid Copper Structures,* J. Electrochem. Soc., Vol. 141, pp. 2842-2848. 1994.

[6] F.W. Preston, *The Theory and Design of Plate Glass Polishing Machines,* J. Soc Glass Technology , Vol. 11, pp. 214-256., 1927.

[7] Z. Stavreva, D. Zeidler, M. Plotner, G. Grasshoff and K. Drescher, *Chemical Mechanical Polishing of Copper for Interconnect Formation,* Microelectronic Engr., Vol. 33, pp. 249-257., 1997.

[8] R. Komanduri, N. Umehara and M. Raghanandan, *On the possibility of Chemo-Mechanical Action in Magnetic Float Polishing of Silicon Nitride,* J. Tribology , Vol. 118, pp. 721-727., 1996.

[9] T. Park, T. Tugbawa and D. Boning, *Pattern Dependent Modeling of Electroplated Copper Profiles,* International Interconnect Technology Conference (IITC), pp. 274-276., 2001.

[10] S.R. Runnels, I. Kim, J. Schleuter, C. Karlsrud and M. Desai, *A Modeling Tool for Chemical-Mechanical Polishing Design and Evaluation,* IEEE Tran. on Semiconductor Mfg., Vol. 11, pp. 501-510., 1998.

[11] *International Technology Roadmap for Semiconductors,* 2001.

[12] D. Ouma, D. Boning, J. Chung, W. Easter, V. Saxena, S. Misra and A. Crevasse, *Characterization and Modeling of Oxide Chemical-Mechanical Polishing Using Planarization Length and Pattern Density Concepts,* IEEE Tran. on Semiconductor Mfg., Vol. 15, pp. 232-244., 2002.