An Analysis of MRAM Based Memory Technologies

by

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B. Tech., Metallurgical and Materials Engineering (2002)
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Submitted to the Department of Materials Science and Engineering
in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Materials Science and Engineering

at the

Massachusetts Institute of Technology

September 2006

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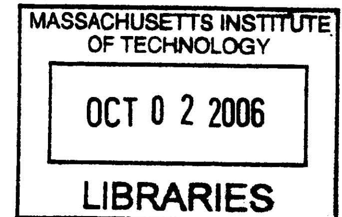

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Submitted to the Department of Materials Science and Engineering on August 18, 2006 in Partial Fulfillment of the Requirements for the Degree of Master of Engineering in Materials Science and Engineering

ABSTRACT

MRAM is a memory (RAM) technology that uses electron spin to store information. Often been called "the ideal memory", it can potentially combine the density of DRAM with the speed of SRAM and non-volatility of FLASH memory or hard disk, and all this while consuming a very low amount of power. However, it is the need for a fast and non-volatile computer memory that has been the key driver for evolution of this technology. At the moment, MRAM is in its final stages of development and much of the current research concentrates on issues like reducing the write current, increasing the density and making the process more reproducible.

A lot of companies are pursuing research on this technology and are likely to introduce it into the market in the near future. However, it will be a while before MRAM can replace conventional memories. Nevertheless, since MRAM can resist high radiation, and can operate in extreme temperature conditions, it is likely that we will see the first MRAM in applications that need such properties.

Thesis Supervisor: Caroline A. Ross
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Chapter 1: Technology Analysis

1.1 Introduction

The history of scientific research and technological development is replete with examples of breakthroughs that have advanced the frontiers of knowledge, but seldom does it record events that constitute paradigm shifts in broad areas of intellectual pursuit. One notable exception, however, is that of spin electronics, wherein information is carried by electron spin in addition to, or in place of its charge. It is now well established in scientific and engineering communities that Moore's Law, having been an excellent predictor of integrated circuit density and computer performance since the 1970s, now faces great challenges as the scale of electronic devices has been reduced to the level where quantum effects become significant factors in device operation. Electron spin is one such effect that offers the opportunity to continue the gains predicted by Moore's Law, by taking advantage of the confluence of magnetics and semiconductor electronics. The use of both charge and spin degrees of freedom in semiconductors is expected to enable a revolutionary class of electronics whose functionality will surpass that of existing semiconductor technology.

Spin electronics combines semiconductor microelectronics with spin-dependent effects that arise from the interaction between electrons and a magnetic field. Since the characteristic length for spin-dependent effects is on the order of 1 nm compared to 10 nm for semiconductor electronics, spin-electronic devices have the potential to achieve much higher integration densities. Conventional electronics is based on the number of charges and their energies, and device performance is limited in speed due to energy dissipation, whereas spin electronics is based on the direction of spin and spin coupling, and is capable of much higher speeds at low power consumption. The advantages of spin-electronic devices would include non-volatility permitting data retention in non-powered conditions, increased integration densities, higher data processing speeds, low electrical energy demands, and fabrication processes compatible with those currently used in semiconductor microelectronics. There is strong evidence that the technology shift, taking place from semiconductor electronics to spin-dependent devices will help to meet

the sensing and storage demands of information technology in the 21st century. During the next decade, spin electronics will accelerate development in quantum computing, communications, and revolutionary molecular and chemical systems.

To date, the principal applications of spin-electronic devices have been in read heads for magnetic discs, and in magnetic field sensors. However, the greatest impact of spin-electronic devices is expected to be in magnetic random access memories (MRAM) to be used in conjunction with, or as replacements for, EEPROM, DRAM and flash memory in computer applications, where MRAM's lower writing energy, faster writing times, and no wear-out with writing cycle become significant factors. Thus, given its potential attributes, MRAM can essentially replace all the incumbent memory technologies and capture the semiconductor memory market segment that keeps growing at a steady pace. The drawback to this new technology, however, is the fabrication complexity that makes it difficult for MRAM to be implemented into the industry.

There are many attributes of Magnetic Random Access Memory, but in order to fully understand the impact that the technology could have on various industries, one must understand the technology itself. The history and current configurations of MRAM technology are explained in the following pages.

1.2 A Very Brief History of MRAM

While spintronic transistors and logic lie off in the future, magnetic memories are in use now. In fact, magnetic memory is not a new idea at all. The earliest mainframe computers used magnetic memory cores that were very similar to MRAM in that they used a matrix of current carrying wires to program magnetic elements. The "modern" MRAM grew out of research work that began in the late 1980s. In this type of technology information is stored through the magnetic polarization of thin films of magnetic material that are integrated with semiconductor materials. MRAM make use of the magneto-resistance (MR) effect, in which magnetic fields cause a change in the electrical resistivity of a material. Some kinds of MRAM are based on "giant magneto resistance" (GMR) [1,2] that uses thin layers of metallic film to produce an enhanced version of MR in which the effect is considerably stronger than with the "basic" MR effect.

The story of MRAM in its modern form dates back to 1989, which is when IBM announced new discoveries of GMR effects in thin film structures. In 2000, that is, slightly over a decade later, IBM and Infineon established a joint program to develop MRAM using an MTJ approach. Anisotropic MRAM was developed originally by Honeywell and what was then Nonvolatile Electronics (now NVE) back in the 1990s. NVE licensed some of its patents to Motorola and Cyprus. Meanwhile, actual MRAM products have started to be introduced. The year 2004 turned out to be a watershed year for productization of MRAM. Not only did Infineon announce a prototype of a 16-Mbit MRAM chip, but also Freescale, which has inherited Motorola's MRAM business, announced that MRAM was now a standard product that was sampling.

A variety of different kinds of MRAM have been built or at least described in the literature using the basic ingredients described above. These are profiled in the following Table.

Type of MRAM	**Description**
Anisotropic (AMR)	Developed by Honeywell and NVE in the early 1990s, with early work done at Iowa State University. It uses anisotropic magneto-resistance variations in ferromagnetic materials.
Spin Valve	Uses the GMR effect, which was discovered in the late 1980s by researchers in France and Germany. Uses a tri-layer structure consisting of a soft magnetic layer and a harder magnetic layer which are spaced by a thin layer of non-magnetic material. Each layer is between 5 nm and 25 nm thick. Important work on spin valve MRAM was done during the late 1990s by NVE, IBM and at the University of Minnesota. Honeywell is believed to have built and used MRAM using this approach and it has also been developed by Union Semiconductor and (to a very limited extent) by Texas Instruments. Integrated Magnetoelectronics has shown a device that combined spin- valve with a GaAs diode.
Pseudo Spin Valve (PSV)	As the name suggests, this is a variation of the spin valve approach in which the MRAM has two magnetic layers, one of which rotates more easily than the other. Originally described by Motorola in 1996 with some later work from NVE.
Permanent RAM	Developed by Integrated Magnetoelectronics. Described as "a closed flux structure using GMR materials." The GMR thin films are connected in series and are coupled to a magnetic field for programming.
Magnetic Tunnel Junction (MTJ)	Motorola, IBM and Infineon, use the effect of spin alignment on a tunneling current perpendicular to two films that can be spin aligned or unaligned (parallel or antiparallel). Having the current flow perpendicular to the films rather than parallel is architecturally

	simpler, more compatible with standard lithographic techniques and more easily scaled to a dense memory structure. It seems as if MTJ MRAM will be the market leader and Motorola describes its adoption of MTJ as a key development of its MRAM product. Supposedly, higher densities can be achieved using MTJ than with other approaches.
Hall Effect	Uses the Hall Effect in which a current in a thin film is deflected by a magnetic field. Work on Hall Effect MRAMs has been done by Honeywell, Pageant Technologies and at the U.S. Naval Research Lab.

1.3 MRAM Cell Designs

Like other high-density semiconductor memory types, the core of an MRAM is one or more two-dimensional arrays of storage cells. Multiple subdivided arrays are used to speed up access times by shortening the signal paths. Each cell will usually store one bit of information, either "0" or "1". The rows in each array are traversed by parallel polysilicon wordlines running in one direction, while the columns are traversed by parallel bitlines or sense lines running in the orthogonal direction. Storage cells are positioned at the intersections of wordlines and bitlines (or sense lines); this allows each cell to be identified and accessed conveniently by means of a row and a column address. The conductors are used to create magnetic fields at the desired cell location(s) that are of sufficient strength to cause controlled magnetization state changes, but not so strong as to disturb the states of non-addressed cells. The non-addressed cells include cells that are half-selected, that is, cells that have current flowing through one (but not both) of the crossing conductors. Cells that are fully unselected may still be vulnerable to disturbances caused by stray magnetic fields produced by currents in nearby rows and columns.

The various MRAM technologies differ by the implementation of the storage cell. The state of a bit, either "0" or "1" is recorded using the magnetoresistive states of a structure comprising one or more thin film ferromagnetic regions associated with the cell. At least one of the films is programmable (i.e. free) by changing the magnetization vector between two possible orientations. The magnetization in the one or more other ferromagnetic films may remain fixed. Write operations are accomplished by inducing changes in the magnetization in the programmable films using the local magnetic fields

produced by currents driven along the bitlines, wordlines, sense lines, and/or digit lines. Read operations are accomplished by measuring some property of the cell, usually a magnetoresistance that depends on the magnetization state of the free film. In cells that use magnetoresistance, a key figure of merit is the magnetoresistance ratio, MR = $(R_{max} - R_{min}) / R_{min}$, where R_{max} and R_{min} are the maximum and minimum values, respectively, of the programmable cell resistance. Much MRAM development effort has been required to increase the MR from only a few percent to up to over 40% in recently described designs. The remaining subsections briefly review the basic MRAM cell designs that have been reported in the literature.

1.3.1. Anisotropic MRAM

Anisotropic MRAM was investigated in the late 1980s and early 1990s by Honeywell Inc., NonVolatile Electronics Inc. (NVE, a company based in Eden Prairie, Minnesota that was spun off from Honeywell in 1989 to pursue MRAM technology), and by researchers at Iowa State University [3, 4, 5]. The cell name comes from the fact that the programmable Permalloy thin film is shaped to permit only two magnetic polarizations. The sense line through a column of cells is connected in series, in the long direction, to the ferromagnetic cell regions. The wordlines pass orthogonally at a 1.0 μm distance over the cells without making electrical contact with them.

An anisotropic cell is written by passing currents simultaneously along the wordline and sense line. The resulting combined magnetic field at the cell is strong enough to force the polarization in the programmable ferromagnetic region. At half-selected cells, the half-strength magnetic field is insufficient to affect the cell's state. With the wordline carrying a positive direction current (e.g. 30 mA), the two possible sense current directions (positive and negative) are used to force two polarizations that encode either a "0" or a "1". The two polarizations can be sensed by the slightly different resistances (MR $\lesssim$2%) experienced by a positive sense line current when a negative wordline current is present.

Although anisotropic MRAM chips of 16 kbit capacity were reportedly built by Honeywell [6], this early MRAM technology has serious drawbacks. The required write currents are high and the read signals in real arrays are very weak (e.g. $\lesssim$1.0 mV), making

reliable sensing questionable in large, densely packed cell arrays. Work on anisotropic RAM was superceded in the early 1990s by work on MRAMs that exploited the then recently discovered giant magnetoresistive effect.

1.3.2. The Discovery of Giant Magnetoresistance

One of the most significant events in the development of MRAM was the independent discovery in the late 1980s by two European teams – one group led by Albert Fert at the University of Paris- Sud, and a second group led by Peter Grünberg at the KFA research institute at Jülich, Germany – of the giant magnetoresistive (GMR) effect [1, 2]. These two teams observed unexpectedly large magnetoresistive variations (MRs of 6% and 50%, respectively) in layered nanoscale structures containing ferromagnetic films separated by nonmagnetic metallic spacer layers. The sensing current in GMR devices passes in parallel with the spacer layer. When the magnetizations of the two ferromagnetic layers are in a parallel orientation, the electrical resistance is observed to be lower than when the magnetizations are antiparallel.

The theoretical basis of GMR was determined to be spin-dependent scattering of electrons in the ferromagnetic layers [7]. When an electrical current passes through a ferromagnet, the spins of the electrons are quantized, or spin-polarized, along the axis of magnetization with two possible values, which are usually called up (parallel with the field) and down (antiparallel with the field). The minority population of spin-down electrons is strongly scattered during passage through the ferromagnet while the majority population of spin-up electrons passes through with less scattering. Electron scattering at the interfaces between the magnetic and ferromagnetic materials is believed to be an important factor. When both ferromagnetic layers have parallel magnetizations with respect to each other, the spin-up electrons pass through the GMR structure with a lower resistance; when these layers have antiparallel magnetizations, then both the spin-up and spin-down electron populations are more strongly scattered in the GMR structure, and hence a higher resistance is experienced by the cell current.

In the early work, the GMR effect was observed only at low temperatures and in the presence of relatively strong magnetic fields. However, the potential impact of GMR on

magnetic sensors, and hence magnetic memories, was quite apparent. IBM, in particular, was quick to develop GMR sensors that could be used in the recording heads of magnetic hard disks [8]. The discovery of GMR also stimulated much research into other devices, such as monolithic MRAMs.

1.3.3. Spin Valve MRAM

Attempts to exploit the GMR effect in MRAM led to new cell designs called spin valve and pseudo spin valve MRAM cells. Both types of cells include three-layer sandwich structures comprising two magnetic layers (alloys of Ni, Fe and Co) separated by a nonmagnetic metal (often made of Cu), with the entire structure ranging between 5 and 25 nm in thickness. As in other GMR devices, the sensing current is passed along the direction of the layers.

The orientation of the magnetic field in one of the magnetic layers is fixed or pinned as a result of the presence of a fourth antiferromagnetic layer (often of FeMn or IrMn) that is formed along the outside surface of the pinned magnetic layer. The second free magnetic layer can be changed as a result of magnetic fields generated locally by orthogonal electrical currents. The GMR structure is relatively immune to external magnetic fields due to the strong coupling between the two magnetic layers.

Spin valve MRAM cells based on GMR structures were significant improvements over earlier magnetoresistive cells, with MRs increased from at most a few percent up to MRs in the range from 8% to 15%.

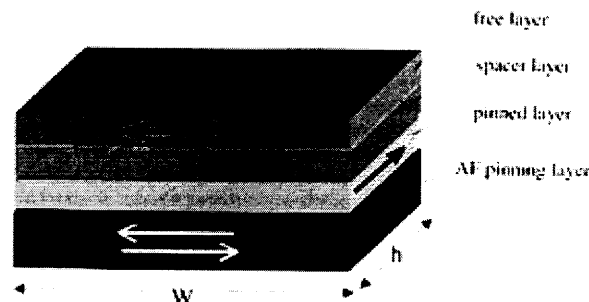


Fig 1: A schematic of spin-valve from ref. [F-1].

Cell reads can be performed in two ways for a spin valve cell. A destructive read can be

performed by comparing the voltage drop along a current-carrying sense line through the cell before and after the cell is over-written into a known state. After the read, the original contents of the cell must then be restored to the cell. A nondestructive read can be performed by comparing the voltage drop of a current path through the cell with the voltage drop produced by a reference cell. This second method requires an access transistor at each cell site that allows the current path to be steered during read operations.

Several important problems affect the spin valve cell. As the cell geometries shrink further, stronger magnetic fields are required to switch the free layer, while at the same time those stronger switching fields tend to disturb the polarization of the pinned layer. These problems threatened to drop the MR back down to a few percent at submicron geometries.

1.3.4. Pseudo Spin Valve MRAM

Pseudo spin valve cells are GMR-based cells that are designed to allow the polarization of two magnetic films to rotate [9]. The two films have different thicknesses so that the thinner sense layer is more susceptible to magnetization changes than the thicker storage layer. Local magnetic fields are generated by passing currents through both a sense line and a wordline, which is electrically isolated from the cell. If the magnetization of the two layers opposes the generated magnetic field, then as the field strength is increased, first the sense layer followed later by the storage layer will switch polarizations. Thus with respect to the sense current path, the cell resistance will be observed to increase momentarily while the two layers have opposite polarizations. If instead the two layers had started out being both polarized in the same direction as the generated field, then no polarization switches, and hence no resistance changes, would occur. Data is recorded by the two possible magnetizations, denoted by "0" and "1" that can be established in the shaped storage layer. Nondestructive read operations involve generating moderately-strong magnetic fields that are strong enough to switch the sense layer, but are not strong enough to switch the storage layer. The moderate field is used to force the sense layer first into the "0"polarization, then back to the "1" polarization. If the storage layer holds

the "0" ("1") polarization, the resistance of the cell will be observed to change from low (high) to high (low). Write operations involve using a stronger local magnetic field to force either the "0" or "1" polarizations on both the sense and storage layers. The written data is determined by the direction of the wordline current. Honeywell has been a pioneer in GMR MRAM technology, and military applications appear to have been one of the intended markets [10]. Its MRAM program led to 256-kb parts in 1997 [11] followed by 1-Mb parts [12].

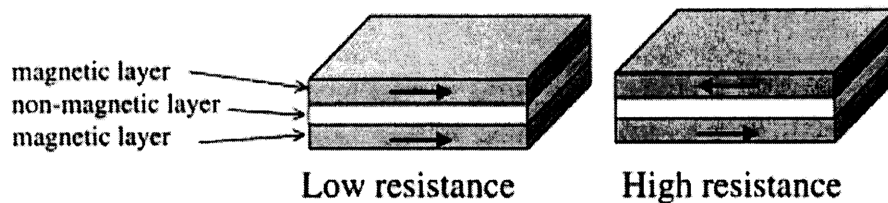


Fig 2: Depiction of GMR effect in a pseudo-spin valve (Ref. F-2)

1.3.5. Magnetic Tunnel Junction MRAM

Most industrial MRAM programs appear to have chosen to pursue an alternative technology to GMR-based MRAM that exploits a quantum mechanical phenomenon called tunneling magnetoresistance (TMR) [13, 14, 15, 16].

Within a ferromagnet, the quantum mechanical spins of the conduction electrons are quantized into two possible vector values: the majority of electrons have their spins aligned up with respect to the magnetic field, while the minority population of electrons will have their spins aligned down. Fig. 3 illustrates the configuration that exhibits switchable TMR. A fixed ferromagnet plate is separated from a free ferromagnet plate by a very thin (e.g. $\lesssim$1.5 nm thick film) insulating barrier. The magnitude of the tunneling current through the barrier is proportional to the product of the densities of spin-aligned electron quantum states in the conduction sub-band of the plates on either side of the barrier. If the magnetizations (and hence the majority electron spins) in the two plates are in parallel, then the majority spin-aligned electrons in the two plates will tunnel more readily across the tunneling barrier. If the magnetizations (and hence majority electron spins) in the two plates are anti-parallel, then the majority spin-aligned electrons in one

plate are inhibited from tunneling to the other plate (and vice versa) because the spin-aligned electron states are in the minority there. Data can be retained in the relative spin orientations of the fixed and free ferromagnetic plates, and the stored data can be sensed by measuring the tunneling current.

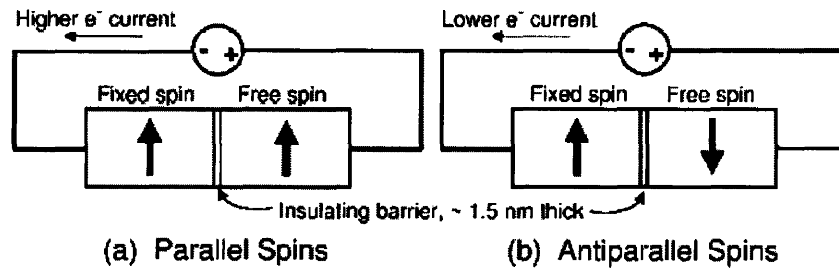


Fig 3: An MTJ and its switching behavior (Source F-3)

The advantages of TMR-based MTJ-MRAM over GMR-based MRAM stem from the far higher MR ratios (about 7% for GMR-based MRAM versus 20% to 40% in MTJ-MRAM).

As shown in Fig. 4, a typical MTJ-MRAM memory cell includes a stack of materials, with an ultra-thin (e.g. $\leq$ 1.5 nm, only a few atomic layers of Al_2O_3) insulating barrier separating two very thin layers of ferromagnetic material (e.g. 10 to 20 atomic layers of iron-cobalt-nickel film). As in a spin valve cell, the magnetic spin orientation in one of the plates is pinned, while that of the other plate is free to be changed. The plates are oblong in shape (viewed from above) to create two preferred magnetizations in the longer (i.e. the easy) direction in parallel with the underlying, unconnected digit line. The digit line is used to create a magnetic field in the shorter (i.e. the hard) direction across the free plate.

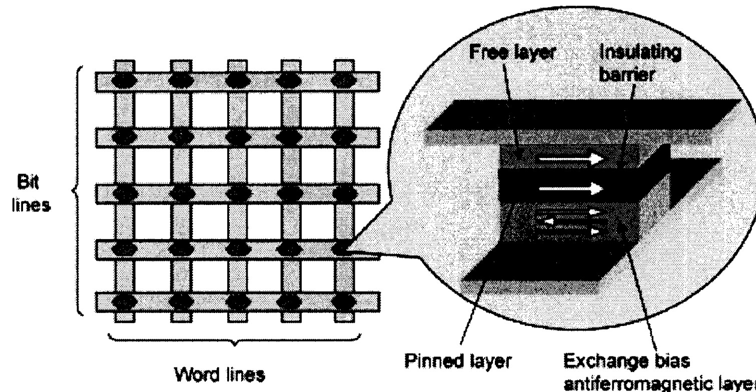


Fig 4: The architecture of an MRAM chip. The blow up displays the structure of MTJ. (Ref. F-4)

The structure of MTJ has continuously improved over the years that has lead to phenomenal improvements on the read/write characteristics as well as its reliability. This is schematically shown in Fig. 5.

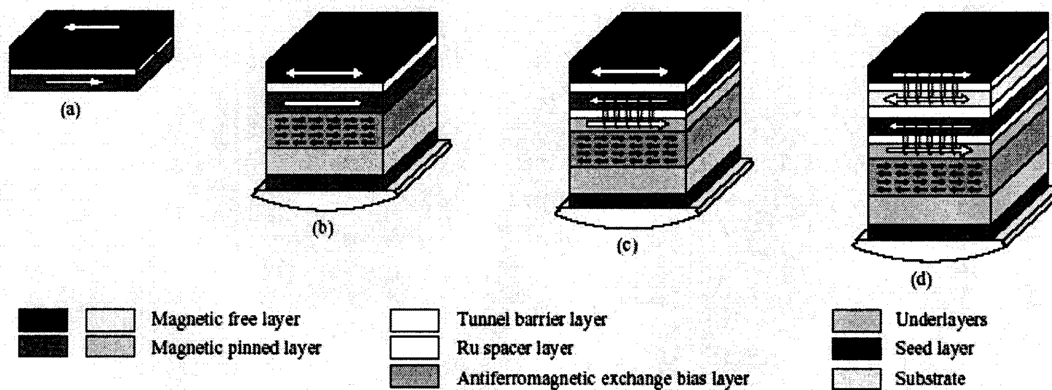


Fig.5: Evolution of tunnel junctions engineered for MRAM applications. (a) Basic magnetic tunnel junction structure consisting of two ferromagnetic metals separated by a thin insulating layer. (b) MTJ with Pinned antiferromagnetic layer (c) MTJ formed by replacing a simple pinned layer with a synthetic antiferromagnetic pinned layer (d) Structure in which both the pinned and free elements consist of antiferromagnetically coupled pairs. (From Ref. F-5)

1.3.5.1 Read mechanism:

Read operations involve passing a sensing current across the tunneling barrier of a single element selectively within an array of elements and measuring the resulting voltage drop. In principle, this is a very simple electronic problem; one connects the top of the MTJ to the bit line and the bottom of the MTJ to the word line. By applying a potential difference

between one bit line and one word line, a current path can be selected that passes through only one element. Hence, the resistance of a single stack can be measured and a single data bit read. Unfortunately, this is not true because of a phenomenon known as "sneak path currents". Fig. 6 illustrates the problem. If current can pass both ways through the MTJs, then current can pass down one element, back up another, and down again through a third. Thus, there will be a component of resistance from all the other elements mixed in with the resistance of the element that is being measured. There are two ways to prevent this. One way is simply to insert a diode in series with each stack, to prevent current coming back up another path. However, the difficulty of integrating a thin film diode with sufficiently little surface roughness on the submicron scale has not yet been solved. The other solution is to integrate a transistor into each cell, allowing a break between each cell and either the word or the bit line. Only a single transistor is switched on during read back of data, ensuring that all of the sense current passes through the element under interrogation. The transistor can be built using standard CMOS processes.

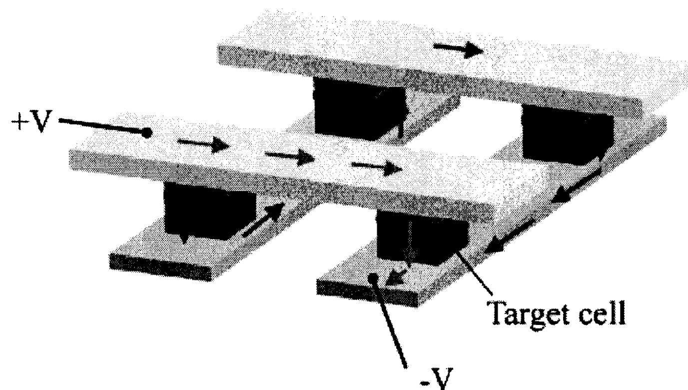


Fig. 6 The problem of sneak path currents during the reading of MRAM cells. The green arrows show the path of the current through the cell that is targeted for reading; the red arrows show how current can also find alternative paths, which mix with that of the target cell, in erroneous data readings. (Ref. F-4)

1.3.5.2 Write operation:

In almost all cases, the MRAM write operation is done by a coincidence of x- and y-currents.

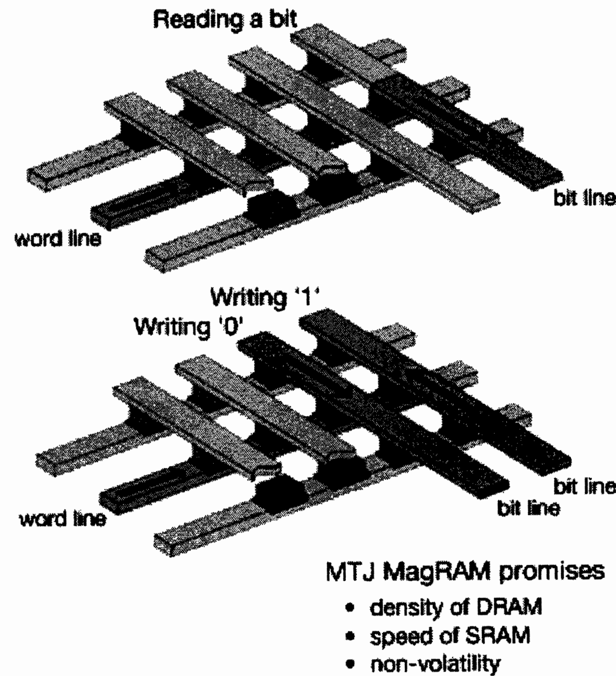


Fig 7: Reading and writing in MRAM (Source F-6)

The write operation in conventional MRAM makes use of the stability boundary curve shown in Fig 8. The boundary curve illustrated is that calculated for a single-domain model of the switching free layer, and is expressed as

$$H_x^{2/3} + H_y^{2/3} = H_i^{2/3}$$

where H_x and H_y are respectively the x and y fields, and H_i is the anisotropy field of the assumed single-domain magnetic element. This functional form is that of a mathematical curve called an astroid, but in the MRAM field the term has generally taken on the meaning of the experimentally obtained switching boundary, which in the best cases only approximates a true mathematical astroid curve.

For field excursions that remain inside the astroid curve, the element is magnetically stable, pointing either to the left or to the right. For field excursions that go outside the astroid curve, the element is written to one definite state.

Many of the largest challenges of MRAM are associated with controlling the write operation, particularly with ensuring that none of the write operations cause an undesired

switching event in any of the half-selected bits (part (a) of Figure 8). Without a carefully balanced pinned layer structure, the astroids can be offset to the right or left. In addition, the element shapes are not perfectly uniform in size, causing the astroid sizes and shapes to vary. Finally, it turns out that the energy barrier that separates the two stable states vanishes as the write field approaches the astroid boundary. Thus, there is a non-negligible probability of the magnetization spontaneously switching by a thermally activated process as this occurs [17]. A more advanced ''toggle'' MRAM write architecture was later introduced by Motorola for a bilayer storage film, as depicted in Fig. 9(d), which considerably lessens the write-control challenges [18].

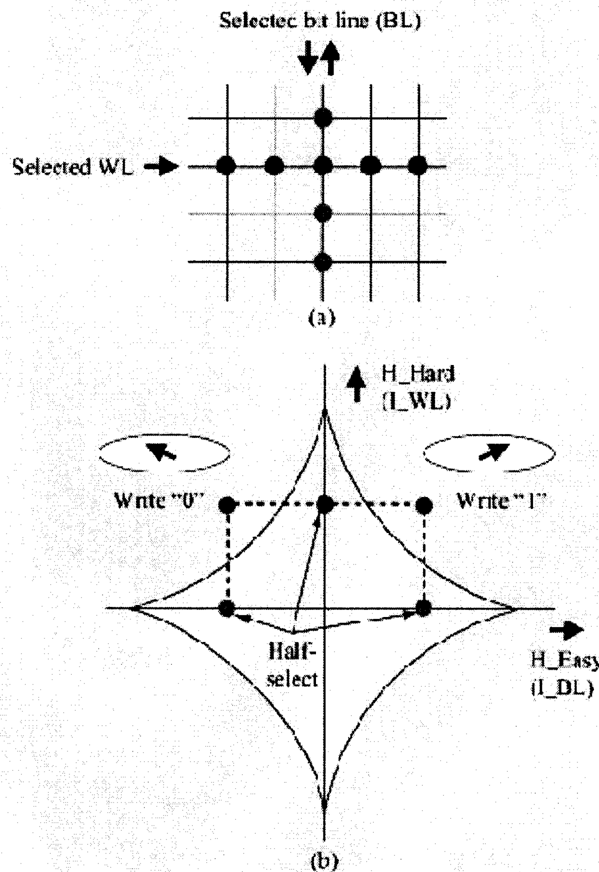


Fig 8: Coincident field selection for writing a magnetic element of an MRAM. (a) Schematic of array with colored dots indicating the selected (red) and half-selected (blue and green) bits. (b) Switching threshold (astroid) curve with appropriate field values indicated for the write operation and with magnetization orientation fields. (Source: Ref F-5)

1.3.6. Toggle MTJ-MRAM

The operating margins of the MTJ-MRAM design described above have been found to be too narrow to allow for sufficiently manufacturable devices [19]. The new toggle MTJ-MRAM (also called as "Savtchenko bit") offers much better operating margins, and could be a significant development [20, 21]. The basic MTJ-MRAM cell is modified as follows: The free plate is formed using a stack of two (or more) ferromagnetic films that have magnetizations that are antiferromagnetically coupled to each other by means of a conductive spacer layer (e.g. of Ru) so as to have roughly opposite magnetizations. Savtchenko switching relies on the unique behavior of a synthetic antiferromagnet (SAF) free layer that is formed from two ferromagnetic layers separated by a non-magnetic coupling spacer layer. This is shown schematically in Figure 9(d).

The synthetic antiferromagnet (SAF) sandwich typically comprises of CoFe/Ru/CoFe, with the Ru thickness being 7-8 A [22]. In this thickness range, the Ru exchange-couples the moments of the two ferromagnetic layers in opposite directions. The new structure dramatically changes the shape of the critical switching curve, as shown in Figure 9(e) [23]. The bit can now tolerate a half-select field many times larger than the smallest required full-select field, thus relaxing the requirement on control of the switching fields from bit to bit. Furthermore, as shown in Figure 9(f), the activation energy under half-select actually increases, thus making the bit more rather than less thermally stable [24]. This essentially eliminates the activated-error problem.

The magnetic poles formed at the edges of each of the two magnetic layers (Fig 9(d)) create dipole fields, which make the two layers line up anti-parallel (AP) in zero field. This flux closure has several ramifications. First, in this flux-closed anti-parallel state, the shape anisotropy does not determine the orientation of the moments in zero field, since there is no net moment. Instead, the zero-field orientation is determined by the intrinsic anisotropy of the two magnetic layers, which is chosen to lie at 45 degrees to the bit lines and word lines (by depositing and annealing the films in a magnetic field). This direction is termed the easy axis. Second, the zero-field activation energy is set by the intrinsic

anisotropy, not by the shape anisotropy, as in Stoner-Wohlfarth switching. Further, the flux closure results in an appreciable reduction in the bit-to-bit dipole field coupling. In the synthetic antiferromagnet configuration considered here, the coupling field, composed of the sum of the dipole and spacer exchange coupling, is substantially smaller, so that the spin-flop switching can be achieved at fields less than 100 Oe.

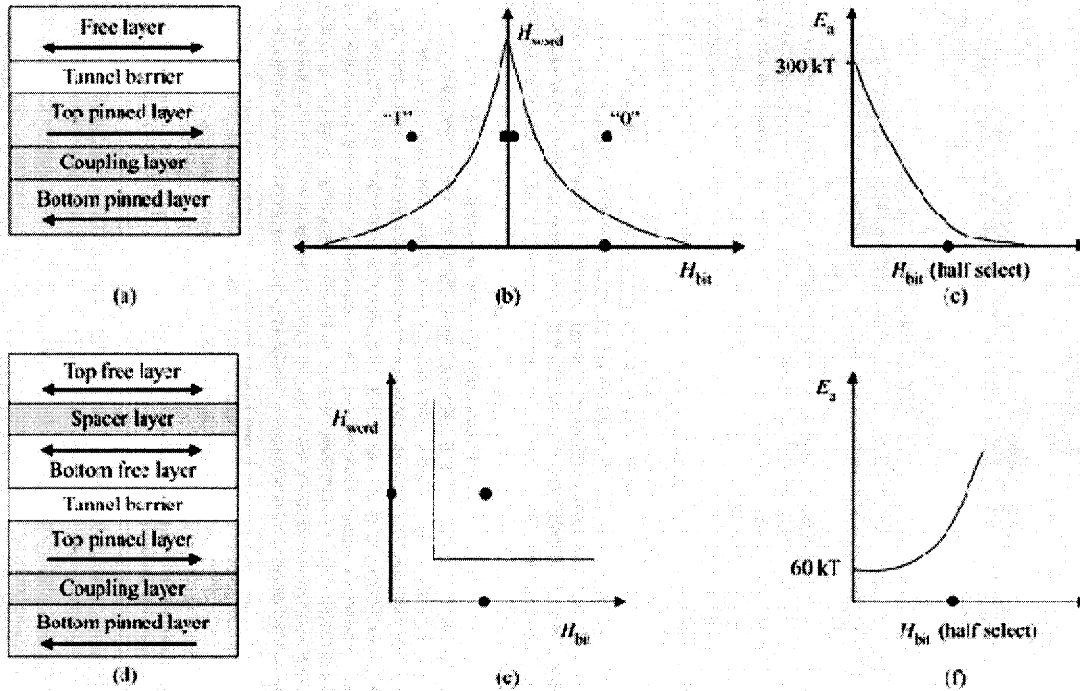


Fig 9. Illustrative switching by Stoner-Wohlfarth reversal (a, b, c) and toggle-MRAM (d, e, f) [F-7]

When a field is applied, the two antiparallel layer magnetizations will rotate to be approximately orthogonal to the applied field, rather than following it. A current pulse sequence is used to generate a rotating magnetic field that moves the free-layer moments through the 180-degree switch from one state to the other, as shown in Fig. 10. Both the free and fixed plates are shaped so as to favor magnetization along an axis that lies at 45° to the X and Y axis of the intersecting digit lines and bitlines, as shown. By pulsing the Y and X-axis currents unidirectionally, a rotating external magnetic field is imposed on the free plate and causes its coupled magnetization components to rotate by 180° with respect to that of the fixed plate.

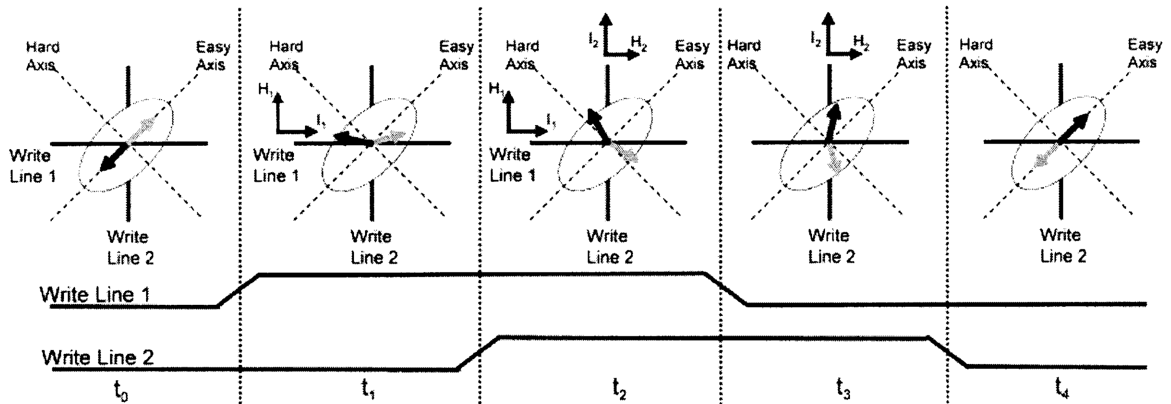


Fig. 10. Schematic of the toggling operation of Savtchenko switching. Pulses are applied in a sequence designed to rotate the SAF 180° to the opposite resistance state (Ref. F-8)

Read operations are performed, as with the original MTJ-MRAM, by measuring the tunneling current, whose magnitude depends on the relative orientation of fixed moment layer and the adjacent free layer. Write operations are performed by initial read operations followed by conditional toggle operations. The toggle MTJ-MRAM therefore incurs the time penalty of a slower write operation. However, as shown in Fig. 11, the operating margins of the toggle MTJ-MRAM are much more relaxed as compared to the conventional MTJ-MRAM. Essentially, it is harder to disturb half-selected cells, which will not experience the required external rotating field, and so the upper bounds on the currents are much higher.

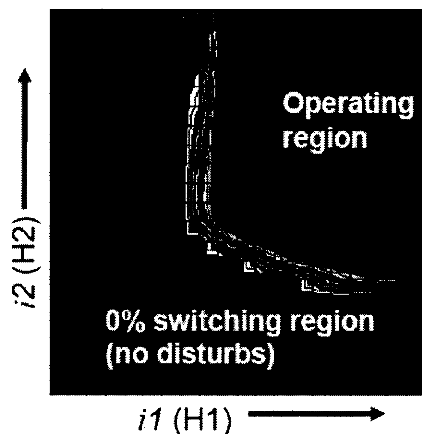


Fig 11. Switching map of an entire 4-Mb die showing the large operating region. (From Ref. F-8)

1.3.7 Spin Momentum Transfer – MRAM:

The toggle MRAM solved a few key issues with conventional MRAMs. However, the problem of scaling down to less than 60 nanometers still posed a problem. One of the significant developments that could be used to circumvent this problem is the spin-momentum-transfer effect (SMT), which was theoretically predicted in 1996 [25,26] and was experimentally observed in 2000 [27].

SMT offers the potential of orders of magnitude lower switching currents and concomitantly much lower energy per bit write. SMT works because of the net angular momentum that is carried by a spin-polarized current and the transfer of this momentum to the magnetization of the free layer. This effect becomes important when the minimum dimension of the memory cell is less than 100 nanometers and becomes more efficient as the cell size is reduced. This is the opposite of what occurs with the use of conventional magnetic field switching, for which the fields necessary to switch a nanoscale cell become larger as the size of the cell shrinks.

The difference between an SMT-RAM and a conventional MRAM is only in write operation mechanism, and read system is the same. A memory cell of the Spin-RAM is composed of a transistor, an MTJ, a word line (WL), a bit line (BL) and a source line (SL). An MTJ has two magnetic layers and a tunnel barrier layer between them, as shown in Fig. 12. One of the magnetic layers is switching layer, and the other is pinned its magnetization direction. A tunnel barrier layer is made of a material like crystallized MgO whose thickness is controlled less than 1nm for the proper resistance area (RA) product of the MTJ. On the write operation, a WL is selected, and positive voltage is applied on a BL or a SL of a selected column. The magnetization direction of a switching layer is controlled by the current direction. On the read operation, a WL is selected, and a voltage of the order of ~0.1 V is applied on a BL of a selected column.

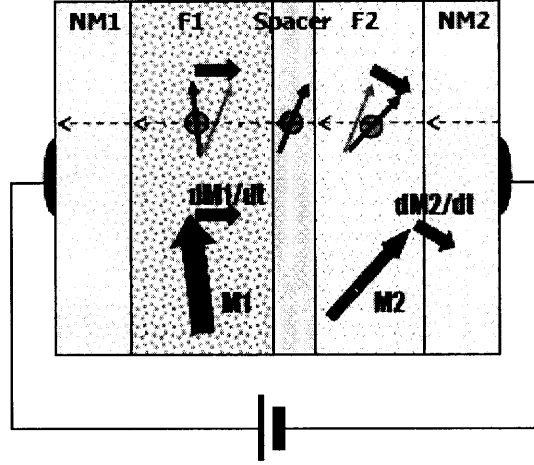


Fig 12. A schematic showing the operation mechanism of spin torque transfer switching. (Ref: F-9)

Quite recently, Sony Corporation fabricated and demonstrated a working model of the SMT-MRAM [28]. In their design, the authors used an STS element that has two ferromagnetic layers, F1 and F2, and a spacer layer in between them. The MTJ in this experiment consisted of a pinned layer (F1), an MgO tunnel barrier layer (Spacer) and a free magnetic layer (F2). When a spin polarized electron flows from F2 to F1, the spin direction rotates according to the directions of magnetic moment M1 and M2. The rotation of spin direction of the electrons in F1 and F2 layer are the origin of a spin torque, $dM1/dt$ and $dM2/dt$, to the magnetic moment M1 and M2. If the given torque is large enough, magnetization of F2, M2, is reversed. Then, the magnetization of F1 and F2 transforms from parallel to anti-parallel alignment (from low resistance state to high resistance state).

According to the authors [28], the switching behavior of the Spin-RAM can be well characterized by the switching current (Ic) and the energy used for the writing process (Δ). Both are simplified as follows:

$$Ic \doteq A * Ms^2 * V$$

$$\Delta = B * Hc_0 * Ms * V$$

where A and B are constants, Ms is magnetic material parameter, Hc_0 is anisotropic magnetic energy, and V is volume of switching layer. As MTJ size decreases, which is

equivalent to smaller V, Hc_0 value increases. Then, Ic is reduced while maintaining a certain amount of Δ. Hence, smaller MTJs will be able to reduce write current according to the theory. This excellent scaling possibility is one of the most attractive features of the Spin-RAM.

Another interesting phenomenon regarding SMT is that the free layer could be rotated in both directions by reversing the direction of the current [27]. This bidirectionality is enhanced when the easy axes of the two magnetic layers have a small misalignment so that the moments of the two magnetic layers (hard and soft) are not collinear.

It appears that SMT switching can significantly improve the performance of MRAM and make it a truly universal memory. A summary of the projected performance of MRAM and SMT-MRAM is shown in the table below, which also includes entries pertaining to the performance of conventional semiconductor memories. It can be seen that SMT-MRAM has the potential to dominate the memory market, particularly because of its nonvolatility and very low power.

	Standard MRAM (90 nm)*	*DRAM* (90 nm)†	*SRAM* (90 nm)†	*SMT-MRAM* (90 nm)*	*FLASH* (90 nm)†	*FLASH* (32 nm)†	*SMT-MRAM* (32 nm)*
Cell size (μm^2)	0.25 256 Mb/cm	0.25 256 Mb/cm	1–1.3 64 Mb/cm	0.12 512 Mb/cm	0.1 512 Mb/cm	0.02 2.5 Gb/cm	0.01 5 Gb/cm
Read time	10 ns	10 ns	1.1 ns	10 ns	10–50 ns	10–50 ns	1 ns
Program time	5–20 ns	10 ns	1.1 ns	10 ns	0.1–100 ms	0.1–100 ms	1 ns
Program energy per bit	120 pJ	5 pJ Needs refresh	5 pJ	0.4 pJ	30–120 nJ	10 nJ	0.02 pJ
Endurance	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$ read, $>10^{6}$ write	$>10^{15}$ read, $>10^{6}$ write	$>10^{15}$
Nonvolatility	yes	no	no	yes	yes	yes	yes

1.4 Fabrication:

1. ***Preparation of the substrate (Fig. 13–1).*** To obtain ideal MTJ device performance, it is critical to achieve atomic-scale flatness over areas of the order of the size of an MTJ. This reduces Néel coupling effects and makes a well-controlled MTJ device [29]. Substrates are thus generally prepared either with a careful silicon wafer

oxidation/cleaning or with the deposition of a dielectric such as silicon nitride on the silicon substrate, followed by a chemical–mechanical planarization (CMP) step to smooth the surface.

2. ***Magnetic film stack deposition (Fig. 13–2)***. The magnetic stack is generally composed of the following layers: a (typically nonmagnetic) seed layer to promote proper polycrystalline growth (e.g., Ta), an antiferromagnet for strong pinning of the reference layer (e.g., PtMn or IrMn), an antiferromagnetically exchange-biased pair of ferromagnets (e.g., CoFe/Ru/CoFe), the insulating tunnel barrier (e.g., Al_2O_3 or MgO), a switchable free layer (e.g., CoFeB/Ru/CoFeB), and a suitably stable cap and hard mask layer (e.g., Ta, TaN, or TiN). Sputtering is used to deposit the metallic layers and the oxide layer is grown by reacting the metal in O_2 plasma.
3. ***Tunnel junction patterning (Fig. 13–3)***. A commonly used, straightforward approach to patterning the MTJs is through the use of a conducting hard mask. Refractory materials commonly used in the semiconductor industry such as Ta, TaN, and TiN are suitable as masks for MTJ patterning. The MTJ shapes are defined in the hard mask by transfer from a first photomask level in a process like the following: apply resist/expose and develop/RIE through hard mask/strip resist. The pattern is further transferred downward to penetrate to (or through) the tunnel barrier, leaving behind a low-resistance base layer, which covers the entire wafer.
4. ***Dielectric encapsulation (Fig. 13–4)***. The encapsulation of the etched MTJs protects them while at the same time forming the environment in which the MT wiring level will be created. The choice of encapsulation is determined from three requirements: a) it must not damage the MTJs; b) it must adhere well to the substrate; and c) it should closely emulate the interlayer dielectrics (ILDs) that would be used in a fully integrated wafer process. The dielectric thickness is chosen such that it will be thick enough to provide the environment for the wiring level above the MTJs.
5. ***Planarization (Fig. 13–5)***. The wiring process adopted is the damascene copper wiring process and hence, the wafers generally undergo a gentle dielectric CMP process at this stage. The purpose of the CMP is to remove topography from the surface that is caused by the underlying MTJs. This step is also the first check of the adhesion of the dielectrics to the underlying metal films, as well as the cohesion of

the metal films to each other.

6. ***Wiring (Fig. 13–6).*** This final step comprises of a photomask-defined trench being etched into the dielectric with RIE. After the trench etching and a suitable cleaning step, the wiring liner film is deposited, along with a thin copper seed layer. This deposition is followed by the electroplating of copper to completely fill the trench and provide enough overburden so that the ensuing CMP step will planarize the metal coincident with the surface of the dielectric. A post-polish cleaning of the wafers is the final preparation step before electrical testing.

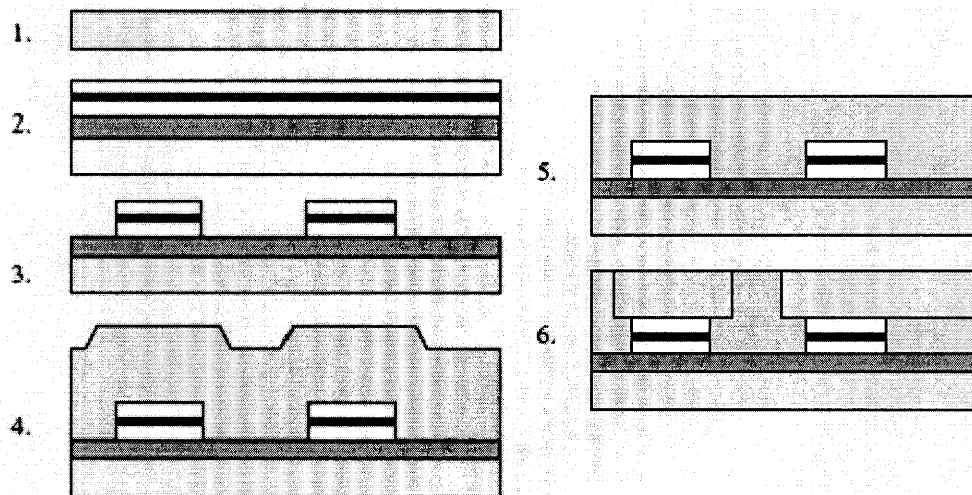


Fig 13. Schematic cross-sectional representation of the basic steps involved in fabricating the short loop. The red lines represent the MTJ tunnel barrier. Source: Ref F-10

1.5 Fabrication Issues:

To accomplish high-density MRAM, the fabrication of a sub-micron MTJ cell array sensitive to cell design and the process, must be a precedent. In light of the fabrication process, the deposition and etching of the MTJ are most critical because the layer-thickness control as well as the spatial thickness uniformity is directly related to the sensing margin. Listed below are a few technical challenges that presently face the MRAM manufacturing process.

1.5.1. Resistance uniformity of sub-micron MTJ cell

The junction resistance is determined by the tunnel barrier (typically, AlOx) thickness. In particular, the resistance uniformity originating from the thickness uniformity of the

tunnel barrier is extremely important since it should distinguish the data status of either 0 or 1 within less than 50% of the resistance difference. Fig. 14 shows how sensitively MR ratio and junction resistance varies depending on the barrier plasma oxidation time. Unlike the resistance that changed linearly as a function of oxidation time, the MR ratio varied nonlinearly. Fortunately, with present day deposition systems, the uniformity of the resistance and the resistance change can be much easily controlled.

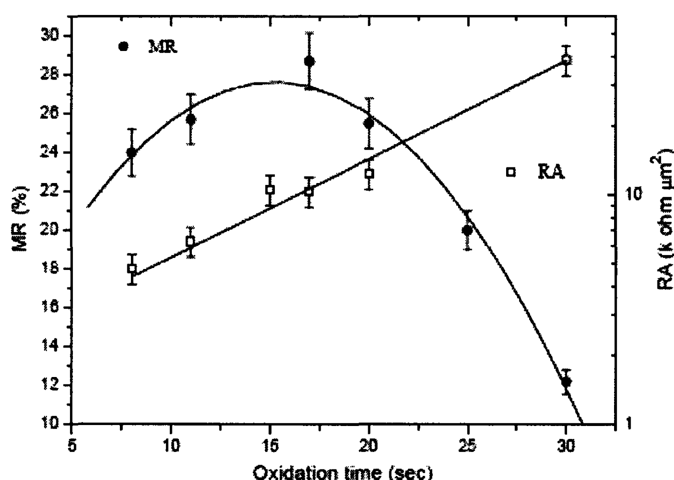


Fig. 14. Variation of MR and resistance in MTJs as a function of barrier oxidation time. From [F-11].

1.5.2 Control on the Switching field:

Another major problem arises due to a spreading of the switching field. This can be avoided or at least minimized by having a very high degree of uniformity in the magnetic properties of the elements. This applies on two levels.

Firstly, the switching field required by one element must be as similar as possible to that required by another element. This requires uniformity in anisotropy across the wafer, which in turn requires identical chemical composition and processing conditions at all points on the wafer. As elements become smaller, however, the switching field will increasingly depend not only on the composition and processing of the magnetic material, but also on the precise shape of the element itself, through a phenomenon known as "Shape anisotropy". Local failures in lithography will, therefore, translate directly into variation in switching field.

The second level on which uniformity applies is the repeatability of the switching process within a single element. One of the surprising observations in the studies of MRAM-like elements is that there can be a large variation in switching field from one cycle to the next within the same element [30]. This is caused by thermal fluctuations, which allow hopping over energy barriers [31] and may select between two competing reversal mechanisms. It is possible to design out these competitions through careful choice of the element's shape. Flat-ended rectangular elements are particularly unpredictable, as the magnetization can form a C-shape, an S-shape [32], or a vortex [33] when it reaches the end of the element. Pulling the flat end of the rectangle out into a point (to form an elongated hexagon) can improve repeatability [34], although forming too sharp a point renders the element very sensitive to small changes in lithographic definition [35].

1.5.3 Half-select instability:

Stability is very important in a memory element. Of particular concern is a problem known as 'half-select instability'. During writing, all of the elements along one bit and one word line are exposed to some magnetic field. According to the Stoner-Wohlfarth astroid, this field should not be sufficiently strong to cause writing to occur, because only one of the required field components is present. These elements are said to be half-selected. However, as one approaches the astroid curve, the stability of the element against thermal fluctuations will be reduced [31]. There is concern that the half-selected elements will have an increased probability of suddenly changing data state, leading to data loss.

1.5.4 Superparamagnetism limit:

Superparamagnetism concerns the loss of magnetic stability as a result of thermal fluctuations that occur when magnetic particles are made too small. This could limit the ability of MRAM to follow Moore's law in the future. As a rule, industry will only invest in the infrastructure needed to establish a new technology if several future generations at progressively higher densities are assured.

Superparamagnetism requires the switching field to be increased in inverse proportion to

the total volume of the magnetic particle. Interestingly, this is easily achievable, either through a change in material from magnetically soft materials, such as permalloy or CoFe, to magnetically harder materials like Fe or FePt, or, as is more probable, through making the element shape more elongated to generate strong shape anisotropy fields. The difficulty comes in then writing data to these stabilized elements: the current density that must be carried in the word and bit lines quickly exceeds the failure threshold of the tracks. Even if the track does not fail immediately, the thermal power dissipation from the chip will be greatly increased, leading to severe thermal management problems. The mathematical form of the dependence of required current density on element size is such that finding new conducting materials that have higher failure thresholds is unlikely to yield much improvement [36]. One of the proposed solution involves [37] heating the antiferromagnetic layer of the MRAM element above its Neel temperature through electrical heating from the currents in the word and bit lines, thus lowering the required write field.

1.6 Research Space of MRAM

In spite of its distinctive advantages, MRAM faces a few hurdles that must be surmounted before it can enter the commercialization stage. Some of the important difficulties are increasing the TMR values, improving the storage density and reducing the current required for switching. However, a number of potential advances in the materials used in MRAM are currently under discussion and experimentation.

At present, most of the research concentrates around increasing the magnitude of the TMR response. This would allow greater tolerances on other aspects of the design, as well as being a prerequisite for some of the future directions of MRAM. One attempt is to change the material in the insulating barrier. Alumina (Al_2O_3) has been the material of choice for most MTJs. However, since Alumina tunnel barriers are amorphous, the maximum TMR that could be achieved is only ~70% [38]. It has been predicted that crystalline tunnel barriers may give rise to much higher TSP and TMR values because of a highly spin-dependent evanescent decay of certain wave-functions, with particular transverse momentum values, across the tunnel barrier [39]. In particular, calculations for

perfectly ordered (100) oriented Fe/MgO/Fe MTJs, suggest TMR values of hundreds or even thousands of percent, for sufficiently thick MgO tunnel barriers [40,41]. Recently, such giant values were realized independently by researchers at IBM and AIST, Japan [42, 43] using crystalline MgO as the insulating barrier, where they reported TMR ratios of ~300%. The impact of such discoveries on various information storage technologies would be immense; for example, MRAM with read performance an order of magnitude greater than current prototypes. This has motivated intense research activities on epitaxial MTJs grown on single-crystalline substrates using molecular beam epitaxy deposition techniques.

An alternative approach is to find a ferromagnetic material with 100% spin polarization that can be integrated into MTJs. The commonly used materials like Ni, Fe, and Co have spin polarizations of less than 80%, which means that the tunnel current is not completely shutoff when the layers are oppositely magnetized. The best devices currently have changes in resistance (called the TMR ratio) of over 40%. A class of magnetic materials called half-metallic ferromagnets [44] should, in principle, provide full polarization, since only one species has any states at the Fermi level. Potential candidate materials theoretically include [45] NiMnSb, PtMnSb, $La_{1-x}Se_xMnO_3$ (LSMO), and CrO_2 – although experimental results to date have not been encouraging.

The TMR ratio is known to decrease with increasing bias voltage, which limits the absolute size of signal that can be obtained during read back. Inomata and coworkers [46] have demonstrated a double tunnel junction in which the TMR depends less strongly on bias voltage and therefore allows high TMR ratios even at moderate bias voltages. The increased fabrication difficulty and cost of a double junction must, however, be taken into consideration.

Efforts have also been made to improve the tolerance limits of the MRAM operation regime. Correct MTJ-MRAM operation depends critically on being able to sense changes in the tunneling current. However, the magnitude of the tunneling current depends exponentially on the thickness of the tunneling barrier. It is therefore critical to maintain tight control on the barrier thickness [47]. Differential and/or self-referencing sensing

schemes have been investigated that are inherently insensitive to the absolute tunneling current in a cell [19]. Variations in the tunneling current can also be masked by the presence of pinhole defects in the insulating barrier, which are hard to entirely avoid when the barrier thickness is less than 1.5 nm [47]. Many variations on the basic MTJ-MRAM cell structure and material composition have been investigated to improve performance and to maximize the operating margins [15, 47].

Advances have also been made in the switching methodology to make the switching robust to disturbances [18, 48] and magnetic cladding of the word lines and bit lines has been used to reduce the write current [15].

As devices scale to smaller sizes, the equilibrium magnetic states and magnetization reversal mechanisms are strongly determined by the interplay of magnetic anisotropies with the physical shape of the element. In fact, on the micrometer scale the shape of the element so fundamentally influences the switching behavior of the magnetization that a large effort has been spent with the purpose of finding the geometries that provide the simplest, fastest, and most reproducible switching mechanism, which are essential prerequisites for device applications [49, 32, 50-53]. Different geometries have been studied for this purpose, from simple circular discs [51, 54] to more advanced needle-shape elements [55]. The magnetic configuration in these elements is defined by the shape of the edges and is very sensitive to shape fluctuations and edge roughness. Thus the switching mechanism in these elements is quite complex. One possible way to overcome these complications in circular elements is to use the vortex state in which the magnetic flux is closed in the element and where the edge roughness and edge domains play a minor role. The zero stray field in this state will also favor high-density storage. However, the vortex is only stable in discs for diameters above some 100 nm [51], depending on the thickness and the material, which limits the density achievable. Moreover, the vortex formation is complex and hard to control [51, 53]. The vortex state can be made more stable if the highly energetic vortex core is removed by using the high-symmetry ring element [56] (Fig. 15), which has been proposed for use in MRAM [49, 57].

Fig. 15. Schematic representations of the vortex state in a ring and a disc. (Source: Ref. F-12)

Current research on MRAMs conducted by Prof. Ross' group at MIT focuses on using a ring-shaped magnetic element which can be scaled down to the order of a few hundred nanometers [58] due to the minimal interaction between these type of elements. Further, these ring structures have the capability to store multiple bits with a high degree of reliability and are responsive to ultra-fast switching.

Two stable vortex configurations, clockwise and counterclockwise vortices, are known to exist in a ring element at remnant state. For MRAM applications, two stable vortices would be used as two distinct bit states, 0 or 1. However, specially designed conducting wires are required, as suggested in a vertical MRAM structure [59], to achieve pure vortex switching. In order to avoid the complex wiring system, an idea on magnetic switching of ring elements by an in-plane magnetic field was sought. Thus, an asymmetric ring element was proposed by a few researchers [60, 61] to meet the in-plane field switching. In this shape, magnetization reversal occurs by the motion of domain walls nucleated at a notch or naturally produced defect during the fabrication process. Recently, two stable magnetization configurations, namely "onion" states, were observed at remnant state in a narrow ring element [62]. The onion state has two symmetrical single domains with head-to-head (HTH) domain walls. A ring element with the onion state rather than the vortex state is more favorable for two-bit states in MRAM devices because it is easier to switch the onion state configuration by an in-plane applied field [62].

Much effort is currently being focused on finding new ways to make use of the spin degree of freedom, as well as the electron's charge. A relevant example of this to the future development of MRAM is the newly discovered phenomenon of spin transfer.

First predicted in 1996 by Slonczewski [25] and Berger [26], the spin transfer effect exploits the fact that when a current flows through a ferromagnetic material, the conduction electrons become spin polarized. If these electrons then pass into another magnetic layer, there will be an interaction between the spin polarization of the carriers and the magnetization of the new host material that can lead to precession of the magnetization. An elegant experimental verification of this has recently been published [28] in which an MRAM cell was switched purely by passing an electrical current through it. No magnetic field was involved in the switching process at all. Spin transfer may provide the solution to superparamagnetism in very small MRAM elements, as a much stronger action can be generated in small elements than could be achieved through the equivalent classical magnetic field. It should, therefore, be possible to stabilize the elements against thermal fluctuations and still be able to write data. It should be noted, however, that the lithography involved in the narrow, nanoscale pillars required to access spin transfer is nontrivial.

Although SMT should contribute significantly to the write speed of MRAM, extremely large magnetoresistive ratios approaching 300% using MgO tunnel barriers [42, 43] should significantly improve the read speed. The overall expected improvement is by a factor of 2 or 3 [63]. Additionally, for performance-optimized MRAM, the overall performance could be improved by a factor of 5 to 6, that is, to 4 to 5 ns compared to 25 to 30 ns in the first MRAMs.

One of the more exotic developments of MRAM would extend its scope from purely memory into digital logic. Many of the advantages promised by MRAM (nonvolatility, radiation hardness, rapid writing, and high density) would be equally appreciated in logic devices such as microprocessors, especially for mobile or highly distributed applications. Some researchers have proposed the concept of nanoscale magnetic logic. One way of viewing this new paradigm would be as a MRAM cell that not only stores information, but can also process it – in short, MRAM that thinks. Richter and coworkers [64] have developed a reconfigurable logic system that uses MRAM cells to define the routing and functionality of the logic circuit.

1.7 Latest developments at Industry

One of the major breakthroughs in the recent times in the field of MRAM was brought out by the IBM – Infineon partnership [65] when they announced the 16 MB prototype in mid-2004. The development of a new 0.18 μm MTJ deposition equipment had made this achievement possible.

Late year before last at the IEDM (International Electron Devices Meeting), several key developments were reported by various companies. The Renesas and Mitsubishi partnership announced new developments [66] in the choice of a new magnetic material, CoFeB (ferrocobalt boron) that produces better results than with the CoFe used previously in Renesas MRAM, including a 30 to 70% higher magneto-resistance ratio.

Using these developments, it is possible to achieve data read times of 5.2ns, making the read cycle approximately 7ns. Furthermore, Renesas claims, it is the world's smallest memory cell at 0.81 square microns.

At the same conference, Toshiba, working in partnership with NEC, announced its new cell architecture based on a cross-point cell [67]. The architecture does have transistors though: it's a kind of hybrid with four cross point (CP) cells controlled by each transistor.

Toshiba says that the new cell architecture realizes a CP cell with fast read times. A typical read time of 250ns is still four times faster than for conventional CP cells, and the cells are the same size as conventional DRAM and CP MRAM.

Toshiba and NEC have also pioneered a new shape for the MTJ; a rectangle with arc shaped bulges on either side. This new shape is responsible for halving the write current compared to previous technology and it reduces write errors (despite fluctuation in the switching characteristics of the cell). The prototype is a 1Mbit chip fabricated using 130nm process technology; it operates on 1.5V.

However, one of the most exciting disclosures in the very recent past was made by Sony Corporation [28]. Late last year, Sony presented details of a type of magnetic memory that utilizes spin torque transfer to effect the switch in magnetic fields, rather than rely on

a current to switch magnetic field in the magnetic tunnel junction (MJT). Sony refers to the new MRAM device as Spin-RAM, and demonstrated a 4 kbit Spin-RAM device that was fabricated on a 180 nm process with 4 metal layers of interconnect. Sony further states that write speed as fast as 2 ns and write currents as low as 200 μA were successfully performed on the test Spin-RAM device. Also, Sony claims that the new Spin-RAM cell structure shows great promise in terms of scalability to 45 nm and future processes, and that reliability of the Spin-RAM cell has been demonstrated through more than 10^{12} write cycles. This was an important discovery as this brings down the write current densities (currently ~ 0.8 MA/cm^2) to less than 1 MA/cm^2 which is considered as a maximum threshold value for a write technology to be scalable.

Chapter 2: Market Analysis for MRAM

2.1 MRAM Market Drivers

MRAM appears to offer some significant advantages that serve as its key drivers:

1. MRAM could "at least potentially" combine the density of DRAM with the speed of SRAM and non-volatility of Flash or disk. This means that a single MRAM chip may replace two chips – RAM and Flash – in certain types of products.
2. MRAM is rad hard, which makes it valuable for military applications.
3. MRAM can withstand shock, magnetic fields and moderate amounts of heat with ease.
4. It has better (more stable) write characteristics than Flash.
5. The manufacturing process for MRAM is already familiar to the semiconductor industry and the technology is similar to that of GMR read heads for disk drives.
6. MRAM generally has good thermal and power consumption characteristics. This will be especially attractive in mobile computing and communications applications, an area to which several MRAM firms are targeting their products.

2.2 Retarding Factors:

MRAM has proved more difficult to commercialize than many of its backers expected and significant problems must still be overcome:

1 MRAM remains an expensive solution, although this is expected to change as volume production ramps up. At present MRAM is likely to prove economical only where either (1) an MRAM chip will replace a Flash and a RAM chip or (2) some characteristic of MRAM offers a clear and distinct competitive advantage, as is the case for MRAM's rad hardness in certain aerospace and defense applications.

2 MRAM scaling remains an important technical challenge. The first generation of MRAM is well below the capacity of today's conventional RAM or Flash chips. MRAM will eventually catch up, but will take several years to do so.

3 Possible long-term legal challenges over patent issues seem likely.

2.3 Competition

At present, there are a number of alternative memory technologies that are being pursued to find the ideal memory that has the attributes of non-volatility, scalability and low cost. Any successful technology that has these attributes will most certainly be a strong competitor to MRAM. In this report, three main embryonic technologies – FeRAM, OUM and 3DM – are being juxtaposed against MRAM.

2.3.1 FeRAM:

Ferroelectric RAM (FeRAM or FRAM) is a type of non-volatile computer memory that is similar in construction to DRAM, but uses a ferroelectric layer – typically lead zirconate titanate (PZT) – to achieve non-volatility. The ferroelectric crystal is placed in between two electrode plates to form a capacitor and holds the data being written and read from the memory cell.

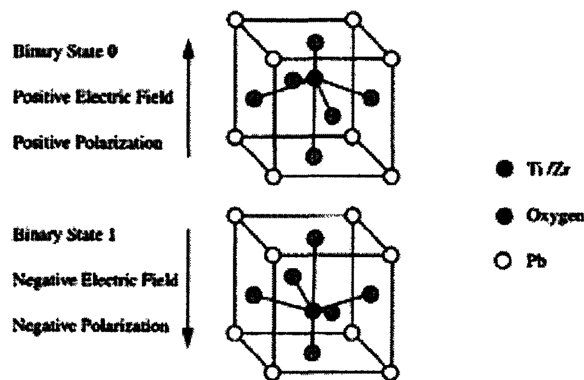


Fig 16: Unit cell structure of a ferroelectric crystal – PZT (Source: Ref. F-13)

The central atom moves according to the direction of the electric field as shown in Fig. 16 when the electric field is applied to the ferroelectric crystal. The way the reading and writing works is that when the atom moves inside the crystal, it passes through an energy barrier, which causes a spike that is detected by the circuit, which sets the memory. The central atom stays in its position even after the electric field is moved, therefore preserving the data. Even if there is a power failure, the FRAM would not lose any data and there is no need for periodic refreshing of the FRAM memory because it retains its data.

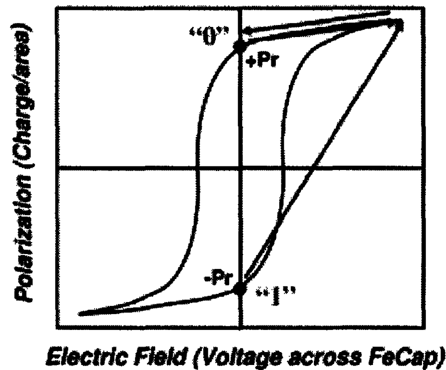


Fig 17: Hysteretic behavior of a ferroelectric material (Source: Ref. F-13)

Operationally FeRAM is similar to DRAM. Writing is accomplished by applying a field across the ferroelectric layer by charging the plates on either side of it, forcing the atoms inside into the "up" or "down" orientation (depending on the polarity of the charge), thereby storing a "1" or "0". Reading, however, is somewhat different than in DRAM. Instead of draining the charge, the transistor instead forces the cell into a particular state, say "0". If the cell already held a "0", nothing will happen in the output lines, whereas if the cell held a "1" the re-orientation of the atoms in the film will cause a brief pulse of current in the output (as they push electrons out of the metal on the "down" side). The presence of this pulse means the cell held a "1". Like DRAM, reading in FeRAM is a destructive process, and requires the cell to be re-written after reading (at least if the state was changed).

Much of the current FeRAM technology was developed by Ramtron International. One major licensee is Fujitsu, who since 1999 has been producing standalone FeRAMs, as well as specialized chips (e.g. chips for smart cards) with embedded FeRAMs within. Several other companies are known to be active in developing FeRAM. For example, since at least 2001 Texas Instruments (TI) has collaborated with Ramtron to develop FeRAM test chips in a modified 130nm process. In the fall of 2005 Ramtron reported that they were evaluating prototype samples of an 8-Mbit FeRAM manufactured using TI's FeRAM process. Fujitsu and Seiko-Epson were in 2005 collaborating in the development of a 180nm FeRAM process. FeRAM research projects have also been reported at Samsung, Matsushita, Oki, Toshiba, Infineon, Hynix, Symetrix, Cambridge University, University of Toronto and IMEC.

The main advantages of FRAM are it has a relatively fast read/write speed and is claimed to have much higher endurance than Flash memory. On the other hand, some problems with FRAM include issues with CMOS integration due to Hydrogen exposure intolerance and requirement of specialized materials in fabrication. Another problem is the inability to operate at high speeds that it is capable of. The reason for this is because of its reading process. It actually reads the data, destroys it, and then rewrites it again after being read. This consumes a bit more time than simply having to read it without having to restore it back. Most importantly, the scalability of FeRAM is largely doubtful as the lowest scale limit seems to be defined by the amount of charge needed to trigger the sense amplifiers and at around 55 nm, the charge stored in the PZT layer may become too small to be detected.

When compared with FeRAM, MRAM has distinct advantages in read/write speed which are governed just by the alignment of magnetic moments. The endurance level for MRAM is at least theoretically infinite where as for FeRAM it is around 10^{10} times due to its destructive read process.

2.3.2 OUM

Ovonic Unified Memory (OUM) is a phase change memory, which uses a reversible structural phase change – between amorphous and crystalline states – as its data storage mechanism. This is made possible by using a chalogenide alloy material. Basically, chalogenide alloy materials use one or more elements from column VI of the Periodic Table. OUM devices use an alloy system of GeSbTe (Germanium-Antimony-Tellurium). The basic operation mechanism of OUM technology is schematically showed in Fig. 18.

The phase change is made possible by heating a small volume of the material with a current pulse to make the transition. As shown, applying a well-designed voltage pulse of a particular amplitude and duration would transform the material from the amorphous state to the crystalline state ("write"). Using another voltage pulse of higher amplitude and shorter duration, would push the crystal back into the amorphous state ("erase"). The resistance contrast of the 2 states might be as high as 3 orders, and the state could be identified ("read") by a pulse of moderate amplitude and duration.

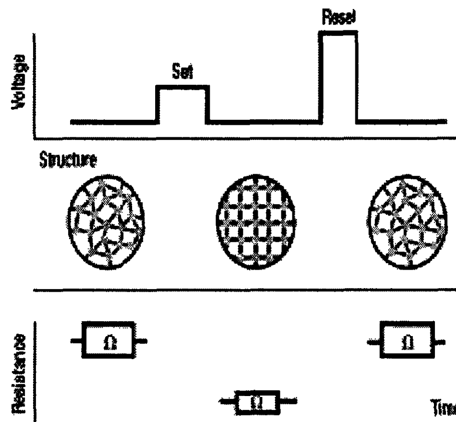


Fig. 18: Operation principle of a memory based on phase change materials (Source: F-14)

OUM is both solid state and XY-addressable, and is an attractive candidate for commercial use as non-volatile computer memory. The ability to read and write with fast speeds puts OUM at a good competitive stance with current popular technologies like Flash memory. Another advantage includes high scalability, which would translate to lower costs. Also, as cell size decreases, the energy required for the phase change should theoretically decrease so the write current needed should scale with the chip.

However, as suggested by Intel, thermal proximity is a concern with OUM devices as their size decreases. Further, as the devices are scaled to smaller sizes, the margin for resistivities becomes smaller, which could impact the read performance. Yet another challenge is the reduction of programming current for lower voltage and lower power operation. Much of these issues still remain to be addressed.

In striking contrast, MRAM is much more evolved and many key issues like the reduction of write current and reliability have already been successfully addressed (in toggle MRAM). Further, the demonstration of Spin-MRAM has opened up a new paradigm with respect to scalability. Thus MRAM looks to be in a much stronger position than OUM technology.

2.3.3 3DM - 3-Dimensional Memory Technology

Matrix Semiconductors has revived a concept that was tested in the 1980's without much success. Matrix plans to use 3-D technology to change IC design from its typical 2-D

form. Instead of shrinking geometries to reach higher densities, lower costs, and increased performance, Matrix has decided to extend vertically from the base. Fig. 19 shows a comparison between 3-D and 2-D architecture. In 2-D IC architecture, the active circuitry rests on the silicon substrate and other layers of insulators and interconnects function as wiring and mechanical strength. On the other hand, in 3-D IC architecture, the active circuitry is deposited in multiple layers on the silicon substrate.

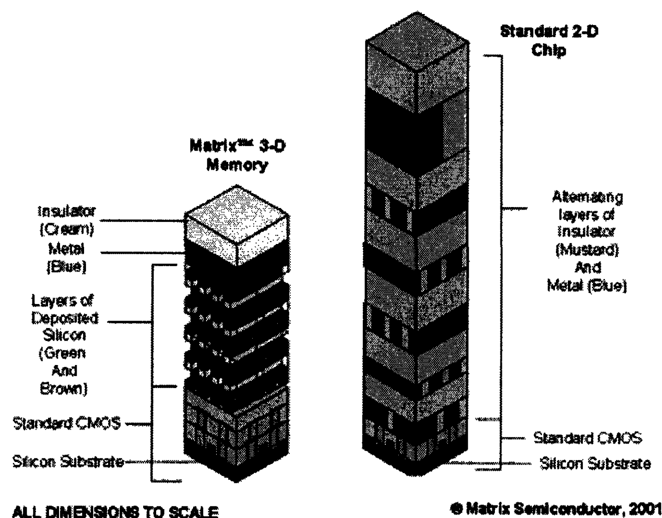


Fig. 19: 3-D vs. 2-D IC architecture. (Source: Ref. F-15)

By utilizing the silicon real estate more efficiently, much cost can be saved. While Flash memory chips can cost $15 each, Matrix chips with similar capacity cost about $9 each. In November 2004, Matrix brought the density to new levels by moving its original design levels of .25 microns to .15 microns. Though this all sounds great, 3-D memory has its catch: it is one time programmable. Fig. 20 shows a Matrix memory chip. Between the wires are microscopic fuses that when blown record data. This process makes data permanent on the chip.

Hence, data can be written only once, and as a consequence, it cannot enter the "infinite write" non-volatile memory segment, which happens to be the prime market for MRAM.

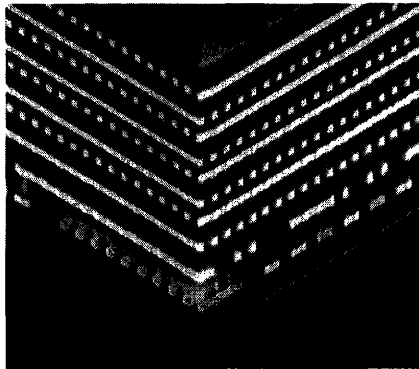


Fig. 20: This picture of a Matrix memory chip shows white bars (wires) and white dots (wire ends). At wire crossings, an electrical charge can blow the fuse. (From Ref. F-15)

2.4 Comparison with Other Memory Technologies

A comparison between MRAM and other ***incumbent*** technologies is given below:

Category	*Parameter*	*SRAM*	*DRAM*	*NOR Flash*	*MRAM*
Cost	Cell area	3.7 μm^2	0.56 μm^2	0.5 μm^2	0.7–1.4 μm^2
	Process cost adder	0%	25%	25%	25%
Performance	Read access	3.3 ns	13 ns	13 ns	5–20 ns
	Write cycle	3.4 ns	20 ns	5 μs	5–20 ns
Power	Data retention	0.6 nA per bit at 85°C	0.2 nA per bit at 85°C	0	0
	Read active	15 pC per bit	7 pC per bit	30 pC per bit	7 pC per bit
	Write active	15 pC per bit	7 pC per bit	30 nC per bit	45 pC per bit
Miscellaneous	Write endurance	Unlimited	Unlimited	10^5 cycles	Unlimited

It can be seen that MRAM has a much higher density than SRAM with the ability to hold data without any refresh power. Another point that is hard to escape our attention is the fact that MRAM has superior characteristics over flash point for point. This makes it extremely attractive to enter both the primary as well as the storage memory segments. The attributes cited here are for the current MRAM designs that are primarily based on the toggle-MRAM architecture. However, future MRAMs will be predominantly based on the Spin-torque-transfer effect and could be expected to have even better characteristics.

As discussed in the previous section, there are a number of other memory technologies that pose competition to the MRAM technology and an assessment of the latter will not be complete without a comparison with the former. Listed below in the table is a comparison between MRAM and a few ***emerging competing*** technologies:

Attribute	FeRAM	OUM (CRAM)	MRAM
Storage mechanism	Ferroelectric capacitor	Amorphous/ crystalline resistivity	FM moment orientation
Read speed	Fast	Fast	Fast
Write speed	Fast	Medium	Fast
Endurance	$>10^{10}$	10^{12}	Infinite
Power	Low	Low	Low
Potential cell density	Medium	High	High
Non-volatility	Yes	Yes	Yes

MRAM appears to be much superior to both FeRAM and OUM – its two main competitors – at least on paper.

2.5 Key Markets for MRAM

It may not be an exaggeration to state that universal memory, which some in the memory industry still dream about will be hard to realize entirely. Nonetheless, MRAM comes closer to this dream than any other commercial product. The main markets for MRAM along with the trends in the respective market segment as well as the problems associated with entering the same are listed in the table that follows.

Market	Market Trends	Need for MRAM	Problems with MRAM
Mobile Computing	Growing rapidly thanks to ubiquitous broadband deployment	Need for high density/capacity for always-on pervasive computing applications	Expensive for all but high-end applications
Cell phones and other handhelds	Cell phones and similar devices becoming multifunctional business tools	Need for high capacity non-volatile RAM--cell phones don't usually have disk drives. Key market for many MRAM firms	MRAM is still too expensive except for high- end smartphones. Some current MRAMs may be too big for this application.
Portable recording and playback devices	Success of iPod provides this market with a lot of attention.	High storage capacity key to success, as HDTV storage becomes common	Same issues as handhelds. MRAM must show clear advantages over mini-disk drives
Home computing and consumer electronics	Home computing becoming part of consumer electronics	Non-volatile RAM useful for instant boot ups. High density could lower the line between portable and fixed devices	Non-volatile memory is not as useful as in mobile communications which is driven by batteries
Enterprise computing and telecommunications	IT spending is beginning to revive and telecom slump is over the worst	This segment is relatively price insensitive--might boost use of MRAM for instant boot ups, BIOS and specialist applications	The segment seems to be mostly satisfied with conventional technologies
Control systems and embedded computing	Over 90 percent of processors are sold into this segment which is benefiting from a renewed interest in low-cost robotics	Much of the market seems to be satisfied with conventional memory. Visual and robotic systems may need especially fast, high-density memory	Price will be an issue for low-end applications especially in the automotive business.
Sensors, smart cards and other "disposables"	Sensors in need for medical homeland security RFIDs being deployed rapidly in retail and other applications	Broad need for non- volatile memories,	Low cost will be critical here, but Micromem is specifically targeting RFID market.
Military	Military focus for technology is considerable given geopolitical situation	Rad hardness very important	Many alternative memory technologies

2.6 Market estimates:

2.6.1. Computing/handheld Memory segment:

The following plot shows an estimate of the non-volatile and total memory segment across the computing industry. It can be seen that there is an increasing demand for memory in general and non-volatile memory in particular due to the ever increasing consumer base that keeps itself up to date with the latest computing technology – mobile or otherwise. According to this estimate by BCC research group, the expected market for

the non-volatile memory is expected to touch $70 billion in another 4 years, which is 3 times as that of today. This can essentially be explained due to the introduction of new memory technologies by then. Flash would have reached its limit by then and hence will have to be replaced by a much superior technology – the key contender here being MRAM.

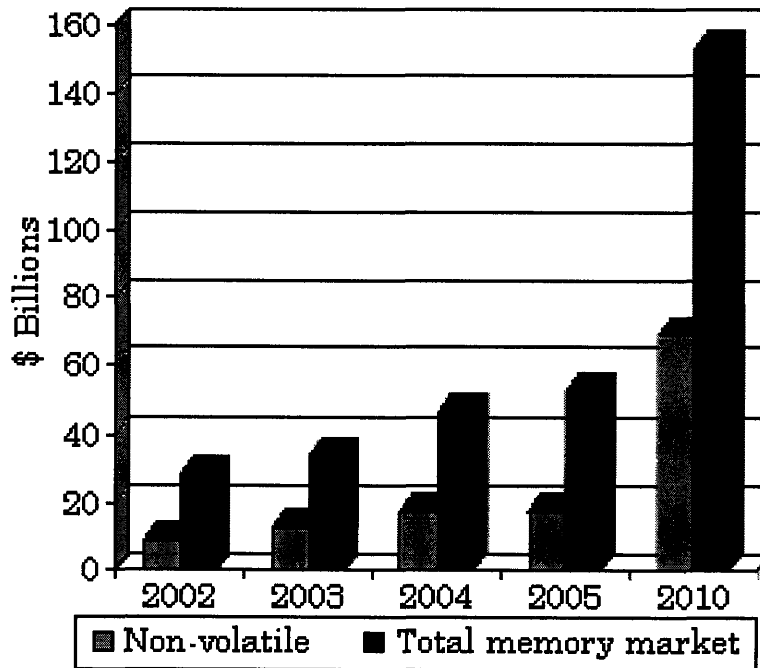


Fig 21: Worldwide Non-Volatile and Total Memory Markets, 2002-2010 ($ Billions). Source: [F-16]

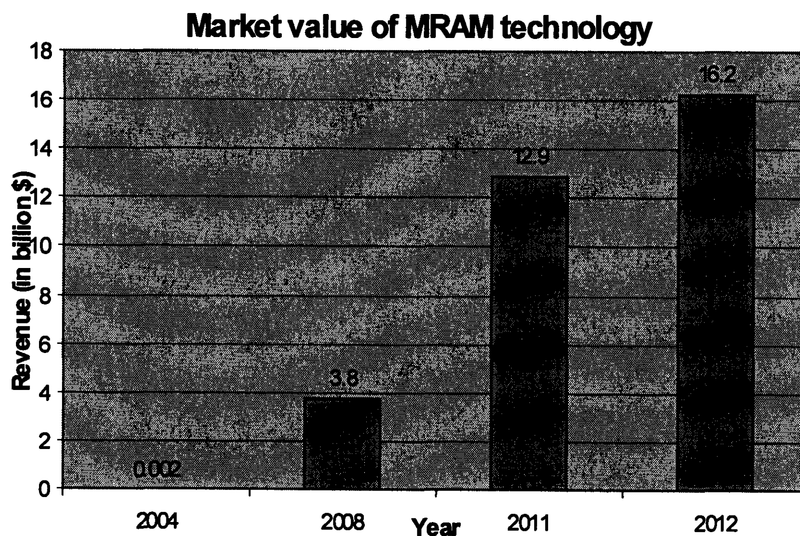


Fig 22: Market estimates for MRAM technology based applications. Data from Ref. F-17

The estimates for MRAM market as projected by Nanomarkets, Inc. seem to indicate that though there might be other concurrent players in the non-volatile segment, MRAM will still have the maximum share of the memory market.

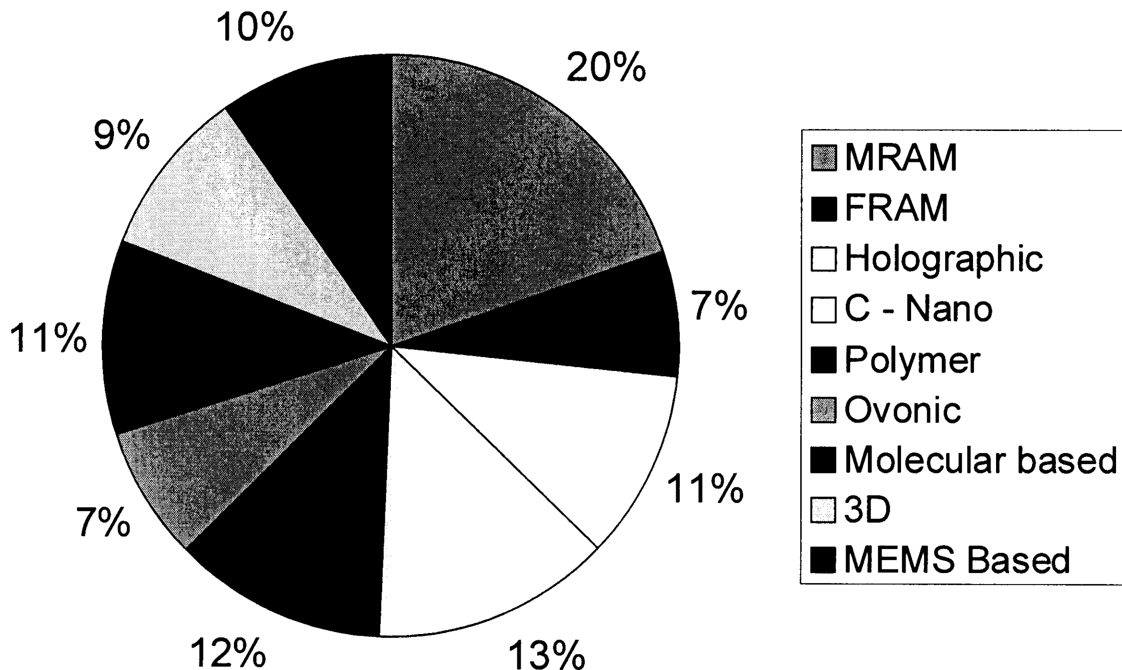


Fig 23: Projected market shares of top nanotechnologies in the year 2011. Data source: Ref. F-18

The above statement is supported by another estimate from Forbes, Inc. that predicts MRAM to have a major share (~20%) of the nanomemory market segment that is pegged to have a total value of $65.7 billion. Thus the potential market size that MRAM could enter is huge and hence an appropriately timed entry into this segment (when flash would have reached its limit – say around 2008-2009) could return rich rewards.

2.6.2 RFID applications:

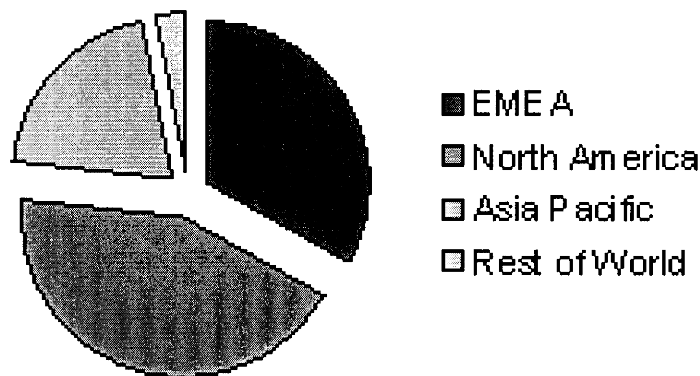
Since mid-2003, WalMart, the Department of Defense, Target, and several large non-US organizations have stated that their top 100 suppliers must have RFID tags on all pallets delivered after 2005. It is estimated that the use of RFID tags, help save an industry giant such as Wal-Mart $1.3 billion to $1.5 billion annually due to the following reasons.

1 Improved fulfillment rates
2 Reduced shipping errors

3 Fewer out-of-stock situations

With a good demand for RFID tags from the above players, the total market size in this area is estimated to be around $7 billion with major contributions of $2.7, $2.0 and $1.4 billion from the North American, EMEA (Europe and Middle East) and the Asia Pacific regions by 2010.

Estimated value share of RFID market in 2010, by region (%)



› DATAMONITOR

Fig 24: Market shares for RFID from different regions. (Source: Ref. [F-19])

Current RFID tags are predominantly made using EEPROM that has the following problems:

1 Poor write endurance (100,000-1,000,000 write cycles),

2 Slow write time (~10ms)

3 High write power (12V)

Replacing EEPROM with an embedded MRAM (EMRAM) can lead to the following advantages:

1 Unlimited write endurance,

2 Writes with no delay (20 ns)

3 Consumes less power (write voltage 5V)

4 Reduces cost ~20% due to the reduction of die size by 50%

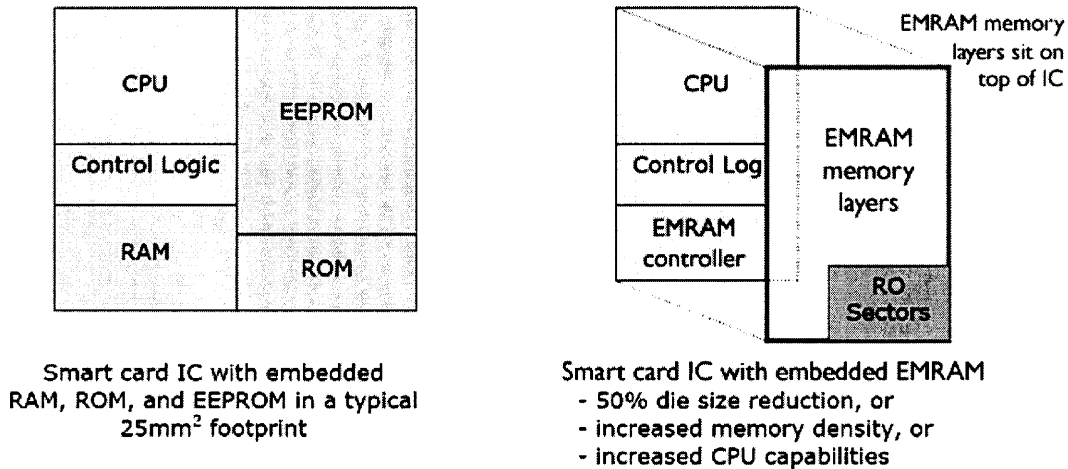


Fig 25: Comparison of EEPROM and EMRAM. From Ref. [F-20].

Thus, for the RFID market, MRAM promises to provide a faster nonvolatile memory than the existing EEPROM and flash memory. MRAM is also a denser memory type, which means that an MRAM chip can offer a higher amount of storage capacity for its size than can chips using other existing memory technologies. Further, for these applications, we do not need a very dense memory like that of DRAM which means entering this segment is much easier than entering the heavily crowded computer memory segment.

The fields in which RFID tags find applications are numerous:

1. Ticketing and access-control
2. Contactless payment cards – Total number of VISA and MasterCard® cards are estimated to be around 4.5 billion. Hence, even a conversion rate of 10% would provide a huge market.
3. Tagging patients, staff and assets in healthcare facilities for error prevention
4. Antiterrorism measures in global logistics
5. Meat and livestock tagging in the face of new legislation against disease
6. Tagging of high value banknotes and drugs for anticounterfeiting

2.6.3 Sensor Market

The research on MRAM technology has advanced the knowledge in the area of spintronics to the extent that several GMR based sensors have already started to make a

huge impact in the sensor technology. The chief advantages of these novel sensors are:

1. Smaller size – critical for medical applications.
2. More sensitivity
3. Cheaper
4. Robust

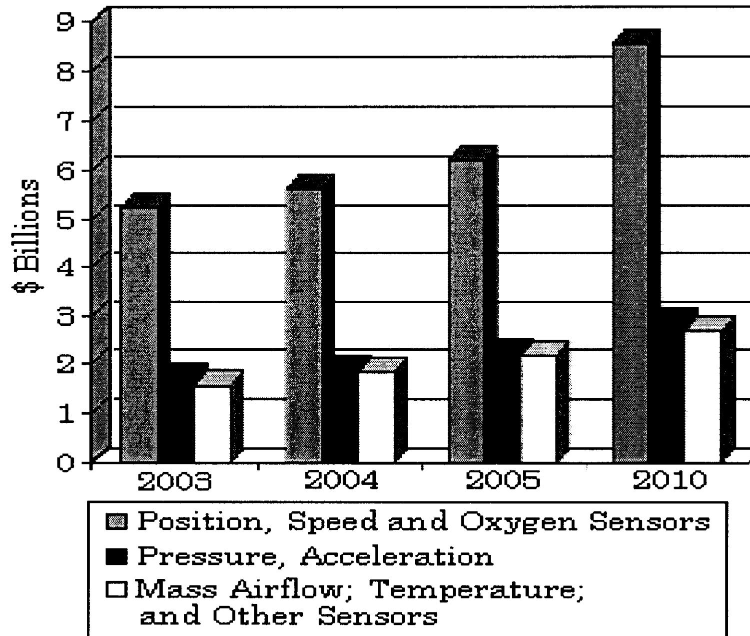


Fig 26: Projected market values of a few key sensor segments in automotive industry. [Source: F-16]

The main market in this segment is driven by three main contributors:

1. Medical Market - $600 million in 2003 projected to reach $845 million in 2008
2. Automotive sensors ~ $8.5 billion in 2010
3. Traffic monitoring, Detection of landmines.

2.7 Most Likely Choices for Commercialization

Although there are many useful applications of MR technology, not all of them will see the push towards commercialization and implementation. The two applications that will most likely see a big push towards commercialization are RFID related electronics and magnetic sensors. Both applications cover a broad range of both consumer and government needs, and are the focus of most of the research that is going on about MRAM today. According to the Mc Kinsey Diagram, they are both new technologies that

can be implemented in old markets. This indicates that the success of the new technology is driven by cost, meaning that if the specific application of MRAM technology can compete with the old technology in terms of overall cost, then the paradigm will shift. The Mc Kinsey diagram for both applications is shown below in the following figure.

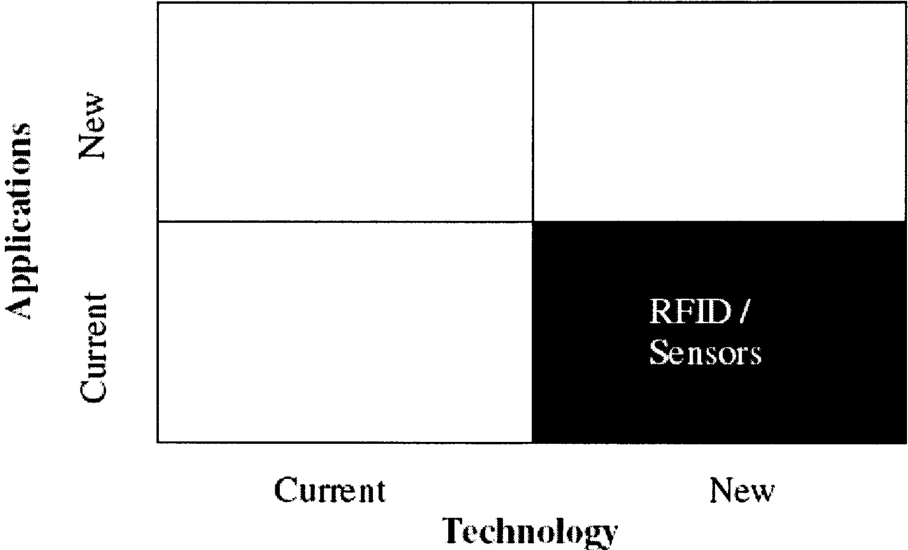


Fig 27: Mc Kinsey diagram for viable MRAM applications

Chapter 3: Intellectual Property Analysis

3.1 Introduction

With MRAM possessing the capability to enter a huge potential market, it is natural to expect many players to compete for the top honors. The following table attempts to summarize the various developmental activities of the firms that appear to be active in the MRAM business at some level. Two leading memory firms, Intel and Micron, appear to have specifically rejected MRAM as a solution and are working on other nanomemory solutions.

3.2 Dominant Firms and related activity

Firm	Involvement with MRAM	Alliances and Partners	Timeframe	Comment
Cypress	Sampling or near sampling. Sees MRAM as a replacement for low power SRAMs	Using NVE IP	Says that it expects $2 million in sales in 2005-2006	Product apparently needs improvement in terms of footprint and power consumption. Major supplier of SRAM
Freescale	Sampling and targeting embedded applications for MRAM. Holds 70 MRAM-related patents	Spin-off from Motorola. May or may not be using some NVE IP in its products. Has licensed technology to Honeywell for defense applications	Available now in limited quantities	Closest to commercialization of all firms. Also working in nanoelectronics alliance with Philips, STMicro and Taiwan Semiconductor
Hewlett-Packard	On-going research. Says MRAM may be used in 3G mobile phones	None known	Originally said it would be making announcements in the 2003 timeframe, but not much said since	Would license IP or create spinoffs, rather than manufacture itself
Honeywell	One of the originators of MRAM technology. Selling products into rad hard military market	Licenses technology from Motorola	MRAM close to or at production stage	Specializes in military applications only. This is unlikely to change
IBM – Infineon	IBM views MRAM as a replacement for embedded DRAM. Flash also seems to be targeted	Work has been transferred to jointly owned French firm, Altis. IBM is backing a Stanford University spintronics center	16 MB prototype in 2005.	Infineon is major supplier of DRAM.
Micromem	Developing MRAM specifically for RFID applications	University of Toronto OCE (a group sponsored by the Ontario government)	Not known.	Currently just conducting R&D

NEC/Toshiba	Alliance targeting EEPROM, SRAM, embedded Flash and DRAM. Will target embedded Flash later		2007 will be "ramp-up" period for MRAM	Both firms are significant players in the SRAM and Flash space. Initial applications expected to be battery backup SRAM for data log storage, with later applications including cell phones
NVE	Hold MRAM patents licensed to Motorola, Cypress and Agilent. Plans to sell MRAM based on Cypress design	Existing licensees. Working with DARPA and DTRA on MRAM R&D	Already engaged in licensing activity. May ship MRAMs in 2006	Value of patents has been questioned. Looking for more licensees
Philips	Involved in nanoelectronics alliance with Freescale, STMicroelectronics and Taiwan Semiconductor that includes MRAM	Motorola, STMicroelectronics	Not known	Philips has shown some research interest in MRAM in publications, but its future intentions have not been specified
Renesas	Has unveiled a prototype 1 Mb RAM	Mitsubishi, Hitachi	Not known	Major manufacturer of Flash and SRAM
Samsung	Actively commercializing MRAM. Has a l6kb test chip		In the pipeline	Largest memory chip firm in the world
Sony	Has demonstrated a test MRAM and believed to be working on a 4 Mb chip		Not known	Major supplier of SRAM
Spintron	Developing a version of MRAM called e-MRAM	Spin-off from the French National Research Center. Backed by Impulse (French incubator) and Primaveris (VC). Also working with STMicro	Prototypes in 2005. Products in 2007-2009	IP/fabless company. "eMRAM" is MRAM embedded in CMOS
Taiwan Semiconductor	Developing MRAM	Main partner is ERSO, a government research body	Not known	ERSO doing basic research. Also involved with STMicro, Philips and Freescale in nanoelectronics alliance

3.3 A few key patents

Obviously, with so many firms in the game, there are bound to be numerous IP conflicts. Nevertheless, a search on the USPTO revealed that the major patent holders both in terms of numbers as well as key technology disclosures happen to be IBM and Motorola, Inc. Both of these firms own close to 170 patents. Most importantly, most of their patents

have led to path breaking improvements in the MRAM research arena and were instrumental in keeping the impetus on MRAM alive. Listed below are a few key patents that might be considered important.

US Patent No	Assignee	Date filed	Inventors	Comments
5,640,343	IBM	March 18, 1996	Gallagher et al.	Disclosure of a novel magnetic memory architecture
5,650,958	IBM	March 18, 1996	Gallagher et al.	MTJs with controlled magnetic response
5,841,692	IBM	July 16, 1997	Gallagher et al.	MTJ with antiferromagnetically coupled pinned layer
5,969,978	The United States of America as represented by the Secretary of the Navy	September 30, 1998	Prinz et al.	Read/write memory architecture employing closed ring elements
6,104,633	IBM	February 10, 1998	Abraham et al.	Intentional asymmetry imposed during fabrication and/or access of MTJ
6,531,723	Motorola, Inc.	October 16, 2001	Savtchenko et al.	Magnetoresistance random access memory for improved scalability
6,545,906	Motorola, Inc.	October 16, 2001	Savtchenko et al.	Method of writing to scalable magnetoresistance random access memory element
6,967,366	Freescale Semiconductor, Inc.	August 25, 2003	Janesky et al.	Magnetoresistive random access memory with reduced switching field variation
6,229,729	Micromem Technologies, Inc.	February 29, 2000	Lienau et al.	Magneto resistor sensor with diode short for a non-volatile random access ferromagnetic memory
5,695,864	IBM	September 28, 1995	Slonczewski et al.	Electronic device using magnetic spin components
6,072,382	Nonvolatile Electronics, Inc.	January 6, 1999	Daughton et al.	Spin dependent tunneling sensor
6,963,098	Nonvolatile Electronics, Inc.	June 23, 2004	Daughton et al.	Thermally operated switch control memory cell

Chapter 4: Business Model

4.1 Keys to Success in the MRAM Market

The most commercially viable alternative to volatile memory, as of today is apparently the MRAM-based technology and is certainly the way to go for future RAM technology. With that said, there are disadvantages in the current MRAM designs that need to be reconciled before the technology can advance from laboratories into industry. There is considerable variability between MRAM devices fabricated on a chip, which limits the manufacture of chips on a large scale. This means that the yield is lower and hence the product is more expensive because there are fewer chips being manufactured. When MRAM is first released, it will be too expensive for most people to buy MRAM-based computer systems. Most of the consumers who purchase the systems will be those that require high power computing and extremely fast computation times, such as research companies and universities.

The majority of the consumers are already happy with the present pace of computing technology and most of them are even ignorant of Moore's Law and its implications. This fact is evident from the poll that was conducted by Pricegrabber.com where 2,379 online shoppers were asked about their choice of notebooks. Quite unsurprisingly, only a fraction of them opted for the high-end notebooks (around $2000) in today's market. It is reasonable to assume that the initial MRAM based notebooks will probably be a few thousand dollars more than even these high-end notebooks and hence it will be unrealistic to believe that convincing an average consumer into an MRAM-based system is an easy task.

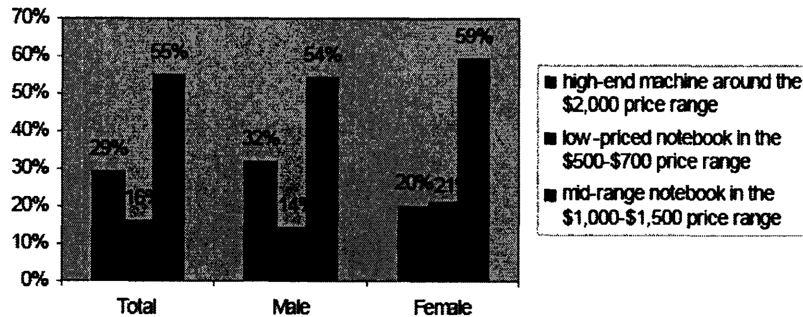


Fig 28: Consumer behavior indicates most of them are already satisfied with what they have [F-21].

Hence the strategy for initial market entry is extremely crucial and a well-planned methodology of introduction can help establish a strong hold on the entire memory segment. There are a variety of potential applications where MRAM could be introduced but according to my personal opinion, it will be the best to have MRAM in an application that eliminates the use of 2 or 3 different memory types simultaneously. Further it will be in the best interests if that application requires non-volatility, does not demand extremely high density and requires that very low amount of power be consumed. One such application that comes to mind is the portable electronics segment that comprises of systems like cell phones, PDAs and mp3 players. The smaller systems can be manufactured at a lower cost on the virtue of their lower density and complexity. Once MRAM based smaller systems get widely accepted, the production cost will automatically come down due to the economies of scale. Subsequently, larger systems like laptops, wireless and automotive systems can be made to incorporate MRAM based components. Finally, the manufacturers can then move onto the largest systems like desktops that incorporate components like SRAM and DRAM and then in time, MRAM would become more cost effective and phase out volatile memory in certain applications. This happens to be the more viable route for introduction of the MRAM based products in today's market atmosphere.

4.2 Possible strategies

Having said so much let us first examine the various strategies pursued by companies in the MRAM space as of today:

Strategy	Advantages	Disadvantages	Firms pursuing this strategy
Early entry with MRAM product	Can establish customer base, distribution channels and "brand name" before others	Can be stuck with obsolete technology	Cypress, Freescale, IBM, Infineon
Later entry with MRAM product	Products embody the latest technology and may be more competitive with conventional RAM than current products	Firms may "miss the boat"	NEC, Toshiba, Renesas, Samsung, Sony, TSMC
Licensing IP	Low costs of entry	Protecting IP can be expensive and hard.	HP, NVE
Fabless – specialist product design	Lowers the threat of competition from "mass market" players. Enables firm to focus on pre-existing strengths in certain markets. Helps firm to develop specialist marketing strengths and products to dominate a niche	Excludes large segments of the MRAM market for possible penetration. Makes success depending on growth in only one applications segment	Honeywell (Defense), Micromem (RFID)
Supplier of non-MRAM technology to MRAM suppliers	Provides the ability to catch the MRAM wave	Not really a "player"	Philips

As we can see, there are three broad strategies that one can adopt as a player in the MRAM market segment. These are:

1. Fab model
2. Fabless design model
3. IP model

In order to get a realistic reasoning for adopting a particular business model, it is necessary to examine all the three models closely.

4.2.1 Fab model

In this type of business model, full scale manufacture of MRAM chips and products are carried out. This involves either building MRAM chips from scratch or using basic MRAM chips to build more complex systems. Both of these are capital intensive and involve a lot of time to setup too. Thus, the rates of return happen to be the lowest in this model due to the fact that MRAM is still not an established memory and will take a while before gaining a foothold in the memory market.

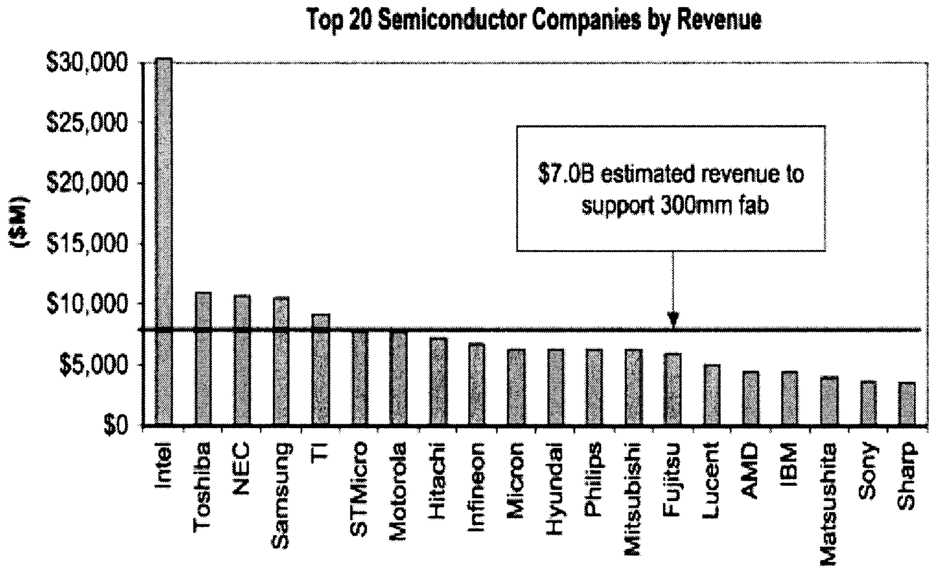


Fig 29: Costs incurred in setting up a full scale fab. Ref: F-22

The plot above gives the revenue distribution among the heavyweights in the semiconductor industry. As can be seen, the fab model is viable only if the estimated revenue falls in the vicinity of $7 billion. Add to that, the widening gap between the fab cost (input) and revenue generated (output) (Fig. 30) only forces one to conclude that a full scale fab model is certainly not a practical option.

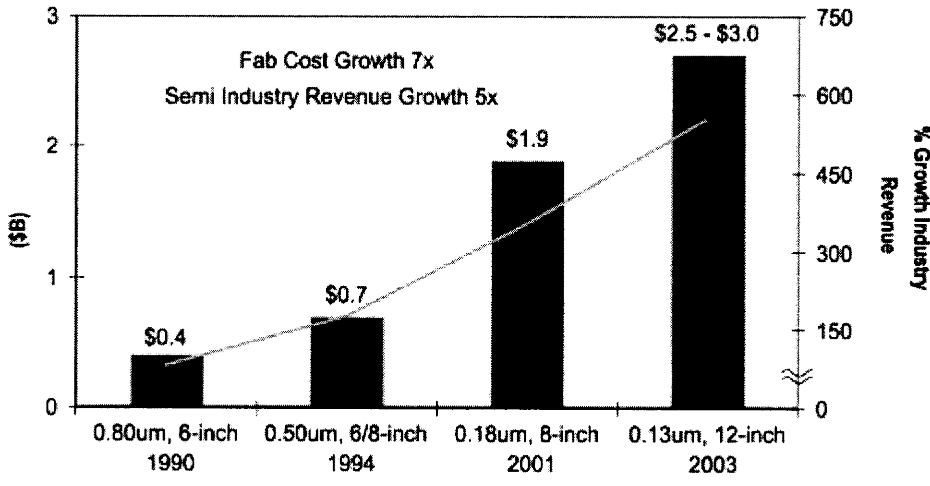


Fig 30: Relative cost and returns in the semiconductor industry. Ref: F-22

4.2.2 Fabless model

Let us now take a close look at the fabless option. A fabless semiconductor company specializes in the design and sale of hardware devices implemented on semiconductor chips. It achieves an advantage by outsourcing the fabrication of the devices to a specialized semiconductor manufacturer – a semiconductor foundry or fab. A fabless company may concentrate its research and development resources on the end market without being required to invest resources in staying current in semiconductor technology.

However, despite the above merits, one should recognize that memory market – unlike software and other technology sectors – is a 'winner takes all' marketplace. A comparison between Cambridge Silicon Radio (CSR), one of 2004's European success stories, and SiliconWave, makes this point emphatically. Both companies were players in the Bluetooth chip market. CSR has been a headline success story (and is now worth around US$785m). SiliconWave, by contrast, was sold for just US$10.8m. There is little middle ground in this market – companies either soar, or fold.

The field of MRAM is no less risky. This can be attributed to the developments that come about every other day adding refinements to the writing mechanism, architecture and numerous other factors that determine the performance of MRAM. Hence, designing a product based on today's best MRAM technology may be obsolete by the end of next week. There are reasons to believe that the previous statement may not be viewed as an exaggeration. As a matter of fact, until Dec 2005, the most talked about (most researched and the one with maximum followers) writing mechanism was the one pioneered by Motorola that was called toggled MRAM using Savtchenko writing. However, in the next 3 months that followed, much of the focus has shifted to a radically different writing mechanism proposed by Sony – the spin torque transfer mode – as this has brought down the required current density drastically and has numerous other advantages like better scalability etc. Thus, it is easily seen that design of a system using Motorola's IP would have resulted in losses as Sony's MRAM is clearly the better of the two.

Therefore, the moral of the story is that there are huge swings in basic technology of

programming of MRAM due to the sheer volume of research that is being conducted throughout the world in this area.

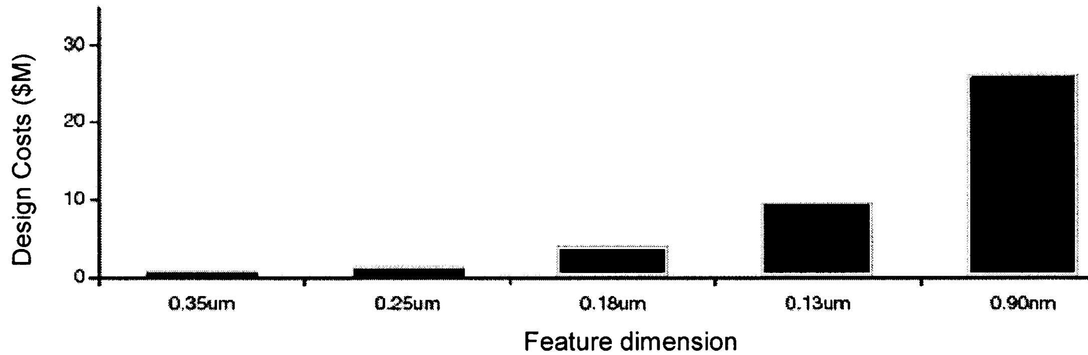


Fig 31: Design costs increase exponentially with scaling down. [Source: Ref. F-23]

Further, as the design scales reach the nm scale, the cost increases almost exponentially as shown in the Figs. 31 and 32. A rough estimate of the amount of capital needed to start a fabless firm can be found below.

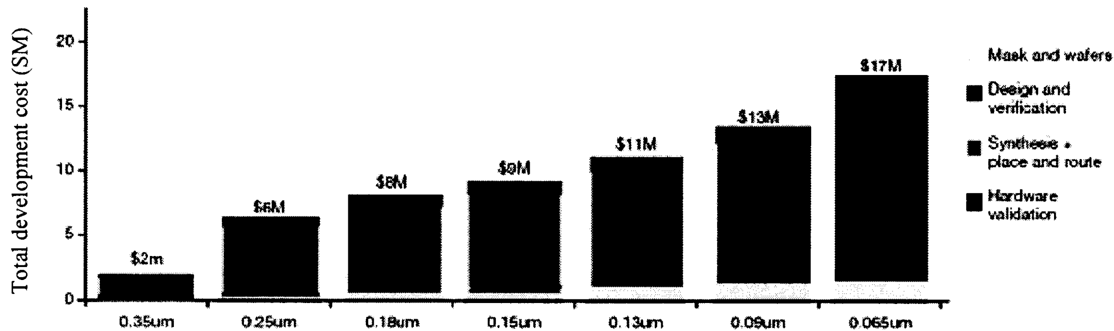


Fig 32: Total developmental costs incurred by a typical fabless firm (2005). [Source: Ref. F-23]

Total Costs involved (**$55-60 million**)

1. Minimum capital required to start a fabless semiconductor - $25 million
2. 2-3 years ($15 million) to get to first products and revenues
3. $10 million in direct employee costs
4. $2 million in tools, facilities, etc.
5. $3 million in manufacturing, test, etc.

If we expect to make $40 million in revenue, it essentially translates to $4 million in earnings (after 15% operating margin & 35% tax rate). Thus, it typically takes ~10-12 years to break-even if we are successful.

Apart from this huge cost incurred, there is also the risk of competition from other companies that work in either the same space or a different nanotechnology. It is highly imperative that we be the first to reach the market with the product because, in today's market, there is no market for a second-to-market product. This is illustrated graphically in the following figure that juxtaposes the market behavior in mid-1990s with that of todays.

As a rough estimate, a 6-month delay in the product release time would result in a 31% revenue loss in mid-90's. However, a 3-month delay in today's market will push back the company's account by $500 million. This assumes extreme importance in MRAM field as the only viable entry routes (at least initially) are embedded MRAMs and there is a high probability that these might already be under production at one of the Motorola (which is the world leader in embedded memories) fab centers.

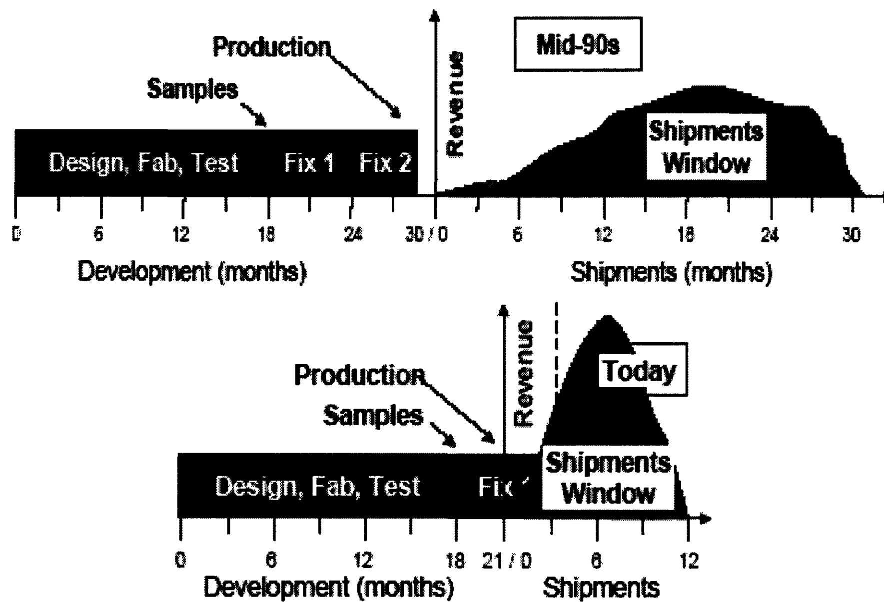


Fig 33: Market and product entry strategies in 90's versus today (From Ref. [F-24]).

In the light of the above said "tantalizing facts", fabless option does not look very attractive either. So all we are left with is just the IP model. However, it remains to be seen if it is worthwhile entering this segment.

4.2.3 IP Model

A search on the USPTO website (as of 23rd July, 2006) reveals that almost 55% of the

patents that were issued on MTJs were from 2003-05. Again, 53% of the patents on MRAM were issued in the last two years. These two facts stand testimony to the amount of research that has been going on in the MRAM field.

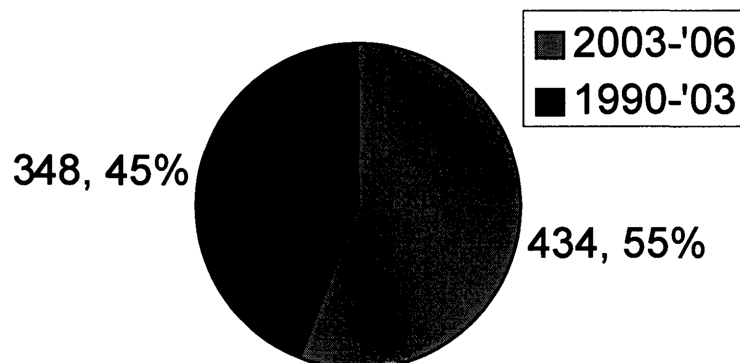


Fig 34: Of a total of 782 patents on MTJs, 434 were issued in 2003-05. Data from [F-25]

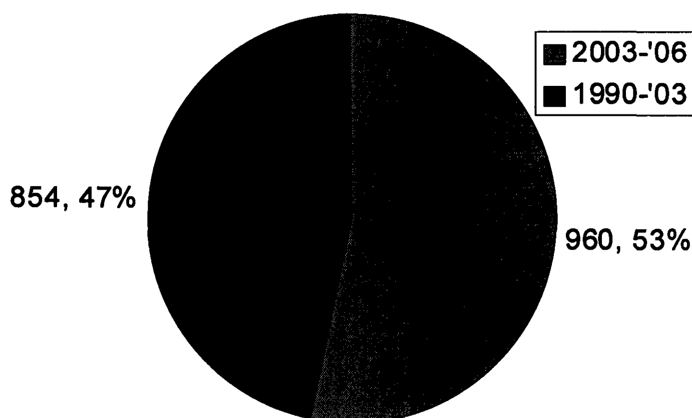


Fig 35: A whopping 960 patents out of 1814 patents on MRAMs were issued in 2003-05 [F-25].

A look at the above pie charts reveals the bitter fact that the IP space is extremely crowded. However, the good news is that MRAM still has problems that need to be resolved. These include:

1. Optimization of write currents, density
2. Scalable architecture
3. An inexpensive process of production

Hence, it is possible for even a small player to create a considerable impact if appropriate results can be achieved. For example, discovery of a new dielectric material that increases the differential resistance or providing a new architecture that results in a

reduction of current can enable in more scaling which means more devices can be fabricated on a single wafer. If we license this patent to a major MRAM player like Freescale or Cypress, this directly translates to a reduction of the process cost. This can be schematically illustrated by the blue curve in the figure shown below. The new memory (MRAM) is currently at a much higher cost than say, flash memory. However, as time proceeds, flash will age and exit the scene (due to scaling problems etc.) and the market will become conducive to MRAM. But this will take some time. If we are able to help our licensee enter the market earlier than their competitor by a reduction in the introduction time – which happens due to the reduction of process cost – (as shown using pink arrow), a sizable portion of the market can be captured. This is exactly the corollary of the fact mentioned in the fabless model section, which implies that an earlier entry by 3 months would result in additional revenue of $500 million.

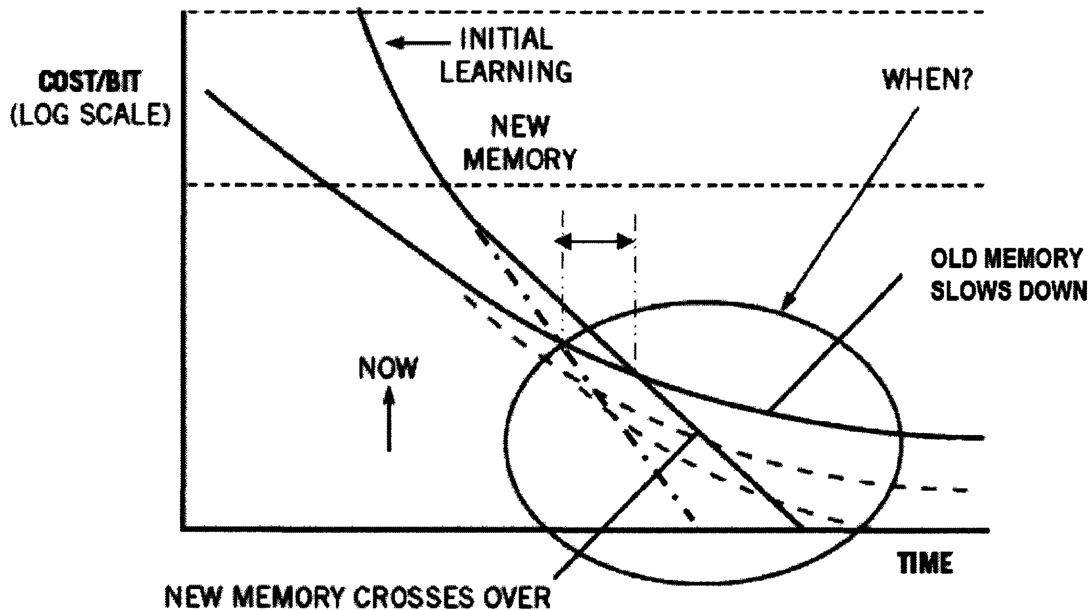


Fig 36: Product entry mechanism illustrated as a function of time and cost. (Adapted from [F-26])

Apart from the above said features, another advantage of the IP model is that it involves minimum risk because IP business models are horizontally focused and hence the IP can be applied to a wide range of markets. An example for this would be entering the GMR based sensor research space using a revolutionary idea, which came about while working on MRAMs. In addition, with such a flurry of activity on MRAM, obtaining VC funding should be relatively easy as MRAM is almost near its market-introduction stage.

As for drawbacks concerning this model, potential lawsuits resulting from the IP property clash may result in delays, which might reduce the "useful" lifetime of the patent. Hence, filing patents aggressively and intelligently so as to exclude the competition from circumventing it in every possible way is important.

Hence, given the present scenario, the IP model seems to be the most practical business model.

4.2.3.1 Revenue generation:

Let us assume that the IP model based company comes out with a great patent that proves very useful to the fab companies. Hence, the IP company can expect to get a royalty of 1-1.5%. In order to cover a spectrum of applications (thereby covering a huge spectrum) it is wise to choose licensees with different market focus. This also helps to make our research area broader. For MRAM based technologies, it is a reasonable choice to choose Freescale, Honeywell and Agilent as the licensees as they serve different non-overlapping sections of the market. Freescale addresses the embedded memory segment, Honeywell caters to the military applications whereas Agilent commands a good market share in medical sensors.

For purposes of calculation, let us peg the total market share that is addressed using the concerned patents at: 10%

From the graph above:

1. Expected Market value (2011): $12.9 Billion
2. Market share: 10%
3. Royalty ~ 1 – 1.5%

Thus, Revenue generated: $12.9 B * 0.1 * 0.015 = $19.4 million over an year which sounds very reasonable for an IP based company.

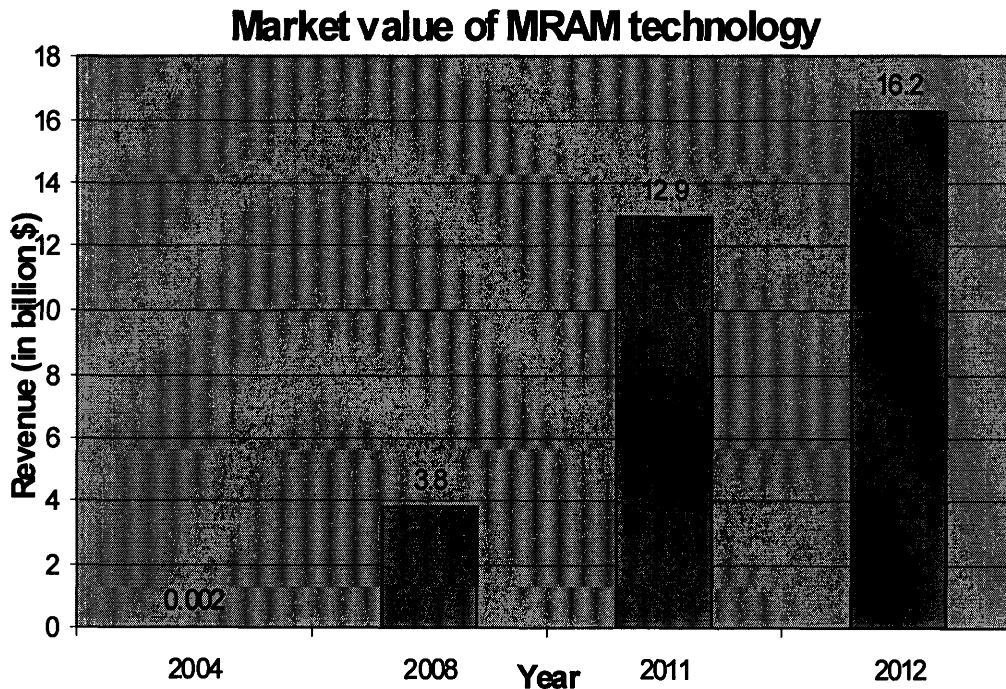


Fig 37: Market estimates for MRAM technology based applications [F-17]

4.2.3.2 Funding resources:

Throughout the past decade, many companies as well as research centers have been receiving constant funding from government agencies as well as other sources like Venture Capitalist funding. The very fact that huge amount of money is being pumped into this technology to this day not only reinstates how much this technology is lucrative but also that it is relatively easy to get funding for establishing a new startup in this field. Listed here are a few funding agencies and the organizations that received the funds:

- Honeywell, IBM, and Motorola received **$50 million** from Defense Advanced Research Projects Agency in 1994 for initial studies on MRAM technology.
- NVE Corporation – A start-up based on IP model received funds from Cypress (a core memory major) during the initial stage. However, after that, it has been receiving funds chiefly from government agencies only.
    - **$6.228 million** – Cypress (Apr 2002)
    - $750,000 – DARPA (Feb 2003)
    - $500,000 – Defense Threat Reduction Agency (DTRA) (Nov 2003)
    - $400,000 – DARPA – For the development of ultra sensitive SDT sensors

(Feb 2005)

- $600,000 – DOD – For development of deep sub-micron Vertical Transport Magnetoresistive Random Access Memory (VMRAM) (Oct 2005)
- **$2 million** – Defense Sciences Office – Bio-Magnetic Interfacing Concepts (BioMagnetICs) program ('02-Dec 05)

- Micromem – Another fabless start-up firm based in Canada raised $1.5 million through VC. It is pursuing designs, which might enable MRAM to enter the RFID market with a competitive edge.

- ITRI and TSMC – The two Taiwan based firms will receive **$300 million** over the next 6 years from the Taiwanese government for exploring MRAM based memory technologies.

- Trikon Technologies – A UK based firm got a grant of **$5.8 million** for developing a Broad Ion Beam Deposition system technology for 300-mm MRAM manufacturing facility (Oct 2005).

Apart from these companies, almost all major universities around the world have at least a few researchers dedicated to the world of spintronics. In most of these universities efforts are on in a direction that aims to make the MRAM technology more feasible in the near future. Examples of such research groups and their area of work is summarized below:

Cambridge-MIT alliance:

The team, led by Prof. Tony Bland at Cambridge University, Prof. Caroline Ross and Dr. Jagadeesh Moodeera at MIT, aims shed more light on the fundamental magnetic properties of nanomagnetic structures. In particular, they have successfully studied the effects of geometric and structural properties on the magnetic switching behavior and state stability. According to their observation, their patented ring shaped magnetic element has a high degree of reliability, ultrafast switching characteristics along with the ability to store multiple bits. Due to these attributes, such nanoring elements could help in the evolution of more sophisticated magnetic data storage devices like the MRAM.

Stanford Center for Magnetic Nanotechnology:

This research center is a part of Stanford University and is headed by Dr. Shan Wang. Some of the ongoing research topics relevant to MRAM technology include:

- New materials and mechanisms for magnetic random access memory (MRAM).
- Spin electronics including using photoelectron emission microscopy for direct imaging of spin injection and investigation of spin configuration in antiferromagnets.
- Spin filters and current-driven spin switching.
- New materials to extend the superparamagnetic limit, such as new high saturation soft magnetic materials for inductive write heads and perpendicular recording disks.

Yet another milestone that was recently realized at Stanford University is the research initiative between IBM and the former called as ***SpinApps***. This partnership will concentrate broadly on the field of spintronics and has eminent scientists like Dr. Stuart Parkin, Dr. Shoucheng Zhang and Dr. James S. Harris leading the group. The program will also get additional funding from the Defense Advanced Research Projects Agency, the U.S. Department of Energy and the National Science Foundation.

Carnegie Mellon University:

This list will not be complete without a mention of Carnegie Mellon University, Pittsburgh. At CMU, Dr. Jian-Gang Zhu, who is also the director of Data Storage Systems Center, leads a group that is currently studying on the fabrication of ring shaped vertical MRAM and micromagnetic modeling of low power vertical MRAM Design.

Spin@RT:

This is a very recent British spintronics consortium that is led by Prof. Brian Hickey at Leeds and includes Cambridge, Imperial, Durham, Glasgow, Exeter and City universities and the Rutherford Appleton Laboratory. It has been awarded £2.3M to look at new and existing ways of applying spintronics, develop new materials and push the limits of our

current understanding of magnetism. The group - Spin@RT - is funded by the Engineering and Physical Sciences Research Council (EPSRC) and is supported by some of the world's biggest hard-drive and electronics manufacturers.

Leeds specializes in making magnetic materials and thanks to £240,000 from the Wolfson Foundation (and £210,000 from the University) they are now using a 'sputter' machine which allows them to fabricate novel magnetic materials in layers with thickness control equivalent to adding or removing a single atom.

Another noteworthy project at the University of Glasgow that has been awarded £425,309 is on "Room Temperature Spintronics" that will study the coherent transport mechanisms which will provide more details on the spin–current torque as well. It has been predicted that coherent transport will improve the magnetoresistance (MR) by more than an order of magnitude. The impact of such an improvement in MR alone on spintronic devices such as MRAM will be immense.

Tohoku University Research Institute of Electrical Communication, Japan:

Prof. Hideo Ohno heads this group that deals with "Spin-Related Phenomena in Ferromagnetic Semiconductor Heterostructures". One of their recent contributions to the MRAM field was the discovery of a Giant TMR (~400%) in an annealed CoFeB/MgO/CoFeB magnetic tunnel junction. The giant TMR effect and spin momentum transfer in the MgO-based MTJs are the key for next-generation spintronic devices such as Gbit-scale MRAM and read heads for ultra-high density hard disk drives.

National University of Singapore, Singapore:

In Singapore, research on MRAMs is conducted chiefly by Associate Prof. Adekunle Adeyeye, whose research interests are mainly in the areas of Spin-electronics & Magneto-electronics Devices, Nanofabrication & Nanomagnetism and Data Storage Technology. He is at present working on a project titled "Half metallic based devices" that aims to create an MRAM device with a better TMR.

Apart from these universities and research institutes, almost all major semiconductor

firms have their own research centers where the MRAM programs continue to show positive results. To quote [68] Dr. Saied Tehrani, director of MRAM technology, Freescale Semiconductors, Inc., "Some companies came in with huge expectations that didn't materialize fast enough for them. I believe MRAM technology still has a lot of promise, and we are seeing that at Freescale. It still is a challenge getting the cost structure and the volumes to the point where it can have a huge impact on giant markets. That is the challenge with any new memory technology."

Hiroaki Yoda, a manager at Toshiba Corp.'s advanced-memory technology department, shares a similar sentiment. Yoda feels that MRAM technology is making rapid progress, citing "great advances" with the introduction of magnesium oxide barriers and spin momentum transfer technologies.

As a result, "nanosecond read speeds are possible and the objective of reducing programming current has become a little more realistic. This is completely different from other emerging memory technology development efforts, in which no big innovations have been made". [68]

Chapter 5: Concluding Thoughts

MRAM technology at the moment is facing a situation that personal computer systems faced in the 1980s just after their introduction. It will be quite a while before MRAM based systems become affordable to the common man and it will probably take even longer to achieve the predicted theoretical efficiencies in all its attributes. However, many people in the industry are quite optimistic about the impact MRAM can create after its inception in the memory segment. But, the reality of the situation is that, although the year 2006 will bring us more functional MRAM chips, they will be simple, and of extremely low density in comparison to that of the DRAM chips and will definitely be more expensive than flash memory. Further, replacing a much evolved memory technology like Flash is very difficult particularly, when it has not reached its scaling limits. Thus, further research is necessary to improve the properties of MRAM so that its capabilities can be fully exploited. Additionally, a novel process that cuts down the fabrication costs can help MRAM to capture a lion's share in the memory market.

These developments are crucial if MRAM is to have a big impact on the electronics industry. In my opinion, the time when MRAM will peak is still a good 3-4 years away. However, due to its superior attributes over both the then incumbent and the emerging memory technologies, it is poised to dominate the memory market thereafter.

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