

**Through-Substrate Interconnects for 3-D  
Integration and RF Systems**

by

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B.S.E., University of Michigan (1996)  
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Submitted to the Department of Electrical Engineering and Computer Science  
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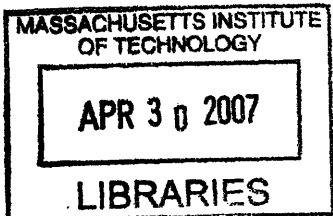
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## Abstract

Interconnects on silicon chips are fabricated on the top surface with an ever-increasing number of metal layers necessary to just meet performance needs. While devices have scaled according to Moore's law, interconnects have lagged. As metal line widths shrink and line lengths increase, parasitic resistance, capacitance, and inductance degrade circuit performance by increasing delays, loading, and power consumption. Separately, silicon has been supplanting GaAs in low-end, consumer RF applications. Improving the high-frequency performance of silicon by reducing ground inductance will project silicon technology into high-end RF and mm-wave applications. Furthermore, silicon-based systems allow for integration with digital blocks for system-on-chip (SoC). However, this introduces digital noise into the substrate, which interferes with the operation of RF/analog circuits.

To address these challenges, we have developed a low-impedance, high-aspect ratio, through-substrate interconnect technology in silicon. Through-substrate vias exploit the third dimension by connecting the front to the backside of a chip so that power, ground, and global signals can be routed on the backside. Substrate vias can also be used to connect chip stacks in system-in-package designs. They also provide a low-inductance ground for RFICs and enable a novel way to reduce substrate noise for SoC.

The fabrication process features backside patterning for routing of different signals on the back of the chip. Fabricated through-substrate vias were fully characterized using  $S$  parameters measured up to 50 GHz. The via resistance, inductance, and sidewall capacitance were extracted from these measurements. We report record-low inductance for high-aspect ratio vias, via resistance less than  $1 \Omega$ , and sidewall capacitance that approaches theory.

We have also examined the application of substrate vias arranged as a Faraday cage to reduce substrate noise for SoC. The Faraday cage is exceptional in suppressing substrate crosstalk, especially at high frequencies: 32 dB better than the reference at 10 GHz, and 26 dB at 50 GHz, at a distance of 100  $\mu\text{m}$ . To better understand its performance, we developed a lumped-element, equivalent circuit model. Simulations show that the circuit model accurately represents the noise isolation characteristics of the Faraday cage. Finally, Faraday cage design guidelines for optimum noise isolation are outlined.

Thesis Supervisor: Jesús A. del Alamo  
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# Chapter 1

## Introduction

### 1.1 Motivation

The invention of the integrated circuit (IC) in 1959 by Jack Kilby and Robert Noyce brought together discrete transistors, resistors, and capacitors onto one chip, and more importantly ushered in the digital age of computing. Before the IC, as circuits using discrete components became more complex, the wire connections between them multiplied and grew to become the obstacle to better performance and reliability and to lower power consumption and cost. The integration of once separate components onto a monolithic piece of semiconductor significantly reduced circuit size and eliminated the need for parasitic, off-chip wire connections by using on-chip interconnects.

Integration and scaling have been the fundamental goals of the semiconductor industry to reduce cost and boost performance. As devices have scaled according to Moore's law, interconnects have lagged. While circuit performance improves as devices scale, interconnect scaling results in longer latency and higher power consumption. Interconnects have quickly become the bottleneck in circuit performance, and managing the need for ever-higher transmission speeds with further scaling is the primary concern for interconnects. Currently, interconnects are laid out on the surface of the chip in an increasing number of metal levels (11 layers at present [9]) and just barely meet performance needs. In addition, continuing integration of circuit functionality onto one chip has been stimulated by the wireless industry for better

portability and lower power consumption. This has increased the complexity of not only circuit design but also the demands on interconnects.

One way to meet these challenges is to explore the third dimension of the chip by employing through-substrate vias. Substrate vias provide a way to connect the frontside of the chip to the backside so that the backside can be utilized for power, ground, and global wiring. A further exploration of 3-D is to stack chips in the same package. Through-substrate vias can provide the interconnect between stacked chips for 3-D integration that also eliminates the need for parasitic bond wires.

The generic nature of through-substrate interconnects lends itself to a wide range of applications. The next sections will give background on several applications and describe the motivation to use through-substrate vias.

### 1.1.1 RF Systems

In millimeter-wave (mm-wave) and radio-frequency (RF) applications, high-frequency performance of silicon technology has been approaching that of III-V semiconductor devices. Fig. 1-1 shows the RF application space over power and frequency, and Fig. 1-2 shows the accompanying device technology for those applications [1]. Currently, silicon-based technologies dominate the low-frequency application space, and III-Vs are used for high-frequency applications. Silicon RF devices have targeted the consumer market with carrier frequencies below 10 GHz [10], and have been replacing GaAs in these low-end, high-volume RF applications because of its lower manufacturing costs and its integration capabilities [10–12]. Furthermore, silicon technology with the help of SiGe has surpassed GaAs FETs, and already holds promise for mm-wave applications as high as 77 GHz [10, 11]. At millimeter-wave frequencies (30–300 GHz), applications include automotive radar for collision avoidance operating at 76–77 GHz [13, 14] and IEEE standard 802.16 wirelessMAN<sup>TM</sup> operating from 10–66 GHz [15].

As silicon RFICs strive for high-performance, high-frequency operation, it becomes increasingly important to reduce all extrinsic parasitics. Of particular concern are the source ground impedance of MOSFETs and the emitter ground impedance of

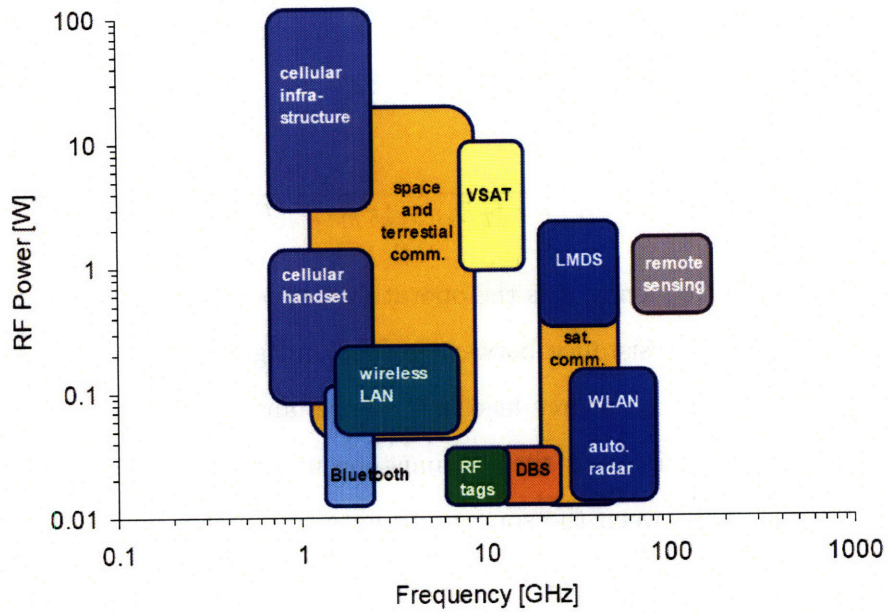


Figure 1-1: RF applications cover a broad range of frequencies and power [1].

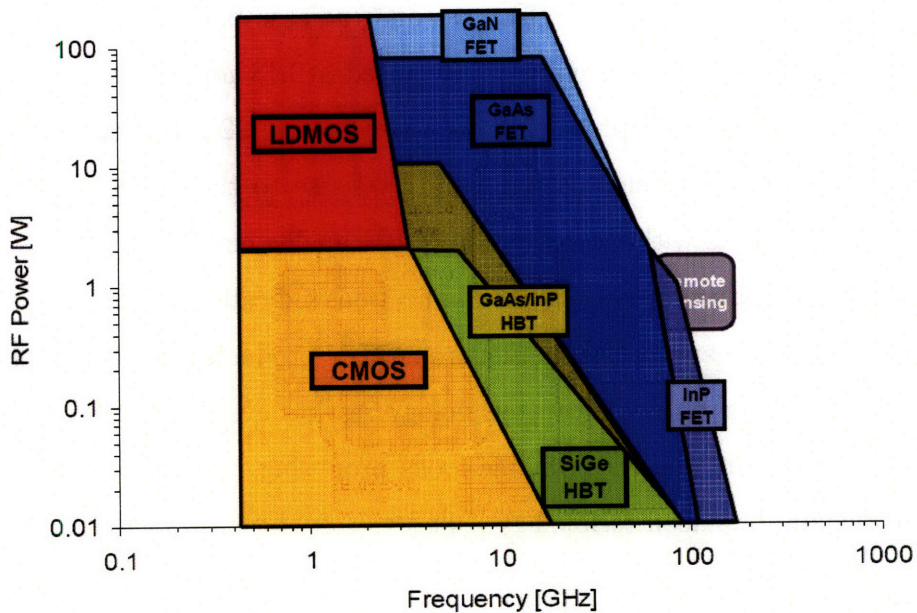


Figure 1-2: Technology landscape in the frequency-power space. Silicon-based technologies occupy the low-frequency regions, while compound semiconductors are used for higher frequencies and power levels [1].

BJTs, which greatly affect the gain, efficiency, and noise characteristics of RF amplifiers [16–19]. The effect of source inductance on gain can be seen from the equation for maximum available gain (*MAG*) of a FET [19]:

$$MAG = \left(\frac{f_T}{f}\right)^2 \frac{1}{4g_d(R_i + R_s + \pi f_T L_s) + 4\pi f_T C_{dg}(R_i + R_s + 2\pi f_T L_s)} \quad (1.1)$$

where  $f_T$  is the cutoff frequency,  $f$  is the operating frequency,  $g_d$  is the drain conductance,  $R_i$  is the channel resistance between source and gate,  $R_s$  is the source series resistance,  $L_s$  is the common source lead inductance, and  $C_{dg}$  is the Miller feedback capacitance. Equation 1.1 shows that  $L_s$  must be minimized along with the input resistance,  $R_i$ , and  $R_s$  between the source and gate to increase gain [19]. Substrate vias are widely used in GaAs and InP microwave and mm-wave ICs to provide low-impedance ground connections [16–18, 20]. Therefore, substrate vias in silicon would be a natural extension from III-Vs for silicon RFICs.

Integration of digital, analog, and RF systems on one chip, “System-on-Chip” (SoC), or in one package, “System-in-Package” (SiP), is believed to be the ultimate goal for RF systems to reduce system cost and increase performance and packing density [11, 21]. Ericsson have already integrated a 0.18  $\mu\text{m}$  Bluetooth radio (2.4 GHz) with digital baseband processing on a single chip [22]. However, integrating RF/analog and digital systems on one chip gives rise to the problem of substrate crosstalk that interferes with the operation of RF/analog circuits [10, 23].

As the current market for low-end RF applications indicates, silicon technology can quickly overtake and capture the market from III-V products because of its mature commercial development. As silicon technology reaches ever higher frequencies, the future of silicon in the mm-wave regime looks promising. However, several critical challenges remain for silicon technology [10]:

- Low-loss interconnects (especially ground, power, and global signals)
- Substrate crosstalk isolation between systems
- Cost-effective, low-loss packaging

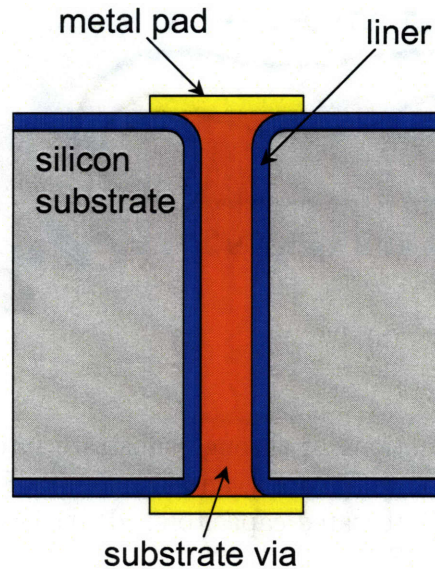


Figure 1-3: Illustration of a cross-section of a through-substrate via.

These issues can be addressed by introducing a through-substrate interconnect technology that minimizes parasitic resistance and inductance. This interconnect is a high-aspect ratio, conductive via with an insulating liner that connects the frontside to the backside of a chip (Figure 1-3). Using this via technology, low-parasitic interconnects for power, ground, and signals can connect directly to devices from the backside through the substrate, reducing bond wires and long metal lines on the surface (Fig. 1-4a). When integrated on a single chip, substrate noise from digital and analog circuits degrade performance of RF systems. A Faraday cage can also be constructed using substrate vias to isolate systems from substrate crosstalk (Fig. 1-4b).

### 1.1.2 3-D Interconnects for Power, Ground, and Signal Distribution in ICs

Interconnects on a silicon chip are traditionally fabricated on the top surface of the substrate. As metal line widths decrease and line lengths increase, parasitic resistance, capacitance, and inductance degrade circuit performance by increasing delays,

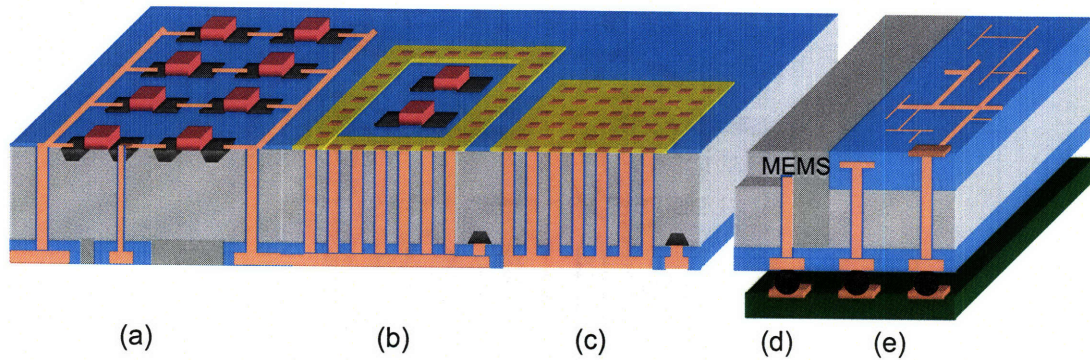


Figure 1-4: Various applications of through-substrate interconnects in silicon: (a) backside interconnect for power, ground, and signals, (b) Faraday cage for substrate noise isolation in SoC, (c) integrated capacitors, (d) backside contact for MEMS, (e) backside package mount for SiP.

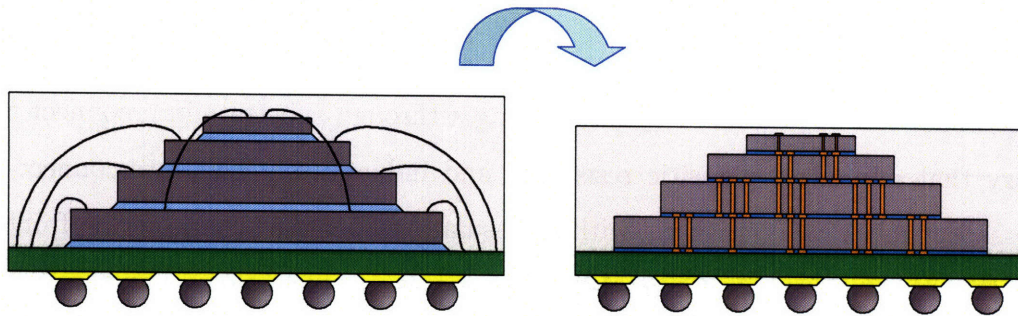


Figure 1-5: Current chip stack technology uses wire bonds to connect chips to each other and to the package. Using through-substrate interconnects in chip stacks would eliminate parasitic bond wires and reduce package size.

loading, and power consumption [24]. A through-substrate interconnect would reduce parasitics by decreasing line length. This would also increase packing density and provide an interconnect for 3-D integration (Fig. 1-4a), specifically for multi-layer silicon die and chip stacks without parasitic wire bonds (Fig. 1-5), and ultimately extend to wafer-level packaging (Fig. 1-4e) [21,24–26]. These examples of SiP can offer the integration of passives, memory, micro-electromechanical systems (MEMS), RF subsystems, and digital blocks, perfect for wireless applications [21].

### 1.1.3 Integrated Capacitors

RF circuits typically require passives (capacitors and inductors), which were traditionally discrete components on the board level. Moving discrete passives on-chip reduces parasitic impedances. Standard on-chip capacitors are metal-insulator-metal (MIM) capacitors using silicon dioxide or silicon nitride with capacitance densities of  $0.1 \mu\text{F}/\text{cm}^2$ . Previously, MIM capacitors using sputtered plasma-enhanced chemical vapor deposited (PECVD) silicon nitride achieved capacitance densities of  $2.7 \mu\text{F}/\text{cm}^2$  [27]. Using high- $\kappa$  dielectrics such as  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$  and  $\text{HfO}_2$  can further increase the capacitance density [9]. However, using the third dimension of the chip can give even higher capacitances per footprint area. Because we use an insulating liner for our through-substrate vias, we can employ them as integrated capacitors.

### 1.1.4 MEMS Backside Interconnect

When designing MEMS, there is often a need to contact the backside of the structure without disturbing the frontside components (Fig. 1-4d). This also would prevent the contact from being exposed to a particularly sensitive or harsh environment of the actual MEMS components, such as in a high-stress or liquid environment [28, 29]. This would also eliminate the need for fragile bond wires [30]. Another important advantage of a backside contact would be to ease packaging constraints and to facilitate wafer-level packaging [28, 31–34]. MEMS packages typically exceed the cost of the device itself and impose severe design constraints [32]. Introducing backside, through-substrate interconnects would reduce packaging size and cost. Additionally, since MEMS are typically constructed using several bonded wafers, through-substrate vias could connect between different layers of a MEMS device. Using substrate vias as an interlevel interconnect has been proposed for a MEMS tunable capacitor [35].

The requirements for a backside contact for MEMS is not as stringent due to the large size of MEMS structures. Via diameters as large as  $200 \mu\text{m}$  have been reported for use in MEMS accelerometers [33]. But via diameters on the order of  $30\text{--}50 \mu\text{m}$  are also common [36, 37]. Furthermore, through-substrate vias of  $100 \Omega$  resistance



Figure 1-6: KOH-etched, gold-plated through-hole contact in silicon, 1-mm wide, 675- $\mu\text{m}$  deep [2].

and 1 pF capacitance were considered satisfactory for MEMS applications such as piezo-resistive cantilever arrays, ultrasound transducer arrays, and proximity sensor arrays [36]. Therefore, the conducting material inside the via did not have to be metallic for those applications. Also, the backside footprint area was not as big a concern. Stepped contact holes with a large footprint of approximately 100  $\mu\text{m}$  on the backside and less than 1  $\mu\text{m}$  on the frontside have been implemented [38]. Because of the loose constraints for MEMS devices, a simple through-substrate interconnect developed for ICs could easily be tailored for MEMS devices.

## 1.2 Overview of Through-Wafer Via Technologies in Silicon

Substrate vias in silicon were initially demonstrated using potassium hydroxide (KOH) (Figure 1-6) [2,39–41]. KOH etching produces a characteristic slanted sidewall ( $54.7^\circ$ ) due its selectivity to etch the  $\langle 100 \rangle$  plane in silicon [42]. Therefore, this approach demanded substantial backside processing that resulted in poor aspect ratio vias with a large footprint at the wafer surface.

To obtain a high-aspect ratio via with near vertical sidewalls, researchers have used an anisotropic, deep reactive-ion etch (DRIE) with an inductively-coupled plasma, initially developed for MEMS fabrication [43]. Using DRIE, aspect ratios as high

as 50 have been reached, but the challenge is to line or fill the vias with metal. Previously, researchers have etched vias of aspect ratios of 2.5 [44], 12 [32], and 17.5 [45]. However, these through-wafer vias had only a thin coating of metal on the inside surface of the via. Completely filling vias with a conducting material has become the objective of recent research for reduced via impedance. A DRIE via used as a metal-insulator-semiconductor (MIS) capacitor with an aspect ratio of 20 was lined with SiO<sub>2</sub> and phosphorus-doped poly-silicon as one electrode of the capacitor, then lined with low-temperature oxide (LTO) for the dielectric, and finally filled with undoped poly-silicon as the second electrode [46]. While this via is completely filled, the resistance of one via was 40  $\Omega$  [46]. Other researchers have used highly-doped polysilicon to fill vias, and have had resistance measurements ranging from 10  $\Omega$  to as high as 350  $\Omega$  [36, 38, 47]. Filling vias with a low-resistivity material has given better results [37, 48–51]. Using copper-filled vias, resistances less than 1  $\Omega$  are possible [37, 50]. Very few papers report measured inductance of through-wafer vias, though [37] has measured very high inductances of 255 pH for copper-filled vias with aspect ratio of 6. Record-low inductance of 42 pH for vias of aspect ratio 4, lined with copper and filled with conductive paste, has been reported by [51].

Besides DRIE, other methods for creating high-aspect ratio, through-via holes with near-vertical sidewalls include laser micro-drilling [52–55] and photo-chemical etching of silicon [52, 56, 57]. With photo-chemical etching, aspect ratios of over 100 can be achieved. However, due to the nature of the etch, only one via size in large pore arrays can be etched. This is ideal for decoupling capacitors [56] but not necessarily as an interconnect. Laser drilling can reach aspect ratios up to 30 [55], and has even become profitable enough to support commercial companies that specialize in drilling vias (XSil Ltd. and ALLVIA, Inc.). However, the surface roughness is greater, and it is less mechanically stable than DRIE vias [58]. Pattern transfer was also slightly better with DRIE [58]. Additionally, laser drilling is a serial process so its throughput is dependent on the number of vias etched [55, 58].

Though there are many variations of fabricating through-substrate vias, we chose to use DRIE to etch our through-substrate vias and to use electroplated copper to fill

them. The DRIE tool is well-characterized at MIT, and I have built and maintained the copper electroplating system at MIT. We also introduce an insulating silicon nitride liner as a barrier to diffusion of copper ions from the via core to the substrate. More importantly, the dielectric liner provides electrical insulation between the silicon substrate and copper via core. Also, by using clever backside processing, power, ground, and signals can be routed through the backside of the same chip.

### 1.3 Thesis Goals and Outline

The goal of this Ph.D. was to further the development and characterization of through-substrate vias that were first introduced in my S.M. thesis. The S.M. thesis was a proof-of-concept study and was the first to develop metal-filled, insulator-lined, through-substrate vias in silicon. With this Ph.D. thesis, we have improved upon the via fabrication process to allow for backside routing of power, ground, and signals on the same chip, unlike the S.M. thesis process which could only support ground vias. The ability to route different signals through the backside of one chip expands the applications for through-substrate vias to RFICs, MEMS, and capacitors, and ultimately to the integration of all these in an SoC or SiP RF system, with digital baseband, RF/analog circuits, and RF MEMS/passives.

This thesis is organized as follows. The first objective of this thesis was to develop an improved through-substrate via process for backside routing of power, ground, and signals. New test structures were designed to fully characterize the through-substrate vias, which required additional processing steps in the fabrication process. The complete fabrication process development will be discussed in Chapter 2.

After fabricating the through-substrate vias, they needed to be fully characterized through high-frequency measurements of inductance, resistance, and sidewall capacitance. The measurement setup and the results will be discussed in Chapter 3.

Once the vias were characterized, an important application for through-substrate vias was examined in Chapter 4. The substrate vias were arranged in a Faraday cage structure to evaluate its performance in suppressing substrate noise. The Faraday

cages were fabricated and measured, and an equivalent circuit model of the Faraday cage was simulated and analyzed.

Finally, the conclusions from this thesis research are summarized in Chapter 5. Also, suggestions for the continuation of this work are recommended.



# Chapter 2

## Fabrication Technology

Fabrication of through-substrate vias required development and thorough characterization of new process steps before integrating into one complete process. Improvements over the S.M. thesis work [8] and changes in the via process to accommodate backside patterning and new test structures include: a deep reactive-ion etch for backside thinning, sidewall smoothing, a conformal silicon nitride liner, efficient copper electroplating, copper chemical-mechanical polishing (CMP), and the introduction of ohmic contacts to the substrate. A cross-section illustration of the new substrate-via design is depicted in Fig. 2-1.

All processing steps were developed and fabricated at the Microsystems Technology Laboratories (MTL) at MIT. Several different types of wafers were used as starting material for this process. Prime 150-mm, p-type and n-type, double-side polished wafers and p-type SOI wafers of medium resistivity were processed for impedance and Faraday cage noise measurements. Low-resistivity, p-type, double-side polished wafers were needed for capacitance and sidewall leakage measurements.

This chapter will introduce the overall process flow in Section 2.1, discuss in detail the development and characterization of the new process steps in Section 2.2, and explain the difficulties when the new steps were integrated into one process in Section 2.3. Finally, in order to keep through-substrate via fabrication a back-end process, modifications to the process are suggested in Section 2.4.

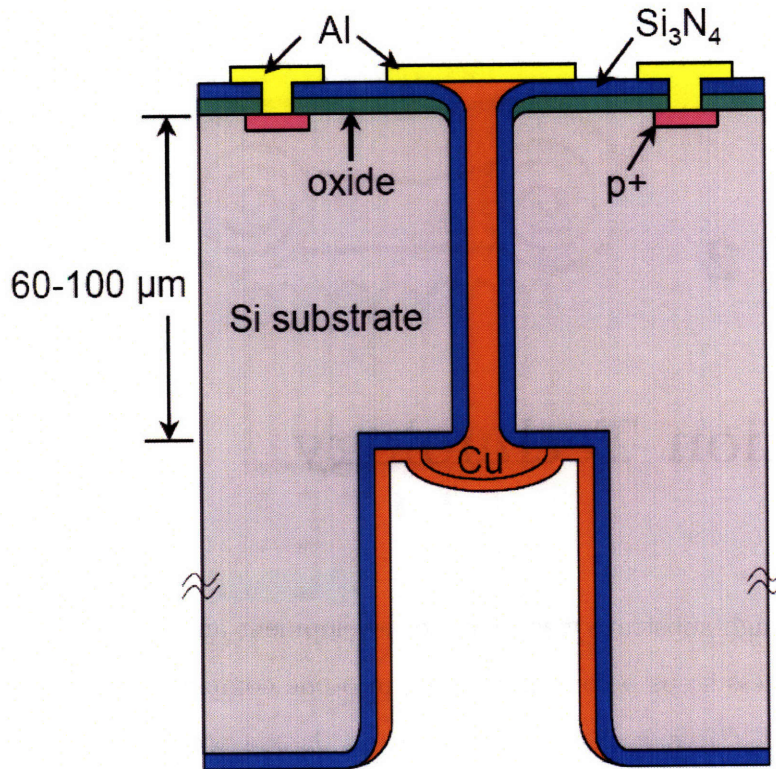


Figure 2-1: Sketch of a cross-section of a through-substrate via.

## 2.1 Fabrication Process Flow

Through-substrate vias were fabricated on n- and p-type wafers ( $0.01\text{--}10\ \Omega\cdot\text{cm}$ ) that were locally thinned to  $60\text{--}100\ \mu\text{m}$  in backside trenches. The vias in the same DRIE trench were connected to each other but not to vias in other trenches so that power, ground, and signals could be routed on backside of the same chip. The process flow is depicted in Fig. 2-2, and the complete fabrication details and recipes are described in Appendix A.

The through-substrate via process began with a boron  $p^+$  implant using thermal oxide and resist as a mask. To thin the wafers down to  $60\text{--}100\ \mu\text{m}$ , trenches were etched from the backside of the wafer using an anisotropic, deep reactive-ion etch (DRIE). DRIE etches nearly vertical sidewalls so that the trenches had a much smaller footprint than when using a KOH etch [2, 8, 41]. The through-substrate vias were

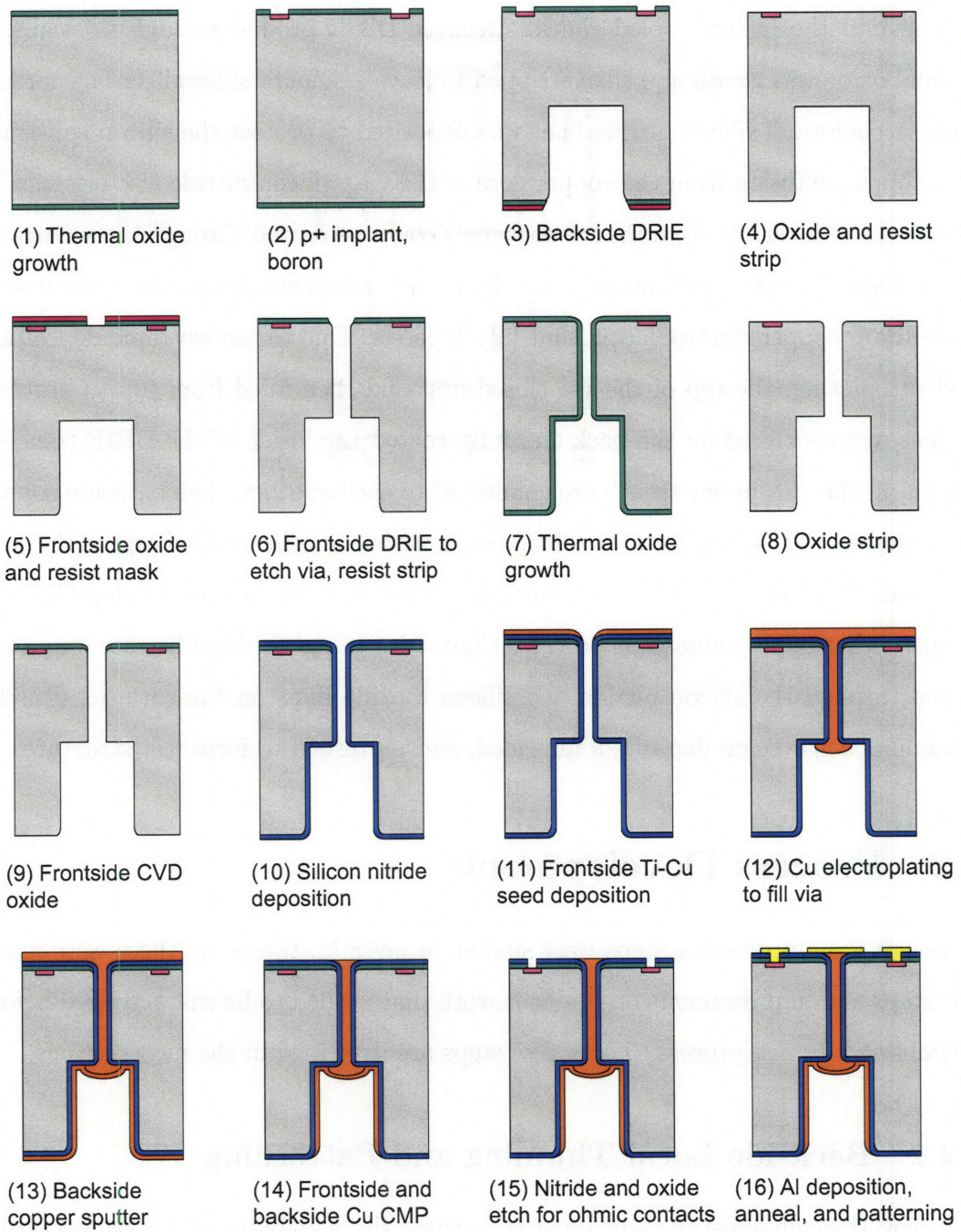


Figure 2-2: Through-substrate via process flow.

etched from the frontside also by DRIE using resist and deposited oxide as a mask. This was a through etch, so a handle wafer was needed to prevent etch gases from passing into the helium-cooled chuck. Because DRIE produces rough sidewalls, a thermal oxide was grown and then stripped to leave a smooth sidewall surface for the liner. A conformal silicon nitride liner was deposited to protect the silicon substrate from copper diffusion from the copper core of the via. Silicon nitride also electrically insulated the substrate from the via so signals could be routed through the substrate.

Proceeding with metallization, a titanium/copper seed was deposited on the frontside to facilitate copper electroplating that filled the via. Due to the isotropic deposition of electroplating, the top of the via closed first and then filled from top to bottom. Copper was sputtered on the back and fully coated the inside of the DRIE trenches so that all the vias in one trench are connected to each another. The backside copper was removed by CMP to isolate each trench from one another while keeping the copper inside the trench intact. The frontside copper was also removed using CMP to complete the copper damascene process. Contact openings to the substrate were then etched through the silicon nitride and silicon dioxide films on the surface. Finally, aluminum was e-beam deposited, annealed, and patterned to form test structures.

## **2.2 Process Development**

Although some processing steps were similar to my S.M. thesis [8], there were many new steps and improvements on previous work that needed to be characterized before assembling into one process. These new steps are described in the next sections.

### **2.2.1 Backside Local Thinning and Patterning**

The new through-substrate via process features the capability of backside routing of power, ground, and signals on the same chip. This required backside patterning of the wafer. The wafer also needed to be thinned to create substrates on the order of 100  $\mu\text{m}$ . Thinning the wafer only locally in DRIE trenches maintained the mechanical stability of the wafer so that it could be further processed, since fabrica-

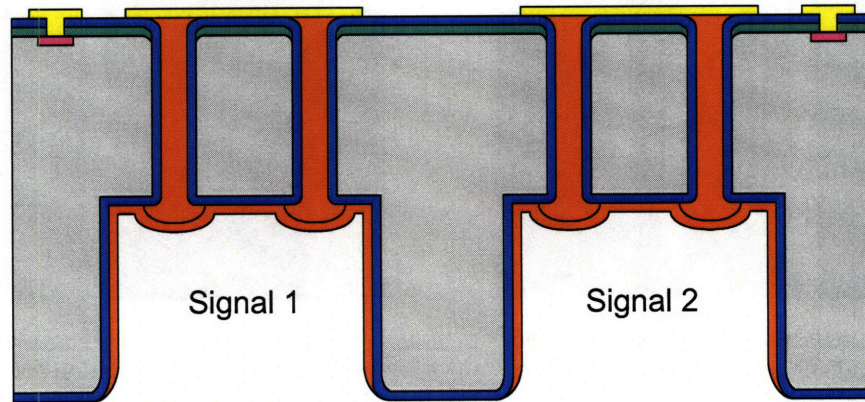


Figure 2-3: Illustration of routing of different signals on the same chip.

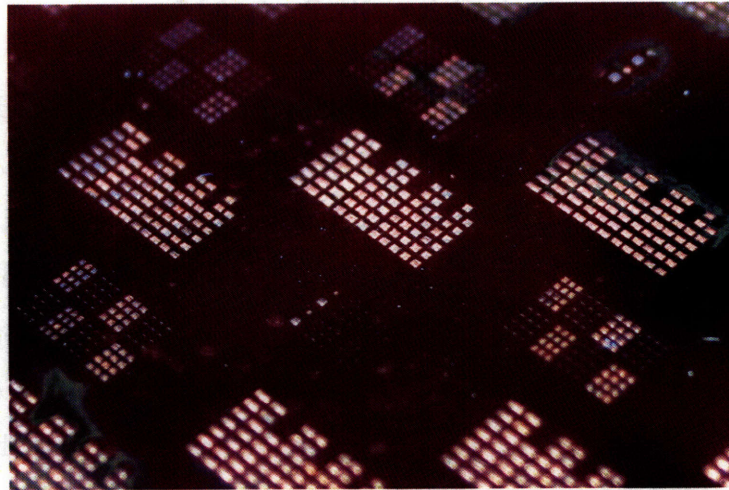
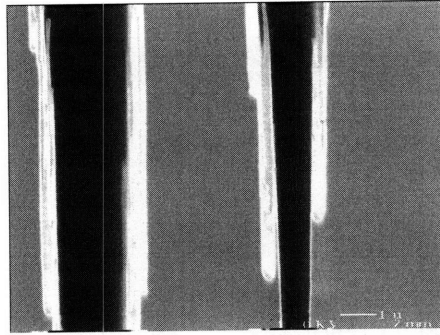
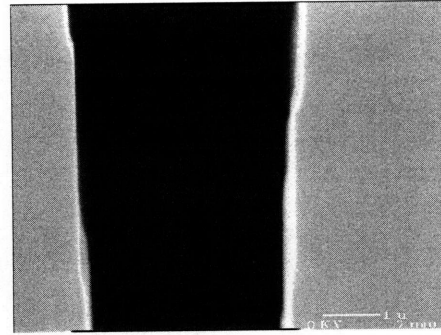


Figure 2-4: Picture of backside DRIE trenches on a finished wafer.

tion experiments in MTL using thin wafers of  $150\text{--}350\text{-}\mu\text{m}$  thick were unsuccessful. By taking advantage of local thinning of the wafer and copper CMP, the backside could be patterned to support multiple signals on the same chip. As seen in Fig. 2-3, through-substrate vias in the same DRIE trench are electrically connected to each other but are isolated from those in other trenches. Finished DRIE trenches on the backside of the wafer are pictured in Fig. 2-4. DRIE will be discussed in the next section.



(a) DRIE pockets etched into the sidewalls of silicon trenches creating a rough surface.



(b) DRIE trench with smooth sidewalls after thermal oxidation and oxide strip.

Figure 2-5: Sidewall smoothing of DRIE trenches.

## 2.2.2 Via Etching and Sidewall Smoothing

The through-substrate vias as well as the backside trenches were etched using Surface Technology Systems DRIE. DRIE is a well-developed process in MTL and was used extensively in my S.M. thesis [8]. Developed by Robert Bosch GmbH, DRIE uses a time-multiplexed, inductively-coupled plasma to etch near-vertical sidewalls in silicon [59]. The alternating cycles of etch ( $\text{SF}_6$ ) and passivation ( $\text{C}_4\text{F}_8$ ) scallop the sidewalls near the surface of the wafer, but the scalloping diminishes as the etch proceeds. However, deeper in the trench/via, pockets etched into the sidewalls roughen the surface, making it difficult to deposit a conformal liner [59]. This DRIE grass is caused by holes in the polymer passivation of the sidewalls and by re-deposition of masking material [59]. A cross-section of trenches displaying DRIE grass is shown in Fig. 2-5a. In order to smooth the sidewalls and ease conformal lining of the vias, thermal oxide was grown to consume the sharp silicon grass and then stripped.  $0.5 \mu\text{m}$  of silicon dioxide was grown at  $1050^\circ\text{C}$  and stripped in buffered oxide etchant (BOE). The resulting smoothed sidewall is shown in Fig. 2-5b.

Another consequence of DRIE is that the via opening widens as the etch proceeds due the slant in the photoresist mask profile and the overetch required to ensure all vias are opened. This produces a small difference between the nominal diameter on

the mask and the actual physical diameter of the via, and consequently, discrepancies in the nominal and actual aspect ratio. Actual aspect ratios will be quoted unless noted otherwise.

### **2.2.3 Silicon Nitride Liner**

As discussed in my S.M. thesis, we chose silicon nitride as the via liner material because of its barrier properties to copper diffusion and its insulating properties to isolate electrical signals of the via from the silicon substrate [60–64]. In my S.M. thesis, we used PECVD to deposit silicon nitride from the front and backside of the wafer [8]. Although PECVD deposits silicon nitride at a low temperature of 400°C, favorable for back-end processing, it was not conformal for trenches of aspect ratios greater than 15 [3, 65].

To improve the conformality of the liner, we decided to use LPCVD nitride in this process, even though the deposition temperature is 775°C. Deposition experiments in silicon trenches show that LPCVD nitride perfectly lines the sidewalls all the way to the bottom. Fig. 2-6 shows PECVD and LPCVD silicon nitride sidewall thickness normalized to the surface thickness of through-substrate vias plotted against via aspect ratio. The sidewall thickness was taken halfway down the via at the thinnest point of the liner. The LPCVD nitride thickness is nearly constant all the way down the via.

### **2.2.4 Copper Electroplating**

The low resistivity of copper allows for high current densities in interconnects, and copper has proven to have increased scalability and better electromigration reliability than Al(Cu) interconnects [66]. Some disadvantages of copper are its poor adhesion to dielectrics and the need for barrier and/or adhesion layers [66]. Copper also has the critical advantage of being able to fill high aspect ratio holes by electroplating.

We used a commercial copper sulfate solution from Enthone-OMI that is used for semiconductor applications and particularly for high-aspect ratio plating. We

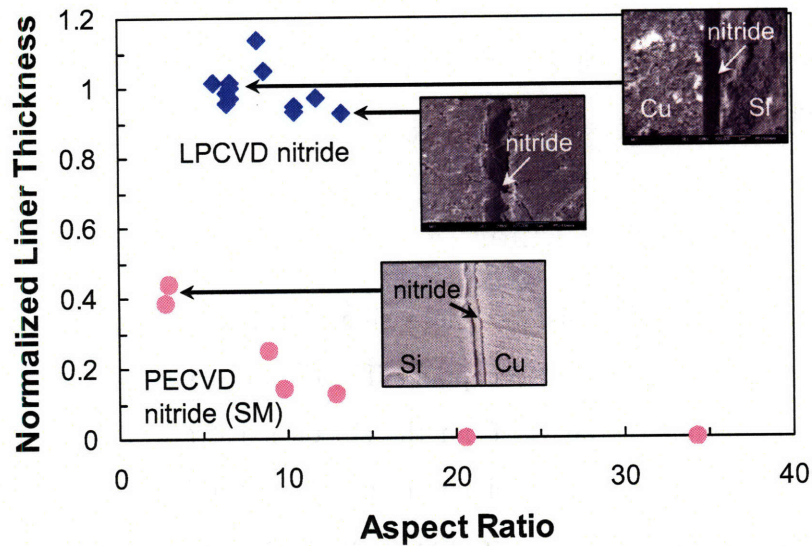


Figure 2-6: Silicon nitride sidewall thickness normalized to surface thickness vs. actual aspect ratio for PECVD nitride from my S.M. thesis and LPCVD nitride. The sidewall thickness was taken halfway down the via at the thinnest point of the liner.

used a Dynatronix DuPR 10-1-3 current supply with a maximum average current of 1 A. We applied a pulse-reverse current, which enhances electro-deposition into high-aspect ratio structures. The dissolution of copper during the negative pulse provides a better concentration gradient of cupric ions in the via than a dc pulse, so that during the subsequent positive pulse, deposition is more uniform and void size is reduced [67–69]. We used the same copper electroplating equipment as in my S.M. thesis, and the details of the setup and electrochemistry can be found there [8]. The basic electroplating procedure remained the same for this new process. However, to improve the efficiency of electroplating and to resolve issues using 150-mm wafers, we implemented several changes for this process.

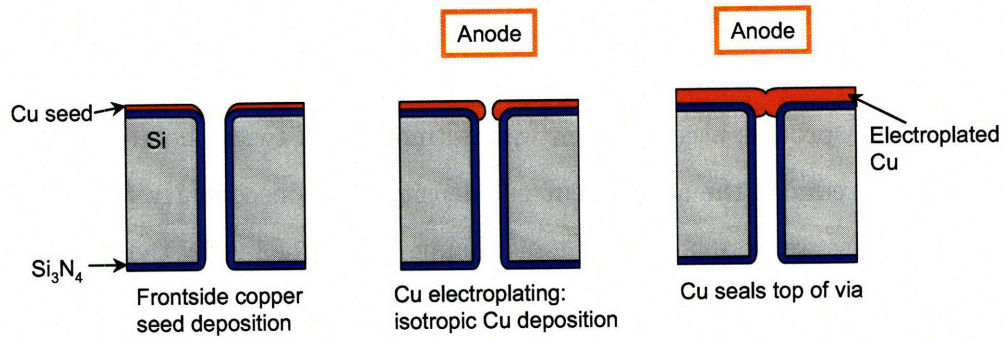
In my S.M. thesis, a Ta-Ti-Cu seed was deposited by e-beam on 100-mm wafers, and the wafer was placed into the copper electroplating solution with the seed facing away from the anode. A pulse-reverse current of 11 mA/cm<sup>2</sup> average was applied. Due to the anisotropy of e-beam deposition and the high-aspect ratio of the vias, the seed did not significantly coat the via sidewalls, and as a result, the seed was perforated.

During copper electroplating, copper deposited onto the seed at the bottom of the via increased in thickness isotropically until the opening closed. Once the via bottom was sealed, the inside of the via filled from bottom to top. This process resulted in a solid Cu core without seams and voids. A similar process has also been reported in [67].

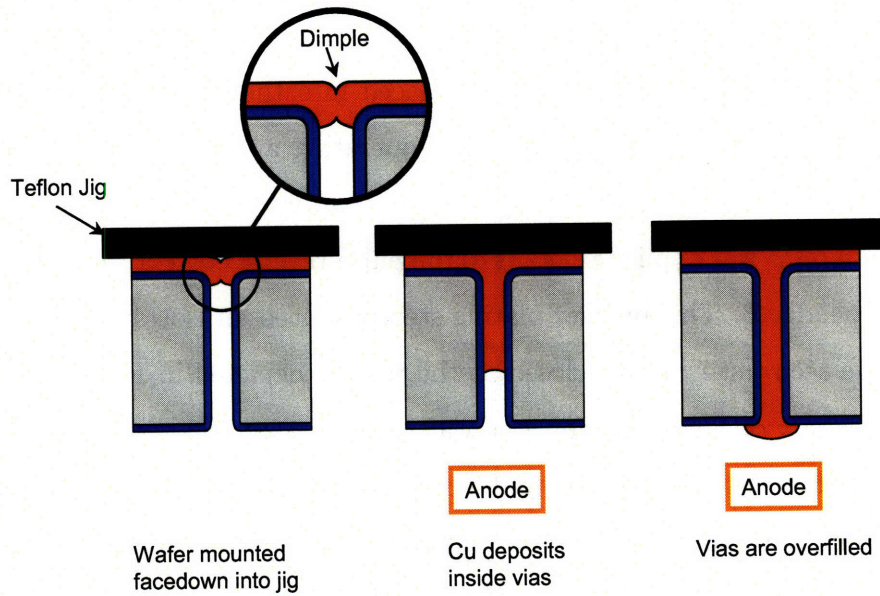
The new via process used 150-mm wafers (more than twice the area of 100-mm wafers), which reduced the applied current density and consequently the rate of deposition. Because we were limited to a maximum current of 1 A by the power supply and the area of the wafer was  $177 \text{ cm}^2$ , the maximum possible current density was  $5.8 \text{ mA/cm}^2$ . Such a low current density would severely prolong the deposition. To solve this problem, we decided to split the electroplating into two steps: blanket plating and jig plating.

After depositing a perforated seed of  $250 \text{ \AA}$  of titanium and  $2000 \text{ \AA}$  of copper on the frontside of the wafer, the wafer was placed into the copper electroplating solution with the seed facing the anode. Since operating at the maximum current frequently produced overcurrent errors on the power supply, a lower average current density of  $4.6 \text{ mA/cm}^2$  was applied. Details of the pulse-reverse current waveform can be found in Appendix B. This blanket plating step produced an isotropic deposition of copper on the seed until the via closed at the top, as depicted in Fig. 2-7a. Due to the non-uniformity of the deposition, the wafer was rotated  $180^\circ$  halfway through the deposition. The cause for the non-uniformity is possibility due to a gradient of copper ions in the bath such that the deposition is greater deeper in the bath. A faster stirring speed would enhance mixing but also increases the dissolved oxygen in the bath. Once all vias had closed, the wafer was removed from the bath.

In the second step, the wafer was placed facedown into a teflon jig so that the frontside would not be exposed to the copper solution (Fig. 2-7b). Loading the wafer into the jig is explained in Appendix C. The jig prevented excess copper from being electroplated onto the frontside so that less copper would have to be removed during CMP. Also, isolating the frontside seed from the solution significantly reduced the surface area to be plated so that a higher current density could be applied.



(a) Blanket plating step.



(b) Electroplating with wafer inserted into jig.

Figure 2-7: Copper electroplating steps to reduce deposition time and excess copper buildup on the seed.

The exposed area was actually too small because only the small amount of copper inside the vias was exposed to the solution. So two 22-cm<sup>2</sup> dummy pieces electrically connected to the cathode (wafer) were also placed into the solution on either side of the jig (see Appendix C). An average pulse-reverse current of 12.5 mA/cm<sup>2</sup> was applied until all vias were filled. The wafer was rotated 180° halfway through the deposition because of the non-uniformity of the deposition, and then the vias were overfilled. Also, because the vias were filled from top to bottom into the backside trenches, the vias could be significantly overfilled without problems in order to ensure that all vias were filled. Since all vias in each DRIE trench would eventually be connected to each other, overplated copper vias that grew into each other actually helped the process. Using the jig, the amount of excess copper plated onto the seed reduced to 10–20 μm from 40 μm of the S.M. process [8].

Pictures of the electroplating jig are displayed in Fig. 2-8, and the jig specifications are described in Appendix C. The jig was composed of two pieces of Teflon, one with a hole slightly smaller than a 150-mm wafer, and a dummy silicon wafer. The processed wafer was placed facedown on the dummy wafer so that the frontside was protected by the dummy wafer. Both were inserted into the jig between the two teflon pieces, which clamped together using teflon screws. O-rings on the inside of each teflon piece ensured a tight seal between the wafer and jig. The jig plating procedure is also detailed in Appendix C.

### **2.2.5 Copper Chemical-Mechanical Polishing**

Chemical-mechanical polishing (CMP) was a critical component to this process. It was required to complete the copper damascene process and to isolate signals on the backside. After copper electroplating, excess copper on the frontside needed to be removed to reveal the through vias. On the backside, the sputtered copper needed to be removed from the surface but kept intact inside the DRIE trenches. Using the copper CMP tool in MTL, the frontside copper was polished off first and then the backside. The CMP tool parameters are listed in Table A.4. Silicon nitride was used as the etchstop. After CMP, the wafers were polished in water with a polyvinyl

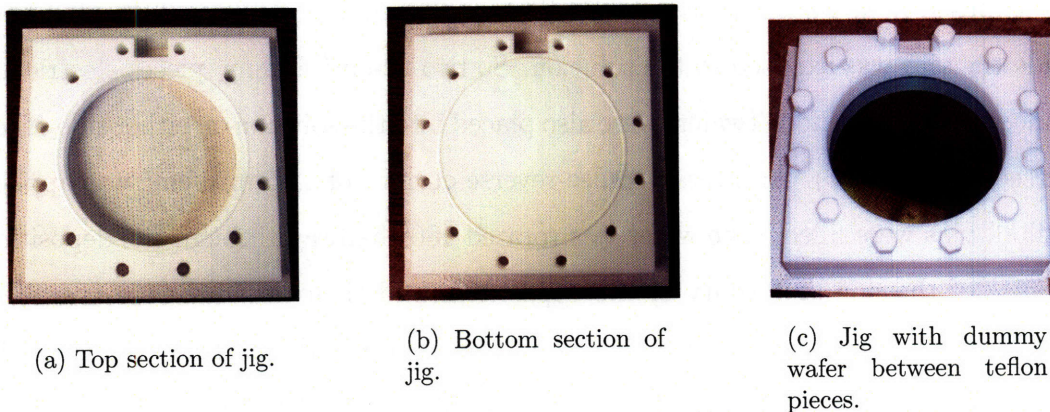


Figure 2-8: Teflon jig to protect wafer frontside during copper electroplating.

alcohol (PVA) sponge and then soaked in dilute citric acid (9000 ppm) to dislodge and remove excess slurry particles.

The difficulty in using the CMP was its propensity to break wafers. Starting with eleven wafers, five whole wafers survived and one partial wafer, which was polished by hand after it had cracked. None of the SOI wafers survived due to the beveled wafer edge of the device layer, so the wafer would slip out from the polish head and break.

CMP revealed some voids present near the top of the vias (Fig. 2-9a). The top of the via was the most critical point in the copper electroplating because the copper solution must reach all way down the via to successfully deposit copper. Although some voiding is apparent, most of the wafer was free from voids (Fig. 2-9b). Dimples present on some vias are a result of the seed closing the via hole during blanket plating and are not voids.

## 2.2.6 Ohmic Contacts

Ohmic contacts to the silicon substrate were needed for the improved test structures and to measure via sidewall capacitance. Ohmic contacts required a high-dose  $p^+$  implant, activation, and an aluminum contact anneal. To avoid sending fragile wafers etched with deep trenches out for implant, the  $p^+$  implant was placed at the beginning

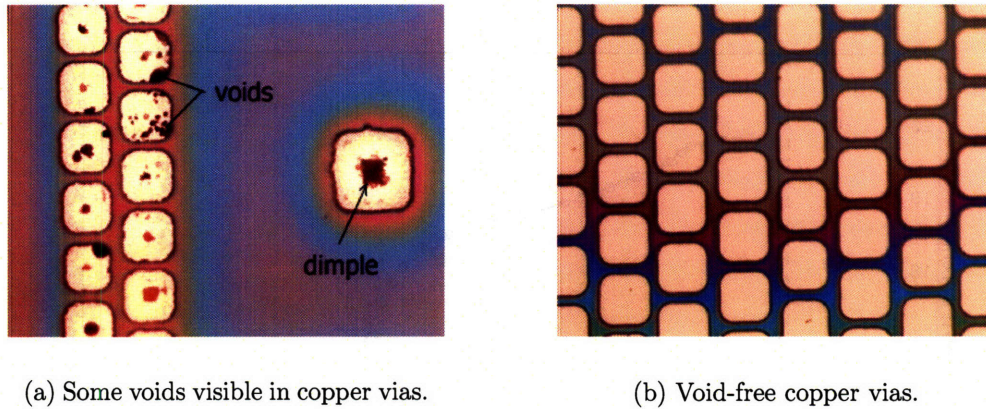


Figure 2-9: Microscope pictures of copper vias after CMP.

of the process. The activation of the implant was combined with the high-temperature (1050°C) thermal oxidation for sidewall smoothing. Because of the long duration of the oxidation (70 minutes), the boron implant would diffuse away from the surface and segregate into the growing silicon dioxide, depleting carriers from the surface [70]. In order to achieve the doping of at least  $6 \times 10^{19} \text{ cm}^{-3}$  required to create an ohmic contact, a high-dose implant was required [70]. From SUPREM simulations, a boron implant of  $2 \times 10^{16} \text{ cm}^{-2}$  at 150 keV gave the needed  $6 \times 10^{19} \text{ cm}^{-3}$  doping near the surface for an ohmic contact. Fig. 2-10 plots the SUPREM simulation of the boron concentration at the silicon surface. Appendix D contains the SUPREM simulation file.

To complete the ohmic contact, aluminum was e-beam deposited on the heavily-doped silicon surface. A sintering anneal at 450°C in forming gas ensured a good contact to the silicon by reducing the native oxide at the surface [70]. Using pure aluminum contacts can produce “spikes” into the silicon substrate because of the high solubility of silicon into aluminum [70]. However, the test structures that use ohmic contacts are on p-type substrates so this was not a concern for this process.

We used the transmission line model (TLM) to determine contact resistance [71]. The resistance between two contacts of identical size, spaced at varying intervals like those in Fig. 2-11 was measured with an HP4155. The contact width,  $w$ , was 50  $\mu\text{m}$ ,

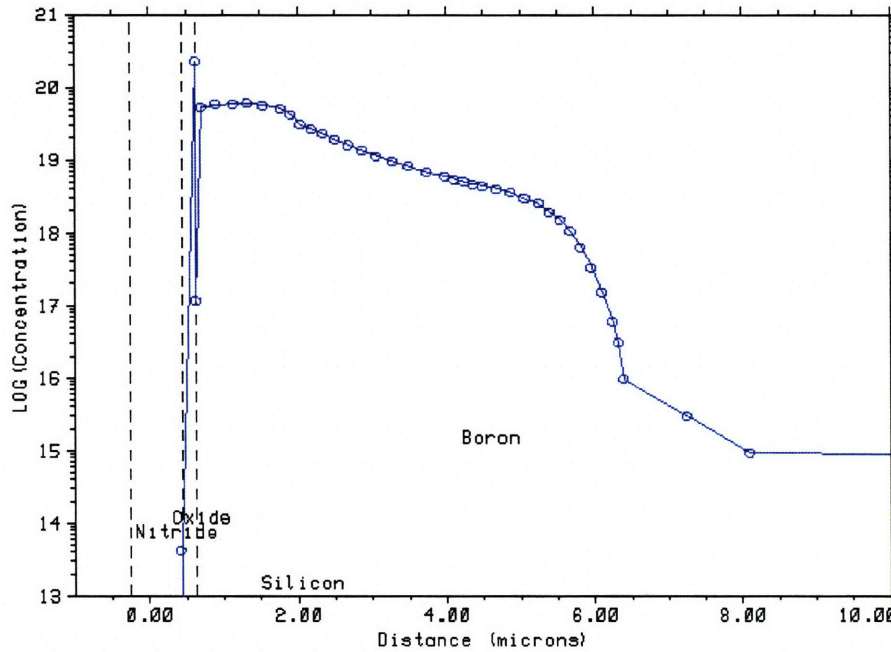


Figure 2-10: SUPREM simulation of the boron doping concentration at the oxide-silicon interface and into the silicon substrate. The implant dose was  $2 \times 10^{16} \text{ cm}^{-2}$  at 150 keV. An oxidation at  $1050^\circ\text{C}$  for 70 minutes activated the dopants. Boron segregation into the oxide is evident as well as diffusion of boron about  $6 \mu\text{m}$  into the substrate.

and the length,  $l$ , was also  $50 \mu\text{m}$ . The measured resistance was plotted against pad separation distance (Fig. 2-12), where the  $y$ -intercept gave the pad contact resistance for both pads,  $2R_c$ , and the slope gave the sheet resistance of the diffusion per unit width,  $\frac{R_{SH}}{w}$ . For the green line (diamonds) in Fig. 2-12, the  $y$ -intercept is  $4.8 \Omega$  and the slope is  $0.14 \Omega/\mu\text{m}$ . This gives a contact resistivity of  $0.24 \Omega\cdot\text{mm}$  and a sheet resistance,  $R_{SH}$ , of  $7 \Omega/\square$  for  $w = 50 \mu\text{m}$ .

However, we want the contact resistance characterized by its contact resistivity,  $\rho_c$ , in  $\Omega\cdot\text{cm}^2$ . First, we must obtain the transfer length defined as [71]:

$$L_T = w \frac{R_c}{R_{SK}} \quad [\mu\text{m}] \quad (2.1)$$

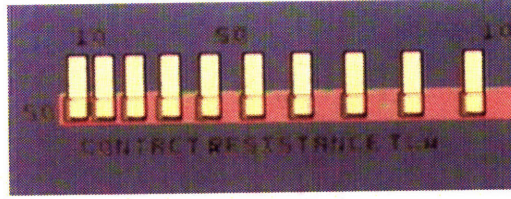


Figure 2-11: Picture of contacts used to measure metal-semiconductor contact resistance. The contact area is  $50 \mu\text{m} \times 50 \mu\text{m}$ .

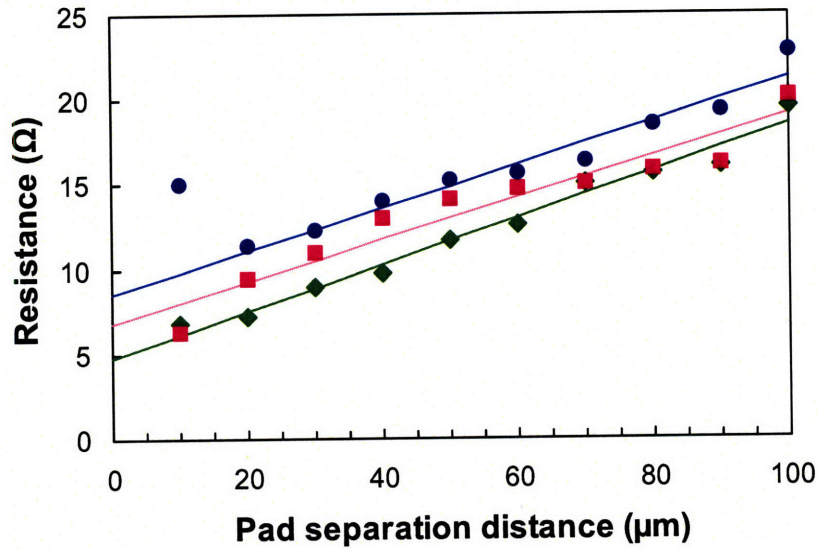


Figure 2-12: Measured resistance vs. pad separation distance. The  $y$ -intercept gives the contact resistance of two pads.

where  $w$  is the width of the contact,  $R_{SK}$  is the modified sheet resistance of the substrate directly under the contact, and  $R_c$  is the contact resistance obtained from Fig. 2-12. The transfer length is the distance from the edge of the contact to where the current density through the contact interface drops to  $1/e$  of the leading edge [70]. From the transfer length, the specific contact resistivity is given by [71]:

$$\rho_c = R_{SK}(L_T)^2 \quad [\Omega \cdot \text{cm}^2] \quad (2.2)$$

We have assumed that annealing of the contact did not significantly change the sheet

resistance under the contact so that  $l \gg L_T$  and so  $R_{SK} = R_{SH}$ . Plugging Equation 2.1 into Equation 2.2 gives:

$$\rho_c = \frac{(R_c w)^2}{R_{SH}} \quad [\Omega \cdot cm^2] \quad (2.3)$$

From the data in Fig. 2-12, Equation 2.3 gave a specific contact resistivity of  $2 \times 10^{-5} \Omega \cdot cm^2$ . This is high for contact resistivity; however, due to non-uniformity in current flow and current crowding around the contact,  $\rho_c$  is overestimated in experimental test structures [70]. Also, the actual doping level at the surface is probably lower than simulations due to out-diffusion of dopants in process steps following the implant. In spite of the high value of  $\rho_c$ , contact resistance was not an issue in our measurements since the currents were small and the contact areas large.

## 2.3 Process Integration

Combining the process steps characterized separately into one complete process required special attention to copper contamination issues and process sequence. The implant was placed ahead of DRIE to avoid sending out fragile wafers. The thermal oxide grown to mask the implant was also used as a mask for the backside DRIE. The backside DRIE is a much longer etch than the frontside, so a thick thermal oxide was needed as the mask, so the backside had to be etched first. Because the implant would be activated during the thermal oxide sidewall smoothing step, additional high-temperature steps after the implant were forbidden. Therefore, the frontside DRIE mask was deposited oxide instead of growing another thermal oxide. Also, because the frontside was etched after the backside, it was a through etch, which was beneficial as an indicator to when the etch was done. Deposition of the nitride liner was the next natural step in order to line the vias and protect the silicon from copper contamination. Next was copper filling of the vias and CMP. Metallization for the test structures proved to be the most troublesome part of the process integration because of unforeseen interactions in chemical processing.

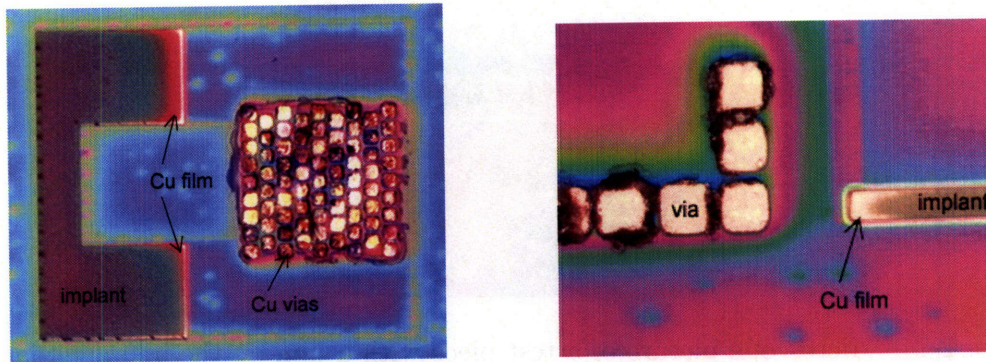


Figure 2-13: Microscope pictures of electroless-plated copper on implanted areas of silicon after etching in BOE. The multi-colored film on the implant had a metallic sheen in areas closest to copper vias.

The first problem in metallization arose when etching contact holes to the  $p^+$  silicon substrate. This required a silicon nitride plasma etch that stopped on silicon dioxide and then a wet etch of silicon dioxide using BOE, both using photoresist as a mask. While the plasma etch was straightforward, the wet etch of oxide presented complications. While etching the oxide in BOE, a multi-colored film appeared on the implanted  $p^+$  silicon but not on undoped silicon. Fig. 2-13 shows pictures of this film on the implanted silicon. This film was characterized by a blue-green hue, and in implanted areas near copper vias, the film had a metallic sheen similar to copper. To verify if the film was indeed copper and not residual oxide, a test piece was etched in a copper etchant solution of 1:1:50 HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O. After the copper etch, the metallic film had disappeared, and the result is shown in Fig. 2-14. The copper film on the implant was apparently the result of electroless plating of copper from the vias onto the high-energy implanted silicon, instigated by the BOE wet etch. The easiest way to avoid this was to use a dry etch. However, a plasma etch for oxide on copper-contaminated wafers was not available in MTL. The best compromise was to use HF gas to etch the oxide, which reduced the severity of the electroless copper plating (Fig. 2-15).

The second issue arose when annealing the aluminum contacts. Initially, the

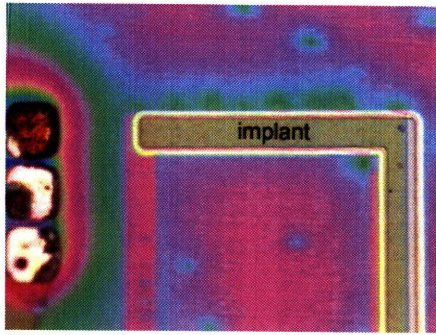


Figure 2-14: Microscope picture of a test piece with a film on the implant that was etched in copper etchant. The metallic sheen has been removed by the copper etch.

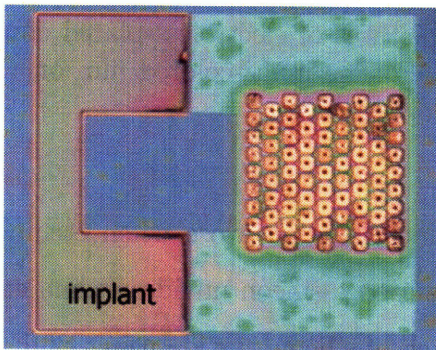


Figure 2-15: Microscope pictures of the silicon implant after etching oxide using HF gas.

contact anneal was the last step in the process, after the aluminum deposition and patterning of test structures. However, because the aluminum also covered the tops of the copper vias, during the anneal, the copper expanded out from the silicon surface due to the thermal expansion mismatch of silicon and copper. Because of this copper extrusion, the aluminum on top of the via detached from the rest of the aluminum pad and was no longer electrically connected (Fig. 2-16). Fig. 2-17 shows pictures of aluminum on copper vias before and after the anneal. To resolve this problem, the metallization was split into two steps: a contact mask and the final metallization mask. The first deposition of aluminum ( $0.4 \mu\text{m}$ ) contacted the implant. This was annealed then patterned with the CONTACT mask, which was the inverse of the NITRIDE etch mask. Fig. 2-18a shows the annealed aluminum contact. In the second step, a thicker aluminum film ( $1 \mu\text{m}$ ) was deposited on top of the aluminum

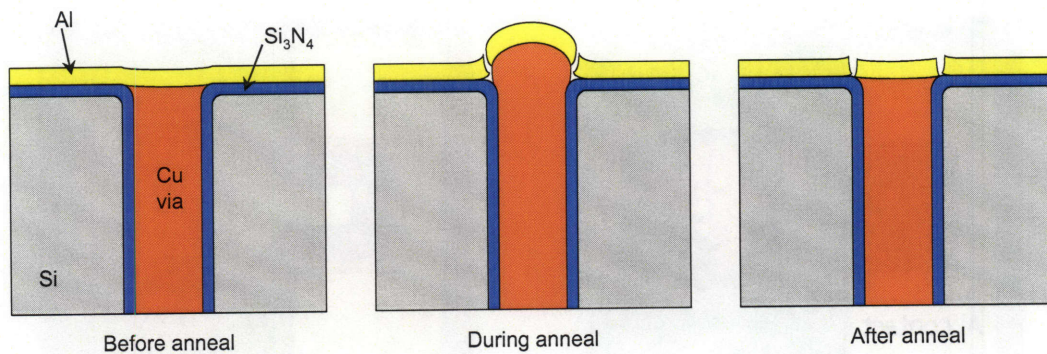
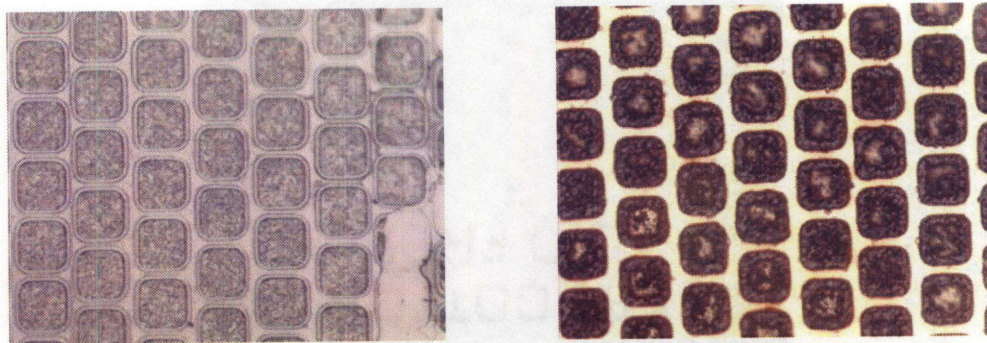


Figure 2-16: Depiction of copper-via extrusion during contact anneal. Aluminum atop the via detaches from the surrounding field aluminum destroying electrical contact to the via.



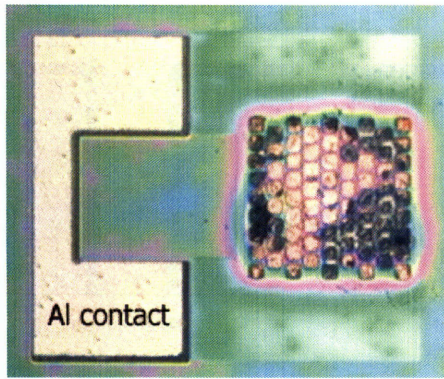
(a) Copper vias before anneal.

(b) Copper vias after anneal. The aluminum on the vias has detached from the surrounding aluminum pad.

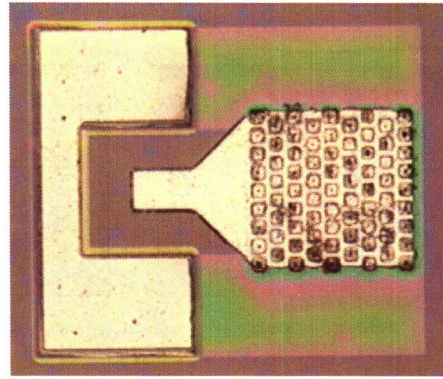
Figure 2-17: Microscope pictures of aluminum film on top of copper vias before and after annealing.

contacts and copper vias and patterned to create the test structure pads (Fig. 2-18b). Since the contacts were already annealed, the aluminum on the copper vias stayed intact.

A cross-section picture of completed through-substrate vias of aspect ratio 8 is shown in Fig. 2-19. Fabricated vias had a nominal diameter of 2–30  $\mu\text{m}$ , with nominal aspect ratios as high as 50.



(a) Annealed aluminum contact on  $p^+$  silicon.



(b) Final aluminum metallization.

Figure 2-18: Microscope pictures of first and second aluminum metallizations.

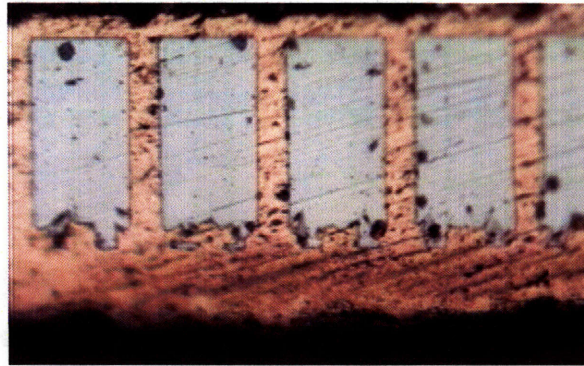


Figure 2-19: Cross-section of through-substrate vias before CMP. The vias are  $13\text{-}\mu\text{m}$  in diameter and  $100\text{-}\mu\text{m}$  in height.

## 2.4 Manufacturing Modifications

Through-substrate via fabrication is intended to be a back-end process. However, the two high-temperature steps used in this process, thermal oxidation for sidewall smoothing and LPCVD silicon nitride, would prevent this. These high-temperature steps were used for expediency to demonstrate the process. The rough sidewalls created by DRIE can be reduced or eliminated by adjusting the etch and passivation process parameters so that the thermal oxidation for sidewall smoothing becomes unnecessary [34, 72]. Also, the sidewalls could be smoothed by chemical etching

[73]. For the barrier liner, we need a conformal, insulating liner deposited at a low temperature. Developing a more conformal PECVD silicon nitride is a possibility, as the PECVD used in my S.M. thesis was not optimized. Another option is to use PECVD tetraethyl orthosilicate (TEOS), which is deposited at 350°C and is significantly more conformal than silicon nitride. TEOS is not a barrier to copper diffusion, so a metal barrier layer of sputtered titanium nitride (TiN) or tantalum nitride (Ta<sub>3</sub>N<sub>5</sub>) would be required [74–76]. Also, silicon oxy-nitride is also an alternative material that is more conformal than silicon nitride [60–62].

## 2.5 Summary

The through-substrate via process required extensive development for each new process step. Backside thinning and patterning, smoothing of DRIE-etched via sidewalls, the silicon nitride liner, copper electroplating and CMP, and ohmic contacts all needed to be characterized before assembling into one process. Careful consideration of process order was essential, and unforeseen complications during process integration were resolved. The next chapters will discuss the via impedance measurements and the application of these vias for substrate noise isolation.



## Chapter 3

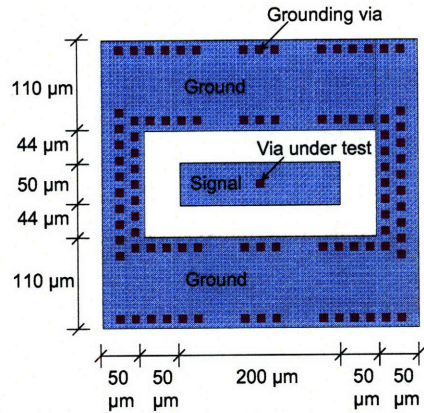
# Measurement and Characterization of Through-Substrate Vias

The new through-substrate via process incorporated several new steps to accommodate new test structure designs that more accurately measure via impedance. The through-substrate vias were electrically characterized by measuring scattering ( $S$ ) parameters of one-port and two-port test structures and extracting the inductance, resistance, and sidewall capacitance of a single via. The measured values were compared to theoretical calculations.

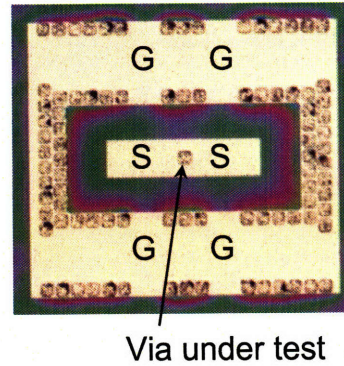
### 3.1 Test Structure Design

We characterized the through-substrate vias using a new two-port, coplanar ground-signal-ground, RF test structure pictured in Fig. 3-1. The ground lines are punctuated by many vias to reduce the impedance from the copper backplane to the ground pads. Ground vias are 10- $\mu\text{m}$  in diameter. The copper backplane lines the backside DRIE trench, which extends to the edge of the aluminum ground pads. The via under test lies in the center of the signal line. Using a two-port test structure instead of the one-port structure in my S.M. thesis reduced the parasitic resistance and inductance, which gave more accurate measurements.

The sidewall capacitance of the via to the substrate was measured using the one-



(a) Layout drawing and dimensions of the impedance test structure.

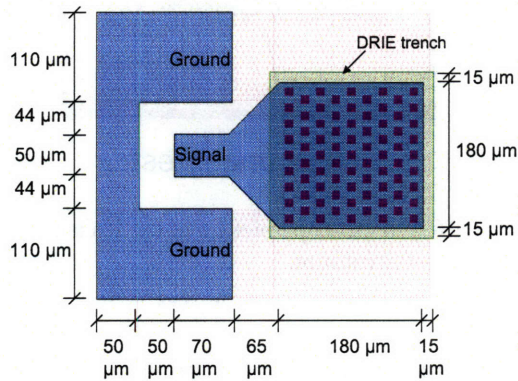


(b) Microscope picture of the impedance test structure.

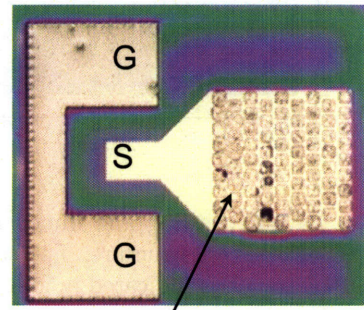
Figure 3-1: Two-port, coplanar RF test structure used to measure the impedance of a single via. Ground vias are 10- $\mu\text{m}$  in diameter. The backside DRIE trench extends to the outside edge of the aluminum ground pads.

port test structures in Fig. 3-2 on  $p^+$  wafers of resistivity 0.03  $\Omega\cdot\text{cm}$  or less. The signal is the top aluminum plate, which is connected to the via array, and ground is the  $p^+$  implant, which is connected to the silicon surrounding the vias. To minimize the impact of pad capacitance, the test structure consists of arrays of 77 and 431 vias in parallel. Vias in the arrays are 10- $\mu\text{m}$  in diameter. The vias in the array are connected to one another at the top through the aluminum pad and at the bottom by a copper backplane that lines the backside DRIE trench. This square trench extends 15  $\mu\text{m}$  beyond the aluminum pad of the array and is indicated in Fig. 3-2.

The integrity of the liner was evaluated by measuring current leakage across the silicon nitride liner using the test structure in Fig. 3-3. The left pad is connected to the top of the copper via(s), which are arranged in arrays of one to four vias in parallel. The right pad is connected to the silicon surrounding the via(s) through an ohmic contact to the substrate. The backside DRIE trench is 110  $\mu\text{m} \times 50 \mu\text{m}$ , indicated in Fig. 3-3. Via diameter was varied from 2–10  $\mu\text{m}$ . Current leakage across the larger via arrays in Fig. 3-2 were also measured.

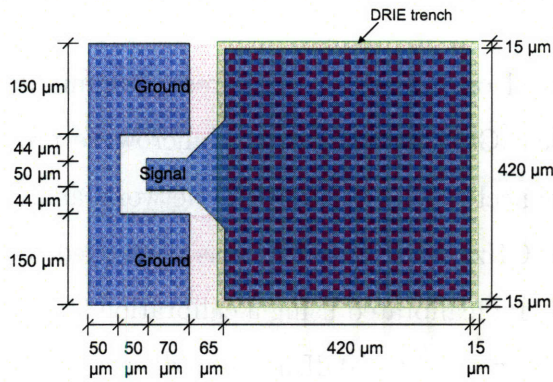


(a) Layout drawing and dimensions of the capacitance test structure with 77-via array.

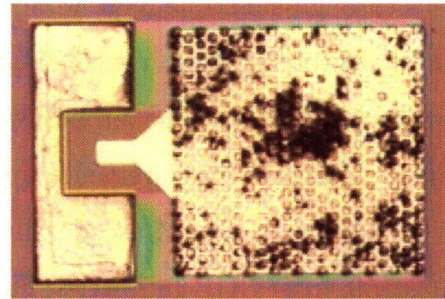


Capacitor via array

(b) Microscope picture of the capacitance test structure with 77-via array.

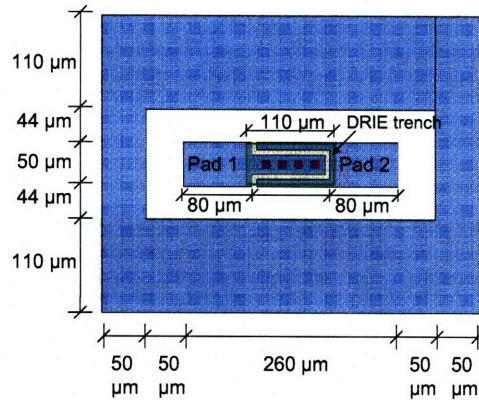


(c) Layout drawing and dimensions of the capacitance test structure with 431-via array.

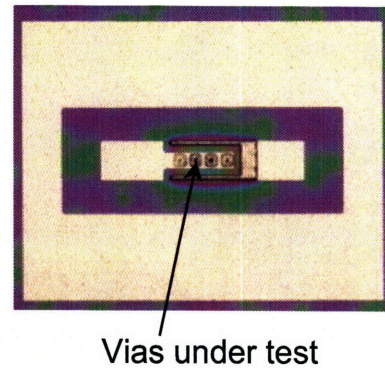


(d) Microscope picture of the capacitance test structure with 431-via array.

Figure 3-2: One-port, coplanar RF test structure used to measure via sidewall capacitance. Vias in the array are  $10 \mu\text{m}$  in diameter and spaced by  $10 \mu\text{m}$ . The backside DRIE trench extends  $15 \mu\text{m}$  beyond the aluminum pad of the via array, indicated in the layout drawings.



(a) Layout drawing and dimensions of the leakage test structure. The backside DRIE trench is indicated in green.



(b) Microscope picture of the leakage test structure.

Figure 3-3: Test structure used to measure current leakage across the silicon nitride liner. Via diameter was varied from 2–10  $\mu\text{m}$ .

## 3.2 Measurement Setup

The through-substrate vias were measured on a Cascade Microtech Summit 9600 thermal probe station using 125- $\mu\text{m}$  pitch, GGB Industries Inc. microwave probes rated to 40 GHz. The probes were connected to an HP8510C network analyzer for  $S$  parameter measurements up to 50 GHz. The HP8510C was controlled using WinCal software from Cascade Microtech and calibrated using a calibration standard substrate from GGB Industries, Inc. Power was set to 10 dBm and 0 dB attenuation.

For the two-port impedance test structure,  $S_{21}$  was measured from 100 MHz to 50 GHz.  $S_{21}$  is defined as the transmission coefficient from port 1 to port 2 when port 2 is terminated by a 50- $\Omega$  matched load. For analysis, measured  $S_{21}$  data was converted to  $Z_{21}$ . For the one-port capacitance test structure,  $S_{11}$  was measured up to 50 GHz and is defined as the reflection coefficient seen at port 1. Measured  $S_{11}$  data was converted to  $Z_{11}$  for analysis. The  $Z$  parameter results will be discussed in the next section.

The leakage current was measured on the same probe station but using dc probes and an HP4155. The wafer chuck was grounded to the HP4155 in all measurements.

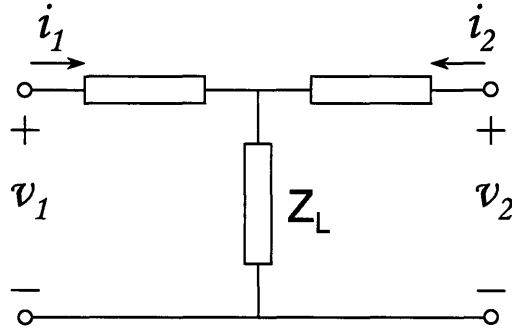


Figure 3-4: Equivalent circuit model of the impedance test structure in Fig. 3-1, where  $Z_{21} = Z_L$ .

### 3.3 Results and Discussion

From the converted  $Z$  parameter data, we were able to extract the inductance, resistance, and sidewall capacitance of a single via. Simple circuit models and theoretical calculations are used to explain these results.

#### 3.3.1 Via Model

$Z_{21}$  measurements of the impedance test structure in Fig. 3-1 can be modeled by the circuit in Fig. 3-4, where  $Z_{21}$  is defined as:

$$Z_{21} = \left. \frac{v_2}{i_1} \right|_{i_2=0} \quad (3.1)$$

which is equivalent to the impedance,  $Z_L$ , so that,

$$Z_{21} = Z_L \quad (3.2)$$

Looking at the real and imaginary  $Z_{21}$  data in Fig. 3-5, the through-substrate via can be represented by a simple circuit model of a inductor and resistor in series and is

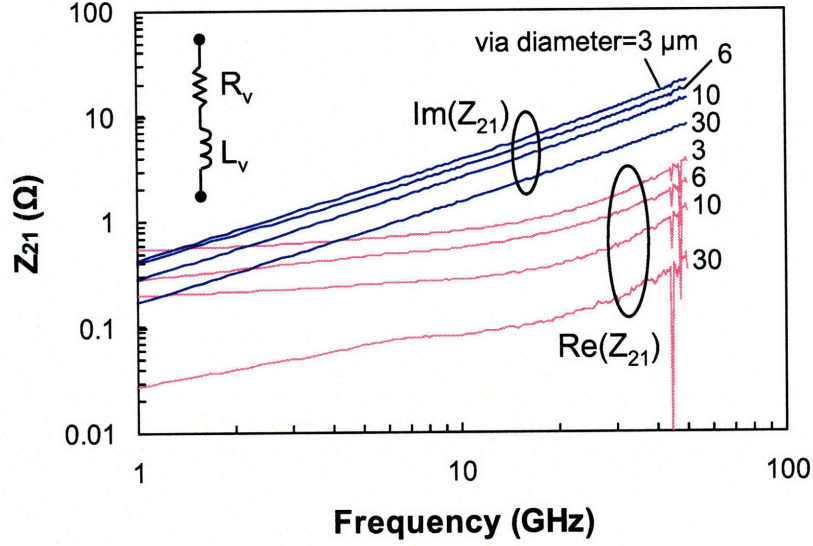


Figure 3-5:  $Z_{21}$  vs. frequency for vias of diameter 3, 6, 10, and 30  $\mu\text{m}$ . The real part represents resistance and rises at high frequency due to the skin effect. The imaginary part increases with a unity slope, indicative of inductance.

defined as [8]:

$$Z_{21} = R_v + j\omega L_v \quad (3.3)$$

The real part represents resistance,  $R_v$ , and the imaginary part,  $\omega L_v$ , rises linearly with frequency. From this circuit model, the resistance and inductance of a via can be extracted from measurements. Fig. 3-5 plots  $Z_{21}$  for different size vias. As via diameter decreases, both the resistance and inductance increase.

As seen in Fig. 3-5, the real part increases with frequency due to the skin effect. At higher frequencies, the resistance increases as current crowds to the sidewalls of the via. Current travels along the copper via sidewall down to the skin depth, which is defined as [77]:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad [m] \quad (3.4)$$

where  $f$  is the frequency,  $\mu$  is the permeability, and  $\sigma$  is the conductivity. For non-magnetic materials, the permeability is  $4\pi \times 10^{-7}$  H/m, and the conductivity of copper is  $5.80 \times 10^7$  S/m. At 1 GHz, the skin depth in copper is 2.1  $\mu\text{m}$  and decreases to 0.3

$\mu\text{m}$  at 50 GHz. This is thin enough to affect the resistance and inductance in even the smallest diameter via ( $2 \mu\text{m}$ ) and is apparent in the  $Z_{21}$  measurements.

### 3.3.2 Inductance

Via inductance and resistance were extracted from  $S$  parameter measurements taken using the impedance test structure shown in Fig. 3-1. Fig. 3-6 plots the extracted inductance (blue diamonds), which was taken at 10 GHz from three different wafers, against nominal aspect ratio. Previous work [3] is also plotted in Fig. 3-6 (pink circles). The new data shows a much lower inductance, attributed to reduced parasitics of the two-port test structure. To our knowledge, this is the lowest inductance reported for high-aspect ratio, through-substrate vias. Record-low inductance of 150 pH/mm for small-aspect ratio vias of aspect ratio 2.6 and 3.9 has been reported by [51]. The spread in the data in Fig. 3-6 is due to the variation in substrate thickness ( $60\text{-}100 \mu\text{m}$ ) from the backside DRIE trench etch, which affects the actual aspect ratio and the calculation of inductance per unit length. For example, for a  $10\text{-}\mu\text{m}$  diameter via, the aspect ratio for a substrate thickness of  $100 \mu\text{m}$  would be 10 and for a substrate thickness of  $60 \mu\text{m}$  would be 6. An average via height of  $80 \mu\text{m}$  for the aspect ratio was used for the data in Fig. 3-6.

We now put these results in the context of established via inductance models. The theoretical self-inductance of a cylindrical wire of non-magnetic material in free space has been derived by E. B. Rosa as [4]:

$$L = \frac{\mu_0}{2\pi} \left[ h \cdot \ln \left( \frac{h + \sqrt{h^2 + r^2}}{r} \right) + r - \sqrt{h^2 + r^2} + \frac{h}{4} \right] \quad [H] \quad (3.5)$$

where  $\mu_0 = 4\pi \times 10^{-7}$  H/m,  $h$  is the height, and  $r$  is the radius of the cross-section. Assuming  $h \gg r$ , this can be approximated by [4]:

$$L = \frac{\mu_0}{2\pi} h \left( \ln \frac{2h}{r} - \frac{3}{4} \right) \quad [H] \quad (3.6)$$

This approximation breaks down for small aspect ratios, and reaches an error of 10%

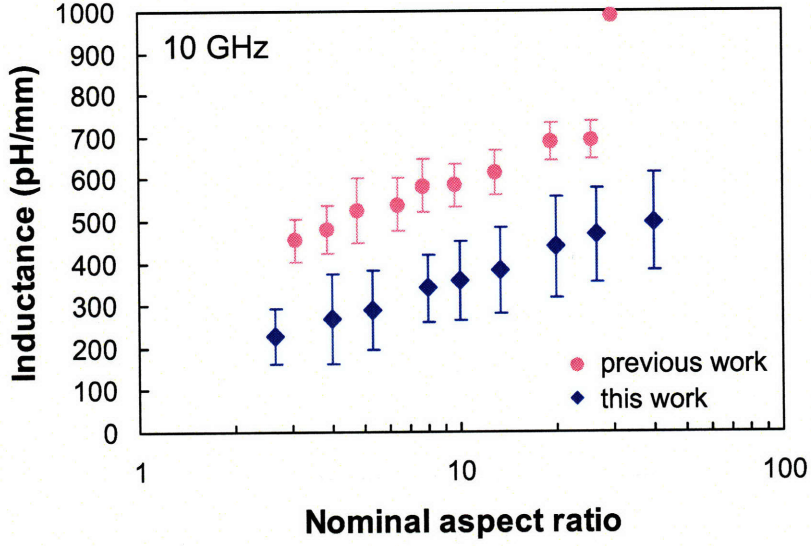


Figure 3-6: Via inductance vs. nominal aspect ratio of a via at 10 GHz. The measured inductance data (blue diamonds) falls below previous work [3] (pink circles) by using a two-port test structure.

at an aspect ratio of 2.65, which is the lower limit of our data. At high frequencies when the skin effect dominates, the self-inductance decreases to [4,5]:

$$L = \frac{\mu_0}{2\pi} h \left( \ln \frac{2h}{r} - 1 \right) \quad [H] \quad (3.7)$$

which is a small change from Equation 3.6. Rearranging Equation 3.7 in terms of aspect ratio,  $a = \frac{h}{2r}$ , we get:

$$\frac{L}{h} = \frac{\mu_0}{2\pi} (\ln 4a - 1) \quad [H/mm] \quad (3.8)$$

where  $h$  is in mm. The self-inductance per unit length depends only on the aspect ratio of the via. This high-frequency equation by Rosa (Equation 3.8) is plotted in Fig. 3-7 with the measured inductance data, and greatly overestimates inductance at high-aspect ratios. Goldfarb *et al.* [6] have empirically modified Equation 3.5 to match their measurements and numerical simulations of a cylindrical via hole to:

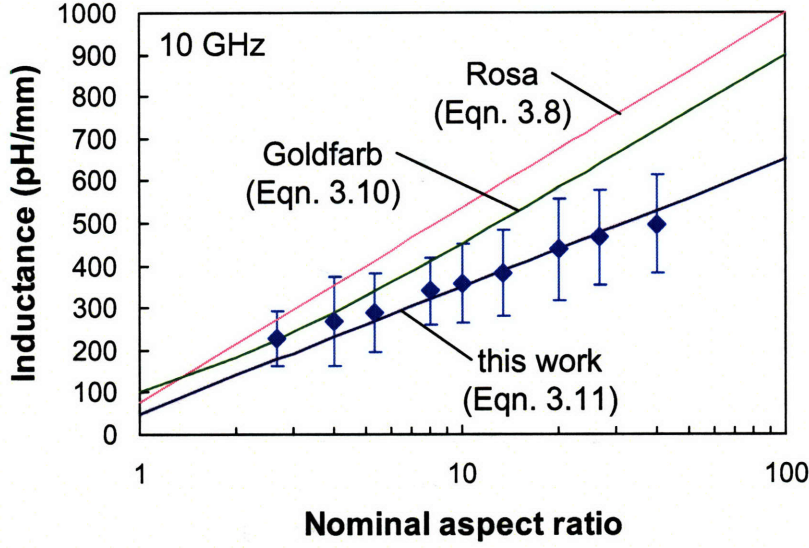


Figure 3-7: Measured via inductance (blue diamonds) plotted with several theoretical models by Rosa (Equation 3.8 [4,5]), Goldfarb *et al.* (Equation 3.10 [6]), and the author (Equation 3.11).

$$L = \frac{\mu_0}{2\pi} \left[ h \cdot \ln \left( \frac{h + \sqrt{h^2 + r^2}}{r} \right) + \frac{3}{2} \left( r - \sqrt{h^2 + r^2} \right) \right] \quad [H] \quad (3.9)$$

They have eliminated the  $h/4$  term and multiplied the second term by an empirical factor of  $3/2$ . When rearranged in terms of aspect ratio, Equation 3.9 becomes:

$$\frac{L}{h} = \frac{\mu_0}{2\pi} \left[ \ln \left( 2a + \sqrt{1 + (2a)^2} \right) + \frac{3}{2} \left( \frac{1 - \sqrt{1 + (2a)^2}}{2a} \right) \right] \quad [H/mm] \quad (3.10)$$

where  $h$  is in mm. This is also plotted in Fig. 3-7. Although less than Rosa (Equation 3.8 [4,5]), Goldfarb *et al.* [6] still overestimate inductance at high-aspect ratios. However, their empirical equation was formulated only for aspect ratios up to 5 [6], while our data reaches aspect ratios of 40. In order to fit our measured inductance data and data from [51], we generated an empirical inductance model modified from Rosa (Equation 3.8):

$$\frac{L_v}{h} = 0.65 \left[ \frac{\mu_0}{2\pi} (\ln 4a - 1) \right] \quad [H/mm] \quad (3.11)$$

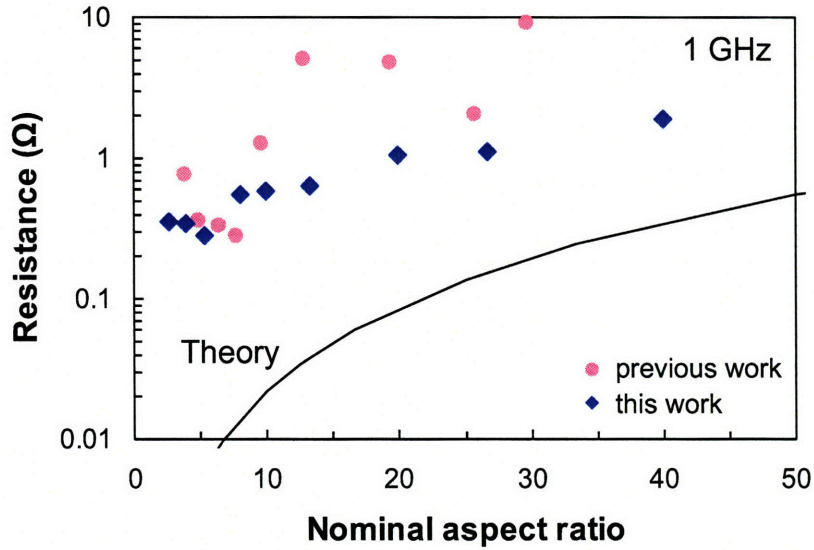


Figure 3-8: Via resistance vs. nominal aspect ratio of a via at 1 GHz. The measured data (blue diamonds) has lower resistance than previous work [3] (pink circles) by using a two-port test structure.

which simply multiplies Equation 3.8 by a factor of 0.65. This model is also plotted in Fig. 3-7 and matches the inductance data well.

### 3.3.3 Resistance

Via resistance was extracted directly from the real part of  $Z_{21}$ . The resistance was taken at 1 GHz to minimize the effects of skin depth, and is plotted in Fig. 3-8 (blue diamonds) against nominal aspect ratio. An average substrate thickness of  $80 \mu\text{m}$  was used to calculate aspect ratio. The resistance is approximately  $1 \Omega$  or less and decreases with via diameter.

The calculation of theoretical resistance of copper vias is straightforward. The resistance of a via for dc current is defined as [77]:

$$R_v = \frac{h}{\sigma A} \quad [\Omega] \quad (3.12)$$

where  $h$  is the height of the via,  $\sigma$  is the conductivity, and  $A$  is the cross-sectional

area of the via. For a 100- $\mu\text{m}$  high via, 10- $\mu\text{m}$  in diameter (aspect ratio of 10), the theoretical resistance is 0.02  $\Omega$ . The theoretical resistance is also plotted in Fig. 3-8 along with data from this work and previous work [3]. The new via measurements showed a significant drop in resistance compared to previous work [3] with less scatter. This is partly due to the better two-port test structure. Using the one-port test structure from my S.M. thesis showed significant sensitivity to where the probes were placed on the signal line. In addition, the new process had improved metallization since the vias were filled from top to bottom and had a better frontside CMP process. The S.M. process had larger process variation due to non-uniform filling of the copper vias from bottom-up filling [8].

### 3.3.4 Sidewall Capacitance

The sidewall capacitance of the via to the substrate was measured using the one-port capacitor test structures in Fig. 3-2 with via arrays of 77 and 431 vias. Fig. 3-9 plots  $|Z_{11}|$  against frequency for each array size.  $|Z_{11}|$  follows a simple model of a capacitor, resistor, and inductor in series, from which we extracted via sidewall capacitance. The impedance is defined as:

$$Z_{11} = R_c + j \left( \frac{\omega^2 L_c C_c + 1}{\omega C_c} \right) \quad (3.13)$$

where  $R_c$  is the total resistance of the via array,  $L_c$  is the total inductance of the via array, and  $C_c$  is the total capacitance of the via array test structure. The resonant frequency is:

$$\omega_0 = \sqrt{\frac{1}{L_c C_c}} \quad (3.14)$$

which occurs at the minimum  $|Z_{11}|$  as seen in Fig. 3-9. At frequencies below the resonant frequency,  $C_c$  dominates so that:

$$|Z_{11}| \simeq \frac{1}{\omega C_c} \quad (3.15)$$

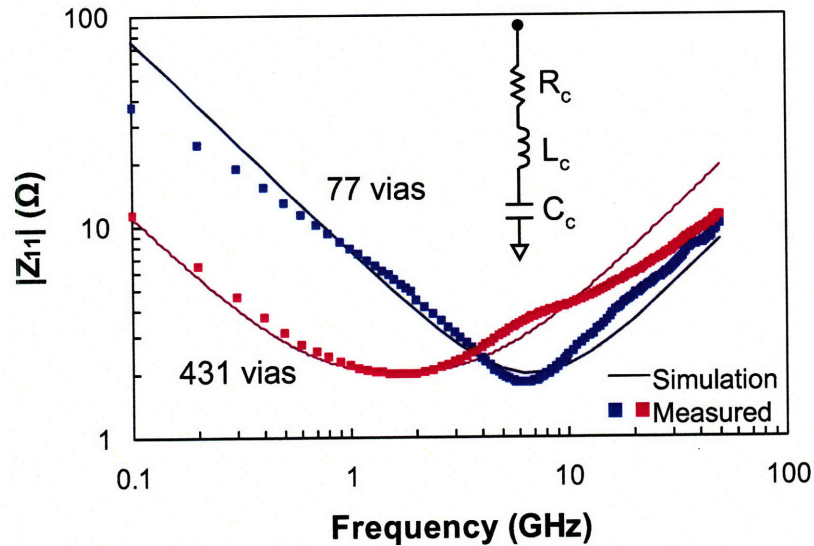


Figure 3-9:  $|Z_{11}|$  vs. frequency for via arrays of 77 and 431 vias, measured using the capacitance test structure in Fig. 3-2. This structure can be represented by a capacitor in series with a resistor and inductor. Simulations of this model are plotted in the solid line for each via array. Via sidewall capacitance was extracted from this model.

and so the sidewall capacitance was extracted at these frequencies. To verify this circuit model, we simulated it with Agilent ADS software using the extracted resistor, capacitor, and inductor values. The simulations closely match the measured data as seen in Fig. 3-9. The mismatch at high frequencies is likely due to the skin effect.

The average extracted capacitance is plotted in Fig. 3-10, and the average extracted inductance is plotted in Fig. 3-11. The inductance of a single via was taken from Fig. 3-6 for via of aspect ratio 10. The capacitance of a single via was taken from separate measurements of the impedance test structure, which will be discussed later. From Fig. 3-10, the extracted capacitance for 77-via and 431-via arrays was 20 pF and 132 pF, respectively. Dividing by the number of vias, capacitance for a single via comes to 0.27 pF and 0.31 pF, respectively. Separately, if we take the slope of the capacitance line in Fig. 3-10, we get a capacitance of 0.31 pF for an individual via. This approaches the theoretical capacitance of 0.33 pF for a 10- $\mu\text{m}$  diameter, 100- $\mu\text{m}$  high via. The theoretical capacitance was calculated from the following formula:

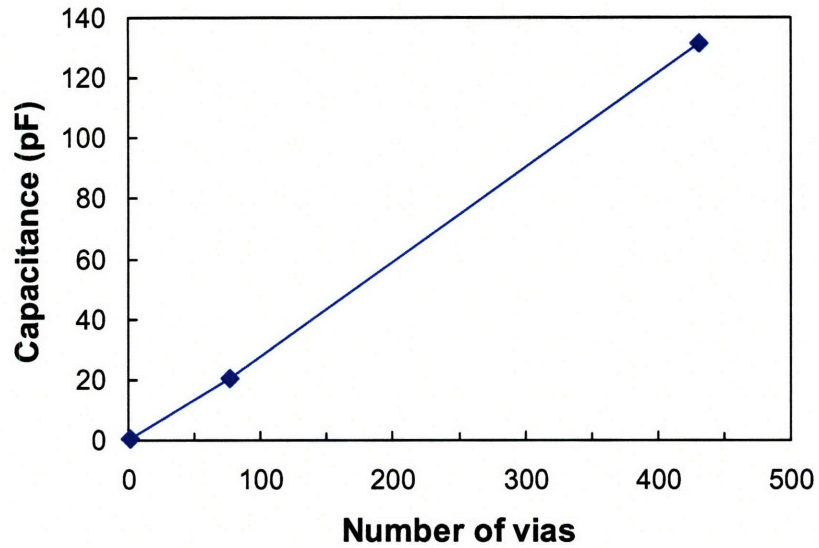


Figure 3-10: Extracted capacitance from measurements of the test structures in Fig. 3-2. Vias are  $10\text{-}\mu\text{m}$  in diameter and  $100\text{-}\mu\text{m}$  high. Capacitance for one via was taken from the slope of the capacitance line.

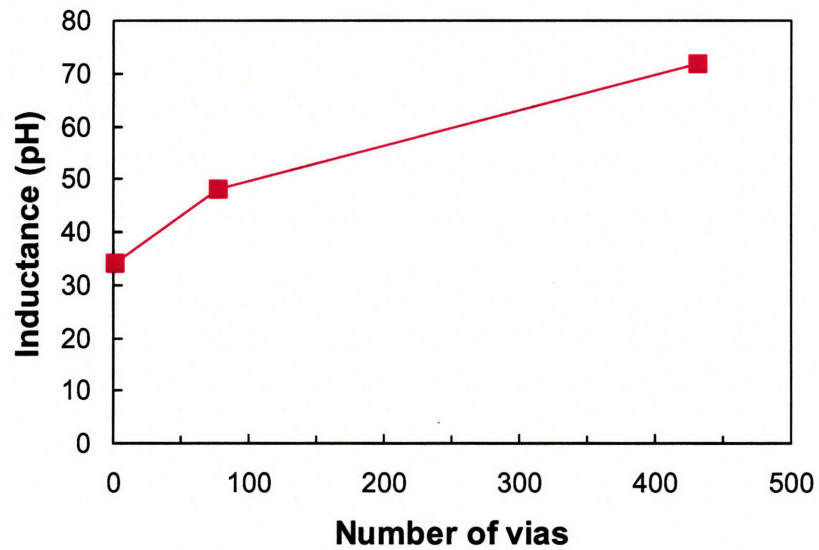


Figure 3-11: Extracted inductance from measurements of the test structures in Fig. 3-2. Vias are  $10\text{-}\mu\text{m}$  in diameter and  $100\text{-}\mu\text{m}$  high. The inductance increases with number of vias due to increasing mutual inductance.

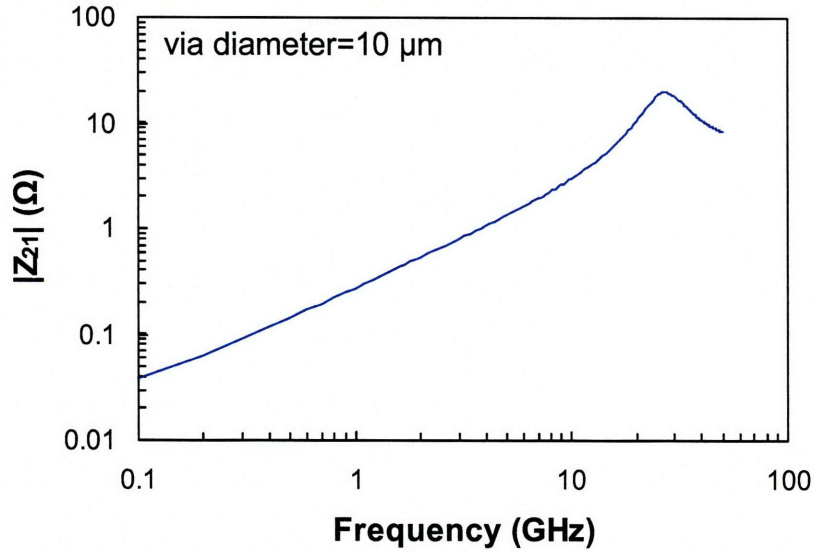


Figure 3-12:  $|Z_{21}|$  vs. frequency of a 10- $\mu\text{m}$  diameter via measured using the two-port impedance test structure in Fig. 3-1 on  $\text{p}^+$  wafers.  $|Z_{21}|$  peaks at the resonant frequency.

$$C_{th} = \frac{\epsilon_0 \epsilon_r (2\pi r h)}{t_{SiN}} \quad [F] \quad (3.16)$$

where  $\epsilon_0$  is the permittivity of free space,  $8.85 \times 10^{-14}$  F/cm,  $\epsilon_r$  is the dielectric constant of silicon nitride, 7.5,  $r$  is the radius of the via cross-section,  $h$  is the height of the via, and  $t_{SiN}$  is the thickness of the silicon nitride liner, 7000 Å.

Sidewall capacitance data was also obtained from  $Z_{21}$  measurements from the two-port impedance test structure in Fig. 3-1 on  $\text{p}^+$  wafers.  $|Z_{21}|$  of a 10- $\mu\text{m}$  diameter via is plotted in Fig. 3-12. The resonant frequency occurs at the peak in  $|Z_{21}|$  and is defined as:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{1}{L_i C_i}} \quad (3.17)$$

where  $L_i$  is the via inductance and was extracted from the imaginary part of  $Z_{21}$  at frequencies below the resonant frequency.  $C_i$  is a composite of the via sidewall capacitance and the parasitic capacitance of the test structure.  $C_i$  was calculated from Equation 3.17 using  $f_0$  and  $L_i$ , and is plotted in Fig. 3-13 (blue diamonds).

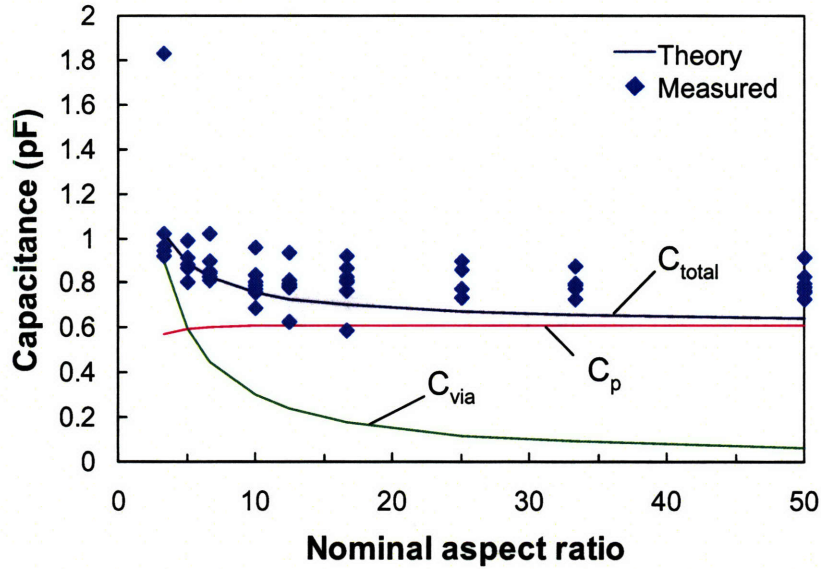


Figure 3-13: Extracted capacitance vs. nominal aspect ratio of measurements of the test structure in Fig. 3-1 on  $p^+$  wafers. Measured capacitance,  $C_i$  is plotted in blue diamonds. Theoretical calculations of the via sidewall capacitance,  $C_{via}$ , and pad capacitance,  $C_p$ , sum to the total capacitance,  $C_{total}$ .

This test structure is actually a distributed network of via inductance and resistance, and via sidewall capacitance and pad capacitance. A simplified network is pictured in Fig. 3-14, from which we can formulate an equation for the total capacitance:

$$C_{total} = \frac{C_{via}}{2} + C_p \quad [F] \quad (3.18)$$

where  $C_{via}$  is the theoretical via sidewall capacitance and  $C_p$  is the signal pad capacitance to the substrate.  $C_{via}$  was calculated using Equation 3.16 and is plotted in Fig. 3-13.  $C_p$  was calculated from the following:

$$C_p = C_T(A_{pad} - A_x) \quad [F] \quad (3.19)$$

where  $A_{pad}$  is the signal pad area, which is  $50 \mu\text{m} \times 200 \mu\text{m}$ ,  $A_x$  is the cross-sectional

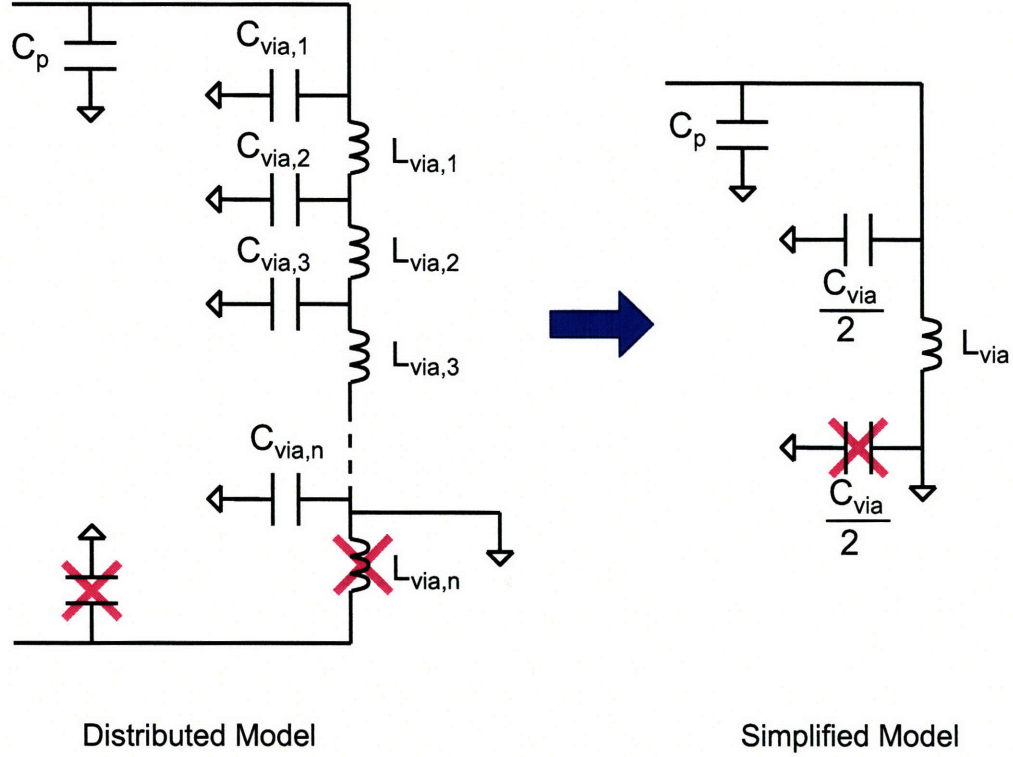


Figure 3-14: Distributed network of the impedance test structure when measuring capacitance.

area of the via under test, and  $C_T$  is defined as follows:

$$\frac{1}{C_T} = \frac{1}{C_{SiN}} + \frac{1}{C_{oxide}} \quad (3.20)$$

$$C_{SiN} = \frac{7.5\epsilon_0}{t_{SiN}} \quad [F/cm^2] \quad (3.21)$$

$$C_{oxide} = \frac{3.9\epsilon_0}{t_{oxide}} \quad [F/cm^2] \quad (3.22)$$

where  $t_{SiN}$  is 7000 Å and  $t_{oxide}$  is 2000 Å. From these equations,  $C_T = 6.12 \times 10^{-9}$  F/cm<sup>2</sup>, and  $C_p$  and  $C_{total}$  are plotted in Fig. 3-13. Looking at Fig. 3-13, the pad capacitance overwhelms the sidewall capacitance except at small aspect ratios.  $C_{total}$  falls on the measured  $C_i$  data, providing some confirmation that the sidewall capacitance is close to theoretical values. The measured value of  $C_i$  at aspect ratio 10 was used as the single via point in Fig. 3-10.

Nearly perfect scaling of capacitance with the number of vias is seen in Fig. 3-10. Using vias with a 1:1 pitch for high-density integrated capacitors, the expected capacitance per footprint area is about  $0.1 \mu\text{F}/\text{cm}^2$ , which is similar to standard thin-film capacitors. By increasing the aspect ratio to our processing limit of 50,  $0.4 \mu\text{F}/\text{cm}^2$  can be reached. By decreasing the silicon nitride thickness from 700 to 100 nm, an even greater capacitance of  $2.7 \mu\text{F}/\text{cm}^2$  is attainable. A higher capacitance density will require a dielectric with a higher dielectric constant. This is promising for via applications such as decoupling capacitors and integrated capacitors.

### 3.3.5 Mutual Inductance

Through-substrate vias in the large via arrays in the capacitance test structure (Fig. 3-2) are connected in parallel. If a single via is represented by a circuit model of a resistor and an inductor in series, both the resistance and inductance should drop with larger via arrays. However, the total inductance actually increases with more vias as seen in the inductance data of Fig. 3-11. This is due to mutual inductance. (The resistance changes little because it is swamped by the test structure parasitic resistance.) With more vias in parallel, the self-inductance decreases, but the mutual inductance increases faster, so that the total inductance goes up. This is an important consideration when using these vias in high-frequency circuits.

## 3.4 Liner Integrity

We tested the integrity of the LPCVD silicon nitride liner by measuring the current leakage across the dielectric liner using the test structures in Fig. 3-3 and Fig. 3-2 on  $p^+$  wafers. Fig. 3-15 plots the measured current across the liner of four vias in parallel (Fig. 3-3) against an applied voltage of -1 to 1 V. The leakage was measured from the copper via to the silicon substrate for via diameters 2 to  $10 \mu\text{m}$ . For the test structure with four vias in parallel, the current leakage was in the sub-pA range for all structures on this die and lies within the same current range as the open test structure. These currents are below the noise floor of the measurement setup. Other

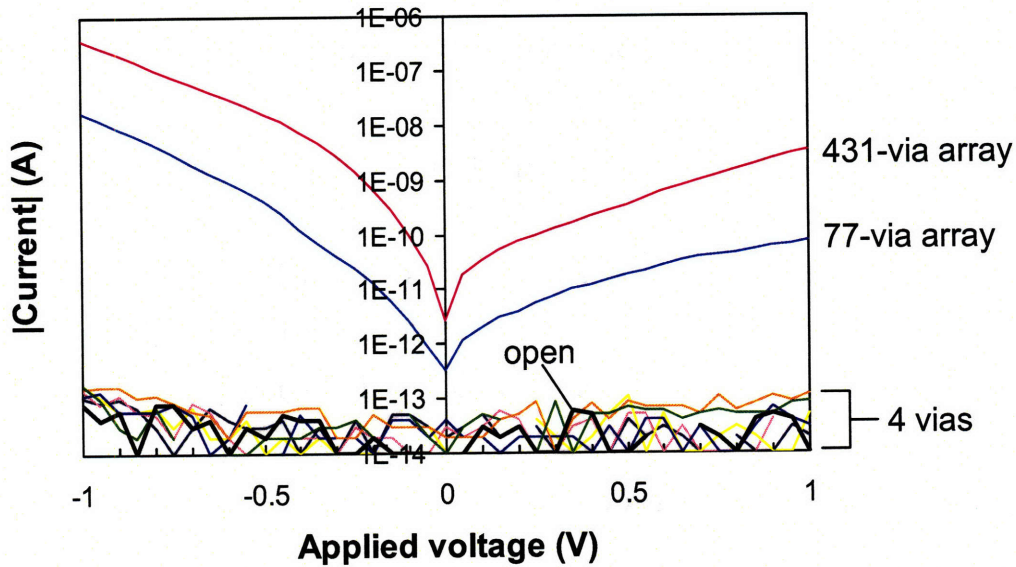


Figure 3-15: Current leakage vs. applied voltage across four vias in parallel for different via diameters (2–10  $\mu\text{m}$ ), and for 77-via and 431-via arrays. The via diameter is 10  $\mu\text{m}$  for the via arrays. The leakage for the open test structure is indicated by the thick black line.

die showed similar results. However, measurements of the larger via arrays in Fig. 3-2 showed that some vias were actually shorted to the substrate. Via arrays that were not shorted had current leakage less than 1  $\mu\text{A}$  for the 431-via array and sub-pA to 100 nA range for the 77-via array. Fig. 3-15 shows measurements of each size via array that was not shorted.

It is not entirely clear if the shorts were due to defects in the liner in the via sidewall or at the top surface. It is likely that during the nitride etch step, the photoresist was thinner around the edges of the via in the via arrays due to uneven coating over the vias. The unprotected silicon nitride was etched, revealing the silicon substrate. Also, the nitride was already thinner at this point due to the CMP.

### 3.5 Summary

*S* parameter measurements to characterize the through-substrate vias show that the copper via can be represented by a simple equivalent circuit of a resistor and inductor in series, from which via resistance and inductance were extracted. The resistance was less than  $1\ \Omega$  and decreased with via diameter. The via inductance was the lowest ever reported for vias of aspect ratio greater than 4. Using via arrays, via sidewall capacitance was also extracted to be 0.31 pF of a single via with  $10\text{-}\mu\text{m}$  diameter and  $100\text{-}\mu\text{m}$  high. We also tested the integrity of the silicon nitride liner with current leakage measurements. Fully characterizing the through-substrate vias provides the basis for vias to be incorporated in circuits and other applications.



## Chapter 4

# Faraday Cages for Substrate Noise Isolation

One of the possible applications of high-aspect ratio, through-substrate vias is subsystem isolation in mixed-signal circuits. Through-substrate vias for substrate noise isolation was explored in my S.M. thesis as a proof-of-concept study with remarkable results. In order to better understand their performance, we fabricated Faraday cages with the new process in various configurations, measured their performance, and compared the measurements to simulations of a lumped-element circuit model.

### 4.1 Motivation

Suppression of substrate crosstalk is critical to enable one-chip systems that integrate noisy logic with sensitive analog and low-noise RF circuits, commonly referred to as System-on-Chip (SoC). Designers of mixed-signal and RF circuits have raised concern about the problem of substrate crosstalk between sensitive RF and analog circuits and noisy digital blocks. Digital blocks inject noise into the common substrate during each switching transient, and the noise propagates through the substrate to disrupt the operation of analog and RF circuits because they lack the noise margins of digital logic. Furthermore, future systems will require densely-packed circuits operating at high frequency, which will only exacerbate the problem.

Substrate noise isolation requirements for integrating a microprocessor with a low-noise amplifier (LNA) for various wireless standards were derived in [78]. A Signal-to-substrate Noise Ratio (SsNR) of at least 20 dB is required to guarantee a bit-error rate (BER) less than  $10^{-9}$  [79]. For Bluetooth, this translates to an isolation requirement of  $-22.8$  dB at 2.4 GHz and  $-20.3$  dB at 5.2 GHz, which can be mitigated by standard isolation techniques [78]. For 802.11b, the isolation requirement increases to  $-28.8$  dB at 2.4 GHz and  $-26.3$  dB at 5.2 GHz, and can be achieved through creative design of standard techniques but at the cost of die area [78]. Cellular/PCS systems are even more stringent and require at least  $-75$  dB of isolation at 900 MHz and  $-74$  dB at 1.9 GHz [78]. Standard techniques will not be enough to satisfy these requirements and unorthodox strategies will be needed. Next-generation systems, such as 3G, will have even stricter requirements and operate at frequencies reaching into the mm-wave regime (30 GHz and greater). For example, IEEE 802.16 WirelessMAN<sup>TM</sup> will operate from 10–66 GHz [15] and automotive collision avoidance radar operates at 76–77 GHz [13, 14].

These concerns have motivated substantial work on substrate noise isolation techniques, which will be summarized in the next section.

## 4.2 Review of Substrate Noise Isolation Techniques

Substrate noise can be reduced by blocking or filtering the noise before it interferes with sensitive devices. While some circuit designers have proposed to actively filter or cancel noise injected into the substrate using circuits or active guard rings [80–83], most techniques to reduce substrate noise have concentrated on engineering the actual substrate.

Traditional approaches to reduce substrate crosstalk include guard rings [22, 84–94], silicon-on-insulator (SOI) substrates [85, 95–101], high-resistivity substrates [102–105], junction-isolated wells [79, 85, 90, 96], and combinations of these. Slightly more exotic are proton bombardment [106] and deep trenches [107]. These methods are attractive because they are less invasive and require little modification to existing sil-

icon fabrication technology. The drawback of using SOI or high-resistivity substrates is they cease to work at high frequencies when the substrate becomes capacitive. Guard rings are not deep enough to shunt noise that travels deeper in the substrate. Junction-isolated wells and deep n-wells have shown the best results of these techniques.

However, unconventional techniques have achieved better crosstalk suppression, such as porous silicon [108,109], metal-filled through-wafer trenches [41,110] and air trenches [111], SOI on metal with a Faraday cage [112], and even total substrate transfer [113]. A comparison between different crosstalk isolation schemes is difficult due to different reference structures and test structure designs. A key consideration when evaluating crosstalk isolation schemes is the footprint of the isolation structure. For example, [22] uses a 300- $\mu\text{m}$  wide p-type wall to shield the Bluetooth radio from digital blocks, and in [41] and [108], the trench is 60- $\mu\text{m}$  and 100- $\mu\text{m}$  wide, respectively. Also, non-standard fabrication processes can affect device operation, such as the buried metal ground that lies under the buried oxide of SOI in [112].

While all of these isolation techniques have their advantages and disadvantages, we have proposed a novel isolation scheme that combines exceptional crosstalk suppression into the mm-wave regime with a small footprint. We have exploited the high-aspect ratio of through-substrate vias to demonstrate a Faraday cage that suppresses substrate crosstalk [3,8,114]. The Faraday cage consists of a ring of substrate vias shorted to a copper backplane on the backside of the substrate and grounded through a ring of metal on the frontside (Fig. 4-1). This Faraday cage isolation structure can provide the substrate noise suppression needed for next-generation RF and mm-wave systems.

### 4.3 Test Structure Design and Measurement

The test structures used to measure substrate noise with and without the Faraday cage are similar to those in my S.M. thesis [8]. The new test structures are pictured in Fig. 4-2. The pad dimensions are slightly different and the ground pads are now

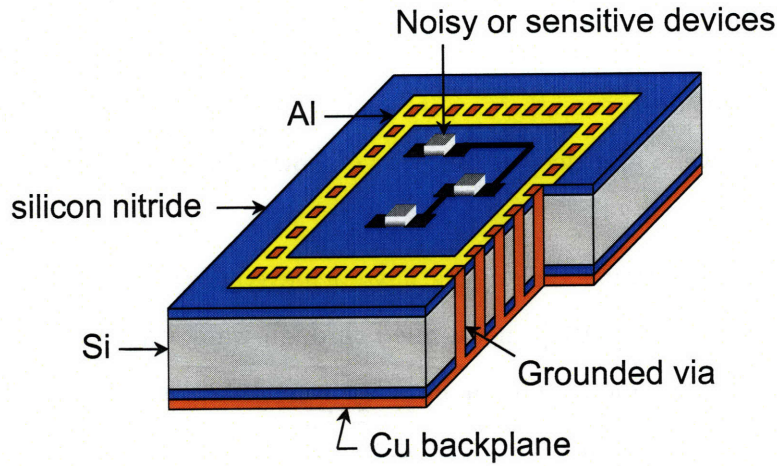
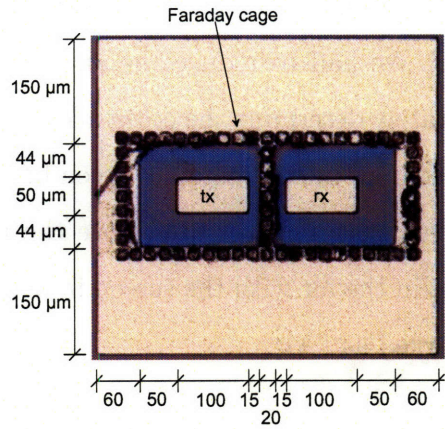


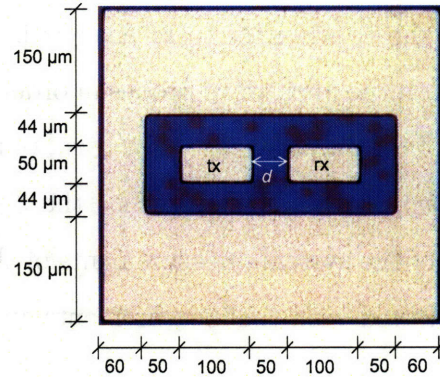
Figure 4-1: Illustration of the Faraday cage isolation structure using through-substrate vias.

connected to each other through aluminum on the surface. The test structure is a two-port, RF, coplanar ground-signal-ground configuration. The signal pads are the transmitter (tx) and receiver (rx), each  $50 \mu\text{m} \times 100 \mu\text{m}$ . The tops of the vias of the Faraday cage are connected to the ground pads, and at the bottom they are connected to each other through a copper plate lining the backside DRIE trench. This copper backplane is grounded through the via connections and is isolated from other test structures and the wafer chuck. The backside DRIE trench dimensions extend to the edge of the frontside aluminum ground pads.

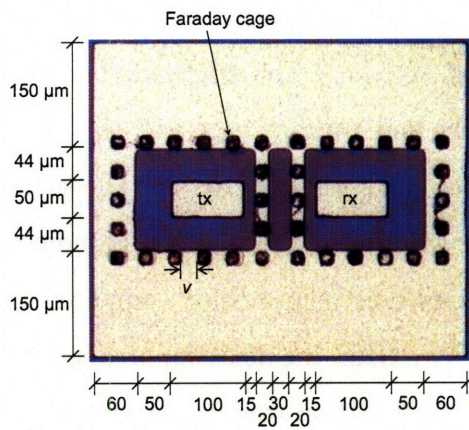
The Faraday cage has two arrangements: (type I) where a single Faraday cage is placed between the transmitter and receiver as in Fig. 4-2a, and (type II) where the transmitter and receiver pads each are surrounded by a Faraday cage as in Fig. 4-2c. To vary the via density of the Faraday cage, the separation,  $v$ , between the vias of the Faraday cage varies from  $10 \mu\text{m}$  to  $70 \mu\text{m}$ . The distance,  $d$ , between transmitter and receiver varies from  $50 \mu\text{m}$  to  $400 \mu\text{m}$ . The reference structure pictured in Fig. 4-2b has aluminum pads and no Faraday cage, but still has the copper backplane, so that the structure of the reference is exactly the same as the cage test structure minus the Faraday cage vias. The test structure pictured in Fig. 4-2d was measured to observe



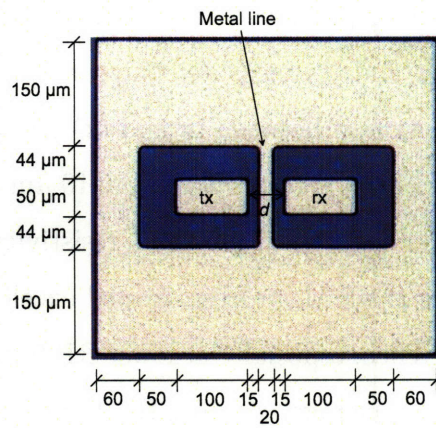
(a) Picture and dimensions of the type I Faraday cage test structure at a  $50\text{-}\mu\text{m}$  separation between transmitter and receiver. Vias are  $10\text{ }\mu\text{m}$  in diameter and spaced by  $10\text{ }\mu\text{m}$ .



(b) Picture and dimensions of the reference test structure at a transmission distance,  $d$ , of  $50\text{ }\mu\text{m}$ .



(c) Picture and dimensions of the type II Faraday cage test structure at a  $100\text{-}\mu\text{m}$  separation between transmitter and receiver. Vias are  $10\text{ }\mu\text{m}$  in diameter and spaced by  $30\text{ }\mu\text{m}$ .



(d) Picture and dimensions of a test structure with a  $20\text{-}\mu\text{m}$  wide metal line between transmitter and receiver.  $d = 50\text{ }\mu\text{m}$ .

Figure 4-2: Two-port, coplanar ground-signal-ground, RF test structure used to measure the substrate noise. Vias in the Faraday cage are  $10\text{ }\mu\text{m}$  in diameter. The back-side DRIE trench has the same outer dimensions as the aluminum ground pads for all test structures.

the effect of the metal line without the Faraday cage on substrate noise suppression.

We measured  $S_{21}$  up to 50 GHz using the same measurement setup as the impedance measurements described in Section 3.2. The figure-of-merit to evaluate substrate noise from the transmitter to receiver is  $|S_{21}|$  in dB. We had to reduce the air crosstalk between the microwave probes in order to accurately determine the crosstalk suppression of the Faraday cage. For this, we introduced a grounded metallic screen between the two probes. To show that the  $S$  parameter measurements are above the noise floor of the system, measurements of the probes in the air with the screen in between are plotted with the measurements and are marked as “Air”.

## 4.4 Measurement Results and Discussion

### 4.4.1 Measurements of Previous Work

We have previously demonstrated a Faraday cage noise isolation structure [3, 8, 114, 115], and its measurements are shown in Fig. 4-3 [3]. The transmission distance (separation between tx and rx) for the reference and Faraday cage was 100- $\mu\text{m}$ . The vias of the Faraday cage were 10  $\mu\text{m}$  in diameter and spaced by 10  $\mu\text{m}$ . The substrate thickness was 77  $\mu\text{m}$  and resistivity was p-type, 10–20  $\Omega\cdot\text{cm}$ . The Faraday cage from the S.M. process showed excellent substrate noise suppression compared to the reference, especially at lower RF frequencies. At 1 GHz, the noise suppression was 43 dB on average. At 10 GHz, the suppression was 30 dB on average. And at 50 GHz, the suppression was 16 dB on average [3].

### 4.4.2 Faraday Cage Measurement Results

Measurements on test structures using our new via process are plotted in Fig. 4-4 of a p-type wafer and Fig. 4-5 of an n-type wafer. Both types show similar features in their measurements, confirming that wafer type is not significant for substrate noise. These figures plot  $|S_{21}|$  of a reference and several Faraday cages of different via densities at a distance of 100  $\mu\text{m}$ . For the type I Faraday cage (Figs. 4-4a and 4-5),

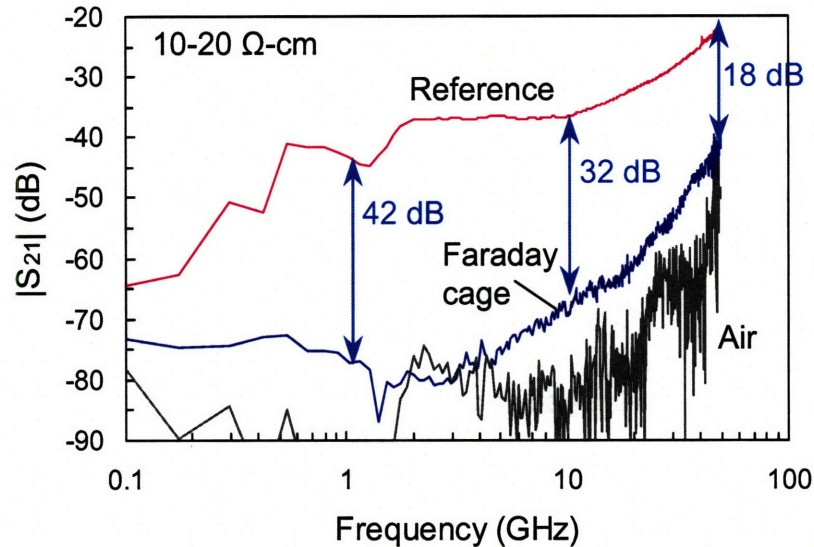
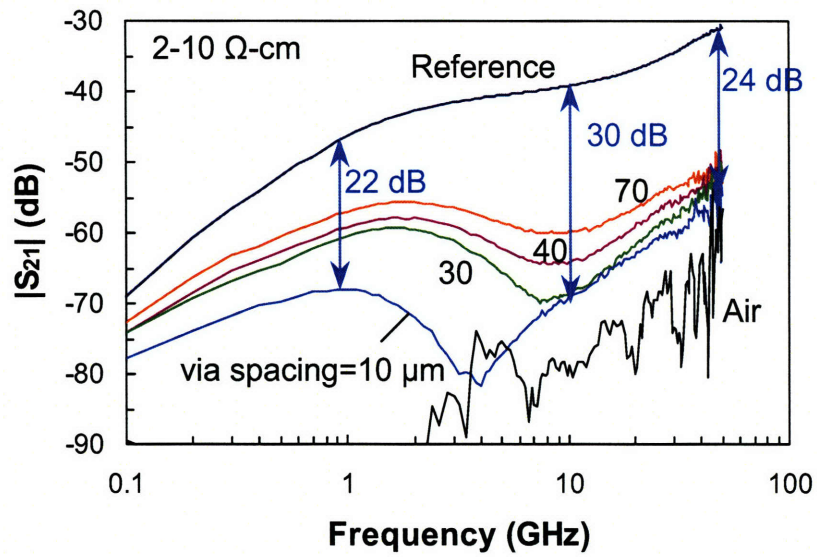


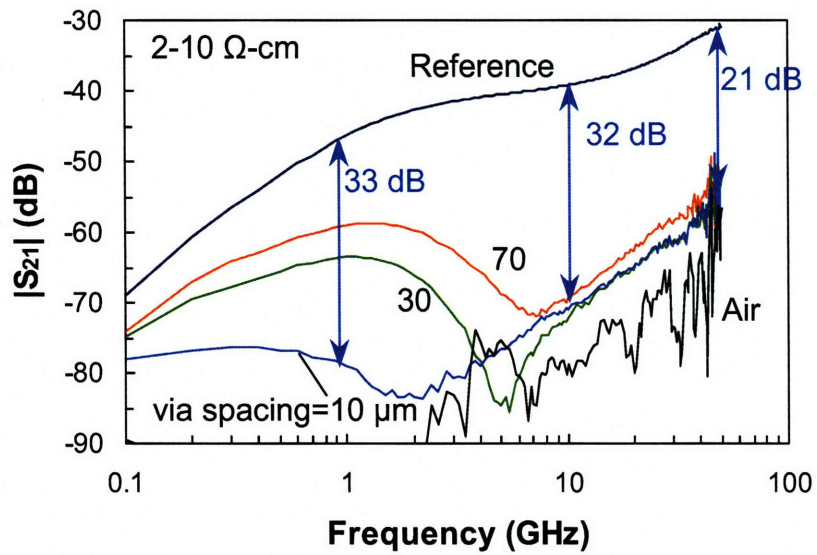
Figure 4-3:  $|S_{21}|$  vs. frequency at a transmission distance of  $100\ \mu\text{m}$  from previous work [3]. The vias of the Faraday cage are  $10\ \mu\text{m}$  in diameter and spaced by  $10\ \mu\text{m}$ . The substrate thickness is  $77\ \mu\text{m}$  and resistivity is p-type,  $10\text{--}20\ \Omega\text{-cm}$ .

the cage shows exceptional isolation especially at high frequencies (31 dB at 10 GHz, average, compared to the reference) and into the mm-wave regime (21 dB at 50 GHz, average, compared to the reference). At 10 GHz, this is comparable to the isolation of [3], but at 50 GHz the new Faraday cage performs better by 5 dB on average. This is likely due to the reduced resistance of the substrate vias using the new process. Using the type II Faraday cage configuration provides even better noise suppression because each transmitter pad and receiver pad is surrounded by its own Faraday cage (Fig. 4-4b). At 10 GHz, the noise suppression is 32 dB better than the reference, and at 50 GHz, 26 dB better than the reference on average. Although the Faraday cages still perform well at low frequencies, compared to high frequencies the performance suffers. At 1 GHz, the type I Faraday cage is 15 dB better than the reference, and the type II cage is 22 dB better. The broad peak in substrate crosstalk at low frequencies was not observed in [3, 115] and will be examined in Section 4.6.1.

At low to mid-frequencies, decreasing via spacing (or increasing via density) improves Faraday cage isolation. However, at high frequencies, the impact of via density



(a)  $|S_{21}|$  vs. frequency for different via spacing of the type I Faraday cage.



(b)  $|S_{21}|$  vs. frequency for different via spacing of the type II Faraday cage.

Figure 4-4:  $|S_{21}|$  measurements of Faraday cages and a reference at a transmission distance of  $100\ \mu\text{m}$ . The substrate resistivity is p-type, 2-10  $\Omega\cdot\text{cm}$ .

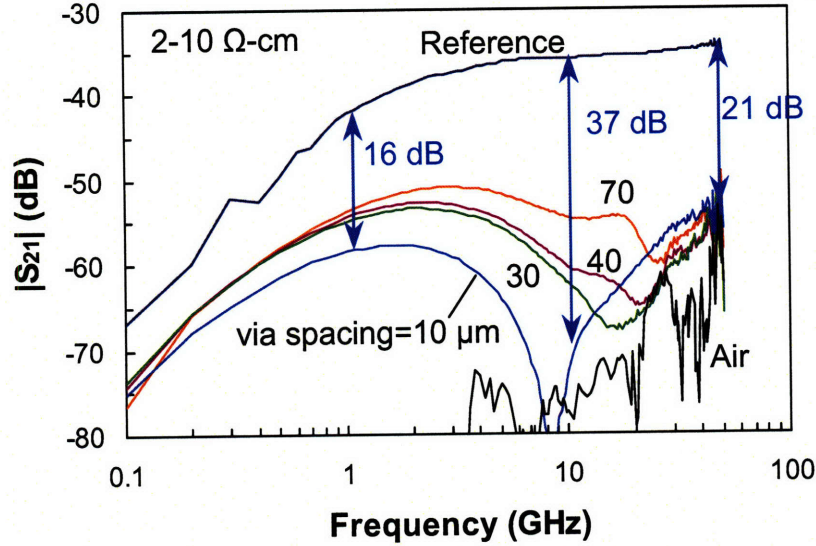


Figure 4-5:  $|S_{21}|$  vs. frequency at a transmission distance of  $100 \mu\text{m}$  for different via spacing of a type I Faraday cage. The substrate resistivity is n-type,  $2\text{--}10 \Omega\cdot\text{cm}$ .

diminishes. This observation will be discussed in Section 4.6.

### 4.4.3 Reference Measurement Results

Looking at the reference measurements in Figs. 4-3, 4-4, and 4-5 provides insight into substrate noise propagation.  $|S_{21}|$  first rises with frequency, plateaus, and then starts to rise again as frequency increases. The first rise in  $|S_{21}|$  is due to capacitive coupling between the pad and the substrate [116]. Then  $|S_{21}|$  flattens out at low to mid-frequencies. Because the silicon substrate is semi-conducting, it shares characteristics of a conductor and insulator. At these frequencies, the substrate acts as a resistor, and so  $|S_{21}|$  is unaffected by frequency. At higher frequencies, the substrate capacitance dominates, which causes  $|S_{21}|$  to rise again [78, 116]. This transition frequency corresponds to the dielectric relaxation time constant of the substrate, and is defined as:

$$\tau_d = \frac{\epsilon_0 \epsilon_r}{\sigma} = \epsilon_0 \epsilon_r \rho \quad (4.1)$$

where  $\epsilon_r$  is the dielectric constant of silicon, 11.9,  $\sigma$  is the conductivity, and  $\rho$  is the resistivity of the substrate. The corresponding frequency is then:

$$f_d = \frac{1}{2\pi\tau_d} = \frac{1}{2\pi\epsilon_0\epsilon_r\rho} \quad (4.2)$$

The dielectric relaxation transition frequency for wafers of resistivity 1  $\Omega\cdot\text{cm}$  is 152 GHz, and for 10  $\Omega\cdot\text{cm}$ , 15 GHz. Higher-resistivity substrates provide better substrate crosstalk isolation at frequencies when the substrate is resistive, but at high-frequencies when the substrate becomes capacitive, the effect of resistivity converges [90, 116]. At these high frequencies, the reduction in substrate noise by the Faraday cage can prove most effective.

#### 4.4.4 Transmission Distance

The effect of transmission distance,  $d$ , on substrate crosstalk for the reference test structure is plotted in Fig. 4-6. Because of the high resistivity of the substrate, the substrate does not act as a single node, so increasing the separation distance reduces substrate crosstalk. The Faraday cage test structure also shows this dependence in Fig. 4-7. To observe the effect of just a metal line on substrate crosstalk, an additional test structure with a grounded, 20- $\mu\text{m}$  wide aluminum strip between transmitter and receiver pictured in Fig. 4-2d was also fabricated. Its measurements are plotted in Fig. 4-8 along with the open reference. The metal line suppresses substrate noise by a few dB compared to the open reference structure at close distances, 50–100  $\mu\text{m}$ . However, at greater distances, its effect diminishes and becomes negligible by 400  $\mu\text{m}$ .

#### 4.4.5 Faraday Cage Type

The two types of Faraday cages behave differently at increasing transmission distances. Fig. 4-9 plots both cage types at transmission distances of 100 and 400  $\mu\text{m}$ . At 100  $\mu\text{m}$ , the type II cage performs better, which is logical since a double cage would suppress more noise than a single cage. However, at a farther distance of 400  $\mu\text{m}$ , the type II cage is actually worse than type I. Looking at the layout drawing

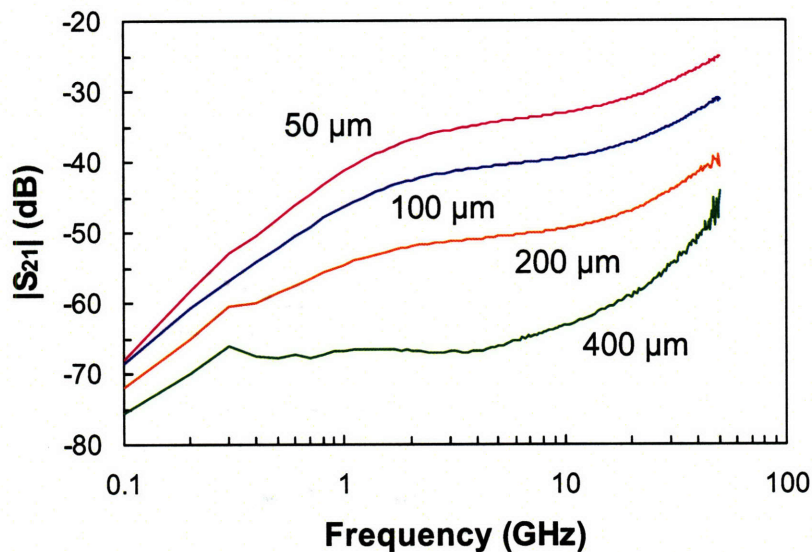


Figure 4-6:  $|S_{21}|$  vs. frequency of the reference test structure at varying transmission distances between 50 and 400  $\mu\text{m}$ . Substrate resistivity is 2–10  $\Omega\cdot\text{cm}$ .

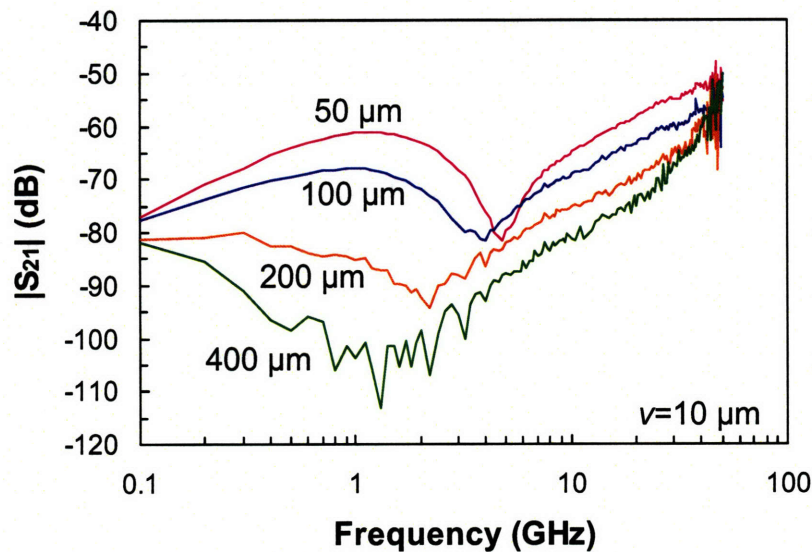


Figure 4-7:  $|S_{21}|$  vs. frequency of the type I Faraday cage at varying transmission distances between 50 and 400  $\mu\text{m}$ . The vias of the Faraday cage are 10  $\mu\text{m}$  in diameter and separated by 10- $\mu\text{m}$ . Substrate resistivity is 2–10  $\Omega\cdot\text{cm}$ .

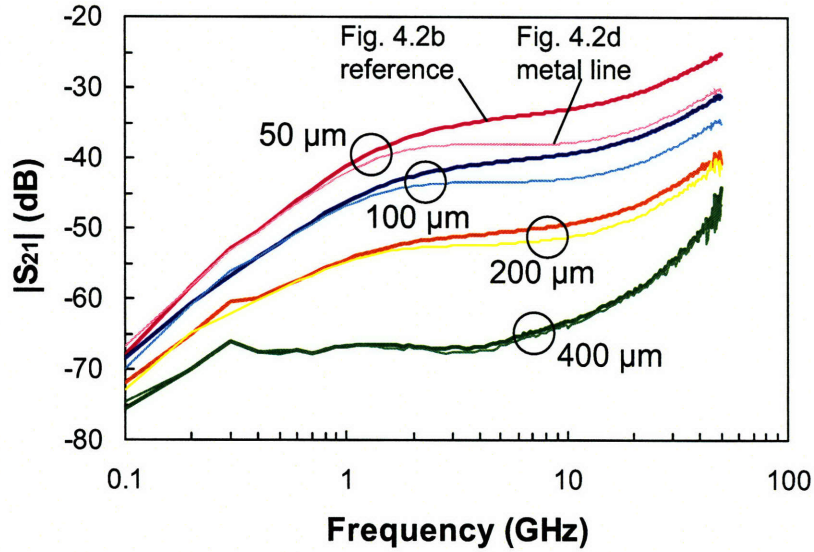


Figure 4-8:  $|S_{21}|$  vs. frequency of the reference test structure (Fig. 4-2b, thick lines) and test structure with a metal line (Fig. 4-2d, light-colored lines) at varying transmission distances between 50 and 400  $\mu\text{m}$ . Substrate resistivity is 2–10  $\Omega\cdot\text{cm}$ .

of the type I cage test structure at 400  $\mu\text{m}$  in Fig. 4-10a, the Faraday cage is in the center of the structure with vias surrounding the entire substrate between the pads. The distance to the center line is farther than to vias to either side, so as the signal propagates through the substrate, it is attenuated by not only the substrate but also the grounded sideline vias. In contrast, the type II cage shown in Fig. 4-10b has Faraday cages closely surrounding both pads but no sideline vias in between the pads. Therefore, once the signal passes through the first Faraday cage, the signal is only attenuated by the substrate. Table 4.1 lists average values of substrate noise suppression for both Faraday cage types at via spacing of 10 and 30  $\mu\text{m}$  for distances of 100 and 400  $\mu\text{m}$ . The reference  $|S_{21}|$  values have been subtracted from these values.

## 4.5 Lumped-Element, Equivalent Circuit Model

The substrate noise isolation measurements showed excellent substrate crosstalk suppression into the mm-wave regime. To better understand the performance of the

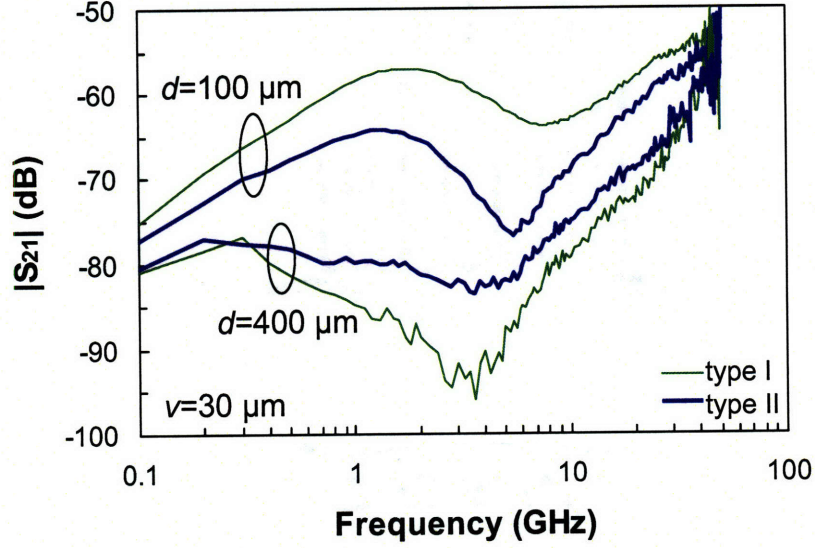
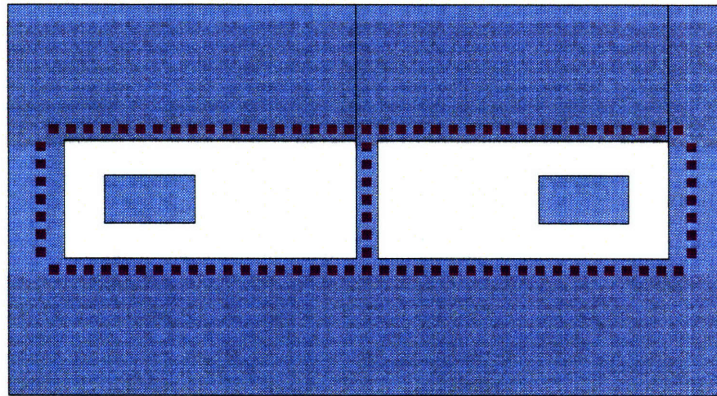


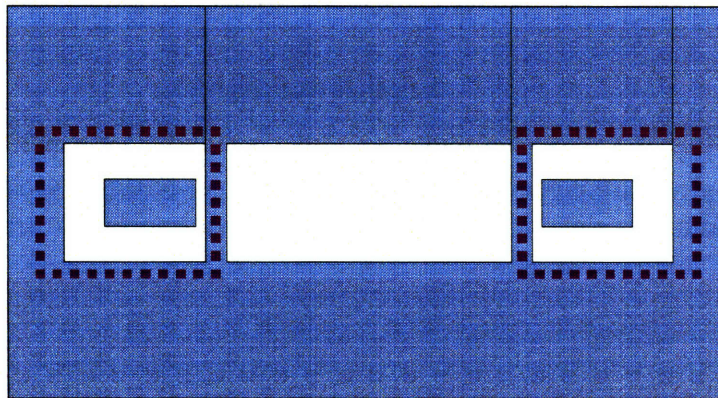
Figure 4-9:  $|S_{21}|$  vs. frequency of the both Faraday cage types at transmission distances of 100 and 400  $\mu\text{m}$ . Via spacing is 30  $\mu\text{m}$  and substrate resistivity is 2–10  $\Omega\cdot\text{cm}$ .

Table 4.1: Average substrate noise suppression for type I and II Faraday cages with the reference subtracted, for via spacing,  $v$ , of 10 and 30  $\mu\text{m}$  and transmission distance,  $d$ , of 100  $\mu\text{m}$  and 400  $\mu\text{m}$ .

	$v = 10 \mu\text{m}$		$v = 30 \mu\text{m}$	
	type I	type II	type I	type II
$d = 100 \mu\text{m}$				
1 GHz	15 dB	22 dB	11 dB	13 dB
10 GHz	31 dB	32 dB	20 dB	27 dB
50 GHz	21 dB	26 dB	21 dB	24 dB
$d = 400 \mu\text{m}$				
1 GHz	39 dB	31 dB	29 dB	18 dB
10 GHz	34 dB	26 dB	27 dB	17 dB
50 GHz	15 dB	13 dB	14 dB	13 dB



(a) Layout drawing of a type I Faraday cage.



(b) Layout drawing of a type II Faraday cage.

Figure 4-10: Layout drawings of type I and II Faraday cage test structures at a transmission distance of  $400\ \mu\text{m}$ . The backside DRIE trench has the same outer dimensions as the frontside aluminum ground pads.

Faraday cage, we developed a lumped-element circuit model and simulated the circuit to match measurements. From the simulations, we gained insight into the noise suppression mechanisms of the Faraday cage.

#### 4.5.1 Reference Equivalent Circuit Model

The equivalent circuit model of the Faraday cage isolation structure was constructed by first examining the reference test structure. As explained in Section 4.4.3, at

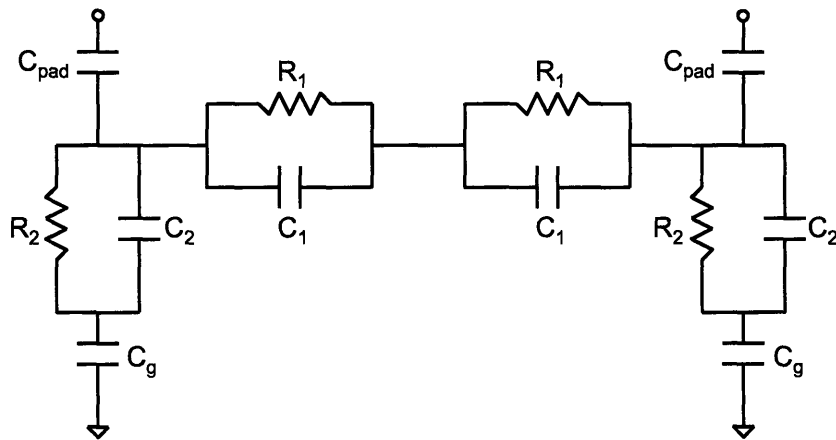
frequencies below that corresponding to its dielectric relaxation time constant, the silicon substrate behaves as a simple resistor. But at higher frequencies, the substrate begins to act as a lossy dielectric. This demands a parallel resistor-capacitor combination [88,98,99,117]. A suitable model for the reference structure is therefore one that is similar to the SOI model in [98] and the high-resistivity substrate model in [99]. The resulting circuit model is depicted in Fig. 4-11a.  $R_1$  and  $C_1$  represent the substrate between the transmitter and receiver, and the central node is the substrate halfway between transmitter and receiver. The split in the substrate is needed for the Faraday cage model, which will be discussed in the next section.  $R_2$  and  $C_2$  are lumped to represent the substrate underneath the signal pads to the ground pads.  $C_g$  is the capacitance from the substrate to ground pads.  $C_{pad}$  is the pad-to-substrate capacitance. The copper backplane for the reference structure is floating since there is no connection to the backplane without substrate vias present.

### 4.5.2 Faraday Cage Equivalent Circuit Model

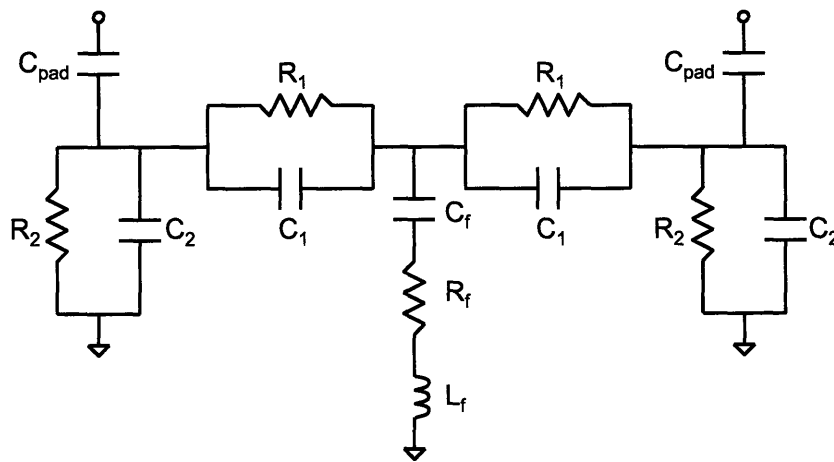
We next developed a lumped-element, equivalent circuit model to approximate the Faraday cage test structure and is depicted in Fig. 4-11b. The Faraday cage model extends from the reference model by adding the ground shunt provided by the vias. From the central node, the *RLC* shunt to ground represents the vias of the Faraday cage. Due to the excellent integrity of the silicon nitride liner, the Faraday cage sidewall capacitance,  $C_f$ , needed to be introduced in this shunt.  $C_f$  connects the silicon substrate to the metal via, which is represented by the via model of a resistor,  $R_f$ , and inductor,  $L_f$ , in series.  $C_g$  is eliminated in the Faraday cage model because the copper backplane is connected to ground through the vias so that  $C_g$  is essentially infinite.

### 4.5.3 Comparison to Previous Circuit Models

These models differ from those developed for the S.M. process [7]. (The Faraday cage circuit model for the S.M. process is depicted in Fig. 4-12 [7].) Unlike the S.M.



(a) Equivalent circuit for the reference test structure. The capacitance,  $C_g$ , represents the capacitance from the substrate to the ground pads. The center node is the substrate halfway between transmitter and receiver.



(b) Equivalent circuit for the Faraday cage test structure. The center  $RLC$  shunt to ground represents the vias of the Faraday cage.

Figure 4-11: Lumped-element, equivalent circuit models of the reference and Faraday cage test structures.

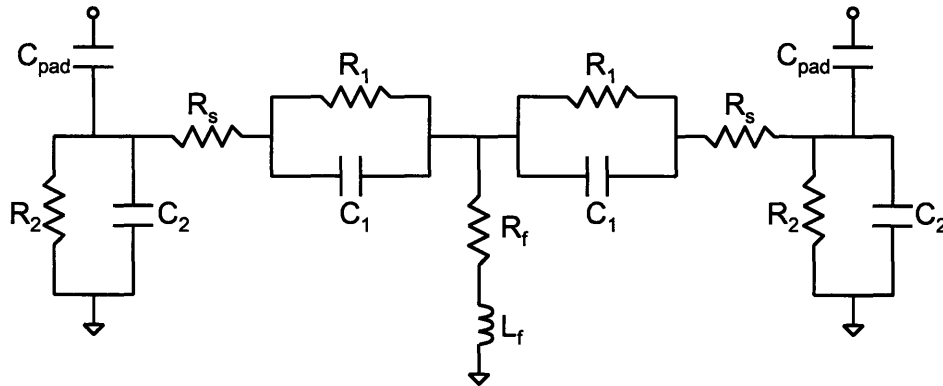
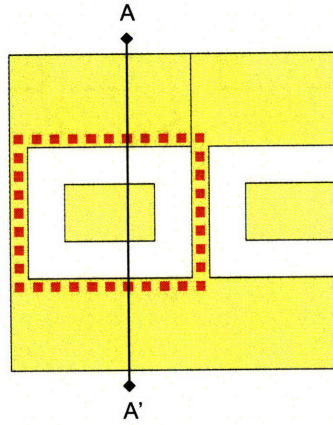


Figure 4-12: Equivalent circuit model of the Faraday cage test structure fabricated with the S.M. process [7].

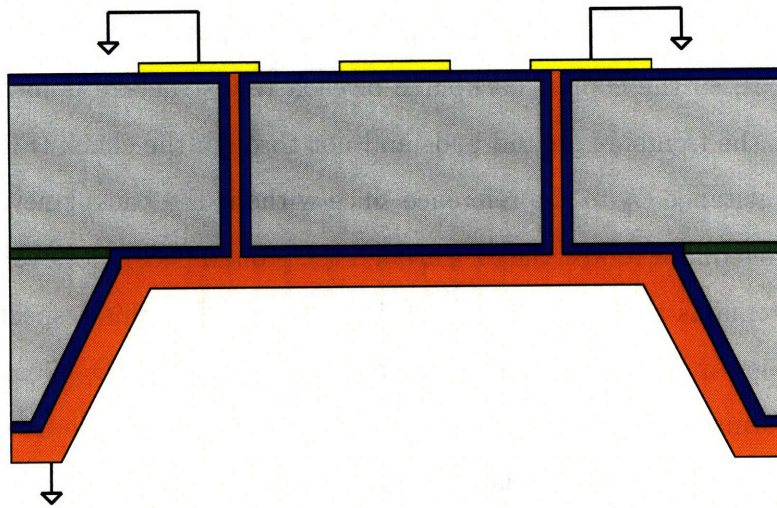
process in which the entire wafer backside was connected by copper and grounded through the chuck (Fig. 4-13), the new process has copper only in isolated, backside DRIE trenches, so the copper backplane of each test structure is locally grounded through only the frontside ground pads and not through the chuck (Fig. 4-14). This adds the capacitance  $C_g$  to the reference since without the backplane grounded, the capacitance is reduced to just the area around the ground pads. However, the Faraday cage model remains the same as the previous model [7] in this respect because the backplane is grounded through the substrate vias. The LPCVD silicon nitride liner is more conformal and of better quality than the PECVD nitride used in the S.M. process. This introduces the via sidewall capacitance,  $C_f$  into the Faraday cage model. Also, the spreading resistance,  $R_s$ , in previous work [7] is eliminated in the new models.

## 4.6 Circuit Simulations

After developing the lumped-element models, we simulated the equivalent circuit using Agilent Technologies Advanced Design System (ADS) software. The simulation

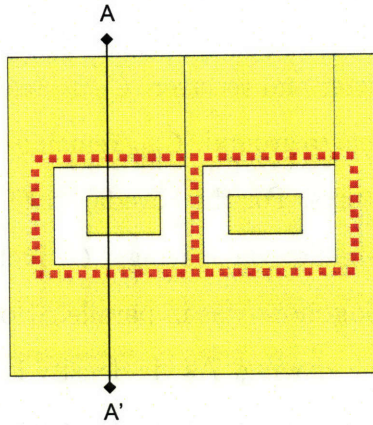


(a) Layout drawing of the S.M. Faraday cage test structure at  $d = 100 \mu\text{m}$ .

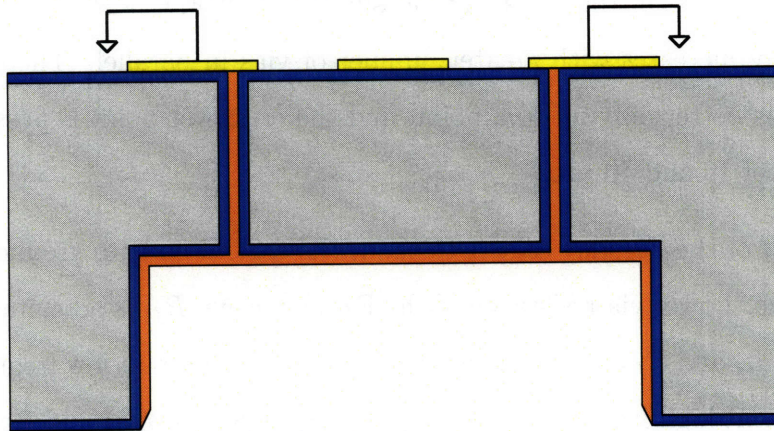


(b) Cross-sectional drawing of the S.M. Faraday cage test structure taken at line A-A'. Besides the ground pads, the backside copper backplane was also grounded through the chuck.

Figure 4-13: Drawings of the Faraday cage test structure used in my S.M. thesis work [8].



(a) Layout drawing of a type I Faraday cage test structure at  $d = 100 \mu\text{m}$ .



(b) Cross-sectional drawing of a type I Faraday cage test structure taken at line A-A'.

Figure 4-14: Drawings of the type I Faraday cage test structure.

results accurately match the measurements in Fig. 4-4a for different via spacings. Both simulation and measurement data are shown in Fig. 4-15 with the corresponding component values listed in Table 4.2. The lumped-element values follow a logical succession as the via density increases (decrease in via spacing from 70 to 10  $\mu\text{m}$ ).  $C_1$  decreases and  $R_1$  increases as the via spacing decreases because less substrate is present between the transmitter and receiver.  $C_2$  decreases and  $R_2$  increases also because less substrate is available to ground.  $C_{pad}$  remains constant because the pad size is identical for all test structures. For the Faraday cage circuit branch,  $R_f$  decreases with more vias in parallel (smaller via spacing).  $C_f$  increases because of greater via sidewall surface area by adding more vias in parallel. However,  $L_f$  shows a minimum between the 30 and 40- $\mu\text{m}$  via spacing. As via density increases, more vias are put in parallel so that the self-inductance decreases, but placing vias in close proximity to one another increases the mutual inductance. We see the competing effect of decreasing self-inductance and increasing mutual inductance. For very dense cages (10- $\mu\text{m}$  spacing), the Faraday cage inductance increases substantially due to rising mutual inductance. As seen in the via-array measurements in Fig. 3-11, The overall inductance actually increases with greater number of vias in parallel. Therefore, using a denser cage is better only up to a point, and the crossover point is possibly between via spacings of 10 and 40  $\mu\text{m}$ .

The effect of the Faraday cage is to shunt the central node to ground through the substrate vias. Lower via resistance of the Faraday cage,  $R_f$ , is advantageous as seen in Fig. 4-16.  $L_f$  and  $C_f$  are more complicated.  $C_f$  dominates at low frequencies, while  $L_f$  dominates at high frequencies. The minimum in  $|S_{21}|$  seen at mid-frequency is the resonance between  $L_f$  and  $C_f$  when both short out and the behavior is determined by  $R_f$ . To verify this, we varied values of  $C_f$  and  $L_f$  separately. Fig. 4-17 shows simulations where  $C_f$  was varied from 1 to 11 pF with all other elements held constant to values in Table 4.2 for  $v = 30 \mu\text{m}$ . As  $C_f$  increases with a denser cage, the vias gain a better grasp on the substrate so that more substrate current can be shunted to ground, and  $|S_{21}|$  drops. At the limit as  $C_f$  goes to infinity (when  $C_f$  is eliminated), the peak at low frequencies disappears and the substrate noise is minimized (Fig. 4-

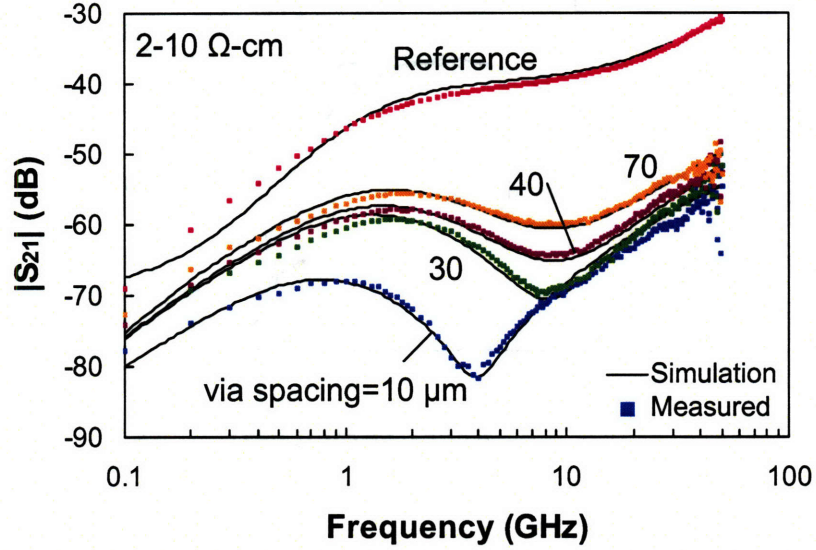


Figure 4-15:  $|S_{21}|$  vs. frequency of measurements and simulations of the lumped-element models in Fig. 4-11 for type I Faraday cages with different via spacing and the reference. The transmission distance was  $100 \mu\text{m}$ .

Table 4.2: Lumped-element values obtained from simulations of the Faraday cage and reference shown in Fig. 4-15.

	Reference	$v = 10 \mu\text{m}$	$30 \mu\text{m}$	$40 \mu\text{m}$	$70 \mu\text{m}$
$C_1$	2.5 fF	1 fF	1 fF	3 fF	3 fF
$R_1$	3.5 k $\Omega$	1.2 k $\Omega$	750 $\Omega$	700 $\Omega$	650 $\Omega$
$C_2$	20 fF	50 fF	50 fF	50 fF	60 fF
$R_2$	500 $\Omega$	900 $\Omega$	500 $\Omega$	450 $\Omega$	400 $\Omega$
$R_f$	–	2 $\Omega$	3 $\Omega$	5 $\Omega$	8 $\Omega$
$L_f$	–	165 pH	75 pH	70 pH	90 pH
$C_f$	–	10 pF	5 pF	4.5 pF	3.5 pF
$C_{pad}$	0.3 pF	0.3 pF	0.3 pF	0.3 pF	0.3 pF
$C_g$	1.5 pF	–	–	–	–

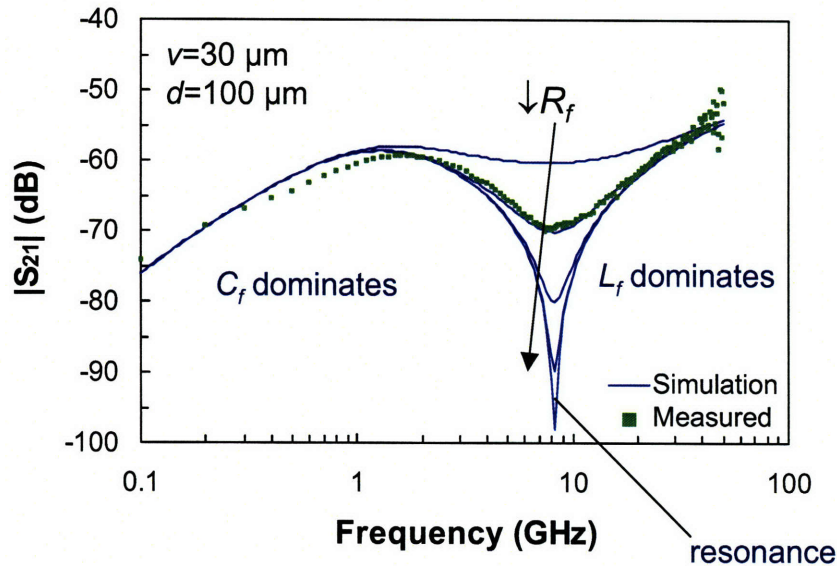


Figure 4-16:  $|S_{21}|$  vs. frequency of Faraday cage simulations varying  $R_f$  (0.1–10  $\Omega$ ) while other values were held constant.  $|S_{21}|$  drops with smaller values of  $R_f$ . The transmission distance was 100  $\mu\text{m}$  and via spacing 30  $\mu\text{m}$ .

17). In this instance, the low-frequency behavior is dominated by  $R_f$ . In Fig. 4-18,  $L_f$  was varied from 50 to 150 pH, and at high frequencies when  $L_f$  dominates, decreasing  $L_f$  reduces  $|S_{21}|$ .

#### 4.6.1 Via Sidewall Capacitance

The peak in  $|S_{21}|$  of the Faraday cages at low frequencies was not present in measurements of the S.M. process. Simulations of the S.M. Faraday cage model (Fig. 4-12) are plotted in Fig. 4-19 and match measurements. The equivalent circuit model for the S.M. process lacks the sidewall capacitance,  $C_f$ , in the center shunt because of a defective nitride liner. Comparing the circuit simulations of the S.M. process with the current process confirms that the peak in crosstalk at low frequencies is due to  $C_f$ .

For vias to be effective in suppressing crosstalk, the frequency has to be high enough for  $C_f$  to short out. With more vias, this occurs at lower frequencies (Fig. 4-

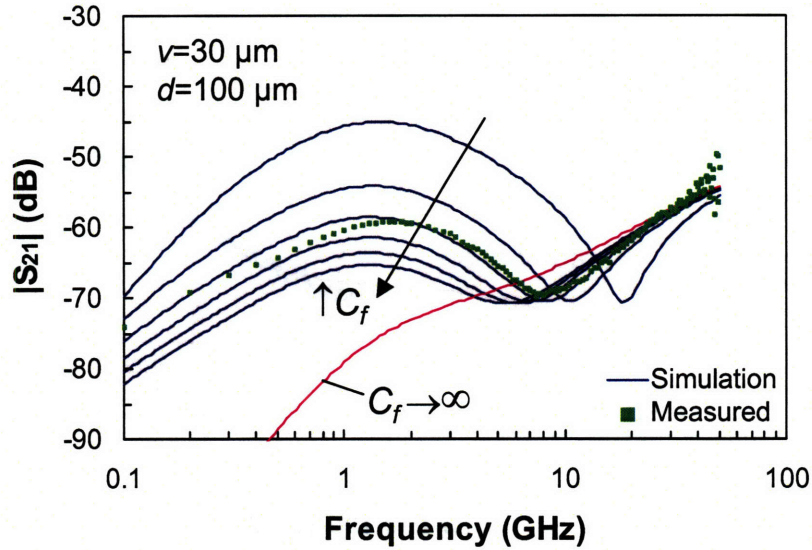


Figure 4-17:  $|S_{21}|$  vs. frequency of Faraday cage simulations varying  $C_f$  (1–11 pF) while other values were held constant.  $|S_{21}|$  drops with higher values of  $C_f$  at low to mid-frequencies.  $|S_{21}|$  is minimized at the limit when  $C_f$  goes to infinity ( $C_f$  is eliminated). The transmission distance was 100  $\mu\text{m}$  and via spacing 30  $\mu\text{m}$ .

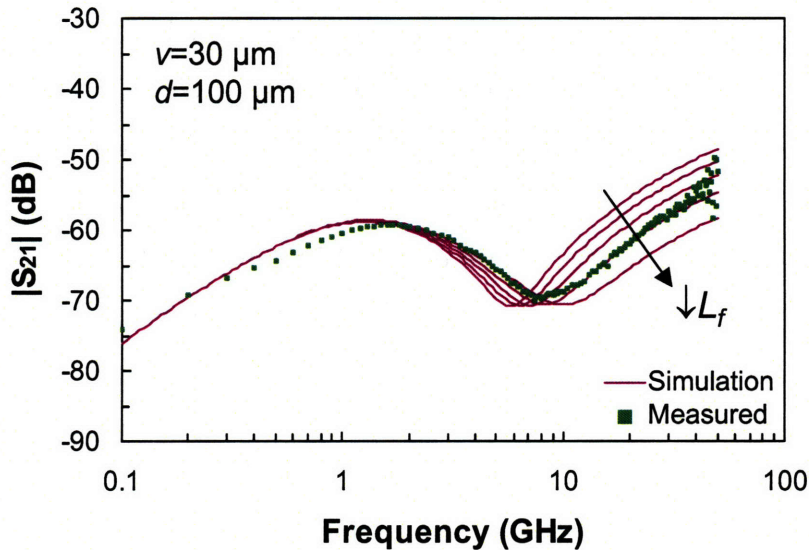


Figure 4-18:  $|S_{21}|$  vs. frequency of Faraday cage simulations varying  $L_f$  (50–150 pH) while other values were held constant.  $|S_{21}|$  drops with lower values of  $L_f$  at high frequencies. The transmission distance was 100  $\mu\text{m}$  and via spacing 30  $\mu\text{m}$ .

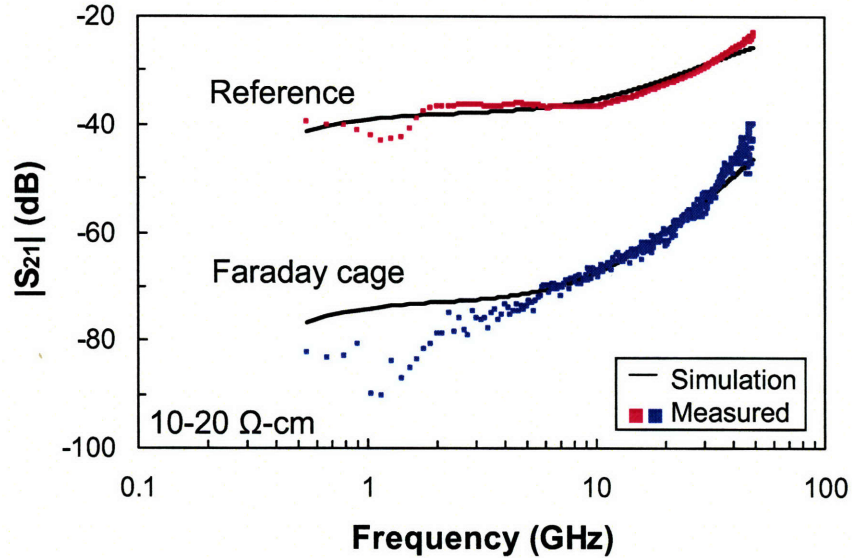


Figure 4-19:  $|S_{21}|$  vs. frequency of measurements and simulations of the lumped-element model in Fig. 4-12 for Faraday cages fabricated using the S.M. process. The vias of the Faraday cage were  $10\text{-}\mu\text{m}$  in diameter and separated by  $10\text{-}\mu\text{m}$ . The transmission distance was  $100\ \mu\text{m}$ . Substrate resistivity was  $10\text{-}20\ \Omega\cdot\text{cm}$ .

15). The pink line in Fig. 4-17 shows the simulation result for a Faraday cage without  $C_f$  but with all other elements held at their original values in Table 4.2. This shows that  $|S_{21}|$  at low frequency is minimized by eliminating  $C_f$ .  $C_f$  can be completely eliminated by using a metal liner instead of an insulator. Simulations of the Faraday cage circuit model without  $C_f$  are plotted in Fig. 4-20 with varying values of  $R_f$  and in Fig. 4-21 with varying values of  $L_f$ . Without  $C_f$ ,  $R_f$  determines the low-frequency behavior,  $L_f$  dominates the high-frequency behavior, and the  $LC$  resonance disappears. Therefore, the smaller the  $R_f$  and  $L_f$  branch is, the more effective the ground shunting of the substrate between the transmitter and receiver, resulting in a reduction in crosstalk.

#### 4.6.2 Transmission Distance

Circuit simulations of type I Faraday cages with varying transmission distance is shown with measurement data in Fig. 4-22. The via spacing is  $30\ \mu\text{m}$ . The cor-

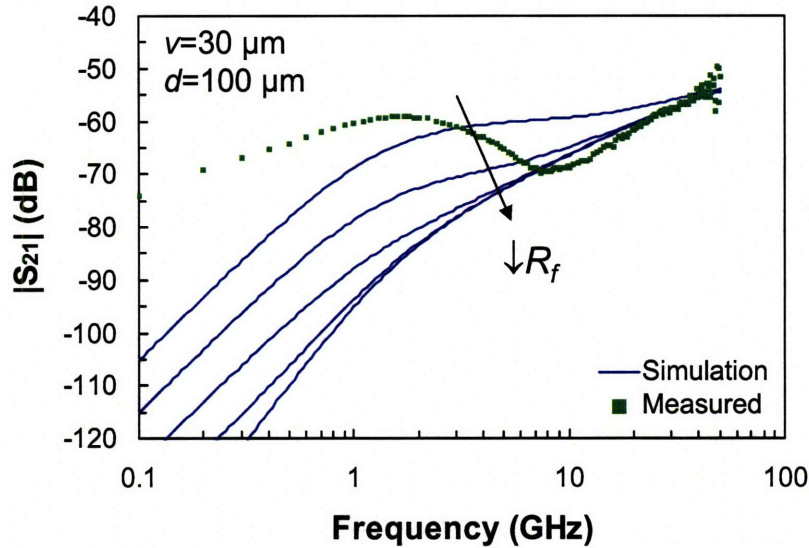


Figure 4-20:  $|S_{21}|$  vs. frequency of simulations of the Faraday cage model without  $C_f$ .  $R_f$  was varied from 0.1–10  $\Omega$  while other values were held constant. The transmission distance was 100  $\mu\text{m}$  and via spacing 30  $\mu\text{m}$ .  $R_f$  dominates the low-frequency behavior, and smaller values of  $R_f$  reduces  $|S_{21}|$ .

responding component values are listed in Table 4.3. Increasing the transmission distance increases the amount of silicon between the two pads. This translates to increase in substrate resistance and decrease in capacitance. To match simulation to measurement, we increased  $R_1$  and  $R_2$  accordingly; however, decreasing  $C_1$  and  $C_2$  had little effect on  $|S_{21}|$ , so these remained unchanged to simplify the simulations. Also, as  $d$  increases, the type I Faraday cage extends so that more vias are included in the cage on all sides. The increase in number of vias changes the  $RLC$  shunt so that  $R_f$  decreases, and  $L_f$  and  $C_f$  increase.

## 4.7 Faraday Cage Design Guidelines

Findings from the Faraday cage measurements and simulations can be summarized into design guidelines for use in mixed-signal circuits to reduce substrate noise. First, even without the Faraday cage, increasing the transmission distance reduces substrate

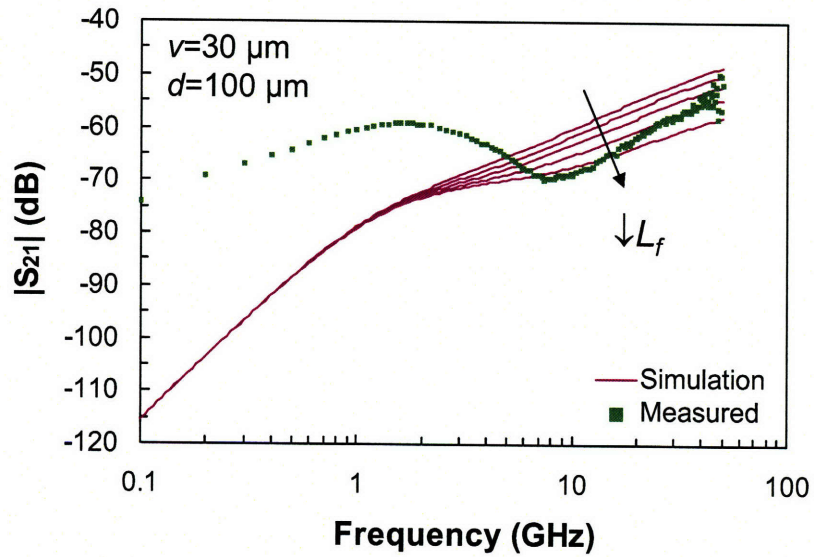


Figure 4-21:  $|S_{21}|$  vs. frequency of simulations of the Faraday cage model without  $C_f$ .  $L_f$  was varied from 50–150 pH while other values were held constant. The transmission distance was 100  $\mu\text{m}$  and via spacing 30  $\mu\text{m}$ .  $L_f$  dominates the high-frequency behavior, and smaller values of  $L_f$  reduces  $|S_{21}|$ .

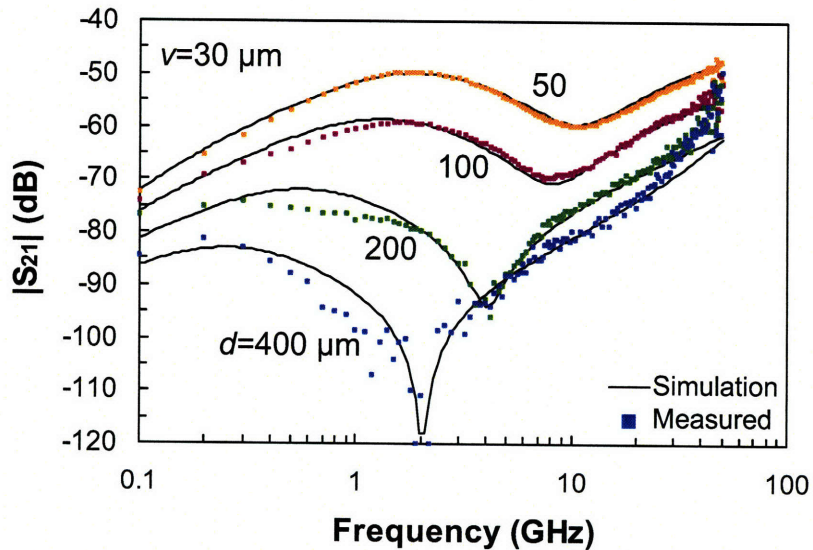


Figure 4-22:  $|S_{21}|$  vs. frequency of measurements and simulations of the lumped-element models in Fig. 4-11 for type I Faraday cages with increasing transmission distance,  $d$ . Via spacing is 30  $\mu\text{m}$ .

Table 4.3: Lumped-element values obtained from simulations of the Faraday cage and reference shown in Fig. 4-22.

	$d = 50 \mu\text{m}$	$100 \mu\text{m}$	$200 \mu\text{m}$	$400 \mu\text{m}$
$C_1$	1 fF	1 fF	1 fF	1 fF
$R_1$	400 $\Omega$	750 $\Omega$	1.8 k $\Omega$	3.8 k $\Omega$
$C_2$	50 fF	50 fF	50 fF	50 fF
$R_2$	400 $\Omega$	500 $\Omega$	1.2 k $\Omega$	3.2 k $\Omega$
$R_f$	3.5 $\Omega$	3 $\Omega$	1 $\Omega$	0.2 $\Omega$
$L_f$	55 pH	75 pH	140 pH	290 pH
$C_f$	4 pF	5 pF	12 pF	21 pF
$C_{pad}$	0.3 pF	0.3 pF	0.3 pF	0.3 pF

crosstalk. However, placing large distances between circuit blocks wastes chip area, so it is impractical. At short distances, the type II Faraday cage, which has a cage surrounding the transmitter and a cage surrounding the receiver, performs better than the type I design. Even though at farther distances the type I cage outperforms the type II, as stated earlier, large distances between circuit blocks is not an efficient use of space, so it is unlikely that distances as great as  $400 \mu\text{m}$  will be used. Therefore, the type II design is recommended over type I.

Reducing the resistance of the Faraday cage,  $R_f$ , will reduce substrate noise. Eliminating the via sidewall capacitance by using a metal liner instead of a dielectric will reduce the low-frequency substrate noise and eliminate the  $LC$  resonance. Reducing the Faraday cage inductance,  $L_f$ , will reduce substrate noise at high frequencies. The via density of the Faraday cage determines  $L_f$ , which has two competing mechanisms, self-inductance and mutual inductance. The minimum inductance lies between via spacings of 10 and  $40 \mu\text{m}$ .

## 4.8 Summary

Through-substrate vias arranged in a Faraday cage have proved to be an effective strategy to suppress substrate crosstalk, especially at high frequencies. On average,

the type I Faraday cage has reduced substrate noise by 31 dB at 10 GHz, and 21 dB at 50 GHz, compared to a reference structure. Using a type II cage surrounding both transmitter and receiver improves isolation even more, 32 dB at 10 GHz, and 26 dB at 50 GHz. The low-frequency performance of the Faraday cage is hindered by the via sidewall capacitance that shorts out at higher frequencies. Eliminating this capacitance by using a metal barrier liner instead of silicon nitride will alleviate this problem.

In order to better understand the performance of the Faraday cages, we developed lumped-element, equivalent circuit models of the test structures and simulated them in Agilent ADS. From these simulations, we have determined that the substrate vias of the Faraday cage act as an *RLC* shunt to ground that draws substrate current. To achieve optimum isolation, a low via resistance and elimination of sidewall capacitance is needed. The inductance is correlated to the number of vias and via spacing of the cage and needs to be optimized depending on the frequency of operation. At low frequencies a denser cage performs better. However, at high frequencies, isolation improves up to a point between via spacings of 10 and 40  $\mu\text{m}$ .

# Chapter 5

## Conclusions and Suggestions for Future Work

### 5.1 Conclusions

We have developed a low-impedance, through-substrate interconnect for backside routing of power, ground, and signals. A through-substrate via technology can be used as a low-inductance ground for RFICs, an interconnect for 3-D integration, or even a MEMS backside contact. Using the via sidewall capacitance, integrated capacitors are also possible.

We have fully characterized the inductance, resistance, and sidewall capacitance of the through-substrate via using  $S$  parameters. Simple equivalent circuit models accurately describe this via technology up to 50 GHz. To our knowledge, the substrate vias have the lowest reported inductance for aspect ratios greater than 4. The via sidewall capacitance approaches the theoretical calculation, and measured via resistance has been minimized by using a two-port test structure and better metallization with the new process. Accurate via impedance measurements will allow designers of devices, circuits, and MEMS to use substrate vias in their designs.

The application of through-substrate vias as a method for substrate noise isolation has been demonstrated and evaluated using  $|S_{21}|$  measurements up to 50 GHz and simulations of lumped-element, equivalent circuit models. Using substrate vias as

a Faraday cage to surround noisy and sensitive circuits has shown a reduction in substrate crosstalk of 32 dB at 10 GHz and 26 dB at 50 GHz at a distance of 100  $\mu\text{m}$ , compared to a reference structure. These significant results warranted investigation into the isolation mechanism of the Faraday cage, which led to the development of an equivalent circuit model and circuit simulations. These simulations have shown that the circuit model accurately represents the noise isolation characteristics of the Faraday cage, specifically that the substrate vias of the cage shunt substrate noise to ground. Finally, guidelines for Faraday cage design for optimum substrate noise isolation were outlined.

## 5.2 Suggestions for Future Work

### 5.2.1 Fabrication Improvements

The fabrication of through-substrate vias required the most effort in this Ph.D. thesis, especially in development and characterization of process steps. Due to the complexity of the process and equipment limitations in MTL, several steps could be improved upon.

Further study on copper electroplating would be required to reduce and eliminate the voids in the copper deposits. A power supply with higher maximum current would increase the blanket plating deposition rate. The problems discovered when wet etching oxide with an exposed high-dose implant could be remedied by using a plasma etch for oxide, which is currently unavailable in MTL for copper-contaminated, 150-mm wafers.

As mentioned in Section 2.4, in order to keep this process a back-end process, the high-temperature steps need to be eliminated: the thermal oxide sidewall smoothing and LPCVD silicon nitride steps. Adjusting the DRIE parameters to reduce DRIE grass or using a chemical etchant to smooth the sidewalls was suggested. To replace LPCVD nitride, an alternate liner of PECVD TEOS as the insulator with a metal barrier liner such as TiN or TaN can be used instead.

### 5.2.2 Test Structures

Using a two-port test structure to measure via inductance and resistance showed improved measurements as a result of lower parasitics. A two-port capacitance test structure with low parasitic capacitance is needed. The two-port test structure used for current leakage (Fig. 3-3) was originally intended to measure via sidewall capacitance. However, the  $S_{21}$  measurements were confusing due to the lack of a good ground. The capacitance was also measured using the two-port impedance test structure in Fig. 3-1 on  $p^+$  substrates. However, the sidewall capacitance of a single via was swamped by the pad capacitance.

### 5.2.3 Liner Integrity

The integrity of the silicon nitride liner was an issue not thoroughly resolved. A study as to where in the via structure the silicon nitride failed in some vias would reveal if it is a processing issue during CMP and the nitride etch, or if the silicon nitride itself is defective.

### 5.2.4 Faraday Cages

From Section 4.6.1, the Faraday cage performance at low frequencies is hindered by the via sidewall capacitance introduced by the insulating liner. For the purpose of substrate noise isolation, through-substrate vias with only a metal barrier liner would eliminate this capacitance and improve low-frequency suppression of crosstalk.

### 5.2.5 Integration on a Chip

The ultimate test of through-substrate vias as a 3-D interconnect and as a shunt for substrate noise would be to fabricate them into devices and circuits and measure their impact on circuit performance.



# Appendix A

## Through-Substrate Via Fabrication Process

The complete through-substrate via process flow is described in Table A.1. The process is divided into four sections: p<sup>+</sup> implant, backside patterning, frontside processing, and metallization. Recipes for the DRIE tools and copper CMP are also included.

Starting material:

- Prime 150-mm, p-type Boron, <100> silicon wafers, double-side polished, 1–10  $\Omega\cdot\text{cm}$ , 650–700  $\mu\text{m}$  thick
- Prime 150-mm, n-type Phosphorus, <100> silicon wafers, double-side polished, 2–10  $\Omega\cdot\text{cm}$ , 592–607  $\mu\text{m}$  thick
- Prime 150-mm, p-type Boron, <100> silicon wafers, double-side polished, 0.01–0.03  $\Omega\cdot\text{cm}$ , 481  $\mu\text{m}$  thick
- SOI 150-mm, p-type Boron, <100> silicon wafers, 10–20  $\Omega\cdot\text{cm}$ , 100- $\mu\text{m}$  device layer, 1- $\mu\text{m}$  BOX, 450- $\mu\text{m}$  handle wafer
- Quartz 150-mm wafers (for handle wafer mount – step 23)

Table A.1: Through-Substrate Via Process

Process Step	Machine name	Laboratory
<b>P<sup>+</sup> implant</b>		
1 RCA clean	rca-ICL	ICL <sup>1</sup>
2 Thermal oxide growth: 1 $\mu\text{m}$ , wet, 1050°C	5D-ThickOx	ICL
3 Photolithography: <i>IMPLANT</i> mask		TRL <sup>2</sup>
HMDS recipe 5	HMDS-TRL	
Standard resist OCG825:	coater	
dispense 500 rpm, 12 s		
spread 750 rpm, 12 s		
spin 2000 rpm, 30 s		
Prebake: 95°C, 30 min	prebakeoven	
Exposure: continuous 2.3 s	EV1	
Develop: OCG934 1:1, 1 min	photo-wet-l	
Postbake: 120°C, 30 min	postbake	
4 Oxide etch	AME5000	ICL
recipe: BASELINE OX NEW, 297 s		
5 Resist strip, 1 min	asher-ICL	ICL
6 p <sup>+</sup> implant: Boron $2 \times 10^{16} \text{ cm}^{-2}$ , 150 keV	<i>outsource</i>	CORE <sup>3</sup>
7 Post-implant piranha clean	acidhood2	TRL
<b>Backside</b>		
8 Photolithography: <i>DRIE</i> mask		TRL
HMDS recipe 3	HMDS-TRL	
AZ9260 resist:	coater	
static dispense (golf ball size)		
spread 500 rpm, 9 s		
spin 3000 rpm, 60 s		
edge bead removal 4000 rpm, 10 s		
Prebake: 95°C, 1 hr	prebakeoven	
Cool down, wait 15 min		
Exposure: back-to-front alignment, hard contact	EV1	
Interval: 15 s exp, 15 s wait, 4 intervals		
Outgassing, wait 20 min		
Develop: AZ440 MIF, 2 min	photo-wet-l	
9 Frontside resist coat, OCG825	coater	TRL
dispense 500 rpm, 9 s		
spread 750 rpm, 9 s		
spin 3000, rpm 30 s		

<sup>1</sup>ICL: Integrated Circuits Laboratory<sup>2</sup>TRL: Technology Research Laboratory<sup>3</sup>CORE: Core Systems, Inc., 1050 Kifer Road, Sunnyvale, CA 94086

Process Step	Machine name	Laboratory
Postbake: 95°C, 30 min	prebakeoven	
10 Oxide etch: BOE ultrasonic, 14 min	acidhood2	TRL
11 Alignment marks		TRL
Etch recipe: ALIGNMRK, 30 s	sts2	
Paint alignment marks with AZ4620 resist		
Bake resist: 95°C, 25 min	prebakeoven	
Cover alignment marks with capton tape		
12 Backside DRIE	sts2	TRL
recipe: OLE3 3–5 hr, until 100 $\mu\text{m}$ left		
13 Polymer etch: ALIGNMRK, 20 s	sts2	TRL
14 Resist strip, barrel asher, 1 hr	asher-TRL	TRL
15 Resist strip, piranha, 20 min	acidhood2	TRL
16 Oxide strip: BOE ultrasonic	acidhood2	TRL
17 BOX etch ( <i>for SOI wafers only</i> )	centura	ICL
recipe: c2f6, 180 s (backside)		
<b>Frontside</b>		
18 Piranha clean	premetal-green	ICL
19 CVD oxide 5000 Å	DCVD	ICL
recipe: OXIDE 5KA CHA		
20 Photolithography: <i>VIA</i> mask		TRL
HMDS recipe 3	HMDS-TRL	
AZ4620 resist, using o-ring chuck:	coater	
static dispense 12s		
spread 3500 rpm, 60 s		
spin 5000 rpm, 10 s		
edge bead removal (acetone)		
Prebake: 95°C, 1 hr	prebakeoven	
Exposure: front-to-back alignment, hard contact	EV1	
continuous 9 s		
Develop: AZ440 MIF, 1:40 min	photo-wet-1	
Postbake: 95°C, 30 min	prebakeoven	
21 Oxide etch: BOE ultrasonic, 5 min	acidhood2	TRL
22 Alignment mark etch: ALIGNMRK, 30 s	sts2	TRL
23 Handle wafer mount: AZ4620 resist		TRL
2000 rpm, target mount on quartz wafer	coater	
Paint alignment marks with AZ4620 resist		
Bake horizontal: 95°C, 20 min	prebakeoven	
Cover alignment marks with capton tape		
24 Frontside DRIE	sts2	TRL
recipe: OLE3 2–4 hr, until through		
25 Polymer etch: ALIGNMRK, 20 s	sts2	TRL

	Process Step	Machine name	Laboratory
26	Acetone dismount, ~1 day	Solvent-noAu	TRL
27	Resist strip, barrel asher, 1 hr	asher-TRL	TRL
28	Resist strip, piranha, 20 min	acidhood2	TRL
<b>Liner</b>			
29	RCA clean	rca-TRL	TRL
30	Thermal oxide growth 0.5 $\mu\text{m}$ , wet, 1050°C, 70 min	A2-WetOxBond	TRL
31	Oxide strip, BOE ultrasonic, 10 min	acidhood2	TRL
32	Piranha clean	premetal-green	ICL
33	CVD oxide recipe: OXIDE 2KA CHA	DCVD	ICL
34	Piranha clean ( <i>optional if going directly to vtr</i> )	premetal-green	ICL
35	Silicon nitride LPCVD, 775°C, 7000 Å	vtr	ICL
<b>Metallization</b>			
36	Ti-Cu seed deposition (frontside) Ti 250 Å, Cu 2000 Å	ebeamAu	TRL
37	Cu electroplating, blanket plating Pulse-reverse, 810 mA, front facing anode	plating-bench	ICL
38	Cu electroplating in jig Pulse-reverse, 670 mA, back facing anode	plating-bench	ICL
39	Cu sputter deposition, 2 $\mu\text{m}$ (backside)	perkin-elmer	TRL
40	Cu CMP frontside, 30–50 min	Cu-CMP	ICL
41	Cu CMP backside, 10–30 min	Cu-CMP	ICL
42	Water polish, PVA sponge	Cu-CMP	ICL
43	Post-CMP clean: 9000 ppm citric acid Mix 45 g citric acid powder with 1 L water Dilute with additional 4 L water, soak 10 min	acidhood-EML acidhood	EML <sup>4</sup> TRL
44	Photolithography: <i>NITRIDE</i> mask OCG825 resist: dispense 500 rpm, 12s spread 750 rpm, 12 s spin 3000 rpm, 30 s Prebake: 95°C, 30 min Exposure: continuous 2.3 s Develop: OCG934 1:1, 1:10 min Postbake: 120°C, 30 min	coater    prebakeoven EV1 photo-wet-1 postbake	TRL
45	Nitride etch, oxide etchstop recipe: NITRIDE, 15–22 min	sts1	TRL
46	Oxide etch (frontside), HF gas, 2:30 min	acidhood	TRL

<sup>4</sup>EML: Exploratory Materials Laboratory

	Process Step	Machine name	Laboratory
47	Resist strip, NMP in ultrasonic bath	photo-wet-Au	TRL
48	Al deposition, 0.4 $\mu\text{m}$	ebeamAu	TRL
49	Contact anneal, forming gas, 450°C, 30 min	B1-Au	TRL
50	Photolithography: <i>CONTACT</i> mask		TRL
	HMDS recipe 3	HMDS-TRL	
	AZ4620 resist:	coater	
	static dispense 25s		
	spread 2000 rpm, 60 s		
	spin 3500 rpm, 10 s		
	edge bead removal (acetone)		
	Prebake: 95°C, 1 hr	prebakeoven	
	Exposure: hard contact	EV1	
	Interval: 5 s exp, 4 s wait, 4 intervals		
	Develop: ample AZ440 MIF, 1:55 min	photo-wet-l	
	Postbake: 95°C, 30 min	prebakeoven	
51	Al etch, OCG934 developer, 20–30 min	photowet-r	TRL
52	Resist strip, NMP soak	photowet-r	TRL
53	Al deposition, 1 $\mu\text{m}$	ebeamAu	TRL
54	Photolithography: <i>METAL</i> mask		TRL
	HMDS recipe 3	HMDS-TRL	
	AZ4620 resist:	coater	
	static dispense 25s		
	spread 2000 rpm, 60 s		
	spin 3500 rpm, 10 s		
	edge bead removal (acetone)		
	Prebake: 95°C, 1 hr	prebakeoven	
	Exposure: hard contact	EV1	
	Interval: 5 s exp, 4 s wait, 4 intervals		
	Develop: ample AZ440 MIF, 1:55 min	photo-wet-l	
	Postbake: 95°C, 30 min	prebakeoven	
55	Al etch, HF 50:1, 5 min	acidhood	TRL
56	Resist strip, NMP soak	photo-wet-Au	TRL

Table A.2: OLE3 recipe for the DRIE tool sts2

	Passivation Cycle	Etch Cycle
SF <sub>6</sub> flow rate	0	140 sccm
SF <sub>6</sub> active time	0	14 s
C <sub>4</sub> F <sub>8</sub> flow rate	95 sccm	0
C <sub>4</sub> F <sub>8</sub> active time	12.5 s	0
Etch overlap	–	0.5 s
Platen power	0	140 W
Coil power	600 W	600 W
Pressure (APC angle)	31 mTorr	31 mTorr

Table A.3: NITRIDE recipe for the sts1

Parameter	Value
SF <sub>6</sub> flow rate	160 sccm
C <sub>4</sub> F <sub>8</sub> flow rate	120 sccm
Platen power	30 W
Coil power	800 W
Pressure (APC angle)	30 mTorr

Table A.4: Polish parameters for the copper CMP (recipe: jowu#1)

Parameter	Value
Down force	10 psi
Zone 1	1 psi
Zone 2	1 psi
Spindle speed	20 rpm
Table speed	32 rpm
Slurry	100 mL/min

Copper CMP slurry iCue 5306E was obtained from Cabot Microelectronics Corp. and mixed with 2.5% hydrogen peroxide

# Appendix B

## Copper Electroplating

### Specifications

This appendix details the copper electroplating specifications, including pulse-reverse current supply waveform and calculations.

For blanket plating, we chose a duty cycle,  $D$ , of 0.83 and an average current density,  $J_{av}$ , of 4.6 mA/cm<sup>2</sup>. For jig plating, we used an average current density of 12.5 mA/cm<sup>2</sup>. The positive (forward) pulse was 5 ms, and the negative (reverse) pulse was 1 ms. Refer to Table B.1 for the complete plating variables for both blanket and jig plating. Fig. B-1 shows the current density waveform. Equations to calculate the plating variables are listed below. The duty cycle and average current density are defined as:

$$D = \frac{t^+}{t^+ + t^-} \quad (\text{B.1})$$

$$J_{av} = J_{av}^+ - J_{av}^- \quad (\text{B.2})$$

$$J_{av}^+ = M \times J_{av} \quad (\text{B.3})$$

$$J_{av}^- = (M - 1) \times J_{av} \quad (\text{B.4})$$

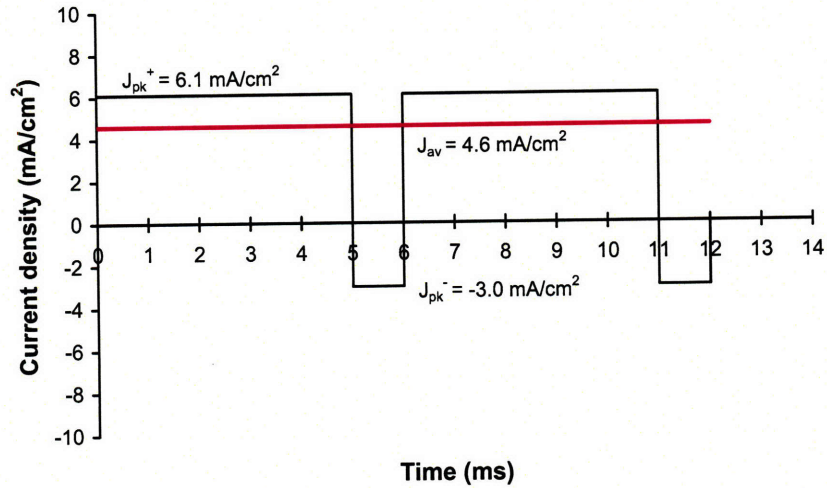
Table B.1: Copper electroplating variables

Parameter	Variable	Blanket Plating	Jig Plating
Surface area	$A$	177 cm <sup>2</sup>	44 cm <sup>2</sup>
Duty cycle	$D$	0.83	0.83
Positive pulse	$t^+$	5 ms	5 ms
Negative pulse	$t^-$	1 ms	1 ms
Average current density	$J_{av}$	4.6 mA/cm <sup>2</sup>	12.5 mA/cm <sup>2</sup>
Multiplication factor	$M$	1.2	1.2
Average forward current density	$J_{av}^+$	5.1 mA/cm <sup>2</sup>	15.0 mA/cm <sup>2</sup>
Average reverse current density	$J_{av}^-$	-0.5 mA/cm <sup>2</sup>	-2.5 mA/cm <sup>2</sup>
Average forward current	$I_{av}^+$	900 mA	660 mA
Average reverse current	$I_{av}^-$	-90 mA	-110 mA
Forward peak current density	$J_{pk}^+$	6.1 mA/cm <sup>2</sup>	18 mA/cm <sup>2</sup>
Reverse peak current density	$J_{pk}^-$	-3 mA/cm <sup>2</sup>	-15 mA/cm <sup>2</sup>

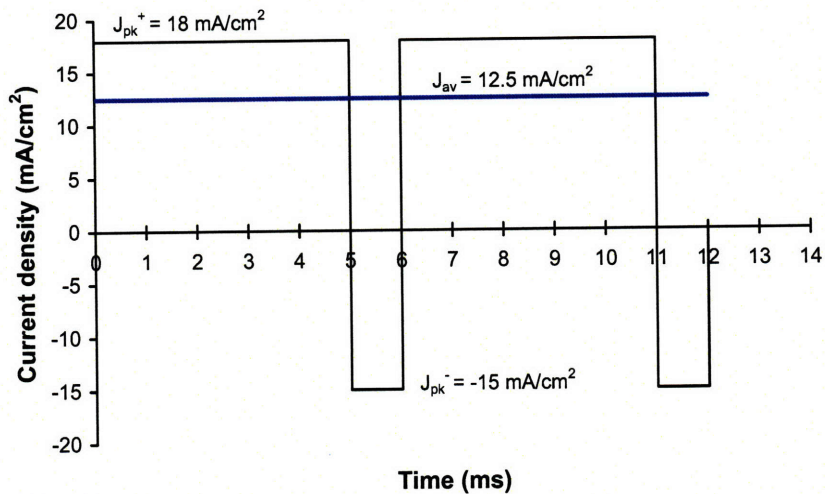
where  $t^+$  is the positive pulse,  $t^-$  is the negative pulse,  $M$  is the multiplication factor,  $J_{av}^+$  is the average forward (positive) current density, and  $J_{av}^-$  is the average reverse (negative) current density. The average forward current,  $I_{av}^+$ , and the average reverse current,  $I_{av}^-$ , are the values displayed on the Dynatronix current supply. The peak current densities for forward and reverse can be calculated as follows:

$$J_{pk}^+ = \frac{J_{av}^+}{D} \quad (\text{B.5})$$

$$J_{pk}^- = \frac{J_{av}^-}{1 - D} \quad (\text{B.6})$$



(a) Blanket plating waveform. The average current density is 4.6 mA/cm<sup>2</sup>. The peak forward current density is 6.1 mA/cm<sup>2</sup>, and the peak reverse current density is -3 mA/cm<sup>2</sup>.



(b) Jig plating waveform. The average current density is 12.5 mA/cm<sup>2</sup>. The peak forward current density is 18 mA/cm<sup>2</sup>, and the peak reverse current density is -15 mA/cm<sup>2</sup>.

Figure B-1: Current density waveforms used for copper electroplating.

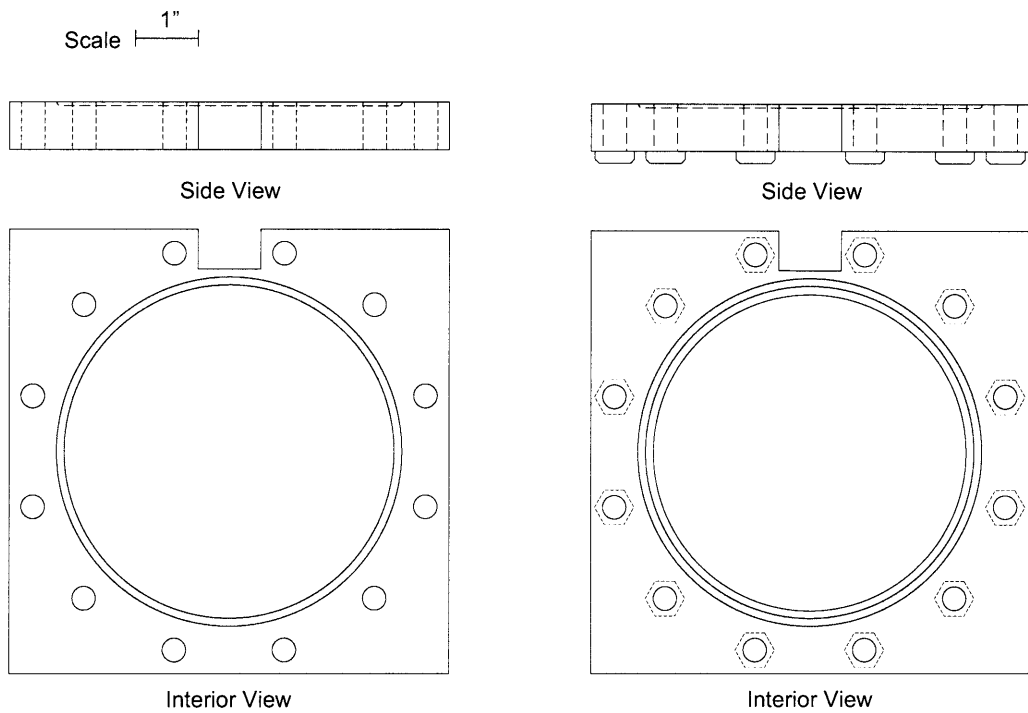


# Appendix C

## Electroplating Jig Specifications

This appendix describes the physical specifications for and the use of the Teflon jig for copper electroplating. The jig was custom-made by the MIT machine shop. The jig is constructed from two 7-inch square pieces of Teflon machined to the dimensions shown in Fig. C-1. Each Teflon piece fits a Teflon O-ring on the interior side. The dummy wafer and fabricated wafer fit in between the top and bottom Teflon pieces, which are secured together with twelve Teflon screws. There is a cutout at the top of the jig so that the cathode electrode can connect to copper seed of the fabricated wafer.

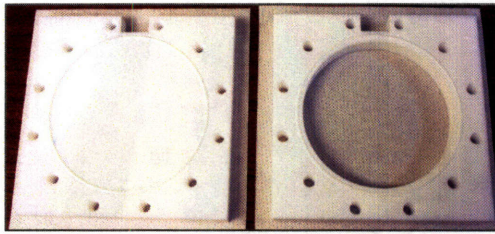
Fig. C-2 describes loading of the fabricated wafer into the Teflon jig and assembling the jig, and Fig. C-3 describes the preparation for jig plating in the electroplating bath.



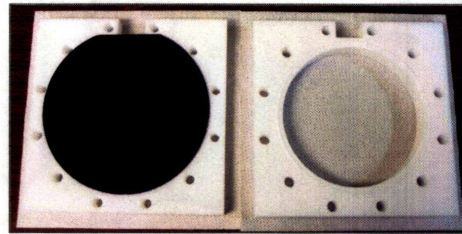
(a) Side view and interior view of the bottom section of the jig.

(b) Side view and interior view of the top section of the jig.

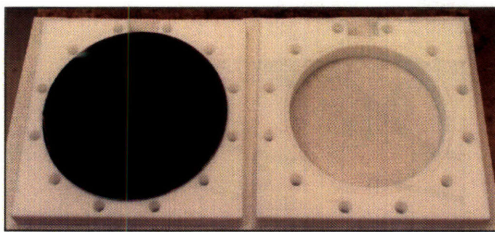
Figure C-1: Mechanical drawings of the Teflon jig. The Teflon O-ring (in gray) has an interior diameter of  $5\frac{1}{4}$  inches and is an  $\frac{1}{8}$ -inch thick.



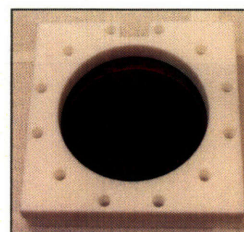
(1) Teflon jig with interior side showing.



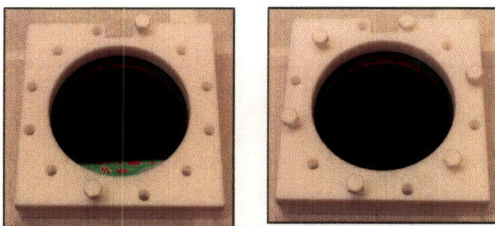
(2) Place dummy wafer on jig bottom piece, polished side facing up. The wafer flat is at the top.



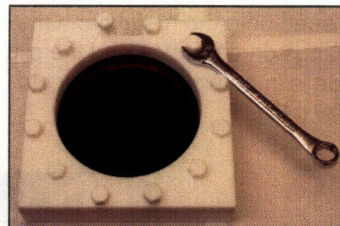
(3) Place fabricated wafer facedown on top of dummy wafer. The wafer flat is placed at any point but the top.



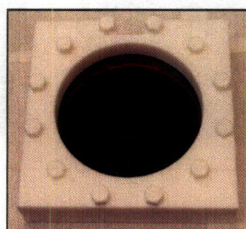
(4) Place jig top piece on top of fabricated wafer so that the O-ring touches the wafer.



(5) Screw in by hand opposing sides until all screws are in.



(6) Tighten screws using wrench.



(7) Wafer is ready for jig plating.

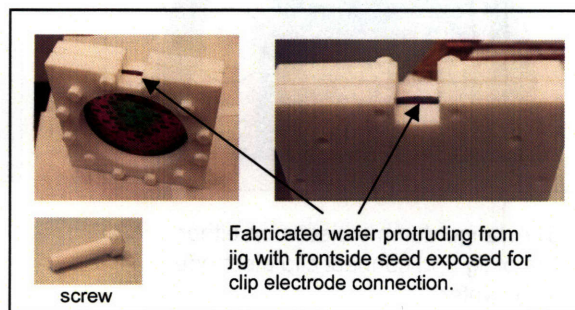
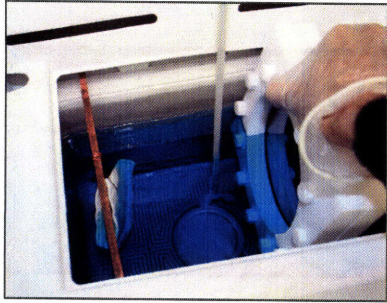
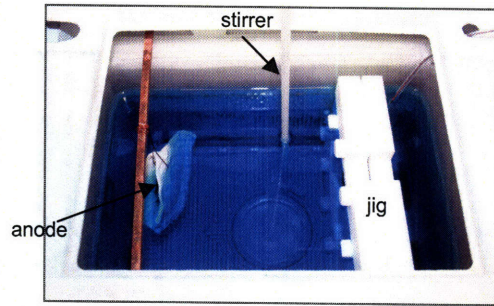


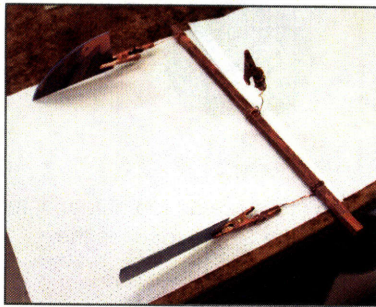
Figure C-2: Loading of the fabricated wafer into the Teflon jig.



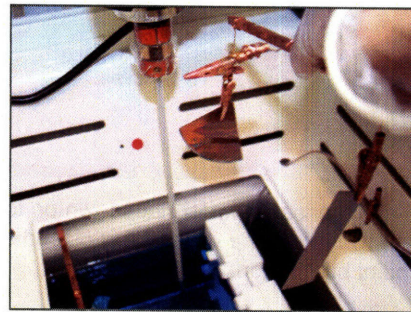
(1) Place Teflon jig into electroplating bath with wafer facing anode.



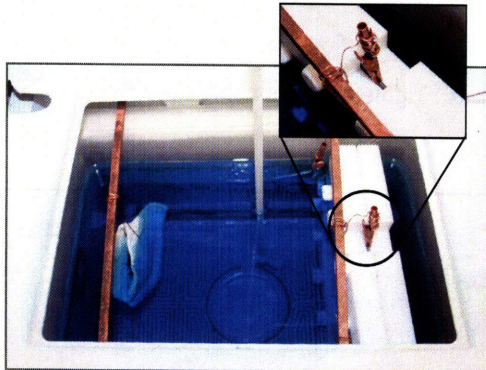
(2) Arrangement of the anode and jig in electroplating bath.



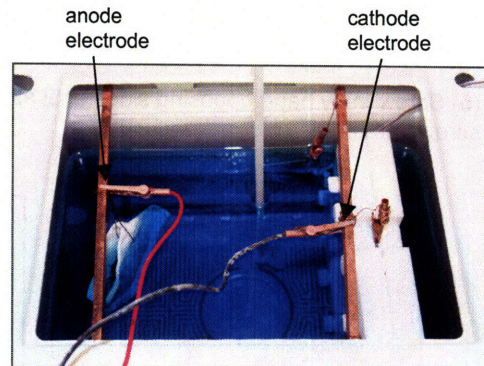
(3) Arrange dummy wafer pieces with copper seed onto the metal bar. One piece hangs on each side and the clip electrode is in between to connect to the wafer in jig.



(4) Place dummy pieces into bath.



(5) Arrange dummy pieces on either side of jig and connect clip electrode to the wafer.



(6) Clip electrodes to anode and cathode metal bars.

Figure C-3: Arranging the Teflon jig and dummy wafers in the copper electroplating bath for jig plating.

# Appendix D

## SUPREM Simulations

This appendix contains the SUPREM simulation file for the p<sup>+</sup> boron implant.

```
$Joyce Wu   October 2004
$x0experiment2d.inp
$Diffusion after implant for contacts
$Adding oxide capping layer before oxidation-diffusion

$LINE Y LOC=6 SPA=0.02
$Automatic grid
INITIALIZE  BORON=9E14

$Grow masking oxide 1um
DIFFUSION  TEMP=1050  TIME=200  WETO2

$Etch oxide mask layer
ETCH      OXIDE      ALL

$TED model
METHOD PD.FULL

$Implant boron
IMPLANT   BORON      DOSE=2E16  ENERGY=150 PEARSON

$Oxide cap layer DCVD
DEPOSITION OXIDE      THICKNESS=0.3
DIFFUSION  TEMP=400   TIME=5      INERT

$Oxidation and nitride liner dep
DIFFUSION  TEMP=1050  TIME=20     DRYO2
```

```
DIFFUSION  TEMP=1050  TIME=70  WETO2
DIFFUSION  TEMP=1050  TIME=20  DRYO2
SELECT     Z=DOPING
PRINT.1D   LAYERS X.V=0
```

```
ETCH       OXIDE      ALL
```

```
$Deposit DCVD oxide
```

```
DEPOSITION OXIDE      THICKNESS=0.2
DIFFUSION  TEMP=400   TIME=5    INERT
```

```
DEPOSITION NITRIDE THICKNESS=0.7
DIFFUSION  TEMP=775   TIME=233  INERT
```

```
$Contact anneal
```

```
DIFFUSION  TEMP=450   TIME=30   INERT
```

```
$Save
```

```
SAVEFILE   OUT.FILE=x0experiment2d
```

```
$Plot results
```

```
SELECT     Z=LOG10(BORON) TITLE="Active Boron" LABEL=LOG(Concentration)
PLOT.1D    X.VALUE=0 BOTTOM=13 TOP=21 RIGHT=10 LEFT=-1 LINE.TYP=1 COLOR=4
SYMBOL=2
LABEL      X=4.2 Y=15.1   LABEL=Boron
LABEL      X=-0.2 Y=13.8  LABEL=Nitride
LABEL      X=0.3 Y=14     LABEL=Oxide
LABEL      X=1.5 Y=13.1   LABEL=Silicon
```

```
$Print interface
```

```
SELECT     Z=BORON
PRINT.1D   SILICON/OXIDE
$PRINT.1D  SILICON/NITRIDE
```

```
$Print layer information
```

```
SELECT     Z=DOPING
PRINT.1D   LAYERS X.V=0
```

```
$Sheet resistance
```

```
ELECTRIC   X=0.0
```

```
Stop
```

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