Length Effects on the Reliability of Dual-Damascene Cu Interconnects

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***Abstract*-- The effects of interconnect length on the reliability of dual-damascene Cu metallization have been investigated. As in Al-based interconnects, the lifetimes of Cu lines increase with decreasing length. However, unlike Al-based interconnects, no critical length exists, below which all Cu lines are 'immortal'. Furthermore, we found multi-modal failure statistics for long lines, suggesting multiple failure mechanisms. Some long Cu interconnect segments have very large lifetimes, whereas in Al segments, lifetimes decrease continuously with increasing line length. It is postulated that the large lifetimes observed in long Cu lines result from liner rupture at the bottom of the vias, which allows continuous flow of Cu between the two bond pads. As a consequence, the average lifetimes of short lines and long lines can be higher than those of lines with intermediate lengths.**

***Index Terms*-- interconnects, reliability, length effects**

I. INTRODUCTION

Over the past few years, copper has become the metal of choice for chip-level interconnects in high-performance integrated circuits. Compared to conventional Al metallization, Cu interconnects have the advantage of lower resistivity and are expected to have improved reliability.[1] Nevertheless, failure due to electromigration (EM) remains a major reliability concern in Cu interconnects, as experienced in Al metallization. EM is the current-induced diffusion of atoms due to the momentum transfer from moving electrons. EM can lead to failure at certain points along the interconnect, when an atomic flux divergence occurs at those points. This atomic flux divergence leads to either a compressive or tensile stress, which can result in extrusions and short circuit failures, or voiding and open circuit failures, respectively. This investigation focuses on the effects of the interconnect line length on EM-induced failures. An understanding of these effects is crucial for accurate assessment of the reliability of Cu-based interconnects.

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II. EXPERIMENTAL

Dual-damascene Cu-interconnect structures have been fabricated by the Institute of Microelectronics (IME), Singapore, and International Sematech Inc., USA, for this study. The EM test structures consist of straight-line segments terminating at vias at each end. Lines of different widths and lengths, as well as metallization level – lower metallization 1 (M1), or upper metallization 2 (M2), have been tested. In all the test structures, Ta metal liners surround the Cu interconnect lines at the side and bottom, while a Si_3N_4 inter-level dielectric layer encapsulate them at the top. The dual-damascene vias at both ends of a line are connected to the bond pads through much wider connector lines. These connectors are 5 to 10 times wider than the test line, so that EM failure will not occur in them before the test line, as they are carrying lower current densities. For the M1 level structures, the EM test structure lies in the lower level of metallization. The vias are located above the test line, and the connector lines are in the upper metallization level. Conversely, for M2 structures, the test lines are in M2 while the connector lines are in M1. See Figure 1.

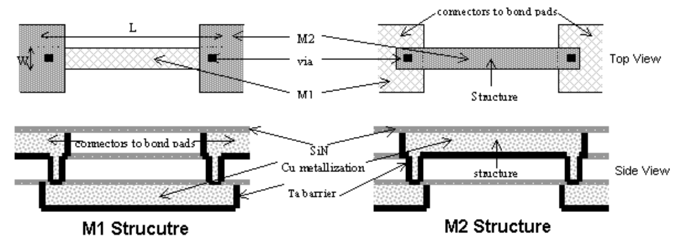

Fig. 1. Schematic top and side views of the M1 and M2-type dual-damascene interconnect structures fabricated by the IME, Singapore, and Sematech Inc., USA.

For this study, we carried out package-level and wafer-level constant-current EM stress experiments. Wafer-level tests were performed at MIT and package-level tests were carried out at IME, Sandia National Laboratories, and Intel Corp. For all the experiments, the test temperature was maintained at 350°C and the current densities were varied in the range of 2.0 to 3.6MA/cm^2.

III. Results

The median-times-to-failure (t_{50}'s) for different lengths of M1 Cu lines, fabricated by Sematech and IME, are shown in Table I and II respectively.

TABLE I
Test data for M1 Structures Fabricated by Sematech. Here, j is the current density, t_{50} is the median time to failure, σ is the standard deviation in the lognormal failure times, % unfailed lines is the percentage of lines that did not fail at the end of the test time.

Structure	Pre-test annealing	Length (μm)	Width (μm)	j (MA/cm²)	t_{50} (mins)	σ	% unfailed lines	test time (mins)	Decrease in MTTF (%)
M1	No	1000	0.30	2.0	3138	≥1.12	23.1	13659	--
M1	Yes	1000	0.30	2.0	2430	≥1.22	7.70	16631	22.5
M1	No	100	0.30	2.0	1158	0.76	0	4851	--
M1	Yes	100	0.30	2.0	996	0.48	0	2373	14.0
M1	No	50	0.30	2.0	4854	≥0.49	20.0	8511	--
M1	Yes	50	0.30	2.0	4356	≥1.01	25.0	9691	10.2

TABLE II
t_{50}'s for M1 and M2 Structures Fabricated by IME

Structure	Length (μm)	Width (μm)	j (MA/cm²)	t_{50} (mins.)	σ	% unfailed lines	test time (mins.)
M1	800	0.28	2.5	1720	≥1.07	6.7	28731
M1	100	0.28	2.5	1230	≥0.85	6.3	11541
M1	50	0.28	2.5	1262	0.62	0	23189
M1	20	0.28	2.5	9820	≥1.74	37.5	23189

Several observations can be made from the two sets of data. First, the lifetimes of the interconnect segments is minimum for lines that are 100μm in length, and increase with *both* decreasing segment length *and* with increasing segment length. Second, the deviation in the time to failure is also a minimum for lines of intermediate length. Third, the deviations in the time to failure of long and short lines are sufficiently high to suggest the operation of multiple failure mechanisms.

IV. Discussion

A. Blech Immortality

In general, the total atomic flux under electromigration in a straight segment of interconnect is described by the Blech-Korhonen model[2,3]:

$$J_a = \frac{Dc_a}{kT}\rho\,|\,j\,|\,z^* q - \frac{Dc_a}{kT}B\frac{\partial\mu_\sigma}{\partial x}\quad, \qquad (1)$$

where J_a is the atomic flux, D is the diffusivity, c_a is the atomic concentration, ρ is the resistivity, j is the current density, z^* is the effective valence of the atoms, q is the fundamental charge, B is the effective bulk modulus, and μ_σ is the chemical potential associated with the induced stress.

The first term on the right of equation 1 represents the forward flux due to the electron wind force, which generates a tensile stress at the cathode – the electron source, and a compressive stress at the anode – the electron sink. This, in turn, generates a backward flux due to the stress-induced gradient in chemical potential, which opposes the electron wind force. If the interconnect segment does not fail, the forward and backward fluxes will balance each other. Under steady state conditions, the maximum stress difference $\Delta\sigma_{max}$ within an interconnect segment of length L occurs at the electrodes, and has a magnitude given by[2,4]

$$\Delta\sigma_{\max} = \frac{z^* q\rho(jL)}{2\Omega} \qquad (2)$$

where Ω is the atomic volume.

Based on the Blech model, if $\Delta\sigma_{max}$ falls below the critical value which initiates failure, EM will not lead to failure and the interconnect will be 'immortal'. The critical stress for the initiation of tensile failure is the stress required for void nucleation, and the critical stress required to initiate compressive failure is the stress required to initiate the flow of the metal into the dielectric at the anode (e.g., the stress required to crack a brittle dielectric). From equation (2), the Blech criterion for immortality is:

$$(jL)_{\text{crit,nuc}} = \frac{2(\Delta\sigma_{\text{crit}})\Omega}{Z^* q\rho} \qquad (3)$$

For Al interconnects, the critical stress for void nucleation is estimated to be about 600MPa.[5]

B. Immortality Due to Resistance Saturation

In Al technology, refractory metal layers (TiN or Al_3Ti or both) are usually used as anti-reflection coatings on top of the Al lines. In addition, they are often used as under-layers too. These refractory metal layers are highly electromigration resistant and do not electromigrate even under conditions that would lead to copious electromigration of Al. Therefore, even if the critical stress for void nucleation is reached in Al, a void can grow to span the width and thickness of the Al layer without causing an open-circuit failure because current can shunt around the void through the refractory over- and under-layers. Once a void nucleates, it will continue to grow until the back stress balances the electron wind force. At this point, void growth will stop and the resistance of the interconnect segment will saturate. If the increase in resistance at saturation is lower than the failure criterion, then the line is considered immortal due to resistance saturation. The resistance at saturation is a function of the line length and the current density so that there is a critical minimum jL product that defines the range of this immortality, $(jL)_{crit,\Delta R}$. Resistance saturation was first demonstrated experimentally by Filippi and co-workers.[6,7] and for Al technology $(jL)_{crit,\Delta R}$ is about 4000A/cm.[6]

C. Probabilistic Immortality in Short Cu Lines

A number of investigations on the effects of decreasing line length on the reliability of Cu-based interconnects have been carried out. Ho *et. al* reported that M2-type interconnects of

length L=90μm, when stressed at a current density j of 1.0MA/cm^2, do not fail, so that $(jL)_{crit.}$>9000A/cm.[8] Hau-Riege found that for 10.5μm-long M1-type interconnects, the probability of failure drops dramatically for 10.5μm-long lines tested at 2.0MA/cm^2, compared to longer lines tested at the same current density.[9,10] This suggests that the $(jL)_{crit,nuc}$ *is less* than 2100A/cm, since even below this product, some lines still fail. However, as will be argued below, due to the fundamental difference in failure mechanisms between M1 and M2 type interconnects,[11] while the (jL) value reported by Hau-Riege corresponds to a upper bound for $(jL)_{crit.,nuc.}$, the (jL) value reported by Ho *et. al* corresponds to $(jL)_{crit.,\Delta R}$ for Cu.

In current Cu-technology, Si_3N_4, an electrical insulator, is used as an inter-level diffusion barrier and as a capping layer for interconnects. Therefore, in M1 type interconnect structures, even when a low-volume void forms at a via, it can cause an open circuit failure if it spans the bottom of a via as shown in Figure 2(a). This is because the void will block the current flow since the Si_3N_4 layer cannot shunt current as the refractory metal layers do in Al technology. Also, the Si_3N_4 layer provides sites for relatively easy void nucleation, and contributes to the low stress needed for void nucleation in Cu.[11] As a result, in M2-type interconnect structures, voids that nucleate and grow at the Cu/Si_3N_4 interface, must grow to span the line and the refractory metal liner must fail for line to fail. See Figure 2(b). Thus, in M1-type interconnects true immortality requires that the conditions for void nucleation not being reached,[11] while in M2-type structures, true immortality only requires that the electron wind force not exceeding the back stress, which is equivalent to the resistance saturation scenario in Al interconnects.

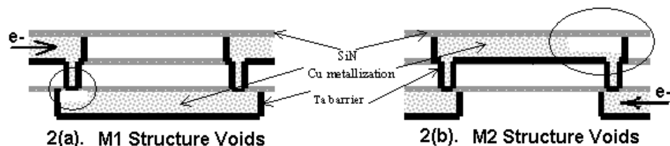

Fig. 2. (a) Formation of a mall fatal void directly below the via in M1-type structures. (b) Formation of a large void at the Cu/Si_3N_4 top interface in M2-type structures.

Hau-Riege's reported $(jL)_{crit.}$ value describes the probabilistic range for immortality due to void-growth saturation in M1-type structures, and constitutes an upper limit for $(jL)_{crit,nuc}$. Ho *et. al* reported a $(jL)_{crit.}$ determined for M2-type structures, giving a value for $(jL)_{crit,\Delta R}$ for these structures. This value for M2-structures may be deterministic. However, for M1 structures, only (jL)crit.nuc is deterministic. The probabilistic nature of $(jL)_{crit,\Delta R}$, in Cu, which contrasts with is deterministic nature in Al, is a consequence of the relative ease of void nucleation in current Cu technology, and because of the wide range of void volumes that can be tolerated or can be fatal, depending on the void shape and location. The net result is that the (jL) product for true immortality for current Cu technology is smaller than that for Al technology.

We find that for M1 structures, as the line length is decreased, the median-time-to-failure and the probability of immortality begins to increase at a (jL) product of 10000A/cm for the Sematech samples and 5000A/cm for the IME samples. These (jL) products suggest that void nucleation is highly probable inside the line, since it is much higher than the upper bound for $(jL)_{crit,nuc}$ reported by Hau-Riege. Therefore, majority of the structures failed. However, the (jL) products are near the range of the $(jL)_{crit.,\Delta R}$ reported by Ho *et al*. This fact suggests that immortality could exist as well due to partially-spanned voids, i.e., the back stress balancing the electron wind force, if the void location is such that the bottom of the via is not blocked. See Figure 3. Therefore, a fraction of the short line structures did not fail.

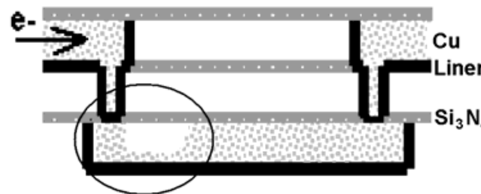

Fig. 3. Partially-spanning, non-fatal void formed inside M1-type structures, under the condition of $(jL) > (jL)_{crit.,\Delta R}$.

D. Probabilistic Immortality of Very Long Lines

For the very long interconnect segments considered in the current study, 800μm and 1000μm lines fabricated by IME and Sematech respectively, high values of the lognormal variance, σ, were observed and some lines did not fail after very long test times. The stress difference, $\Delta\sigma$, that should develop in 1000μm long lines tested at 2.0MA/cm^2, and 800μm long lines tested at 2.5MA/cm^2, should be approximately 5200MPa (taking Z^*=1[12] and ρ=4.0μΩ-cm at 350°C in equation 2). Clearly, this stress is more than sufficient to cause void nucleation if the refractory liners at the bottom of the vias block electromigration. The voids that form under these conditions would also grow to cause significant resistance increases. The apparent immortality observed in some of the long lines suggests that the refractory metal liners in one or both of the vias in these were not, in fact, blocking. We propose that the apparent immortality of a subpopulation of long lines is the result of EM-stress induced rupture of the Ta liners at the vias, as schematically illustrated in Figure 4. Rupture of the liners would allow continuous flow of Cu to and from the lead lines and contact pads, and these serve as large sinks and reservoirs for Cu[13]. However, liner rupture in the absence of reservoirs and sinks would contribute to a globally reduced reliability.

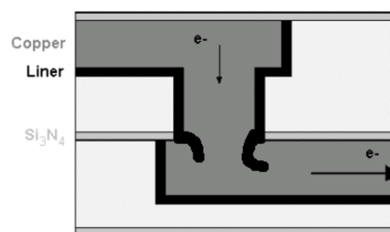

Fig. 4. Schematic view a ruptured liner at the bottom of a dual-damascene via, at the cathode end.

V. SUMMARY

We observe that the median time to electromigration-induced failure of via-to-via dual-damascene Cu lines is minimum for lines of intermediate length, and increases with decreasing *or* increasing line length. We observe that the variation of the lifetime is *also* a minimum for lines of intermediate length. Both long and short lines have the *possibility* of being "immortal", though due to fundamentally different mechanisms. While the probability that a line will be immortal increases with increasing or decreasing line length, the impact of these phenomena on reliability is unclear since chip-level reliability depends on the mechanism that leads to the earliest failures. One consequence of probabilistic immortality is that the reliability-limiting failure mechanism can be masked in tests on long and short lines. The phenomenology reported here for Cu interconnects is very different from what has been observed in similar experiments on Al-based interconnects. This points to the need for the development of new test and reliability assessment strategies for Cu-based interconnects.

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