Physics and Fabrication of Quasi-One-Dimensional Conductors

by

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Abstract

To facilitate research in Quantum Effect Electronics (QEE), it is necessary that a reliable fabrication technology be developed to maximize the likelihood that a particular device will exhibit observable quantum effects. By having a controlled process, it becomes possible to fabricate more demanding structures, and to experimentally explore new areas of device physics. In this thesis, the fabrication technology developed for the fabrication of quasi-one-dimensional (Q1D) conductors in the GaAs/AlGaAs system using x-ray lithography will be described, including modeling tools that have been developed to better understand some critical process steps. In addition, results will be analyzed with respect to simple theories that have been proposed over the past several years to describe such devices. These Q1D conductors are harnessed in a new type of Q1D planar resonant tunneling transistor (Q1D-PRESTFET) with one-dimensional emitter and collector, that is predicted to exhibit very strong resonances in electron transport.

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Table of Contents

Abstract 2

Acknowledgments 3

1 Introduction 10
- 1.1 QEE overview 12
- 1.2 Lithography overview 17

2 Theoretical Background 25
- 2.1 Theory of Q1D conductors 25
  - 2.1.1 Ballistic transport 25
  - 2.1.2 Diffusive transport 30
- 2.2 Theory of resonant tunneling 37

3 Modeling of X-ray Mask Patterning 45
- 3.1 Electron scattering cross-sections 47
- 3.2 Energy loss mechanisms 48
- 3.3 Model implementation 51
- 3.4 Modeling of resist development 54
- 3.5 Modeling results 55

4 Fabrication Technology 64
- 4.1 Nanolithography technology 64
  - 4.1.1 System considerations 64
  - 4.1.2 X-ray mask blank preparation 68
  - 4.1.3 X-ray mask fabrication 71
- 4.2 Modulation-doping 73
  - 4.2.1 Conventional HEMT 75
  - 4.2.2 Back-gated HEMT 78

4.3 Q1D conductor fabrication . . . 80
4.3.1 Conventional processing . . . 80
4.3.2 X-ray lithography of small samples . . . 82
4.3.3 Precise etching of GaAs . . . 83
4.4 Q1D-PRESTFET fabrication . . . 88

5 Measurements **91**
5.1 Mobility degradation during lithography . . . 91
5.2 Q1D conductor results . . . 96
5.3 Q1D-PRESTFET results . . . 101

6 Conclusions **104**

Appendix A Processing sequence **110**

Appendix B X-ray lithography of small samples **121**

Bibliography **128**

List of Figures

Figure 1.1 Evolution of minimum device size with time. 11

Figure 1.2 (a) Device schematic of prototypical QEE device, (b) potential seen by electrons when dots are loosely coupled, and (c) potential seen by electrons when dots are isolated. 13

Figure 2.1 Schematic diagram of ballistic one-dimensional conductor. 26

Figure 2.2 Convolution method for ballistic one-dimensional transport, including voltage broadening and thermal broadening. 28

Figure 2.3 Quantized conductance steps measured in a split-gate device showing the "quantum staircase" (from [30]). 29

Figure 2.4 Convolution method for the thermodynamic density of states and conductivity, including thermal broadening and impurity broadening. 32

Figure 2.5 Schematic of energy potential seen by electrons traveling along a Q1D conductor. 35

Figure 2.6 Summary of model for calculating the conductance of a diffusive Q1D conductor using the convolution method. 38

Figure 2.7 Conduction-band energy as a function of position for a double barrier resonant tunneling device for various applied voltages, along with typical current/voltage relationship showing resonance condition at V_1. 39

Figure 2.8 Transmission probability versus energy in direction perpendicular to a "sloppy" tunneling barrier. 40

Figure 2.9 Two-dimensional point source of electrons radiating onto a resonant tunneling double barrier. 41

Figure 2.10 Current versus Fermi energy for idealized resonant tunneling transistors with 3D, 2D, and 1D emitters and collectors.. 44

Figure 3.1 Top view of finished x-ray mask written using scanning-electron-beam lithography. The large pad areas (~20×20μm) were exposed at approximately twice the dose of the line. 46

Figure 3.2 Schematic illustration of electron energy versus distance traveled (after [42]). 49

Figure 3.3 Schematic of (a) small angle forward scattering and (b) long range backscattering of electrons. 56

Figure 3.4 Energy deposition at the surface and base of a 300nm freestanding film of PMMA on plating base. 57

Figure 3.5 Energy deposition at the base of a 300nm film of PMMA on plating base for substrates corresponding to freestanding PMMA, PMMA on a membrane, and PMMA on bulk silicon. 58

Figure 3.6 Modeled energy deposition in resist for the pattern shown in Figure 3.1, for various substrates. 59

Figure 3.7 Resist contours at 30 second intervals during development, for the energy deposition pattern corresponding to a freestanding film in Figure 3.6. 60

Figure 3.8 Resist contours at 30 second intervals during development, for the energy deposition pattern corresponding to a thin membrane in Figure 3.6. 61

Figure 3.9 Resist contours at 30 second intervals during development, for the energy deposition pattern corresponding to a bulk silicon substrate in Figure 3.6. 61

Figure 3.10 Modeled energy deposition for two 100nm lines separated by 100nm, on various substrates. 62

Figure 3.11 Resist contours are various times during development for the energy deposition pattern corresponding to a bulk silicon substrate in Figure 3.10. 63

Figure 4.1 (a) Schematic of x-ray lithography source used in this work. (b) Close up of proximity gap. 65

Figure 4.2 Attenuation of x rays for materials commonly used in x-ray mask fabrication, as a function of x-ray wavelength. 67

Figure 4.3 X-ray mask blank fabrication sequence. 69

Figure 4.4 Schematic of finished x-ray mask, along with interferogram showing the flatness of the mask membrane. 70

Figure 4.5 (a) Schematic of electron-beam patterning of an x-ray mask. (b) Electroplating of gold x-ray absorbers using developed resist as a mold. 72

Figure 4.6 Thick electroplated gold patterns on master x-ray masks after patterning by electron-beam lithography for (a) etch mask used to define Q1D wires, (b) tunnel-gate mask to define tunneling barriers for the Q1D-PRESTFET, (c) sample grid-gate patterns used to fabricate grid-gate HEMTs, and (d) gate pattern for deep-submicron short-channel MOSFET. 74

Figure 4.7 (a) Typical layer structure for modulation-doped GaAs/AlGaAs HEMT. (b) Energy band diagram for (a). 76

Figure 4.8 Potential seen by electrons at the plane of the two-dimensional electron gas when a lateral superlattice potential is applied to HEMT structures with different spacer thicknesses. 78

Figure 4.9 Measured electron density versus back-gate bias for various top-gate voltages, for a back-gated HEMT. 80

Figure 4.10 (a) Schematic overview and (b) schematic cross-section of completed Q1D device. 81

Figure 4.11 (a) Exposure fixture for conformable x-ray lithography on samples smaller than the x-ray mask membrane diameter. (b) Schematic showing x-ray mask membrane conforming around a small sample. 84

Figure 4.12 Modeled confining potential seen at the plane of the electron gas for the device shown in Figure 4.10 for various etch depths. 85

Figure 4.13 Image in Linnik interferometer during etching (a) before and (b) after initial enhancement. 86

Figure 4.14 Phase of fundamental spatial frequency in Figure 4.13 as function of position along the x direction. 87

Figure 4.15 Scanning electron micrograph of typical Q1D conductor device, with many parallel Q1D conductors. 88

Figure 4.16 (a) Overview, (b) cross-section, and (c) potential seen by electron in Q1D-PRESTFET. Note that this device is an enhancement mode device, so tunnel gate must be biased positively to turn on the Q1D electron gas. 89

Figure 4.17 Scanning electron micrograph of typical Q1D-PRESTFET device, with many parallel Q1D conductors and tunnel gate. 90

Figure 5.1 (a) Electron mobility and (b) electron density before and after electron-beam irradiation as a function of temperature. 93

Figure 5.2 (a) Electron mobility and (b) electron density before and after x-ray irradiation as a function of temperature. 94

Figure 5.3 Calculated energy deposition in a GaAs substrate as a function of depth, with and without a PMMA coating, for a 50keV electron beam.. 96

Figure 5.4 Measured conductance for a Q1D device of the type shown in Figure 4.15. 97

Figure 5.5 Schematic of potential seen by electrons in Figure 5.4 (arrows indicate direction of current flow).. 98

Figure 5.6 Temperature dependance of the transconductance of a Q1D device. 98

Figure 5.7 Length dependence of the transconductance of a Q1D device. 99

Figure 5.8 Conductance of a Q1D device for various drain-source biases.. . . . 100

Figure 5.9 (a) Schematic cross-section, and (b) potential seen by electron in Q1D-PRESTFET. 102

Figure 5.10 Potential seen at the plane of the two-dimensional electron gas for tunnel gates with various pitches.. 103

Chapter 1
Introduction

As the density of electronic systems continues to increase, there is a consensus that conventional electronics are rapidly approaching fundamental limits that may not be possible to overcome. Because of these concerns, there has been significant interest in recent years in basic research into potential successor technologies. Some characteristics that would be desirable in an ideal successor technology include having critical operations enhanced by smaller dimensions, information represented by tokens that do not suffer from statistical limitations as devices scale, and easy integration into new system architectures based on massively parallel, distributed designs, in order to circumvent the interconnect bottleneck. One technology that can potentially meet all these requirements is Quantum Effect Electronics (QEE) [1].

The development of computational systems during the past century has been characterized by the continued reduction of minimum feature sizes, as shown in Figure 1.1. As each class of computation device began to run into physical limits, a new paradigm of computation emerged to overcome these physical limitations. Currently, it is far from clear what direction the successor to very large scale integration (VLSI) will take. In recent years, there has been intense

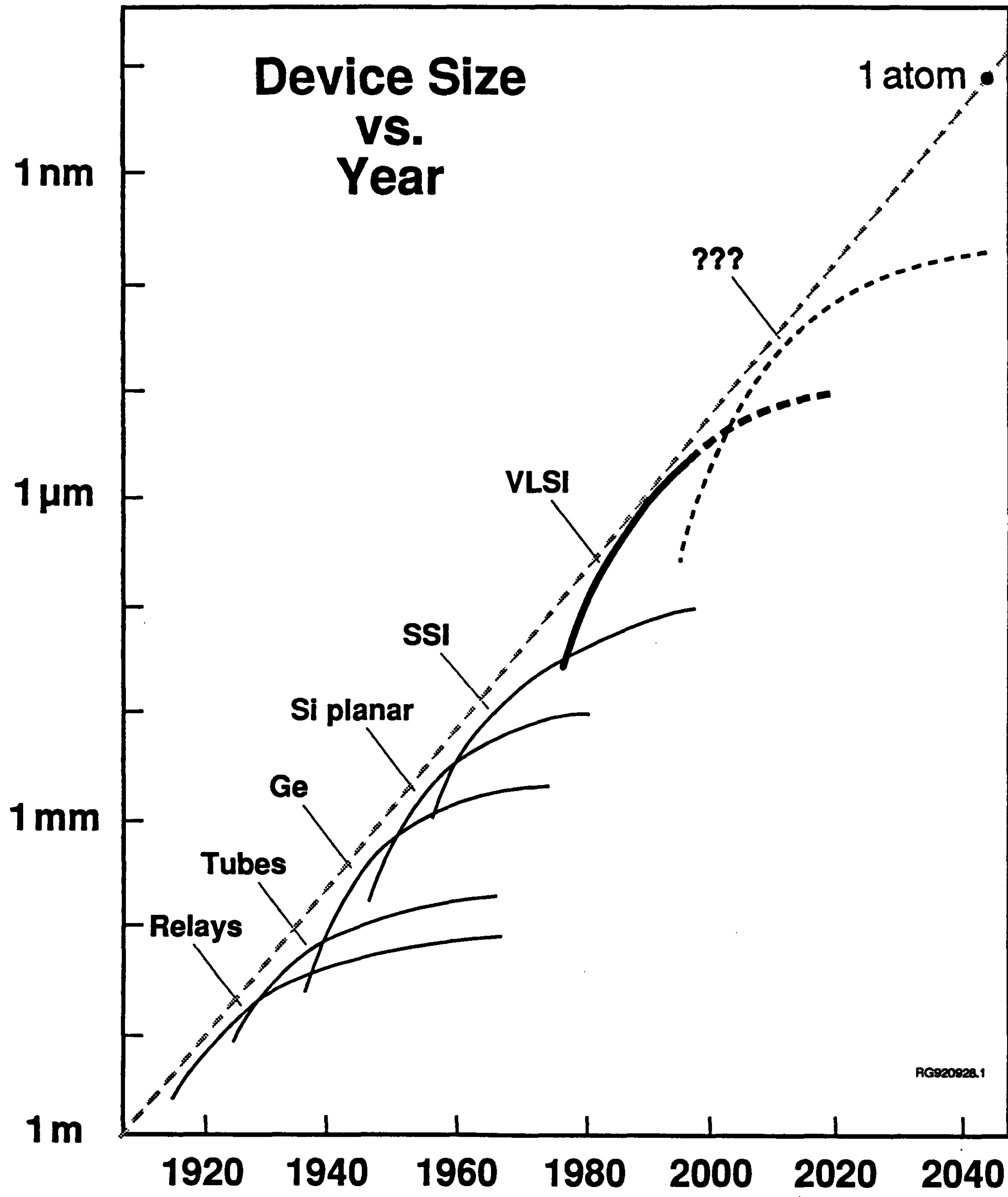


Figure 1.1 Evolution of minimum device size with time.

research activity into electronic systems based on materials other than silicon (such as gallium-arsenide and indium-phosphide) [2], computation harnessing interactions between light and matter [3,4], computations based on superconductivity [5], and computation based on the quantum nature of matter [1]. It is this last alternative that is considered in this work.

1.1 QEE overview

Typically, QEE refers to electronic devices whose operation is dominated by the quantum nature of matter. These devices usually exploit reduced dimensionality in order to enhance quantization effects, and thus require critical device dimensions to be less than the electron coherence length. This places considerable stress on the fabrication technology, as well as the materials technology. Examples of QEE devices include resonant tunneling structures [6,7], arrays of zero-dimensional quantum dots (0D) [8], and one-dimensional conductors (ballistic [9,10] and diffusive [11]).

A prototypical QEE device is shown schematically in Figure 1.2. In this device, a very fine pitch grid gate is used to electrostatically define a very dense array of coupled zero-dimensional quantum dots, as shown schematically in Figure 1.2 (b). By adjusting the voltage on the gate, these quantum dots can be isolated from one another, as shown in Figure 1.2 (c). With a grating of pitch 200 nm, each dot is electrically on the order of 30 nm in diameter, with a density of 2.5×10^9 dots/cm^2. Moreover, optical measurements on this system [12] have shown that there are ~5 electrons per dot, indicating that it may be feasible to use an electron as an information token. By controlling the degree of coupling between adjacent wells, it is

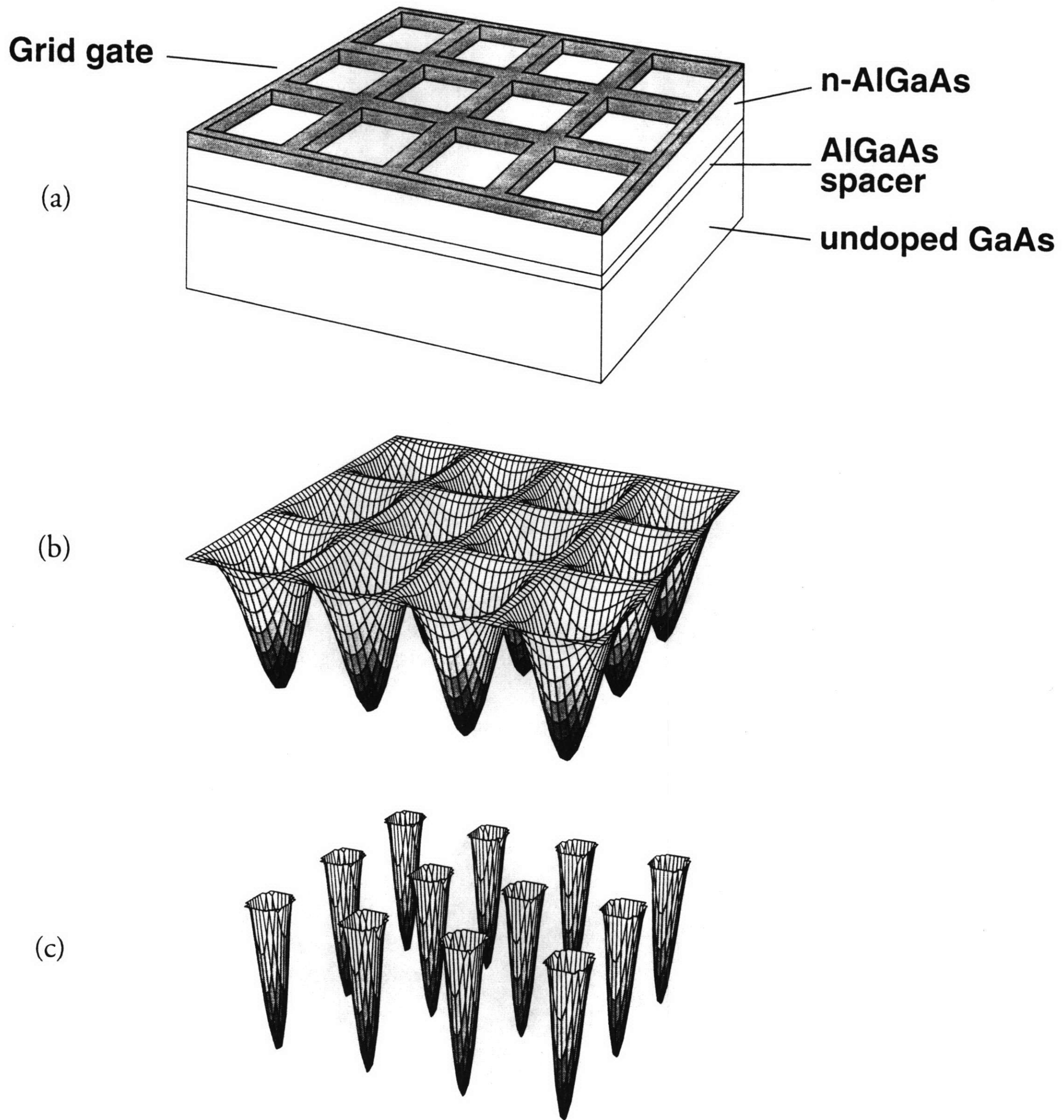


Figure 1.2 (a) Device schematic of prototypical QEE device, (b) potential seen by electrons when dots are loosely coupled, and (c) potential seen by electrons when dots are isolated.

conceivable that near neighbor communication via wave function overlap can be harnessed, eliminating the need for wiring.

Although there have been few proposals for computation systems based on QEE, the nature of these devices seems to make them good candidates for computation using cellular automata [13] which rely on only near neighbor interactions. Also, there has been a significant amount of effort made to develop logic families that rely on multi-state logic, in order to enhance the functionality of individual devices [14].

However, there are many practical problems that must be addressed when evaluating QEE as a potential successor technology to VLSI. First and foremost, current fabrication and materials technologies are not sufficiently advanced to permit fabrication of devices with characteristics that are usable at room temperature, while at the same time being externally controllable. For example, resonant-tunneling diodes have been reported that have very impressive non-linearities even at room temperature [15]. Unfortunately, these are two-terminal devices, with characteristics critically dependant on single-atomic layer control during fabrication. An alternative three terminal device, the planar resonant-tunneling field-effect transistor (PRESTFET) [7], allows external electrostatic control of the device's non-linearities, but requires operation at temperatures below 10K.

Despite these practical concerns, it is expected that as fabrication and materials technologies becomes more advanced, quantization effects will persist to higher temperatures, and that devices will become more immune to process variations. What is not currently clear is the type of computational system these devices will be used in. Some issues to consider include:

- *What compelling advantage does the new paradigm offer?*
  In order to supplant conventional electronics, a new paradigm of computation must have a compelling advantage in order to motivate a conversion to the new technology. In order to properly evaluate the relative strengths of different technologies, it is important to extrapolate the performance gains to conventional electronics if the same highly advanced fabrication and materials technologies required for the new technologies were available (e.g., how well will conventional CMOS-based logic perform with minimum feature sizes well below 100 nm, and operating temperatures below 100 K?).

- *Are there identifiable state variables?*
  In order to interpret the results of a computation, it is necessary to attribute meaning to the resulting state of the system. For conventional digital logic, this usually means assigning a binary value of 1 to "on" devices, and a binary value of 0 to "off" devices. A computation system based on QEE will require clearly identifiable states that can be interpreted as a particular type of information token.

- *How predictable are interactions?*
  Computation usually is interpreted as tokens interacting to give a meaningful result. In order to have a reliable computation, the interactions between the tokens ought to be sufficiently predictable that the computation gives the same result, with a very low error rate.

- *How can tokens be refreshed?*
  In order for tokens to be stable over time, it is often necessary to add energy to the system to refresh the devices responsible for maintaining the token. If there is no way to refresh tokens, more likely than not, the second law of

thermodynamics will cause the system to run "down hill" and decay with time, causing a loss of information content.

- *How to initialize system and how to get results out?*
  To do useful computation, it is necessary to initialize the system with tokens to be processed, and afterwards, read out the processed tokens as a result. It is this necessity that has led to the interconnect bottleneck that is beginning to plague conventional electronics. Many proposals for alternate systems extol the virtues of local computation to avoid the necessity of interconnects. However, most of these proposals do not address the fundamental question of how the system will be initialized, and how the final results will be read out.

- *How to design?*
  Perhaps the most important issue to consider is how amenable the new paradigm is to design. Computation systems today are of sufficient complexity that it is impractical to approach designing a system without specifying components at a much higher level of abstraction than fundamental devices (i.e., half-adders as opposed to individual transistors or even AND gates). Systems which require a very large number of devices to work coherently simply do not lend themselves to design, and hence have little practical utility.

Even with all these concerns, computation based on quantum phenomena is sufficiently compelling and holds enough promise to warrant basic, exploratory research. Research in QEE has led to many important advances in the understanding of mesoscopic transport, and has motivated a great deal of thinking about the fundamental nature of computation and information. Perhaps more importantly from a practical standpoint, QEE has served as a

technology driver for areas critical to the semiconductor industry, including lithography and materials technologies.

For this thesis, emphasis has been placed on developing the fabrication technology necessary to enable basic, exploratory research in quasi-one-dimensional (Q1D) conductors, while making an effort to ensure that the same technology can be applied to the manufacture of more conventional electronic systems. By developing a controlled process, it becomes possible to harness these Q1D conductors in a new type of Q1D planar resonant tunneling field-effect transistor (Q1D-PRESTFET) with one-dimensional emitter and collector, that has been predicted to exhibit very strong resonances in electron transport [16]. At the same time, the manufacturing technology which is being developed can be directly applied to the manufacture of more conventional devices, such as deep-submicron MOSFETs.

1.2 Lithography overview

It is clear from Figure 1.1 that there has been continual pressure on engineers to develop tools that are capable of defining finer and finer features. The primary motivator for this trend has been the drive to increase the computing ability of integrated circuits by decreasing the area needed for individual transistors, and hence, increasing the density of functional units on a single chip. As transistor densities continue to increase, there is an ever increasing need for lithography tools that can reliably pattern features well below 1 μm, to within very tight tolerances, and with no defects.

For the microelectronics revolution of the past several decades, the primary means of artificially patterning substrates during manufacturing has been optical lithography, where ultraviolet

(UV) light is used to chemically alter the solubility of a polymer film (resist). The resist is then used to selectively mask certain areas during subsequent processing steps. Initially, patterns were defined by placing a glass mask with chromium patterns in contact with the substrate, and illuminating with an appropriate source (proximity printing).

However, as feature sizes continued to decrease and tolerances became more strict, the industry began to move to optical projection printing, where a reduction camera is used to image a mask on the substrate. For these systems, the ultimate resolution is diffraction limited to

$$p_{\min} = \frac{\lambda}{2NA} , \tag{1.1}$$

where $p_{\min}$ is twice the minimum resolvable feature size, λ is the wavelength of light used, and NA is the numerical aperture of the lens (<1 for exposure in air).

The need for finer and finer minimum feature sizes has driven the wavelength farther and farther into the UV range, to the point where advanced research in optical lithography is being done with wavelengths as low as 193 nm, using ArF excimer lasers [17]. As optical lenses are not ideal, the move to shorter wavelengths has greatly increased the costs of reduction systems, which not only require many lenses to correct for aberrations, but must also be manufactured to tolerances that are a small fraction of the wavelength of intended use.

Even with ideal optics, manufacturing at deep-UV wavelengths can be problematic for another reason. Typically, the spatial extent over which an optical system can properly focus an image (the depth of focus, or DOF) is given by

$$DOF = \pm \frac{\lambda}{2NA^2} \quad , \tag{1.2}$$

requiring that all substrates be planar to within several wavelengths. Not only does this requirement restrict substrate types and place great stresses on sample preparation for lithography (planarization), but it also requires that multilayer resist systems be used because it is difficult to pattern resist with a thickness that is comparable to the DOF. These factors greatly increase the complexity of the process, and hence the cost of manufacturing. Moreover, because temperature variations alter the refractive properties of the lenses, modern optical stepper must dynamically adjust the focus of the lenses during an exposure in order to compensate for temperature variations due to heating from the light source.

For sub-100 nm lithography, there are currently several candidates:

- *Scanning electron-beam lithography (SEBL)*

  In SEBL, a focused beam of high energy electrons is used to write a pattern in an electron-beam sensitive resist [18]. Usually, patterns are written in a raster pattern. In commercial systems, electron energies are typically on the order of 50 keV, with minimum feature sizes on the order of 30 nm. Unfortunately, pattern generation is a serial process and thus very time intensive. Some variations on SEBL have been implemented to increase throughput, but these have been limited to gains on the order of 10–100 (not sufficient to become viable for manufacturing).

  Because electrons are light particles, they tend to scatter within the substrate and can return to expose resist in remote areas, leading to the proximity effect. (SEBL and the proximity effect are discussed in much greater detail in Chapter 3.)

- *Focused-ion-beam lithography (FIBL)*

  FIBL is very similar to SEBL, except a focused beam of heavy, high energy ions are used rather than electrons [19]. Because of the high mass of the ions, patterning done using FIBL is mostly immune from proximity effects. Unfortunately, there are many substrates that are damaged by the high-energy ions, making FIBL unsuitable for some applications. Moreover, sources and optics for FIBL are not currently as advanced as those used in SEBL, making the technology more problematic.

- *Proximity x-ray lithography*

  First demonstrated in 1971 [20], proximity x-ray lithography is a return to proximity printing, where a soft-x-ray source ($0.5\,nm < \lambda < 4\,nm$) is used rather than a UV source. These wavelengths are certainly compatible with sub-100nm lithography. More importantly, there is the added benefit of absorption without scattering at these wavelengths. This is because most materials have an index of refraction ~1 at the soft-x-ray wavelengths, making x-ray lithography unaffected by substrate composition and topography. This coupled with a very large depth of focus permits exposures with extremely vertical side walls with single layer resist systems, independent of resist thickness or substrate composition. Because proximity printing is essentially a shadow casting configuration, there is no need for highly sophisticated optical elements with large fields of view. From a manufacturing perspective, x-ray lithography is a parallel process, making it suitable for commercial environments, where throughput is critical.

  Unfortunately, mask fabrication for x-ray lithography is extremely challenging for several reasons. First, because proximity printing is a shadow casting technique, absorbers on an x-ray mask must be patterned

at the same size that is ultimately desired on the substrate. This is in contrast with optical projection lithography, where mask features are usually 5–10 times larger than the ultimate feature size. Second, working with the soft-x-rays requires the use of extremely thin support membranes for the mask patterns. This is to avoid attenuation of the x rays by the mask itself. Typically, x-ray masks are on the order of one to several microns thick, while being tens of millimeters in diameter. The thinness (and hence perceived fragility) of the membranes is of great concern, since x-ray lithography requires the mask/substrate gap to be on the order of ~10μm. In a production setting, where it is required that a mask rapidly step across the surface of a wafer, the proximity of the mask to the substrate is a serious concern.

From a QEE perspective, a suitable lithography technology must have the requisite resolution, be fairly reliable, be able to work with the odd-sized substrates typically used in research, and not adversely affect the advanced materials that are typically required for QEE work. Of the techniques cited above, SEBL is the most commonly used in the fabrication of QEE devices, primarily because its superior resolution and flexibility. However, there have been some indications that high-energy electrons may adversely affect some of the materials commonly used in QEE research [21,22]. Also, the proximity effect necessitates the use of thin resist in order to resolve the finest features. The thickness of resist limits the thickness of metal that may be deposited, often making it difficult to reliably manufacture devices that are immune from stray-electrostatic charge.

From a manufacturing perspective, the primary issue is cost effectiveness. This typically means a system that is capable of reliably and repeatably patterning various substrates with high

throughput. Also, the systems needs to be able to maintain high precision over very large areas, with minimal distortion. Finally, an ideal system will offer a high degree of process latitude, making the manufacturing process immune from minor fluctuations in such parameters as exposure time and environmental factors (e.g. humidity and temperature). Of the viable technologies for sub-100nm lithography, the only one that can realistically meet these criteria is x-ray lithography, primarily due to the parallel nature of x-ray lithography, the properties of materials at x-ray wavelengths, and the simplicity of proximity printing.

For this work, the decision was made to develop the x-ray lithography technology as a means of fabricating QEE devices. During the course of this work, much of the same technology has been applied to the fabrication of deep-submicron MOSFETs [23], optoelectronic devices [24], and devices for research into magneto-optics [25]. In many ways, the research into QEE has become a technology driver that is benefitting research in other areas.

In this thesis, the fabrication technology developed for the fabrication of QEE devices will be described. Specifically, the fabrication of quasi-one-dimensional (Q1D) conductors in the GaAs/AlGaAs system using x-ray lithography will be used as a demonstration of the capabilities of the new technology. These techniques for repeatably fabricating Q1D conductors in a highly controlled way will ultimately be harnessed in the fabrication of a new type of Q1D planar resonant tunneling transistor (Q1D-PRESTFET) with one-dimensional emitter and collector, that has been predicted to exhibit very strong resonances in electron transport.

In Chapter 2, a brief introduction will be given to the theory of transport in one-dimensional systems in both the diffusive and ballistic regimes. Also, a theoretical basis for the predicted strong resonances in the Q1D-PRESTFET will be presented.

In Chapter 3, a detailed model will be presented for the patterning of x-ray masks using SEBL. By taking into account both exposure effects and development effects, it will be demonstrated that there is a fundamental benefit to patterning x-ray masks using SEBL and then using x-ray lithography to pattern samples, rather than using SEBL directly.

Chapter 4 will present a detailed account of the fabrication technology developed and used in this thesis, including the fabrication of x-ray masks and the techniques that have been developed to permit the use of standard x-ray masks to expose nonstandard substrates. Also, the processing technology that has been developed to fabricate Q1D conductors will be presented, including a high-precision etching technique for GaAs that has a depth resolution of less than 1 nm. This etching technology will be shown to be the basis for reliably fabricating Q1D conductors and Q1D-PRESTFETs.

Chapter 5 includes the experimental results of this work, including the finding that electron-beam lithography may significantly damage substrates typically used in QEE research, while x-ray lithography does not. The lack of damage with x-ray lithography is an important justification for the development of a fabrication technology that is suitable for the device geometries and substrates typically used in QEE research. In addition, measurements of conductance modulation in Q1D conductors will be presented along with a discussion of the preliminary efforts that have been made to fabricate Q1D-PRESTFETs.

Finally, some conclusions will be presented in Chapter 6, along with a summary of ongoing work.

Chapter 2
Theoretical Background

2.1 Theory of Q1D conductors

2.1.1 Ballistic transport

When the length of a given device is much less than either than elastic or inelastic scattering length of an electron in a particular device geometry, the electron transport in the device is described as being ballistic. In the ballistic limit, Landauer's formula [26,27] can be applied to calculate the conductivity of the device.

For the one-dimensional device shown schematically in Figure 2.1, the conductivity as a function of energy, applied voltage, and temperature can be expressed as [28]

$$I_{1d}(E,V,T) = e\int v_{1d}(\varepsilon)T_{1d}(\varepsilon,V)N_{1d}(\varepsilon)[f_{left}(\varepsilon-E,T) - f_{right}(\varepsilon-E,T)]d\varepsilon \qquad (2.1)$$

where e is the electronic charge, v_{1d} is the group velocity of electrons traveling from the left to the right contact, $T_{1d}(E,V)$ is the transmission coefficient through the active region of the device, N_{1d} is the one-dimensional density of states for electrons moving from the left to the

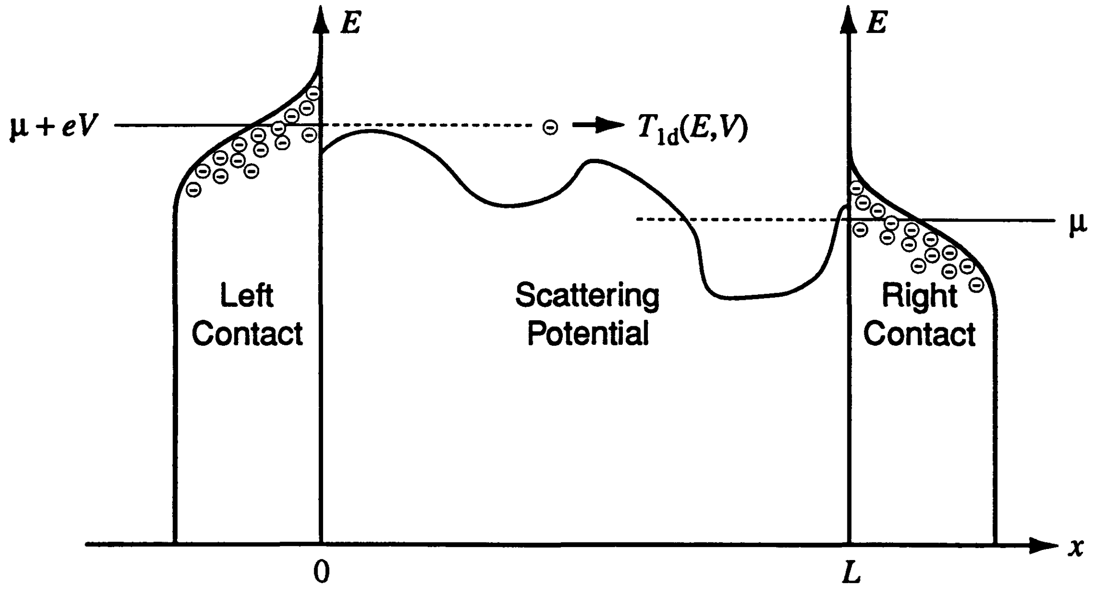


Figure 2.1 Schematic diagram of ballistic one-dimensional conductor.

right contact, and $f_{\text{left,right}}(E,T)$ is the distribution of electron in the left and right contact respectively.

For one-dimensional electrons, the product of the electron group velocity and the electron density of states is given by

$$\begin{aligned} v_{1\text{d}}(E)N_{1\text{d}}(E) &= \left[\frac{\left|\frac{dE}{dk}\right|}{\hbar}\right]\left[\frac{1}{\pi\left|\frac{dE}{dk}\right|}\right] \\ &= \frac{1}{\pi\hbar} \quad . \end{aligned} \tag{2.2}$$

Following the derivation of Bagwell and Orlando [29], if we assume that the distribution of electrons in the contacts is described by the Fermi-Dirac distribution, the electron distribution in the contacts can be written as

$$f(E-\varepsilon,T)=[1-\theta(E-\varepsilon)]\otimes f'(E,T) \quad , \tag{2.3}$$

where $\theta(E)$ is the unit step function,

$$f'(E,T)\equiv-\frac{df}{dE}(E,T)=\frac{1}{4kT}\operatorname{sech}^2\left[\frac{E}{2kT}\right] \quad , \tag{2.4}$$

and convolution is defined by

$$\begin{aligned} f(x)\otimes g(x) &= \int_{-\infty}^{+\infty} f(x-x')g(x')dx' \\ &= \int_{-\infty}^{+\infty} f(x')g(x-x')dx' \quad . \end{aligned} \tag{2.5}$$

If the potential V is applied to the left contact, the difference in the distribution of electrons in the contacts in Equation (2.1) can be written as

$$f(\varepsilon-(E+eV),T)-f(\varepsilon-E,T)=\{\theta(\varepsilon-E)-\theta(\varepsilon-(E-eV))\}\otimes f'(E,T) \quad , \tag{2.6}$$

separating out the effects of finite voltage and finite temperature on the distribution of electrons in the contacts into independent functions.

Equation (2.1) can now be rewritten as

$$I_{1d}(E,V,T)=\frac{e}{\pi\hbar}T_{1d}(E,V)\otimes W(E,V)\otimes f'(E,T) \quad , \tag{2.7}$$

where $W(E,V)=[\theta(E+eV)-\theta(E)]$ is the voltage broadening function. Equation (2.7) is depicted graphically in Figure 2.2.

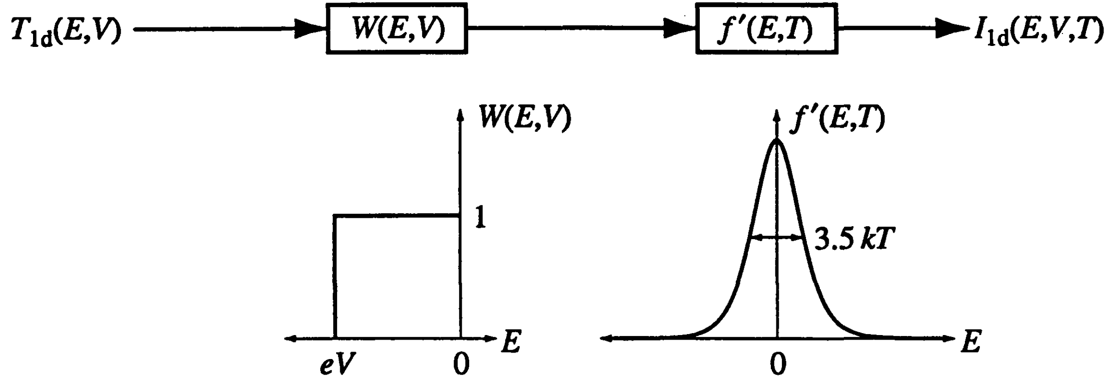


Figure 2.2 Convolution method for ballistic one-dimensional transport, including voltage broadening and thermal broadening.

In the case of a ballistic Q1D conductor, electrons are confined to discrete energy subbands as they travel through the conductor. Because it is assumed there is no scattering in the wire, the contribution of each subband can be considered individually. For an energy subband at E_1, the one-dimensional transmission coefficient can be written as $T_{1d}(E,V)=\theta(E-E_1)$.

In the limit of small V and low temperature, the current in the device is then given by

$$I_{1d}(E,V) = \frac{e^2}{\pi\hbar}\theta(E-E_1) \quad , \tag{2.8}$$

where $\frac{e^2}{\pi\hbar}$ is the quantum contact resistance [9,10]. Similarly, the higher energy subbands contribute $\frac{e^2}{\pi\hbar}$ of conductance, leading to the familiar "quantum staircase" shown in Figure 2.3.

For separable potentials, Equation (2.1) can be generalized to higher dimensionality systems using the relations

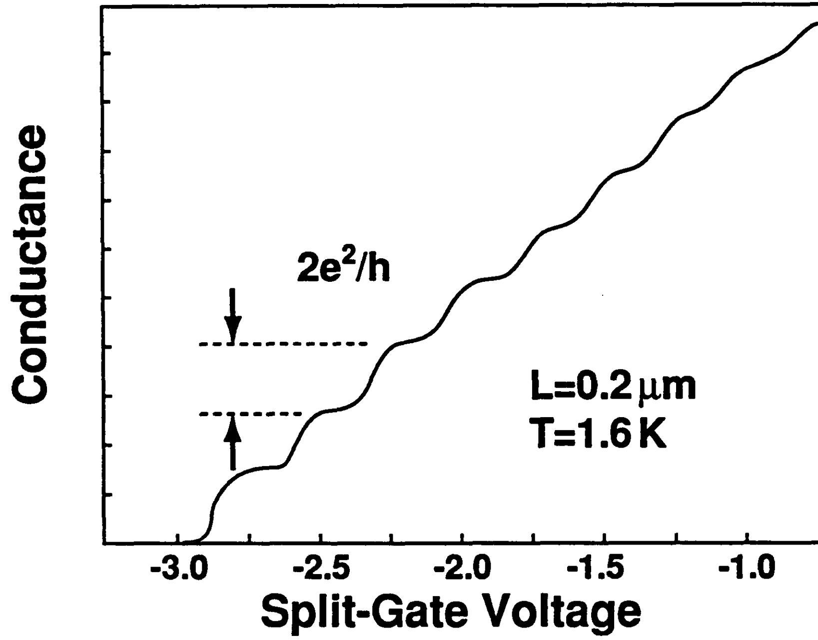


Figure 2.3 Quantized conductance steps measured in a split-gate device showing the "quantum staircase" (from [30]).

$$J_{2d}(E,V,T) = I_{1d}(E,V,T) \otimes \frac{1}{2} N_{1d}^{x}(E) \tag{2.9}$$

and

$$J_{3d}(E,V,T) = I_{1d}(E,V,T) \otimes \frac{1}{2} N_{1d}^{x}(E) \otimes \frac{1}{2} N_{1d}^{z}(E) \quad . \tag{2.10}$$

In these equations, the factor of one-half is included to avoid counting spin states twice. These relationships will be discussed further in Section 2.2 as part of the discussion of resonant tunneling in various dimensions.

2.1.2 Diffusive transport

When the length of the active region of a device becomes many times both the elastic and inelastic scattering length of electrons within the device, transport is said to be diffusive. In this regime semiclassical methods can be used to calculate the conductivity of electrons [31,32].

Semiclassically, the conductivity tensor at zero temperature is given by

$$\sigma^{ij}(E) \equiv e^2 v_i(E) v_j(E) \tau(E) N(E) \ , \tag{2.11}$$

where v is the electron group velocity, τ is the electron scattering time, and N is the electron density of states. At finite temperatures, Equation (2.11) becomes

$$\sigma^{ij}(E,T) = e^2 \int_{-\infty}^{+\infty} v_i(\varepsilon) v_j(\varepsilon) \tau(\varepsilon) N(\varepsilon) f'(E-\varepsilon,T) d\varepsilon \ , \tag{2.12}$$

where $f'(E,T)$ is the derivative of the Fermi-Dirac distribution as defined before.

Recasting Equations (2.11) and (2.12), the temperature dependent conductivity can be written as

$$\sigma^{ij}(E,T) = \sigma^{ij}(E) \otimes f'(E,T) \ , \tag{2.13}$$

separating out the thermal component of the conductivity into the thermal broadening function, which has a full width at half maximum of $3.5kT$.

Similarly, the thermodynamic density of states can be shown to be

$$N(E,T) \equiv \frac{\partial n(E,T)}{\partial E} = \int_{-\infty}^{+\infty} N(\varepsilon) f'(\varepsilon - E, T) d\varepsilon$$
$$= N(E) \otimes f'(E,T) \quad , \qquad (2.14)$$

where n is the electron density at finite temperature T, given by

$$n(E,T) = \int_{-\infty}^{+\infty} N(\varepsilon) f(\varepsilon - E, T) d\varepsilon \ . \qquad (2.15)$$

Additionally, because inelastic scattering leads to phase randomizations in the diffusive regime, energy levels are broadened by the impurity broadening function [33]

$$A(E,\tau) = \frac{1}{\pi} \frac{\hbar/2\tau}{E^2 + (\hbar/2\tau)^2} \qquad (2.16)$$

which has a full width at half maximum of $\frac{\hbar}{\tau}$.

When the effects of impurity broadening are included in Equation (2.12), the full conductivity tensor can be written as

$$\sigma^{ij}(E,T,\tau) = \sigma^{ij}(E) \otimes f'(E,T) \otimes A(E,\tau) \quad , \qquad (2.17)$$

and the full expression for the density of states written as

$$N(E,T,\tau) = N(E) \otimes f'(E,T) \otimes A(E,\tau) \quad . \qquad (2.18)$$

This convolution method is shown schematically in Figure 2.4.

A clear consequence of casting the conductance of diffusive devices in terms of convolutions with a thermal and impurity broadening function is the establishment of observability criteria

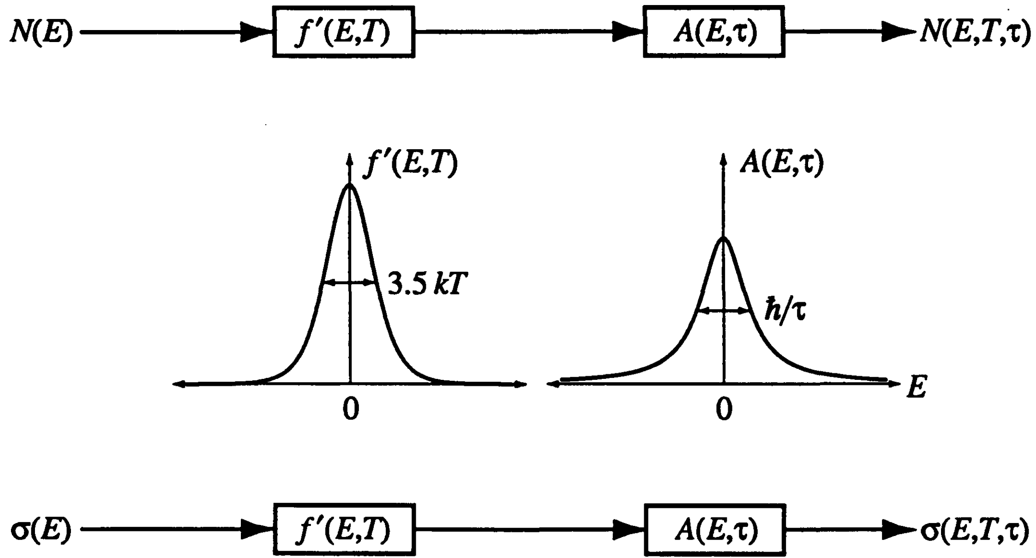


Figure 2.4 Convolution method for the thermodynamic density of states and conductivity, including thermal broadening and impurity broadening.

for the manifestation of quantum effects. In order to be observable, structure in the conductance must have a sufficiently large energy range ΔE, such that $\Delta E > kT$ and $\Delta E > \frac{\hbar}{\tau}$. For example, a ΔE of 10 meV corresponds to a thermal broadening equivalent to an electron temperature of 33 K, and an impurity broadening equivalent to a two-dimensional electron mobility of 1700 cm^2/Vs in GaAs.

For a strictly one dimensional conductor, where electrons are free to move only in the y direction, the conductance can be written as

$$\sigma_{1d}^{yy}(E) = e^2 v_y^2(E) \tau(E) N_{1d}^{y}(E) \quad , \tag{2.19}$$

where group velocity for the electrons is given by

$$
\begin{aligned}
v_y(E) &= \frac{1}{\hbar}\frac{\partial E_{1d}^{y}}{\partial k_y} \\
&= \sqrt{\frac{2E}{m}} \quad ,
\end{aligned}
\tag{2.20}
$$

the dispersion relation for one dimensional electrons is given by

$$
E_{1d}^{y} = \frac{\hbar^2 k_y^2}{2m} \quad ,
\tag{2.21}
$$

and the one-dimensional density of states for electrons is given by

$$
\begin{aligned}
N_{1d}^{y}(E) &= \frac{2}{\pi}\left|\frac{\partial E_{1d}^{y}}{\partial k_y}\right|^{-1} \\
&= \frac{1}{\pi\hbar}\sqrt{\frac{2m}{E}} \quad .
\end{aligned}
\tag{2.22}
$$

The scattering time from state k to k' is given by Fermi's Golden Rule as

$$
\frac{\hbar}{\tau_{k,k'}} = 2\pi n_{\mathrm{imp}} |\langle k'|V|k\rangle|^2 N(E) \quad ,
\tag{2.23}
$$

where n_{imp} is the density of scatterers, $N(E)$ is the density of states at state k, and $|\langle k'|V|k\rangle|^2$ is the matrix element coupling states k and k'. If an isotropic scattering cross-section with a white noise power spectrum is assumed, Equation (2.23) simplifies to

$$
\frac{\hbar}{\tau(E)} = 2\pi n_{\mathrm{imp}} |V|^2 N(E) \quad ,
\tag{2.24}
$$

where $|V|^2$ is a constant.

For higher dimensional systems, it is more straightforward to use an alternative form of the Drude conductivity,

$$\sigma(E) = \frac{e^2 n(E)\tau(E)}{m} \quad . \tag{2.25}$$

For two-dimensional systems, the quantity $n_{\mathrm{imp}}|V|^2$ in Equation (2.24) can be derived from the two-dimensional electron mobility by noting that for a two-dimensional electron gas with mobility μ, $N_{2\mathrm{d}}(E) = \frac{m}{\pi\hbar^2}$ and $\tau_{2\mathrm{d}} = \frac{m\mu}{e}$, giving

$$n_{\mathrm{imp}}|V|^2 = \frac{e\hbar^3}{2\mu m^2} \quad . \tag{2.26}$$

Assuming that this value does not change between a two-dimensional and Q1D system, the scattering time can be expressed as a function of the two-dimensional mobility and the two-dimensional density of states of the Q1D system as

$$\tau(E) = \frac{\mu m^2}{\pi e\hbar^2} \frac{1}{N_{2\mathrm{d}}^{\mathrm{Q1D}}(E)} \quad . \tag{2.27}$$

Therefore, the two-dimensional conductivity of a device as a function of energy can be determined once the two-dimensional density of states of the system is known. By integrating the density of states to calculate the electron density as a function of energy, it is then possible to parametrically plot conductance versus electron density, which is what is typically measured experimentally.

Figure 2.5 Schematic of energy potential seen by electrons traveling along a Q1D conductor.

Because the potential in Q1D conductors of the type shown in Figure 2.5 is separable (that is electrons are confined along the x direction and free along the y direction), the two-dimensional density of states for these wires can be written as

$$N_{2d}^{Q1D}(E) = \frac{1}{2} N_{1d}^{x}(E) \otimes N_{1d}^{y}(E) \quad , \tag{2.28}$$

where $N_{1d}^{y}(E)$ is the one-dimensional density of states for a free electron as given by Equation (2.22), and $N_{1d}^{x}(E)$ is dependent on the confining potential.

To calculate $N_{1d}^{x}(E)$ for various confining potentials, Bagwell [34] implemented a computer model to calculate the band structure for a given periodic potential. For the present work, a computationally simpler model is used in which bound states within the wire are considered to be tight binding states, with the remaining states with energies above the confining potential treated as free-electron-like states. Except for states with energies near the top of the confining

potential, this simplified model is a very good approximation to the full band structure calculation [35].

With these assumptions, the one-dimensional density of states in the direction of confinement can be expressed as

$$N_{1d}^{x}(E) = \underbrace{\sum_{i=1}^{n} \frac{2}{W_i} \delta(E - E_i)}_{\text{Bound States}} + \underbrace{\sqrt{\frac{2m}{\pi^2 \hbar^2}} \frac{1}{\sqrt{E - (E_{\text{top}} - E_{\text{area}})}} \theta(E - E_{\text{top}})}_{\text{“Free” States}} , \qquad (2.29)$$

where n is the number of bound states, E_i is the energy of subband i, W_i is the effective width of wire for subband i, E_{top} is the energy of the top of the confining potential, and

$$E_{\text{area}} = \frac{1}{2m} \left(\pi\hbar \sum_{i=1}^{n} \frac{1}{W_i} \right)^2 \qquad (2.30)$$

is a correction to the “free” electron density of states to account for electron states already being modeled as bound states.

Combining Equations (2.29) and (2.22), it is possible the calculate the two-dimensional density of states for the Q1D system using Equation (2.28). Conductivity as a function of energy can be calculated using Equation (2.25) by using this density of states to calculate the scattering time as a function of energy using Equation (2.27), and integrating it to find the electron density as a function of energy. Conductivity can then be plotted parametrically as a function of electron density.

The proceeding model is shown graphically in Figure 2.6 for a strictly one-dimensional conductor, and a sample Q1D potential with three bound states and a transition region above the confining potential. Temperature broadening equivalent to 1.2 K is included in Figure 2.6 as well.

2.2 Theory of resonant tunneling

Another class of device that has received much attention recently are those based on resonant tunneling [36]. Such devices have demonstrated the ability to work at very high frequencies [6,14], with quantum effects that are quite robust, even at room temperature [15]. There have also been several reported circuit applications of resonant tunneling devices [37]

The basic principle of these devices is shown in Figure 2.7. By sandwiching a narrow bandgap material (GaAs) between two large bandgap materials (AlGaAs), a quantum well is formed with, in this case, a single bound state, E_r. Because the Fermi level is below the conduction-band edge of the wide band gap material, electrons need to tunnel through both barriers for a current to flow. As such, there is very little current as a voltage is applied across the structure. However, for this type of double barrier system, electrons with an energy at the same level as the bound state in the well can tunnel through both barriers with probability of one. Therefore, as the voltage increases to the point where the bound state is at the same energy level as an occupied state in the emitter, there is a sharp increase in the number of electrons that pass through the system, leading to a peak in current at V_1. As the voltage continues to increase across the sample, the bound state falls below the level of the emitter, moving the device off resonance, and hence a lower current is obtained at V_2. As the voltage continues to

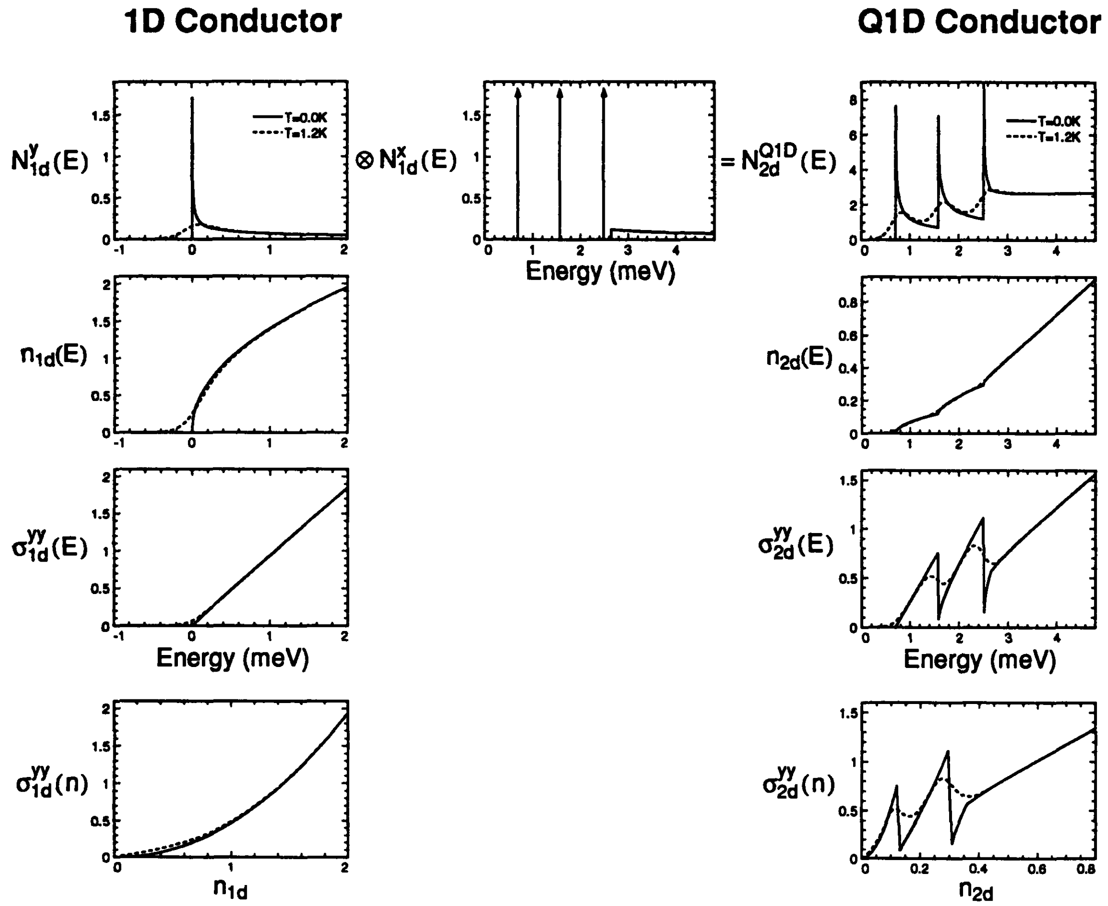


Figure 2.6 Summary of model for calculating the conductance of a diffusive Q1D conductor using the convolution method.

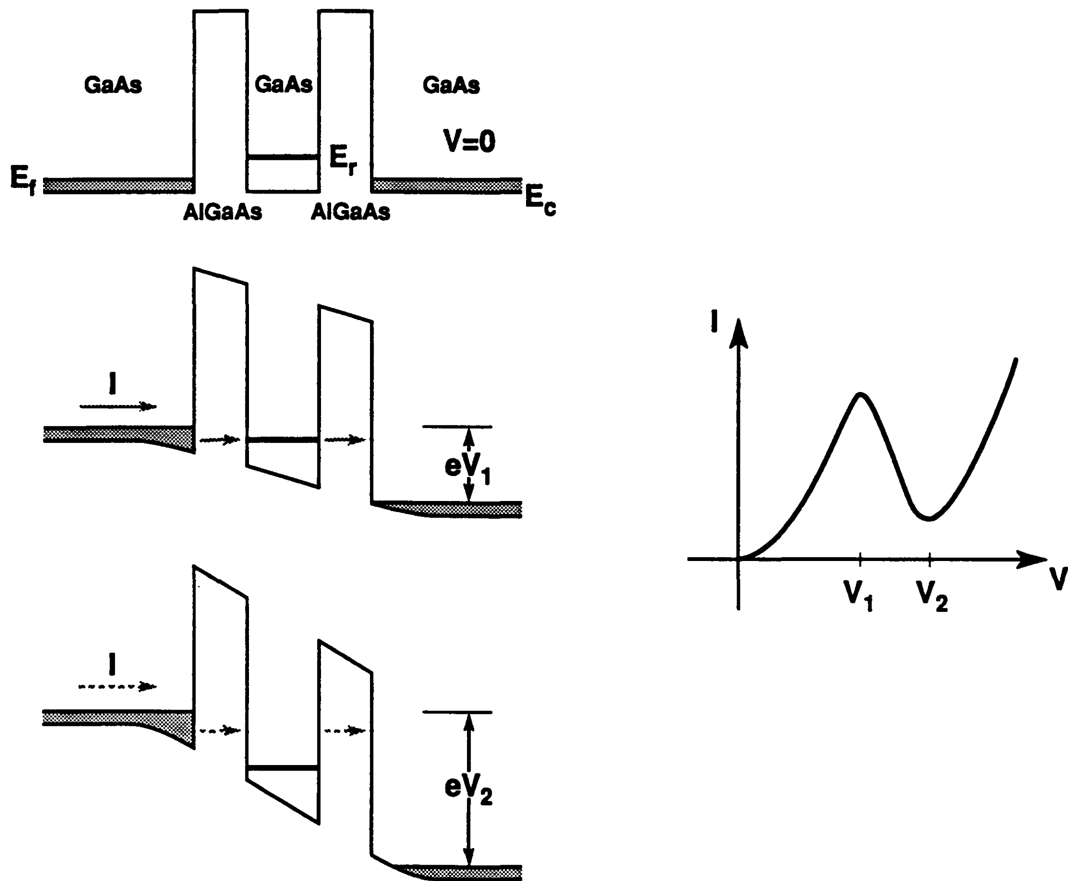


Figure 2.7 Conduction-band energy as a function of position for a double barrier resonant tunneling device for various applied voltages, along with typical current/voltage relationship showing resonance condition at V_1.

increase, the electrons in the emitter become energetic enough to pass over the tunnel barriers, and the current increases again.

In many ways, resonant tunneling can be thought as an electronic equivalent of the Fabry-Perot resonant cavity from optics [38], where two perfectly reflecting mirrors allow light to pass through unreflected, if the distance between the mirrors is an integral multiple of a half wavelength. In essence, the resonant barrier is acting as an energy filter in the direction normal to the barrier, with a transmission probability of one at E_r, and zero elsewhere. As with

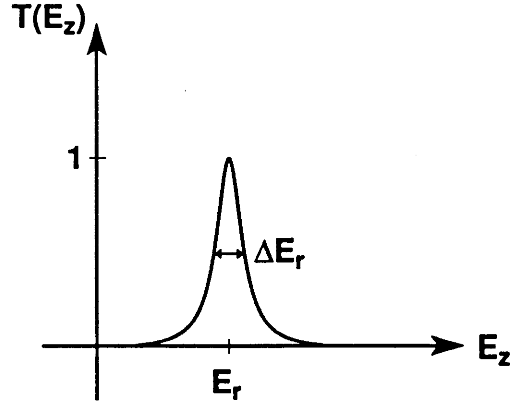


Figure 2.8 Transmission probability versus energy in direction perpendicular to a "sloppy" tunneling barrier.

Fabry-Perot cavities, if the "mirrors" are not perfectly reflecting, there is some softness to the resonance, so that it has some characteristic width ΔE_r, centered around E_r, as shown in Figure 2.8.

In the case of a one-dimensional region on either side of the tunneling barriers (a 1D emitter and collector), the current through the barrier as a function of energy mirrors the transmission probability and is given by

$$\begin{aligned} I_{1d}(E, V \approx 0, T \approx 0) = e\,n(E)v_z(E) &= e\,\Delta E \int v_z(\varepsilon)T_{1d}(\varepsilon)N_{1d}(\varepsilon)d\varepsilon \\ &= \frac{e}{\pi\hbar}\Delta E\, T_{1d}(E) \\ &= \frac{e^2 V}{\pi\hbar} T_{1d}(E) \end{aligned} \quad , \qquad (2.31)$$

where T_{1d} is given by Figure 2.8,

$$\Delta E = \begin{cases} eV & eV < \Delta E_r \\ \Delta E_r & eV > \Delta E_r \end{cases} \quad , \qquad (2.32)$$

and V is the applied voltage.

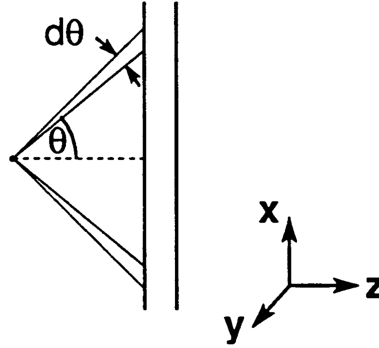


Figure 2.9 Two-dimensional point source of electrons radiating onto a resonant tunneling double barrier.

In order to calculate the current versus energy for a resonant tunneling device with a two-dimensional emitter, the techniques described in Section 2.1.1 can be used to increase the dimensionality of Equation (2.31) to two [16]. Alternatively, an electron counting procedure can be extended to two dimensions.

Referring to Figure 2.9, for an isotropic two-dimensional point source of electrons, the number of electrons in a given arc $d\theta$ is given by

$$\begin{aligned} n(E) &= \Delta E \, N_{2\mathrm{d}}(E) \frac{d\theta}{2\pi} \\ &= \Delta E \frac{m}{\pi\hbar^2} \frac{d\theta}{2\pi} \quad . \end{aligned} \tag{2.33}$$

Because the tunnel barriers filter electron based on their momentum perpendicular to the barriers, for electrons incident at an angle θ, only electrons with energy $E = \frac{E_r}{\cos^2\theta}$ will be able to resonantly tunnel through the barriers. Differentiating and solving for $d\theta$, Equation (2.33) can be rewritten in terms of energy as

$$
\begin{aligned}
n(E) &= \Delta E \frac{m}{\pi\hbar^2} \frac{1}{2\pi} \frac{1}{\sqrt{E-E_r}} \frac{\sqrt{E_r}}{2E} 2\, dE \\
&= \frac{\Delta E}{2\pi\hbar} \Delta E_r \frac{1}{v_z} N_{1\mathrm{d}}(E-E_r) \qquad ,
\end{aligned} \tag{2.34}
$$

where the range of electron energies that may resonantly tunnel is given by

$$
dE = \frac{\Delta E_r}{\cos^2\theta} = \Delta E_r \frac{E}{E_r} \quad , \tag{2.35}
$$

the velocity of tunneling electrons in the direction of current flow is given by

$$
v_z = \sqrt{\frac{2E_r}{m}} \quad , \tag{2.36}
$$

and $N_{1\mathrm{d}}$ is the one-dimensional density of states for a free electron, as defined in Equation (2.22).

Combining Equations (2.34) and (2.36) and summing over all the point emitters along the x direction, the current versus energy expression for a resonant tunneling device with a two-dimensional emitter and collector is given by

$$
\begin{aligned}
I_{2\mathrm{d}}(E) &= e L_x n(E) v_z \\
&= \frac{e}{\pi\hbar} \Delta E \frac{L_x}{2} \Delta E_r N_{1\mathrm{d}}(E-E_r) \quad ,
\end{aligned} \tag{2.37}
$$

where L_x is the length of the device in the x direction.

By performing a similar analysis for the case of a three-dimensional emitter and collector, it can readily be shown that

$$I_{3d}(E) = \frac{e}{\pi\hbar}\Delta E \frac{L_x L_y}{2}\Delta E_r N_{2d}(E - E_r) \tag{2.38}$$

where L_y is the length of the device in the y direction.

For the case of multiple resonant levels in the system, the total current can be calculated by adding the contribution of each channel. These results are summarized in Figure 2.10.

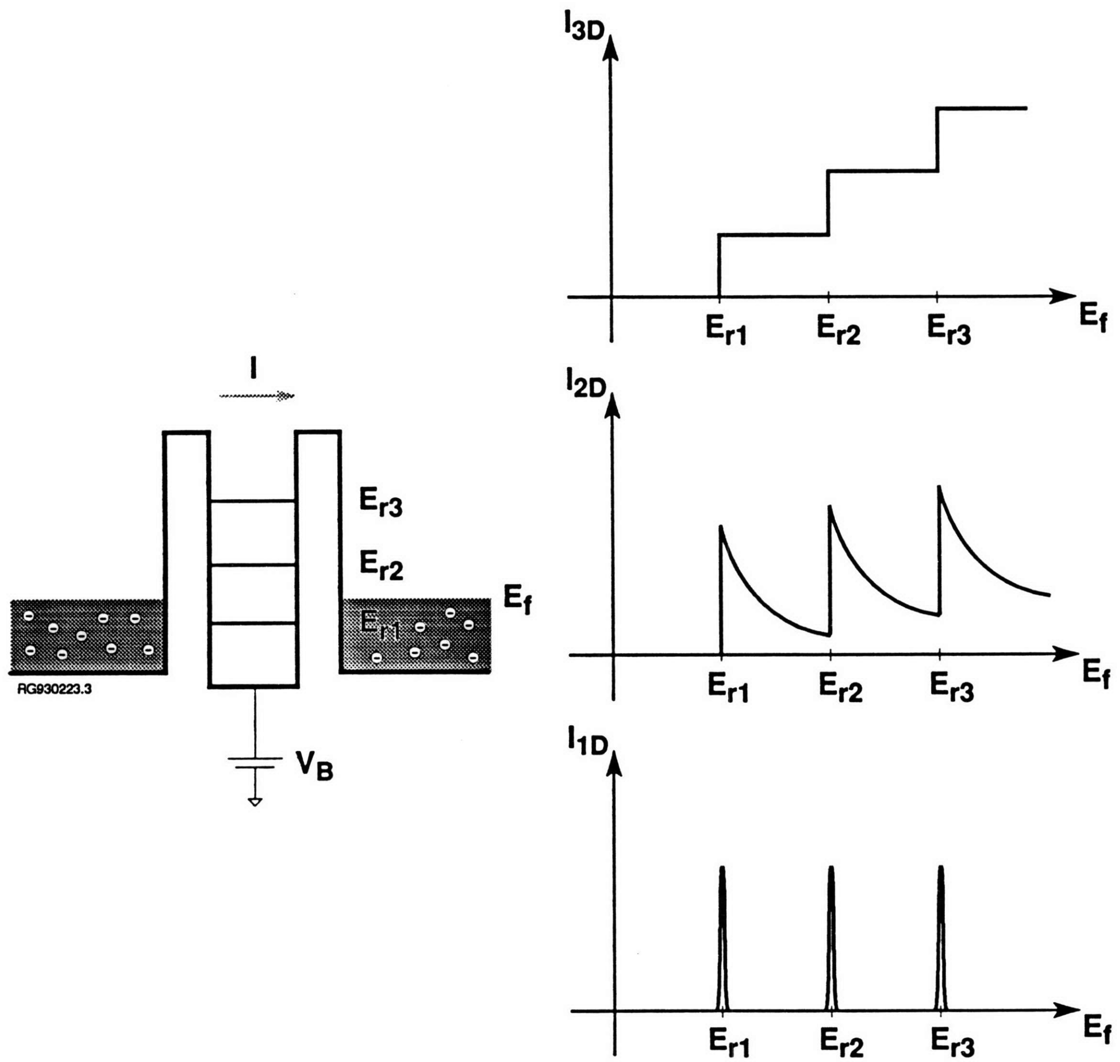


Figure 2.10 Current versus Fermi energy for idealized resonant tunneling transistors with 3D, 2D, and 1D emitters and collectors.

Chapter 3
Modeling of X-ray Mask Patterning

As noted previously, during mask fabrication there is an unusual degree of process latitude when patterning x-ray membranes using electron-beam lithography. This is clearly shown in Figure 3.1, where a fine line has been written between two very large, overexposed regions in relatively thick resist with no proximity correction. If such a pattern were written on a bulk substrate, it is unlikely the lithography would be successful.

To better understand the process of electron-beam lithography on x-ray mask membranes, a Monte Carlo model for electron scattering and energy loss was implemented to quantitatively evaluate energy deposition during electron-beam lithography. Such models have been successfully used by many authors to better understand the energy deposition during electron beam lithography on various substrates [39,40,41,42]. The model described in this chapter is an extension of the one developed by Hawryluk *et al.* [40,41,43], modified to include inelastic processes after Murata *et al.* [42]. Inclusion of inelastic processes has been shown to be important when modeling patterning over high-atomic-weight substrates [44].

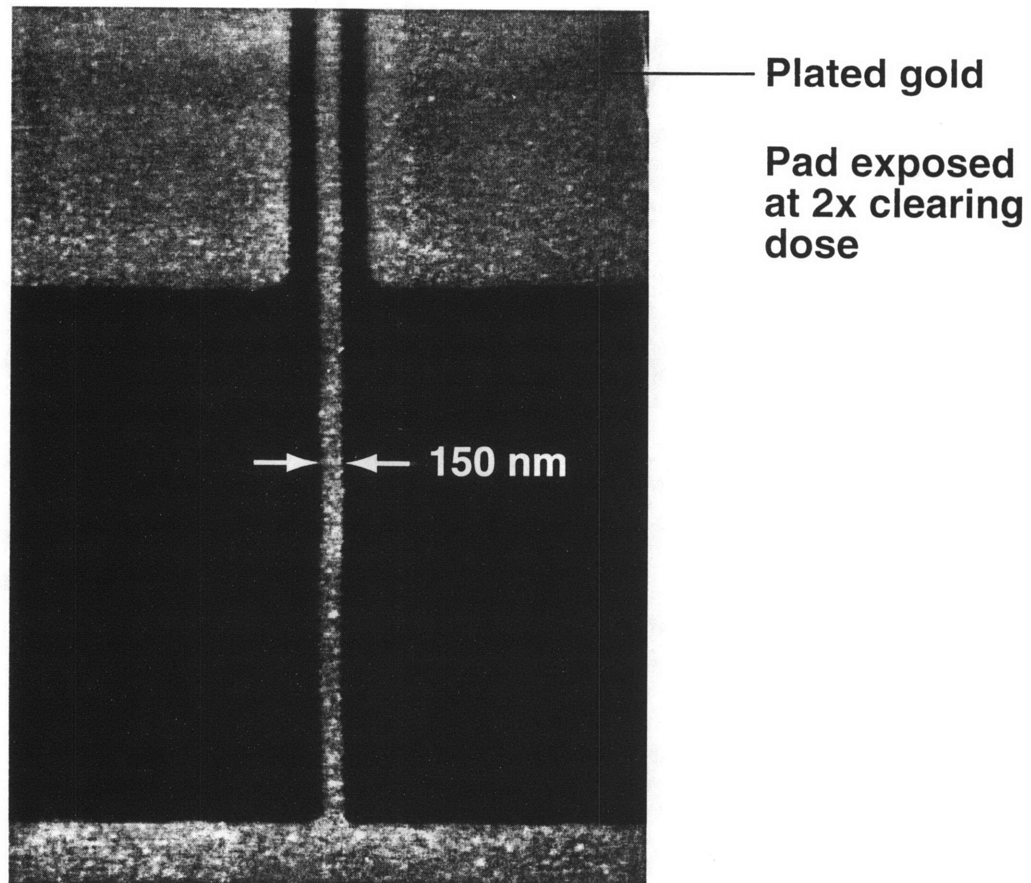


Figure 3.1 Top view of finished x-ray mask written using scanning-electron-beam lithography. The large pad areas (~20×20μm) were exposed at approximately twice the dose of the line.

As is typical for Monte Carlo models, the trajectories of a large number of electrons (typically 15000) are tracked through a given sample and between different scattering events. At each scattering event, a random number is used to decide if the scattering is elastic or inelastic, based on the relative scattering cross-sections. If the scattering is elastic, the trajectory of the electron is altered and it continues to the next scattering event. If inelastic, a secondary electron is created and allowed to travel in the sample. Secondary electrons are not permitted to spawn more secondaries. After the flight of the secondary electron has terminated, the primary electron is then allowed to continue through the sample.

In addition, a resist development model has been implemented [45] in order to evaluate the influence of patterning parameters on resist profiles.

3.1 Electron scattering cross-sections

For elastic scattering, the differential scattering cross-section for scattering into solid angle Ω is calculated using the screened Rutherford cross-section [40]

$$\frac{d\sigma^{el}}{d\Omega} = \frac{Z(Z+1)e^4}{16E^2\left(\sin^2(\theta/2)+\alpha^2\right)^2}\ , \tag{3.1}$$

where σ^{el} is the cross-section for elastic scattering, Z is the atomic number of the scattering atom, e is the electronic charge, E is the energy of the electron, and

$$\alpha = 2.33\frac{Z^{1/3}}{\sqrt{E}} \tag{3.2}$$

is the atomic screening parameter given by Nigam *et al.* [46].

The total elastic cross-section is calculated by integrating Equation (3.1) over the full solid angle to give

$$\sigma^{el} = \frac{\pi Z(Z+1)e^4}{4E^2\alpha^2(\alpha^2+1)}\ . \tag{3.3}$$

The inelastic scattering cross-section was calculated using the classical cross-section for a coulomb interaction with free-electrons [47],

$$\frac{d\sigma^{\text{in}}}{d\varepsilon} = \frac{\pi e^4}{E^2}\left[\frac{1}{\varepsilon^2} + \frac{1}{(1-\varepsilon)^2}\right] \tag{3.4}$$

where ε is the normalized energy transfer to the secondary electron. Because the two electrons that result from an inelastic event are indistinguishable, the electron with the lower energy is labeled as the "secondary" electron. This implies that $0<\varepsilon<0.5$.

In order to avoid an infinite cross-section at $\varepsilon=0$, a cut-off value ε_c for energy transfer to secondaries was assumed [42]. By setting this cut-off value, very low energy electrons are neglected when calculating energy deposition. The total inelastic cross-section can then be calculated as

$$\sigma^{\text{in}} = \int_{\varepsilon_c}^{1/2} \frac{\pi e^4}{E^2}\left[\frac{1}{\varepsilon^2} + \frac{1}{(1-\varepsilon)^2}\right] d\varepsilon = \frac{\pi e^4}{E^2}\left[\frac{1-2\varepsilon_c}{\varepsilon_c(1-\varepsilon_c)}\right] . \tag{3.5}$$

For smaller ε_c, Equation (3.5) implies a larger number of inelastic collisions (and hence secondary electrons), but a smaller average energy transfer per collision. Hence, there is a significant savings in computational time by neglecting very low energy electrons, with only a small change in the computed energy profiles [42]. For this work, a value of 0.01 was used for ε_c.

3.2 Energy loss mechanisms

Energy deposition is modeled in the continuous slowing down approximation between scattering events. Electron energy versus distance traveled is shown schematically in Figure 3.2. Given an electron with initial energy E_0, the electron continuously dissipates energy as it

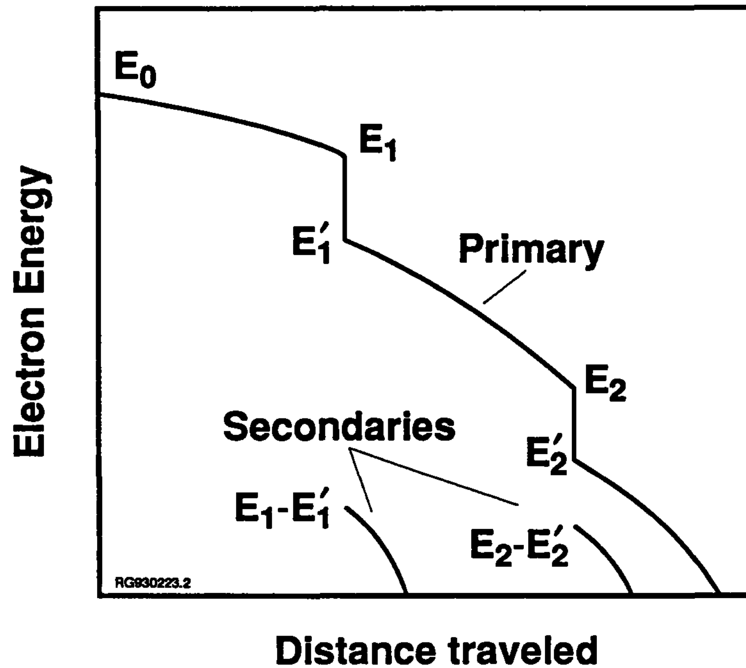


Figure 3.2 Schematic illustration of electron energy versus distance traveled (after [42]).

travels through the sample, occasionally undergoing elastic collisions. At some point (E_1), the electron undergoes an inelastic collision, spawning a secondary electron with energy $E_1 - E_1'$. The secondary is then tracked until all its energy has been dissipated in the sample. The primary electron then continues with reduced energy E_1', and so on.

Internally, the sample being modeled is divided into cells typically with a volume of $(10\,\text{nm})^3$. Energy dissipated in a given cell is assumed to be dissipated uniformly within that cell. Electrons are tracked until their energy falls below 300 eV, at which time the remainder of their energy is deposited in the current cell.

Berger *et al.* [48] have derived an expression for the spatial rate of energy loss for an electron passing through a solid to be

$$\left(\frac{dE}{ds}\right)_{\text{Bethe}} = -\frac{\pi e^4 n_{e^-}}{E}\left\{\ln\left[\frac{\tau^2(\tau+2)}{2(I/mc^2)}\right] + F^-(\tau)\right\} , \tag{3.6}$$

where E is the energy of the electron, s is the distance traveled, τ is the electron kinetic energy in terms of the rest energy of the electron mc^2 (510.976keV), n_{e^-} is the density of electrons per unit volume in the substrate, I is the mean excitation energy, and

$$F^-(\tau) = 1 - \frac{\tau(\tau+2)}{(\tau+1)^2} + \frac{[\tau^2/8 - (2\tau+1)\ln 2]}{(\tau+1)^2} \quad . \tag{3.7}$$

For nonrelativistic energies ($\tau << 1$, or $E < 100\,\text{keV}$), Equation (3.6) reduces to the usual Bethe energy loss formula,

$$\left(\frac{dE}{ds}\right)_{\text{Bethe}} = -\frac{2\pi e^4 n_{e^-}}{E}\ln\left[1.166\frac{E}{I}\right] \quad . \tag{3.8}$$

The excitation energy for elements with atomic number $Z > 13$ is given empirically by [48]

$$I = Z\left(9.76 + 58.8Z^{-1.19}\right)\text{eV} \quad . \tag{3.9}$$

For some low atomic weight elements that are typically present in resists, I is generally taken to be 18.7 eV for hydrogen, 78 eV for carbon, 85 eV for nitrogen, and 89 eV for oxygen [48].

For a generalized substrate consisting of several different independent elements, the total energy deposition due to elastic scattering can be derived [49] by summing over all i elements such that

$$\left(\frac{dE}{ds}\right)_{\text{Bethe}} = -\frac{2\pi e^4}{E}\sum_i n_{e_i^-} \ln\left[1.166\frac{E}{I_i}\right]$$
$$= -\frac{2\pi e^4 n_{e^-}}{E} \ln\left[1.166\frac{E}{\langle I \rangle}\right] \quad , \tag{3.10}$$

where

$$\ln\langle I \rangle = \sum_i \frac{n_{e_i^-} \ln I_i}{n_{e^-}} \tag{3.11}$$

is the effective mean excitation energy for the substrate.

Energy dissipation due to inelastic scattering events with a normalized energy transfer below ε_c is modeled as an additional term in the expression for spatial rate of energy loss. The continuous energy loss due to these low energy inelastic scattering events is given by [42]

$$\left(\frac{dE}{ds}\right)_{\text{in}} = -\sum_i n_{e_i^-} \int_{\varepsilon_c}^{1/2} E\varepsilon\left(\frac{d\sigma^{\text{in}}}{d\varepsilon}\right) d\varepsilon$$
$$= -\frac{\pi e^4 n_{e^-}}{E}\left\{2 - \frac{1}{1-\varepsilon_c} - \ln[4\varepsilon_c(1-\varepsilon_c)]\right\} \quad . \tag{3.12}$$

The total spatial rate of energy loss for an electron passing through a solid can then be expressed as the sum of Equations (3.10) and (3.12).

3.3 Model implementation

To calculate energy deposition in a given sample, the trajectories of a large number of electrons are followed individually. Initially, electrons are assumed to be traveling normal to the sample surface, with the position of the electron relative to the center of the beam calculated using a

random number generator, assuming a gaussian distribution within the beam. Note that the algorithm described in reference [49] for calculating the initial position of the electron results in a position that is described by a Rayleigh distribution rather than a normal (Gaussian) distribution. For this work, a Gaussian deviate transformation algorithm is used [50] to give the proper distribution.

The step length, Δs, for the electron flight in a particular layer is calculated using the expression

$$\Delta s = -\lambda_{\text{tot}} \ln R_1 \tag{3.13}$$

where R_1 is a pseudo-random number between 0 and 1, and λ_{tot} is the calculated mean free path for the electron in the layer, given by

$$\begin{aligned} \frac{1}{\lambda_{\text{tot}}} &= \sum_i N_i \sigma_i^{\text{el}} + \sum_i n_{e_i^-} \sigma_i^{\text{in}} \\ &= \frac{1}{\lambda_{\text{el}}} + \frac{1}{\lambda_{\text{in}}} \end{aligned} \quad , \tag{3.14}$$

where N_i is the number of atoms of species i per unit volume, λ_{el} is the elastic mean free path, and λ_{in} is the inelastic mean free path.

If Δs is so large as to remove the electron from the layer, the electron is propagated to the edge of the layer, depositing energy in cells according to Equations (3.10) and (3.12). A new Δs is then calculated for the new layer, and the flight of the electron continues. If Δs is sufficiently small for the electron to remain within the layer, the electron is propagated a distance Δs, depositing the appropriate energy. At the end of this step, the type of scattering event is

randomly determined using the probability of elastic collision, $p_{el}=\lambda_{tot}/\lambda_{el}$, and the probability of inelastic collision, $p_{in}=\lambda_{tot}/\lambda_{in}$.

If the scattering event is determined to be elastic, the scattering atom type is randomly determined using the probabilities $p_i^{el}=\lambda_{el}N_i\sigma_i^{el}$, where p_i^{el} is the probability that the electron scattered off an atom of species i. The electron is then deflected by angle θ, where [49]

$$\cos\theta=\frac{R_2(1+2\alpha_i^2)-\alpha_i^2}{R_2+\alpha_i^2} \quad . \tag{3.15}$$

Because of symmetry, the azimuthal angle is given by $\phi=2\pi R_3$, where R_3 is again a pseudo-random number.

If the scattering event is determined to be inelastic, the position of the primary is stored with energy $(1-\varepsilon)E$, and a secondary electron is spawned with energy εE, where the normalized energy transfer ε is calculated by solving

$$R_4=\frac{\int_{\varepsilon_c}^{\varepsilon}\left(\frac{d\sigma^{in}}{d\varepsilon}\right)d\varepsilon}{\int_{\varepsilon_c}^{1/2}\left(\frac{d\sigma^{in}}{d\varepsilon}\right)d\varepsilon} \tag{3.16}$$

for ε, where R_4 is another uniform pseudo-random number.

The primary electron is deflected by angle γ, where

$$\sin^2\gamma=\frac{2\varepsilon}{2+\tau-\tau\varepsilon} \quad , \tag{3.17}$$

and the secondary leaves at an angle ζ determined by

$$\sin^2\zeta = \frac{2(1-\varepsilon)}{2+\tau\varepsilon} \quad . \tag{3.18}$$

An interesting consequence of Equations (3.17) and (3.18) is that since the energy imparted on secondaries is normally quite small, secondaries tend to travel in the direction normal to the flight of the primary. As such, they tend to expose the region immediately around the path of the primary.

After a secondary electron is spawned, it is modeled much as the primary, except that inelastic events are no longer permitted. The secondary is tracked until its energy falls below 300 eV, at which point its remaining energy is deposited in the current cell, and the tracking of the flight of the primary continues.

Electrons are tracked until either they dissipate all their energy, they leave the sample, or they travel so deep in the sample that they no longer have sufficient energy to return to the region of interest.

3.4 Modeling of resist development

After a statistically large number of primary electrons have been tracked, the energy deposition in the sample is tabulated into the equivalent of the point-response function of the electron beam for the particular substrate geometry, at various depths. To find the energy deposition in the substrate (usually a resist) for a particular pattern, the point response is convolved with the

pattern geometry, including dose information. The results are tabulated as the energy deposited per unit volume, as a function of lateral position and depth in the resist.

In order to model the development of PMMA resist, the resist is assumed to have a surface dissolution rate as a function of absorbed energy given by [51]

$$R(D) = R_{\mathrm{dark}}\left(1+\frac{D}{D_0}\right)^{\alpha} \quad , \tag{3.19}$$

where R_{dark} is the development rate for the unexposed resist, D is the absorbed energy, D_0 is the threshold absorbed energy for exposure, and α is the power law the resist obeys. For the PMMA and developer used in this work, R_{dark}=0.017 nm/s, D_0=270 J/cm^3, and α=2.78, after the experimental work of Hawryluk *et al.* [41].

In order to dynamically model resist development, a string development model was implemented after Jewett *et al.* [52]. In this model, the surface of the resist is modeled as a development contour. During a particular time step Δt, every point along the contour is moved a distance $R\Delta t$ in a direction normal to the contour, where R is the dissolution rate for that particular point, as given by Equation (3.19). A new contour is then fit to the surface, and the process is continued.

3.5 Modeling results

The two types of scattering that effect resolution in electron-beam lithography are shown schematically in Figure 3.3. The first, shown in Figure 3.3 (a) is forward scattering, which results from small angle deflections of the high-energy primary electrons as they travel through

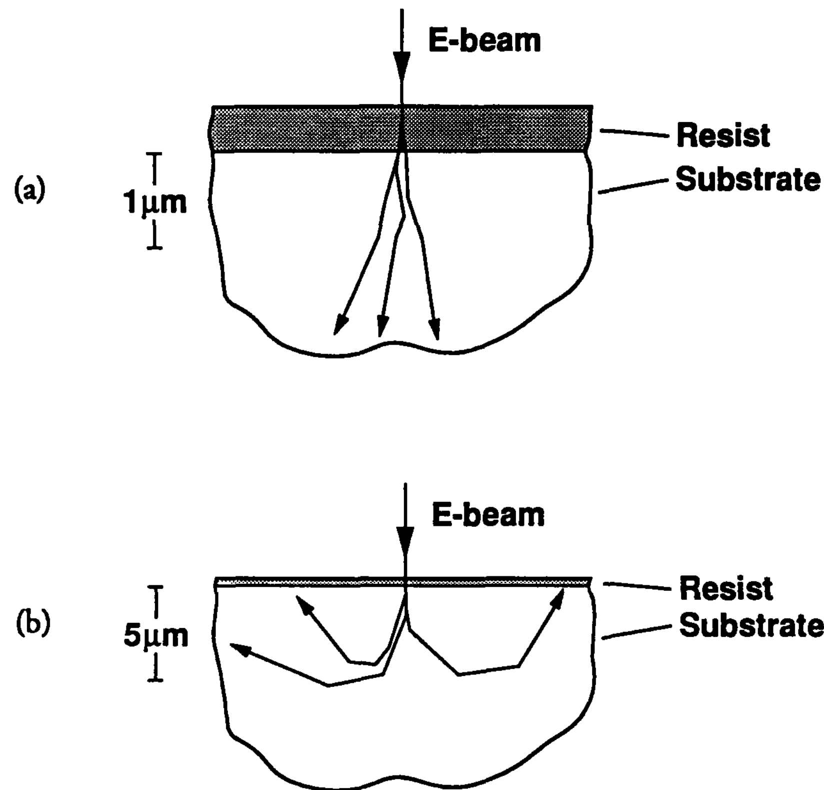


Figure 3.3 Schematic of (a) small angle forward scattering and (b) long range backscattering of electrons.

the resist. Depending on the thickness of the resist, this may result is a slight undercut profile when the pattern is developed. Figure 3.4 shows the energy absorbed in a 300 nm-thick freestanding film of PMMA on a plating base, at two depths in the PMMA. The energy deposition curves are for an infinitely long line written with a 50 keV beam of electrons and a beam diameter of 50 nm. It is readily apparent that the energy deposition profile broadens as the beam travels through the resist.

The second type scattering, shown schematically is Figure 3.3 (b), is long range backscattering. In this case, electrons actually travel into the substrate and then back into the resist, exposing regions many microns away from the point of initial entry. For dense patterns, such as those

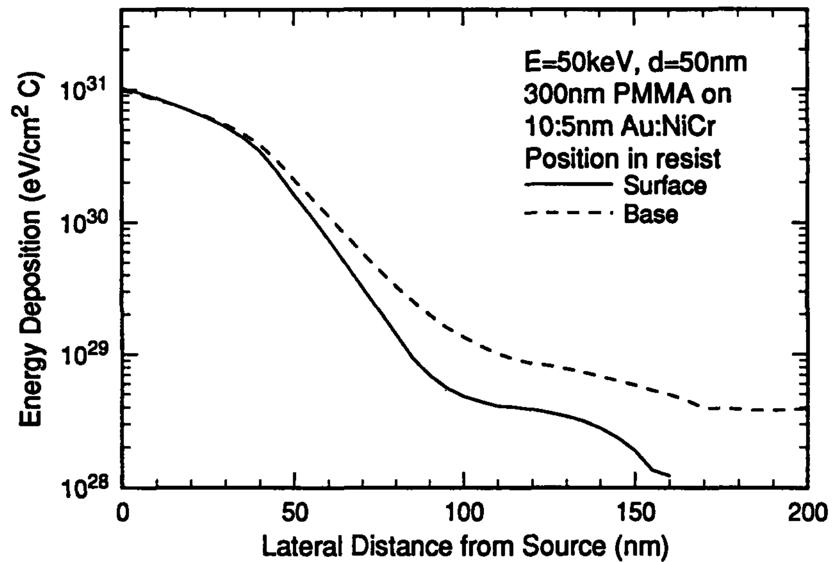


Figure 3.4 Energy deposition at the surface and base of a 300 nm freestanding film of PMMA on plating base.

for complex circuits, this long-range proximity effect can be a serious problem. As mentioned previously, one of the main advantages of electron-beam lithography on a x-ray mask membrane is the fact that primary electrons tend to exit the backside of the membrane, and not scatter back into the resist at some remote location.

The virtue of a membrane substrate is clearly shown in Figure 3.5, where the energy deposition at the base of a film of PMMA on plating base is plotted for substrates corresponding to a freestanding film of PMMA (best case in terms of minimizing back scattering), PMMA on an 1 µm-thick x-ray mask membrane, and PMMA on bulk silicon. Note that in the immediate vicinity of the beam, the energy deposition profiles are nearly identical. In fact, the integrated energy deposition in the region within 50 nm of the beam centers differ by less than four percent. However, the profiles begin to noticeably diverge about 200 nm from the beam center. Although the energy deposition far away from the beam center is several orders of magnitude

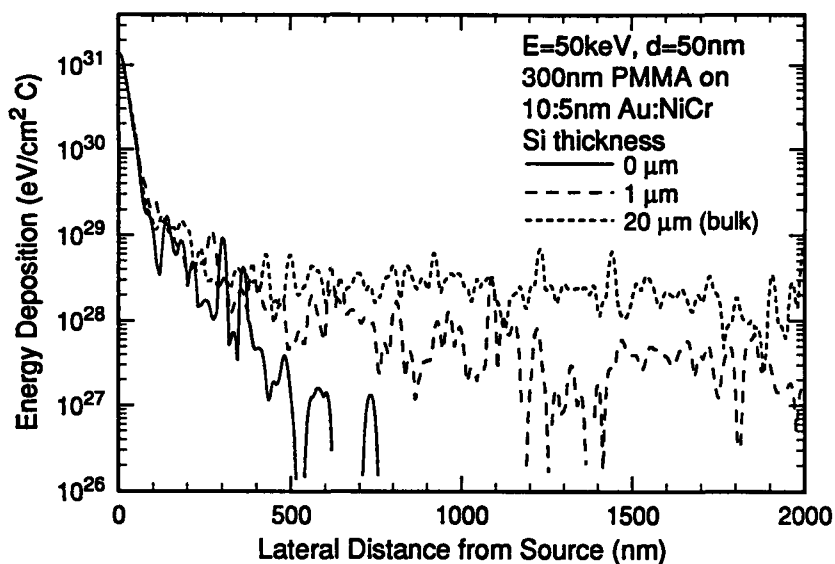


Figure 3.5 Energy deposition at the base of a 300 nm film of PMMA on plating base for substrates corresponding to freestanding PMMA, PMMA on a membrane, and PMMA on bulk silicon.

lower than at the beam center, this background level can extend for many microns (more than 10 µm in the case of bulk silicon). In fact, relative to a free standing film of PMMA the total integrated energy deposited in the resist is 8% higher when patterning a membrane, and 17% higher when patterning on a bulk silicon substrate. When patterning a large feature next to small feature, this background level can have a significant effect on process latitude.

As an example, Figure 3.6 shows the modeled energy deposition in resist for the pattern shown in Figure 3.1. The sample is taken to be a 300 nm-thick film of PMMA, a plating base of 10:5 nm Au:NiCr, and silicon substrates of various thicknesses, with a 50 keV beam of 50 nm diameter. The energy deposition curves are given at the base of the PMMA resist, where proximity effects are most pronounced. The silicon thicknesses correspond to a freestanding film of PMMA, PMMA on a 1 µm thick silicon membrane (equivalent to an x-ray mask), and PMMA on bulk silicon

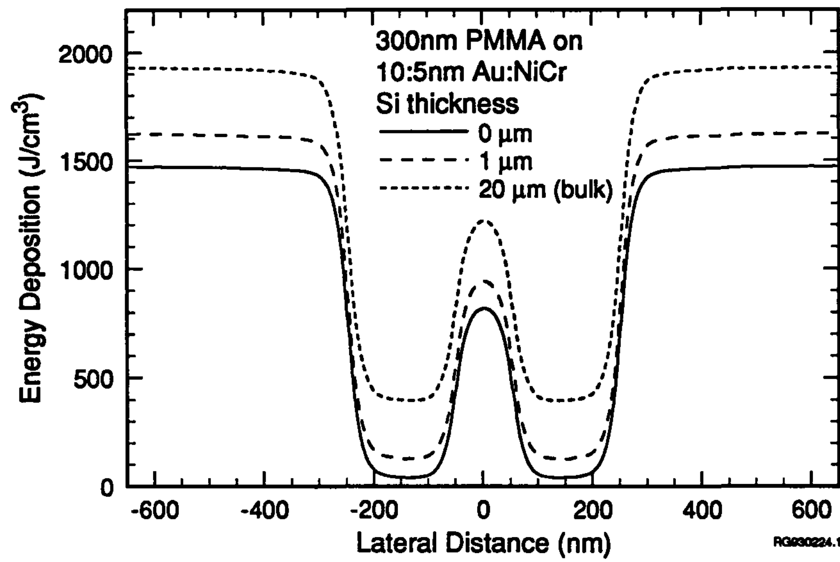


Figure 3.6 Modeled energy deposition in resist for the pattern shown in Figure 3.1, for various substrates.

As can be seen in the figure, there is a significant reduction in contrast when the exposure takes place on a bulk silicon substrate. For this pattern, the contrast is 3:1 for bulk silicon, 7.3:1 for a 1 µm silicon membrane, and 21:1 for a freestanding film of PMMA. (Contrast is defined as the ratio of the energy deposition in the middle of the line to the background energy deposition.)

This reduction in contrast is well known as the proximity effect. The predicted contrast enhancement for the membrane case agrees well with the large experimentally observed process latitude when exposing on membranes.

It is interesting to note that the "signal" level (i.e., the relative dose at the line middle) is approximately the same for all three case in Figure 3.6. The "noise", or background level being contributed by backscattering from the large open areas is what is primarily responsible for the reduction in contrast. The difference becomes strikingly clear when resist development is

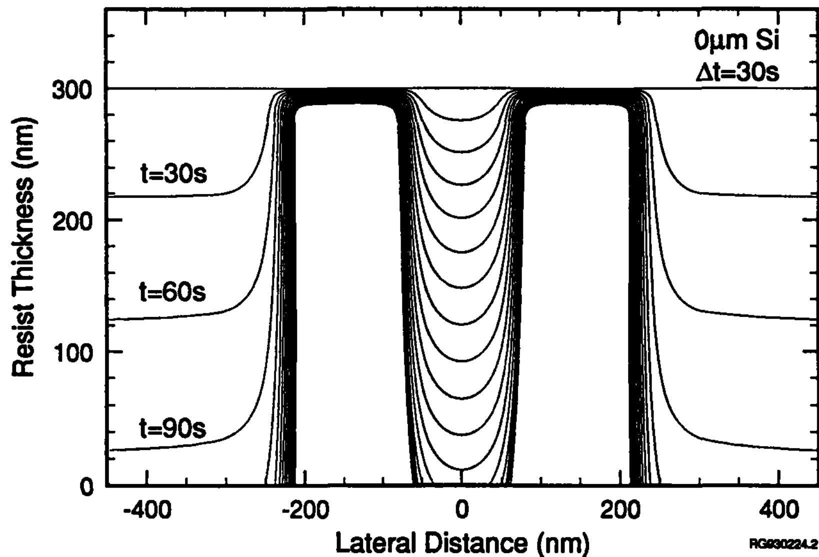


Figure 3.7 Resist contours at 30 second intervals during development, for the energy deposition pattern corresponding to a freestanding film in Figure 3.6.

modeled for these exposures [45]. In the case of PMMA, the dissolution rate is usually modeled as increasing as the cube of energy deposition, accentuating even small differences in areal image contrast.

A large background exposure level can have other, more subtle effects on process latitude. Because resist development is a dynamic process, certain regions of resist may be exposed to the developer for large amounts of time during the development process. If the background exposure level is high, these regions will then tend to develop laterally, adversely affecting linewidth control. This can be clearly seen by comparing Figures 3.7–3.9, which show resist profiles at various times during development for the pattern shown in Figure 3.6, for a freestanding film of PMMA (Figure 3.7), PMMA on a membrane (Figure 3.8), and PMMA on bulk silicon (Figure 3.9).

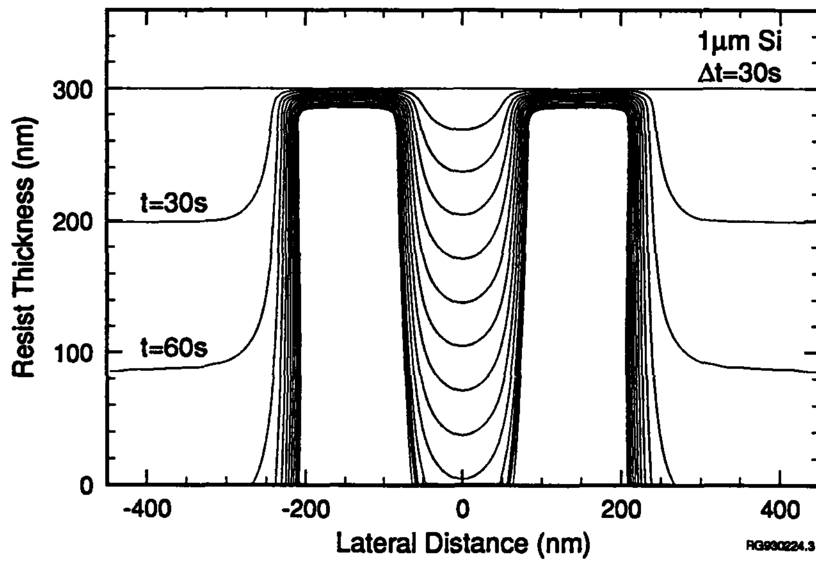


Figure 3.8 Resist contours at 30 second intervals during development, for the energy deposition pattern corresponding to a thin membrane in Figure 3.6.

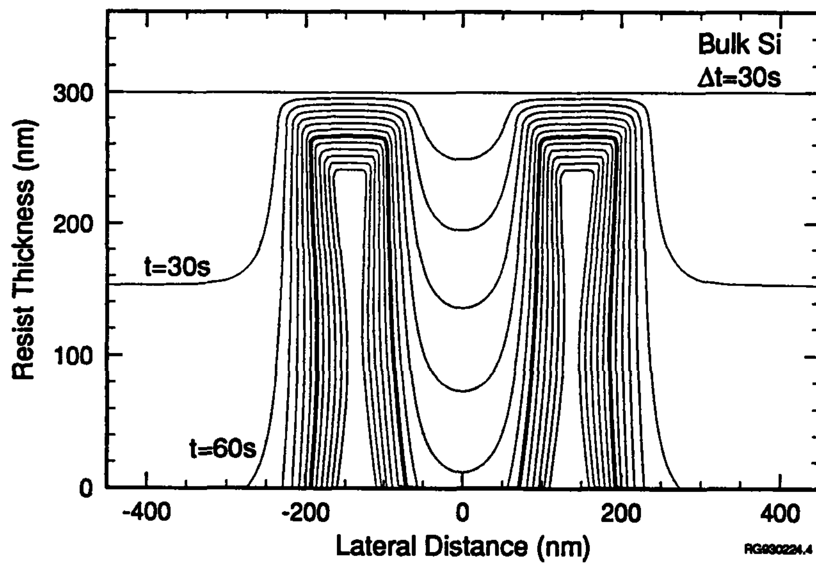


Figure 3.9 Resist contours at 30 second intervals during development, for the energy deposition pattern corresponding to a bulk silicon substrate in Figure 3.6.

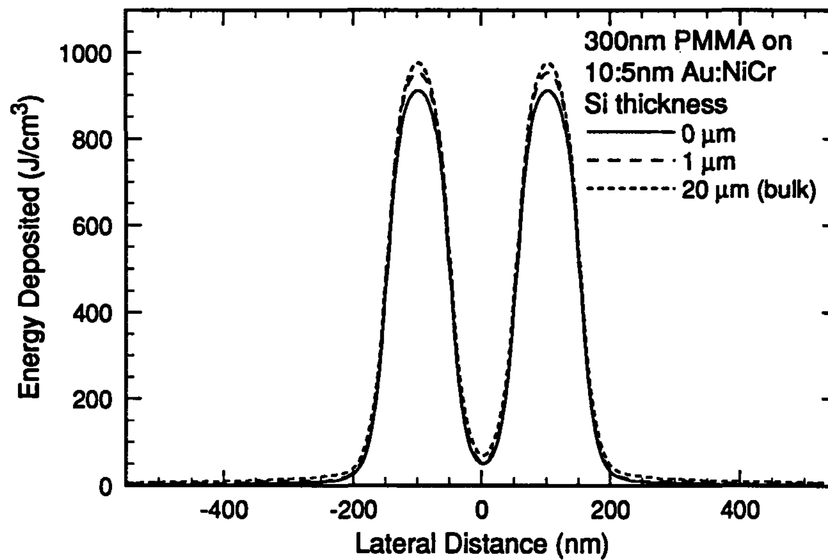


Figure 3.10 Modeled energy deposition for two 100 nm lines separated by 100 nm, on various substrates.

In all cases, the outside region develops away within the first few time steps, while the narrow region takes a considerably longer time to develop out. While the center line is developing out, the edges of the wide regions are exposed to developer and are developing laterally. In the cases of Figure 3.7 and Figure 3.8, there is very little lateral development, and development terminates quite nicely, implying a high process latitude. However, the same is not true of Figure 3.9, where there is appreciable lateral development while the center line develops out. Additionally, there is a significant loss of resist thickness, which may or may not cause a problem in subsequent processing steps, such as electroplating or liftoff.

The benefits of working with a x-ray mask membrane become less pronounced when features are isolated, as can be seen in Figure 3.10. In this case, there are two 100 nm lines separated by 100 nm in an otherwise clear field. For all three substrates, contrast is very good (14:1 in the case of bulk silicon) with very little variability in the region of interest. The low density of the

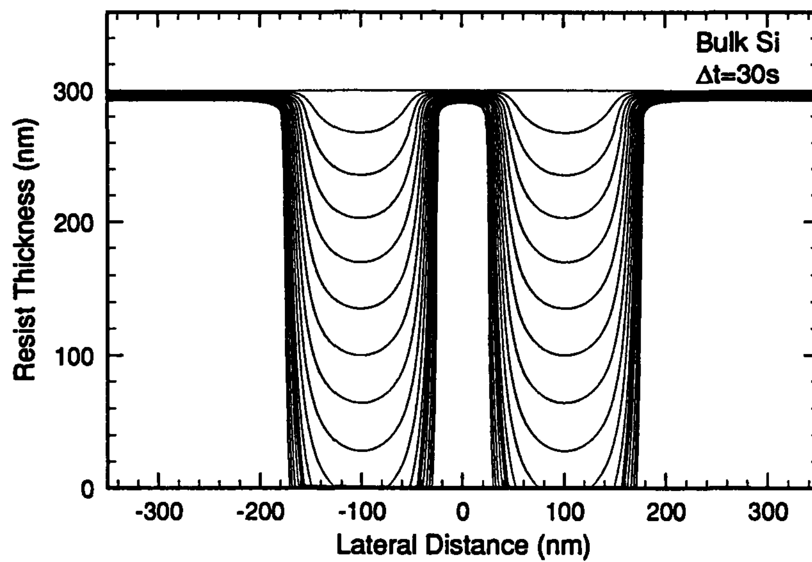


Figure 3.11 Resist contours are various times during development for the energy deposition pattern corresponding to a bulk silicon substrate in Figure 3.10.

written pattern diminishes the effect of the background energy deposition from long-range backscattered electrons.

The resist profile during development for the energy deposition pattern corresponding to a bulk silicon substrate is shown inFigure 3.11. The development profiles for the cases of a freestanding film of resist and resist on a membrane are nearly identical. As is apparent from the figure, in order to pattern 100nm lines separated by 100nm, it is necessary to introduce a bias during the electron-beam patterning. In this case, a 10nm bias is required to achieve the desired linewidth.

Chapter 4

Fabrication Technology

4.1 Nanolithography technology

4.1.1 System considerations

Much work has been done within the Submicron Structures Laboratory (SSL) to develop proximity x-ray lithography as a viable tool for advanced semiconductor manufacturing. A schematic of the proximity x-ray system used in this work is shown in Figure 4.1 (a). X rays are generated by bombarding a water-cooled copper target with high energy electrons (8 keV). The incident high-energy electrons have a certain probability of exchanging energy with inner shell electrons, causing ionization and thereby creating an inner shell hole. An x ray is emitted when an electron from a higher energy level fills this hole. The emitted x ray wavelength is thus characteristic of the target material. For the source used in the work, the x-ray wavelength corresponds to the Cu_L line ($\lambda = 1.32$ nm). The target serves as a "point source" for x rays which then irradiate the substrate through the x-ray mask, as shown in Figure 4.1 (b).

X-ray lithography has many advantages for patterning features below 100 nm, including short wavelength compatible with printing small features ($\lambda \sim 1$ nm), no requirement of complicated

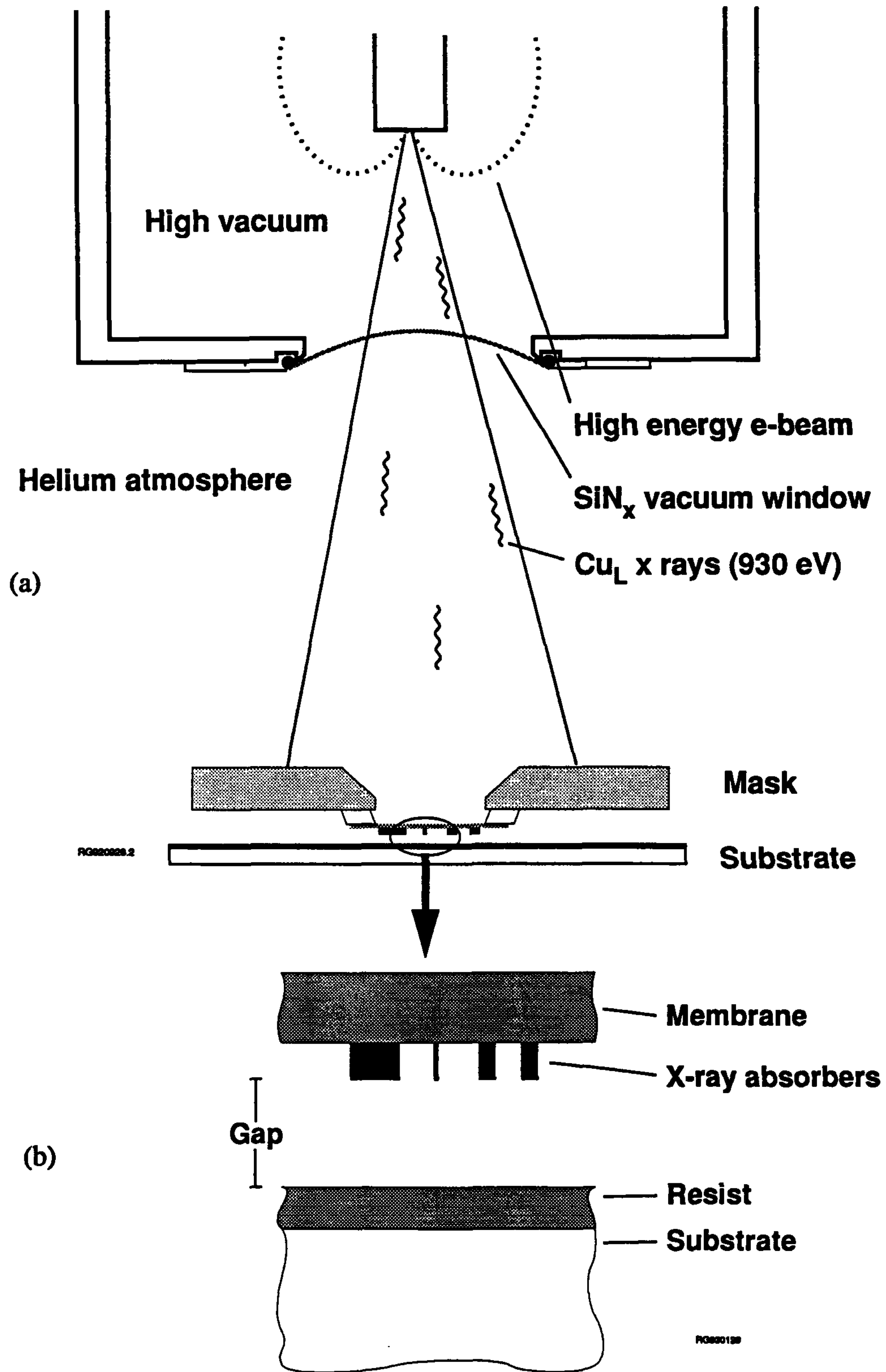


Figure 4.1 (a) Schematic of x-ray lithography source used in this work.
(b) Close up of proximity gap.

optics to correct for aberrations and distortions, and absorption without scattering, making exposure substrate independent and devoid of scattering effects such as standing waves and the proximity effect. Also, x-ray lithography enjoys a very large depth-of-focus compared to optical projection lithography, making exposures virtually independent of substrate topography. These factors combine to permit the achievement of vertical resist side walls, even with thick resist.

Many of the advantages of x-ray lithography stem from the simplicity of proximity printing, which is essentially a shadow casting technique. However, this gives rise to a tremendous technological challenge in mask fabrication. Because proximity printing is a 1:1 process, features on the mask must be the same size as what is ultimately desired on the substrate.

In addition, the gap between the mask and the substrate must be quite small in order to avoid diffraction effects. For a proximity printing technique such as x-ray lithography, the minimum feature size, W, is given by the expression

$$W = \sqrt{\frac{\lambda G}{\alpha}} \quad , \tag{4.1}$$

where G is the gap between the x-ray mask and the substrate, λ is the wavelength of the source, and α is a parameter that can be as large as 1.5 if exposing with a source with an optimized spatial coherence [53]. For the wavelengths used in x-ray lithography, Equation (4.1) implies that in order to print a 100 nm feature with $\lambda = 1$ nm, a gap of less than 15 μm is required.

Several factors must be considered when selecting the appropriate materials for the mask membrane and the x-ray absorber. First, in order to maximize throughput, care must be taken

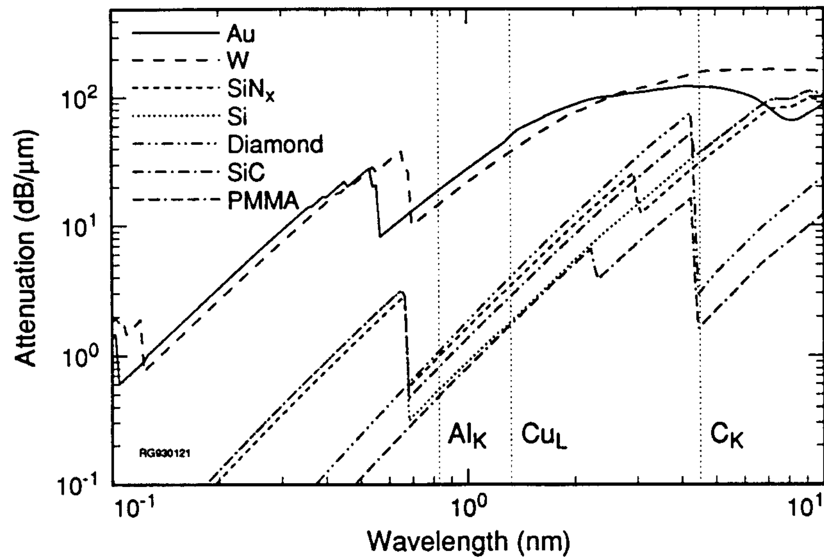


Figure 4.2 Attenuation of x rays for materials commonly used in x-ray mask fabrication, as a function of x-ray wavelength.

to select a membrane material that is reasonably transparent at the x-ray wavelengths of interest. The attenuation versus wavelength of various materials that are commonly used for x-ray mask membranes and absorbers are shown in Figure 4.2. For silicon-nitride, which is the membrane material used in this work, attenuation at the Cu_L line is 3 dB/µm, implying a maximum reasonable membrane thickness of 1–2 µm.

In addition, absorber materials must be sufficiently thick as to significantly attenuate x rays, without being so thick as to make fabrication technologically prohibitive. For example, ~200 nm of gold is required for 10 dB attenuation at the Cu_L line. Thus, it is not uncommon to require that absorbers be taller than they are wide.

Secondly, in order to be manufacturing compatible, an x-ray mask technology is required that can work at small mask/substrate separations while minimizing the risk that the mask will crash into the substrate. For gaps of ~10 µm, this means that the x-ray mask membrane must be

optically flat over the entire diameter of the mask (which is usually 30 mm or more), and quite strong. In addition, because semiconductor manufacturing requires several levels of lithography, the mask needs to be distortion free to some small fraction of the minimum linewidth.

Lastly, to be useful in production, it is important that prolonged exposure to x-ray radiation not change the properties of the mask material. There is some concern that silicon-nitride may not be completely radiation hard, although there are indications that silicon-nitride can be made radiation hard by excluding oxygen from the chamber during deposition [54]. Even if silicon-nitride is shown to be unsuitable for manufacturing due to radiation softness, it is nevertheless very useful for research and development.

4.1.2 X-ray mask blank preparation

For this work, extensive use was made of the SSL's standard 31 mm-diameter silicon-nitride x-ray mask blanks [55,56]. These masks consist of an optically flat, ~1 µm thick silicon-nitride membrane supported on a silicon ring anodically bonded to an optically flat Pyrex© frame.

The mask fabrication process is shown schematically in Figure 4.3. First, low-stress silicon-rich silicon-nitride is deposited on silicon wafers using low-pressure chemical-vapor deposition (LPCVD). The silicon-nitride is removed from the back surface of the mask, and the wafers are quartered. Next the bare silicon surface is anodically bonded to an optically flat Pyrex ring, manufactured from a material chosen to a thermal expansion coefficient that closely matches silicon. The bonding is done by applying 1500 V between the silicon wafer and the Pyrex ring while heating the components to ~300 °C. After bonding, the silicon-nitride of the front

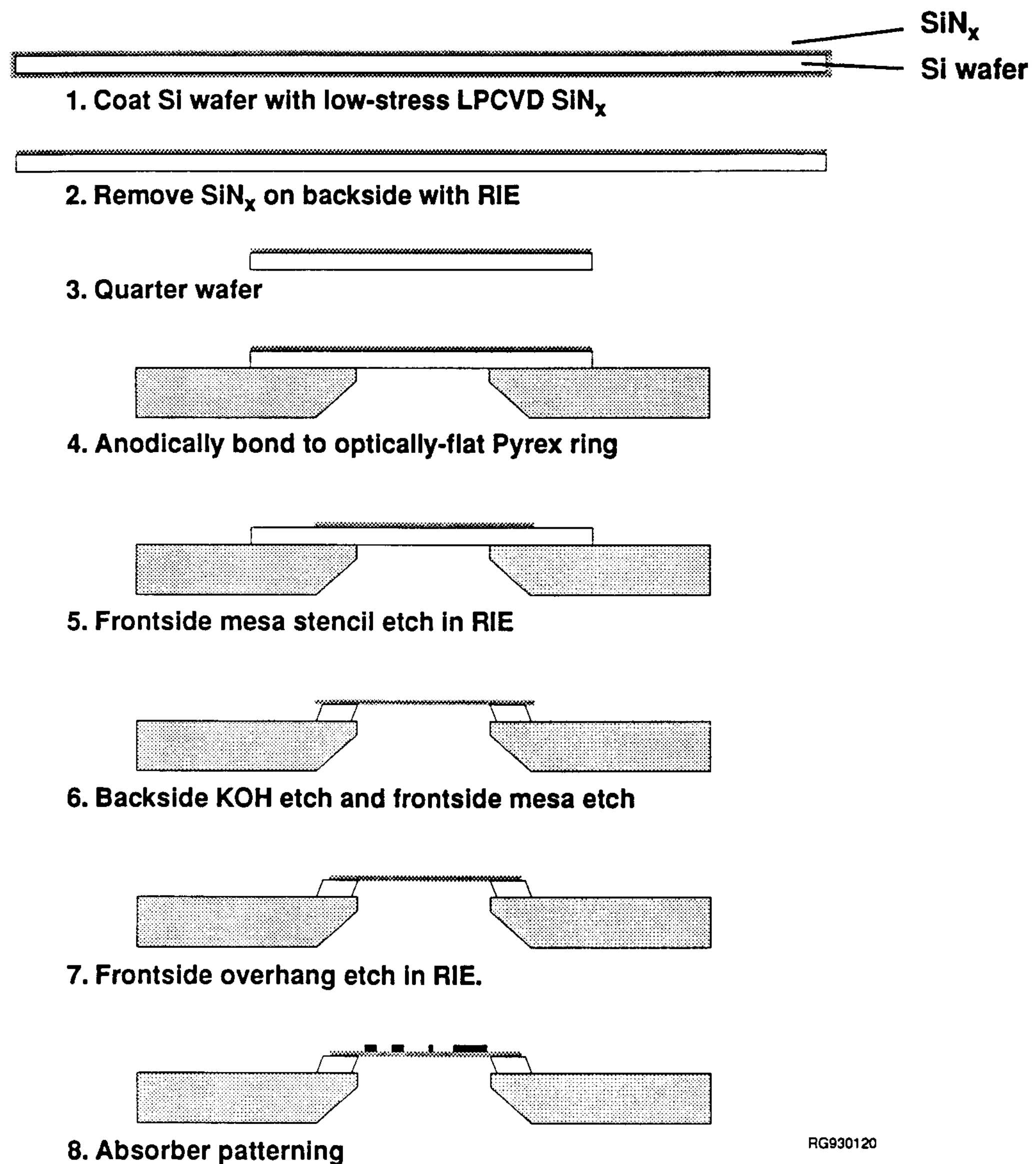


Figure 4.3 X-ray mask blank fabrication sequence.

surface is patterned, and the silicon is etched in KOH. What remains is a freestanding silicon-nitride film supported by a narrow rim of silicon which has been anodically bonded to the Pyrex ring. Finally, the silicon-nitride near the edge of the mesa rim is etched away to eliminate any overhang and facilitate electrical contact over the mesa edge in subsequent steps.

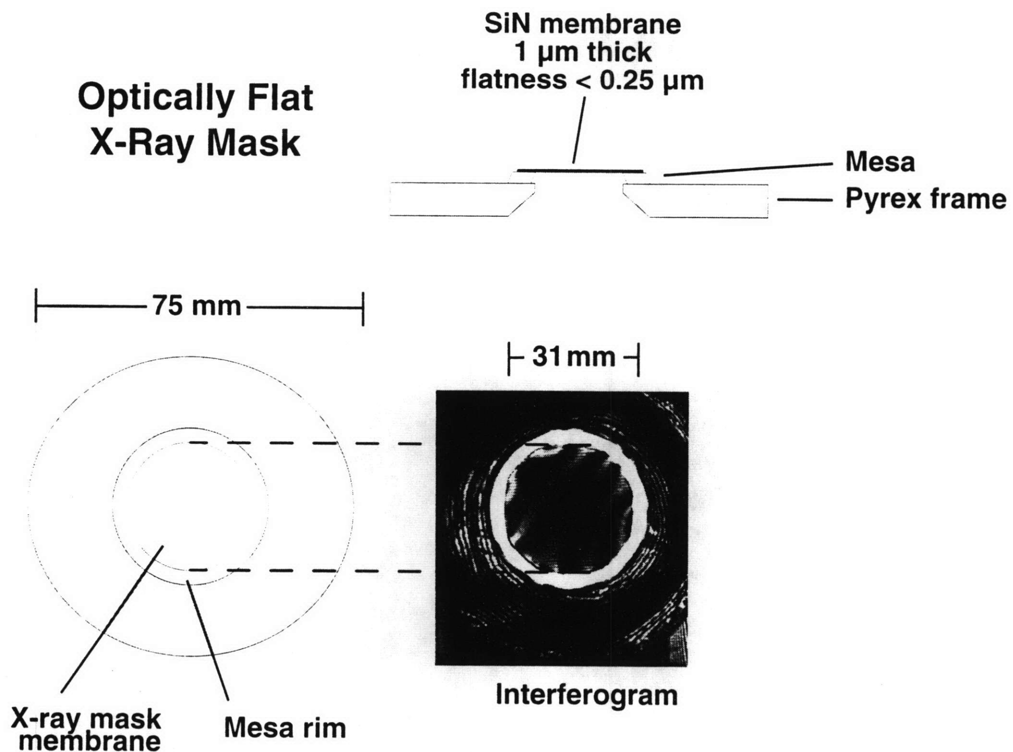


Figure 4.4 Schematic of finished x-ray mask, along with interferogram showing the flatness of the mask membrane.

The finished masks are optically flat to less than 250 nm, as shown in Figure 4.4, although there is usually bowing on the order of 1 μm along the mesa rim. This degree of flatness is sufficient for working at mask/substrate gaps of 3 μm in a research setting, although there is still room for improvement. However, a process has been recently developed [57] that results in masks that are flat to less that 100 nm, with minimal distortion on the mesa rim. This new flip-bonding technique also promises to greatly simplify mask manufacturing.

After cleaning, a thin plating base (NiCr:Au; 5:10 nm) is deposited on the membrane area, followed by a thick contact layer (Au 200 nm) on the mesa rim and Pyrex ring. The latter is to facilitate good electrical contact to the thin plating base. The membrane is then immediately coated with 300 nm of poly-(methyl-methacrylate) (PMMA) resist (typically 950 K molecular

weight). The resist is removed at four spots along the mesa rim, and the mask is baked at 180°C for one hour. Afterwards, the region where the resist was removed is scratched to provide a feature that can be focused on prior to patterning using direct-write electron-beam lithography.

4.1.3 X-ray mask fabrication

After a mask pattern has been designed, it is converted into a form suitable for a JEOL JBX-5DII electron-beam lithography system, and transferred electronically to the Naval Research Laboratory in Washington, D. C. The x-ray mask blank is then typically patterned using an acceleration voltage of 50 keV, a beam current of 500 pA, and an areal dose of 450 $\mu C/cm^2$. Large features are patterned at a significantly higher beam current to minimize writing time.

There are several advantages when patterning x-ray mask membranes as opposed to bulk samples. First, the optical flatness of the membranes ensures that the beam will be well focused across the entire sample. This is in contrast to bulk samples, which typically have a potato-chip like surface. This variable surface profile causes the electron beam to become defocused in various areas, causing a blurring of features.

Second, because patterns are being written on a thin membrane, a significant portion of the incident electrons exit the back side rather than scatter back into the resist, as happens on solid substrates. This backside escape serves to minimizes the proximity effect [59], as discussed in Section 3.5 and shown schematically in Figure 4.5 (a). As a result, there has been little need to alter the exposure dose for different pattern geometries in order to achieve a reasonable degree of process latitude.

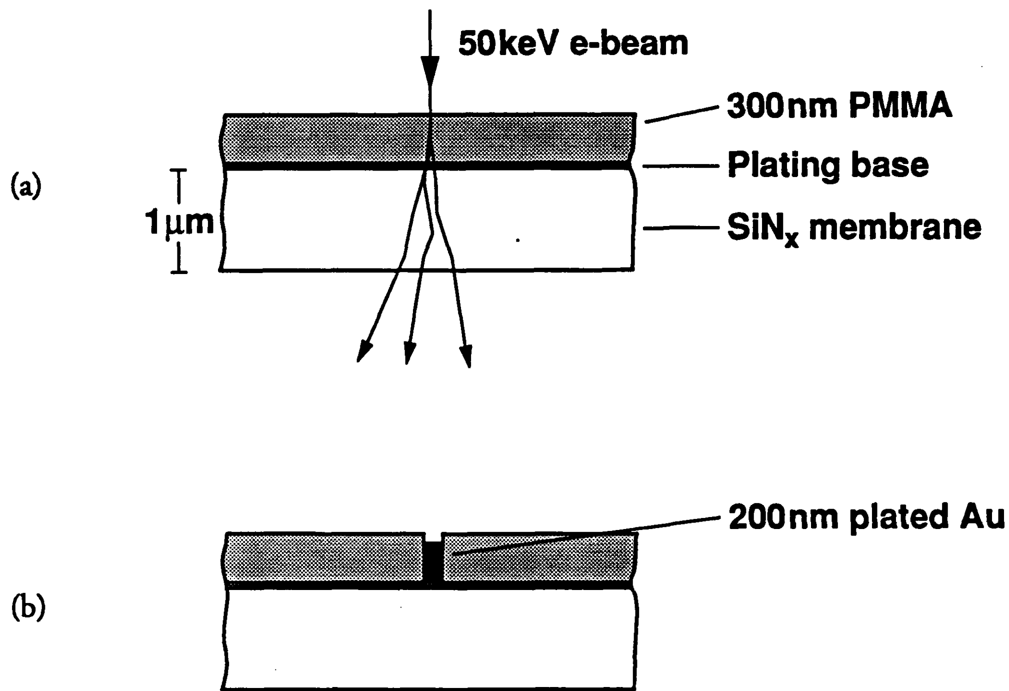


Figure 4.5 (a) Schematic of electron-beam patterning of an x-ray mask.
(b) Electroplating of gold x-ray absorbers using developed resist as a mold.

This enhanced process latitude when patterning x-ray mask membranes is quite significant for manufacturing, where gigabit scale circuits require writing of dense patterns over very large areas with stringent linewidth control.

After exposure, the masks are immersion developed in a bath of 1:2 methyl-isobutyl-ketone (MIBK):isopropal alcohol (IPA) at 21 °C for 75 seconds, followed by a 30-second rinse in IPA. After a 6 second etch in an O_2 reactive ion etcher to remove any residual resist, low-stress gold absorber is electroplated [59] to a thickness of at least 200 nm, as shown in Figure 4.5 (b), which corresponds to 10 dB attenuation for Cu_L x-rays (λ=1.32 nm). After inspection in a scanning-electron microscope, the resist is removed with an O_2 plasma, and 3 µm thick aluminum studs are evaporated at several points along the mesa rim.

Figure 4.6 shows some typical scanning-electron micrographs of completed x-ray masks, taken after patterning by electron-beam lithography, development, and electroplating with gold absorbers. It is interesting to note the well-defined corners in the Figures 4.6 (a) and (c). The small radius of curvature gives some indication of the ultimate resolution attainable with the JOEL system used in this work.

At this point, the master x-ray mask is replicated onto another x-ray mask, producing a "child" mask. Replication serves two purposes: (1) to reverse the polarity of the master mask so that the child mask is suitable for exposing PMMA (a positive resist), and (2) to minimize risk to the master mask by removing it from everyday use. Replication of the master mask is typically done at a mask-to-mask gap of 3 μm to minimize diffraction effects, with the gap being set by the aluminum studs. The child mask is then developed and electroplated with gold absorbers. Finally, the absorber patterns on the child mask are encapsulated with a 400 nm-thick layer of polyimide. The polyimide serves both to protect the patterns and as an insulating layer during device processing.

4.2 Modulation-doping

For many years, there has been significant interest in developing electronic devices using GaAs, primarily because of the high electron mobility available in this material system compared to silicon. The first and most popular of these devices was the metal-semiconductor field-effect transistor (MESFET), in which carriers travel along a doped-channel whose conductivity can be modulated by a gate.

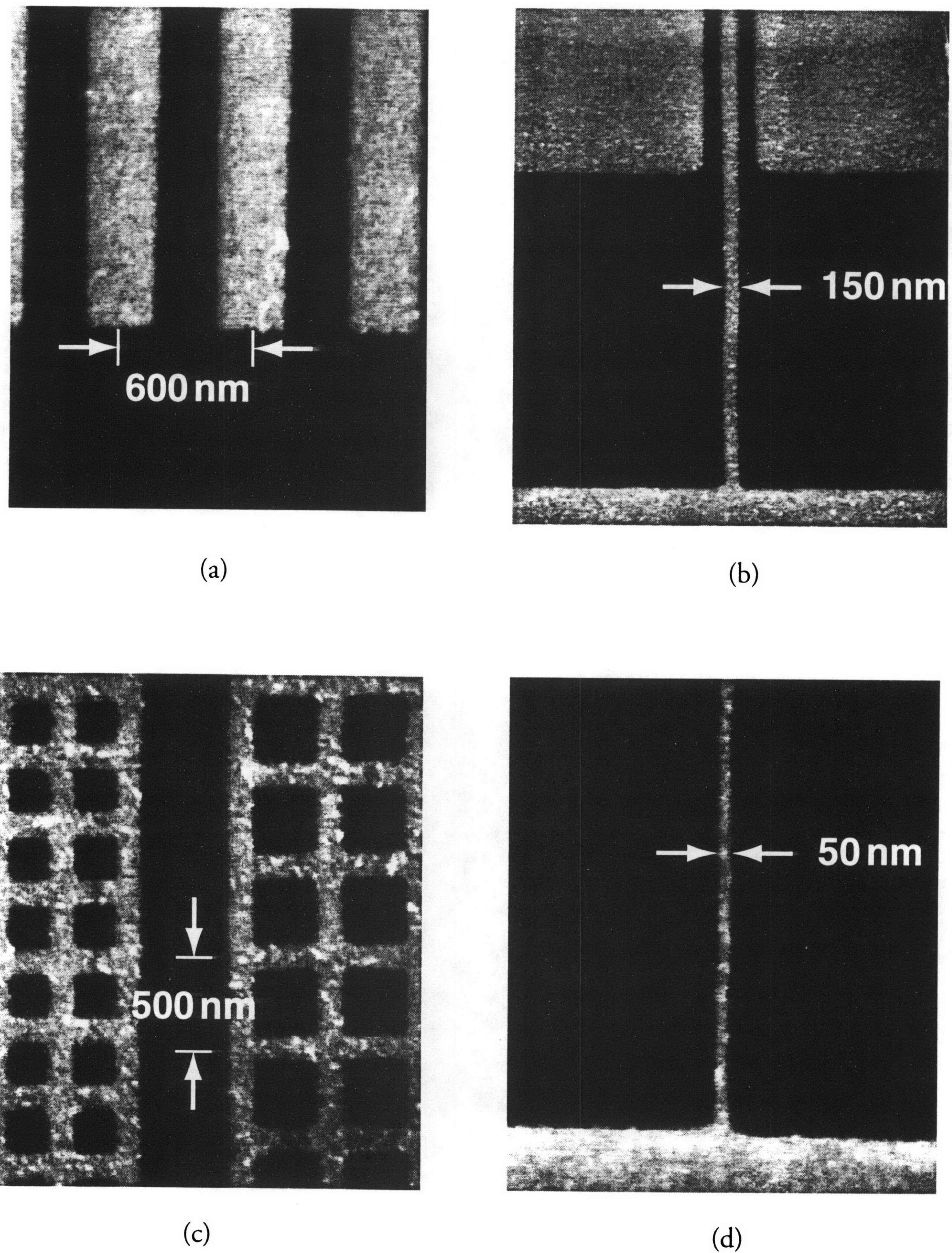


Figure 4.6 Thick electroplated gold patterns on master x-ray masks after patterning by electron-beam lithography for (a) etch mask used to define Q1D wires, (b) tunnel-gate mask to define tunneling barriers for the Q1D-PRESTFET, (c) sample grid-gate patterns used to fabricate grid-gate HEMTs, and (d) gate pattern for deep-submicron short-channel MOSFET.

The need for more control in fabricating MESFET structures motivated the development of advanced material growth techniques such as molecular-beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). These growth techniques have become sufficiently advanced that it is possible to control material deposition on a monolayer by monolayer basis, making possible the growth of abrupt heterojunctions.

For the GaAs/AlGaAs system, the ability to control material composition during growth has led to "band-structure engineering" and the development of many novel structures, including the heterojunction bipolar transistor (HBT) [60], the resonant tunneling diode (RTD) [61], and the high electron mobility transistors (HEMT or MODFET) [62]. Of these, the HEMT has had the greatest impact in physics studies, including a central role in the discovery and investigation of the quantization of conductance [9,10], and the integer [63] and fractional [64] quantum Hall effect (although the first observation of the quantum Hall effect was in the silicon system).

4.2.1 Conventional HEMT

In conventional GaAs MESFETs, the channel between source and drain is usually made with highly n-doped GaAs. As a result, the electrons which carry current in the device travel through the same layer that contains the ionized impurities that give rise to these electrons. The coulombic interaction between the electrons and ionized donors leads to ionized impurity scattering, which is the principle cause of low electron mobility in these structure.

Ionized impurity scattering can be greatly reduced using modulation-doping. In 1978, Dingle *et al.* [65] reported the first modulation-doped structure in a GaAs/AlGaAs superlattice,

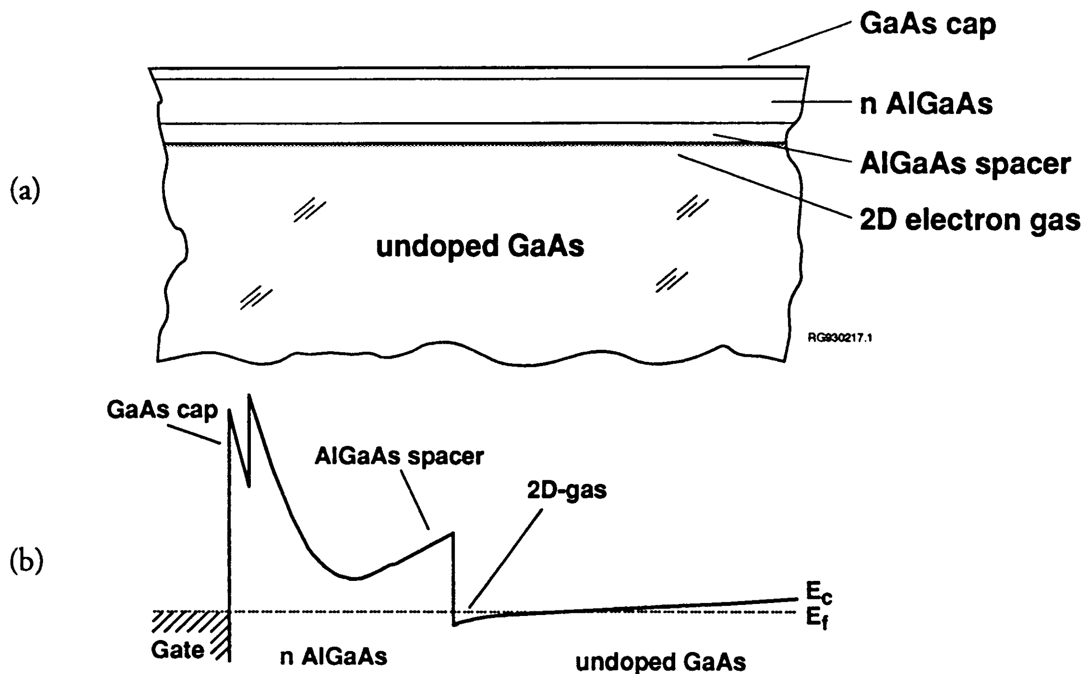


Figure 4.7 (a) Typical layer structure for modulation-doped GaAs/AlGaAs HEMT. (b) Energy band diagram for (a).

which was selectively doped only in the wide bandgap AlGaAs. By separating the carriers from the impurities that induce them, ionized impurity scattering is greatly reduced, leading to significantly higher electron mobilities than can be achieved in conventional doped-GaAs structures.

A schematic of a modulation-doped GaAs/AlGaAs heterojunction is shown in Figure 4.7, along with the band diagram for the system. By growing a doped layer of the wide bandgap AlGaAs on top on an undoped layer of the narrow bandgap GaAs, electrons diffuse from the AlGaAs to the GaAs. The depletion layer in the AlGaAs then attracts the electrons back to the heterointerface, confining the electrons to a very narrow (~8 nm) potential well. The band

bending at the interface leads to quantization of the electron energies perpendicular to the surface and hence, a two dimensional electron gas.

By separating the electrons from the doped material and confining them to the undoped material, ionized impurity scattering is significantly reduced. Scattering can be further reduced by including an undoped wide bandgap AlGaAs spacer layer between the doped layer and the undoped layer to further separate the electrons from the ionized impurities.

Because ionized impurity scattering is the dominant scattering mechanism in these devices at low temperature, HEMT structure have been reported with extremely high electron mobilities at cryogenic temperatures. The current record is $1.1\times10^{7}\,cm^{2}/Vs$ at 4.2 K [66], compared with a maximum attainable mobility of $10^{4}\,cm^{2}/Vs$ for conventional MESFET structures. As was discussed in Section 2.1.2, low temperature mobility is an important figure of merit for quantum-effect devices.

At low temperatures, the primary remaining scattering mechanisms include remote ionized impurity scattering and interface roughness at the AlGaAs/GaAs interface. By suitably controlling growth conditions, it is possible to minimize interface roughness [67]. Also, by increasing the spacer thickness, impurities can be further removed from the carriers. However, if the spacer thickness becomes too large, the electron density in the two-dimensional electron gas begins to decrease, reducing the screening of remote impurities, and hence, reducing the mobility [68].

For quantum effect devices that derive their functionality from electrostatic confinement of carriers, a wide spacer has the negative effect of further removing the gate electrodes from the

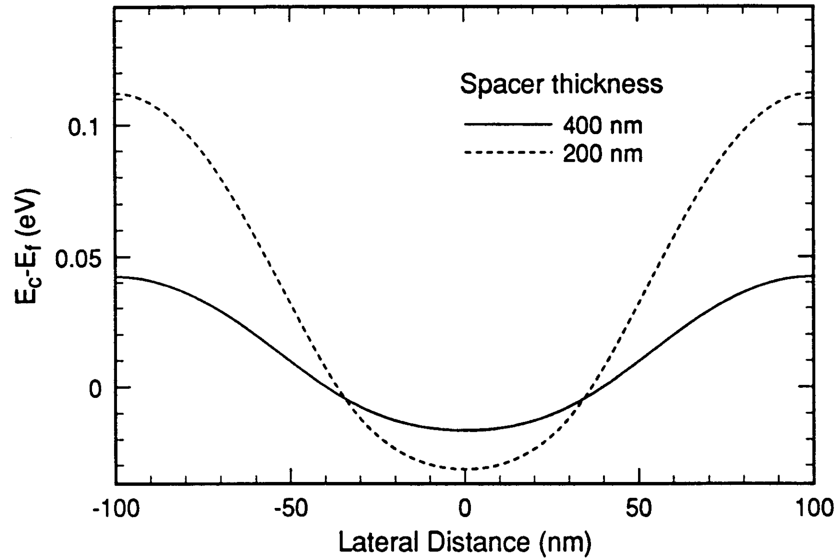


Figure 4.8 Potential seen by electrons at the plane of the two-dimensional electron gas when a lateral superlattice potential is applied to HEMT structures with different spacer thicknesses.

electrically active region of the device, causing confinement potentials to become softer, and hence, weaker quantization. This is shown schematically in Figure 4.8.

For this work, conventional device substrates are high quality AlGaAs/GaAs modulation-doped material grown in a Varian GEN II MBE system at Purdue University, typically starting with a 1 µm undoped GaAs buffer on a semi-insulating GaAs substrate followed by a 20 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer, 30 nm $Al_{0.3}Ga_{0.7}As$ doped n-type to $1.5\times10^{18}\,cm^{-3}$, and a 5 nm GaAs cap doped n-type to $1.5\times10^{18}\,cm^{-3}$. At 4.2 K, Hall mobilities after processing are typically on the order of $6\times10^{5}\,cm^{2}/Vs$, with electron densities on the order of $5\times10^{11}\,cm^{-2}$.

4.2.2 Back-gated HEMT

An alternative type of HEMT is the back-gated HEMT, where a doped-substrate can be used to modulate the density of electrons in the two-dimensional electron gas. This is particularly

useful for field-effect controlled QEE devices, where a finely patterned surface gate is used to induce a confining potential that the electrons in the channel interact with. By being able to independently control the electron density, the back gate can be used to probe the confining potential established by the surface gate. This is in contrast to similar devices fabricated on a conventional HEMT substrate, where the surface gate modulates the electron density and the confinement potential seen by the electrons at the same time.

This utility of this added capability was clearly shown by Meirav *et al.* [69], where a back-gated inverted HEMT configuration [70] was used to fabricate a single-electron transistor. In this device, gates on the surface of the device were used to define a single quantum dot, and the back gate used to add electrons, one at a time, to the quantum dot, changing the conductivity of the device by over two orders of magnitude.

For this work, some preliminary characterization was done of back-gated device substrates of high quality AlGaAs/GaAs modulation-doped material grown in a Varian GEN II MBE system, starting with a 300 nm GaAs buffer heavily doped p-type, on a p-type GaAs substrate, followed by 700 nm of p-type GaAs, a 100 nm undoped $Al_{0.3}Ga_{0.7}As$ barrier layer, 900 nm of undoped GaAs for the channel layer, a 20 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer layer, 60 nm $Al_{0.3}Ga_{0.7}As$ doped n-type to $1.5\times10^{18}\,cm^{-3}$, and a 5 nm GaAs cap doped n-type to $1.5\times10^{18}\,cm^{-3}$. Electron density versus backgate bias is shown in Figure 4.9, clearly showing the ability of the back gate to modulate the electron density in the two-dimensional electron gas.

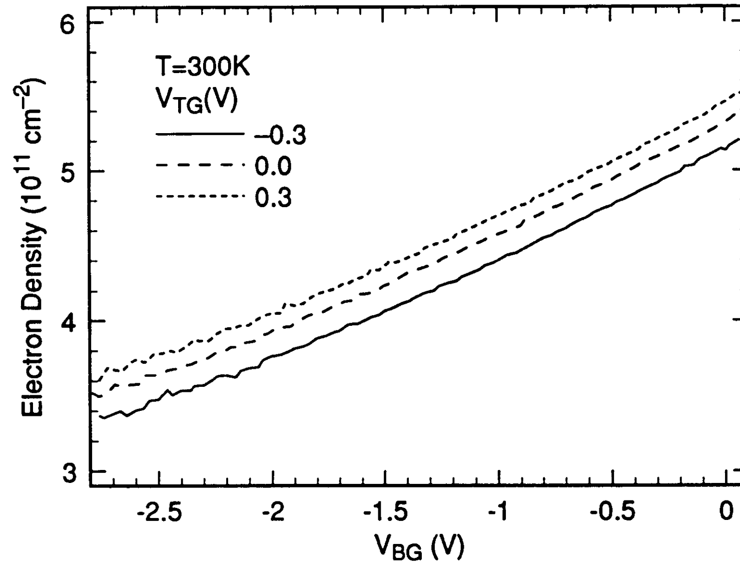


Figure 4.9 Measured electron density versus back-gate bias for various top-gate voltages, for a back-gated HEMT.

4.3 Q1D conductor fabrication

A schematic overview and cross-section of the device to be described in this section is shown in Figure 4.10. By etching away the doped material in selected areas, surface depletion can be used to deplete the two-dimensional electron gas in specific areas [71]. By suitably controlling the etch depth, a series of parallel Q1D wires that have electrical widths ideally below 100 nm may be fabricated. By placing a gate over the wires, it is possible to capacitively control the density of electrons in the wires, and thus probe the confining potential. Because the energy level separation is small, devices need to be measured at cryogenic temperatures (<10K) to resolve these individual levels.

4.3.1 Conventional processing

Devices are first isolated by etching in an NH_4OH:H_2O_2:H_2O (5:3:80) solution for 6 seconds, etching through the plane of the two-dimensional electron gas. Ohmic contacts are

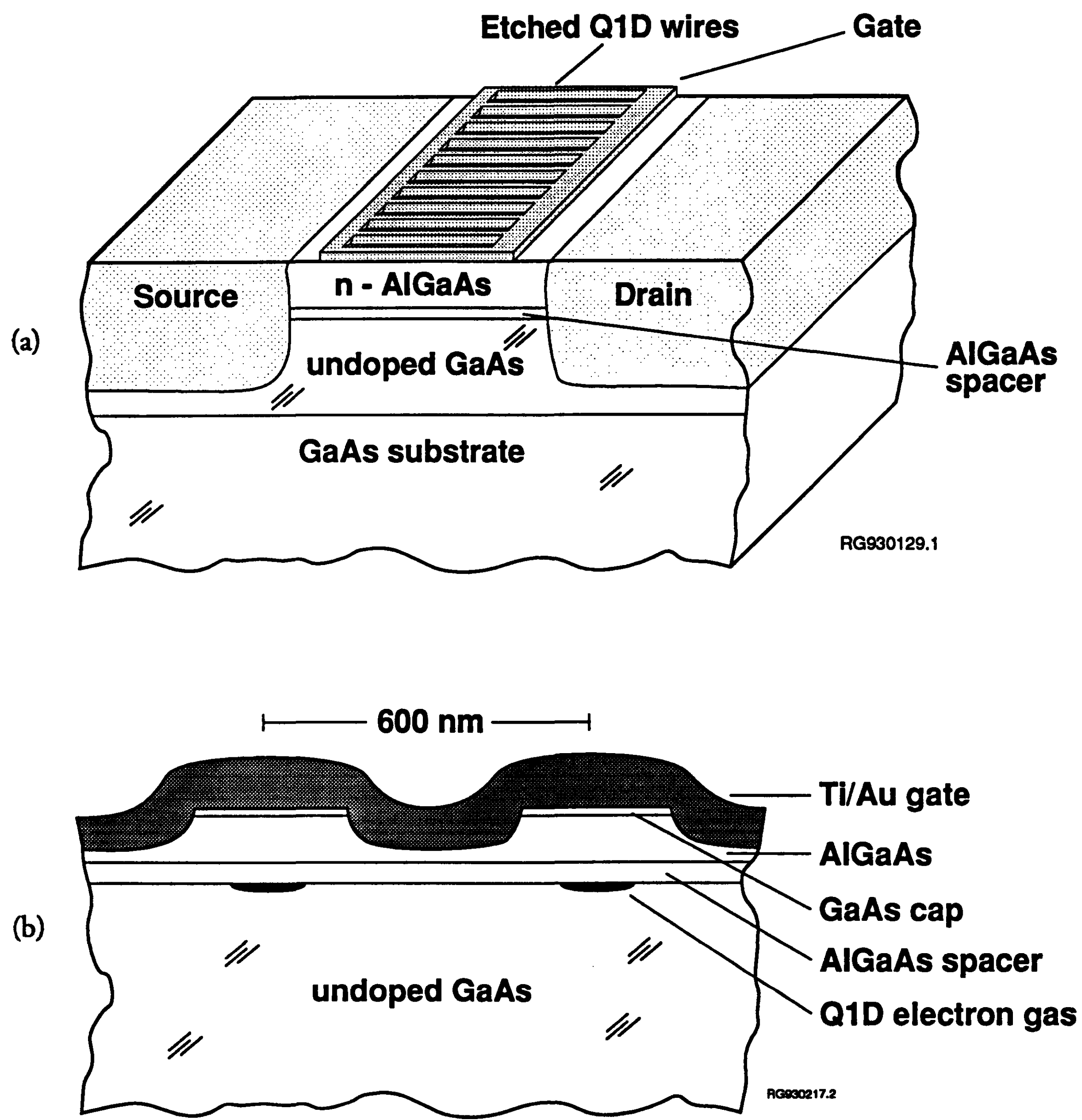


Figure 4.10 (a) Schematic overview and (b) schematic cross-section of completed Q1D device.

then evaporated (Ni:Au:Ge:Au:Ni:Au; 2:4:22:44:10:30 nm) using an electron-beam evaporator, and alloyed at 450 °C for 10 seconds. Back-gated samples are typically alloyed at 430 °C to minimize the risk of the ohmic contacts diffusing through to short to the conducting substrate. Bonding pads are then deposited (Ti:Au; 20:130 nm). The samples are then cleaved into individual dies (typically 5×7 mm) and coated with 200 nm of PMMA.

4.3.2 X-ray lithography of small samples

Because resolution in proximity x-ray lithography is limited primarily by the mask-to-sample gap [53], it was necessary to develop a technique to expose, at a sufficiently small gap, small samples (e.g. 5×7 mm) with large area x-ray masks (31 mm-diameter). With samples larger than the size of the mask membrane, controlling this gap is relatively straightforward using a microgap technique [55]. In this technique, aluminum studs on the mesa rim of the membrane set the mask/substrate separation. However, there are many circumstances where it is not feasible to commit a large substrate to a single experiment. Examples include the fabrication of quantum-effect devices and devices for magneto-optical studies [12,25], both of which typically make use of high quality, high mobility AlGaAs/GaAs modulation-doped material. For these types of samples, a novel conformable x-ray mask technology was developed to enable exposure of arbitrary sized samples using standard x-ray masks [72].

The daughter mask and substrate are aligned by first planarizing the mask with respect to the substrate, which is mounted on an alignment stage. Once aligned, the substrate is raised to come into gentle physical contact with the mask. A voltage, typically 40–100 V, is then applied between the substrate and the plating base of the mask to bring the two into gentle electrical contact (the polyimide on the front side of the mask serves as an insulating layer). Once in

contact, the vacuum that is holding the substrate to the alignment stage is released, leaving substrate suspended in contact with the mask.

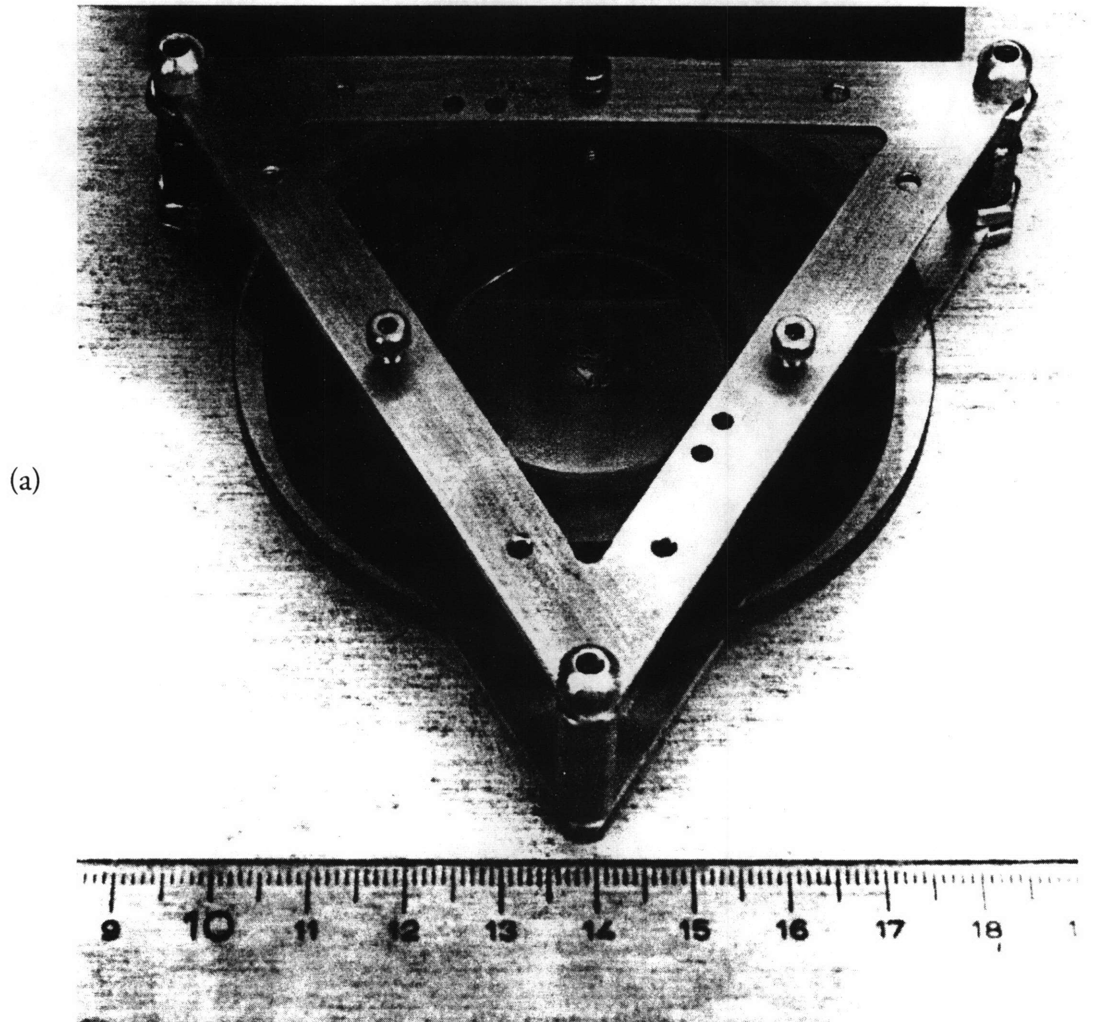
The mask/sample combination is then loaded into the specially designed exposure fixture shown in Figure 4.11 (a). A partial vacuum is then applied to the inside of the fixture, causing the x-ray mask membrane to deflect down around the sample and conform around any particles or resist buildup at the sample edges and corners, as depicted schematically in Figure 4.11 (b). The vacuum is controlled by use of a pressure regulator to less than 100 torr below atmospheric pressure. Empirically, the silicon-nitride membranes are extremely robust, even in the presence of large particles (> 10 μm) on the sample. However, these membranes can be quite fragile when subject to shear. Typical gaps between mask and sample are estimated to be less than 1 μm.

The sample is exposed in an electron-bombardment x-ray source operating at the Cu_L line ($\lambda = 1.32$ nm). The particular source used in this work is fitted with a silicon-nitride vacuum window [73], which allows exposure in a helium atmosphere. The silicon-nitride window also prevents stray high-energy electrons from bombarding the sample during the exposure, thus eliminating sample degradation during lithography [21]. After exposure, the partial vacuum is released and the sample is removed from the mask.

4.3.3 Precise etching of GaAs

After development, the Q1D wires are defined by a chemical etch to a depth of ~35 nm using a solution of H_2SO_4:H_2O_2:H_2O (1:1:40) at 18 °C, which yields an etch rate of approximately 2–3 nm/s [74]. A chemical etch is used in order to prevent damage to the sample surface [71].

(a)



(b)

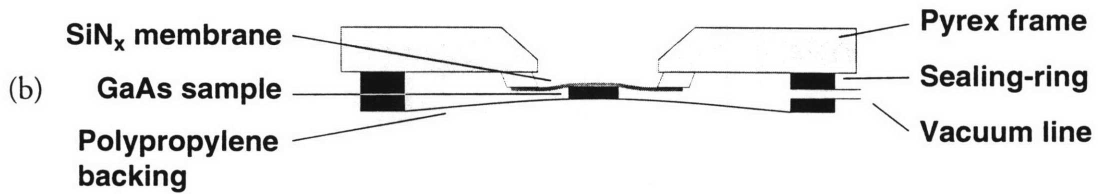


Figure 4.11 (a) Exposure fixture for conformable x-ray lithography on samples smaller than the x-ray mask membrane diameter. (b) Schematic showing x-ray mask membrane conforming around a small sample.

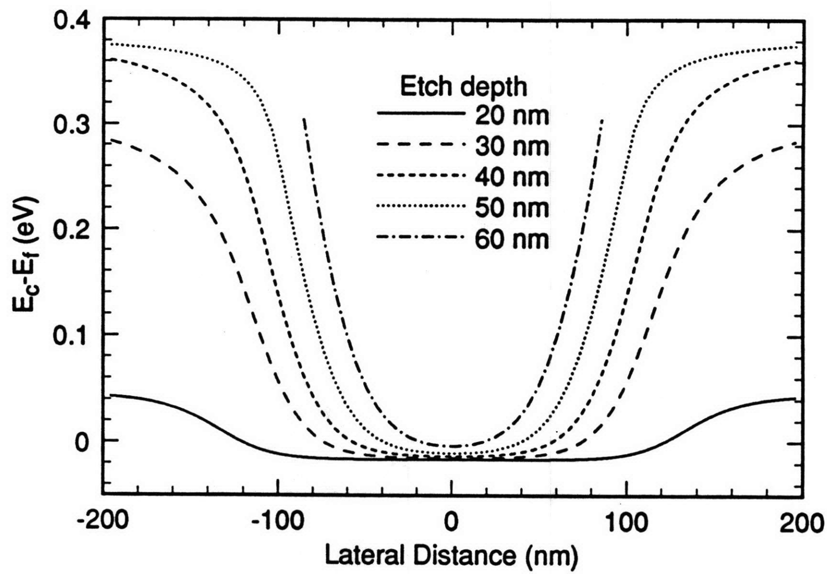


Figure 4.12 Modeled confining potential seen at the plane of the electron gas for the device shown in Figure 4.10 for various etch depths.

By etching away the doped material, the two-dimensional electron gas is depleted immediately beneath the etched regions, leaving behind many parallel quasi one-dimensional wires. By controlling the etch depth, the electrical width of the wires, and hence the degree of confinement, can be controlled. This is shown in Figure 4.12, where the simulated potential seen by an electron at the plane of the electron gas is shown for various etch depths. The simulation assumes an etch mask with a period of 600 nm and a linewidth of 300 nm.

Because the actual etch rate varies unpredictably from sample to sample, etch depth is monitored using a Linnik interferometer. After a brief period of etching, the sample is removed from the etching solution, rinsed, and measured in the interferometer. By monitoring how the interference fringes shift, it is possible to deduce the etch depth.

Since one fringe-spacing represents an optical-path difference of $\lambda/2$ (273 nm for the wavelength used in this work), additional effort must be made to resolve depth changes on the

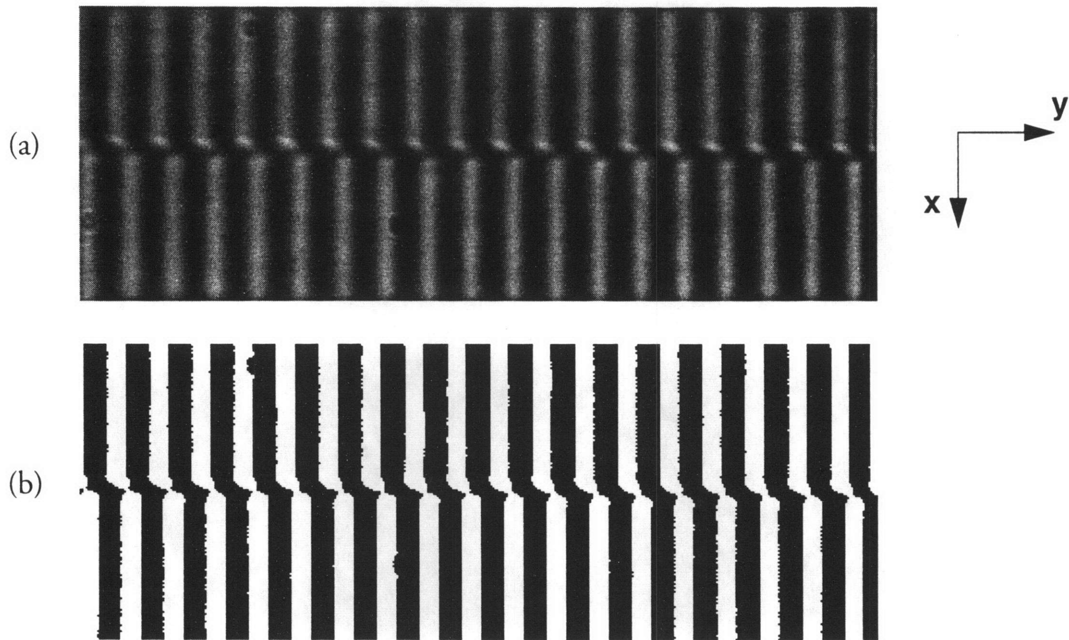


Figure 4.13 Image in Linnik interferometer during etching (a) before and (b) after initial enhancement.

order of 5 nm, which is required for reproducibility. In order to get such resolution, a charge coupled device array is used to electronically image the interferometric fringes of the Linnik interferometer. The digitized image is then digitally enhanced, and the fringe offset extracted using Fourier analysis techniques. A typical image before and after the initial enhancement is shown in Figure 4.13. The discontinuity in the fringe pattern corresponds to the boundary between the etched and unetched regions.

In order to extract the fringe offset with high precision, a spatial Fourier transform is done with the image in the y direction. Figure 4.14 shows the phase of the fundamental spatial frequency as a function of x. By fitting a line to the phase data in the etched and unetched regions it is possible to extract the phase-offset between the regions, which yields the

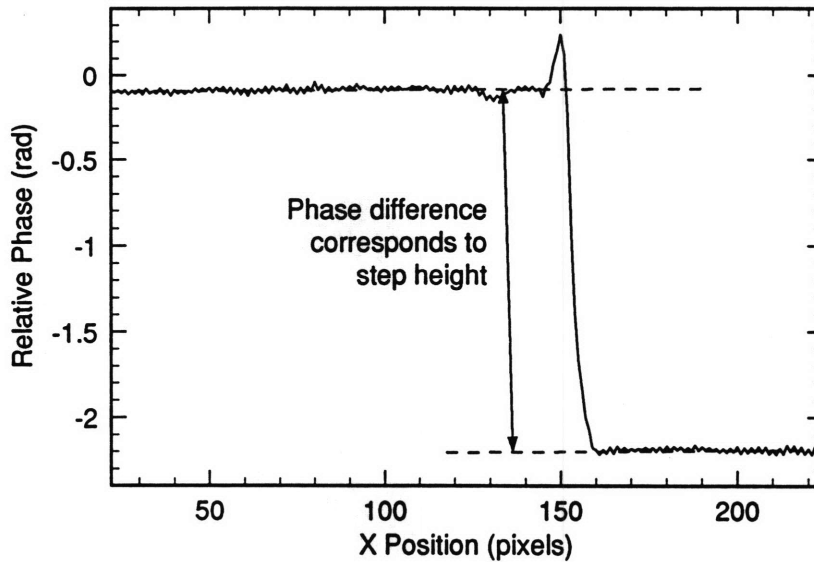


Figure 4.14 Phase of fundamental spatial frequency in Figure 4.13 as function of position along the x direction.

optical-path difference (and hence, the difference in height) between the two regions. This difference is measured frequently during etching, until the desired etch depth is reached.

It is interesting to note that the phase noise between pixels in Figure 4.14 is on the order of 1.6 nm. This low phase-noise means that given a sufficiently large number of fringes in the sampling window (>10), it is possible to easily resolve depth changes of the order of 2 nm by comparing the phase difference of the dominant spatial frequency in the etched and unetched regions. The repeatability of measurements is less than 1 nm.

After etching, the PMMA is removed and a Ti:Au (20:130 nm) gate is deposited over the wires. A scanning-electron micrograph of a typical finished device is shown in Figure 4.15.

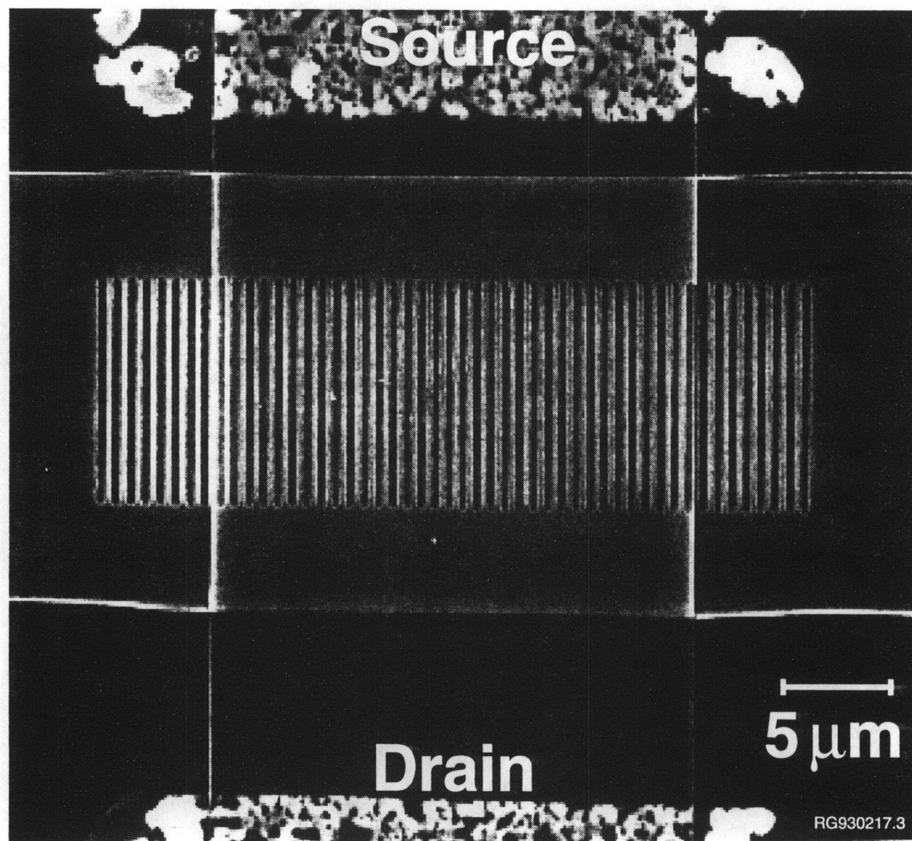


Figure 4.15 Scanning electron micrograph of typical Q1D conductor device, with many parallel Q1D conductors.

4.4 Q1D-PRESTFET fabrication

A schematic overview and cross-section of the Q1D-PRESTFET is shown in Figure 4.16. The fabrication sequence for the Q1D-PRESTFET is very similar to that of the Q1D conductors described in the previous section. After devices have been isolated and ohmic contacts defined, Q1D conductors are patterned and etched as described in Sections 4.3.2 and 4.3.3. After etching, the PMMA is removed and the sample is recoated with 300 nm of PMMA, and exposed with a second x-ray mask, having patterns similar to those shown in Figure 4.6 (b).After exposure, the sample is developed and Ti:Au (20:80 nm) lifted off.

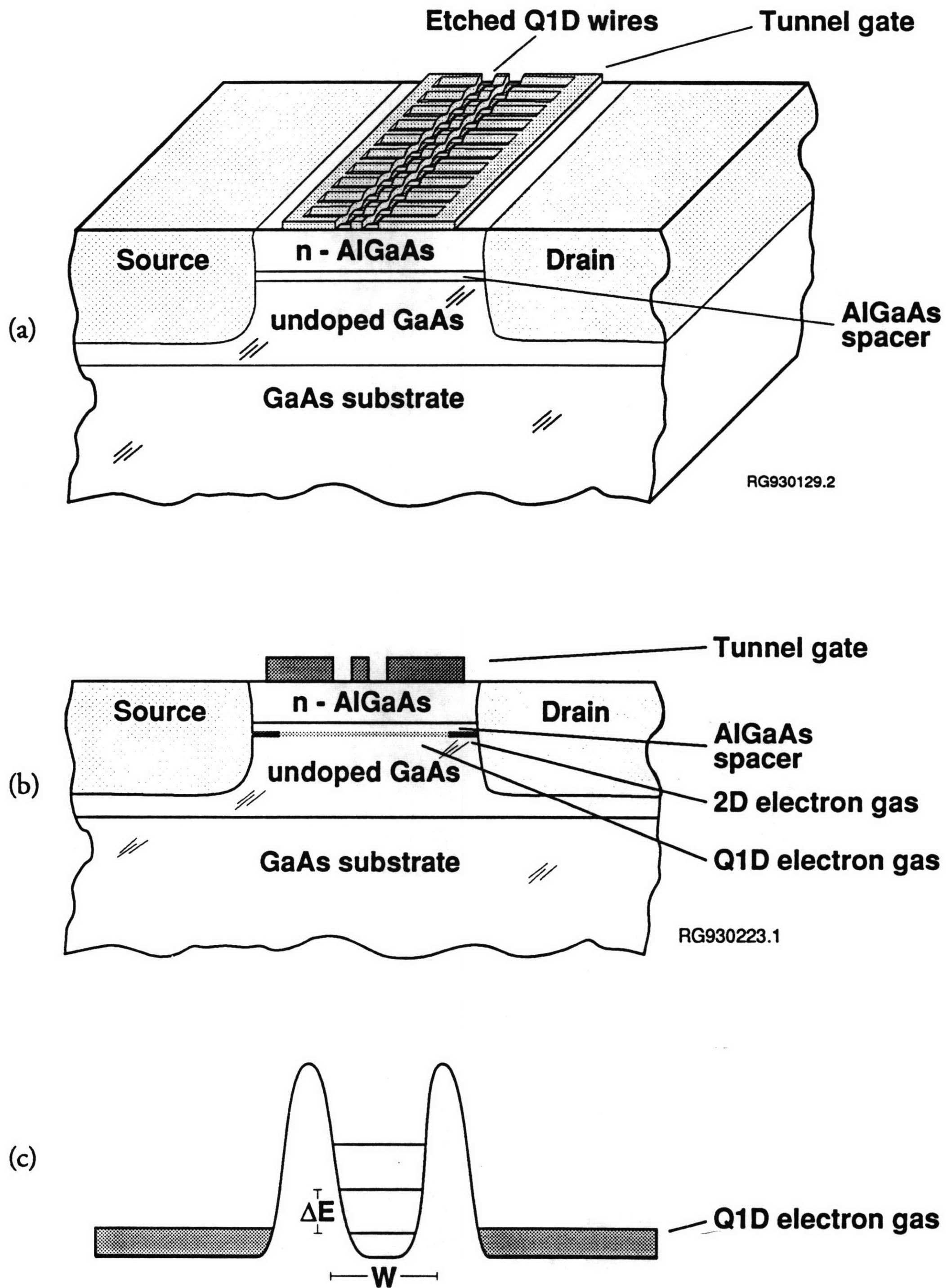


Figure 4.16 (a) Overview, (b) cross-section, and (c) potential seen by electron in Q1D-PRESTFET. Note that this device is an enhancement mode device, so tunnel gate must be biased positively to turn on the Q1D electron gas.

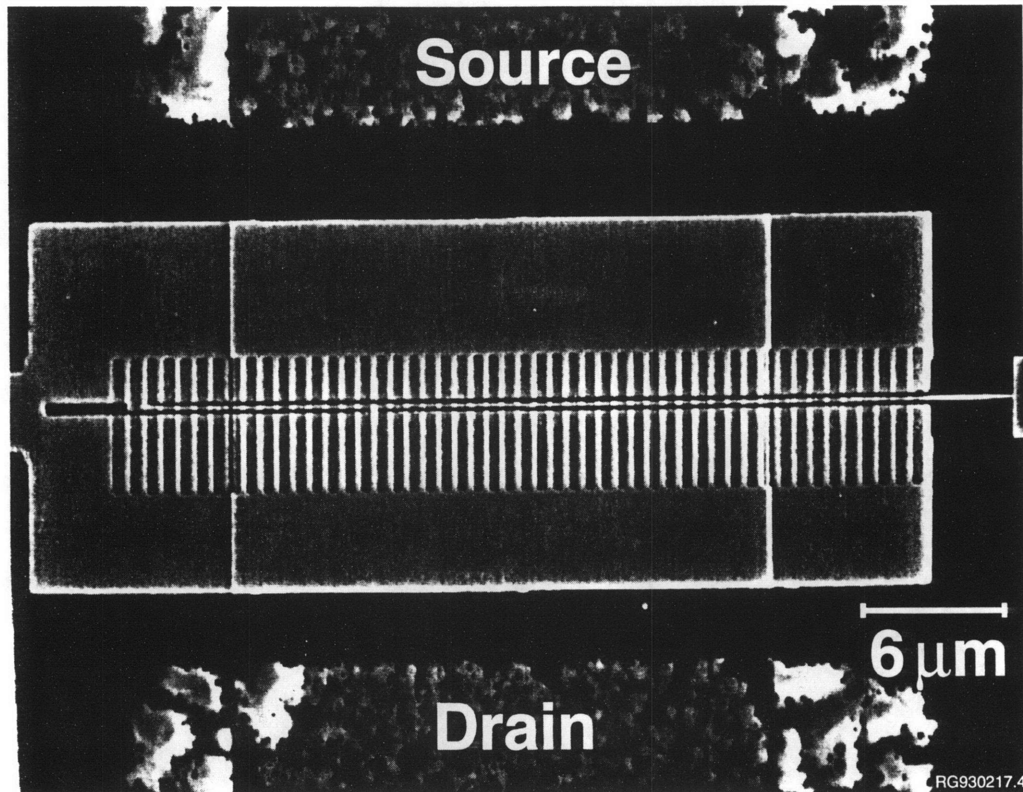


Figure 4.17 Scanning electron micrograph of typical Q1D-PRESTFET device, with many parallel Q1D conductors and tunnel gate.

For the Q1D-PRESTFET device, chemical etching of the Q1D conductors is required to minimize damage to the GaAs surface. This permits the deposition of a high-quality Schottky gate over the Q1D conductors. A scanning-electron micrograph of a typical finished device is shown in Figure 4.17.

Chapter 5
Measurements

5.1 Mobility degradation during lithography

Low-temperature mobility is an important figure-of-merit for QEE, where device operation generally relies on electrons being coherent over a long characteristic length. The higher the mobility in a particular sample, the higher the temperature at which quantum effects may be observed. Typically, quantum-effect devices require extremely small features (<100 nm) defined by either direct write electron-beam lithography (as is usually the case), x-ray lithography, or ion-beams. It is clear that mobility degradation by such high energy particles must be avoided.

In order to evaluate the suitability of these various lithography methods for QEE device fabrication, the mobility degradation in high-mobility, modulation-doped GaAs/AlGaAs samples was measured before and after irradiation in a JEOL JBX-5DII electron-beam lithography system, as well as before and after irradiation by Cu_L x-rays (λ=1.32 nm) in a helium atmosphere [21]. In all cases, samples were irradiated under conditions typical for

exposing poly-(methyl-methacrylate) (PMMA) with fine geometries [40,41], except that the samples were not actually covered with resist.

Hall mobility and two-dimensional electron density were measured before and after illumination over the temperature range of 4.2–300 K. At 4.2 K, mobilities were typically on the order of $6\times10^5\,cm^2/Vs$, with electron densities on the order of $5\times10^{11}\,cm^{-2}$ after illumination. After characterization, some of these same bonded Hall bars were exposed in a JEOL JBX-5DII electron-beam lithography system at an acceleration voltage of 50 keV, a beam current of 500 pA, and an areal dose of $450\,\mu C/cm^2$. One device on each header was left unexposed as a monitor. Other devices were exposed with a Cu_L x-ray source ($\lambda=1.32\,nm$). The particular source used in these experiments is fitted with a silicon-nitride vacuum window [73], allowing samples to be exposed in a helium atmosphere. The x-ray exposed Hall bars were irradiated with an areal dose of x-rays corresponding to roughly twice that necessary to completely expose the resist. Because these samples were already bonded in headers, it was not practical to coat them with PMMA. However, by irradiating devices that had already been characterized, sample to sample variations could be neglected. After irradiation, all the Hall bars were remeasured.

As shown in Figure 5.1 (a), the electron-beam-exposed samples all suffered significant mobility degradation, with typical mobilities on the order of $2\times10^4\,cm^2/Vs$ at 4.2 K, a degradation by a factor of 30. Room temperature mobilities were typically $2\times10^3\,cm^2/Vs$, a degradation of roughly a factor of two. Electron densities were lower after irradiation, as shown in Figure 5.1 (b), but not enough to account for the large degradation in mobility. The unexposed

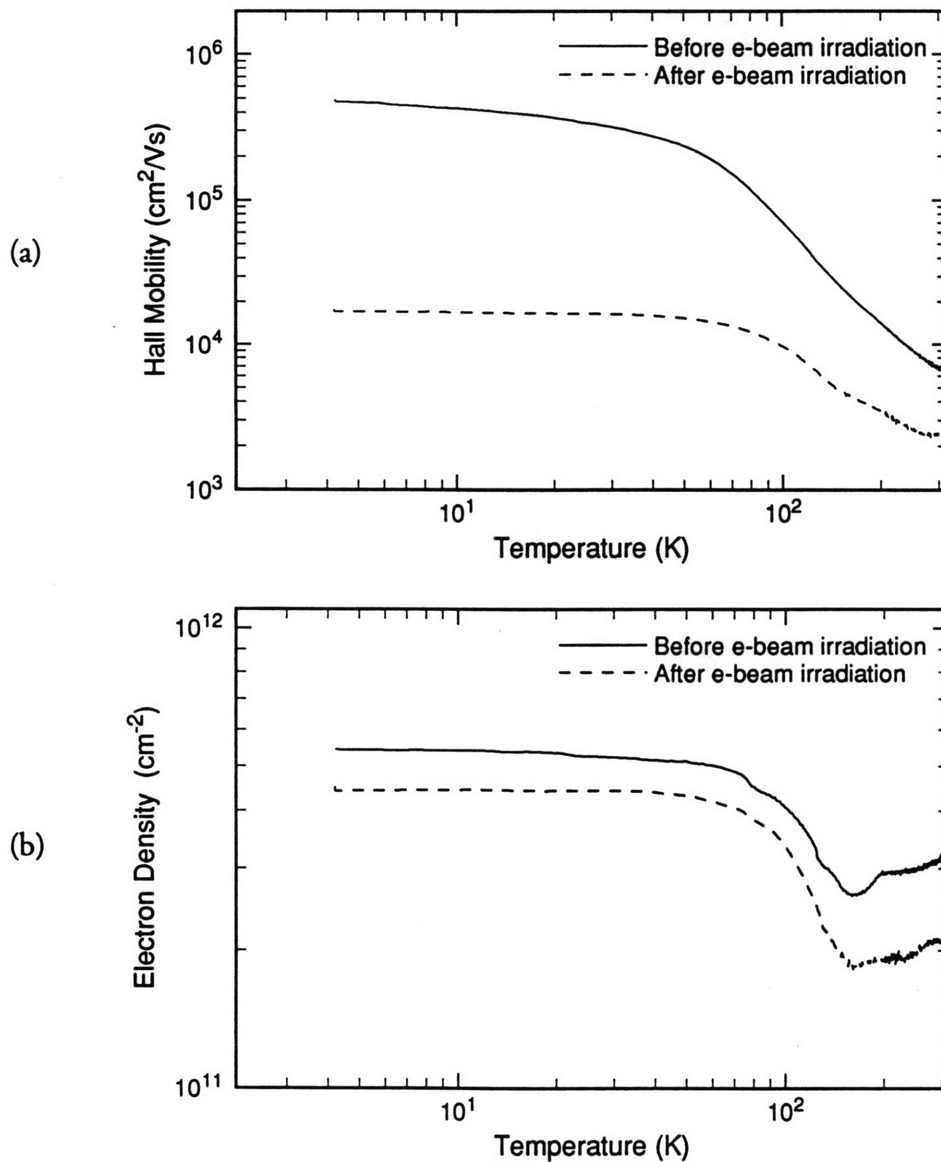


Figure 5.1 (a) Electron mobility and (b) electron density before and after electron-beam irradiation as a function of temperature.

Hall bars on the same header showed no change in mobility or electron density, eliminating the possibility of degradation due to sample handling.

In contrast, the x-ray exposed samples suffered from no apparent degradation in mobility, as shown in Figure 5.1 (a), with a negligible change in electron density, as shown in Figure 5.1 (b). In other experiments, some samples were exposed with x-rays in a vacuum

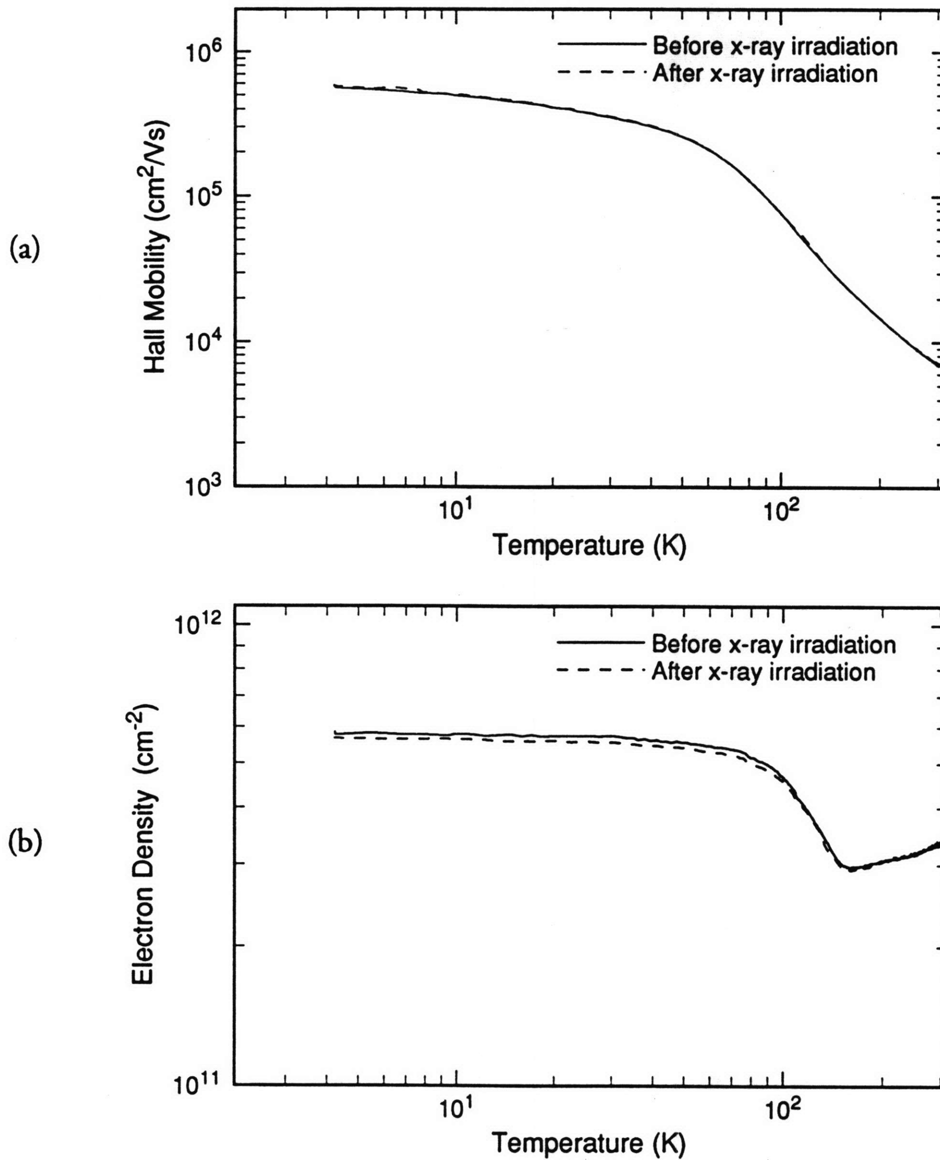


Figure 5.2 (a) Electron mobility and (b) electron density before and after x-ray irradiation as a function of temperature.

chamber, where the samples could be bombarded by stray high-energy electrons. These samples also showed mobilities degradations of a factor of ten, although it was not possible to quantify the electron dose received by the sample.

It is important to emphasize that in order to directly compare the mobility of a given device before and after irradiation, the irradiated devices were already bonded in headers. A

consequence of this is that the devices were not covered with resist as they typically would be during lithography. Therefore, while the conditions of this experiment correspond well with the case of electron-beam evaporation of metals, it is not clear what effect the presence of resist might have on the extent of damage.

Unfortunately, the damage mechanism during electron-beam irradiation has not been isolated. The electron energy of 50 keV is not sufficient to displace lattice atoms, which requires a threshold energy of about 250 keV [75]. Recent research has shown that similar but distinguishable defects can be introduced into bulk GaAs far below this threshold energy using electron beams with energies as low as 3 keV [76,77]. It cannot be excluded that a similar damage mechanism is at work in this case. Another possible damage mechanism may be localized heating due to the very fine beam diameter used during the electron-beam exposures.

However, some recent measurements indicate that the mechanism for damage after irradiation with high-energy electrons may be mediated by processing steps before the electron-beam irradiation. Further study is needed to determine if mobility degradation in indeed attributable to a combination of electron-beam irradiation with other factors.

Calculated energy deposition in the substrate as a function of depth in the substrate is shown in Figure 5.3 for a GaAs substrate with and without a PMMA coating. Clearly, the calculation indicates that the presence of resist does not noticeably affect the energy deposition in the GaAs substrate.

These results indicate that in order to minimize damage to substrates during processing, it may be necessary to utilize x-ray rather than electron-beam lithography to define fine geometries.

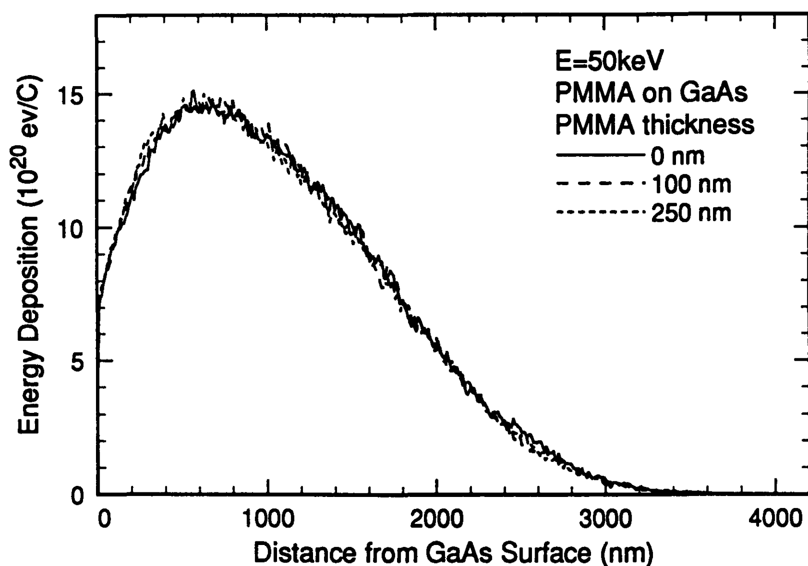


Figure 5.3 Calculated energy deposition in a GaAs substrate as a function of depth, with and without a PMMA coating, for a 50keV electron beam.

In addition, it has been recently reported [22] that electron-beam lithography may not be compatible with the use of back-gated samples of the type describe in Section 4.2.2. Using a similar back-gated layer configuration to that described in Section 4.2.2, the authors found that high energy electrons can induce a leakage path between the surface and the backgate, severely limiting the utility of the backgate. They attributed this leakage to damage caused by the high-energy electrons. To date, no such leakage has been observed in back-gated samples patterned with x-ray lithography, although there has not been a systematic study to evaluate the affect of x rays on these samples.

5.2 Q1D conductor results

After completion, devices are cleaved and bonded into device headers. Devices are then measured at cryogenic temperatures (typically 4.2K) using conventional lock-in techniques. Figure 5.4 shows the measured conductance and transconductance for a typical device. As can

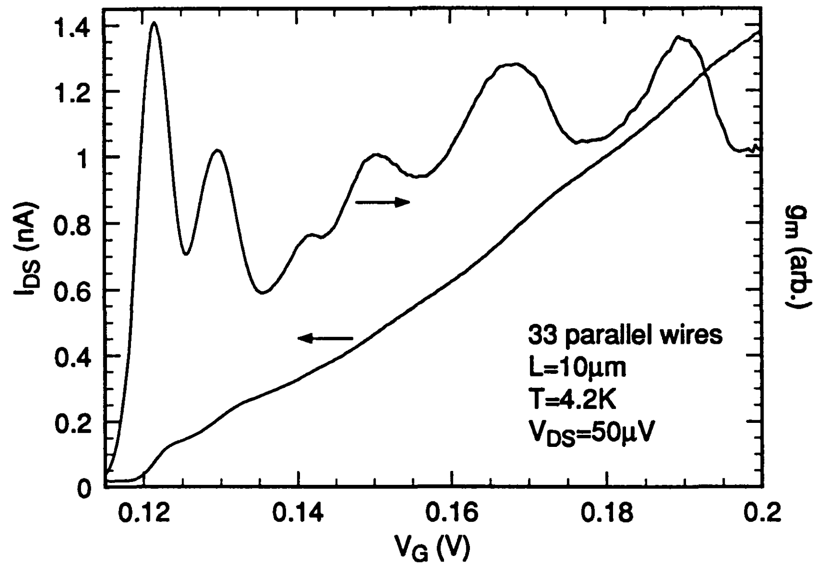


Figure 5.4 Measured conductance for a Q1D device of the type shown in Figure 4.15.

be seen in transconductance, these devices exhibit a clear series of enhancements in conductance as a function of gate voltage. As discussed in Section 2.1.2, these conductance modulations are attributed to the sweeping of the Fermi level through the electronic subbands induced in the wires [78]. A schematic of the potential seen by the electrons is shown in Figure 5.5.

For these particular devices, although the subbands are clearly manifested, the relative weakness of the conductance modulations can be attributed to small energy sub-band separations. This is consistent with the small amount of gate voltage required to sweep the Fermi level between energy bands. By comparing the background conductance for the wire devices with conventional two-dimensional transistors on the same substrate, it can be shown from geometric arguments [11] that the electrical width of the wires is of the order of 100 nm, resulting in an average energy level spacing of ~0.5–1 meV.

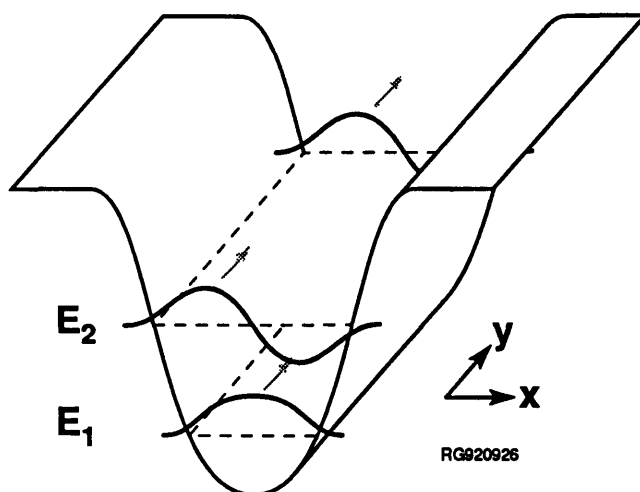


Figure 5.5 Schematic of potential seen by electrons in Figure 5.4 (arrows indicate direction of current flow).

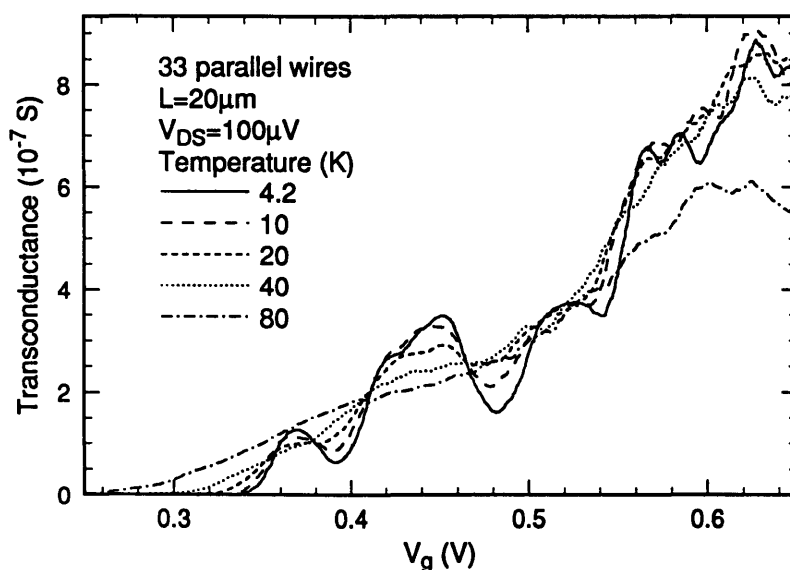


Figure 5.6 Temperature dependance of the transconductance of a Q1D device.

In order to increase the energy level separation (and hence, the minimum temperature where these effects manifest themselves), the etch depth of the confinement etch was slightly increased in a subsequent batch of devices. Figure 5.6 shows the typical temperature dependance of the transconductance of one of these Q1D devices fabricated in a different

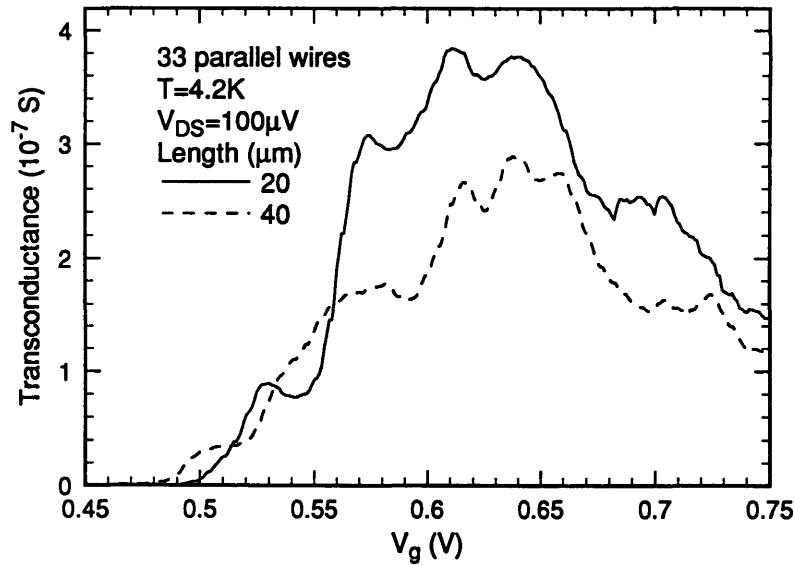


Figure 5.7 Length dependence of the transconductance of a Q1D device.

batch from the device shown in Figure 5.4. Again by geometrical arguments, it can be shown that the electrical widths of wires in this device are on the order of 85 nm, corresponding to an average energy level spacing of ~1–1.5 meV. This is consistent with the thermal smearing of the features in the transconductance with temperature.

By the time these particular devices were fabricated, the GaAs etching technology described in Section 4.3.3 had become sufficiently robust that etching was very consistent for all devices on the die (approximately 60 devices). In fact, all twelve devices with lithographic wire widths the same as the device shown in Figure 5.6 exhibited very similar conductance modulations, verifying the robustness of the fabrication process.

An example of this similar behavior is shown in Figure 5.7, where the transconductance for two Q1D devices of different lengths is plotted. Although the peak positions do not exactly correspond, there is a reasonable correlation in the gate voltage where modulation appear.

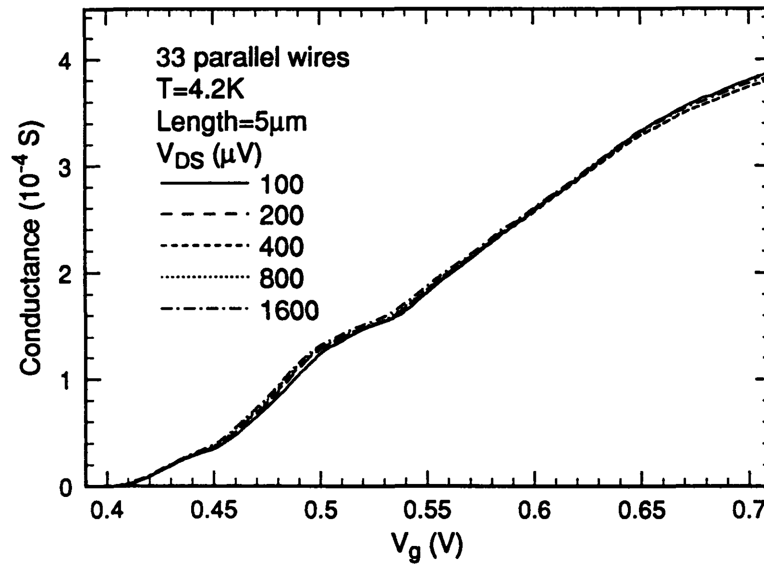


Figure 5.8 Conductance of a Q1D device for various drain-source biases.

In addition, the observed conductance modulation have proven to be quite insensitive to voltage broadening, as shown in Figure 5.8. In fact, current levels for the device in Figure 5.8 became sufficiently high at V_{DS}=2000µV that it became necessary to make DC measurements of the device using a Hewlett-Packard 4145 semiconductor parameter analyzer, rather than AC measurements with a lock-in amplifier. Although it is difficult to directly compare the DC to the AC measurements because of the significantly noisier signal in the DC measurements, features in the conductance for this particular device could still be clearly distinguished at drain-source voltages as high as 50 mV, and in the derivative of the conductance as voltages as high as 200 mV.

The insensitivity of the device in Figure 5.8 to applied voltage in indicative of a short inelastic scattering length in the Q1D conductors. To understand this, consider that a long, diffusive Q1D conductor can be thought of as a multiple ballistic Q1D conductors in series. If the

voltage drop across these ballistic segments becomes larger than the energy separation of the subbands (ΔE), features in the conductance of the device become less observable, as discussed in Section 2.1.1. Assuming ΔE~2 meV, a wire length of 5 μm, and a maximum drain-source voltage before features begin smearing of ~50 meV, the inelastic scattering length, or the average length of the ballistic segments in the conductors, can be calculated to be ~200 nm.

One possible explanation for this relatively short inelastic scattering length may be channel roughness caused by rough sidewalls after chemical etching. If this is the case, it may be possible to smooth the sidewalls of the etched wires by doing a second, smoothing etch in Br_2:CH_3OH (1:1000) as suggested by Shiraki *et al.* [79]. Smoother side walls may have the added benefit of enhancing the conductance modulations, by minimizing local variations in wire widths.

5.3 Q1D-PRESTFET results

As was shown in Figure 4.17, Q1D-PRESTFET devices have been fabricated. Unfortunately, the particular device geometry used for these device was apparently not optimal for observing the predicted resonances discussed in Section 2.2.

When these devices are measured at liquid helium temperatures, the electrical characteristics of these devices are very similar to those shown in Figure 5.6 for Q1D conductors, except that current levels are significantly suppressed. It is believed that the current suppression is due to low conductance through the tunneling region of the device.

A possible reason for the lack of observable resonances in these devices may be the size of the quantum well in the tunneling region. If the well is too wide (W in Figure 5.9 (b)), then the

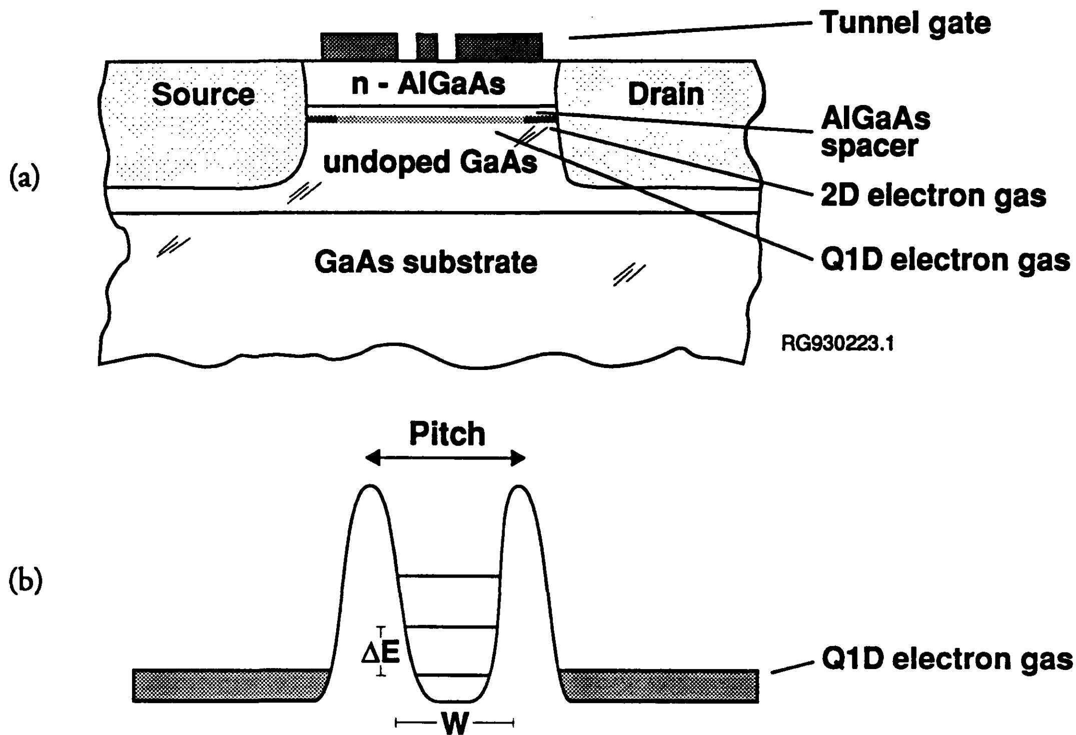


Figure 5.9 (a) Schematic cross-section, and (b) potential seen by electron in Q1D-PRESTFET.

energy level separation in the well (ΔE) may be too small to resolve resonant tunneling through individual levels.

The potential seen by electrons by electrons in a two-dimensional electron gas for various gate geometries is shown in Figure 5.10. Although these are not the potentials seen by electrons in an etched Q1D structure, they are a good approximation, showing the benefits of smaller geometries.

Based on modeling results shown in Figure 5.10, it is estimated that the well width of the particular devices that were fabricated are ~200 nm, giving an energy level separation on the order of 0.2 meV (or equivalently, a temperature of 0.5 K). Currently, there are efforts under

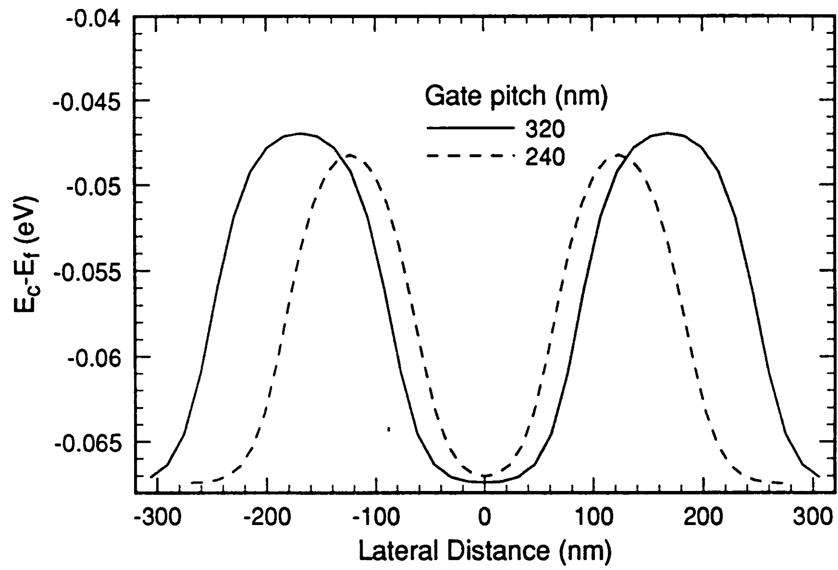


Figure 5.10 Potential seen at the plane of the two-dimensional electron gas for tunnel gates with various pitches.

way to reduce the size of the quantum well by decreasing feature sizes on the tunnel gate shown in Figure 5.9 (b). By decreasing the well size to ~100 nm, resonant effects ought to be observable at liquid helium temperatures.

Chapter 6
Conclusions

Each generation of computing technology has at some point run into fundamental limitations, eventually being supplanted by a newer technology. For the past several decades, computation based on conventional electronics has been enjoyed a phenomenal degree of success, ushering in the information revolution. However, as system densities continue to increase, physical limits are beginning to come into conflict with basic requirements of computing using conventional electronics.

The question that is currently being asked is what form a potential successor technology may take? Will it be comprised of more evolutionary changes, as have been seen over the past couple decades, or will a more revolutionary technology, better suited to the strengths and limitations of ultra-dense systems, rise to a dominant position?

It is these types of questions which have been driving the exploratory research into electronic systems based on quantum phenomena over the past 10 years. Much effort has been made to understand the underlying physics that govern such devices, with the hope of eventually harnessing these devices for computation.

In the short term, research into QEE has placed enormous pressure on engineers to develop and refine technologies necessary to manufacture these exploratory devices. At the same time, QEE research has required materials and lithography that are beyond the current state of the art. As such, QEE has served as a powerful technology driver in these key areas.

For this work, special emphasis has been placed on the development of a highly robust fabrication technology for the manufacture of quasi-one-dimensional conductors. An important component has been the development of x-ray lithography as a technique for patterning these devices. Because x-ray lithography is well suited to the fabrication of sub-100 nm electronics, the development of x-ray lithography for long range QEE research has had the important collateral benefit of developing a lithography technology that is compatible with the manufacture of more traditional devices, such as deep-submicron MOSFETs and optoelectronic devices.

Several advantages of x-ray lithography when fabricating QEE devices have been demonstrated, including a lack of damage to high quality substrates during processing, high process latitude and repeatability. In addition, it has been demonstrated that there is a significant increase in process latitude when patterning x-ray masks using electron beam lithography as opposed to patterning solid substrates, implying that there may be fundamental advantages in patterning devices using electron-beam patterned x-ray masks, rather than patterning devices using electron-beam lithography directly. The high density patterns required for modern integrated circuits place considerable stress on electron-beam lithography, because of the proximity effect.

Modeling tools have been developed and implemented to explain and quantitatively predict this phenomena by modeling both exposure of resist by high-energy electrons, and resist development. Experiments to verify the accuracy of these tools are ongoing.

The utility of x-ray lithography has been demonstrated by successfully fabricating Q1D conductors. The good linewidth control of x-ray lithography coupled with high-precision chemical etching of GaAs capable of sub-nanometer vertical resolution, has made it possible to repeatably and reliably define Q1D conductors in high-quality GaAs/AlGaAs substrates. In addition, chemical etching of GaAs serves to minimize damage to the GaAs surface, permitting the formation of high-quality Schottky contacts to the Q1D conductors.

Using x-ray lithography combined with high-precision chemical etching, Q1D conductors have been successfully fabricated on high-quality modulation-doped substrates. Conductance modulations attributed to the reduced dimensionality of these conductors have been observed at temperatures as high as 30K. The temperature behavior of these devices are consistent with the calculated electrical width of these devices (~85nm).

Perhaps more importantly, it has been demonstrated that Q1D conductors can be reliably fabricated in large numbers, making it possible to fabricate more complicated devices. Preliminary attempts have been made to fabricate a planar resonant-tunneling field-effect transistor with Q1D emitter and collector (Q1D-PRESTFET), that has been predicted to exhibit very strong resonances in electron transport.

Although Q1D-PRESTFETs were successfully fabricated using two aligned levels of x-ray lithography, no resonances in electron transport were observed at liquid helium temperatures.

It is believed that this is due to an inability to resolve tunneling through quantized levels within the device. Efforts are ongoing to reduce critical feature sizes in an effort to increase the energy level separation within the tunneling region of the device, and hence, enhance the detectability of resonant tunneling through these energy levels.

Technologically, there are several areas where things may be improved. First, efforts should be made to further push the resolution limits of patterning x-ray masks using electron-beam lithography. Not only are finer feature sizes important for QEE research, but it is also important to experimentally find the limits of current technology. Such information is needed so that objective evaluations can be made regarding the suitability of these technologies to advanced manufacturing of conventional integrated circuits, particularly with respect to linewidth control and pattern placement.

Second, efforts to explore the limits of electron-beam patterning of x-ray masks should be integrated with an effort to enhance and extend the modeling tools that have been developed in this work. If it can be demonstrated that these modeling tools can be used to quantitatively model patterning of x-ray masks with electron-beam lithography, it would then be possible to conduct an extensive theoretical study of the process window for different pattern geometries.

Third, from a material stand point, additional work should be done to harness the potential benefit of back-gated substrates in QEE research. By using a back-gate to probe the confining potential set by a surface gate, interpretation of device behavior will become more straightforward.

In addition, there is still the open question of how high-energy electrons degrade the low-temperature mobility of high-quality modulation-doped GaAs/AlGaAs substrates.

From a device stand point, there are several areas where this work may be extended. First, by reducing the lithographic width of the Q1D conductors, it ought to be possible to further reduce the electrical width, and hence, increase the maximum temperature where quantum effects are observable.

Second, as discussed earlier, an effort should be made to reduce critical feature sizes in the Q1D-PRESTFET in order to observe resonant tunneling in quasi-one-dimensional systems. Although the harnessing of this type of planar device for practical application will be difficult because of the requirement for low temperature operation, the demonstration of strong resonance in planar devices may serve as the basis for future work in advanced materials technology. If such a material technology were to enable fabrication of analogous devices with critical lengths on the order of several atomic monolayers, room temperature operation of resonant tunneling devices with reduced dimensionality emitter and collector may become a reality.

Third, the etching technology that has been developed for this work is directly applicable to a variety of QEE devices. Although chemical etching has the disadvantage of fixing the confinement potential, modeling has shown that the confinement potential induced by chemical etching can be significantly deeper than that which can be achieved using field-effects. In addition, by setting a confinement potential using chemical etching, it is then possible to independently set another confining potential using field-effects (this is the basis of the Q1D-PRESTFET device described in this work).

Finally, with some innovative design, it may be possible to fabricate devices where it is possible to electrostatically define a Q1D conductor while at the same time being able to electrostatically define tunneling barriers. This type of device would offer the greatest degree of flexibility during characterization, especially if it were possible to probe the electrostatically defined confinement potential using a back-gated substrate.

Appendix A
Processing sequence

This appendix describes the procedures that have been developed for the fabrication of GaAs/AlGaAs devices for research in QEE. These procedures will be described in a fair amount of detail in order to be of greater use to those who may continue this work.

For the work described in this thesis, high quality AlGaAs/GaAs modulation-doped material was supplied by Prof. Michael Melloch at Purdue University. These substrates are grown in a Varian GEN II molecular-beam epitaxy (MBE) system, typically starting with a 1 µm undoped GaAs buffer on a two inch diameter, semi-insulating GaAs substrate, followed by a 20 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer, 30 nm $Al_{0.3}Ga_{0.7}As$ doped n-type to $1.5\times10^{18} cm^{-3}$, and a 5 nm GaAs cap doped n-type to $1.5\times10^{18} cm^{-3}$.

Some older MBE systems require that the sample be held down using indium during the growth process. This typically leaves a great deal of indium on the backside of the GaAs substrates. This indium needs to be removed before further processing. This procedure is described in detail in reference [80].

After receipt (and if necessary, indium removal), wafers are given a tracking number (e.g., MBE19) and cleaved into smaller pieces for further processing. GaAs is significantly more fragile that other semiconductors, like silicon. Care must be taken to avoid shattering the substrate during cleaving. If necessary, it may be wise to practice cleaving blank GaAs substrates before attempting to cleave MBE grown material. After cleaving, pieces are assigned individual tracking numbers (e.g., MBE19a, MBE19b, etc.).

1. *Solvent clean*

   In order to have consistent results, care must be taken to maintain the quality of the GaAs surface during processing. Given the susceptibility of GaAs to most conventional semiconductor cleaning methods, GaAs samples are typically cleaned with a combination of heated solvents. Samples should be cleaned in glassware dedicated exclusively to cleaning GaAs, to reduce the chances of cross contamination that may adversely affect the samples.

   In a well ventilated area with an explosion-proof hotplate, boil the sample for 5 minutes in trichlorethane with hotplate on 120°C. To avoid superheating of the solvent, make sure that some rough surface (e.g. a dipping basket) is available for vapor to condense around. Never walk away from heated solvents. While spraying with acetone to prevent drying, transfer the sample to an acetone filled beaker and heat for 5 minutes with hotplate on 60°C. Transfer to beaker filled with methanol and heat for 5 minutes with hotplate on 140°C. Rinse sample in flowing deionized water (DI water) for 60 seconds and blow dry with the nitrogen air gun. Remember that it is important to keep the surface of the sample wet when transferring between solvents so that any contaminants dissolved in the solvents do not dry on the surface of the sample.

2. *Spin coat with photoresist*

Immediately after cleaning, spin coat the sample with Shipley 1813 photoresist at a spin speed of 3500 rpm for 30 seconds. This gives a film ~1.5µm thick. Bake in a 90°C oven for 25 minutes.

3. *Mesa etch exposure*

The first step in device fabrication is to electrically isolate devices from one another. This is accomplished by etching the region between devices deep enough to deplete the two-dimensional electron gas, leaving behind a mesa structure.

Prepare the OAI optical aligner for exposure of small samples using the 400nm mirrors. Coarsely align mesa mask to edge of cleaved wafer, bring mask into vacuum contact with sample, and expose (exposure time ~3.5 seconds).

4. *Develop resist*

Prepare a mixture of 5:1 DI H_2O:Microposit 351 developer and develop sample for 10 seconds, rinse in DI water for 60 seconds, and blow dry. Check development under microscope (remember to properly filter microscope light with the yellow filter). Repeat until sample is completely developed out. If development time to too long or too short, adjust exposure time accordingly.

A thorough DI water rinse after development is absolutely **crucial**, in order to minimize ionic contamination from the developer solution. In combination with other chemicals, the components of the developer can aggressively etch GaAs.

5. *Mesa etch*

In a beaker dedicated to mesa etching, mix 5:3:80 NH_4OH:H_2O_2:H_2O, adding the H_2O_2 last. Using teflon tweezers, mix the solution (metal seems to catalyze the etch). Using the same tweezers, immerse the GaAs sample in the etchant for 6 seconds for an etch depth of ~200 nm. Immediately rinse in DI water for 2 minutes and blow dry. If step coverage over the mesa edge is a concern, etch for less time to form a shallower mesa.

6. *Solvent clean*

After removing photoresist with acetone, solvent clean the sample.

7. *Spin coat with photoresist*

8. *Ohmic contact exposure*

Before continuing, make arrangements to have the electron-beam evaporator available for ohmic metallization (see step 12).

Align the ohmic contact mask with the sample in the optical aligner and expose.

9. *Develop photoresist*

10. *UV ozone clean*

In order to remove any organic contaminants that may still remain on the surface of the GaAs sample after development, clean the sample in the UV ozone system for one minute. The ozone gently volatilizes any organic materials on the surface of the sample without bombarding the sample with high-energy particles. It also oxidizes the GaAs surface.

This step is critical to ensure that no contaminants become trapped between the exposed GaAs surface and the evaporated metal.

11. *Oxide dip (optional)*

If making good ohmic contacts is causing difficulty, the surface can be further prepared by etching away any surface oxides before depositing the ohmic metallization. This can be done by dipping the sample in 1:10 $NH_4OH:H_2O$ for 3 seconds, using teflon tweezers. Do not rinse the sample afterwards. IMMEDIATELY after blow drying the wafer, mount on evaporation plate and put it into the evaporation chamber.

12. *Ohmic metal deposition*

Securely mount sample on evaporation plate and put it into the evaporation chamber. Sample should pump down overnight. Mark sample for liftoff (i.e. second shutter). Standard GaAs ohmic metal deposition is Ni:Au:Ge:Au:Ni:Au 2:4:22:44:10:30 nm.

13. *Metal liftoff*

Before continuing, make arrangements to use the rapid thermal annealer (RTA) in the building 13 Microlab for step 16.

In order to dissolve the remaining photoresist on the sample to lift off the ohmic metal, gently heat some acetone in a beaker dedicated to metal liftoff on an explosion-proof hotplate. Place the sample in the heated acetone and let it sit for ~60 seconds. If the optical lithography resulted in a good liftoff profile, it should be possible to complete the liftoff by rinsing in acetone. If this does not work, it may be necessary to use ultrasound.

Rinse with acetone, then methanol, making sure that sample does not dry. Rinse with DI water and inspect in optical microscope.

14. *Solvent clean*

    Before annealing the sample to form the ohmic contacts, it is **critical** that the sample be thoroughly cleaned. Contaminants on the surface during the anneal may potentially degrade the surface quality of the sample, making it impossible to form good Schottky contacts for the gates.

15. *UV ozone*

16. *RTA*

    Immediately load sample into clean pyrex dish and load into a vacuum container. Transfer to Microlab immediately and anneal in RTA at 450°C for 10 seconds (435°C for back-gated samples). (Speak with the lab manager of the Microlab to arrange for training on the RTA)

    When finished, load the sample in the vacuum tin and return it to the SSL.

A.1 Q1D conductor fabrication process

17a. *Solvent clean*

Make arrangements to have the e-beam evaporator available for step 24a.. Because the sample has been removed from the lab, it is especially important to thoroughly clean the sample when it is back in lab.

18a. *UV ozone clean*

19a. *Spin coat with photoresist*

20a. *Contact pad exposure*

Align and expose the sample with the contact mask. This mask defines the large bonding pads as well as the gates for the conventional HEMT devices.

21a. *Develop*

22a. *UV ozone clean*

23a. *Oxide dip (optional)*

24a. *Contact metal deposition*

Sample should be marked for liftoff. Standard GaAs Schottky contact metal deposition is Ti:Au 20:130 nm, or Ti:Pt:Au 20:20:110 nm.

25a. *Metal liftoff*

26a. *Cleave sample*

Carefully cleave sample into individual dies and give each a tracking number (e.g., MBE19a1, MBE19a2, etc.) From this point on, only handle samples with teflon tweezers to avoid chipping edges. Any chipping of the edges may make it difficult to properly expose the sample.

27a. *Solvent clean*

28a. *UV ozone clean*

29a. *Expose sample with Q1D wire mask*

Prepare samples and expose with Q1D wire mask as described in Appendix B.

30a. *Develop PMMA*

Develop sample in 40:60 MIBK:IPA for about ~10 seconds, and rinse with IPA for 20 seconds. Monitor development under optical microscope. Repeat until exposed resist has completely developed away.

31a. *UV ozone clean*

32a. *Prepare etchant*

Etching of GaAs can at times seem to be a black art. In order to minimize variability, it is critical that every effort be made to ensure that glassware and other tools used during etching does not become contaminated with other chemicals.

In a dedicated beaker, mix 1:40 H_2SO_4:H_2O and cool to 18 °C while gently stirring with a magnetic stirrer. Make certain that the solution is not exposed to metals, as these seem to catalyze the etching of GaAs.

33a. *Measure height of resist*

Because the initial etch rate of GaAs is unpredictable, it is necessary to monitor the etch depth while etching. Thus, it is necessary to measure the height of resist in a monitor area prior to etching. One way to do this is using the Linnik interferometer. After some signal processing, it is possible to detect depth changes ~1 nm using the Linnik.

Note that the resist thickness measured in the Linnik is different from the actual resist thickness because the resist is transparent. However, since etch depth is measured as the change in resist height during etching, the actual resist height is unimportant.

34a. *Activate etchant*

Once the rest of the etchant is at the proper temperature, add H_2O_2 to the beaker such that the final ratio is 1:1:40 H_2SO_4:H_2O_2:H_2O. The H_2O_2 is added last because it tends to disassociate in solution. Turn off the magnetic stirrer.

35a. *Etch sample*

Using teflon tweezers, immerse the sample in a beaker of DI water to wet the surface, then etch the sample for 10 seconds. Rinse the sample in the beaker of DI water, by letting DI water flow over the edge of the beaker for 60 seconds. Monitor the etch depth with the Linnik interferometer. Repeat as necessary to achieve the desired etch depth of 25–30 nm. Before continuing etching, briefly stir the etchant and prepare a new rinse beaker with DI water. Note that this particular etchant has an etch rate of ~1–3 nm/s.

36a. *Solvent clean*

Make arrangements to have the e-beam evaporator available for step 42a before beginning solvent clean.

37a. *UV ozone clean*

38a. *Spin coat with photoresist*

39a. *Gate metal exposure*

Align and expose the sample with the gate mask. This mask defines the continuous gates that run over the etched wires.

40a. *Develop photoresist*

41a. *UV ozone clean*

42a. *Gate metal deposition*

Sample should be marked for liftoff. Standard GaAs gate metal deposition Ti:Au 20:80 nm, or Ti:Pt:Au 20:20:60 nm.

43a. *Metal Liftoff*

44a. *Inspect finished devices and measure*

A.2 Q1D-PRESTFET fabrication process

17b. *Cleave sample and etch wires*

See steps 26a–35a above.

18b. *Solvent clean*

19b. *UV ozone clean*

20b. *Expose with tunnel-gate mask*

Prepare samples and expose with tunnel-gate mask, as described in Appendix B. This mask places tunneling fingers across the wire that have already been etched.

21b. *Develop PMMA*

Make arrangements for step 24b before developing the sample.

22b. *UV ozone clean*

23b. *Oxide dip (optional)*

24b. *Gate metal deposition*

See step 42a.

25b. *Metal liftoff*

26b. *Inspect finished devices and measure*

Appendix B
X-ray lithography of small samples

This appendix describes in detail the procedures that have been developed for aligned x-ray lithography on small samples. For procedures describing the fabrication of x-ray mask blanks, see Appendix C of reference [81]. For a description of x-ray mask preparation and processing, see Appendix A–D of reference [30].

1. *Sample preparation*

   When preparing small samples for x-ray lithography, it is important to make sure that the surfaces and edges of the sample do not have protrusions or large particles. Remember that the x-ray mask will be pulled into contact with the sample. For GaAs samples, this requires that samples only be handled with teflon tweezers to avoid chipping of sample edges.

2. *Spin coat with x-ray resist*

   Care must be taken when spin-coating small samples so that resist does not coat the back of the sample (this is a problem when samples are smaller that the spin chuck). One way to do this is to use a dropper to deposit a single drop of resist on the sample, then immediately start the spinner to minimize the amount of

resist that flows over the edge of the sample and onto the spin chuck. Regardless, there will probably be some resist that gets on the spin chuck. This has the unfortunate affect of causing the sample to stick to the spin chuck. If this happens, take care not to try to force the sample off of the spin chuck. This can mangle the edges of the sample, making it useless for x-ray lithography. Instead, using a dropper, place a drop or two of acetone at the very edge of the spin chuck. The acetone will seep under the sample, dissolving any resist that may have dried there. If too much acetone is used, it may overflow onto the surface of the sample. After the resist on the backside of the sample has dissolved, it should be easy to remove the sample using teflon tweezers.

Alternatively, a new spin chuck has been recently made specifically for spinning of small samples. By having the chuck area smaller than the sample size, it is possible to spin coat samples with resist without resist depositing on the backside.

For this work, the x-ray resist PMMA (3% 950 MW) is used, spun on at a speed of 4000 rpm for 60 seconds, for a thickness ~200 nm.

3. *Clean backside*

If the samples are to be used in aligned exposures which require electrostatic contact, care must be taken to make sure that there is no residual resist on the backside of the sample that could lead to poor electrical contact. If there is, soak the corner of a clean-room towel with acetone and gently wipe the backside of the sample against the towel.

4. *Bake resist*

Bake samples for 60 minutes at 150°C.

If you do not require alignment, skip to step 14.

5. *Prepare aligner*

   If the x-ray exposure requires alignment to an existing feature, then the aligner stage on Head 3 needs to be prepared. Begin by placing the grounding plate on the silicon pin chuck. This plate serves two purposes. First, it serves as a conducting ground plane that contacts the backside of the sample. Thus, it needs to be grounded. Because many portions of the aligner are not grounded, be sure to check for continuity between the ground plate and true ground using a multimeter.

   Second, the small hole in the center of the ground plate serves as an adaptor for the vacuum pinchuck so that small samples can be held with vacuum during alignment. Note that it may be necessary to place a thin rubber seal below the edge of the ground plate to ensure a good vacuum seal.

   Next, ensure that the top portion of the aligner that holds the x-ray mask is electrically isolated from the rest of the stage. Connect the variable voltage source to the top portion of the aligner. The voltage source will be used to apply a potential between the mask and the substrate.

6. *Inspect mask*

   Using the fiber light, inspect the polyimide coated x-ray mask for particles. If present, attempt to remove them using a nitrogen gun. If they remain, it is not advisable to attempt to scratch them off the surface. Unfortunately, there is currently no reliable way to remove stubborn particles from the surface of x-ray masks.

7. *Mount sample*

Using teflon tweezers, place the sample on the grounding plate and turn on the substrate vacuum. It may be necessary to gently press down the grounding plate to form a good seal with the vacuum pin chuck. Check to see that the sample is secure and set the micrometers to the middle of their range.

8. *Inspect samples*

Carefully inspect the edges of the samples for large particles using the optical microscope on the aligner stage. If there are particles, attempt to blow them off the sample using the nitrogen guns. If the particles are embedded in the resist, then it may be necessary to gently scratch off the particle using a rounded metal tip. This ought to be done under the microscope so that devices are not damaged. Remember that you may be creating particles while you do this, so proceed with caution. Any particle protruding more than 5μm may cause problems with the alignment and exposure.

9. *Load mask*

Load the mask into the aligner and replace leveling screws. The polyimide at the edge of the Pyrex ought to have been removed so that the plating base is in good electrical contact with the top portion of the aligner.

10. *Planarize mask*

In order to properly align the mask to the substrate, it is necessary to first make sure that the mask surface and the sample surface are coplanar. To do this, start the `align` program on the PC which controls Head 3. This program allows you to adjust the height of the Z-stage. Slowly raise the substrate until it comes into contact with the mask. Be careful not to raise the stage too aggressively so as to not puncture the mask.

Based on where the substrate touches, lower the stage and adjust the attitude of the mask accordingly. Raise the sample again until it comes into contact at a corner. Repeat until various points around the edge of the sample all come into contact at the same time. If this is not possible because of a particularly large particle on the substrate, lower the Z-stage, remove the mask, and inspect the sample under the optical microscope to find and remove the particle.

11. *Align mask to substrate*

Once the sample and mask are coplanar, lower the sample 10µm below the point of last contact with the mask. Using the microscope fixture (10× lens) on the aligner in conjunction with the CRT display, align the mask to the substrate, switching to higher magnification objectives as necessary. (Recently it has been determined that the long working distance 20× lens (H20×) has sufficient resolution for alignment, as well as a sufficiently long working distance so that there is no risk of mask damage.)

12. *Contact sample*

Once mask and substrate are aligned, raise the Z-stage until the sample gently contacts the mask, then lower to the point where the mask is just not touching the sample. Begin raising the voltage on the mask, until some portion of the mask comes into electrostatic contact with the substrate (it may be necessary to raise or lower the sample to initiate the electrostatic contact). Continue to raise the voltage to increase the diameter of this area to at least 4 mm^2. (Note that the voltage required for contract varies depending on the conductivity of the substrate. Conducting substrates require far less voltage than semi-insulating substrates.)

If feature sizes are particularly small, it may be necessary to apply an even larger voltage in order to achieve intimate electrostatic contact across the entire sample. This guarantees a zero-gap exposure, which may be crucial for masks with extremely fine geometries. However, this does place the mask at greater risk, so first determine if intimate electrical contact is necessary for the patterns on a particular mask by exposing several monitor samples and inspecting the results in the scanning electron microscope.

After contact has been established, lower voltage to below 30V and disconnect the electrical contact to the mask. The sample will remain stuck to the mask, presumably due to van der Waals forces.

13. *Remove mask from fixture*

Now that the sample is in contact with the mask, it is possible to remove the mask from the fixture and have the sample remain in contact with the mask. First turn off the substrate vacuum. This will cause the sample to rise up into the mask. Vent the vacuum line to remove any residual vacuum, and slowly lower the stage until the sample remains suspended from the mask. Remove the mask from the stage.

14. *Load into mask fixture*

Set up the vacuum regulator for the conformable mask fixture, and gently load the mask/sample combination into the fixture. Make sure that the o-ring seal on the underside of the mask is centered in the fixture. Secure the mask in the fixture using the set screws.

15. *Apply gentle vacuum*

With vacuum regulator set all the way down, slowly open the vacuum valve to the fixture. This will evacuate the area around the sample, causing the mask to deflect over the sample. Enough vacuum should be applied such that the edges of the sample are well defined, but not so much that the mask comes into contact with the polypropylene backing.

16. *Load fixture in x-ray chamber*

Place fixture on lab jack inside the exposure chamber and carefully raise the stage until the fixture is within 4 cm of the vacuum window. Center the sample with respect to the vacuum window. Seal chamber and flush with helium until the oxygen content of the chamber is below 400 ppm.

17. *Expose*

Typical exposure times for PMMA with the Cu_L x-ray source running at 8 keV and 75 mA at this source/substrate distance is 12 hours using the first generation vacuum window.

Note: monitor exposures ought to be done for all new x-ray masks to determine the optimal exposure time.

18. *Remove sample from mask*

After removing the mask/sample combination from the fixture, carefully pick the sample off the mask using a "vacuum wand". If the sample is large and is in intimate contact with the mask, it may be necessary to spray IPA around the edge of the mask and gently lift up the edges with the vacuum wand to allow IPA to flow between the mask and the substrate. If this is the case, consult with someone who has done this before attempting to remove the sample.

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