38

Techniques for Low Distortion Buffering of High Speed Switched Capacitor ADC's

by

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Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of
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Abstract

Harmonic distortion arises in switched capacitor circuits due to the interaction between the resistance of the CMOS switch, the load capacitor, and the parasitic capacitors of the switch. As the voltages across the capacitors vary, current is drawn through the resistance of the switch. Since the resistance of the switch is nonlinear as the input varies, a nonlinear voltage appears at the output of the switch. In addition, as the values of the parasitic capacitors vary nonlinearly with voltage, the current drawn through the switch resistance is nonlinear. A nonlinear voltage is present at the input of the switch due to the nonlinear current drawn through a source impedance. To minimize the magnitude of the distortion terms, the resistance and parasitic capacitors of the switch are linearized and reduced, and the source resistance is isolated from the capacitors. The switch resistance is linearized by the use of a 'bootstrap' technique, wherein the gate is driven to track the input, yielding a constant V_{GS}, despite input variations. By appropriately sizing the device, a compromise is reached between the size of the switch resistance and the size of the parasitic capacitors associated with the switch. The source resistance is isolated from the switch by a buffer which is implemented with a source follower. A bootstrap technique is used on the source follower to linearize its response. A bootstrapped source follower buffer isolating an optimized bootstrapped PMOS switch from the source impedance yields -72dB total harmonic distortion (THD) performance for a 20MHz input signal. This is a -24dB improvement over a simple non-optimized NMOS switch. For applications under 20MHz, bootstrapping the source follower buffer with a two-stage amplifier buffer is recommended. However, for applications in the 20-40MHz range, a cascoded PMOS source follower buffer is advised.

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Table of Contents

1 Introduction 13
1.1 A Sampling Switched Capacitor Circuit 13
1.2 Sources of Nonlinearity in the Switched Capacitor Circuit 14
1.3 Performance Objectives of the Nonlinearity Reduction Circuit 16
1.4 Thesis Organization 17
2 Design Issues 19
2.1 Switch Options 19
2.2 Bootstrapped Switch 21
2.3 Switch Limitations 24
2.4 Charge Injection From the Switch 25
2.5 Input Buffer Criteria 27
2.6 Input Buffer Options 28
2.6.1Source Follower Buffer 28
2.6.1.1Techniques for Improving Distortion in the Source Follower Buffer 29
2.6.1.2Gate to Drain Buffering 30
2.6.1.3Source to Drain Buffer 37
2.6.2Operational Amplifier Buffers 38
2.6.3Inverting Amplifier Buffer 43
3 Limitations and Implementation Issues 47
3.1 Bootstrap Circuit Limitations 47
3.2 Switch Buffer Limitations 51
3.3 Impedance Enhanced Current Source 51
3.4 ESD Protection Circuitry and Pad Model 53
3.5 Capacitor Compensation Technique 54
4 Implementation 59
4.1 Constant Voltage Source for the Switch 59
4.2 Switch Back Gate Buffer 59
4.3 Dummy Switch 60
4.4 Source Follower Buffer 61
4.4.1Source Follower Back Gate Buffer 61
4.4.2Source Follower Drain Buffer 61
4.5 Impedance Enhanced Current Source Amplifiers 64
5 Results 67
5.1 Simulations 67
5.2 Calculation of THD 69
5.3 THD Results 70
6 Conclusion 73
Appendix A Explanation of Total Harmonic Distortion 75
Appendix B Code for Simulation of Total Harmonic Distortion 77
Bibliography 79

List of Figures

Figure 1.1: Switched capacitor circuit. 13
Figure 1.2: Sample and hold amplifier. 14
Figure 1.3: Simplified network of the switched capacitor circuit. 15
Figure 1.4: Nonlinearity of Ron. 16
Figure 2.1: Improved switch block. 24
Figure 2.2: Charge split in a PMOS switch. 25
Figure 2.3: NMOS source follower and small-signal model. 29
Figure 2.4: Buffered source follower. 31
Figure 2.5: Cascoded source follower. 33
Figure 2.6: Cascoded source follower with level shift. 35
Figure 2.7: Simple single-stage amplifier configured as a buffer. 39
Figure 2.8: Two-stage amplifier configured as a buffer. 40
Figure 2.9: Folded cascode amplifier configured as a buffer. 41
Figure 2.10: Linearizing the input pair of an amplifier. 42
Figure 2.11: Inverting amplifier as a buffer. 44
Figure 2.12: Buffer amplifier feedback system. 45
Figure 3.1: Circuits for bootstrapping the gate of a switch to the source. 47
Figure 3.2: Switched capacitor bootstrap circuit. 49
Figure 3.3: Simple NMOS current source. 52
Figure 3.4: Impedance enhanced NMOS current source. 53
Figure 3.5: Pad model and ESD protection circuit. 53
Figure 3.6: CDB for various size NMOS 56
Figure 3.7: CDB for various size PMOS. 57
Figure 3.8: Methods of compensating nonlinear capacitors. 57
Figure 3.9: Compensated total parasitic capacitance. 58
Figure 4.1: Switch back gate buffer. 60
Figure 4.2: Switch, dummy switch, and load 61
Figure 4.3: Cascoded source follower drain buffer for input buffer. 62
Figure 4.4: Folded cascode drain buffer. 63
Figure 4.5: Two-stage drain buffer. 63
Figure 4.6: Impedance enhancement amplifier for PMOS current sources. 64
Figure 4.7: Impedance enhancement amplifier for NMOS current sources. 65
Figure 5.1: Simulated waveforms and an FFT of the improved switch 68
Figure 5.2: Simulated waveforms and an FFT of the input buffer. 69
Figure 5.3: Transient response of the buffer and improved switch. 69
Figure 6.1: Top-level input buffer and improved switch. 73

List of Tables

Table 2.1: Average switch resistance and capacitance for L=0.6mm 20
Table 2.2: Charge split in PMOS switch 26
Table 5.1: Simulated THD Performance (Nominal) 70
Table 5.2: Simulated THD Performance (125 deg C/ slow models) 70
Table 5.3: Simulated THD Performance (-45 deg C/ fast models) 71
Table 5.4: Simulated THD Performance @ 38.125MHz 71

Chapter 1

Introduction

1.1 A Sampling Switched Capacitor Circuit

The nonlinear combinations of the circuit elements seen in Figure 1.1 result in harmonic distortion of the voltage across C_{IN}. In the case where the source resistance of the input is not negligible (50Ω to 1KΩ) and the input signal is fast (10 MHz and above), the total harmonic distortion (THD) may rise above acceptable levels.

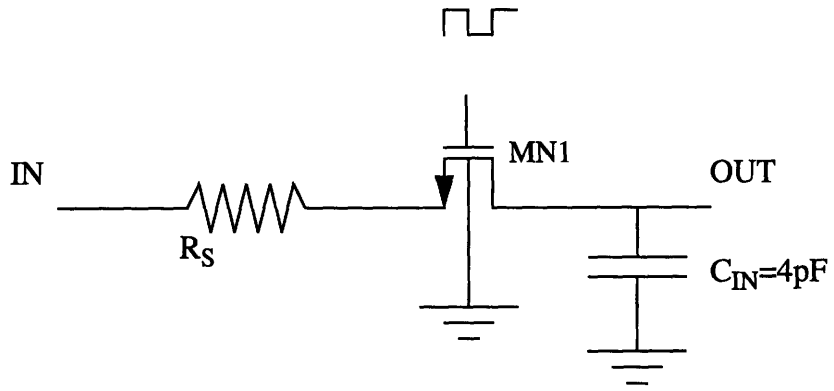

Figure 1.1: Switched capacitor circuit.

One example of this circuit occurs in an A/D Converter. In video applications, the input signal moves too fast for the converter to process in continuous time. For this reason, sample and hold amplifiers (SHA) precede ADC's or are incorporated into the converter on-chip [1]. When the clock turns on a sampling switch, a SHA tracks the input voltage. It holds the voltage last placed on the sampling capacitor when the clock turns the sampling switch off. A differential input SHA similar to the one proposed by Yen and Gray [2] can be seen in Figure 1.2. Switches Q_{S1} and Q_{S2} are closed during track mode, QS3 is switched to common mode level, and QS4 is open. The input capacitance of the SHA plus parasitics of the sampling switch are modeled by C_{IN} of Figure 1.1 (the summing nodes of the amplifier act as low impedance virtual grounds). Switch Q_{S1} is mod-

eled by MN1 in Figure 1.1, and the series resistance is representative of the impedance of an off-chip anti-aliasing passive filter network.

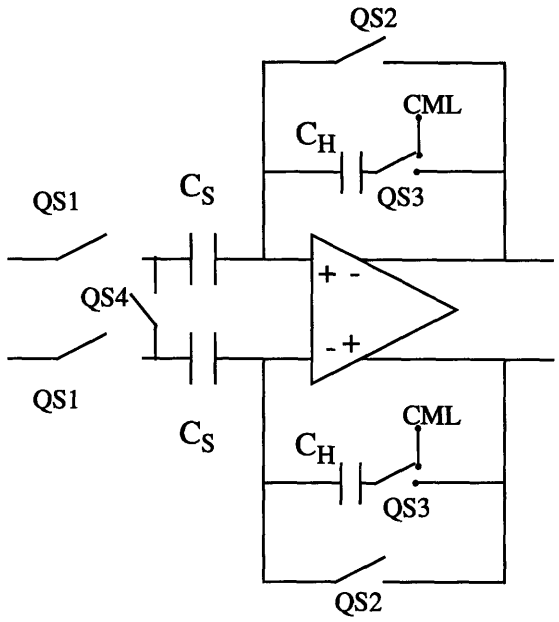

Figure 1.2: Sample and hold amplifier.

1.2 Sources of Nonlinearity in the Switched Capacitor Circuit

Distortion in the circuit of Figure 1.1 can be traced to the modulation of the impedance of MN1 and the interaction of the nonlinear parasitic capacitors of MN1 with linear and non-linear resistive elements. Figure 1.3 is obtained by assuming that the gate of MN1 is driven by a clock, thus it behaves as an AC ground. The linear source resistance (R_s) and the parasitic capacitor from the source to the well of MN1 create an attenuation which is frequency dependent and input signal dependent. The attenuation is nonlinearly dependent on the input signal, since C_{BS} varies nonlinearly with V_{BS}. A similar problem occurs with the 'on resistance' (R_{on}) of MN1 and the drain to well parasitic capacitor.

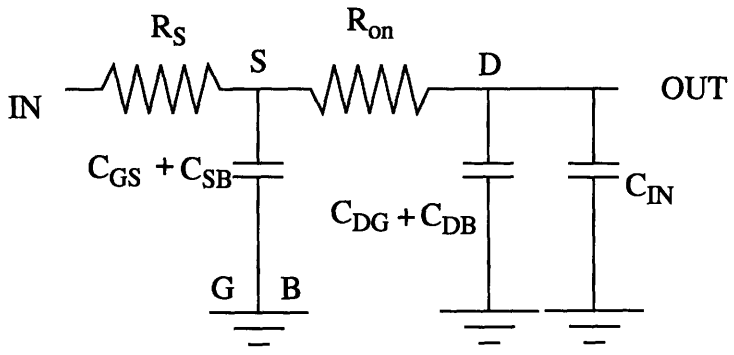

Figure 1.3: Simplified network of the switched capacitor circuit.

The value of R_{on} varies with V_{GS}. For input signals which are smaller than AVDD-V_T, the voltage from the gate to the source is larger than V_T when the clock is high. AVDD refers to the positive analog supply of the circuit (+5V). AVSS refers to the analog ground of the circuit. Since the drain can assume a value close to the input voltage (V_{DS} is less than V_{GS}-V_T), MN1 is in triode region. When MN1 is turned on by applying AVDD to the gate, the input signal (present on the source) is passed through R_{on}. However, as the drain and source vary with the input, the gate potential remains at AVDD. Thus, the gate to source voltage modulates with the input. Since R_{on} of MN1 is dependent on this voltage, the resistance is not constant.

$$R_{on} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)} \tag{1.1}$$

The threshold voltage (V_T) is also dependent on the voltage applied from the well to the source of the transistor:

$$V_T = V_{T0} + \gamma[\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}] \tag{1.2}$$

In a NMOS device, the well is the p-substrate, which is usually connected to ground. V_{BS} varies with the input signal, causing nonlinearity in R_{on}. If the voltage at the source of MN1 is nonlinear due to the nonlinear current drawn through R_S and C_{BS}, R_{on} also

exhibits nonlinearity due to the dependence on V_{GS}. The nonlinear characteristic of R_{on} can be seen in Figure 1.4 for various MN1 aspect ratios, with 1KΩ input resistance and a 4pF C_{IN}:

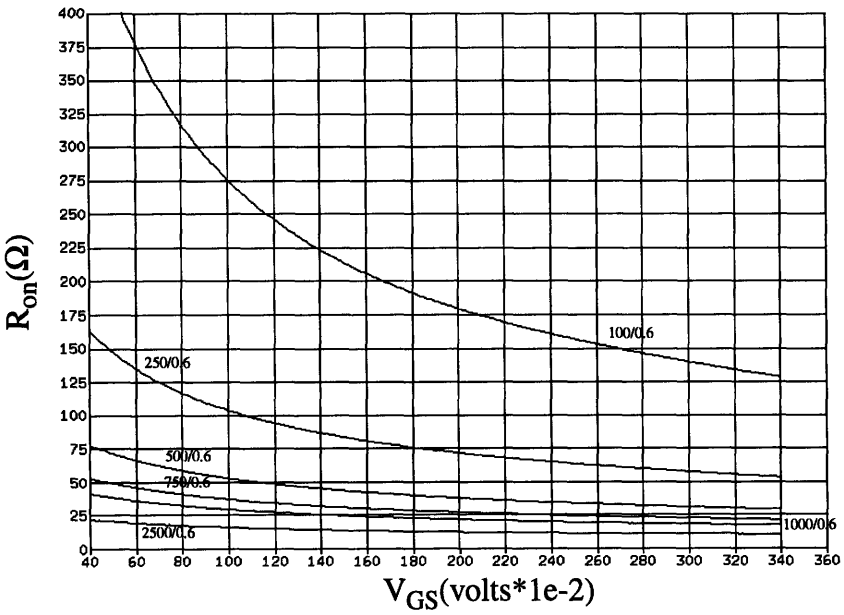

Figure 1.4: Nonlinearity of R_{on}.

The network formed by the nonlinear R_{on} and the parasitic capacitors of MN1 in triode region yields the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{(R_S C_1 s + 1)(R_{on} C_2 s + 1)} \tag{1.3}$$

The parallel combination of C_{GS} and C_{SB} is represented by C_1, and C_2 represents the parallel combination of C_{GD}, C_{DB}, and C_{IN}. Thus, it can be seen that the relationship between the input and output is nonlinear (for AC signals) due to the nonlinearity of R_{on} and the MN1 parasitic capacitors. A circuit must be designed to reduce the nonlinearity of the switched capacitor circuit of Figure 1.1.

1.3 Performance Objectives of the Nonlinearity Reduction Circuit

Accuracy: 12 bits

Sampling Rate:	20 MSamples/s
Power Supply:	+5V
Input Swing:	1Vp-p single ended or differential
Technology:	TSMC 0.6μ CMOS
Load:	4pF
THD:	-72dB up to 20MHz input signal
	-64dB from 20-40MHz input signal

1.4 Thesis Organization

Chapter 2 provides an explanation of the design issues and the concerns of attaining the performance goals.

Limits to the performance of the circuit and problems implementing parts of the circuit are discussed in Chapter 3.

Chapter 4 presents three circuits similar in theory, but different in performance. The merits of each circuit are discussed.

The simulated performance of the proposed circuits is summarized in Chapter 5.

Chapter 6 concludes with recommended solutions for the issues of the first chapter.

Chapter 2

Design Issues

2.1 Switch Options

A NMOS device with a gate drive alternating between ground and AVDD is perhaps the simplest implementation of a switch. However, this switch presents several obstacles for achieving the distortion performance stated in the Performance Objectives. It is possible to reduce the magnitude of the distortion somewhat through careful circuit design techniques as discussed below.

To reduce the distortion associated with R_{on} the resistance can be decreased, made more linear, or a combination of both. Increasing the ratio of the width of the device to the length of the device lowers R_{on}. This reduces the magnitude of the distortion terms associated with R_{on}. However, by increasing the device size, the parasitic capacitors have also increased proportionally, since in triode region:

$$C_{GS} \cong C_{GD} \cong \frac{1}{2} WLC_{ox} \tag{2.1}$$

$$C_{SB} = \frac{C_{sb0}}{\sqrt{\left(1 + \frac{V_{SB}}{\Psi_0}\right)}} \cong C_{DB} = \frac{C_{db0}}{\sqrt{\left(1 + \frac{V_{DB}}{\Psi_0}\right)}} \tag{2.2}$$

where C_{sb0} and C_{db0} are proportional to the device source and drain region areas, respectively. The large parasitic capacitors react with a large input resistor producing an unacceptable amount of distortion. Thus, this design practice is not an effective way of reducing the THD for the case of a 1KΩ input resistor, unless the resistor can be buffered from the capacitors of the switch. Table 2.1 illustrates typical switch resistance and parasitic capacitance for a 9.375MHz 1V peak-to-peak sine wave centered at 1.5V, for 125 degrees C and slow models, with a 4pF load and a 5V gate drive.

Table 2.1: Average switch resistance and capacitance for L=0.6μm

W (μm)	R_{on} (Ω)	C_{bd} (fF)	C_{bs} (fF)	C_{gd} (fF)	C_{gs} (fF)
20	288	20.5	30	15.8	17.1
50	111	57	47	40	42
100	54	102	95	79	86
250	20.5	257	210	197	215
500	9.5	495	410	392	425
750	6.1	750	595	590	635
1000	4.5	975	790	790	850
2500	1.6	2320	1880	1950	2140
5000	0.8	4450	3600	3950	4250

There is another way to decrease R_{on}. The resistance of the switch varies inversely with the difference between V_{GS} and V_T, from Equation 1.1. Increasing this value reduces R_{on}. There are two ways to increase the value of V_{GS}-V_T. The threshold voltage can be decreased or the gate to source voltage can be increased. Since the well of a NMOS device is connected to ground, V_T is a process-determined variable, as can be seen in Equation 1.2. Different processes can be used to achieve lower V_T, decreasing the value of R_{on}. Applying a voltage higher than AVDD to the gate increases the gate to source voltage. Boosting the gate reduces the value of R_{on} while keeping the parasitic capacitor values constant, but these parasitics still exist. They present the same problem stated above when they interact with the large series resistance, unless isolated from R_s by a buffer. Increasing the gate drive to 7V decreases R_{on} to about 80% of the values shown in Table 2.1 for a 5V gate drive. This is some improvement, but gate overdrive requires a switched capacitor circuit to store a voltage on a holding capacitor and then switch the plates of the capacitor onto the switch's gate and source terminals. The extra switches add more nonlinear capacitors and nonlinear resistors in the signal path of the circuit. In addition, reliability is a concern if voltages across the devices become too large. Nonetheless, this is a valid option for improving the THD performance of the switch.

Eliminating the effects of the parasitic capacitors would be ideal, since this would reduce the THD of the circuit. In the instance of the NMOS switch, the circuit would then

consist of the input resistance in series with the on resistance of the device, forming a low pass filter with the load capacitance. The only nonlinear element in the circuit would be R_{on}. However, it is not possible to eliminate the effect of all parasitics using a NMOS device. The well is connected to ground, so the voltages across C_{BS} and C_{DB} vary with input. The values of the capacitors change nonlinearly with the input, thus the current they draw is nonlinear.

The logical choice is to employ a PMOS switch. Then it is possible to eliminate some of the nonlinearity of the parasitic capacitors, since the well is not connected to ground. However, by using a PMOS device, the resistance of the switch increases since $\mu_p<\mu_n$. The input range of the switch is now also changed. The input can go high, as long as the source potential is above V_G-V_{Tp} (the difficulty lies in making the 'above the rail' boosted gate drive to turn the switch off), but care must be taken to ensure very large voltages do not appear across the junctions of the device causing the transistor to break down. On the other hand, the input can now only go as low as AVSS-V_{Tp} (a later section will explain why the minimum V_G is AVSS).

2.2 Bootstrapped Switch

Switching the well to connect to the source when the switch is conducting eliminates the nonlinear effect of C_{BS}. However, by tying the well to the source, the source must now drive the nonlinear well to substrate capacitor.

For inputs greater than $|V_{Tp}|$, the device is in triode region when the gate is grounded. The drain tracks the source closely, with a small modulating voltage differential because of the finite R_{on}. When the well is connected to the source, this reduces the nonlinear effect of C_{DB} to an extent, since both the drain and the well follow the source fairly closely. V_{DS} is only modulating slightly with the input signal, so the current drawn from the drain is fairly constant. An added benefit of tying the well to the source can be seen by examining Equation 1.2. Since V_{BS} is approximately zero, V_T has now been reduced to V_{T0}. Thus, the difference between V_{GS} and V_T has been increased. This reduces the

value of R_{on} in Equation 1.1. More importantly, the nonlinearity of R_{on} due to V_T has been removed, since V_{BS} is now constant.

However, the nonlinearity of R_{on} due to the modulation of V_{GS} still exists. As can be seen from Figure 1.3, C_{GS} and C_{DG} still draw current through this nonlinear resistance. The parasitic $C_{well\text{-}substrate}$ draws nonlinear current from the input, since the well is connected to the source. To tackle the problem of nonlinear switch resistance, it seems necessary to keep V_{GS} constant. By 'bootstrapping' the gate to the source with a constant voltage when the switch is conducting, this constant V_{GS} is achieved. From Equation 1.1, it can be seen that R_{on} is dependent on V_{GS}-V_T. When the switch is conducting, the voltage from the well to the source is also constant if the well has been connected to the source as discussed in the previous paragraphs. Thus, the V_{GS}-V_T term has become linear and independent of the input voltage. By controlling this voltage, the value of R_{on} can not only be made constant, it can also be made smaller with increasing values of the constant voltage. For a PMOS device to conduct, the gate voltage must be below the source voltage, so V_{GS}-V_T in Equation 1.1 becomes V_{SG}+V_{Tp} for a PMOS switch, since V_{Tp} is negative. Thus, a constant voltage placed between the source and the gate of a PMOS switch must have a positive value greater than the absolute value of the threshold voltage if the switch is to remain in the triode region. Increasing the constant voltage value makes V_{SG}+V_{Tp} larger, reducing the value of R_{on}.

In addition, by bootstrapping the gate voltage to the source voltage, the nonlinear effects due to C_{GS} and C_{DG} can be nulled. The gate voltage remains V_b volts below the source, keeping the transistor in triode region while providing a constant V_{GS}. Since the voltage across C_{GS} is constant, no current flows through this capacitor. Also, since the assumption is made that V_{DS} is small, the gate voltage is also tracking the drain voltage (a first order approximation). Thus, the current through C_{GD} is very small. The well is at the same potential as the source, which is a constant V_b above the gate potential. Thus, V_{BG} is constant, so the current through C_{GB} is also approximately zero. Virtually all of the

nonlinear effects of the parasitic capacitors have been significantly reduced, except that of the well to substrate capacitor.

To fabricate a PMOS device, an n-well is placed in the p-substrate. It is then doped with p+ to create the drain and source. In doing this, parasitic capacitance is created between the well (n-well) and the p-substrate. Even if the well is connected to the source, the substrate is connected to ground, so $C_{well\text{-}sub}$ exists as a major source of nonlinearity. To eliminate the effect of the nonlinear current pulled through this capacitor, it is necessary to drive the well with a buffer from the source (Figure 2.1). The capacitor is no longer drawing current from the source (resulting in poor THD), but rather from the buffer. If the buffer is perfectly linear, the well tracks the source ideally, so the current through C_{BS} is essentially zero. S1 and S2 connect the well to the output of the back gate buffer and AVDD, alternately. The well cannot be constantly connected to the output of the buffer, since MP1 is turned off. When the switch is cutoff, the well would follow the input, which may be less than the voltage held on C_{IN}. If this occurs, the junction diode between the drain of MP1 and the well becomes forward biased, bleeding charge from C_{IN}. To prevent this from occurring, the well is connected to AVDD when the switch is not conducting.

Bootstrapping the gate and back gate (well) to the source greatly reduces the nonlinear effects of the parasitic capacitors. As a result, a larger PMOS switch can be used to obtain the same R_{on} as a NMOS switch, without the penalty usually associated with increasing the switch size: increased nonlinear current drawn through larger nonlinear parasitic capacitors. The R_{on} size/linearity trade-off between using a bootstrapped and boosted gate NMOS (a small fairly nonlinear R_{on}) versus a bootstrapped and boosted gate PMOS (a medium-sized linear R_{on}) can be overcome by increasing the aspect ratio of the PMOS switch, yielding a small linear R_{on}. Thus, for applications requiring very good THD performance, a bootstrapped and boosted gate PMOS switch is the optimal choice.

2.3 Switch Limitations

In the previous section, a proposition for a linearized switch is described. Through a series of improvements, sources of nonlinearity are eliminated or reduced, resulting in an improved switch consisting of a PMOS device with the well driven by a buffer from the source and a constant voltage bootstrapping the gate to the source.

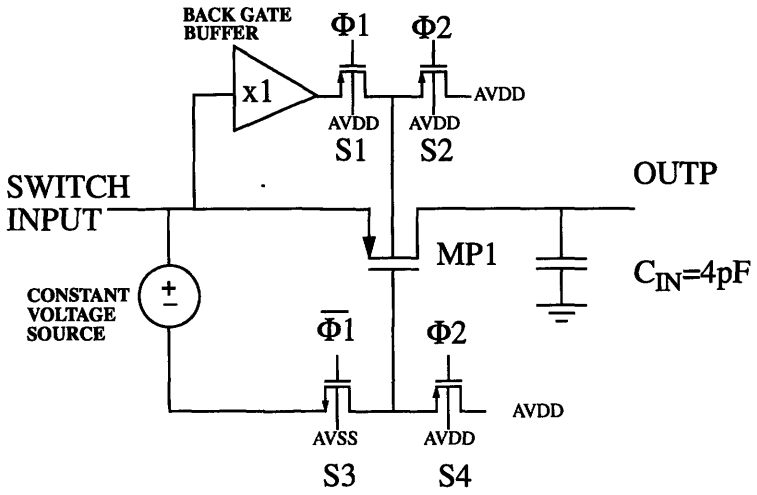

Figure 2.1: Improved switch block.

However, this is not necessarily the most suitable switch. The constant voltage source or buffer may possess distortion problems which outweigh the benefits gained through using them. When a simple switch can be used which meets the performance specifications, there is no need to complicate matters by adding unnecessary surrounding circuitry. In some cases a NMOS switch is adequate, while a bootstrapped and boosted gate PMOS switch is overkill. Since the main input switch is being turned 'on' (Φ1 low) and 'off' (Φ2 low) by alternating the gate drive between a bootstrapped version of the input signal and AVDD, other switches must be employed to perform this task (S1-S4 in Figure 2.1). These switches do not have to be as linear as MP1, so simple non-bootstrapped NMOS and PMOS devices are used.

Although the methods described in the previous section do much to improve the distortion performance of the switch, implementing an ideal constant voltage source and buffer is impossible. Thus, R_{on} is not completely linear and some current flows through

the parasitic capacitors. To reduce the distortion to acceptable levels requires a buffer which separates the input resistance from the current drawn by the capacitors of the switch. Additionally, the buffer is required to isolate the input signal from the effects of charge kickback from the switch.

2.4 Charge Injection From the Switch

As the gate drive alternates between AVDD and V_b below the input of the switch, charge is pushed and pulled onto the parasitic capacitors of the switch. For example, consider the switch transition from the nonconducting mode to conducting mode as shown in Figures 2.2a and 2.2b.

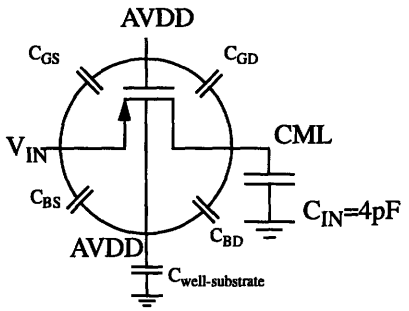

Figure 2.2a. Time t_{0-}

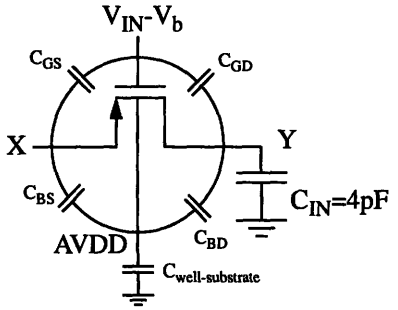

Figure 2.2b. Time t_{0+}

Figure 2.2: Charge split in a PMOS switch.

To simplify, assume the back gate is permanently connected to AVDD. In nonconducting mode, the gate is driven to AVDD, the source of the switch is driven by the input, the drain is switched to common mode level, and the well is driven by AVDD. The drain is switched to common mode level to simulate the actual differential circuit. The circuit considered thusfar is single-ended, but the actual circuit has two identical parallel paths since the SHA is differential (see Figure 1.2). In hold mode, the bottom plate of the sampling capacitors (C_S) are connected to push the differential charge stored on the capacitors onto the two hold capacitors. Thus, when the two C_S plates are connected, the drains of the sampling switches are driven to the common mode level of the inputs [3].

In the conducting mode, the gate is driven to V_b below the input. At the same time, the source is driven by the input and the drain is connected to C_{IN}. The back gate is still connected to AVDD. If it is assumed that AVDD is 5V, V_b is 2V, V_{IN} (at the instant the switch begins to conduct) is 2V, and the common mode level is 3V. X and Y represent the unknown values the input and output of the switch transition to due to the charge injection from the capacitors. These node voltages are solved for below. The charge existing on the parasitic capacitors and C_{IN} can be seen in Table 2.2:

Table 2.2: Charge split in PMOS switch

Capacitor	**Charge at time t_{0-}**	**Charge at time t_{0+}**
C_{GS}	$(5-2)C_{GS}=3C_{GS}$	$(0-X)C_{GS}$
C_{BS}	$(5-2)C_{BS}=3C_{BS}$	$(5-X)C_{BS}$
C_{GD}	$(5-3)C_{GD}=2C_{GD}$	$(0-Y)C_{GD}$
C_{BD}	$(5-3)C_{BD}=2C_{BD}$	$(5-Y)C_{BD}$
$C_{well-sub}$	$5C_{well-sub}$	$5C_{well-sub}$
C_{IN}	$3C_{IN}$	$(Y)C_{IN}$

By examining the two sides of the switch separately, approximations for X and Y can be found. X is unknown, even though the source is driven by the input, since this node glitches with the transition between t_{0-} and t_{0+}. The charge on C_{GS} and C_{BS} is conserved from time t_{0-} to t_{0+}.

$$3C_{GS}+3C_{BS} = (-X)C_{GS}+(5-X)C_{BS}$$

Using parasitic capacitor values measured in simulation of a 750/0.6 PMOS switch to solve for X yields -0.16V. Similarly, assuming a 4pF load capacitor,

$$2C_{GD}+2C_{BD}+3C_{IN} = (-Y)C_{GD}+(5-Y)C_{BD}+YC_{IN}$$

yields 4.18V for Y. Immediately after the gate is driven to V_b below the input, the switch begins to conduct, and ideally X=Y=2V. However, using the charge split model, the output glitches to a value much higher than the ideal output of 2V, and the input drops much lower than the ideal input of 2V. These glitches vary nonlinearly with input signal (the charge varies with the nonlinear capacitor values). Also, if the glitches are too large and the input and output cannot settle to the desired values within half a period of the sampling clock (25ns), the distortion performance of the circuit is affected. For these reasons, it is important to either buffer the input from switch charge injection, or to cancel the charge which is being injected. Cancellation methods are not completely accurate. In addition, it was determined in the previous section that a buffer is necessary to separate the nonlinearities of the switch from the input resistance. Thus, the most practical solution is to design a robust buffer.

2.5 Input Buffer Criteria

The input buffer between the source resistance and the switch must have high input impedance and very low output impedance, so that current drawn through the parasitic capacitors of the switch does not induce a large nonlinear voltage at the output of the buffer. The buffer must have bandwidth at least a factor of ten greater than the frequency of the input signal, while introducing little distortion in the signal path. The buffer must be able to accommodate a fairly wide output swing, and be capable of recovering from glitches caused by the opening and closing of the switch. Several low distortion buffer circuits have been investigated previously, but none have addressed the joint concerns of high input impedance, high bandwidth, and low distortion [4]-[7].

The current drawn from the buffer can become significant. For a 20MHz 1V peak-to-peak sine input, the slew rate is approximately:

$$SR \approx \frac{1V}{25ns} = \frac{40V}{1\mu s} = \frac{I}{C} \tag{2.3}$$

For MP1 ideally bootstrapped and the well buffered (all parasitic capacitors theoretically draw no current), the 4pF load capacitor draws the current necessary to slew one volt in 25 nanoseconds from the input buffer:

$$I = \frac{40V(4pF)}{1\mu s} = 0.16mA \tag{2.4}$$

So the input buffer must have a fast slew rate and the ability to supply 0.16mA of current.

2.6 Input Buffer Options

The gain of the buffer between the input resistance and the switch is ideally unity. The bandwidth sought (a decade beyond the input frequency) may not be accomplished with an operational amplifier if the distortion is to be kept to minimum levels. In addition, an operational amplifier may be more complex than the problem requires, since high gain is not necessary. Therefore, a logical choice for the input buffer is a source follower. Although this circuit introduces a DC level shift, it is the simplest method for achieving high input impedance, low output impedance, high bandwidth buffering. While the source follower is the most simple circuit, it is not the most effective.

2.6.1 Source Follower Buffer

As mentioned above, the source follower presents a high input impedance and a low output impedance over a fairly wide frequency range. However, the source follower is highly nonlinear, resulting in unacceptably large THD. We can estimate V_{GS} of a NMOS source follower to first order using Equation 2.5:

$$I_D = \frac{1}{2}\kappa'\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2.5}$$

where λ models the effect of channel length modulation, V_T is the threshold voltage of the NMOS device, and $\kappa'=\mu_n C_{ox}$. Solving for V_{GS}:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{\kappa'\frac{W}{L}(1 + \lambda V_{DS})}} \tag{2.6}$$

Thus, from Equation 1.2, V_{GS} varies nonlinearly with V_{BS}. The square root function is not linear, so V_{GS} varies nonlinearly with V_{DS}.

When the small-signal model is analyzed, more sources of nonlinearity are apparent. A NMOS source follower with an ideal current source and a capacitor as the load is pictured in Figure 2.3, along with the small signal model of an NMOS transistor.

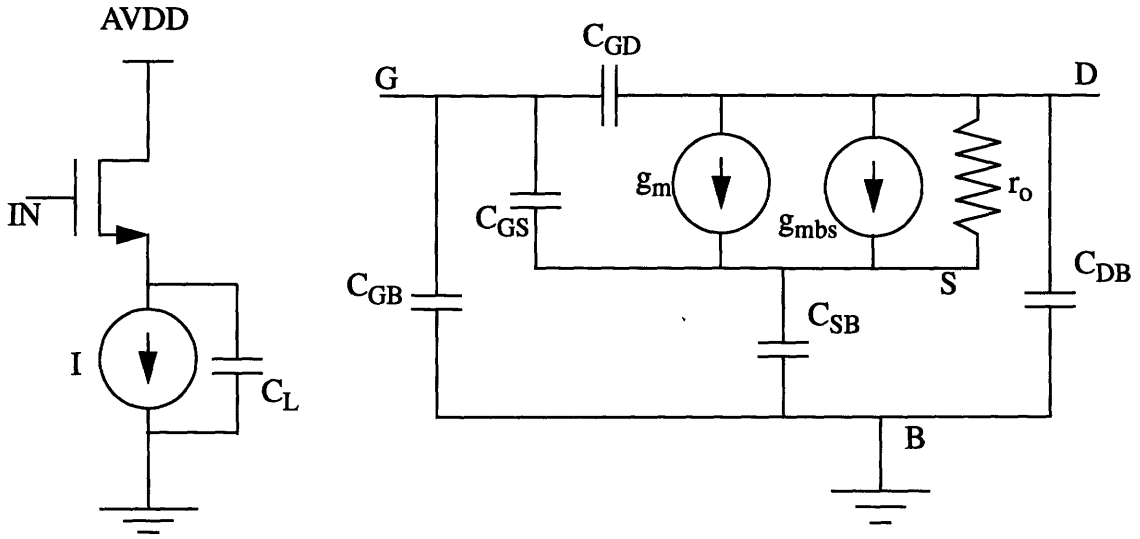

Figure 2.3: NMOS source follower and small-signal model.

Every parasitic capacitor and the load capacitor source or sink currents which are frequency dependent. For example, if the input signal is $A\sin\omega t$, then the current required to charge the load capacitor is $AC_L\omega\cos\omega t$. For different input frequencies, each capacitor draws varying current from the drain current. This is another source of nonlinearity, since with I_D varying, V_{GS} is nonlinear as a function of frequency. In addition to this, as can be seen from Equation 2.2, C_{DB} and C_{SB} vary nonlinearly with V_{DB} and V_{SB}. The nonlinear current which they draw alters the drain current and consequently, V_{GS} is nonlinear.

2.6.1.1 Techniques for Improving Distortion in the Source Follower Buffer

As is the case with the switch, to eliminate the variation due to the back gate effect, a PMOS device is used. The well can then be connected to the same potential as the source. This has the effect of keeping V_T and C_{SB} constant for varying inputs as can be seen in Equations 1.2 and 2.2. However, $C_{well\text{-}substrate}$ draws nonlinear current from the source, so a buffer can be used to drive the well to track the source. In this way, the current will no

longer be drawn from the source, but instead will be supplied by the buffer. Improving the modulation due to the drain to source variation is more difficult.

If the solution were as simple as creating a voltage drop between the gate and the drain nodes, forcing current through a diode connected transistor or poly resistor would suffice. However, if either of these methods are used, this configuration no longer functions as a voltage buffer. The disturbances on the source caused by the switch charge injection will cause a variation in the drain current of the source follower. This current will be supplied by the input signal, through the constant voltage source, to compensate for the variation on the source. Since disturbances on the output would be directly reflected in the input signal, the input is no longer buffered from the switch.

2.6.1.2 Gate to Drain Buffering

One option for reducing V_{DS} modulation is to directly buffer the drain from the gate of the source follower. However, this requires a linear buffer which is capable of driving C_{DB} and withstanding the glitches due to the switch charge injection.

The source follower buffer actively opposes disturbances at its output. In the section on charge injection, it was determined that switch transitions cause glitches at the input and output of the switch. If a source follower is driving the switch, some of the glitches are counteracted. For example, a glitch in the positive direction pulls the source of the source follower upwards. Thus, the transistor turns on more (V_{GS} becomes larger), increasing the drain current of the follower. This current is drawn from the capacitors and the switch, pulling the source potential back down. Similarly, a glitch in the negative direction pulls the source of the follower down, decreasing the drain current. The current source can supply more current to the switch and capacitors, increasing the potential of the source. Thus, the large glitch on the input of the switch calculated in Section 2.4 is reduced by the buffer.

In addition to this reduction factor, the source follower has another attribute which facilitates designing a buffer to drive the drain to track the gate. A disturbance which appears on the source is rejected by the drain. Consider the small signal model of a PMOS

source follower shown in Figure 2.4. Since the back gate is driven by a buffer from the source, the g_{mbs} current source is zero. For small signal disturbances on the source of the follower, the gate appears to be an AC ground with respect to the source (this is assuming the source follower behaves linearly and the source voltage ideally tracks the gate voltage). Thus, v_{sg} becomes v_s, and the current due to the g_m transconductance is simply $g_m v_s$.

$$v_d = [(v_s - v_d)g_{ds} + g_m v_s]R_{out} \tag{2.7}$$

Rout is the output impedance of buf1 in Figure 2.4. Rearranging the terms to solve for the ratio of v_d to v_s yields:

$$\frac{v_d}{v_s} = \frac{g_m + g_{ds}}{\left(\frac{1}{R_{out}} + g_{ds}\right)} \approx \frac{g_m}{\left(\frac{1}{R_{out}} + g_{ds}\right)} \tag{2.8}$$

If buf1 has a low output impedance, $1/R_{out} >> g_{ds}$, so the far right term becomes $g_m R_{out}$.

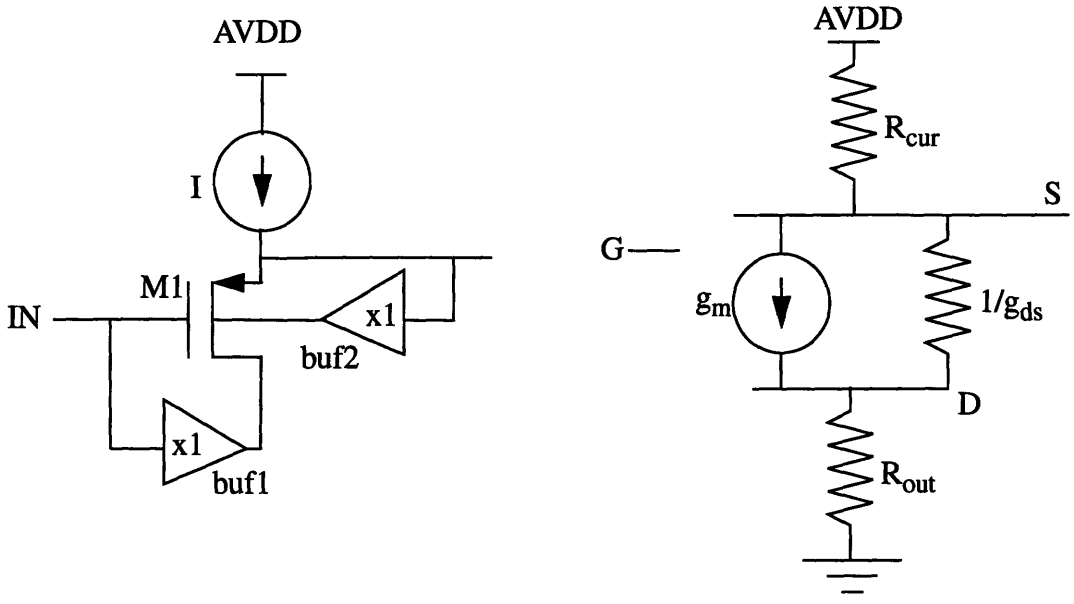

Figure 2.4: Buffered source follower.

Since the disturbances on the drain side are reduced by a factor of $g_m R_{out}$, the buffer driving the drain does not have to recover from the same magnitude glitches present at the

source of M1, as long as R_{out} is less than $1/g_m$ of M1. However, since the glitches are occurring very quickly (<1ns), the drain buffer does have to possess a high slew rate and large bandwidth.

Another benefit making the requirements on the drain buffer less strict is the attenuation of a signal from the drain to the source of a source follower. Again referring to Figure 2.4, if the drain tracks the gate (assuming the buffer driving the drain is accurate) and the source tracks the gate to first order, the gate can be considered to be an AC ground with respect to the drain and the source.

$$v_s = [g_m(-v_s) + g_{ds}(v_d - v_s)]R_{cur} \tag{2.9}$$

Rearranging and solving for the ratio of v_s to v_d yields:

$$\frac{v_s}{v_d} = \frac{g_{ds}}{\left(\frac{1}{R_{cur}} + g_{ds} + g_m\right)} \approx \frac{g_{ds}}{g_m} = \frac{1}{g_m r_o} \tag{2.10}$$

Since the disturbance on the drain of M1 is reduced by a factor of the gain of M1, the linearity requirement of the drain buffer is less stringent than that of the source follower itself.

With these benefits in mind, a logical solution is a NMOS source follower buffering the drain of M1 from the gate. The some of the nonlinearity of an NMOS source follower is correctable. Using an operational amplifier buffer to drive the drain of the source follower to track the source is discussed later in this chapter. Although the nonlinearity due to V_{DS} variation can be reduced, the nonlinearity due to V_{BS} variation cannot be corrected. The inaccuracy of the NMOS source follower is discussed in the next section, and this would also affect the linearity of M1. Therefore, an NMOS source follower is not linear enough to drive the drain of M1 to the accuracy level required by this switched capacitor circuit. A more linear option is a PMOS source follower.

A second PMOS source follower directly from the gate of M1 to the drain is an option (Figure 2.5), even though it could provide a positive level shift which would cause M1 to go into triode region if V_{SG} of M2 is too large. This can be avoided by increasing the

aspect ratio of M2, thereby decreasing the level shift, but the large parasitics of M2 on the drain of M1 and the input node may limit the bandwidth and the distortion performance of the circuit.

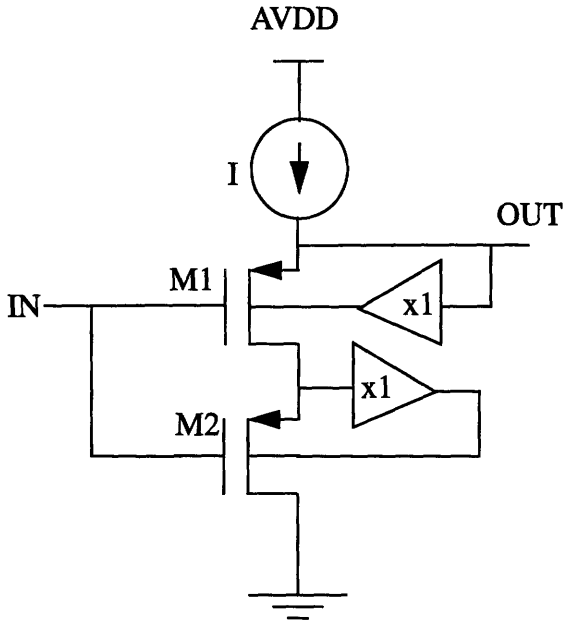

Figure 2.5: Cascoded source follower.

For a 1V peak to peak 9.375MHz input, centered around 1.5V common mode (the factors determining this common mode level will be examined later), M1 should be in the range of 600/0.6 to 800/0.6 with approximately 4mA of drain current. This range is optimal for simulations with a 600/0.6 to 800/0.6 PMOS switch and a 4pF load capacitor (C_{IN} in Figure 1.1). The switch gate and back gate are ideally buffered from the input of the switch (the gate drive is set by an ideal 2V constant voltage). The ideal switch range has the appropriate balance between the switch resistance (the larger the aspect ratio, the smaller R_{on} becomes) and the size of parasitics C_{DB} and $C_{well\text{-}substrate}$ (the smaller the ratio, the smaller the parasitics). Given these general values, V_{SG} of M1 is approximately 1.3-1.5V. To ensure operation in the saturation region, V_{DS} should be at least 0.5V. Thus, the V_{SG} of M2 must be less than 0.8-1V. With 4mA of drain current, a device on the order of 10000/0.6 is necessary to ensure both devices operate in the saturation region. The

THD of the output of M1 increases from -93dB (for M1 = 800/0.6 with ideal buffers from the gate to the drain and the source to the back gate) to -80.4dB (for M1 = 800/0.6 and M2 = 10000/0.6 with the back gates ideally buffered and the drain of M4 connected to AVSS).

The large size of M2 is limiting the performance, so using a level shifted version of the input to drive the gate of M2 would allow equal size aspect ratios for M1 and M2 without forcing M1 into triode region. As with the switch, there are a number of solutions for accomplishing the level shift.

A capacitor can be charged to a constant voltage (1V for instance) during one phase of a clock. During the second phase, the top and bottom plates of the capacitor can be switched to the gates of M1 and M2, creating a 1V drop between the two gates. However, this switched capacitor circuit may not be a valid option, since the parasitic capacitance of the switches and the glitches from charge injection cause problems at the input of the buffer. Another solution forces current through a poly resistor or a diode connected transistor as shown in Figure 2.6a. The limit to this constant voltage's distortion performance is the linearity of the current sources. The current sources have nonlinear capacitors associated with them, and these capacitors interact with the source impedance to limit the THD performance at node IN. In addition, if a diode connected device is used, the parasitic capacitors associated with the diode, in conjunction with the 1KΩ input resistor also degrade the THD performance. The merits of various constant voltage schemes are discussed in more detail in Section 3.1.

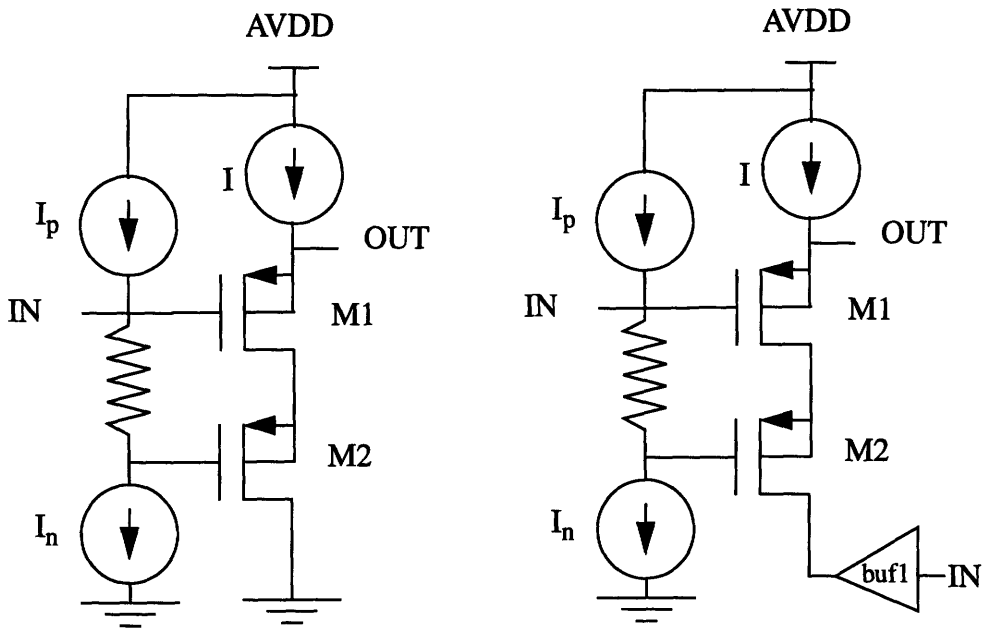

Figure 2.6: Cascoded source follower with level shift.

If M2 worked as a perfect source follower, the drain voltage of M1 would be a constant voltage minus V_{SG2} below the gate of M1. So V_{SD1} could be set at a constant voltage slightly larger than the V_{DSAT} of M1, ensuring that M1 always remained in saturation and maintained a constant V_{DS}. This would eliminate the modulation of V_{GS} due to the nonlinear dependence on V_{DS} as seen in Equation 2.6.

However, M2 does not act ideally since V_{SG2} is also distorted due to the modulation of V_{DS2}. To rectify this problem, a buffer could be used to drive the drain of M2 from node IN (buf1 in Figure 2.6b). In this way, the gate and drain of M2 would track the input. Hence, V_{SG2} would be more linear, and the source voltage of M2 (which is the drain voltage of M1) would track the input. Thus, V_{DS} variation would not occur for the M1 source follower. If the back gates of M1 and M2 were driven by buffers from their respective sources, the nonlinear effect of the C_{DB}, C_{BS}, and $C_{well\text{-}substrate}$ parasitic capacitors would

be virtually eliminated. Of course, the linearity of the buffers and constant voltage determine the extent to which the nonlinear capacitors and transconductances affect the THD.

Buffering the drain of M2 requires more circuitry to realize the extra source follower and constant voltage, so what advantage does this have over a direct buffer on the drain of M1? The answer is shown by Equation 2.10. If M2 is the same size as M1, the rejection factor for a disturbance on the drain of M2 appearing on the source of M1 is $(g_m r_o)^{-2}$. In other words, the buffer driving the drain of M2 (buf1 in Figure 2.6b) can be less linear than the source of M1 by a factor of the square of the gain of M1. Thus, the benefit of using M2 is relaxed drain buffer requirements.

Note that if the area (WL) of M2 is made larger than that of M1, $g_{m2}r_{o2} > g_{m1}r_{o1}$.

$$g_m r_o = \frac{2L_{eff}}{V_{GS}-V_t}\left(\frac{dX_d}{dV_{DS}}\right)^{-1} \propto \sqrt{\frac{W}{L}}L = \sqrt{LW} \tag{2.11}$$

The drain current of the source follower is constant, so $(V_{GS}-V_t)^2$ must decrease if the aspect ratio is increased (Equation 2.5). Thus, $|V_{GS}-V_t|$ is inversely proportional to the square root of the aspect ratio. The remainder of the second term in Equation 2.11 is proportional to the length of the device. The gain of a source follower $(g_m r_o)$ is proportional to the square root of the device area. If the area of M2 is greater than that of M1, buf1 can be less linear than if M1 equals M2. However, the area of M2 can not be increased indefinitely. The parasitic capacitors of M2 become larger, decreasing the bandwidth of the buffer.

How well does the drain buffer recover from glitches appearing on the source of M1? In Figure 2.4, glitches at the source of M1 appear on the drain, multiplied by $g_m R_{D1}$. R_{D1}, the impedance at the drain of M1, is approximately equal to R_{out} using the assumptions of Equations 2.7 and 2.8. R_{out} is the output impedance of buf1 in Figure 2.4. Adding M2 equal to M1 (Figure 2.6b) changes the multiplication factor from the source of M1 to the drain of M1 (source of M2) to $g_{m1}R_{D1new}$. R_{D1new} is the parallel combination of the output impedance of M1 (infinite with the ideal current source I) and the impedance into the

source of M2 ($1/g_{m2}$). R_{D1new} reduces to $1/g_{m2}$, so the multiplication factor (g_{m1}/g_{m2}) is approximately one. The multiplication factor from the source of M2 to the drain of M2 is $g_{m2}R_{out}$ (from Equation 2.8). Thus, the total factor from the source of M1 to the drain of M2 is $g_{m1}R_{out}$, which is unchanged from the simplified term of Equation 2.8.

$$\frac{v_{d2}}{v_{s1}} = \frac{v_{d1}}{v_{s1}}\frac{v_{d2}}{v_{s2}} = (g_{m1}R_{D1new})(g_{m2}R_{out}) = \left(\frac{g_{m1}}{g_{m2}}\right)(g_{m2}R_{out}) = g_{m1}R_{out} \tag{2.12}$$

In contrast, when the drain of M2 is connected to AVSS (Figure 2.6a), a disturbance on the source of M1 appears directly on the source of M2. As mentioned in the previous paragraph, if M1 equals M2, the multiplication factor from the source of M1 to the drain of M1 (g_{m1}/g_{m2}) is unity. This disturbance affects the linearity of M2, since V_{GS2} is non-linearly dependent on V_{DS2}. The multiplication factor can be decreased by increasing the aspect ratio of M2, which increases g_{m2}. However, the parasitic capacitance at the source of M2 also increases, decreasing the bandwidth of the buffer.

2.6.1.3 Source to Drain Buffer

A buffer from the source of M1 to the drain appears to be the most direct and accurate method of maintaining a constant V_{DS}. A voltage drop from the source to the drain is needed to keep M1 in saturation. An NMOS source follower buffer from the source to the drain can provide this voltage drop. As mentioned in the previous section, an NMOS source follower limits the THD performance at the drain of M1. The NMOS source follower is a poor choice because it is nonlinear and inaccurate. Referring to Figure 2.3 for small signal inputs,

$$v_s = \frac{g_m(v_g - v_s)}{g_{mbs} + g_{ds}} \tag{2.13}$$

$$\frac{v_s}{v_g} = \frac{g_m}{g_m + g_{mbs} + g_{ds}} \tag{2.14}$$

The signal at the source of the NMOS (the drain of M1) is an attenuated version of the M1 source voltage. For example, if $g_{mbs} = 0.2g_m >> g_{ds}$, then $v_s = 0.83v_g$. If $v_{s1} = v_g = 10\text{mV}\sin\omega t$, $v_{d1} = v_s = 8.3\text{mV}\sin\omega t$, so $|v_{ds1}| = 1.7\text{mV}\sin\omega t$. Since V_{GS1} varies nonlin-

early with V_{DS1}, the attenuation of the NMOS source follower causes nonlinearity in M1. A PMOS source follower can buffer the drain of M1 from the source. A constant voltage equal to $V_{SGPMOS} + V_{DSAT1}$ is needed between the source of the second PMOS follower and the drain of M1 to keep M1 in saturation. The constant voltage source and PMOS buffer loop is too slow to respond to fast input signal variations and charge kickback from the switch. The loop attempts to drive the drain of M1 to keep V_{DS1} constant. However, the loop input signal is delayed from the M1 input signal, so the drain voltage of M1 always lags the source voltage. In Figure 2.6b, the constant voltage source and PMOS follower (M2) loop receives its input the same time M1 does, so the same delay is not present. The additional parasitic load on the output of M1 degrades the performance of the input buffer. Finally, the benefits of the M1 source to drain disturbance reduction (Equations 2.8 and 2.10) are lost when the drain is buffered from the source. A disturbance on the source of M1 appears on the drain. Thus, a cascode PMOS source follower from the gate of M1 to the drain is most effective (Figure 2.6b).

2.6.2 Operational Amplifier Buffers

The source follower is a good choice to buffer the input resistance from the nonlinear components of the switch, but it requires much peripheral circuitry to linearize the output. An operational amplifier buffer requires less peripheral circuitry to implement. Three types of class A amplifiers are considered: a single-stage differential pair with current mirror load, a standard two-stage amplifier, and a folded cascode amplifier. The operational amplifier buffer must have high input impedance (so current is not drawn from the input signal), low output impedance (so the resistance reacting with the parasitics of the switch is not large), high open loop gain at the operating frequency of the switched capacitor circuit, and linear performance out to the operating frequency. The first criteria prevents current drawn from the input signal, and the second prevents large RC products in conjunction with switch parasitics. The last criteria is partly a function of the others.

The distortion of the input stage of the amplifier of Figure 2.7 is high. Even if PMOS input devices are used (V_{BS} variation is eliminated), the drain of mp1 modulates with the input signal, while the drain of mp0 remains constant. The buffer configuration forces

both inputs to track each other, so equal current flows through both legs of the amplifier. However, mn3 is diode-connected, while mn4 is not. Thus the drain of mn3 is at a potential of V_{GS3}, while the drain of mn4 varies with input. The sources of mp0 and mp1 are connected together, and they track the input signal (mp0 and mp1 are source followers). The V_{DS} of mp0 varies with the input signal, while the V_{DS} of mp1 varies little compared to V_{DS0}. From Equation 2.6, V_{GS0} and V_{GS1} are nonlinear and not equal. Thus, the output voltage is nonlinear with respect to the input signal. The quadratic dependence of the input pair on the current and V_{DS} makes the distortion high. The output varies, modulating V_{GS4} nonlinearly. Since V_{GS3} equals V_{GS4}, the drain of mp0 also modulates nonlinearly due to the variation of the output. In addition, parasitic capacitors draw nonlinear current from the current source and the current mirror. This amplifier is a poor choice because the distortion is high, and the gain-bandwidth (GBW) product is limited. Increasing the size of the input pair increases g_m, but C_L also increases, so the GBW product is limited.

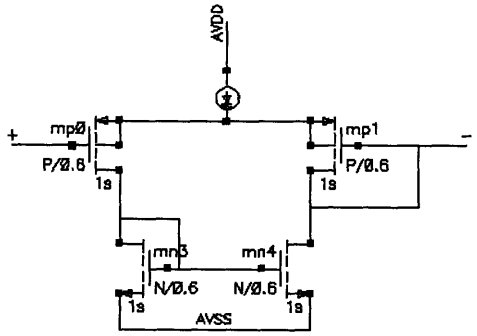

Figure 2.7: Simple single-stage amplifier configured as a buffer.

The two-stage design of Figure 2.8 is more linear than the single-stage amplifier discussed above. The drains of mn7 and mn8 are constant, since equal constant current flows through both legs. V_{GS7} approximately equals V_{GS8}, so the V_{DS}'s are approximately equal and constant. The sources of mp5 and mp6 track the input, so the V_{DS}'s of mp5 and mp6 vary with the input. V_{GS6} and V_{GS5} are both nonlinear due to the quadratic characteristic of a source follower. This distortion is similar to that of V_{GS0} of the single-stage amplifier. However, the difference between V_{GS6} and V_{GS5} is small compared to the dif-

ference between V_{GS1} and V_{GS0} of the single-stage amplifier. The distortion of the output stage is similar to that of the single-stage amplifier. V_{DS10} varies with output, affecting the drain voltage of mp6 nonlinearly. The GBW of the two-stage can be made greater than that of the single-stage. Increasing the aspect ratio of the input pair and decreasing C_c increases the GBW product.

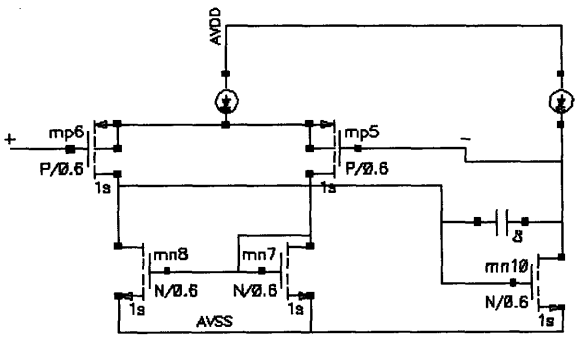

Figure 2.8: Two-stage amplifier configured as a buffer.

The folded cascode of Figure 2.9 also has lower distortion than the buffer of Figure 2.7. Like the two-stage amplifier, the drains of mp11 and mp12 are held constant, although in this case the cascode devices mn17 and mn18 perform the task. The drain variation of mp11/12 can be made equal to that of mp5/6 by appropriately sizing devices and currents. Examining Figure 2.8, equal currents flow through both legs of the first stage. However, the output of the second stage causes modulation on the drain of mp6 which is not seen on the drain of mp5. This modulation is equal to the output signal divided by the gain of the output stage ($\sim g_{m10}r_{o10}$). Similarly, from Figure 2.9, the drain of mp12 is modulated differently than mp11. This modulation is equal to the output signal divided by the gain of mn18 ($\sim g_{m18}r_{o18}$) (see Equation 2.10). Correctly sizing the device aspect ratios and drain currents can keep these two modulation factors close in size. However, other factors such as bandwidth and slew requirements may make it impractical to size these ratios and currents equally for a two-stage and folded cascode. The small signal

gain of the folded cascode is the transconductance of the input pair times the output resistance (~$g_{m11}[g_{m18}r_{o18}r_{o12}//g_{m16}r_{o16}r_{o14}]$). The GBW is limited by g_{m12}/C_L.

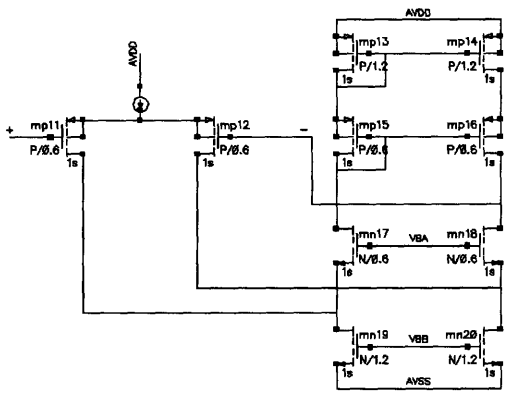

Figure 2.9: Folded cascode amplifier configured as a buffer.

The two-stage and folded cascode amplifiers have similar distortion characteristics, superior to the single-stage amplifier. Higher GBW products also make these buffers more attractive than the buffer of Figure 2.7. The other amplifiers have better THD performance than the single-stage buffer because the distortion of the input pair is matched. The difference between the V_{GS}'s of the input pair is smaller for the two-stage and folded cascode, compared to the simple single-stage.

How can these two amplifiers be improved? Increasing the gain of the amplifier at the operating frequency reduces the effect of the output stage distortion on the input stage; the GBW product must be increased. Increasing the transconductance of the first stage of the two-stage amplifier increases the gain and the crossover frequency, while keeping the same -3dB frequency. Decreasing the size of the compensation capacitor (C_c) increases the -3dB point and crossover frequency, while keeping the same gain. Either of these changes increases the GBW of the two-stage amplifier. Increasing the transconductance of the input pair of the folded cascode has the same effect it had for the two-stage. Decreasing the output load capacitance has the same effect as decreasing the C_c of the two-stage. C_c must not be reduced so much that the phase margin drops below an acceptable level, making the amplifier unstable.

Cascoding the output stage of the two-stage amplifier increases the DC gain, but the open loop -3dB point moves back proportionately so the GBW product remains the same. The variation of the drain of mp6 is divided by this larger gain, making the differential V_{DS} variation from mp5 to mp6 smaller. The cascode device can be made smaller than mn10 while still increasing the gain of the output stage by $g_{mcas}r_{ocas}$. The smaller device reduces the total parasitic capacitance at the output stage, extending the position of the second pole. This extension allows a smaller C_c, improving the GBW product.

Mirroring the current of the input pair allows current amplification. If the mirror ratio is 1:N, the effective transconductance of the input stage increases N times. A current mirror adds poles and zeros, but small mirror devices extend these poles and zeros beyond the region of concern. Increasing the effective transconductance of the input pair by N increases the GBW by a factor of N; the output referred distortion is divided by N.

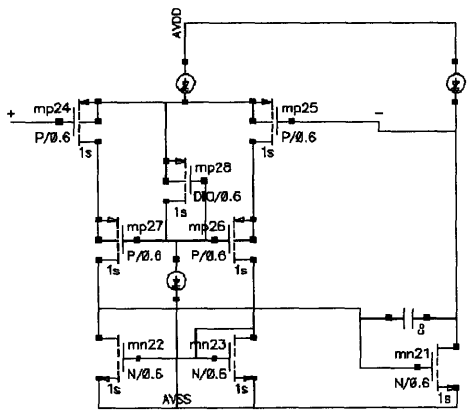

Figure 2.10: Linearizing the input pair of an amplifier.

Bootstrapping the drains of the input differential pair to track the sources eliminates the V_{DS} variation. In Figure 2.10, current is forced through a diode (mp28) to create a level shift which drives the gates of cascode devices mp26/27. The gates of mp26/27 track the sources of mp24/25. Cascodes mp26/27 force the drains of mp24/25 to track their own sources, keeping the V_{DS}'s of mp24/25 constant.

The lag between the source and drain voltages of the input pair is problematic. However, the source followers mp26/27 are sized for fast response times. The drains of the

input pair track a nonlinear version of the source voltage, causing another problem. The source voltages of mp24/25 are buffered from the drains by nonlinear source followers (mp26/27). The V_{DS} variation is nonlinear, but the variation is smaller than when the bootstrap technique is not used. Thus, the benefits of this circuit outweigh the problems.

The response to large glitches from the switch is a concern when using an amplifier configured as a buffer. Distortion at the output of the buffer appears on the negative input of the differential pair. This closed loop system has a bandwidth lower than the frequency of the glitch; the glitch propagates through the signal path of the amplifier before the buffer can react. The glitch returns to zero quickly, but the buffer recovers from the transient slowly. A large PMOS source follower with a large current source in the output stage of the amplifier improves recovery time. A PMOS follower is used to reduce the nonlinearity due to V_{BS} variation which cannot be cancelled in an NMOS follower. The source follower reduces the size of the glitch, but the amplifier must cope with a disturbance on the input. The input devices are small, with low drain current compared to the large, high current source follower. Small input devices are necessary to reduce the parasitic capacitance at the input. Consequently, to maintain the gain of the input stage, the current source supplying the input pair must be reduced. The small input devices have a slower transient response time than the large source follower. The response time is determined by the g_m/C time constant. The reduced current available to the input devices limits their g_m. In contrast, the PMOS follower has a large drain current source, so its g_m is larger in proportion to its parasitic capacitors than the g_m/C ratio of the input pair. The output of the amplifier buffer cannot settle completely from a glitch at the input in the time required (~25ns); thus it is not a good option for the input buffer.

2.6.3 Inverting Amplifier Buffer

The common mode variation of the input devices causes a problem for the buffer amplifier configuration. As the input signal swings 1V peak-to-peak, the common mode level (CML) of both the positive and the negative inputs varies. The gates and sources of the input pair vary with input signal. If the bootstrap technique is used on the input devices, the drains also vary with input. Despite these improvements, some nonlinearity is present.

If the common mode of the input pair is kept constant, distortion due to the quadratic characteristic of the devices is reduced. The distortion of the output stage then becomes dominant. However, the CML of the input pair of the amplifier buffer can not be kept constant. The input signal appears on the gate of one input device, and the output appears on the gate of the other device. An alternative is to configure the amplifier as an inverting amplifier buffer. Theoretically the CML of the input devices of Figure 2.11 do not change.

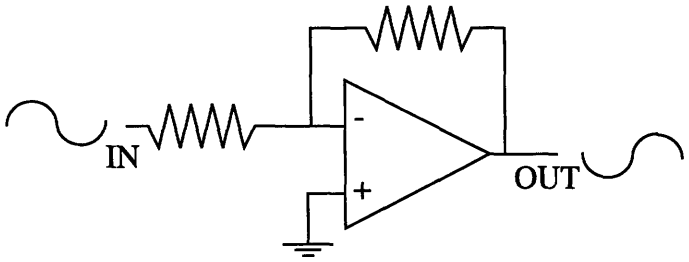

Figure 2.11: Inverting amplifier as a buffer.

The negative input terminal is driven to track the grounded positive input terminal. Even when node IN varies, the two terminals of the amplifier remain constant, improving the differential input stage distortion. In addition, the output stage distortion is reduced by the open loop gain of the amplifier at the operating frequency. Reducing the distortion via feedback has been used before in amplifier designs [7].

The reduction of the distortion in the output stage of the buffer is shown by modeling the amplifier as a feedback system. Assume the amplifier has been compensated to behave like a single pole system. The DC gain is high, the crossover frequency is at least a decade beyond the operating frequency, and the second pole occurs well beyond crossover. The amplifier can be modeled as shown in Figure 2.12. This is a simple model of the amplifier and its distortion components. Distortion does not only occur in the input and output stages of the amplifier, but rather in each transistor. However, to illustrate buffer distortion, this model suffices.

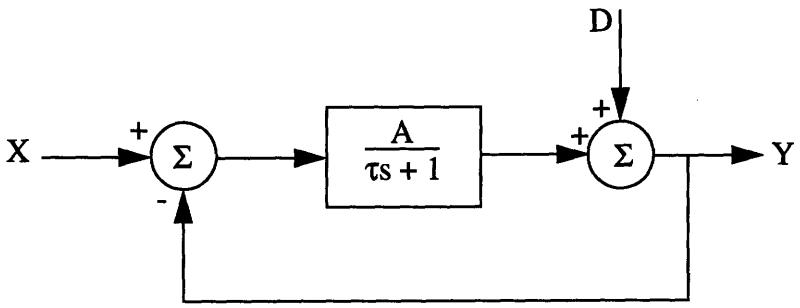

Figure 2.12: Buffer amplifier feedback system.

The input of the buffer is X, the output is Y, D is the nonlinear output stage disturbance, A is the open loop DC gain of the amplifier, and $1/\tau$ is the location of the -3dB point.

$$Y = D + \frac{A}{\tau s + 1}(X - Y) \tag{2.15}$$

Solving for Y:

$$Y = \left(\frac{\tau s + 1}{\tau s + 1 + A}\right)D + \left(\frac{A}{\tau s + 1 + A}\right)X \tag{2.16}$$

The amplifier is designed with crossover at least a decade beyond the operating frequency, so $A/(\tau s+1) > 10$. Thus, $\tau s + 1 + A$ reduces to approximately A.

$$Y = \left(\frac{\tau s + 1}{A}\right)D + X \tag{2.17}$$

The distortion of the output stage of the buffer is divided by the open loop gain of the amplifier at the operating frequency. An amplifier with high gain at the operating frequency is desired.

Although the output is not connected directly to the negative input, glitches from the switch propagate through the feedback network quickly. These glitches appear on the negative input and node IN. The closed loop inverter must respond to a fast transient, but the settling time of the amplifier is too slow to make the inverter a good choice for the input buffer. Therefore, the cascode PMOS source follower of Section 2.6.1.2 is the best

choice for the input buffer. Driving the drain of the cascode device with a buffer improves the linearity of the source follower (Figure 2.6b).

Chapter 3

Limitations and Implementation Issues

3.1 Bootstrap Circuit Limitations

Practical limits to the effectiveness of the bootstrap technique are the size, impedance, and linearity of the abstracted circuit used. The magnitude and linearity of R_{on} (the resistance of a pass transistor in the conducting mode) are directly related to the size and linearity of the mechanism bootstrapping the gate of the switch (see Equation 1.1).

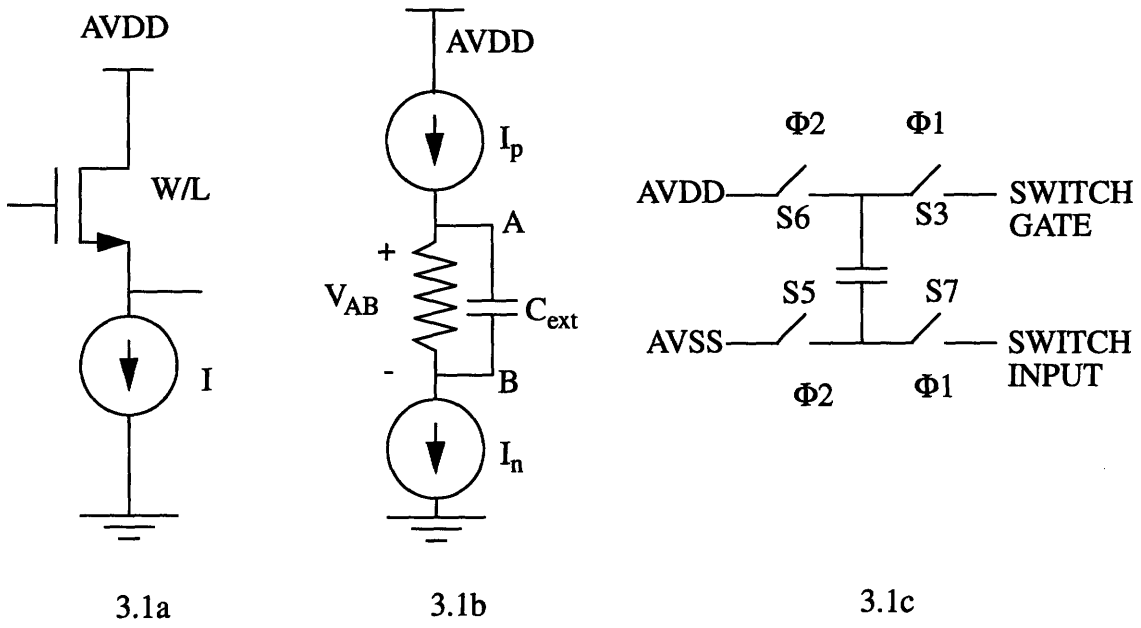

Figure 3.1: Circuits for bootstrapping the gate of a switch to the source.

A fixed drain current source follower can be used as a constant voltage source (Figure 3.1a). Setting the aspect ratio and drain current determines the value of V_{GS}. However, since the drain and well are fixed and the source varies with the input, V_{DS} and V_{BS} change with the input. These variations modulate V_{GS} nonlinearly. A PMOS source follower reduces the nonlinearity associated with the back gate effect. For conduction, the gate voltage of the PMOS switch must be below the source voltage. The positive level

shift of a PMOS source follower does not let the PMOS switch conduct. An NMOS source follower is too nonlinear, so this constant voltage source is not used.

In theory, the constant voltage can be made larger and larger, reducing R_{on} until the dynamic range of the input signal is compromised. In practice, the supplies are one of the limits of the size of the constant voltage.

The constant voltage source can be implemented with a resistor and two current sources (Figure 3.1b). These current sources require headroom below the positive and above the negative supplies to operate. The smallest voltage available to drive the gate of the PMOS switch (node B) is AVSS + ΔV_N, and the input (node A) cannot swing above AVDD-ΔV_P. ΔV_N and ΔV_P are the minimum V_{DS} required to keep an NMOS and a PMOS device in saturation, respectively. The large external capacitor (C_{ext}) provides a low impedance path for high frequency AC signals. The linearity of the constant voltage is determined by the linearity of the current sources and the interaction of the parasitics of I_n and I_p with the resistor and other elements connected to nodes A and B.

The current and resistor constant voltage source has several problems. For example, the constant voltage source is sensitive to charge kickbacks from the switch (see Section 2.4). If C_{ext} is large compared to the parasitics of the current source I_n (C_p), the glitch will cause an acceptably small change in V_{AB}. Increasing C_{ext} with respect to C_p increases the ratio $C_{ext}/(C_{ext}+C_p)$. This ratio describes the size of the glitch appearing on node B. If $C_{ext} >> C_p$, the same size glitch appears on nodes A and B, making the high frequency component of V_{AB} small. This ensures that V_{GS} of the PMOS switch remains linear, even for large glitches. Creating linear current sources is another difficulty of implementing the constant voltage source. Since the voltages at nodes A and B vary with input signal, the V_{DS} of the current sources also varies, modulating the drain current of these sources. This error can be improved by cascoding the current sources and by using impedance boosting techniques. Placing an amplifier in feedback around the cascode device boosts the impedance of the current source by the gain of the amplifier. This technique is discussed in upcoming Section 3.3. The final problem involves the parasitic capacitors of I_n and I_p.

These capacitors cause distortion by drawing nonlinear current from the constant voltage source and the switch. The cascode devices of I_n and I_p are as small as headroom constraints allow, to reduce the effects of these parasitic capacitors.

The gate of an NMOS switch can be bootstrapped or boosted above the positive supply by a switched capacitor circuit (Figure 3.1c). In one method, AVDD-AVSS is held on the storage capacitor during phase two. In phase one, this voltage is added to the input signal by switching the bottom plate of the storage capacitor onto the source of the PMOS switch and the top plate onto the gate. Another method charges the capacitor during phase two, then switches the capacitor onto a clock pulse node and the gate of the PMOS switch during phase one, creating a gate drive of AVDD-AVSS+V_{clk}.

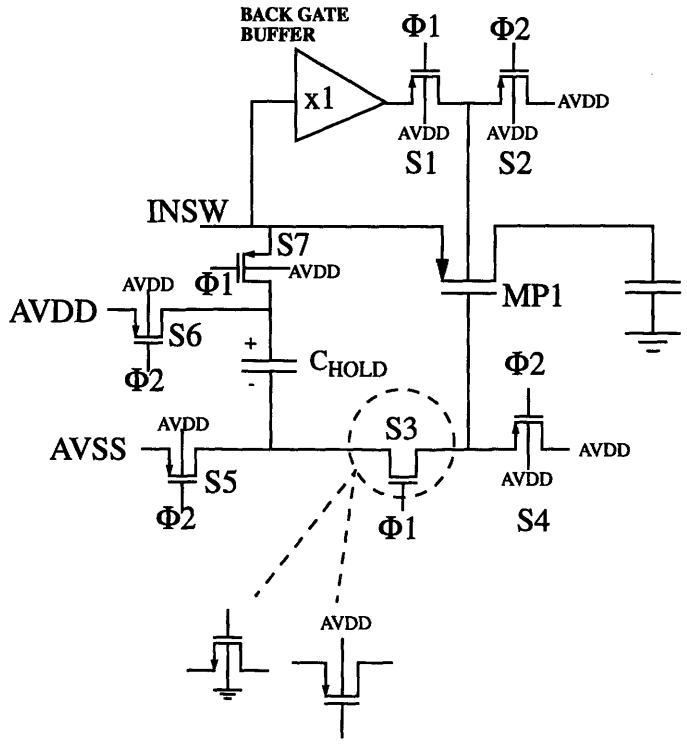

Figure 3.2: Switched capacitor bootstrap circuit.

The gate of a PMOS switch cannot be easily bootstrapped below ground by a switched capacitor constant voltage source. The difficulty is with switches S5 and S3 in the figure above. The input signal to the switch (INSW) varies between +3.5V and +2.5V, and

C_{HOLD} is switched between AVDD (+5V) and ground. The back gate buffer drives the $C_{well\text{-}substrate}$ capacitor of MP1 as described in Section 2.2. The gate drive can vary between -1.5V and -2.5V if the switches are ideal. However, if S5 is implemented with an NMOS device, the BS diode of S5 becomes forward biased when the source falls below AVSS. Charge is bled from C_{HOLD}, and the gate of MP1 is fixed at a diode threshold below ground. The NMOS device is replaced by a PMOS switch with the well connected to AVDD to prevent the DB diode from becoming forward biased. This requires the source of S5 to be changed from AVSS to $|V_{TP}|$, so S5 can conduct (if the source of S5 remains at AVSS, the PMOS switch requires a gate voltage of AVSS-$|V_{TP}|$ to conduct). If S3 is an NMOS switch, when the bottom plate of C_{HOLD} falls below AVSS, the DB and BS diodes of S3 are forward biased. If the switch is a PMOS device, the well can be connected to +5V to prevent the diodes from becoming forward biased. However, the switch cannot conduct a voltage less than AVSS + $|V_{TP}|$, unless a gate drive below ground is generated. To generate this negative voltage requires another bootstrap circuit similar to the one above. Neither S3 nor S5 of the additional gate boosting circuit can conduct, since both have negative voltages on their sources, requiring even more negative gate drives. This endless circle requires more and more negative gate voltages. Thus, a bootstrap voltage must not drive the gate below AVSS to avoid this problem.

The top plate of C_{HOLD} is charged to AVDD, and the bottom plate is charged to 2.5V during phase one. The capacitor holds 2.5V during phase two. Thus, the gate of MP1 can be driven between 1V and ground (INSW-2.5V) if S3 and S5 are NMOS switches. This corresponds to a bootstrap voltage of 2.5V when MP1 is conducting. V_{GS} of MP1 is kept constant, improving the linearity of R_{on}, as discussed in Section 2.2. Switch S7 must be small so the nonlinear parasitic capacitors do not load MP1 adversely, drawing nonlinear current from node INSW. This switched capacitor constant voltage source dissipates less power than the current and resistor constant voltage source of Figure 3.1b, since the two impedance boosted current sources are not needed in the implementation of the former.

3.2 Switch Buffer Limitations

The need for a buffer from the source of the switch to the back gate is discussed in Section 2.2. The buffer reduces nonlinearity of R_{on} due to V_{BS} modulation, maintains the linearity of C_{BS}, and drives $C_{well\text{-}substrate}$.

The buffer driving the back gate of the switch must have a high input impedance so that it does not draw current from the input of the switch. In addition, the buffer must have low output impedance so the filter formed by the buffer impedance and $C_{well\text{-}substrate}$ does not attenuate high bandwidth inputs. The buffer must have a GBW product a factor of ten greater than the frequency of the input signal of the switch, while introducing little distortion in the signal path. The back gate buffer must have a high slew rate to drive the parasitic capacitors of the switch quickly as the input slews 1V/25ns. In this instance, a simple single-stage differential pair with a current mirror load is a sufficient buffer.

The current drawn from the buffer is significant. The voltage of the back gate in hold mode ($\Phi 2$ low) is 5V (see Figure 2.1). When the clocks transition, bringing MP1 into track mode, the back gate is driven to a buffered version of the switch input. If the input is 2.5V, the buffer slews -2.5V (from 5V to 2.5V). The current to charge and discharge C_{BS} and $C_{well\text{-}substrate}$ is supplied by the buffer. If the clock transitions in less than a nanosecond and C_{BS} and $C_{well\text{-}substrate}$ are 0.75pF each, the buffer must supply -3.75mA:

$$i_{buffer} = \frac{(-2.5V)(0.75pF + 0.75pF)}{1ns} = -3.75mA \tag{3.1}$$

3.3 Impedance Enhanced Current Source

The current source supplying the source follower input buffer must be linear and must possess a high output impedance. High R_{out} is necessary because the drain of the current source varies with the input signal. A simple current source is shown in Figure 3.3. The source is connected to AVSS and the gate is driven by a DC bias source. If the voltage of the drain varies, the drain current will vary by v_{ds} times g_{ds}. If the current source is cas-

coded with M7 (Figure 3.4), the drain current will vary by v_{ds} divided by $g_{m7}(r_{o6})(r_{o7})$. For a drain variation of 1V peak-to-peak, a gain of ten for M7, and an r_{o6} of 1KΩ, the drain current varies by 100μA. This error could be as large as the desired drain current. A drain current variation this large causes changes in V_{GS} of the source follower and results in poor THD performance.

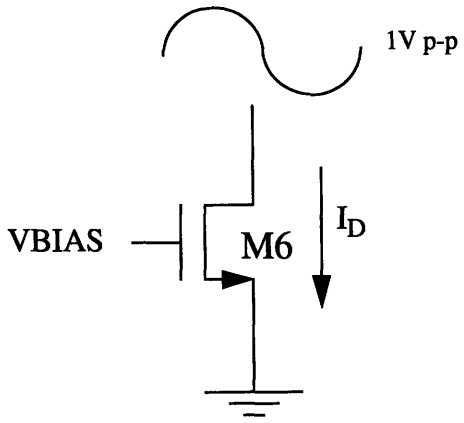

Figure 3.3: Simple NMOS current source.

Enhancing the output resistance of the transistor minimizes the effect of the drain variation. If the open-loop gain of the operational amplifier in Figure 3.4 is $A_v(s)$, the drain current variation is now v_{ds} divided by $g_{m7}r_{o6}r_{o7}A_v(s)$. Thus, for an $A_v(s)$ of one thousand, the 1Vp-p variation causes a 0.1μA drain current variation.

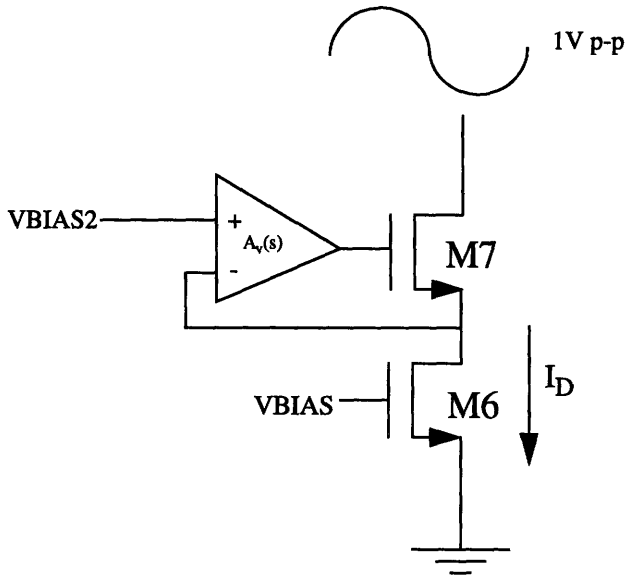

Figure 3.4: Impedance enhanced NMOS current source.

3.4 ESD Protection Circuitry and Pad Model

The user supplies an external signal to the A/D chip, so a pad model is included in the circuit simulations. ESD protection circuitry is also added to this model. The result is seen in Figure 3.5:

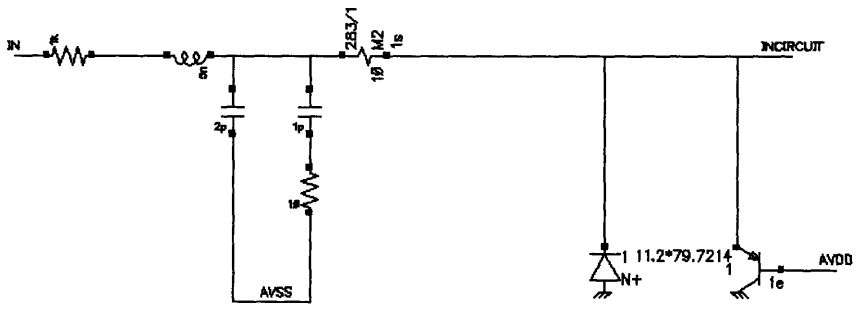

Figure 3.5: Pad model and ESD protection circuit.

The parasitic capacitors of the ESD circuit interact with the 1KΩ source impedance to cause poor THD performance. Specifically, the nonlinear capacitance of the N+ diode and C_π of the pnp transistor are problematic. Connecting the ESD circuit, the pad model, and the series resistance to an ideal source (perfectly linear input signal), an ADICE5 (Analog Devices' version of SPICE) simulation yields a THD of -63.33dB with respect to the fundamental level. The input of the simulation is a 1V peak-to-peak 9.375MHz sine wave with a 1.5V CML, run at 125 degrees C with slow models. The performance goal of -72dB THD for a 20MHz input is unattainable before the buffer and switch have been considered. Eliminating the ESD circuitry improves the THD performance. However, ESD protection is critical, so this circuit remains on the chip. Another option utilizes capacitor compensation to linearize the ESD capacitance.

3.5 Capacitor Compensation Technique

A plot of C_{DB} for NMOS transistors of various sizes is shown in Figure 3.6 (the gate and source are grounded). The value of C_{DB} for PMOS devices of various sizes for the same drain sweep is shown in Figure 3.7 (the gate, well, and source are connected to AVDD). Both figures show the nonlinear characteristic of the parasitic capacitors. These nonlinear capacitors, in conjunction with the series resistor, limit the THD performance of the circuit. The capacitor characteristic can be made more linear by adding another capacitor in parallel with the first [8]. The second capacitor has a nonlinear characteristic opposite that of the first. In Figure 3.7, the first derivatives of the PMOS C_{DB} curves are positive. To compensate, a capacitor with a negative first derivative is attached to the drain node of the PMOS device. The curves in Figure 3.6 have positive derivatives, so an NMOS is used to compensate the nonlinearity of the PMOS parasitic capacitor (Figure 3.8a). Attaching an NMOS device to the drain of the PMOS device achieves the desired effect. The gate of the NMOS is connected to the source and AVSS.

The cancellation of part of the nonlinear characteristic of the PMOS C_{BD} capacitor is seen in Figure 3.9. The curves of Figure 3.6 do not precisely match corresponding curves in Figure 3.7, so the nonlinearity is not completely cancelled. However, a more linear capacitance over the region of operation is achieved through this compensation technique.

Only C_{BD} is considered, since the capacitors due to gate overlap are more linear compared to C_{BD}. Also, C_{BS} and $C_{well\text{-}substrate}$ do not affect the circuit since the back gate and the source of the PMOS device are connected to AVDD, and the back gate and the source of the NMOS device are connected to AVSS.

An NMOS device is compensated with a PMOS device (Figure 3.8b). The back gate of the PMOS is connected to the gate and AVDD, and the drain of the PMOS is connected to the source and node A. Again, the notable NMOS parasitic is C_{BD}, since the back gate and source are connected to AVSS. However, the compensation PMOS device is not connected as it is in Figure 3.8a. The nonlinear C_{BD} and the nonlinear C_{BS} act in parallel as the compensating capacitor.

The dominant parasitic of the ESD protection circuit is $C\pi$ of the pnp device. Compensating with another pnp transistor, the THD of the circuit simulated in Section 3.4 is -79.6dB. The base of the compensation pnp is connected to INCIRCUIT (Figure 3.5), and the collector and emitter are connected to AVSS. The MOS compensation techniques described above are used on the parasitic capacitors of the impedance enhanced current sources. This compensation scheme increases the total capacitance of node A, which is detrimental to some circuits in terms of lowered bandwidth or added instability.

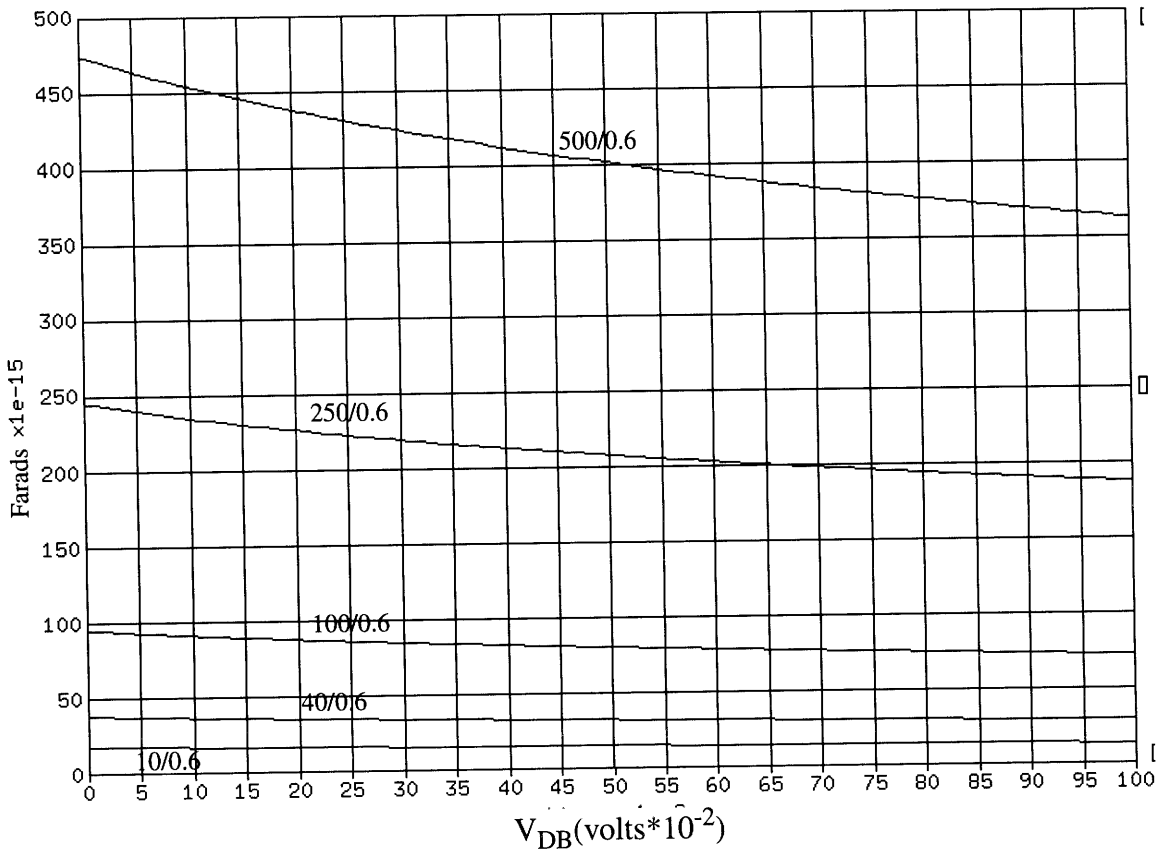

Figure 3.6: C_{DB} for various size NMOS.

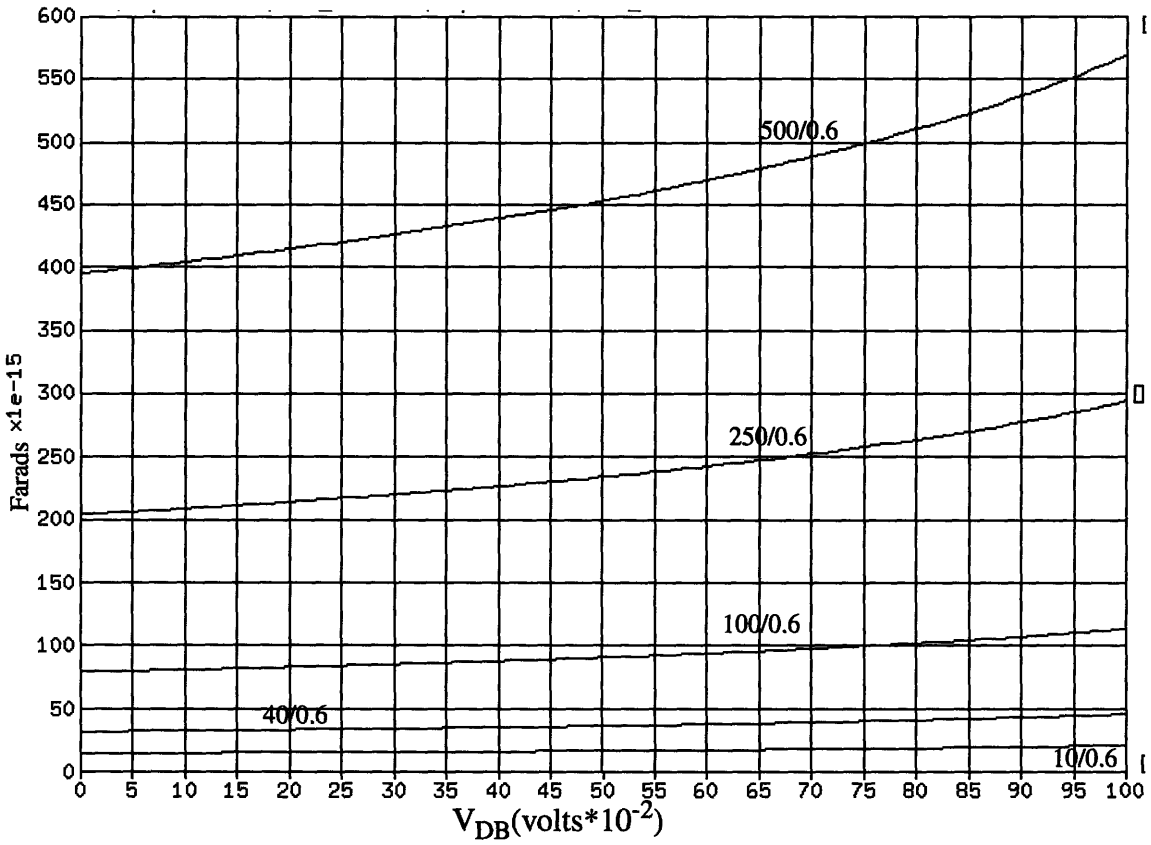

Figure 3.7: C_{DB} for various size PMOS.

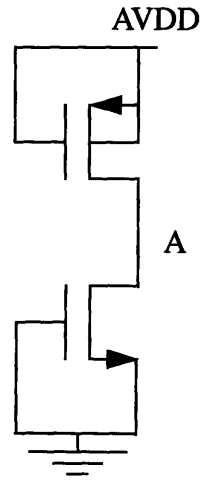

Figure 24a.

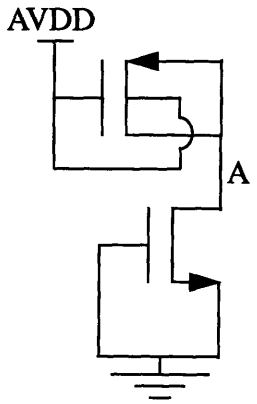

Figure 24b.

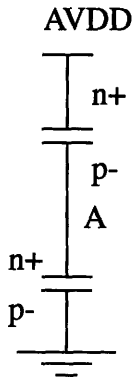

Figure 24c.

Figure 3.8: Methods of compensating nonlinear capacitors.

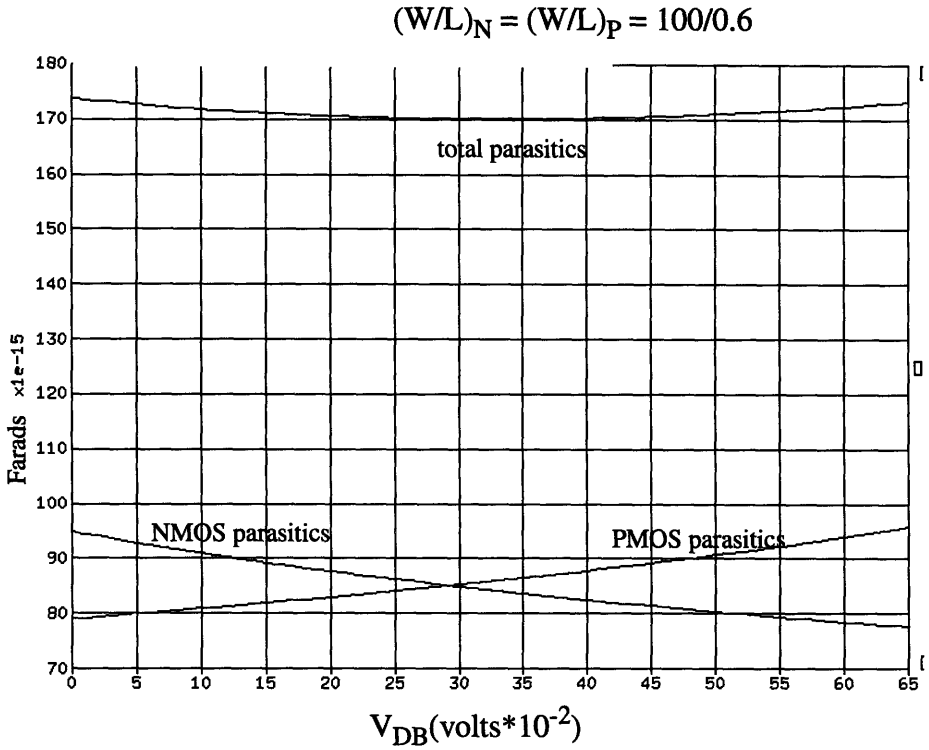

Figure 3.9: Compensated total parasitic capacitance.

Chapter 4

Implementation

4.1 Constant Voltage Source for the Switch

A switched capacitor constant voltage source provides a 2.5V bootstrap voltage (see Figure 3.2). The top plate of the 10pF C_{HOLD} is charged to 5V and the bottom plate is charged to 2.5V during hold mode. The 2.5V source is generated by a 1KΩ-1KΩ resistor divider between AVDD and AVSS. The plates are charged through two 50/0.6 PMOS switches (S5 and S6). The gate of the 800/0.6 MP1 switch is driven to AVDD by a 10/0.6 PMOS device (S4). During the track mode, the bottom plate of C_{HOLD} is connected to the gate of MP1 through a 30/0.6 NMOS device (S3). Simultaneously, the top plate of C_{HOLD} is connected to the source of MP1 by a 30/0.6 PMOS device (S7).

4.2 Switch Back Gate Buffer

A differential pair and a current mirror load comprise the back gate buffer (Figure 4.1). Devices and currents are sized for a GBW product above 200MHz (a decade beyond the 20MHz sampling frequency). The amplifier exhibits a flat open-loop gain of 25dB up to 30MHz.

Switches mp36 and mp61 of Figure 4.1 connect the back gate of MP1 to AVDD and the back gate buffer output, respectively (modeled by S2 and S1 in Figure 3.2). A trade-off is made between switch resistance (speed) and switch parasitic capacitance (linearity). The aspect ratio of mp36 is 10/0.6. The aspect ratio of mp61 is 50/0.6, so the back gate of MP1 can transition from AVDD to the back gate buffer output voltage quickly. This aspect ratio is determined to be optimum by simulation. If mp61 is smaller, the back gate of MP1 settles to the buffer output value too slowly. The settling time of the back gate affects the size of the charge glitch onto the input node of the switch (see Section 2.4). If mp61 is larger, the parasitic capacitors cause an unacceptable amount of distortion at the output of the back gate buffer.

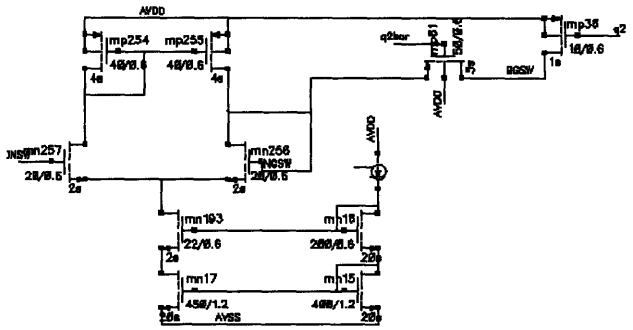

Figure 4.1: Switch back gate buffer.

4.3 Dummy Switch

A dummy switch (MP2) reduces the magnitude of the charge glitch from MP1 (Figure 4.2). Placing a 750/0.6 PMOS device (MP2) in parallel with the parasitics of MP1 improves the THD performance. The back gate, source, and drain of MP2 are connected to the source of MP1. The gate of MP2 is driven by a signal 180 degrees out of phase with the gate drive of MP1. The gate of MP2 is driven to AVDD when the gate of MP1 tracks the input, and vice versa. MP2's gate drive is generated by a switched capacitor circuit similar to that of Section 4.1, except the clock phases q1 and q2 are exchanged for q2bar and q1bar, respectively.

If the back gate of MP1 was permanently connected to AVDD, MP2 would be half the size of MP1. The charge injection caused by the transition of one side of C_{GS1} would be cancelled by $C_{GS2} + C_{GD2}$ moving out of phase with MP1 [9]. However, for the circuit of Figure 4.2, the back gate of MP1 alters between a buffered version of INSW and AVDD. MP2 is sized such that C_{GS2} and C_{GD2} approximately cancel the charge injection due to C_{GS1}, C_{BS1}, and $C_{well\text{-}substrate1}$.

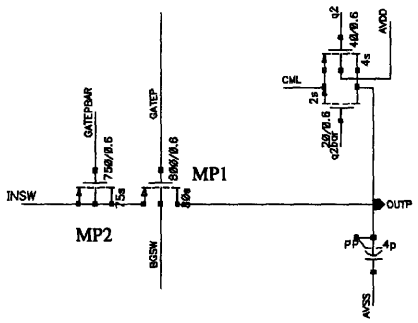

Figure 4.2: Switch, dummy switch, and load.

4.4 Source Follower Buffer

A PMOS source follower (M1 in Figure 4.3) isolates MP1 and MP2 from the input resistance. The source follower is 800/0.6 and has a drain current of 4mA. These values were determined through simulations. The source follower has a large aspect ratio and small length for maximum g_m and minimum parasitic capacitance.

4.4.1 Source Follower Back Gate Buffer

The back gate buffer for the source follower input buffer (Section 2.6.1.1) is another PMOS source follower (M3 in Figure 4.3). The drain of this follower is connected to AVSS. The PMOS follower is 200/0.6 and has 2.55mA of drain current. This buffer provides a positive level shift from the input, so the back gate of the main source follower buffer is shifted higher than the source. This is advantageous because C_{BS} is more linear reverse biased than forward biased.

4.4.2 Source Follower Drain Buffer

Two similar methods of buffering the drain are presented. The first employs a cascoded PMOS source follower (M2) to drive the drain of M1 (Figure 4.3). M2 is 800/0.6 and its drain is connected to AVSS. The drain of M2 is not buffered because the THD improves a few dB in exchange for the increased area and power demands of an additional buffer. The gate voltage of M2 is generated by a current/resistor constant voltage source con-

nected between the gates of M1 and M2. The impedance enhanced current sources of the constant voltage source force 200μA through a 2.5KΩ poly resistor.

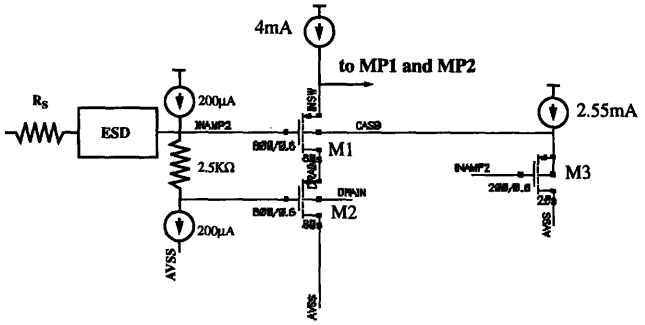

Figure 4.3: Cascoded source follower drain buffer for input buffer.

The second drain buffer is best implemented by a two-stage amplifier (Figures 4.5), but a folded cascode drain buffer is also simulated (Figure 4.4). The amplifier buffer must be at least -60dB linear, with a large GBW product. More importantly, it must respond quickly to the glitches appearing on the drain of M1. For inputs less than 20MHz, the folded cascode buffer performs better than the two-stage buffer. The performance of the two-stage should be superior, since the two-stage amplifier has a higher GBW product and is more linear than the folded cascode. The folded cascode's exceptional performance is due to a cancellation of nonlinearities which is not guaranteed under all conditions. Although the cancellation holds under process, temperature, and frequency variations in ADICE5, it will likely not hold true under 'real world' conditions. A combination of the nonlinearities of the back gate buffer, the impedance enhanced current source of M1, and the folded cascode attain better performance than should theoretically be possible. The R_{out} of the folded cascode is $1/G_{m1}$. The transconductance of the input pair of the folded cascode buffer (G_{m1}) is one-fourth the size of the transconductance of M1 (g_{m1}). Thus, a glitch on the source of M1 is amplified by four (g_{m1}/G_{m1}) and appears on the drain. The R_{out} of the two-stage buffer is $1/(G_{m1}R_1G_{m2})$. G_{m1} and G_{m2} are the transconductances of the first and second stages, and R_1 is the output resistance of the first stage. $G_{m1}R_1G_{m2}$ is greater than g_{m1}, so a glitch on the source of M1 appears attenuated

on the drain. The two-stage buffer should have better THD performance than the folded cascode. The drain of M1 should be more linear for the two-stage buffer, so the nonlinear V_{GS} variation of M1 should be smaller than when the folded cascode buffer is used. Additionally, the output stage of the two-stage buffer has higher g_m and more current than the output leg of the folded cascode. This should be an advantage for the two-stage buffer.

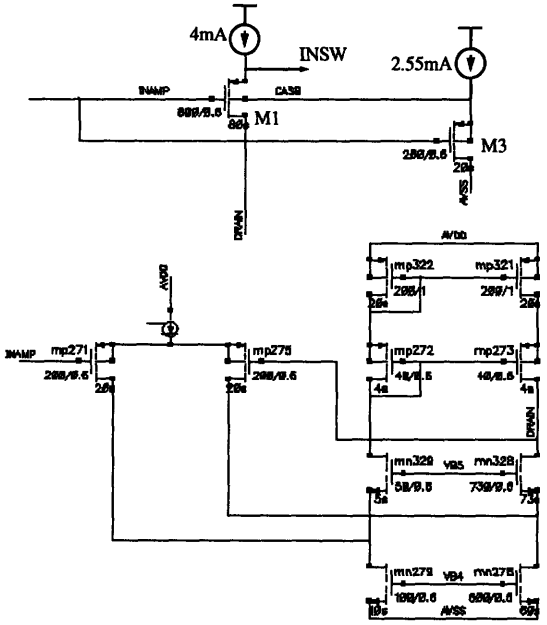

Figure 4.4: Folded cascode drain buffer.

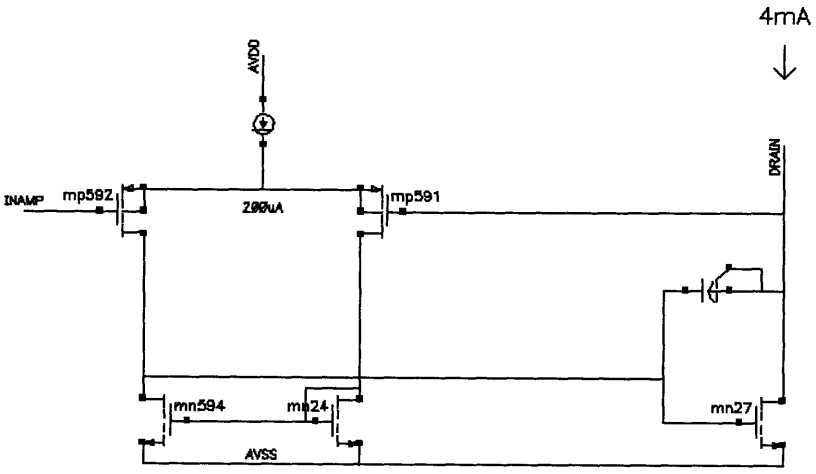

Figure 4.5: Two-stage drain buffer.

4.5 Impedance Enhanced Current Source Amplifiers

Two-stage operational amplifiers boost the impedance of the NMOS and PMOS current sources (Section 3.3). A trade-off is made in these amplifiers between settling time and open-loop gain at 20MHz. The parasitic capacitors of the differential pair of the amplifier, M6, and M7 (of Figure 3.4) limit the performance attainable. If the GBW product of the amplifier is increased, the crossover frequency approaches the second pole. This encroachment reduces the phase margin and settling time in response to transients. Attempting to increase the phase margin reduces the crossover frequency, and the gain of the amplifier at 20MHz is decreased. To respond favorably to the charge injection from the switch, fast settling time is crucial. The gain of the amplifier at 20MHz determines the linearity of the current source. Higher gain yields higher effective impedance, so the current varies less with drain voltage variation. The optimal trade-off is a gain of 30dB at 10MHz and a phase margin slightly less than 45 degrees at crossover. This phase margin could be unsafe, but the simulated amplifier did not oscillate.

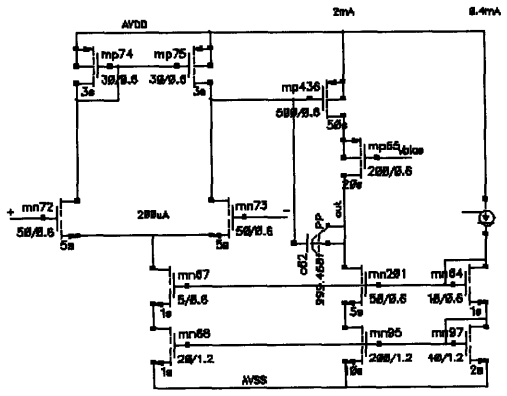

Figure 4.6: Impedance enhancement amplifier for PMOS current sources.

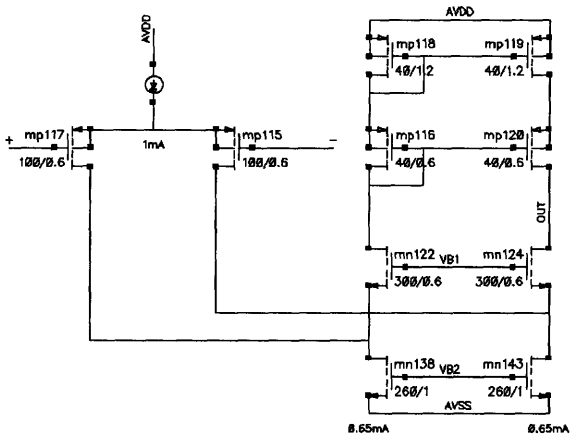

Figure 4.7: Impedance enhancement amplifier for NMOS current sources.

Chapter 5

Results

5.1 Simulations

The schematic capture tool used is Cadence. The simulator tool is ADICE5, an Analog Devices' version of SPICE. Three combinations of temperature and models are used in simulations: 125 degrees C and slow devices (low f_τ), 25 degrees C and nominal models, and -45 degrees C and fast devices (high f_τ). The simulations are referred to as hot/slow (A), nominal (B), and cold/fast (C). The THD performance of the cold/fast simulations are routinely as good as or several dB better than the nominal and hot/slow simulations. The chip will usually operate between 25 degrees C and 125 degrees C because of the heat dissipated by the circuit. For these reasons, some simulations do not include case C.

The common mode level of the simulations is 1.5V. Supplies of ground and +5V suggest setting the CML at 2.5V for maximum dynamic range. However, the PMOS source follower has an inherent 1.5V level shift from input to output. If the CML is set at 2.5V, a 1V peak-to-peak signal reaches 4.5V at the source of the source follower buffer. The linear 4mA current source must function in the remaining 0.5V of headroom. Simulations determined that the size of the cascode device required to meet this constraint is too large. To operate in the prescribed 0.5V, a V_{DS} of 0.25V is allowed for the current mirror device and an additional 0.25V is allowed for the cascode device. For a 4mA current source, the smallest cascode device meeting the requirements is 2240/0.6. The size of C_{DB} and the size of the voltage variation of the drain of the cascode limits the linearity of the current source to -60dB. Decreasing the CML to 1.5V indirectly improves the THD of the circuit. The maximum voltage of the source of the PMOS source follower buffer becomes 3.5V, so 1.5V of headroom remains for the 4mA current source. Consequently, the cascode device is reduced to 250/0.6. The THD performance of the current source improves to -74dB for a 9.375MHz input signal.

Simulated waveforms and an FFT plot of the output of the optimized switch are shown below. The input signal is a 1Vp-p 9.375MHz sine wave. The CML is set to 2.9V, anticipating the 1.4V positive shift of the PMOS source follower buffer. The sampling frequency is 20MHz, and the simulations are case A. The THD of the output of this improved switch is -57dB, since the switch is driven through a 1KΩ source impedance. Reducing the resistance to 10Ω improves the THD to -74dB. The source follower buffer presents this low (~10Ω) output impedance to the switch, justifying its use.

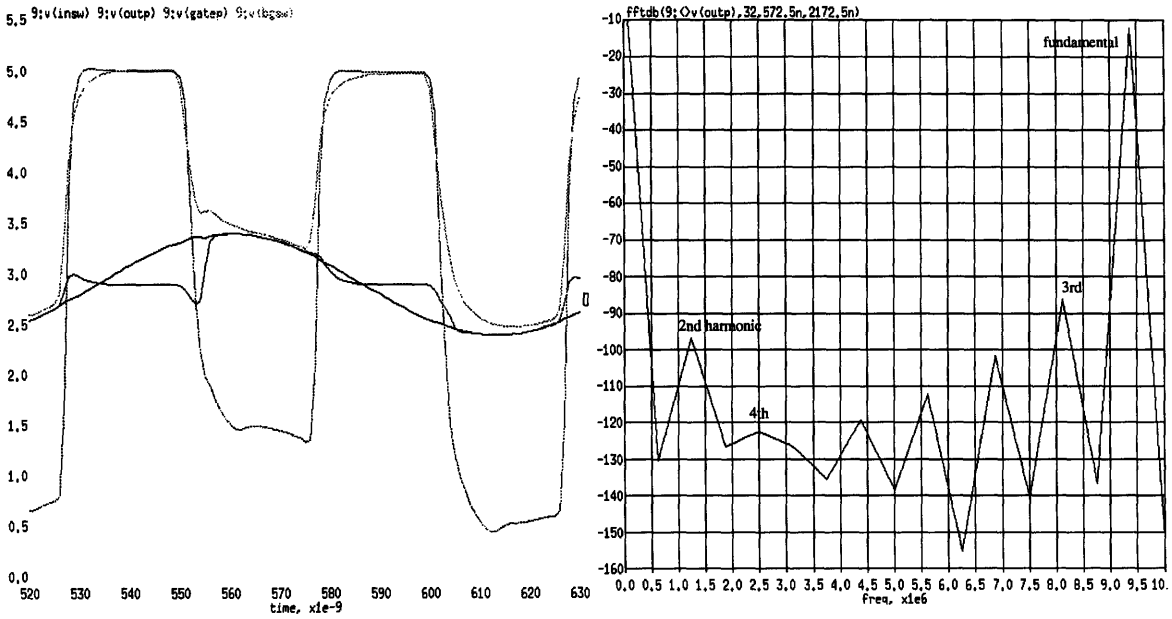

Figure 5.1: Simulated waveforms and an FFT of the improved switch.

Waveforms of the improved buffer block and an FFT of the source voltage of the source follower buffer (M1) are shown in Figure 5.2. INAMP, DRAIN, CASB, and INSW are the gate, drain, back gate, and source of M1, respectively. The drain buffer is a two-stage amplifier. Figure 5.3 shows the transient response of the input and output of the buffer in response to a 1V step at the input of the 1KΩ input resistor (IN).

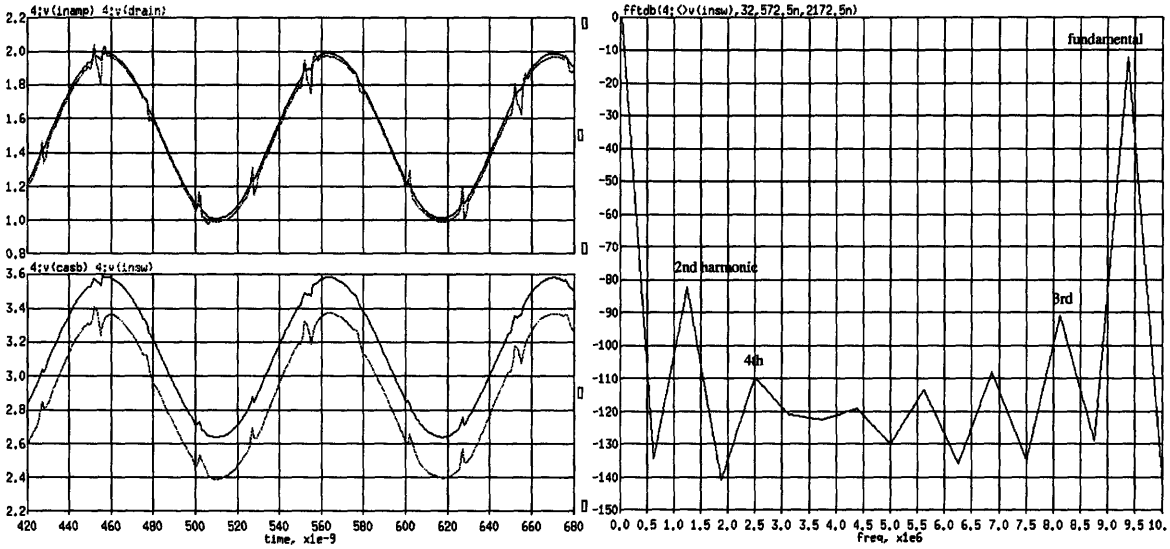

Figure 5.2: Simulated waveforms and an FFT of the input buffer.

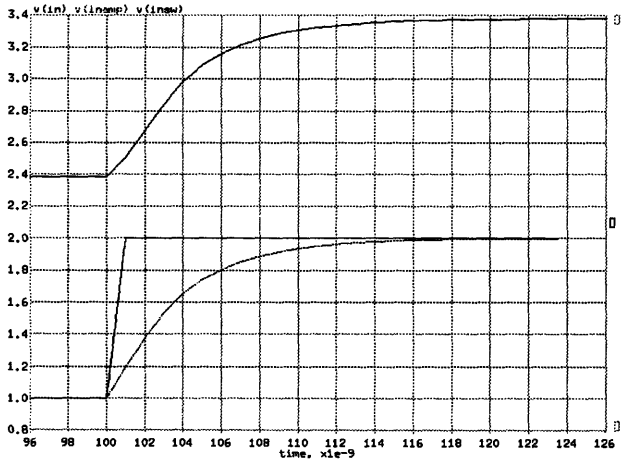

Figure 5.3: Transient response of the buffer and improved switch.

5.2 Calculation of THD

The THD is calculated by taking an FFT of a simulated waveform. The FFT produces a plot similar to that of Figure 5.2 (on the right). The fundamental frequency is located at 9.375MHz for this simulation, and the second and third order harmonics occur at 18.75MHz and 28.125MHz. The second and third harmonics are aliased, and they appear in the FFT plot at 1.25MHz and 8.125MHz, respectively. The sampling frequency is

20MHz, hence Nyquist is 10MHz. For a 32 point FFT, the number of bins is 16: the DC component, the fundamental frequency, and the second through fifteenth harmonic frequencies. The magnitude of each harmonic frequency bin is root-sum-squared to yield the harmonic distortion relative to the fundamental frequency. The fundamental amplitude of the simulations is -12dB. This number is subtracted from the root-sum-square result (less than 0dB) to yield the THD. The program which performs these calculations is shown in Appendix B.

5.3 THD Results

The simulated performance of three circuits with 1V p-p 9.375MHz sine wave inputs centered at 1.5V CML is shown in Tables 3-5. Table 6 illustrates THD performance for the two best circuits in response to a 38.125MHz sine wave input.

Table 5.1: Simulated THD Performance (Nominal)

	1.875MHz	6.875MHz	9.375MHz	19.375MHz
folded cascode drain buffer	-77.9	-81.8	-80.1	-62.0
two-stage amp drain buffer	-88.8	-87.6	-81.7	-64.8
cascoded PMOS followers	-76.4	-76.3	-77.1	-71.9

Table 5.2: Simulated THD Performance (125 deg C/ slow models)

	1.875MHz	6.875MHz	9.375MHz	19.375MHz
folded cascode drain buffer	-78.0	-78.7	-78.2	-52.7
two-stage amp drain buffer	-77.2	-73.7	-71.1	-60.1
cascoded PMOS followers	-74.9	-70.6	-68.3	-59.3

Table 5.3: Simulated THD Performance (-45 deg C/ fast models)

	1.875MHz	6.875MHz	9.375MHz	19.375MHz
folded cascode drain buffer	NS	NS	NS	NS
two-stage amp drain buffer	-90.1	NS	-83.4	-66.7
cascoded PMOS followers	-79.7	NS	-72.3	-81.2

Table 5.4: Simulated THD Performance @ 38.125MHz

	nominal	hot/slow	cold/fast
two-stage amp drain buffer	-58.1	-49.4	-57.4
cascoded PMOS followers	-63.2	-51.5	-71.7

NS: Not Simulated (as explained in Section 5.1).

Chapter 6

Conclusion

The folded cascode buffer driving the drain of M1 has better THD performance below 10MHz. However, at higher frequencies the THD of the cascoded PMOS source follower circuit is higher. The two-stage drain buffer circuit exhibits a blend of the good performance of both circuits. For wideband applications below 20MHz, the two-stage circuit or the cascoded PMOS circuit is recommended. For applications above 20MHz, the cascoded PMOS source follower circuit is advised. The GBW product of the cascoded source follower buffer is higher than that of the folded cascode or two-stage drain buffers. All three circuits utilize the same improved switch circuit. A top-level diagram of the joint buffer and improved switch circuit is shown below:

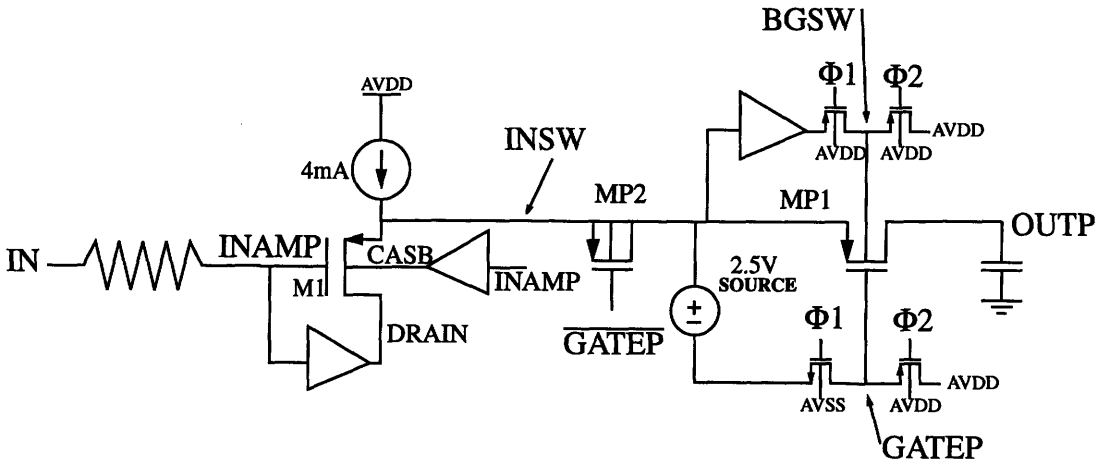

Figure 6.1: Top-level input buffer and improved switch.

All of the mechanisms of harmonic distortion are not compensated for in this circuit. However, this buffer and switch circuit exhibits THD performance which is better than that of an NMOS switch with constant gate drive. Harmonic distortion in various switch circuits has been examined and suggestions have been made to reduce the sources of nonlinearity. Following these recommendations, the THD performance goals are achieved.

Appendix A

Explanation of Total Harmonic Distortion

The output of the circuit in Figure 1.1 is related to the input by a power series. The series consists of a scaled linear function of the input and scaled higher order terms of the input. By applying a sinusoidal signal to the circuit, the input/output relationship can be determined as a function of input frequency [10]. For example, the power series can be represented with the general equation:

$$V_0 = a_1 V_s + a_2 V_s^{\,2} + a_3 V_s^{\,3} + \ldots \tag{A.1}$$

The scale factors can themselves be functions of frequency. The sinusoid input is:

$$V_s = \hat{V}_s \sin \omega t \tag{A.2}$$

Thus, the relationship between the input and output:

$$V_0 = a_1 \hat{V}_s \sin \omega t + a_2 \hat{V}_s^2 (\sin \omega t)^2 + a_3 \hat{V}_s^3 (\sin \omega t)^3 + \ldots \tag{A.3}$$

can be rewritten as:

$$V_0 = a_1 \hat{V}_s \sin \omega t + \frac{a_2 \hat{V}_s^{\,2}}{2}(1 - \cos 2\omega t) + \frac{a_3 \hat{V}_s^{\,3}}{4}(3 \sin \omega t - \sin 3\omega t) + \ldots \tag{A.4}$$

The multiples of the fundamental input frequency ω are called harmonics. The terms associated with these harmonic frequencies are distortion terms, since they are not present in the input signal. The magnitudes of the harmonic terms at a given input frequency ω are root-sum-squared. The magnitude of the input signal is then subtracted from this total, yielding the total harmonic distortion (THD).

Appendix B

Code for Simulation of Total Harmonic Distortion

```
*THIS PROGRAM COMPUTES THE THD OF THE INPUT VOLTAGE WAVEFORM SPECIFIED
*BY &1 = V(IN) BY SUMMING THE ENERGY IN THE FFT BINS EXCEPT FOR THE BIN
*CORRESPONDING TO THE FUNDAMENTAL FREQUENCY OF THE INPUT SIGNAL, FIN
*                                   FIN = (FS/PTS)*BINS
*WHERE FS IS THE CLOCK SAMPLING FREQ, PTS IS THE NUMBER OF POINTS FOR THE FFT
*(MUST BE A POWER OF 2), AND BINS IS THE NUMBER OF BINS SUMMED
*
*ADICE5 INPUT LINE MUST BE OF THE FORM: use thd3 v(out),20meg
*WHERE v(out) IS THE INPUT WAVEFORM FOR &1 AND 20meg IS THE SAMPLING
*FREQUENCY (FS) IN &2
*
*THIS VERSION ACCOUNTS FOR THD CALCULATIONS MADE ON UNDERSAMPLED INPUTS
*(INPUTS GREATER THAN NYQUIST)
*IN THE BELOW NYQUIST CASE, BINS ARE MIRRORED INTO CORRESPONDING BINS ABOVE
*NYQUIST, BUT SHOULD NOT BE COUNTED TWICE.

set sumsqr=0
set bins=15
set pts=32

if bins>pts then
 set osbns=mod(bins,pts)
else
 set osbns=bins
endif
set fs=&2
set fny=fs*osbns/pts
set delta=fny-(fs/2)
set fny2=(fs/2)-delta
set binsz=fs/pts
```

```
set k=0
set j=0

set x=fftm(&1,pts,572.5n,2172.5n)
if (bins/pts >= 1/2) then
 do k=1 to (pts/2)-1 by 1
  if (k*binsz != fny2) then
   if (k*binsz != fny) then
    set sumsqr=sumsqr+ (deval(x,k*binsz))**2
    endif
  endif
 enddo
else
   do j=1 to (pts/2)-1 by 1
    if (j*binsz != fny) then
    set sumsqr=sumsqr+ (deval(x,j*binsz))**2
    endif
   enddo
endif

set thd=0
set thd=20*log10(sqrt(sumsqr))
print thd
set fund=deval(x,fny)
set fundb=20*log10(fund)
print fundb-thd
```

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