Improved Performance Alternator with Fully Integrated Switched-Mode Rectifier

by

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Abstract

The use of Power Electronic circuits has helped to advance the technology of automotive alternators. The use of a Switched-Mode Rectifier (SMR) allows the alternator to run at a load-matched condition, optimizing power and efficiency over all operating speeds. However, the use of SMR's has largely been focused on designs for 42 V alternators.

This thesis presents the design, build, and characterization of an SMR-based alternator that provides improved power and efficiency at the present automotive standard of 14 V. The SMR-based machine was built from commercial electronic devices and packaged such that it could be fully integrated into the alternator housing without impacting the physical structure or reliability.

The SMR-based alternator was characterized in a laboratory environment (25°C ambient temperature) over the standard operating range of 1500 rpm (idle speed) to 6000 rpm (cruising speed). The alternator operated in a load-matched condition, achieving maximum power output up to 2400 rpm and achieved cruising speed output power of 2178 W at full field current of 4.3 A.

Thesis supervisor: David J. Perreault
Title: Professor of Electrical Engineering

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Chapter 1

1. Introduction

In this introductory chapter a motivation for the research is presented. The present alternator architecture is briefly evaluated and the proposed benefits of the new architecture are introduced. The goals of the thesis work are outlined and an organization of the thesis is presented.

1.1 Motivation

Over the years the number of electrically-driven loads in vehicles has continually increased. Manufacturers have introduced a number of new features and functions to the modern automobile and they have sought to make many standard features electrically driven as well. As such, the electrical power required of traditional automotive power generators is increasing as shown in Figure 1.1.

As the trend of increasing electrical power continues to rise, limitations of the

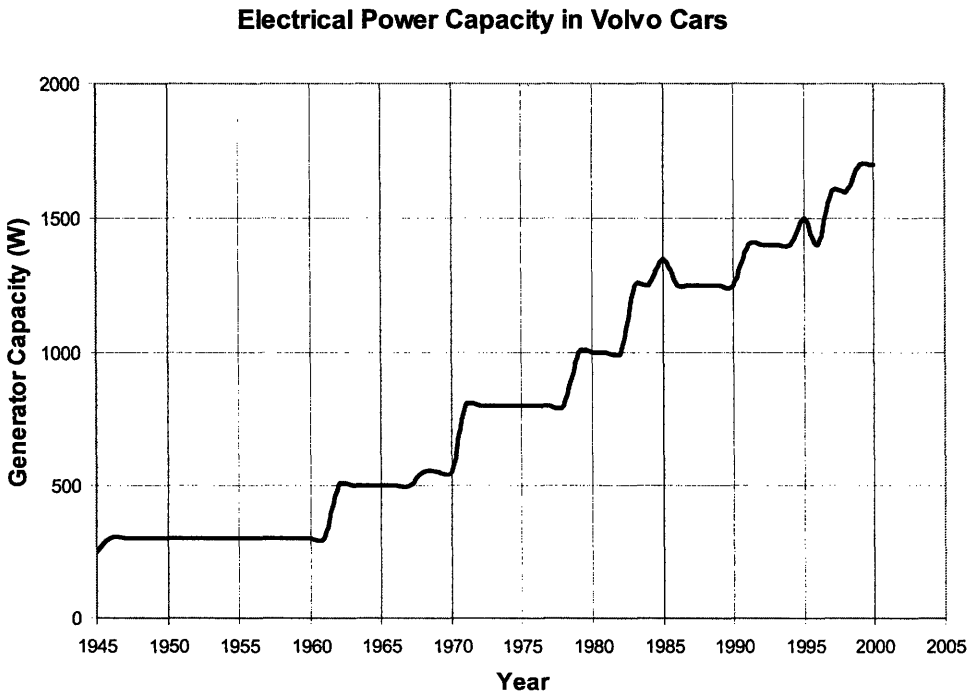

Figure 1.1 Installed electrical power in Volvo cars from 1945-1999[11]

present-day power generation technology available in most cars will soon be reached. Moreover, there is a growing desire to achieve much higher efficiencies than are typically found in conventional Lundell alternators, which are typically below 50% for many operating conditions [1, 6]. In addition to environmental and fuel consumption concerns, higher efficiencies are of commercial interest in truck and fleet vehicle applications where operating costs are a significant purchasing consideration. This has resulted in a need to develop new technologies that will improve performance and meet the growing need for electrical power [1-5].

The push towards a more powerful alternator that can overcome the limitations of the present system faces many practical and financial challenges. There is a substantial research effort focused on using power electronic circuits to address the increasing power and efficiency requirements without sacrificing much of the investments put into the manufacturing infrastructure in place for current Lundell alternators [1-5].

1.2 Theory of Operation

1.2.1 Lundell Alternator with Full Bridge Diode Rectifier

Presently, automobiles are manufactured with a conventional Lundell alternator machine connected to a full-bridge diode rectifier. The Lundell alternator transforms mechanical energy into electrical energy by generating an electromotive force (EMF) that is dependent on the regulated field current, i_f, and the rotational speed of the alternator shaft, ω, [1, 6] as is shown in the expression

$$V_s = k\omega i_f . \tag{1.1}$$

The value k is the machine constant in units of volts-seconds per ampere-radian. The 3-phase sinusoidal voltages generated by the machine are rectified by the full bridge diode

rectifier. The rectified DC voltage then supplies power to various loads throughout the automobile as well as supplying a constant charge to the battery, which is connected to the output of the diode rectifier. The battery serves as a constant voltage load at about 14 V. It is used as a "stand-by" power supply to address the electrical needs of the car when the engine is not running, and to start the automobile's engine.

A simplified electrical model of the alternator machine with constant voltage load is shown in Figure 1.2. The electrical model shown in Figure 1.2 is analyzed in [2]. Based on the analysis in [2], an approximation of the alternator output power can be expressed as

$$P_{out} = \frac{3V_o}{\pi} \frac{\sqrt{V_s^2 - \left(\frac{2V_o}{\pi}\right)^2}}{\omega L_s} \tag{1.2}$$

where V_o is the output voltage, V_s is the peak amplitude of the EMF, ω is the electrical

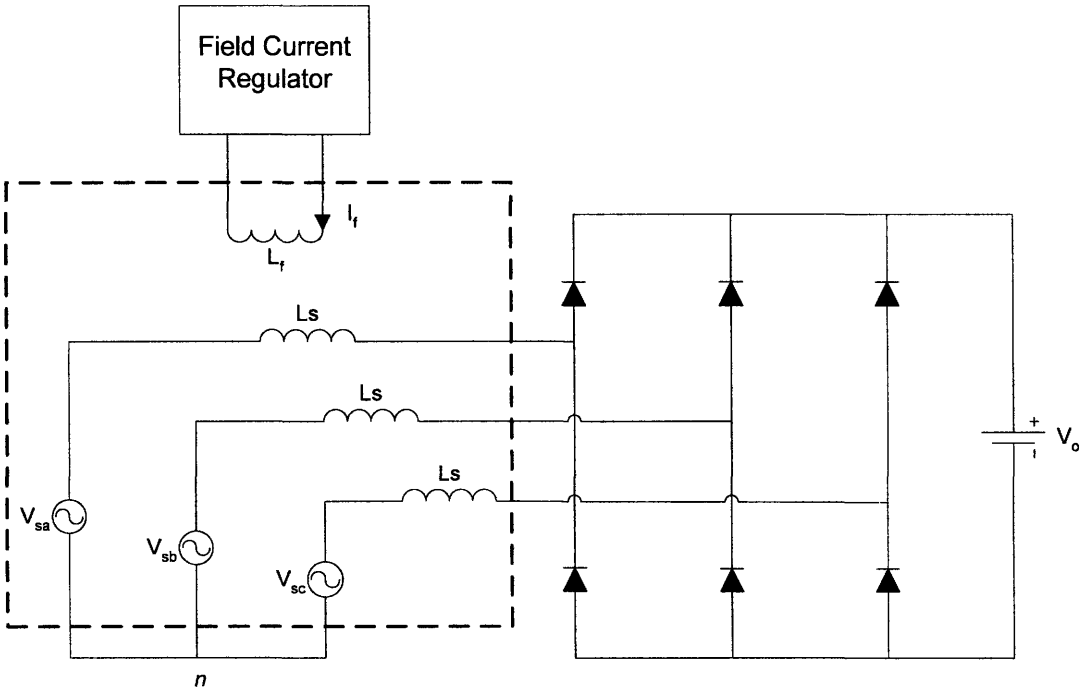

Figure 1.2 Electrical model of Lundell alternator [2]

frequency of the EMF, and L_s is the armature synchronous inductance [2].

At a fixed field current, equation (1.2) can be used to generate a set of curves mapping output power versus output voltage at different operating speeds. These curves are shown for one particular alternator in Figure 1.3. The alternator at any speed and load voltage can provide any power level lower than the corresponding curve, by operating at a field current lower than the one used to generate the curve. The output power capability is maximized at one output voltage for any speed, but is reduced to zero above a certain output voltage [1]. For the alternator of Figure 1.3, a 14 V output is nearly optimal at 1800 rpm. But at higher speeds, 14 volts is far below the power-optimizing voltage. A 42 V load will draw much more power from the alternator at higher speeds

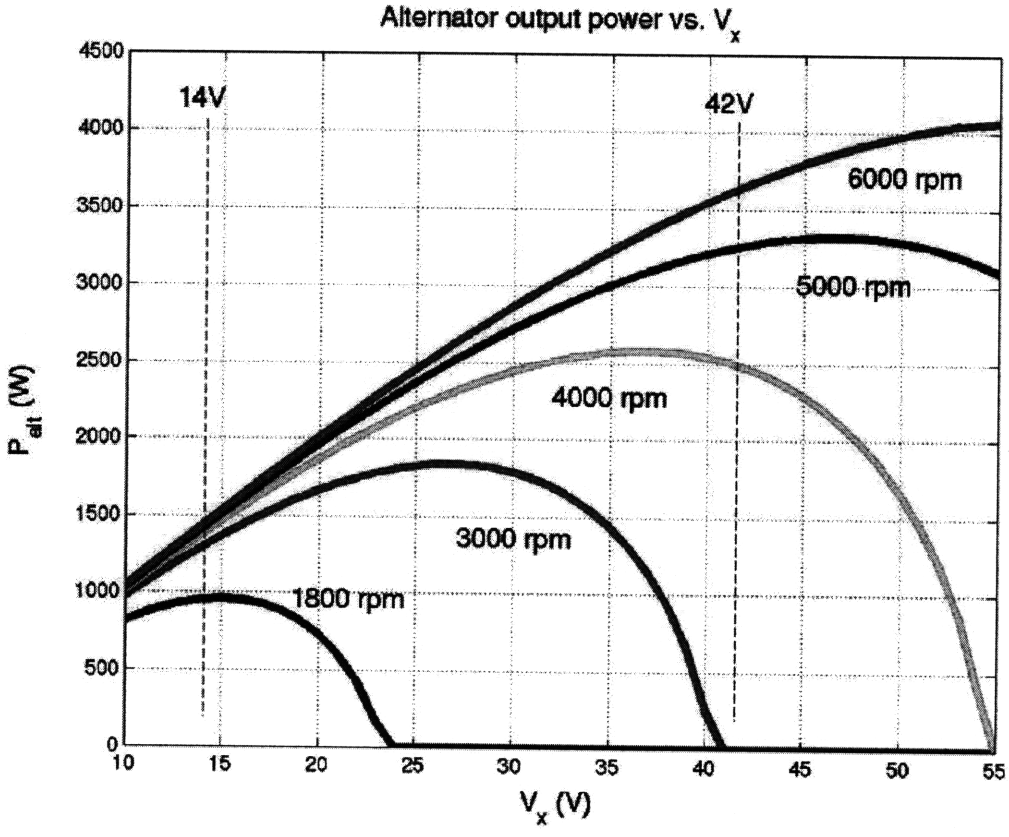

Figure 1.3 Output Power vs. Voltage over different alternator speeds [1]

than the 14 V load can draw at any speed. But below about 3000 RPM, the alternator is unable to deliver any power to a 42 V load.

1.2.2 Switched-mode Rectifier with Load Matching

The concept of load-matching was introduced in [1, 7]. Consider the alternator and switched-mode rectifier shown in Figure 1.4. In this system, a diode bridge is followed by a "boost switch set" comprised of a controlled MOSFET switch Q_x and a diode D_x. This topology incorporates a new control capability into the traditional rectifier structure. The new control capability allows for high frequency modulation of the controlled switch, so that the effective output voltage of the alternator can be matched to the voltage required for maximum power at the given alternator speed [1]. The operation of such a circuit is analogous to a DC-DC boost converter.

The switch Q_x is modulated at a fixed duty ratio d. When the switch is off, the diode D_x conducts and the ac current is working through the rectifier into a voltage v_o.

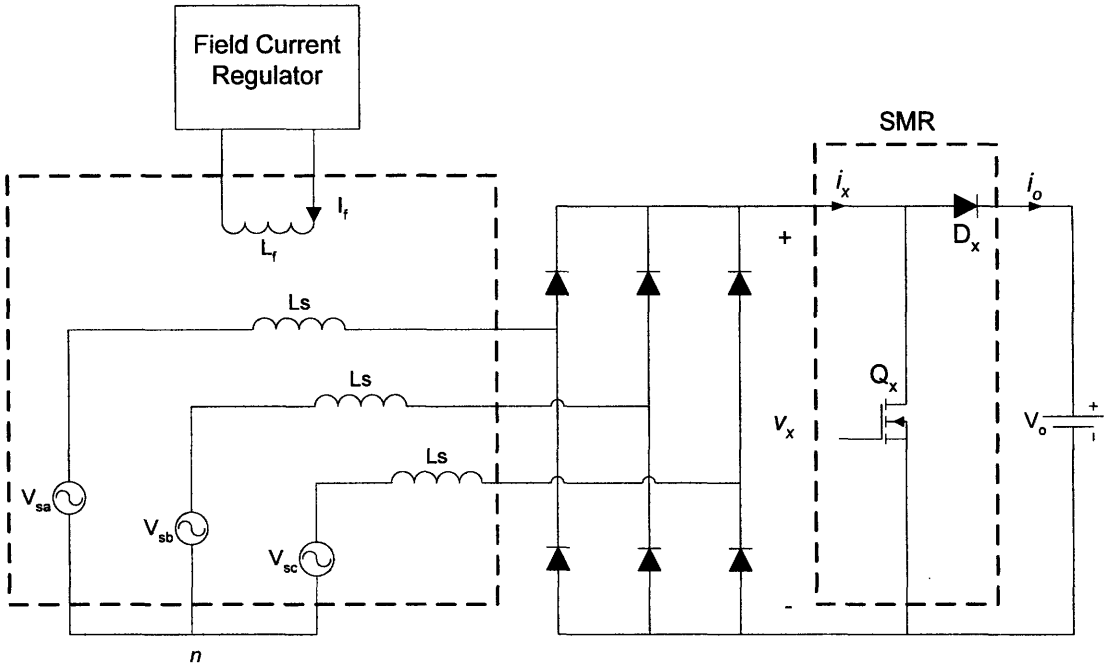

Figure 1.4 Alternator with switched-mode rectifier (SMR) [1]

When the switch is on, the ac current is shunted to ground. This is essentially the same as working through a rectifier into a voltage of zero. On average, the system behaves as if it is working into a voltage source of voltage v_x, where v_x is given by equation (1.3).

$$\langle v_x \rangle = (1-d)v_o \tag{1.3}$$

$$\langle i_o \rangle = (1-d)i_x \tag{1.4}$$

The corresponding output current i_o of the system is given by equation (1.4). This effective voltage scaling is known as load-matching where the voltage seen by the machine, is being scaled to match the optimal load voltage at the given operating speed. The added control freedom made it possible to design an alternator that could operate along the dotted line shown in Figure 1.5, optimizing the alternator's power output and

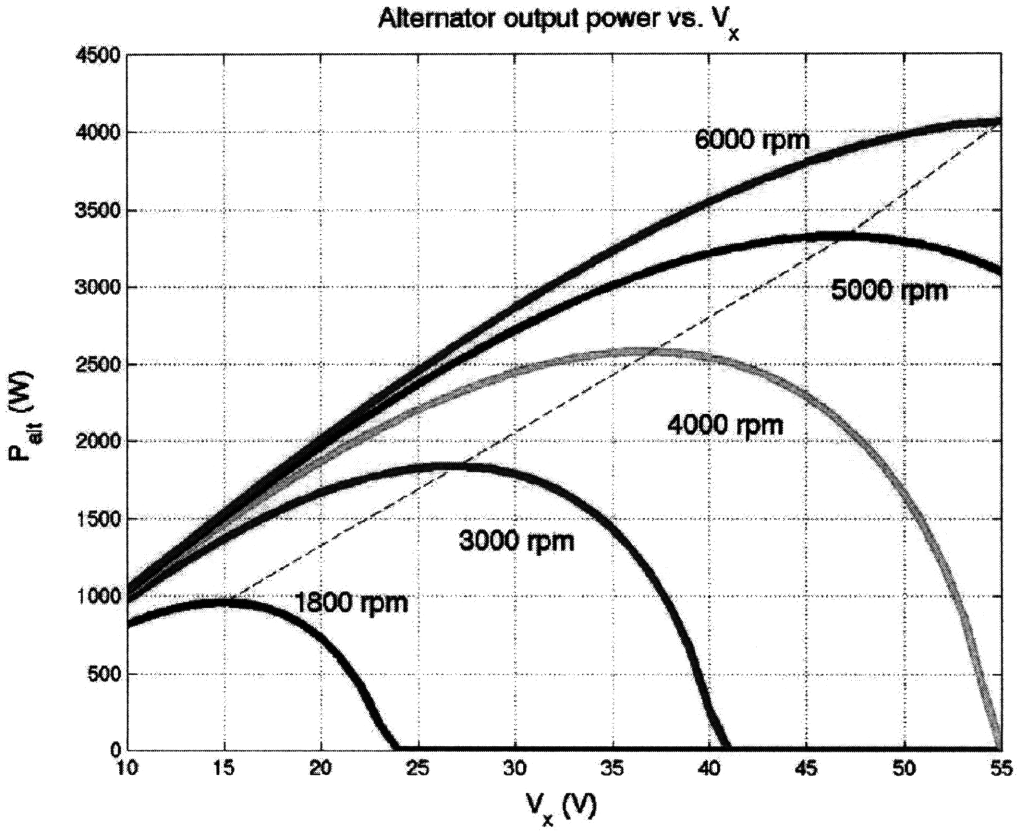

Figure 1.5 Load-matched alternator output

efficiency regardless of speed. This new topology is referred to as a Switched-mode-rectifier or SMR.

1.3 Thesis Objective

Many challenges still exist in making the transition from a conventional to a more powerful and efficient alternator. These challenges are due in large part to the difficulty of incorporating the additional power electronic circuitry into the current alternator structure without affecting the reliability of either the alternator or the circuitry. The under-hood environment of a car poses a harsh environment [16-18] that would expose commercial electronic devices to conditions not normally encountered.

The objective of this thesis is to design and develop an alternator capable of addressing the manufacturing challenges mentioned above while offering improved performance over the conventional Lundell machine. The design will focus on three areas listed below:

1. Increasing average output power into a fixed 14 V output at the high end operating speeds while maintaining the optimal load-matched power capabilities at lower RPM. Previous designs (e.q [1, 5]) have focused on 42 V output designs which have different tradeoffs in the design of the power electronics.
2. Maintaining the improved efficiency provided by the SMR over a wide range of loads. This will be based on the "efficiency optimized control law" proposed but not implemented in [1, 7].
3. Design for manufacturability; that is working with available off-the-shelf devices and implementing a circuit board layout that will not alter the physical structure or manufacturing practices of a present-day alternator design.

Using a combination of the control handles (field current, switch modulation, etc) and working with newer, more capable power products it is possible to optimize the output power from Equation 1.2 such that increased power (up to a fixed level determined by device capability) at any alternator speed can be delivered to a fixed output voltage of 14 V.

1.4 Outline of the Thesis

This design encompasses a variety of technical challenges that can be broken down into the different tasks listed below:

- Device Selection
  Select a set of commercial devices that could meet the electrical, mechanical, and thermal criteria imposed by the design goals.
- Thermal Characterization and Modeling
  Evaluate the electrical performance and operating conditions to reasonably approximate the power dissipation in the devices. Create a model for the thermal transfer capabilities of the devices and experimentally verify the model accuracy.
- Alternator Characterization and Modeling
  Experimentally characterize a commercial alternator to identify important performance parameters such as field current, synchronous inductance, winding resistance, and output power capability. Use parameters to develop a computational model that will calculate the expected performance improvements at different winding ratios. Choose a winding ratio that will satisfy the design goals while not overstressing the devices.
- Implementation of control strategy
  Implement a basic control strategy that will allow for verification of hardware capabilities. This will include the use of duty-cycle modulation, synchronous rectification, zero-crossing detection, and a speed sensor for the alternator.
- Layout and packaging
  Design a PCB and heat sink that will be a form-fit replacement of the diode rectifier in the commercial alternator. All power devices and control circuitry will be contained within the PCB. The PCB and heat sink should not alter the size or structure of commercial alternator housing.
- Design verification
  Experimentally evaluate the new alternator. Verify that the machine parameters scale according to the winding ratio and verify that the performance of the new machine is consistent with the computational model. Attempt to explain any discrepancies between the computational and the experimental results.

Chapter 2

2. Device Selection

One of the major challenges of this design is embedding commercial power electronic devices into a harsh automotive environment [16-18]. The devices must be suited to meet the rigorous operating conditions while being able to optimize performance and maintain reliability. In this chapter the important electrical and thermal parameters for device selection are discussed and a set of power and auxiliary devices is chosen. Finally, test specifications are generated to exercise the devices and validate electrical and thermal performance.

2.1 Power Devices

For the power devices operating in the SMR, performance optimization will be based on power handling capability and thermal transfer capabilities. The SMR will be implemented as a 3-phase MOSFET and diode boost configuration as shown in Figure 2.1. In order to produce the intended output power it was necessary to find commercial MOSFETs and diodes that are capable of handling the voltage and current requirements

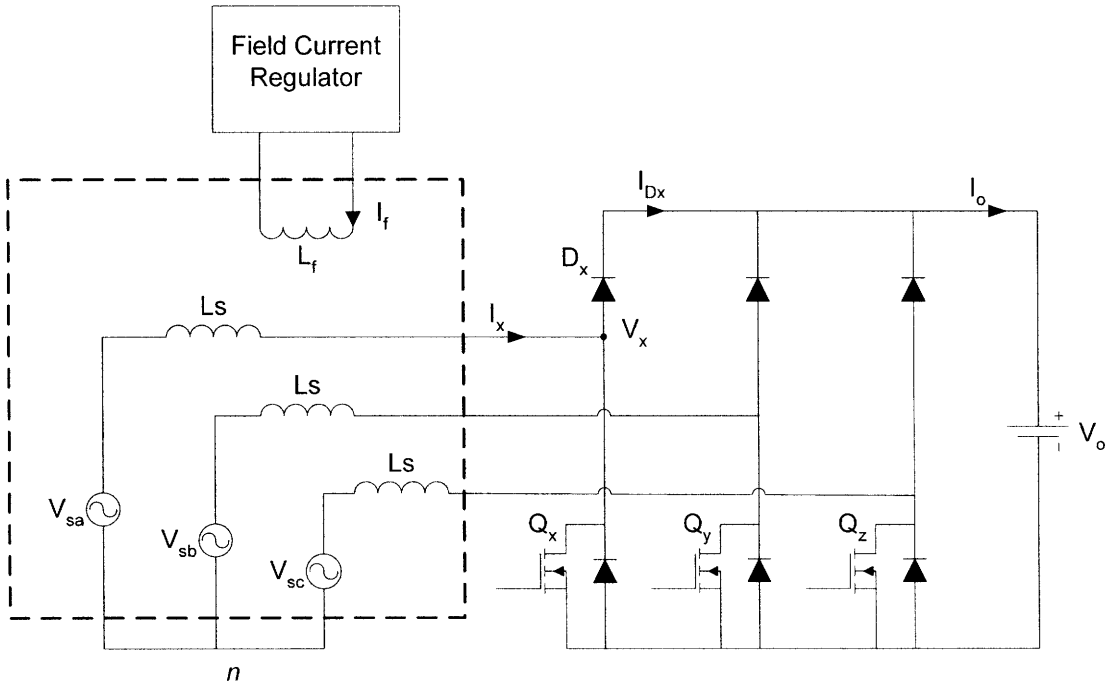

Figure 2.1 Alternator with 3-phase SMR [1]

without being exposed to catastrophic levels of electrical or thermal stress.

2.1.1 MOSFETs

Some of the basic electrical parameters for potential MOSFETs that need to be looked at are breakdown voltage, "on" resistance, gate charge, parasitic input capacitance, junction-to-case thermal impedance, and maximum junction temperature. Ideally the breakdown voltage will be 50% to 100% above the operating voltage seen in the application to provide design margin and overhead to deal with "load dump" transient management. In a 14 V system, the MOSFETs will see approximately 14.5V across drain-to-source under normal operating conditions. A "load dump" transient will cause a voltage spike at the alternator output. The alternator power electronics can be controlled to manage this overvoltage transient with only a very limited device overvoltage of less than 40% (see [10], for example). For this reason, the widely-available class of MOSFETs having a 30 V breakdown voltage specification are well suited for this design. The breakdown voltage should also be limited to 30-40V as higher voltages sacrifice other parameters such as "on" resistance.

Low "on" resistance is another electrical parameter needed to optimize performance. In a low voltage system, any intended output power improvement is implemented in the form of increased current which requires low conduction losses to optimize efficiency and limit thermal stress. In the SMR implementation, the MOSFETs will be switching high peak current (at lower engine operating speeds) as well as acting as a synchronous rectifier throughout the operating range. In both cases, low "on" resistance is needed to minimize conduction losses.

Low gate charge and low parasitic input capacitance are needed to minimize switching losses, for the operating range where high-frequency PWM is used, as well as

Table 2.1: MOSFET descriptions

Manufacturer	PN	V_{ds} (V)	I_d (A)	R_{ds_on} (mΩ)*	$R_{th,jc}$ (°C/W)
IR	IRF2804S	40	75	3.4	0.45
IR	IRF2804S-7P	40	160	2.6	0.5
Fairchild	FDB8860	30	80	3.45	0.43
Fairchild	ISL9N302AS3ST	30	75	3.45	0.49

*** R_{ds_on} rating at 150°C junction temperature**

to minimize stress on the gate driver IC. Low junction-to-case thermal impedance is also needed to minimize the junction temperature of the device. Even with high conversion efficiency, the MOSFETs will dissipate a significant amount of power and it is necessary to keep the junction temperature as low as possible in order to maintain reliability.

A number of MOSFETs from various suppliers were reviewed for possible use. Low "on" resistance was considered the top priority based on previous designs where conduction losses were the primary loss mechanism in the MOSFETs. Based on what was available on the market when this work was initiated, the four MOSFETs in Table 2.1 were chosen for detailed evaluation. It should be noted that all of the MOSFETs in Table 2.1 are rated for 175°C maximum junction temperature and were de-rated to 150°C for all design calculations. The R_{ds_on} value in the table reflects this. The Fairchild PN FDB8860 was found to be unavailable in practice at the time and was scrapped from consideration.

2.1.2 Schottky Diodes

The second power device needed is a Schottky diode. Commercial alternators utilize pin diodes which are very thermally robust but tend to have high forward voltage drops. Schottky diodes have low forward voltage drops which make them ideal for high current

applications. Moreover, the reverse recovery of these devices is negligible, making them well suited to high-frequency switching. The search for surface mount schottky diodes was considerably more difficult than looking for MOSFETs. Only one device that would satisfy the requirements, International Rectifier 112CNQ030A, was found to be available at the time this work was initiated. This particular device is rated up to 110A average current at a forward voltage drop of .39V and with a junction-to-case thermal impedance of .25°C/W. The device junction temperature is only rated up to 150°C and was de-rated to 130°C for all design calculations. Despite the lower temperature rating, this is the only commercial device that provided the necessary power handling capabilities and it was thought that the lower thermal impedance would alleviate some of the concern of junction temperature rise.

2.2 Auxiliary Components

2.2.1 Gate Drivers

A gate driver with low output impedance and high peak current drive capability is needed to optimize the switching performance in the MOSFETs. Ideally a dual totem pole gate driver would be used as it provides dual BJT and MOSFET drives that are capable of sourcing and sinking high peak currents, driving very close to the supply rails, and having low output impedance determined by the parallel combination of the drive transistors. One gate driver that can handle this drive capability is the Texas Instruments UCC27322DGN. The UCC27322DGN is rated at 9A peak drive current which was experimentally verified according to the specification sheet. Also, the driver's peak current capability was tested with 5 V on the output pin. This is significant in that the driver reaches full drive capability during the "plateau" region of a MOSFETs turn-on/off transition.

Good thermal performance is also necessary as the MOSFETs that will be tested require a considerable gate charge to get minimal "on" resistance in the conduction channel of the device. Also, packaging concerns in the final product may make it necessary to eliminate a gate drive resistor meaning that the gate drive losses will be dissipated in the gate driver. The gate drive losses are calculated by

$$P_{gd} = QVf \tag{2.1}$$

where Q is the total gate charge, V is the drive voltage, and f is the switching frequency. For the MOSFETs listed in Table 2.1, nominal gate charge is in the 200nC range at about 15V drive voltage. If the switching frequency is 100KHz, the power dissipation in the gate driver is 300mW.

The UCC27322DGN is available in the MSOP-8 PowerPAD™ package which takes up very little space and has an electrically isolated case that can be connected to the PCB ground plane for heat sinking. This device is available for operation up to 105°C and its datasheet claims a maximum power dissipation of 1.37W at 70°C ambient with a 17.1mW/°C de-rating above 70°C. Nominal ambient temperature in the under-hood environment of the alternator is 85°C which would de-rate the power dissipation capability by about a quarter watt. This leaves plenty of margin for operation at the expected ambient temperature.

2.2.2 Ceramic Capacitors

Capacitors with high current density are also needed for this application. In a boost converter, the output capacitors source current to the load when the MOSFET switch is conducting current and they sink current from the source when the MOSFET is not conducting. Assuming that the boost inductor is large and input ripple current is

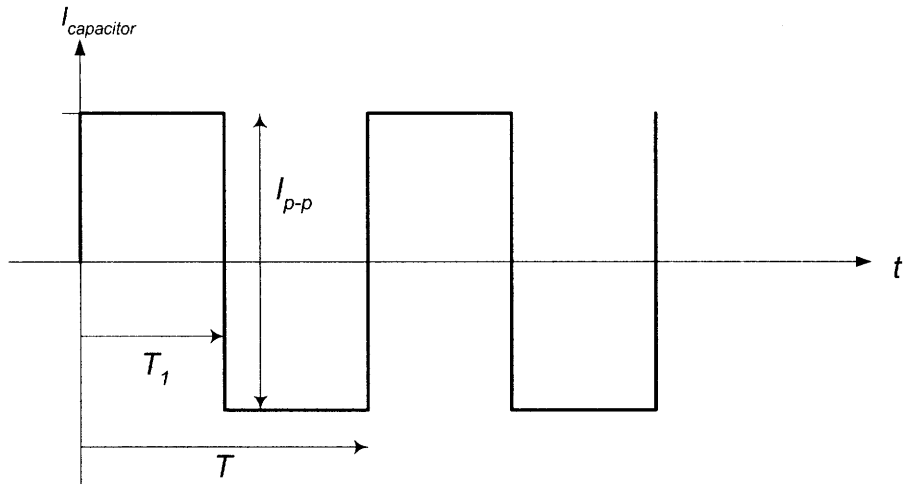

Figure 2.2 Boost output capacitor current waveform

negligible the capacitive current in a boost converter takes the shape of the waveform in figure 2.2.

The RMS current seen by the output capacitors is calculated by the following:

$$I_{RMS} = I_{p-p}\sqrt{d - d^2}; d = \frac{T_1}{T} \tag{2.2}$$

For a boost converter chopping 100A at a 50% duty cycle, the RMS current equates to 50A and it is likely that the SMR would be chopping peak currents in excess of 100A, for close to 50% duty cycle. What is needed is the best current density available in surface mount capacitors. Ceramic capacitors, because of their high Q rating, are the most likely candidate. Datasheets of ceramic capacitors from Murata were examined for voltage rating and RMS current capability. The GRM43ER61C226K ceramic capacitor is commercially available in a standard 1812 package and is rated at 4 A_{rms} capability with a 10°C temperature rise. For the SMR application this was the best available part that satisfied the current density requirements.

2.2.3 Thermal Interface Material

The final component that was needed was an electrical isolation material with high thermal conductivity. In the SMR design, the PCB will be pressed against a heatsink to conduct heat away from the six power devices. The six devices will be operating at four different electrical potentials so it is necessary to provide electrical isolation while maintaining high thermal conductivity. A variety of electrical isolating materials are available from the Bergquist Company. The materials are available in varying thickness and varying degrees of firmness. The thinner materials are referred to as Sil-Pad™ materials. Some of these materials are available in very thin sheets and provide excellent thermal performance with very little applied pressure. The Bergquist Sil-Pad™ 1500ST is a material that is available in 8 mil thickness and is rated as having a thermal impedance of 1.5°C/W for an area equal to a TO-220 device.

2.3 Test Board Specifications

A DC-DC boost converter test circuit, as shown in Figure 2.3, was needed to evaluate the electrical capabilities and thermal transfer characteristics of the 3 MOSFETs and the diode. Based on these test results, one MOSFET would be chosen for use in the three-phase SMR. The test setup requires a DC power supply to drive the input and an output load that could be set to a constant voltage of 14 V and is capable of handling the output

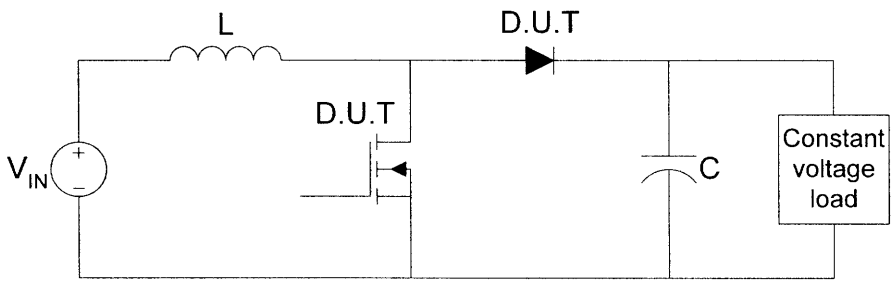

Figure 2.3 Boost converter test circuit

power.

2.3.1 Switching Frequency

Previous work had been put into determining the optimal MOSFET switching frequency for the SMR, and in previous designs [10] the switching frequency was 100 KHz. To remain consistent with the previous effort it was decided that the boost converter would operate at 100 KHz for the initial test run and if the power dissipation due to switching loss was excessive then the switching frequency could be scaled back.

2.3.2 Duty Cycle

Ideally the testing would be performed over a range of duty cycles to measure the relative effects of the switching losses versus the conduction losses. At higher duty cycles it is expected that the conduction losses may dominate and at lower it is expected that the switching losses may dominate. Starting at 50% would give a pretty good indication of what this relation will be between the two and will also serve as an indicator of whether some design changes need to be considered.

2.3.3 Output Power

In the previous design seen in [10] the output power goal of the SMR-based alternator was 1.5 to 2 times that of a commercial alternator. Previous work from [8] had been performed on a commercial alternator that was rated at 12V, 130A or approximately 1.56KW output power. A 1.5 times improvement over the commercial alternator puts the total output power of the SMR at 2.34KW. For the test board we will be working with approximately 1/3 of the capability of the SMR which would put the output power goal at 780W. The boost converter will be driving an HP6050A electronic load set to 14 V in constant voltage operating mode.

Table 2.2: Boost converter test specifications

Parameter	Description	Value
I_{dc}	DC input current	60-120 A
V_o	Output load set voltage	14 V
P_{load}	Power delivered to output load	420-840 W
f_{sw}	MOSFET switching frequency	100 KHz
d	MOSFET switching duty cycle	50%

2.3.4 Input Power

With the output characteristics set to 14 V and 780 W, the output current would be just under 56 A. Given that device testing will be conducted with a converter operating at 50% duty cycle, the input current must be 112 A to test at this output power level. An HP 6011A DC power supply rated for 120 A, 1000 W was available for testing. The input current could also be scaled down to get test data over a range of operating conditions. To summarize, the test specifications listed in Table 2.2 were used to exercise the devices and validate the electrical and thermal modeling.

Chapter 3

3. Thermal Characterization and Modeling

In this chapter the electrical parameters and test specifications are used to approximate the power dissipation in the selected devices. The thermal transfer characteristics of the devices and the PCB are used to calculate the expected temperature rise in the devices and place a specification on the heatsink. A thermal transfer model is created to optimize temperature rise vs. PCB space allocation needed to maintain the devices at a safe operating temperature. The thermal model is also used to design a thermal test circuit board. Testing is conducted with this board and sample devices to validate the accuracy of the model.

3.1 Device Power Dissipation

3.1.1 MOSFET Conduction Loss

In a boost converter MOSFET conduction losses occur when the MOSFET is turned on and the DC input current is shunted directly to ground. Power is dissipated as the input current flows across a small resistance in the MOSFET's conduction channel. The total power dissipation due to conduction loss is calculated by

$$P_{cond} = I_{RMS}^2 * R_{DS\_ON} = I_{DC}^2 * d * R_{DS\_ON} \tag{3.1}$$

where R_{DS_ON} is the temperature dependent resistance in the conduction channel of the MOSFET and d is the switching duty ratio. Each MOSFET's datasheet specifies a maximum value of R_{DS_ON} at 25°C and a normalized multiplier for R_{DS_ON} vs. junction temperature. The calculated values of R_{DS_ON} at the maximum junction temperature of 150°C are listed in Table 2.1 for each MOSFET under consideration. Based on these values of R_{DS_ON} the maximum power dissipation due to conduction loss for any MOSFET under consideration is about 25 W at 120 A_{DC} input current.

3.1.2 MOSFET Switching Loss

Switching loss is frequency dependent power dissipation that occurs during the turn-on and turn-off transitions of the MOSFET. Power is dissipated in the device as both current and voltage are transitioning from one state to another. For a brief time T during these transitions there is simultaneous current through and voltage across the device. Analytically the power dissipation due to switching loss is calculated by

$$P_{sw} = f_{sw} \int_0^T V_{pk} I_{pk} dt \tag{3.2}$$

where f_{sw} is the MOSFET switching frequency, and V_{pk}, I_{pk} are the peak voltage and current simultaneously in the device. Although a simple analytical expression, switching loss is difficult to accurately calculate because it is highly dependent on the parasitic input capacitance which is a nonlinear parameter. Also the switching behavior can be affected by unknown or poorly defined parameters such as PCB trace inductance and parasitic lead inductance.

A MATLAB program was developed in [4] to model the switching behavior of MOSFETs in the boost topology. The program utilizes curve fitting expressions for the nonlinear capacitances to try and accurately calculate the turn-on and turn-off transition time in the devices. Unknown parameters can be obtained experimentally or extracted from PSPICE simulation models and input into the program. The MATLAB program calculates the total switching loss at a given switching frequency. Running the program at a couple of different operating frequencies generates a series of points which can be added to the conduction losses and plotted to show the total power dissipation as a function of the switching frequency. As is shown in Figure 3.1 the maximum power dissipation approaches 50 W at 100 KHz switching frequency.

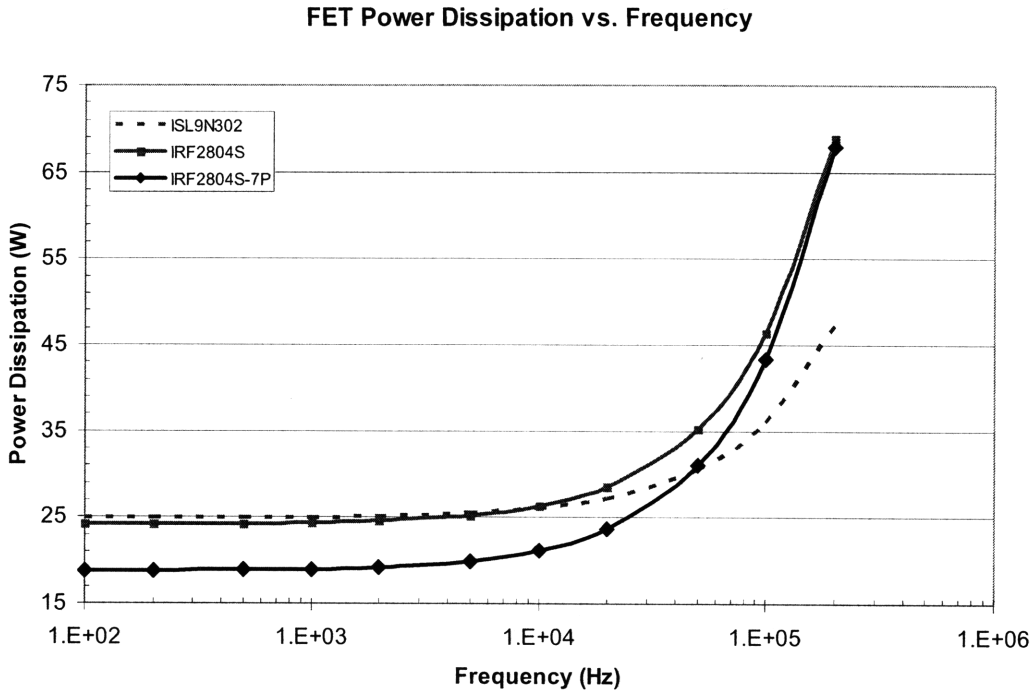

Figure 3.1 MOSFET Power Dissipation

3.1.3 Diode Conduction Loss

In a boost converter, conduction losses occur in the diode when the MOSFET switch is turned off and the DC input current is delivered directly to the output through the diode. Power is dissipated in the device due to the average current through the device and the forward voltage drop needed to carry the instantaneous forward current. The expression for diode conduction loss averaged over a complete PWM period is

$$P_{diode} = V_d * I_{AVG} = V_d * I_{DC} * (1 - d) \tag{3.3}$$

where V_d is the forward voltage drop across the diode, I_{DC} is the instantaneous forward current, and d is the switching duty cycle. The specification sheet for the 112CNQ030ASL diode plots the average power loss vs. average forward current as well as the instantaneous forward current vs. forward voltage drop. Either plot can be used to approximate the diode power dissipation at the different DC input currents. Based on the

Table 3.1: Estimated diode power dissipation

I_{dc} (A)	V_f (V)	P_{diode} (W)
120	0.43	26
100	0.41	20.5
80	0.4	16
60	0.4	12

data from the specification sheet, Table 3.1 was generated to be used as a guideline for the diode power dissipation during testing.

Based on the estimated total power dissipation and the junction-to-case thermal impedances (R_{thJC}) of the devices, a limit is placed on the maximum case temperature of each device. A preliminary PCB design can be generated to calculate what heatsink-to-ambient thermal impedance is needed to maintain the devices at or below that maximum case temperature.

3.2 PCB Thermal Design

3.2.1 Thermal Vias

The use of thermal vias is a common industry technique for limiting the temperature rise in surface mount devices. Thermal vias lie within the dimensions of the solder pad, directly underneath the case of surface mount devices. They electrically connect the top layer solder pad to a bottom layer solder pad providing a thermally efficient path through the PCB. The bottom layer solder pad can then be pressed against a heatsink to further conduct heat away from the device.

The vias are laid out such that there is as much conduction (copper) area as possible connecting the top and bottom solder pads below the device. The total copper conduction area of one via is determined by the copper plating thickness T_{CU} of the via and the hole diameter d of the via.

$$A_{CU} = \pi(T_{CU} + d)T_{CU} \tag{3.4}$$

Given the conduction area of the via and the thermal resistivity ρ of copper, the thermal impedance of a single via can be calculated by

$$R_{th,via} = \frac{\rho * l}{A_{CU}}; \rho \approx 98\frac{mil-^{\circ}C}{W} \tag{3.5}$$

where l is the length of a via or thickness of the PCB. The PCB thickness and drill diameter capability are parameters that were obtained directly from the PCB manufacturer. The plating thickness was assumed to be equal to the copper trace thickness.

3.2.2 MOSFET Layout

The MOSFET design is considered first since it has the tighter design constraints of the two power devices. The thermal design considerations are as follows:

1. The estimated power dissipation is up to 50W
2. $R_{thJC,FET}$ can be as high as .5°C/W
3. $T_{J,MAX} = 150^{\circ}C$
4. The D^2-PAK surface mount package is approximately equal in size to a standard T0-220 package hence the Sil-Pad™ thermal impedance $R_{th,sil-pad} = 1.5\frac{^{\circ}C}{W}$

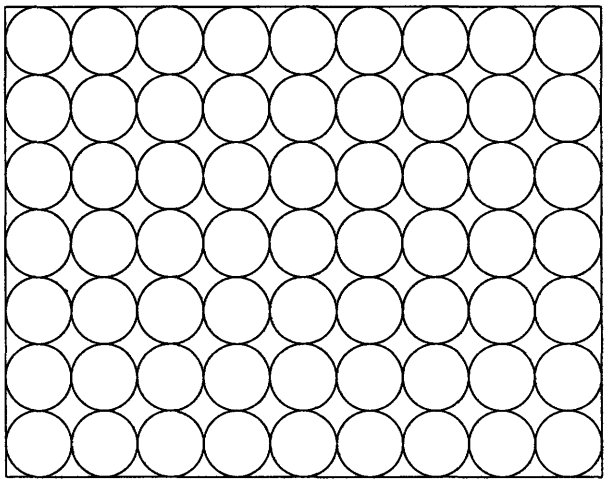

Figure 3.2 Via layout pattern

EagleCAD software was used to layout a pattern of vias underneath the solder pad area of the D^2-PAK. The initial pattern that was laid out is shown in Figure 3.2. This pattern allowed for 63 vias with a hole diameter of 23 mil and a pitch of 50 mil to be drilled within the outline of the D^2-PAK.

Using equations 3.4 and 3.5 and assuming the plating thickness to be equivalent to the trace thickness of $3oz/ft^2$ copper, the calculation for the MOSFET case-to-sink thermal impedance $R_{thCS,FET}$ is carried out as follows

$$A_{CU} = \pi(T_{CU} + d)T_{CU}$$
$$A_{CU} = \pi * (4mil + 23mil) * 4mil = 339.3mil^2$$
$$R_{th,via} = \frac{\rho * l}{nA_{CU}}; n = 63$$
$$R_{th,via} = \frac{98\frac{mil-^\circ C}{W} * 62mil}{63 * 339.3mil^2} = .284\frac{^\circ C}{W}$$
$$R_{thCS,FET} = R_{th,via} + R_{th,sil-pad} = .284\frac{^\circ C}{W} + 1.5\frac{^\circ C}{W}$$
$$\Rightarrow R_{thCS,FET} = 1.784\frac{^\circ C}{W}$$

The case-to-sink thermal impedance from this layout design places the following constraint on the heatsink

$$T_{SINK,MAX} = T_{J,MAX} - P_{FET} * (R_{thJC,FET} + R_{thCS,FET})$$
$$T_{SINK,MAX} = 150^\circ C - 50W * (.5\frac{^\circ C}{W} + 1.784\frac{^\circ C}{W})$$
$$\Rightarrow T_{SINK,MAX} = 35.8^\circ C$$
$$\Rightarrow R_{th,sa} = \frac{T_{SINK,MAX} - T_{ambient}}{P_{FET} + P_{DIODE}} = \frac{35.8^\circ C - 25^\circ C}{76W} \approx .142\frac{^\circ C}{W}$$

For a test board running at 25°C ambient, the $R_{th,sa}$ spec of $.142\frac{^{\circ}C}{W}$ is very difficult to meet with commercial off-the-shelf parts and would leave no overhead margin.

A new design that reduces the case-to-sink thermal impedance needs to be explored. The previous calculations showed that the case-to-sink thermal impedance was dominated by the Sil-Pad™ thermal impedance and not the via layout. Therefore the thermal via layout, while not fully optimized, will suffice.

3.2.3 Heat Spreader Design

A heat spreader is a slab of copper, surrounding the device, which conducts heat away from the device and effectively increases the total area conducting heat down through the board. This is an effective method of decreasing the case-to-sink thermal impedance because it will decrease the thermal impedance through the board and, more importantly, increase the contact area between the Sil-Pad™ and the heatsink. The heat spreader is implemented by expanding the solder pad area of the surface mount package and placing vias all through the expanded area. Copper foil is then soldered on to the areas not covered by the D^2-PAK.

A MATLAB model is developed to approximate the behavior of the heat spreader as a function of the length of the heat spreader for a given foil thickness. The model is

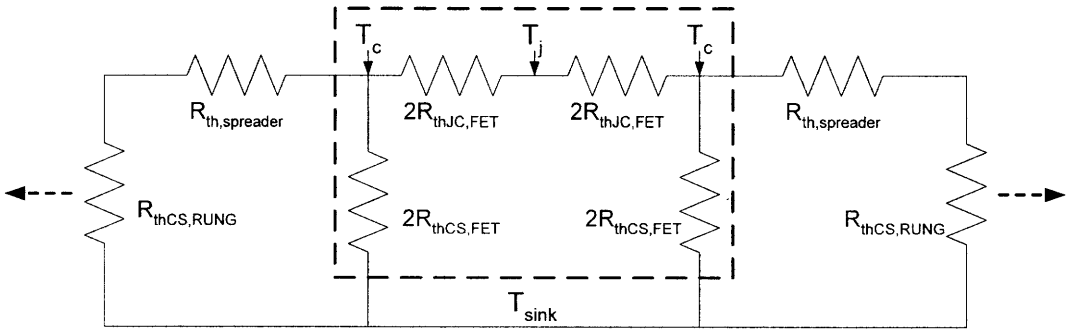

Figure 3.3 Heat spreader ladder network

based on a resistor ladder network as shown in Figure 3.3. For the sake of simplicity it is assumed that heat is conducted away from the device laterally and all area not immediately lateral to the device is ignored. The center point of the ladder is the device junction and the area enclosed by the dashed lines is the total junction-to-heatsink thermal impedance if there was no heat spreader. The case-to-sink thermal impedance of each ladder "rung" $R_{thCS,RUNG}$ is the thermal impedance through the PCB of one row of seven vias plus the thermal impedance of Sil-Pad™ area underneath that row. In this case, each additional row of vias is approximately $1/9^{th}$ the total area of the D^2-PAK. The spreading resistance $R_{th,spreader}$ is the thermal impedance along the copper foil between each "rung" in the ladder. Figure 3.3 is shown with only one "rung" per side of the device but the idea is to continue adding rungs to the ladder until the total MOSFET case-to-sink thermal impedance asymptotically approaches the point of diminishing returns.

Equations 3.4 and 3.5 can be manipulated to calculate the thermal impedances needed for the model;

$$A_{CU} = w * h \tag{3.6}$$

where w represents the width of each rung and h represents the combined thickness of the top layer copper trace and the copper foil. The spreading resistance is

$$R_{th,spread} = \frac{\rho * l}{A_{CU}}; \rho \approx 98 \frac{mil - ^{\circ}C}{W} \tag{3.7}$$

where l is the pitch between rows. Assuming that each rung is seven vias or 350mil wide and the combined thickness of the foil and trace is two $4oz/ft^2$ pieces of copper, the necessary parameters needed for the model can be calculated from equations 3.4-3.7.

$$R_{thCS,RUNG} = R_{th,via} + \left(9 * R_{th,sil-pad}\right)$$

$$R_{thCS,RUNG} = \frac{\rho * l}{nA_{CU}} + \left(9 * 1.5\frac{^{\circ}C}{W}\right); n = 7, l = 62mil$$

$$R_{thCS,RUNG} = \frac{98\frac{mil-^{\circ}C}{W} * 62mil}{7 * 339.3mil^2} + 13.5\frac{^{\circ}C}{W}$$

$$\Rightarrow R_{thCS,RUNG} = 16.06\frac{^{\circ}C}{W}$$

$$R_{th,spread} = \frac{\rho * l}{w * h}; l = 50mil, w = 350mil, h = 10.8mil$$

$$\Rightarrow R_{th,spread} = 1.3\frac{^{\circ}C}{W}$$

These parameters are input into the MATLAB model and used to calculate the effective MOSFET case-to-sink thermal impedance $R_{thCS,FET}$ as a function of the length of the spreader. The model produced the plot presented in Figure 3.4.

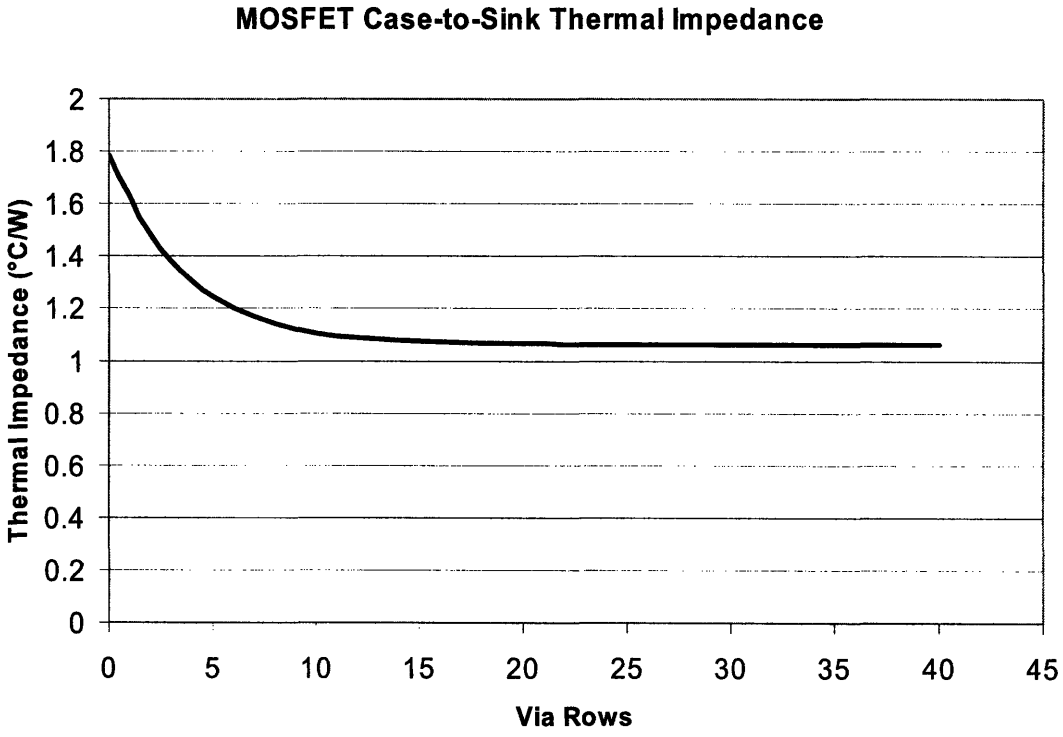

Figure 3.4 MOSFET Heat spreader model results

Around the point of 16-18 total rungs or 8-9 per side of the device, the heat spreader asymptotically approaches the point of diminishing returns where continuing to increase the area produces little improvement. The curve can be rerun at varying foil thickness to see if this always holds true but for the purposes of the test board this may be sufficient to move forward. A quick recalculation of the heatsink specification yields the following results:

$$T_{SINK,MAX} = T_{J,MAX} - P_{FET} * (R_{thJC,FET} + R_{thCS,FET})$$

$$T_{SINK,MAX} = 150^{\circ}C - 50W * (.5\frac{^{\circ}C}{W} + 1.06\frac{^{\circ}C}{W})$$

$$\Rightarrow T_{SINK,MAX} = 72^{\circ}C$$

$$R_{th,sa} = \frac{T_{SINK,MAX} - T_{ambient}}{P_{FET} + P_{DIODE}} = \frac{72^{\circ}C - 25^{\circ}C}{50W + 26W} = R_{th,sa} \approx .62\frac{^{\circ}C}{W}$$

A heatsink thermal impedance of $R_{th,sa} = .62$ is a more reasonable specification and a test board can be built to this specification and tested at 25°C ambient to verify the accuracy of the heat spreader model.

3.2.4 Diode Layout

The thermal design for the 112CNQ030 schottky diode will have greater overhead margin than the MOSFET because the diode is a larger device with lower junction-to-case thermal impedance and the expected power dissipation is lower. The relevant design considerations for the diode are

1. The estimated power dissipation is up to 26W.
2. $R_{thJC,DIODE} = .25\frac{^{\circ}C}{W}$
3. $T_{J,MAX} = 130^{\circ}C$
4. The D61-8-ASL surface mount package is approximately twice the size of a standard T0-220 package hence the Sil-Pad™ $R_{th,sil-pad} = .75\frac{^{\circ}C}{W}$

The diode layout incorporated the same via spacing pattern as was used for the MOSFET. In total, 119 vias of 23mil diameter were placed within the outline of the D61-8-ASL package. Following the same design equations that were used for the MOSFET, the diode's case-to-sink thermal impedance $R_{thCS,DIODE}$ is calculated from the following:

$$A_{CU} = \pi(T_{CU} + d)T_{CU}$$

$$A_{CU} = \pi * (4mil + 23mil) * 4mil = 339.3mil^2$$

$$R_{th,via} = \frac{\rho * l}{nA_{CU}}; n = 119$$

$$R_{th,via} = \frac{98\frac{mil-^\circ C}{W} * 62mil}{119 * 339.3mil^2} = .15\frac{^\circ C}{W}$$

$$R_{thCS,DIODE} = R_{th,via} + R_{th,sil-pad} = .15\frac{^\circ C}{W} + .75\frac{^\circ C}{W}$$

$$\Rightarrow R_{thCS,DIODE} = .9\frac{^\circ C}{W}$$

$$T_{SINK,MAX} = T_{J,MAX} - P_{DIODE} * (R_{thJC,DIODE} + R_{thCS,DIODE})$$

$$T_{SINK,MAX} = 130^\circ C - 26W * (.25\frac{^\circ C}{W} + .9\frac{^\circ C}{W})$$

$$\Rightarrow T_{SINK,MAX} = 100^\circ C$$

$$R_{th,sa} = \frac{T_{SINK,MAX} - T_{ambient}}{P_{FET} + P_{DIODE}} = \frac{100^\circ C - 25^\circ C}{50W + 26W}$$

$$\Rightarrow R_{th,sa} \approx 1\frac{^\circ C}{W}$$

As expected the larger device and lower power dissipation allowed for sufficient copper area to be place within the outline of the D61-8-ASL package and a heat spreader was not needed. Also the diode allows for greater margin on the heatsink so the restrictions imposed by the MOSFET will be used to select an appropriate heatsink for the test board.

3.2.5 Heatsink Selection

The final aspect of the thermal design is the selection of an off-the-shelf aluminum extrusion that satisfies the $R_{th,sa} \leq .62°C/W$ specification. Wakefield Thermal Solutions offers a variety of high fin density aluminum extrusions that are available in 7.4"x 12" size which is large enough for the test PCB. Part number 510-12U is a stock extrusion that is rated at $R_{th,sa} = .24°C/W$ with a 50°C temperature rise. The lower thermal impedance will allow for the devices to operate at less than the maximum junction temperature providing overhead margin and more reliability.

3.3 Test Board Design Verification

3.3.1 Design Objective

The objective of the test board was to validate the electrical capabilities of the devices, the thermal efficiency of the PCB, and the accuracy of the heat spreader model. The test specifications that were developed in Chapter 2 are recalled in Table 3.2

There are four different operating points that will be controlled by a constant current DC power supply. The output will be driving a constant voltage load set for 14 V. At each operating current the circuit will run continuously until the devices reach thermal steady state.

Table 3.2: Boost converter test specifications

Parameter	Description	Value
I_{dc}	DC input current	60-120 A
V_o	Output load set voltage	14 V
P_{load}	Power delivered to output load	420-840 W
f_{sw}	MOSFET switching frequency	100 KHz
d	MOSFET switching duty cycle	50%

3.3.2 Test Methodology

A test methodology was developed to take all measurements and calculate the necessary

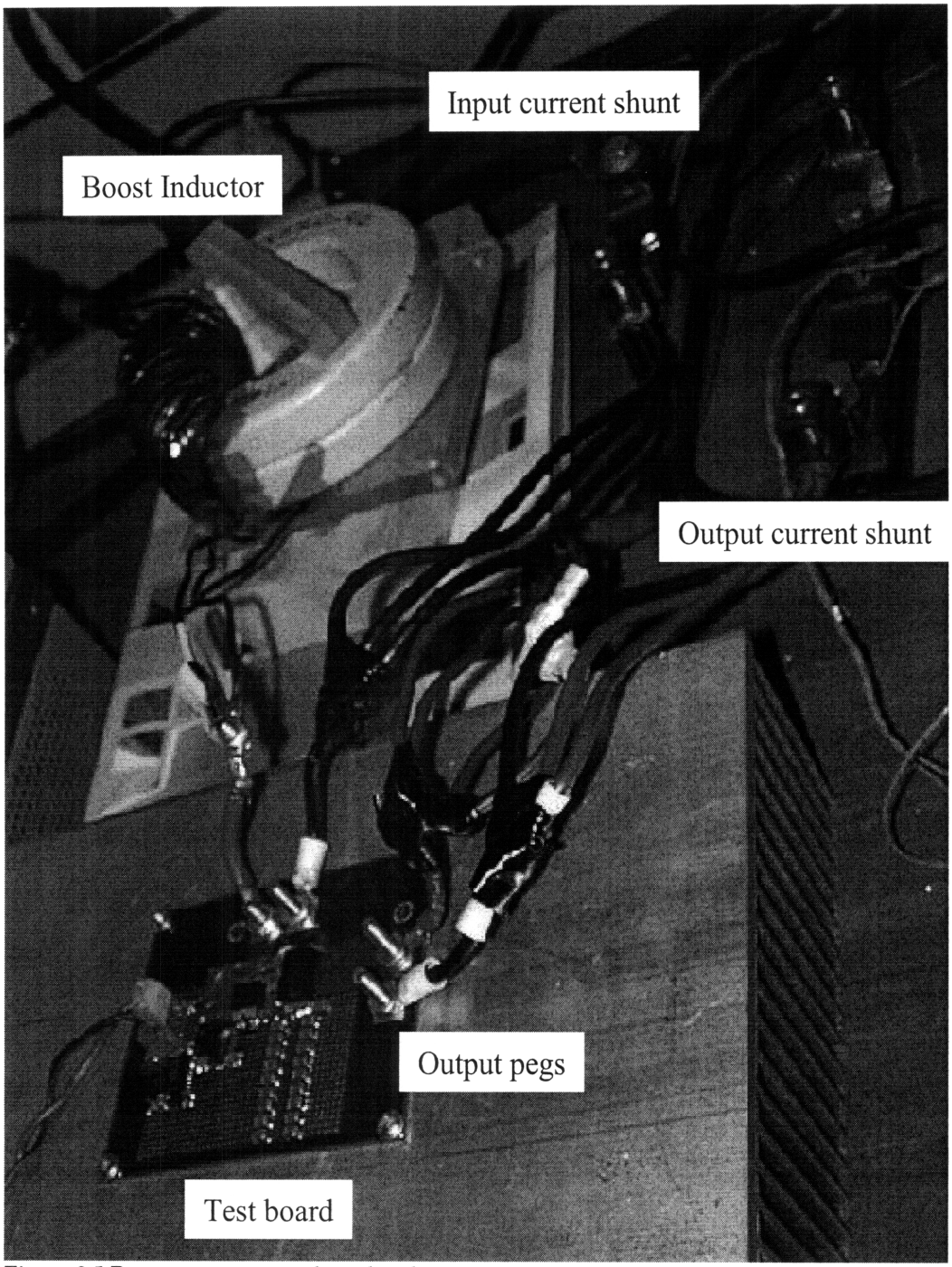

Figure 3.5 Boost converter test board and test setup

performance characteristics of the converter. A picture of the test setup is shown in Figure 3.5. A schematic of the test circuit is available in Appendix A.1.

1. All voltage measurements were made with a Fluke 87III DMM.
2. A 200 A (4A/mV) current shunt is connected on the input line of the converter. The voltage across the shunt is measured to verify DC input current.
3. The DC input voltage with respect to ground is measured directly at the input of the boost inductor.
4. A 100 A (2A/mV) current shunt is connected on the output line of the converter. The voltage across the shunt is measured to verify DC output current.
5. The DC output voltage with respect to ground is measured directly across the output pegs of the test board.
6. The total input power and output power are calculated. The output power is subtracted from the input power with the result representing total power dissipation in the boost converter test circuit.
7. The DC voltage drop across the boost inductor is measured.
8. The boost inductor power dissipation is calculated and subtracted from the total power dissipation with the result representing power dissipation in the two test devices
9. The MOSFET drain voltage with respect to ground is measured while the MOSFET switch is on. The voltage across drain-source is divided by the DC input current to calculate R_{DS_ON}.
10. A K-type thermocouple is used to measure the case temperatures of the MOSFET and diode and the heat sink temperature.

Based on this set of measurements all of the relevant performance characteristics of the devices and PCB can be calculated. Step 8 calculated the device power dissipation and efficiency for each MOSFET-diode pair. Table 3.1 estimated the total diode power dissipation based on data provided in the specification sheet. The remaining device power dissipation is attributed to the MOSFET. Step 9 in the test methodology calculated the MOSFET conduction loss. The remaining MOSFET power dissipation was attributed to switching loss. The individual device dissipation was used in combination with the case temperature and heatsink temperature to determine the case-to-sink thermal impedance of each device. The accuracy of the MOSFET heat spreader model can be validated based on the calculated case-to-sink thermal impedance.

Table 3.3: ISL9N302 – 112CNQ030ASL Test Results

I_{DC} (A)	P_{MOSFET} (W)	P_{diode} (W)	Efficiency	$T_{c,MOSFET}$	$T_{c,diode}$	T_{SINK}	$R_{thCS,diode}$	$R_{thCS,MOSFET}$
60	11.10	12	94.91%	52.7°C	53.1°C	35.4°C	1.48 °C/W	1.56 °C/W
80	23.54	16	93.63%	67.8°C	71°C	40°C	1.94 °C/W	1.18 °C/W
100	35.19	20.5	93.03%	83.6°C	96.5°C	46.5°C	2.44 °C/W	1.05 °C/W
120	Device Failure - No data recorded							

Table 3.4: IRF2804S – 112CNQ030ASL Test Results

I_{DC} (A)	P_{MOSFET} (W)	P_{diode} (W)	Efficiency	$T_{c,MOSFET}$	$T_{c,diode}$	T_{SINK}	$R_{thCS,diode}$	$R_{thCS,MOSFET}$
60	10.89	12	94.93%	47.05°C	46.9°C	34.1°C	1.07 °C/W	1.18 °C/W
80	18.02	16	94.46%	61.75°C	56.25°C	41.8°C	0.90 °C/W	1.11 °C/W
100	27.32	20.5	93.92%	74.1°C	70.4°C	49.45°C	1.02 °C/W	0.90 °C/W
120	41.84	26	92.98%	97.35°C	87.3°C	55.05°C	1.24 °C/W	1.01 °C/W

Table 3.5: IRF2804S-7P – 112CNQ030ASL Test Results

I_{DC} (A)	P_{MOSFET} (W)	P_{diode} (W)	Efficiency	$T_{c,MOSFET}$	$T_{c,diode}$	T_{SINK}	$R_{thCS,diode}$	$R_{thCS,MOSFET}$
60	8.81	12	95.38%	52.8°C	45.4°C	37°C	0.7 °C/W	1.79 °C/W
80	14.08	16	95.10%	65.1°C	59.1°C	47°C	0.76 °C/W	1.29 °C/W
100	20.58	20.5	94.79%	76.1°C	68.7°C	53.1°C	0.76 °C/W	1.12 °C/W
120	31.14	26	94.11%	90.2°C	80.7°C	57.5°C	0.89 °C/W	1.05 °C/W

3.3.3 Test Results

Each device combo was tested at least twice with the test methodology presented in 3.3.2. The averaged results of the two test runs for the ISL9N302 – 112CNQ030ASL combo are shown Table 3.3. To summarize the test data, the Fairchild IRSLN93N was eliminated from consideration because it showed higher power dissipation when operating at lower input currents and in both test runs a device failure occurred at the 120 A_{DC} input. In the first instance the diode and MOSFET failed, so a second test board was constructed with two new devices. In this instance the MOSFET failed again. The reason for the failures was never fully explored as multiple failures and inefficient operation were enough to remove the device from consideration.

Both International rectifier MOSFETs completed successful runs at all operating points. The averaged results for the IRF2804S and IRF2804S-7P device combos are shown in Tables 3.4 and 3.5 respectively. The IRF2804S operated with less efficiency than the IRF2804S-7P particularly at the higher current levels. This would appear to indicate that the lower R_{DS_ON} of the IRF2804-7P makes for a more efficient device. For completeness, a third test run was taken for each of these devices using same board as in the previous two runs. In this 3rd test run the IRF2804S-7P again operated successfully but the IRF2804S failed at the 120 A_{DC} input. Though it did not appear that the junction temperature of the IRF2804S approached a catastrophic level during the previous two test runs, the combination of solder reflow and high temperature operation could have caused enough degradation in the device to cause the failure.

3.4 Single Device Testing

The test board results showed that the International Rectifier IRF2804S-7P MOSFET was the best of the candidate devices for this application. It operated more efficiently and was the only device not to fail during a test run. In fact, this device performed better than the model developed in [4] had predicted so further testing was conducted. A new test board with the selected devices was produced to run a final electrical test and to run a set of single device thermal validation tests.

3.4.1 Final Electrical Validation

Table 3.6: IRF2804S-7P Power Dissipation Data

I_{DC} (A)	P_{MOSFET} (W)	R_{DS_ON} (mΩ)	P_{COND} (W)	P_{SW} (W)	$T_{c,MOSFET}$ (°C)	T_{SINK} (°C)	$R_{thCS,MOSFET}$ (°C/W)
60	9.02	1.69	3.04	5.98	53.5	36.6	1.87
80	14.55	1.82	5.81	8.74	66.3	48.4	1.23
100	21.68	1.96	9.80	11.88	75.6	52.9	1.05
120	31.27	2.16	15.52	15.75	90.1	60.4	0.95

The main focus of the final electrical validation was to derive a better estimation of the switching losses in the IRF2804S-7P MOSFET. The new test board was run under the same operating conditions as the previous board and the numbers were compared with the average of the first three test runs to verify that there was no unreasonable deviation between the two devices. Table 3.6 compiled the MOSFET dissipation numbers including the R_{DS_ON} measurement.

Based on the numbers in Table 3.6, a plot of the switching losses vs. peak switching current is generated and a curve fitting expression is used to accurately model the switching loss. The generated plot with the curve fitting line is presented in Figure 3.6. The curve fitting expression is

$$P_{sw} = .169 * I_{pk} - 4.8 . \tag{3.8}$$

This expression is used later to estimate the switching loss in the SMR as a function of

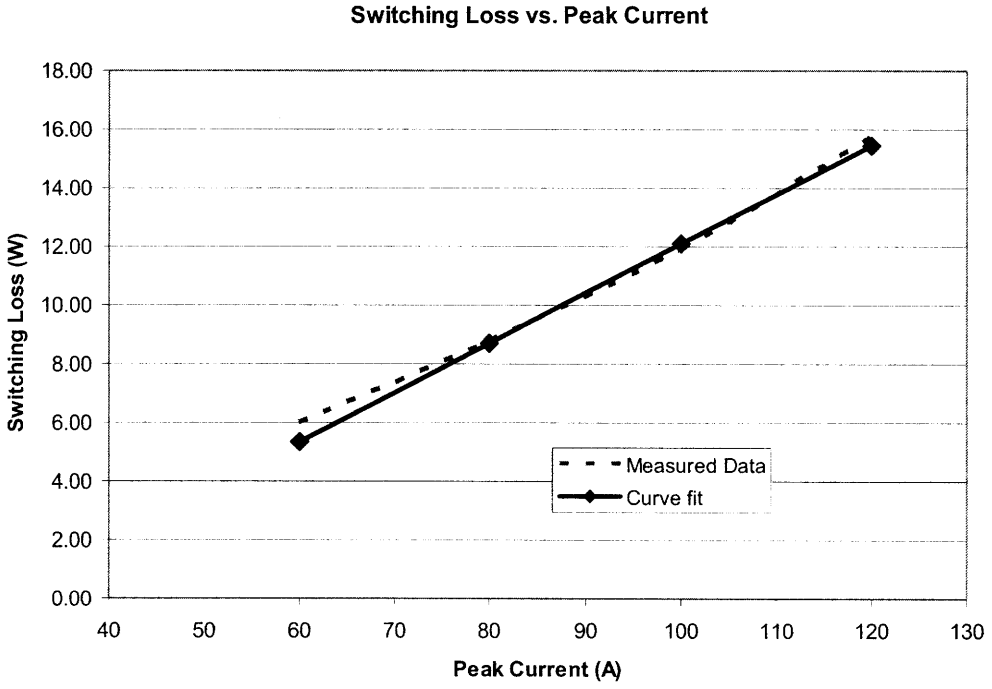

Figure 3.6 MOSFET switching loss measurement with curve fit

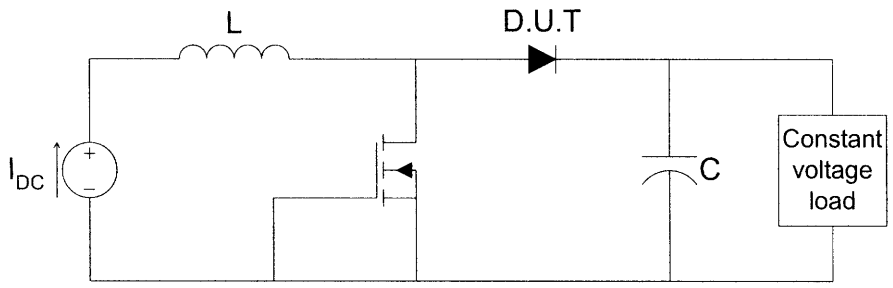

Figure 3.7 Diode thermal test setup

the peak phase current.

3.4.2 Thermal Testing

The variation in thermal impedance at the different operating points prompted the desire to perform single device thermal testing with a controlled test setup. Using the boost test board, each device can be individually tested with a fixed DC current. The diode can be individually tested by using the setup shown in Figure 3.7.

The MOSFET in the boost circuit is tied to ground to ensure that the gate is not enhanced and negligible current flows through that device. The constant voltage load is set to 1 V and the input power supply drives a fixed DC current through the diode. The Fluke 87III DMM is used to take three measurements; the DC current through the output shunt, the diode anode voltage, and the diode cathode voltage. A thermocouple is used to measure the diode case temperature and the heatsink temperature. The data from this test is shown in Table 3.7 and the relevant $R_{thCS,DIODE}$ calculation is carried out as follows

$$P_{diode} = (V_{ANODE} - V_{CATHODE}) * I_{DC}$$
$$R_{thCS,DIODE} = \frac{(T_{c,diode} - T_{SINK})}{P_{diode}}$$

A similar test setup is developed for the MOSFET. The polarity on the input supply is reversed and the DC current is driven into the MOSFET's body diode. A DC

Table 3.8: Diode Thermal Test Data

I_{DC} (A)	V_{ANODE} (V)	$V_{CATHODE}$ (V)	P_{diode} (W)	$T_{c,diode}$ (°C)	T_{SINK} (°C)	$R_{thCS,diode}$ (°C/W)
30	1.621	1.274	10.41	36.7	27.9	0.845
50	1.88	1.524	17.8	47.4	32.2	0.854
70	2.03	1.671	25.13	60.3	39	0.848

supply is used to reverse bias the schottky diode to ensure that no current conducts through that device. Figure 3.8 shows this test setup.

Again, a set of measurements is taken with a DMM and thermocouple to calculate the power dissipation in the device and the thermal impedance through the PCB. This data is compiled into Table 3.8. The diode test data revealed an average $R_{thCS,DIODE}$ of about .85°C/W and the MOSFET test data revealed an average $R_{thCS,FET}$ of about .965°C/W. Both of these numbers are within 6% of the expected value so it stands to reason that the PCB's thermal capability is consistent with theory.

Table 3.7: MOSFET Thermal Test Data

I_{DC} (A)	V_{SOURCE} (V)	V_{DRAIN} (V)	P_{MOSFET} (W)	$T_{c,MOSFET}$ (°C)	T_{SINK} (°C)	$R_{thCS,MOSFET}$ (°C/W)
16	0.769	0.0573	11.3872	38.4	27.6	0.948
32	0.808	0.1014	22.6112	53.6	31.7	0.969
40	0.845	0.146	27.96	59.5	33	0.948
57	0.898	0.209	39.273	71.9	35.6	0.924
70	0.942	0.266	47.32	92.5	43.7	1.031

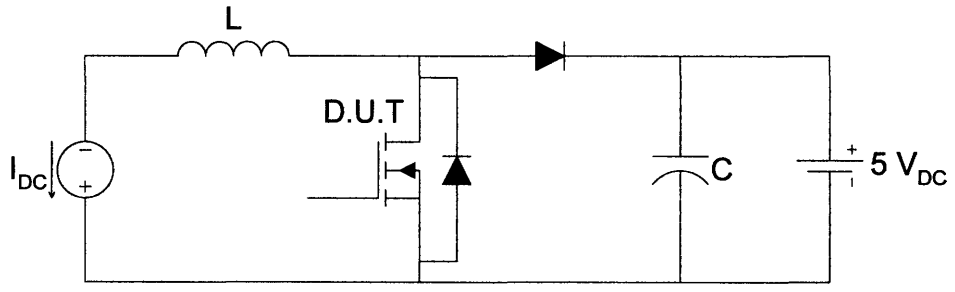

Figure 3.8 MOSFET thermal test setup

Chapter 4

4. Alternator Characterization and Modeling

In this chapter a commercial alternator is experimentally characterized in order to quantify the important electromechanical parameters such as full field current, machine constant, synchronous inductance, stator winding resistance, and output power capability. Equations for modeling the alternator are introduced and the parameter values for the model are selected. A plot is generated to compare the analytical model with experimental results and a best fit curve is achieved.

4.1 Alternator Characterization

4.1.1 Objective

The objective is to select a commercial alternator and run the machine in a controlled test environment to determine its performance capabilities and quantify certain parameters that will be used to develop a computational model of the machine. Ultimately, the stator will be rewound with less turns in the core so as to achieve more efficient utilization of the mechanical input power by operating in a load-matched condition and reducing the machine's largest source of power dissipation. The rewinding ratio (or winding ratio [12]) will be a fraction of the current number of turns selected to obtain optimal power with minimal device stress. The following parameters were needed to develop a model to predict the behavior of the alternator.

1. Nominal full field current
2. Output power vs. operating speed
3. Machine constant, k
4. Synchronous inductance
5. Winding resistance

The alternator purchased for characterization was a Remy part number 92319. A specification sheet provided by the manufacturer detailed the output current of the alternator into a 13V load over the operating range of 1600 to 6000 RPM with a 14.5V voltage regulator set point. The specification sheet claimed a maximum output power of

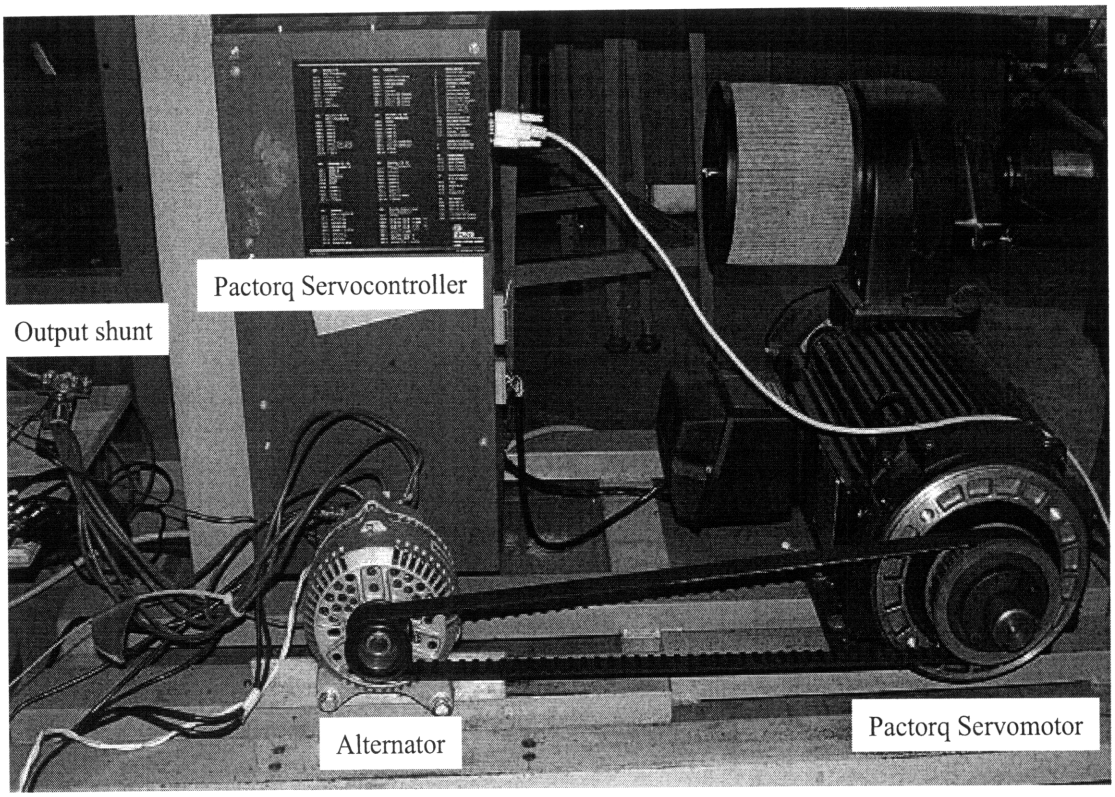

Figure 4.1 Alternator test setup

1818W and a full load capability of 159A. A test setup was implemented to verify these measurements.

4.1.2 Test Setup

The alternator test setup, similar to those used in [1, 3, 5, 8, 10, 12], is shown in Figure 4.1. A Pacific Scientific Pactorq servomotor with a motor to alternator gear ratio of 2.14:1 is used to drive the machine. The servomotor is controlled by a Pacific Scientific SC750 servo controller. A 200 A (4A / mV) current shunt is connected on the output line of the alternator and the output peg is instrumented for a voltage measurement. This is used to measure the output power characteristics. The current return line is bolted directly on to the case of the alternator. The alternator feeds an electronic load (Transistor Devices Dynaload model DLVP 50-300-3000A), set to constant voltage operation at 13 V. Finally, a Hewlett-Packard HP6011A DC power supply is used to

back feed the voltage regulator so that the field current can be controlled (at either constant voltage or constant current) directly by the power supply rather than the regulator.

4.1.3 Field Current

In the manufacturer's test specification and under normal alternator operation, the field current is controlled by the regulator circuit shown in Figure 4.2. Pin A is the regulation point typically set at 14.4V while Pin F is held open. The regulator controls the field excitation current by modulating the switch at some duty ratio *d*. When the switch is closed, excitation current slowly energizes the field winding. When the switch opens, V_F pulls up to a diode drop above V_A and the winding current commutates through the diode.

$$i_f = \frac{V_A - \langle V_F \rangle}{R_f} = \frac{d * V_A}{R_f} \tag{4.1}$$

Full field is defined as the operating point where the duty cycle equals one and the

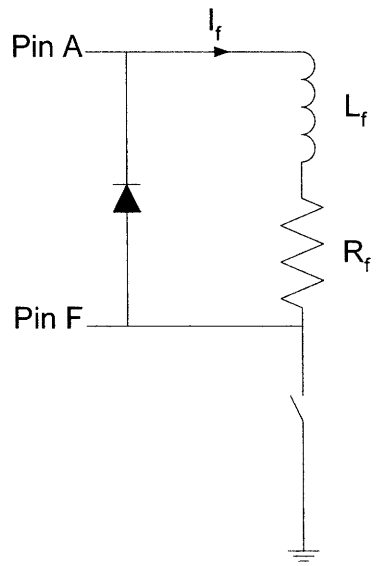

Figure 4.2 Voltage regulator circuit

excitation current settles to a value equal to $\frac{V_A}{R_f}$. Because the winding resistance is temperature dependent and because the charging time constant of the field winding is long, it can take a long time for the field to settle at full excitation.

Connecting a DC power supply across Pins A and F bypasses the regulator switch and allows the regulator circuit to behave as if the duty cycle were equal to one. The power supply voltage can then be set to the nominal regulation voltage of 14.4V while the alternator runs at idle speed. Over time, the field winding resistance will settle to a steady state temperature and the field excitation current will reach a final value that can be defined as full field. For this particular alternator, full field is defined as 4.3 A_{DC}, based on measurements under laboratory conditions (e.g. 25°C). For tests conducted at "full field", we have subsequently used a constant field current drive of 4.3 A_{DC}.

4.1.4 Output Power vs. Operating Speed

The next step in characterizing the alternator is to take output power measurements while running the machine at full field (4.3 A_{DC}) over the 1500 – 6000 alternator RPM operating range. A thermocouple is placed on one of the stator windings to monitor when the machine reaches thermal steady state at each operating point. Two sets of output data were taken during characterization because the commercial machine can be run with two different rectifier configurations; with and without 3rd harmonic "booster" diodes.

4.1.4.1 Output Power with Booster Diodes

Booster diodes are a 4th set of rectifier diodes that are connected to the neutral point of the 3-phase armature winding as shown in Figure 4.3. The booster diodes rectify 3rd harmonic content of the EMF voltage to deliver additional current to the load. Their effect is seen only at higher operating speeds and typically accounts for a 10% -15%

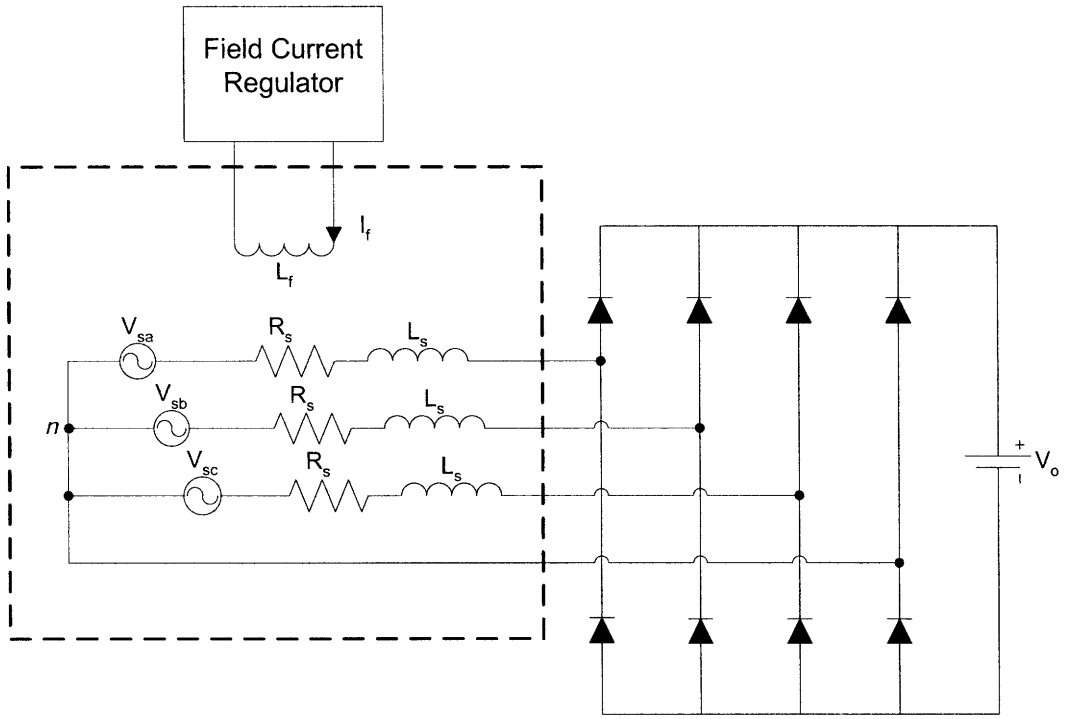

Figure 4.3 Three-phase alternator with booster diode rectifier

increase in average current [6, 15]. The Remy 92319 alternator was equipped with booster diodes in its off-the-shelf configuration.

The output power and winding temperature measurements of the alternator with 3rd harmonic booster diodes are compiled into Table 4.1, and used to generate Figures 4.4 and 4.5. The maximum output power at cruising speed of 6000 RPM is 1761 W with 130 A_{DC} output current. The winding temperature measurements from Figure 4.5 are consistent with [3] where the windings operate at their highest temperature at mid range operating speed and cool down at higher operating speeds despite the machine generating more RMS current.

Table 4.1: Remy 92319 Test Data with Booster Diodes

Alternator RPM	I_o (A)	V_o (V)	P_o (W)	T_w (°C)
1600	67.2	13.237	889.53	125
2000	85.2	13.29	1132.31	159.7
2400	94.68	13.342	1263.22	172.1
2800	103.08	13.361	1377.25	178.2
3200	110.4	13.407	1480.13	178
3600	116.4	13.428	1563.02	174.7
4000	120.68	13.437	1621.58	167.7
4400	122.12	13.483	1646.54	160.6
4800	124.8	13.495	1684.18	153
5400	127.8	13.508	1726.32	147.4
6000	130.32	13.516	1761.41	141.8

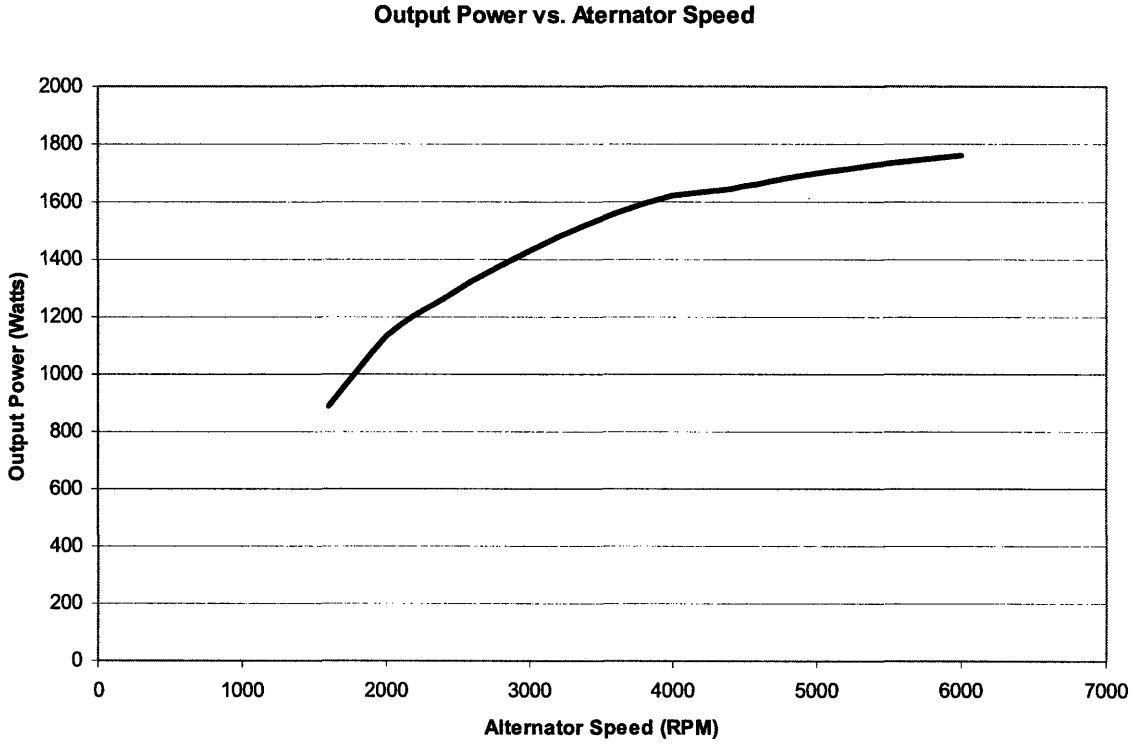

Figure 4.4 Remy 92319 Output power vs. alternator speed; with booster diodes

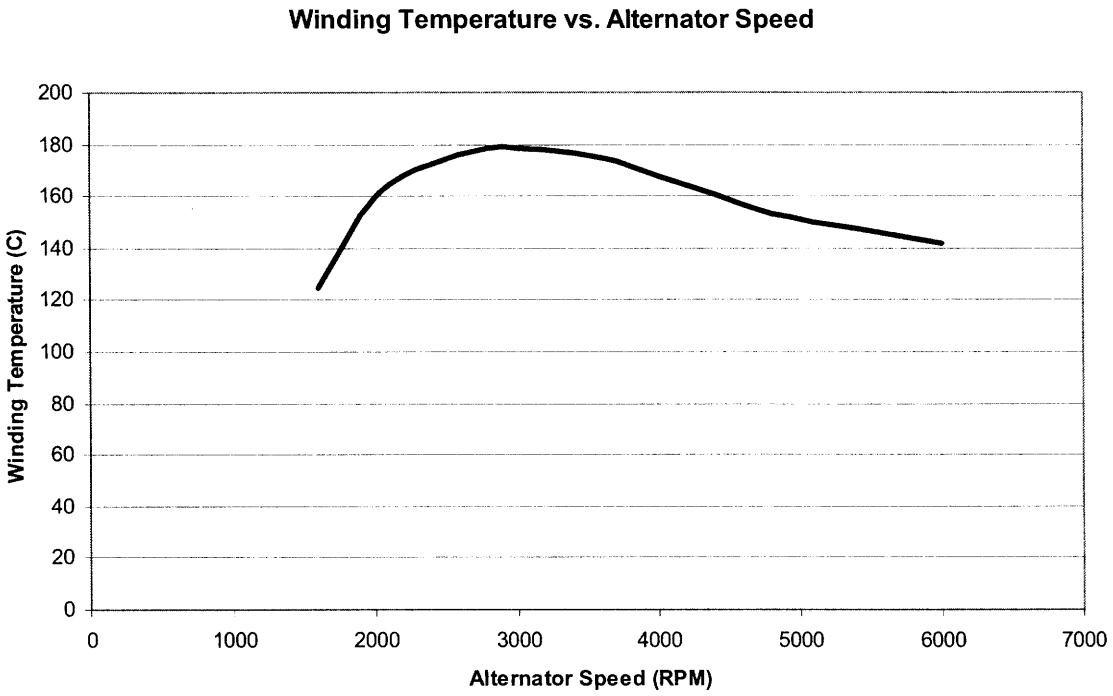

Figure 4.5 Remy 92319 Winding temperature vs. alternator speed; with booster diodes

4.1.4.2 Output Power without Booster Diodes

The two booster diodes in the Remy alternator were identified and removed from the rectifier circuit so that the output power measurements could be taken with a standard 3-phase rectifier. The output power data is compiled into Table 4.2 with a corresponding plot in Figure 4.6.

Table 4.2: Remy 92319 Test Data without Booster Diodes

Alternator RPM	I_o (A)	V_o (V)	P_o (W)
1500	62	13.41	831.42
2000	86.12	13.52	1164.34
2500	97.52	13.55	1321.40
3000	102.32	13.57	1388.48
3500	105.84	13.57	1436.25
4000	108.16	13.59	1469.89
4500	109.76	13.59	1491.64
5000	110.96	13.6	1509.06
5500	111.88	13.6	1521.57
6000	112.6	13.6	1531.36

The maximum output power at cruising speed of 6000 RPM was 1531 W with 113 A_{DC} output current. Since a standard 3-phase, 6-component rectifier was intended for the SMR machine, the data from Table 4.2 and Figure 4.6 were used as the basis for the computational model. No winding temperature data was taken in this configuration because the temperature data from Figure 4.5 provided the necessary information to appropriately size the armature winding in the SMR-based machine.

4.1.5 Machine Constant

Recall from equation 1.1, the peak line-to-neutral EMF voltage generated by the machine is defined by

$$V_s = k\omega i_f \tag{4.2}$$

where i_f is the field excitation current, ω is the rotational speed of the alternator shaft,

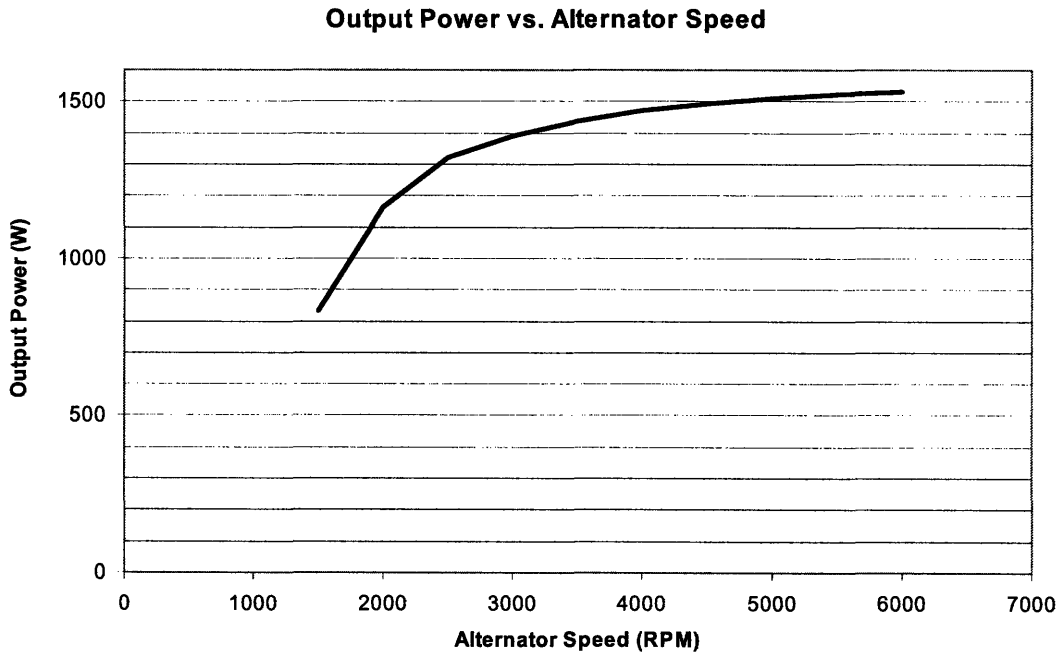

Figure 4.6 Remy 92319 Output power vs. alternator speed; without booster diodes

and k is the machine constant in units of volt-seconds per ampere-radian. The machine constant is an important parameter because it is a coupling factor between the field excitation and the number of turns in the stator winding. When the rewinding ratio of the stator is being considered, the machine constant will scale directly with the number of turns and determine the peak EMF generated by the machine over the operating range.

The value of the machine constant can be obtained by taking a direct measurement of the line-to-neutral voltage with an unregulated open circuit output on the alternator. The manner in which to do this is to disconnect the constant voltage load and operate the machine at full field while monitoring any line-to-neutral voltage with an oscilloscope. Differential scope probes must be used because the neutral point of the 3-phase armature floats with respect to earth ground. Also, the dataset should be limited to lower operating speeds to ensure the protection of the rectifier diodes. The reverse junction of the rectifier diodes will be exposed to the peak line-to-line EMF voltage which is equal to $\sqrt{3} * V_s$. If this value exceeds the maximum rated reverse voltage of the diodes they will begin to avalanche which could thermally overstress the devices and cause failure. The collected dataset is presented in Table 4.3 and uses the equations

$$k = \frac{V_s}{\omega i_f} \tag{4.3}$$

Table 4.3: Machine Constant Test Data

Alternator RPM	ω (rad/sec)	I_f (A)	V_s (V)	k (V-sec/A-rad)
1600	1005.31	4.30	14.45	0.0033
2000	1256.64	4.30	18.10	0.0033
2400	1507.96	4.30	21.65	0.0033
2800	1759.29	4.30	25.20	0.0033
3200	2010.62	4.30	28.60	0.0033
3600	2261.94	4.30	32.25	0.0033

$$\omega = \frac{2\pi * P}{2}\frac{n}{60} = \pi * P\frac{n}{60} \tag{4.4}$$

where n is the rotor RPM and P is the number of poles in the machine to determine the machine constant. This alternator is a 12-pole machine, thus the machine constant for this particular alternator averages to .0033 volt-seconds per ampere-radians.

4.1.6 Synchronous Inductance

Figure 4.7 shows the simplified electrical model of the alternator machine that was introduced in Chapter 1. Each of the three phases is connected to the rectifier through an inductance L_s that is called the synchronous inductance. This synchronous inductance is the effective inductance seen by one phase under the balanced three-phase condition, $i_a + i_b + i_c = 0$, of normal machine operation. It consists of three components: A component of self-inductance due to space-fundamental air-gap flux produced by the

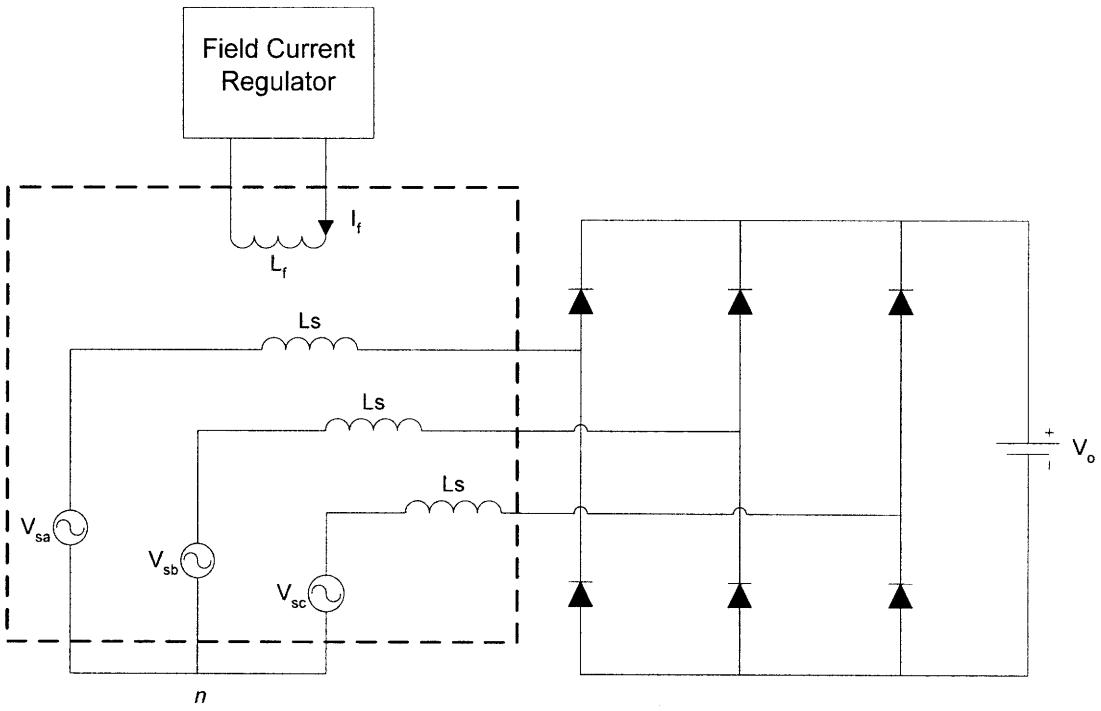

Figure 4.7 Electrical model of Lundell alternator [2]

current in that phase; a component of leakage inductance due to armature leakage flux; and a component of mutual inductance due to space-fundamental air-gap flux produced by currents in the other two phases [9].

If the effect of rotor slots is ignored and the air gap is only attributed to the stator core slots then the synchronous inductance of phase a, is a constant defined as

$$L_{sa} = \frac{3}{2} L_{aa} + L_{al} \tag{4.5}$$

where one part of L_{aa} is the self-inductance component, L_{al} is the leakage inductance component, and a $\frac{1}{2} L_{aa}$ is the mutual inductance component. The ½ factor comes about because the armature phases are displaced by 120°. Also, ignoring salient behavior yields the approximation

$$L_{sa} = L_{sb} = L_{sc}. \tag{4.6}$$

A detailed derivation of (4.5) is carried out in Chapters 4 and 5 of [9] and in [14]. For now this brief explanation is only meant to demonstrate the validity of modeling the synchronous inductance as a function of the current in a single phase even though this is not the case.

The complexity of the synchronous inductance components, especially when considering the affects of rotor displacement makes it difficult to accurately measure this value with any consistency. The course of action taken when trying to determine the value of synchronous inductance is to plot the alternator output power vs. speed and use an inductance value that will generate a best-fit curve at high end operating speeds where the reactive impedance dominates. This will be explored further when the model is developed.

4.1.7 Stator Winding Resistance

The stator winding resistance as a DC parameter at room temperature operation is a straightforward measurement. It is the line-to-neutral resistance of the armature windings, determined by the length of the winding, area of the conductor, and the conductivity of copper. However, the armature windings in the alternator operate far above room temperature and are carrying AC current. The higher temperature decreases the conductivity of copper and AC current induces skin and proximity effects, which effectively reduce the conduction area of the winding. Hence, the effective winding resistance during operation will be greater than the DC value and a DC measurement is of little help as a model parameter.

Like with synchronous inductance, the best course of action is to plot the output

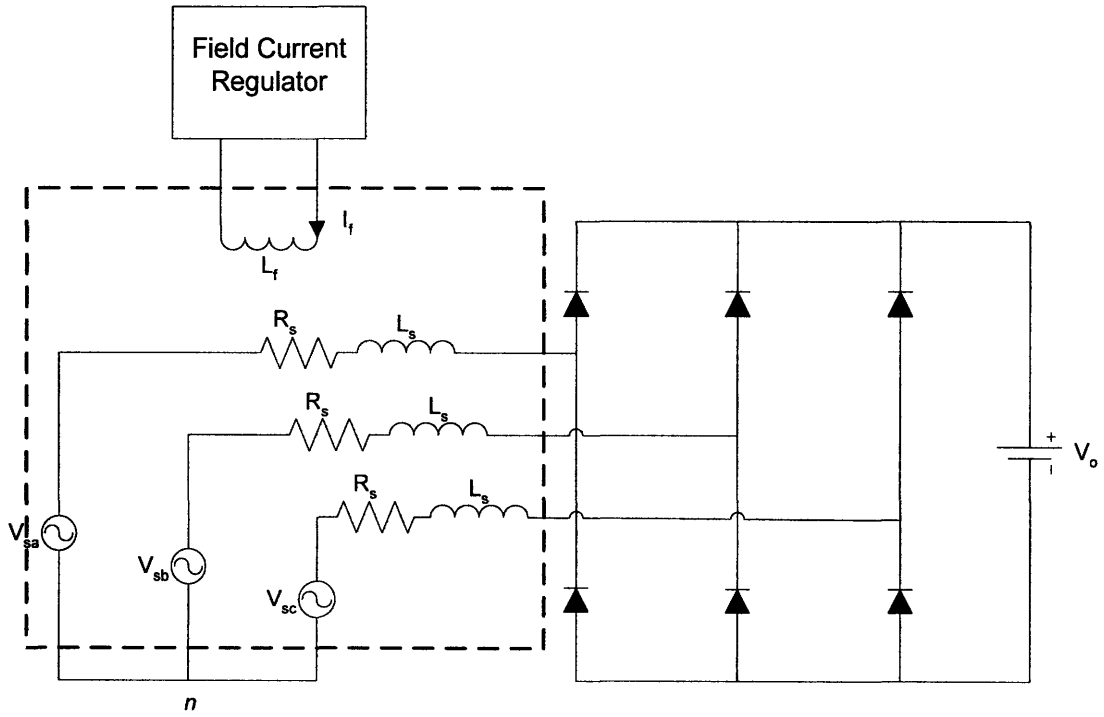

Figure 4.8 Electrical model of Lundell alternator including series winding resistance [2]

characteristics obtained in 4.1.4 and manipulate the winding resistance to find a best-fit curve. Winding resistance will have a greater impact at the lower operating speeds where there is very little reactive impedance. An expanded model of the alternator is shown in Figure 4.8 with the winding resistance placed in series with the synchronous inductance on each phase.

4.2 Alternator Output Model

4.2.1 Fundamental Equations

The fundamental equations of the alternator model are derived in [2] where the analysis of a three-phase bridge rectifier supplied by an inductive AC source and driving a constant-voltage load, as shown in Figures 4.9, is presented. The equations are expanded to include series resistance and the forward voltage drop of the rectifier diodes. The objective here is not to re-derive these equations but rather discuss how the derivations were made and how the electromechanical parameters quantified in section 4.1 fit into these equations.

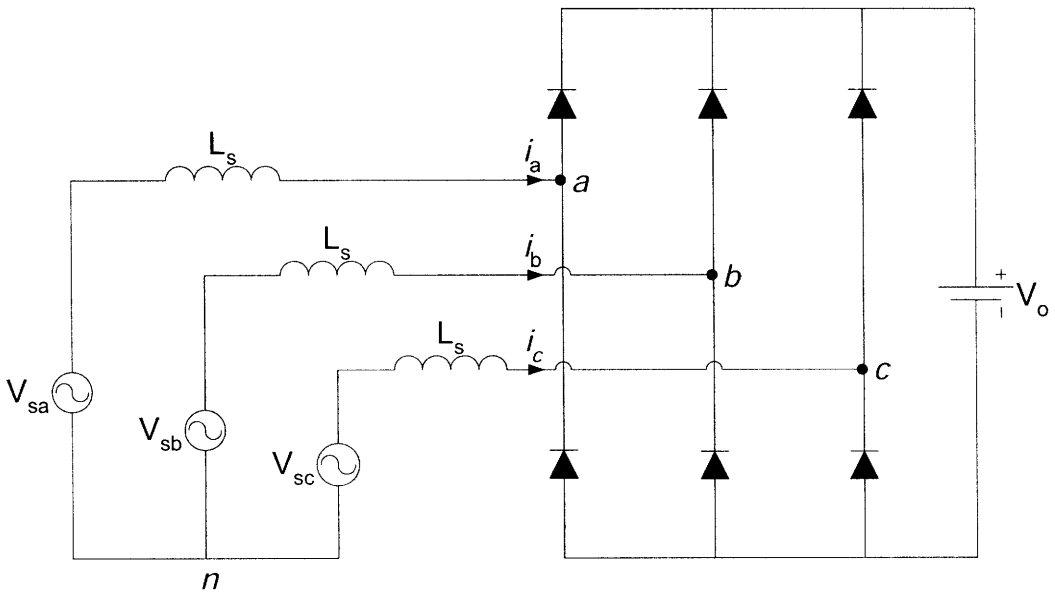

Figure 4.9 Three-phase diode bridge with constant-voltage load and ac-side reactance [2]

Looking at Figure 4.9 there are three source currents, i_a, i_b, i_c and a balanced three-phase set of sinusoidal voltages, V_{sa}, V_{sb}, V_{sc}. The three source voltages are represented as

$$V_{sa} = V_s \sin(\omega t) \tag{4.7}$$

$$V_{sb} = V_s \sin\left(\omega t - 2\pi/3\right) \tag{4.8}$$

$$V_{sc} = V_s \sin\left(\omega t + 2\pi/3\right) \tag{4.9}$$

with magnitude V_s and angular frequency ω. At points a, b, c there is a resultant voltage sink, in phase with the respective source current, and corresponding to the directionality of the current. For example, if it is assumed that the source current i_a is in continuous conduction, the voltage at point a *with respect to neutral,* V_{an}, takes the shape of the waveform in Figure 4.10. The voltages at points b and c take the same form only they are displaced by $2\pi/3$ radians. The waveform in Figure 4.10 can be described by the Fourier Series magnitude coefficients

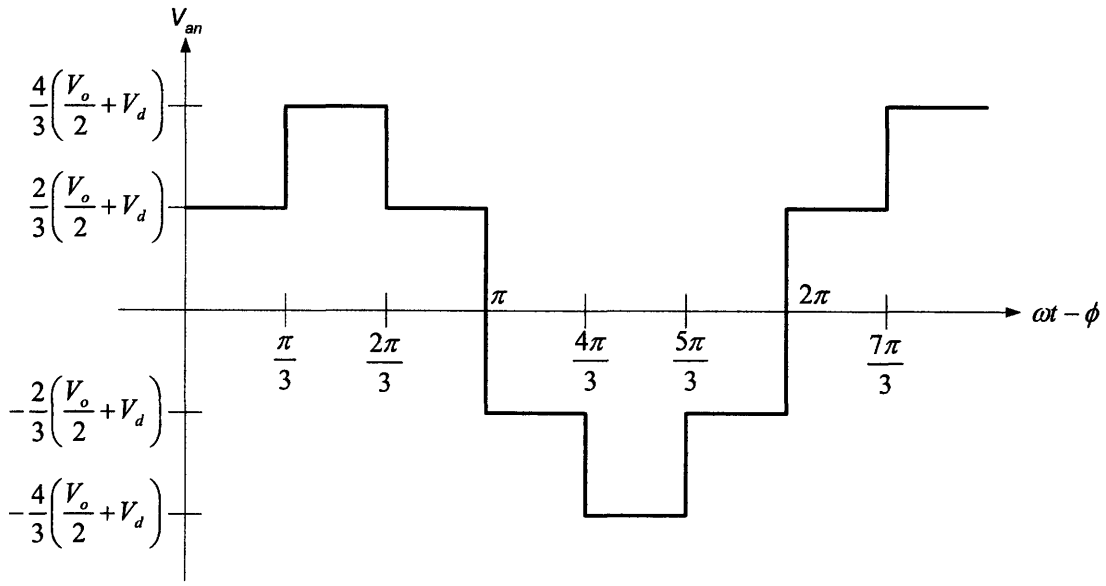

Figure 4.10 Rectifier phase a line-neutral voltage [2]

$$V_{an,k} = \frac{4}{k\pi}\left(\frac{V_o}{2} + V_d\right), \text{ for } k = 1, 5, 7, 11, 13,\ldots \tag{4.10}$$

where the lowest harmonic is the 5th at a magnitude of only 20% of the fundamental. The largest harmonic current component in this phase is also the 5th, and is only 4% of the magnitude of the fundamental because the impedance of L_s rises linearly with frequency. Therefore the voltages V_{an}, V_{bn}, and V_{cn} and the source currents i_a, i_b, and i_c can be approximated by their fundamental components [2].

For phase a, this approximation would yield

$$V_{an} \approx V_{an1} = V_{o1}\sin(\omega t - \phi) \tag{4.11}$$

where $V_{o1} = (4/\pi)(V_o/2 + V_d)$ and Φ is the phase angle between V_{sa} and V_{an1}. Since V_{an1} is in phase with i_{a1}, the current takes the same form, namely

$$i_a \approx i_{a1} = I_{s1}\sin(\omega t - \phi) \tag{4.12}$$

where I_{s1} is the magnitude and Φ is the phase of the fundamental of the line current. These approximations are then used to simplify Figure 4.9 by substituting the entire bridge rectifier constant-voltage load network with equivalent line-to-neutral voltages. Furthermore since each line-to-neutral voltage is in phase with its respective line current, the line-to-neutral voltages can be modeled as an equivalent resistance (R) where R is

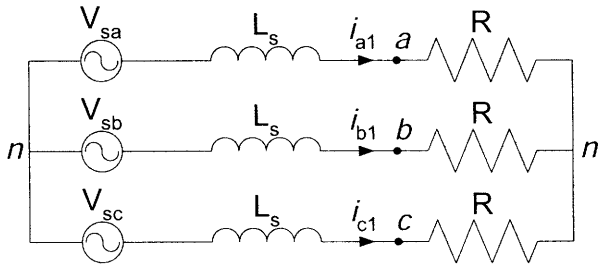

Figure 4.11 Three-phase rectifier model with equivalent resistance R [2]

defined as

$$R \equiv \frac{V_{o1}}{I_{s1}}. \tag{4.13}$$

The simplified model with equivalent resistances is shown in Figure 4.11.

The network in Figure 4.11 can be analyzed to yield an expression for the fundamental of the line current,

$$I_{s1} = \frac{\sqrt{V_s^2 - V_{o1}^2}}{\omega L_s} = \frac{\sqrt{V_s^2 - \frac{16}{\pi^2}\left(\frac{V_o}{2} + V_d\right)^2}}{\omega L_s} \quad . \tag{4.14}$$

Expanding Figure 4.11 to include series resistance complicates the expression but provides for a more accurate model at low operating speeds. This expression is

$$I_{s1} = \frac{V_s^2 - \frac{16}{\pi^2}\left(\frac{V_o}{2} + V_d\right)^2}{\frac{4}{\pi}\left(\frac{V_o}{2} + V_d\right)R_s + \sqrt{(\omega L_s)^2\left(V_s^2 - \frac{16}{\pi^2}\left(\frac{V_o}{2} + V_d\right)^2\right) + R_s^2 V_s^2}} \tag{4.15}$$

where V_s is the peak of the EMF voltage, ω is the angular frequency of the alternator, L_s is the synchronous inductance, R_s is the winding resistance, and V_d is the forward drop of the rectifier diodes. The average output current delivered to the constant-voltage load can then be approximated as

$$\langle i_o \rangle \approx \frac{3}{\pi} I_{s1}. \tag{4.16}$$

Consequently, it follows that

$$P_o = V_o \langle i_o \rangle \tag{4.17}$$

where V_o is the constant-voltage. Equations 4.15-4.17 are the three fundamental equations that along with (4.2) are used to model the output power characteristics of the alternator.

4.2.2 Electromechanical Parameters

Recall from 4.1, parameters such as field current and machine constant were experimentally measured. The machines output characteristics were also measured and used to generate plot of the alternator's output power vs. speed with two rectifier configurations. The last two parameters, synchronous inductance and winding resistance, were not obtained with a direct measurement and were to be determined by using values that would produce a best fit curve of the alternator's output characteristics. It is necessary that these parameters are modeled as accurately as possible as they scale with the square of the winding ratio.

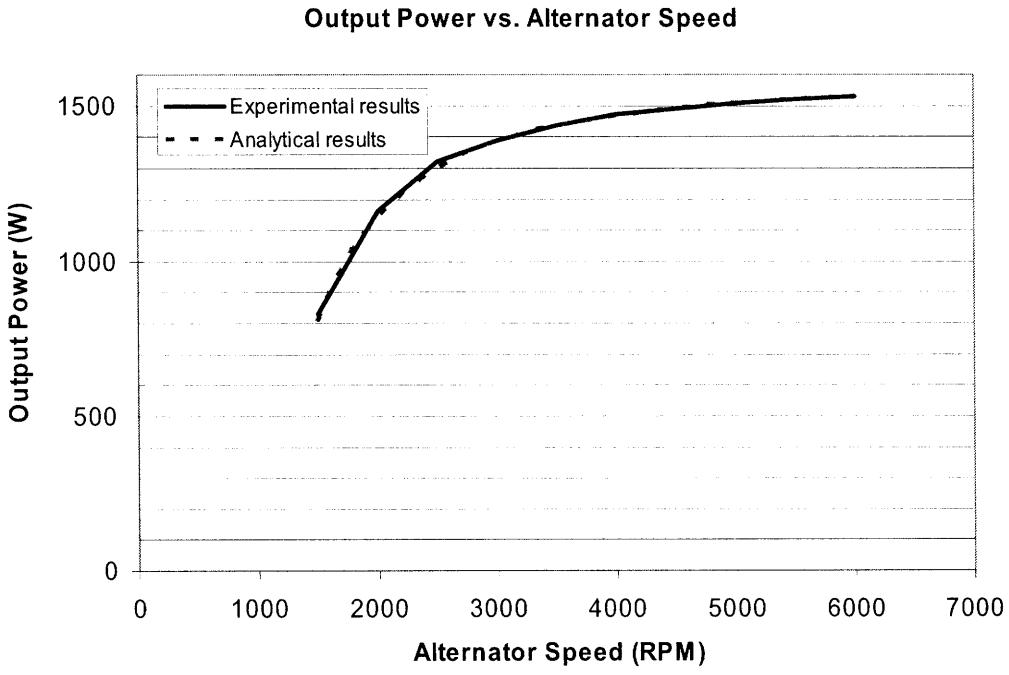

Figure 4.12 Comparison of experimental vs. analytical data of alternator output power

Using Equations 4.2, and 4.15-4.17, a plot is developed to model an alternator driving a 13.5 V load. This plot is then superimposed onto Figure 4.6, the measured output data of the alternator *without* booster diodes. The unknown parameters, L_s and R_s, are varied until the plot forms a best fit curve. The rectifier diode drop is also tweaked but the value of this parameter is unimportant as the properties of schottky diodes used in the SMR will be different than those used in the off-the-shelf diode rectifier and are unchanged by the rewinding ratio. Figure 4.12 shows the experimental output power vs. alternator speed of the off-the-shelf alternator and a superimposed plot of the model developed from Equations 4.2, 4.15-4.17.

The parameters that produced this analytical model were $L_s = 116.5\ \mu H$ and $R_s = 30\ m\Omega$. The analytical model was compared with the measured dataset and the model produced a mean error of less than 1%. These are the values of L_s and R_s that are used for the rewinding design which will be implemented in the following chapter.

Chapter 5

5. Alternator Magnetics Design

In this chapter the additional control capability provided by the SMR is introduced and the use of SMR duty ratio as a control variable is presented. The analytical model equations from the previous chapter are manipulated to include this new design variable. The efficiency-optimized control law is briefly discussed as a means of optimizing the new design variable. The parameters of machine operation are scaled according to the winding ratio and the computational model is used to calculate expected performance improvement and device thermal stress as a function of the stator winding ratio. A winding ratio is chosen that will satisfy the design goals while not overstressing the devices.

5.1 Objective

The objective of rewinding the stator core is to achieve more efficient utilization of the machine's capabilities at the desired output voltage of 14 V. This is done through operating at a load-matched condition over certain operating speeds and also by reducing the effective impedance across the armature windings.

Given a rewinding ratio, m, that is a fraction of the number of original series-turns in the armature, the following equations are used to determine the new electromechanical parameters of machine operation:

$$L_{s,m} = m^2 L_{s,1} \tag{5.1}$$

$$R_{s,m} = m^2 R_{s,1} \tag{5.2}$$

$$k_m = m k_1 \tag{5.3}$$

where the subscript ,m denotes the rewound value and the subscript ,1 denotes the original value. These equations assume that wire size has been adjusted such that wire copper area for each turn is increased by a factor of m, and that a constant copper fill factor of the armature slots is maintained. It follows that the machine current is proportional to the inverse of m,

$$I_{s1,m} \propto \frac{I_{s1,1}}{m}. \tag{5.4}$$

These relationships hold for any value of m and the objective is to specify a value of m that will achieve the design goals with the devices from Chapter 3.

5.2 SMR Duty Ratio Control

The SMR introduces a new control variable which is the switching duty cycle d of the MOSFETs. The duty cycle is the percentage of a MOSFET switching cycle (far shorter than a machine electrical cycle) during which the device is conducting. The importance of the switching duty cycle is that it provides a scaling factor for the effective output voltage "seen" by the alternator machine [1, 7]. This scaling factor can be optimized to produce a load-matched condition which provides the capability of maximum power delivery from the machine to the load at a given operating speed.

The analytical equations introduced in 4.2.1 model the behavior of a standard

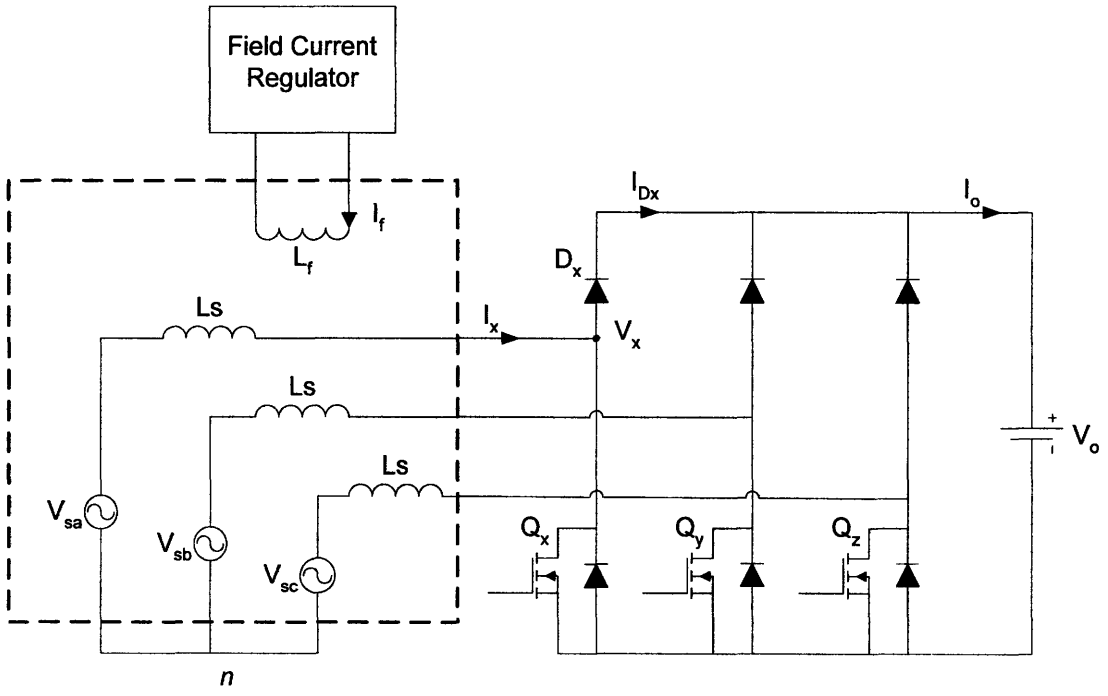

Figure 5.1 Alternator with 3-phase switched-mode rectifier

three-phase rectifier but do not include the duty cycle variable. To see how this variable affects the model, consider Figure 5.1. We focused on one boost switch set made up of a modulated switch, Q_x, and rectifier diode, D_x. Because the switching period T_{sw} is extremely short compared to the armature time constant, the machine reacts to the average voltage value (over a switching cycle) at the rectifier. In particular, the important voltage on the output of the given phase, x, is the local average value of V_x over a switching cycle [13, Chapter 11]. The actual voltage v_x takes the shape of the waveform in Figure 5.2. The local average value of v_x is given by the expression

$$\langle v_x \rangle = d'V_o \tag{5.5}$$

where $d' \equiv 1 - d$. The current i_x is the sinusoidal phase current with peak value I_{s1}. The peak value I_{s1} can then be expressed as

$$I_{s1} = \frac{V_s^2 - \left(\frac{2V_o d'}{\pi}\right)^2}{\frac{2V_o R_s d'}{\pi} + \sqrt{(\omega L_s)^2\left(V_s^2 - \left(\frac{2V_o d'}{\pi}\right)^2\right) + R_s^2 V_s^2}} \tag{5.6}$$

where the output voltage V_o has been replaced by the effective output voltage $d'V_o$ and the diode forward drop has been omitted for simplicity.

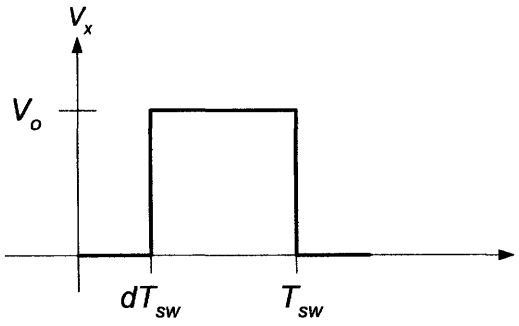

Figure 5.2 Representative voltage waveform of V_x over a switching period T_{sw}.

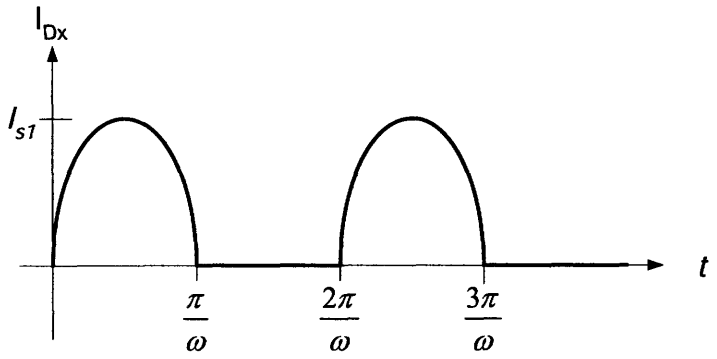

Figure 5.3 Representative current waveform I_{Dx} when $d = 0$

Now consider Figure 5.3 which is the representative current waveform through rectifier diode D_x under the condition that the duty cycle d was zero (i.e. $d'V_o = V_o$). The averaged diode current takes the form

$$\langle I_{Dx} \rangle = \frac{I_{s1}}{\pi}. \tag{5.7}$$

If Q_x were modulating, the current waveform I_{Dx} would take the shape of Figure 5.4. Here the sinusoidal waveform is being "chopped" such that the current through the diode goes to zero for time dT_{sw} when Q_x is conducting and returns to its sinusoidal form during

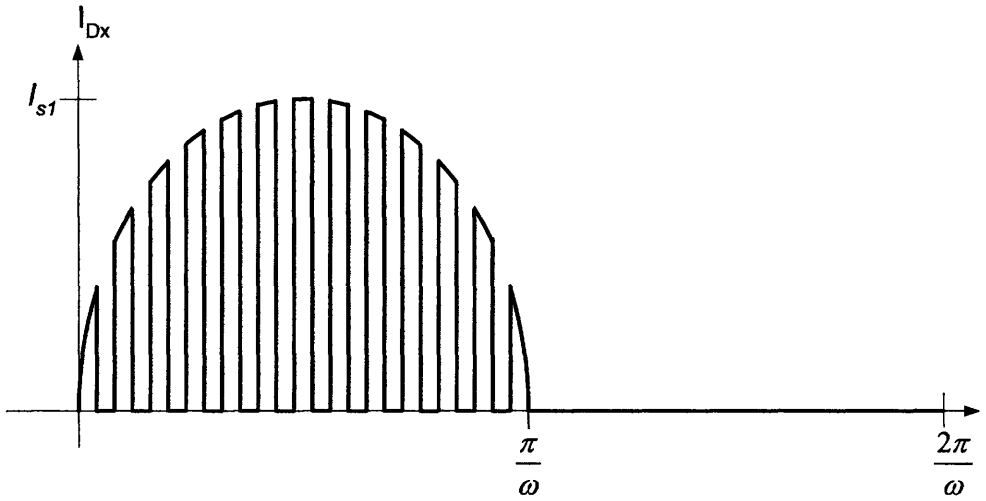

Figure 5.4 Representative current waveform I_{Dx} when $d > 0$

time $d'T_{sw}$ when Q_x is not conducting. It should be noted that one MOSFET switching cycle is much faster than an alternator half-EMF cycle, and Figure 5.4 is only depicted in such a way as to emphasize the effect of switch modulation.

Based on the current waveform in Figure 5.4, the averaged value diode current I_{Dx} can be expressed as

$$\langle I_{Dx} \rangle = \frac{I_{s1}}{\pi} d'. \tag{5.8}$$

The total averaged output current I_o then becomes

$$\langle I_o \rangle \approx 3\langle I_{Dx} \rangle = \frac{3}{\pi} I_{s1} d' \tag{5.9}$$

and the output power delivered to the constant-voltage load is then

$$P_o = \frac{3V_o d'}{\pi} I_{s1} = \frac{3V_o d'}{\pi} \frac{V_s^2 - \left(\frac{2V_o d'}{\pi}\right)^2}{\frac{2V_o R_s d'}{\pi} + \sqrt{(\omega L_s)^2 \left(V_s^2 - \left(\frac{2V_o d'}{\pi}\right)^2\right) + R_s^2 V_s^2}}. \tag{5.10}$$

5.2.1 Efficiency-Optimized Control Law

The SMR has introduced a new parameter d that was incorporated into the fundamental equations of machine operation in the previous section. In [1, 7] a control law is discussed for calculating d in the load-matched condition. The SMR duty ratio control law for achieving load matching is

$$d' = 1 - d = \left(\frac{\sqrt{2}\pi k}{4V_o}\right) \omega i_f \tag{5.11}$$

which shows that the complement of the duty cycle is controlled proportional to the angular frequency and field current. The simplest approach is to set duty ratio to zero and use conventional field control to regulate the output voltage by increasing field

current from zero up to the amount needed to support the output. If still more power is needed at full field current, one can increase duty ratio to provide more power, up to the maximum duty ratio

$$d_{\max} = 1 - \left(\frac{\sqrt{2}\pi k i_{f,\max}}{4V_o} \right) \omega = 1 - C\omega \tag{5.12}$$

where $i_{f,max}$ is the full field current and C is a proportionality constant between duty ratio complement and angular frequency. Note that d_{max} has a minimum value of zero. This control law allows for any power level from zero up to the maximum load-matched power to be achieved at any given speed [1].

It should be noted that the expression for d_{max} in (5.12) was obtained by maximizing the *ideal* output power from (1.2), which omits parameters such as stator winding resistance and the diode forward voltage drop. A more accurate expression for d_{max} is found by maximizing the output power expression (5.10), but this is a mathematically complex operation. The *value* of d_{max} is easily obtained by plotting output power as a function of duty cycle over the operating range, which is ultimately how we derived the optimal duty cycle for maximum load-matched power. We validated maximum power operation of the alternator by testing at $i_{f,max}$ and d_{max}.

5.3 Thermal Considerations for Rewinding Ratio

The goal to achieve a substantial power improvement in a 14 V alternator comes at the cost of higher absolute conduction losses, even though higher efficiency is achieved. Thus, winding ratio is limited primarily by the thermal capabilities of the devices and of the armature winding. The testing conducted in Chapter 3 demonstrated the efficacy of using a copper heat spreader and vias to conduct heat away from the devices and through the PCB. Quantitative thermal impedances were also determined for each device.

5.3.1 Device Power Dissipation

Much of the work needed to estimate the device power dissipation in the SMR has already been done. The averaged current for the rectifier diodes was previously determined in (5.4). Thus the power dissipation of each diode can be expressed as

$$P_{diode} = V_d \frac{I_{s1}}{\pi} d' \tag{5.13}$$

where V_d is the forward voltage drop. A reasonable approximation of $V_d = .5$ V can be made for an instantaneous forward current of up to 200 A.

The MOSFET is more complicated but comparable waveforms have already been presented. In the SMR the MOSFET will have two conduction cycles during any full alternator EMF cycle. The first conduction cycle occurs during the positive current half cycle (i.e. when $i_x > 0$ in figure 5.1) during which the MOSFET acts as a boost converter switch. The "chopped" current traveling through the MOSFET's conduction channel is the difference between the sinusoidal phase current and the chopped current in figure 5.4. This power dissipation component is expressed as

$$P_{cond,boost} = \frac{1}{2}\left(\frac{I_{s1}}{\sqrt{2}}\right)^2 dR_{ds\_on} \tag{5.14}$$

where d is the conducting duty cycle during a 100 KHz switching cycle.

The MOSFET also acts as a synchronous rectifier. That is, the MOSFET is turned-on for the duration of the negative half cycle of current i_x so that ground current returning from the load is delivered back to the three-phase alternator source through the MOSFET's conduction channel. The waveform of Figure 5.3 is analogous to the *source-to-drain* current through the conduction channel during synchronous rectification. This power dissipation component is expressed as

$$P_{cond,boost} = \frac{1}{2}\left(\frac{I_{s1}}{\sqrt{2}}\right)^2 R_{ds\_on}. \tag{5.15}$$

The MOSFET will also have a switching loss component that occurs during the positive half cycle of i_x if the device is switching. An expression for the switching loss as a function of peak switching current was determined in (3.8) for this particular MOSFET. That expression can be halved, since the MOSFET will only switch during half of a line cycle, and taken as a function of the peak line current I_{s1} to determine MOSFET switching loss in the SMR. The total power dissipation in the MOSFET is then

$$P_{FET} = P_{sw}\big|_{d>0} + P_{cond,boost} + P_{cond,synch}. \tag{5.16}$$

These four expressions (5.13) - (5.16) can now be used to analytically estimate device power dissipation as a function of winding ratio. A lower bound on the winding ratio can also be established by making a quick calculation of the maximum power dissipation of each device, under the approximation that the automotive environment where the alternator resides typically approaches ambient temperatures of 85°C. Working with the assumption that the alternator heatsink is ideal, $R_{\theta sa} = 0$, the power dissipation limit for the MOSFET is

$$P_{FET,\max} = \frac{T_{j,\max} - T_{ambient}}{R_{thJC,FET} + R_{thCS,FET}} = \frac{150^\circ C - 85^\circ C}{1.46\frac{^\circ C}{W}} \approx 44.5W$$

where the heat spreader is assumed to be the same size as that used in the test board. The same analysis is carried out for the diode producing the following,

$$P_{diode,\max} = \frac{T_{j,\max} - T_{ambient}}{R_{thJC,diode} + R_{thCS,diode}} = \frac{130^\circ C - 85^\circ C}{1.1\frac{^\circ C}{W}} \approx 41W.$$

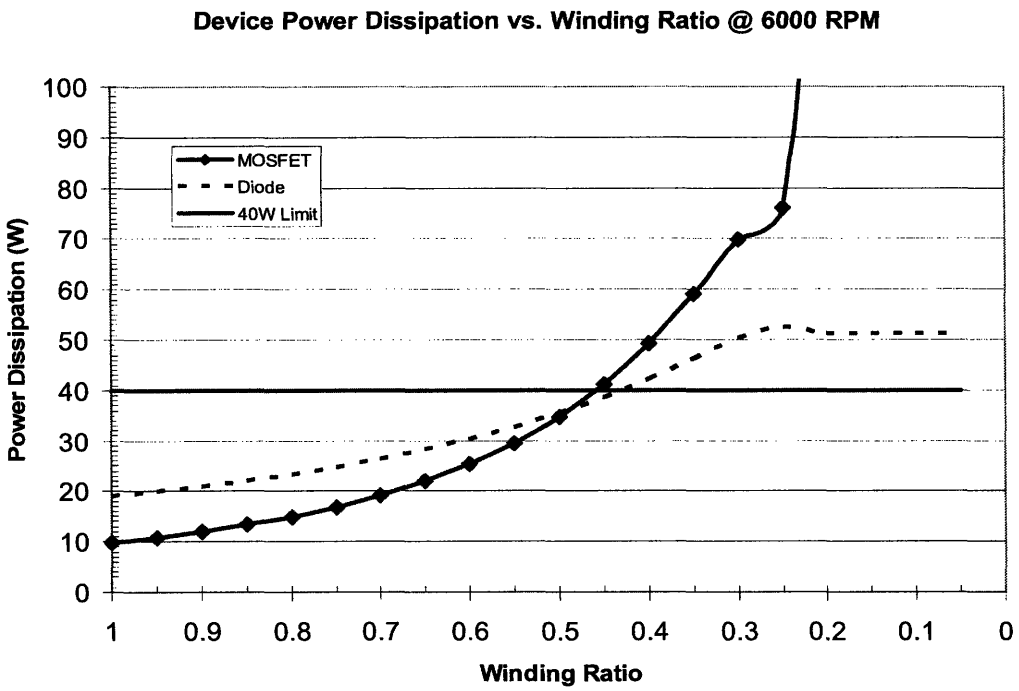

Figure 5.5 Device power dissipation vs. winding ratio @ 6000 alternator RPM

Figure 5.5 is generated using 40 W as an upper limit. This plot represents the MOSFET and diode power dissipation as a function of winding ratio at 6000 alternator RPM. The plot indicates that a stator rewound with less than half the number of series-turns as the original machine would approach the thermal stress limits of the devices, hence .5 will be used as a lower allowed bound for the winding ratio.

Another consideration in the rewinding design is that the MOSFET's thermal stress limit may actually be reached at lower operating speeds when the components of switching loss (3.8) and boost conduction (5.14) are contributing to the total loss. Figure 5.6 is a profile of the MOSFET's power dissipation as a function of alternator RPM at winding ratios of .5, .6, and .7.

The plot in figure 5.6 indicates that the MOSFET's power dissipation limit can be approached at lower RPM, and that lower winding ratios provide for less of a margin.

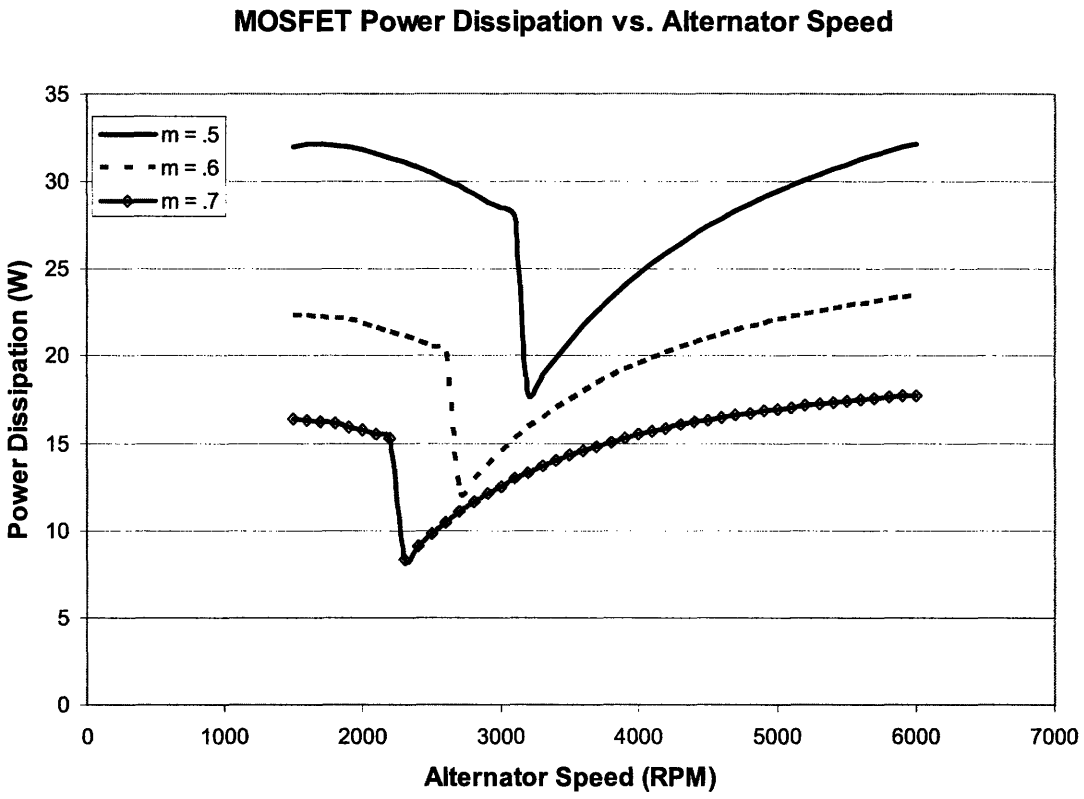

Figure 5.6 MOSFET power dissipation vs. alternator RPM at full power and three different winding ratios.

This is because the MOSFET device will be switching higher peak current for a longer duty cycle to operate in a load-matched condition. This point is further demonstrated in figure 5.7 where the expected output power at winding ratios of .5, .6, and .7, is compared against the 3-phase rectifier without booster diodes at $m = 1$. Figure 5.7 shows that the same output power is achieved at lower RPM for all of the winding ratios despite the MOSFETs working harder.

Figures 5.6 and 5.7 further indicate that a winding ratio of .6 would be a more efficient lower bound, given the expected output power improvement. A rewinding ratio of .5 produces a 17% improvement in high speed output power at the cost of a 40% increase in MOSFET power dissipation, when compared to a rewinding ratio of .6. By

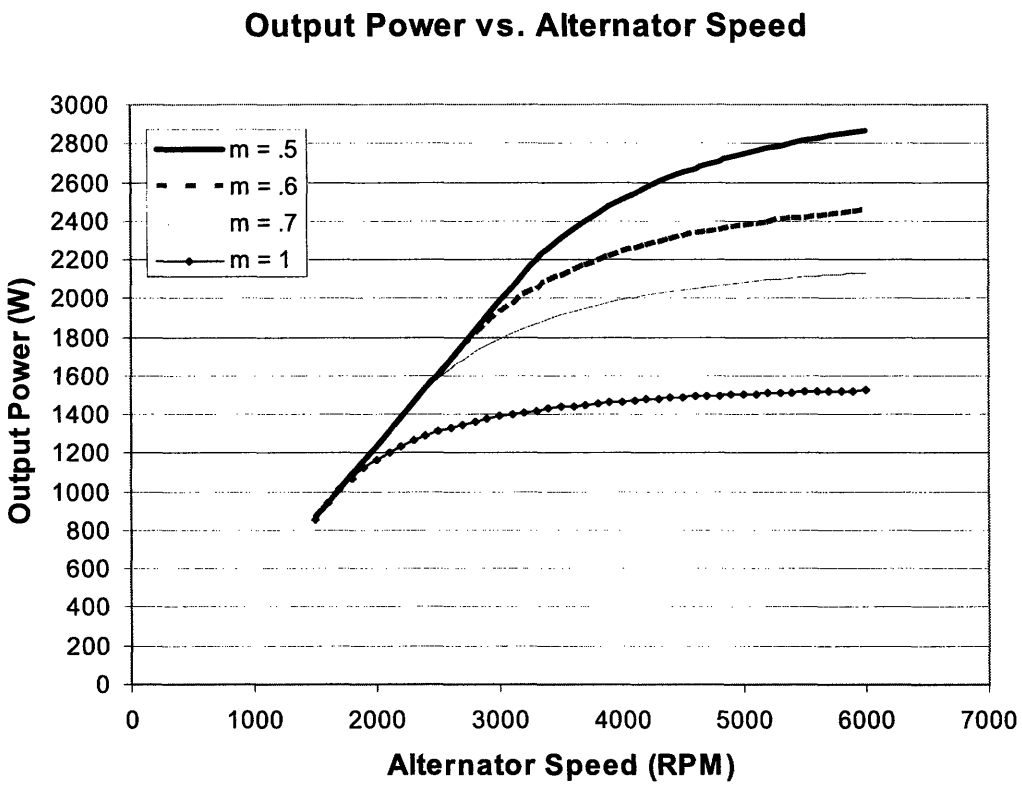

Figure 5.7 Expected output power vs. alternator RPM at three different winding ratios

comparison, the output power improvement between m = .6 and m = .7 is about 15% with only a 30% increase in MOSFET power dissipation.

Figure 5.8 was generated to show the output power improvement of a machine rewound at a ratio of .7 versus the commercial alternator with and without booster diodes. With m = .7, there is an expected 39% output power improvement over a basic three-phase diode bridge rectifier and a 21% improvement over the three-phase rectifier with 3rd harmonic booster diodes. This is a 10% falloff from the original design goal of 50% more power than the standard bridge rectifier. Together, figures 5.6-5.8 show that a rewinding ratio of less than .6 approaches a point of diminishing returns in terms of output power relative to device thermal stress, and a rewinding ratio of greater than .7

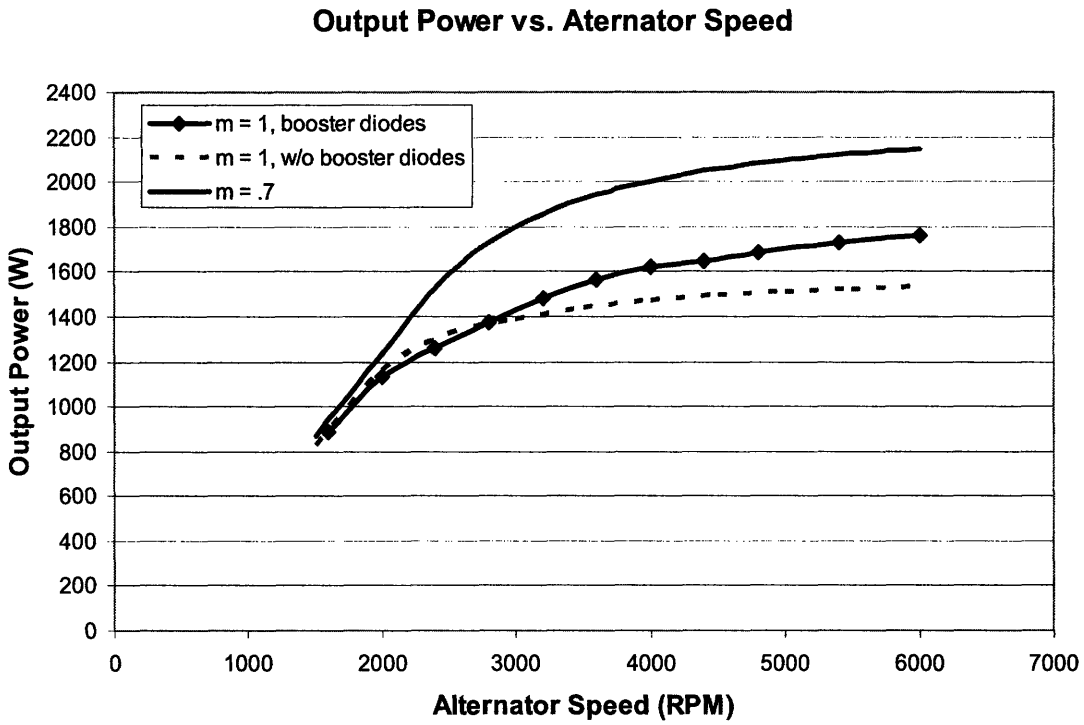

Figure 5.8 Comparison of output power vs. alternator RPM at three different operating conditions

approaches a point where the design goal is falling off by over 10%. Thus, m = .6 and m = .7 will be considered the lower and upper bound, respectively, as we move forward.

5.3.2 Mechanical Specifications

Another factor to consider in the rewinding design is the manufacturability of the rewound stator core. Figure 5.9 shows the top view of the unwound stator core after it was removed from the alternator that was characterized in Chapter 4. The core is approximately 5" in diameter and is made up of 36 slots, with each phase occupying 12 slots. This particular alternator was wound in a wave pattern with two parallel 14 AWG conductors per phase. A wave winding patterns means that a single conductor is wound by going down through a slot, over three slots, and up through a slot as shown by the arrows in Figure 5.9. This pattern continues clockwise around the core until the winding traverses the circumference six times and is terminated three slots over from where it

began. The second conductor for this phase has the same termination points and the same polarity through each slot only it traverses the core counter-clockwise. Each slot then carries 12 turns with the terminating slots carrying a 13^{th} turn. Each phase winding is wound 6 turns per slot or 72 series-turns. This is the nominal number of turns which will be reduced by some winding ratio, m.

The rewinding ratio can be considered either as a ratio of turns per slot or as a ratio of the total number of series-turns. Working with a ratio of turns per slot limits the number of possible choices of m and previous work from [8] has shown that a different winding pattern which allows for more choices of m can be used. Also because this winding pattern was utilized in [8] the manufacturing capability has already been proven.

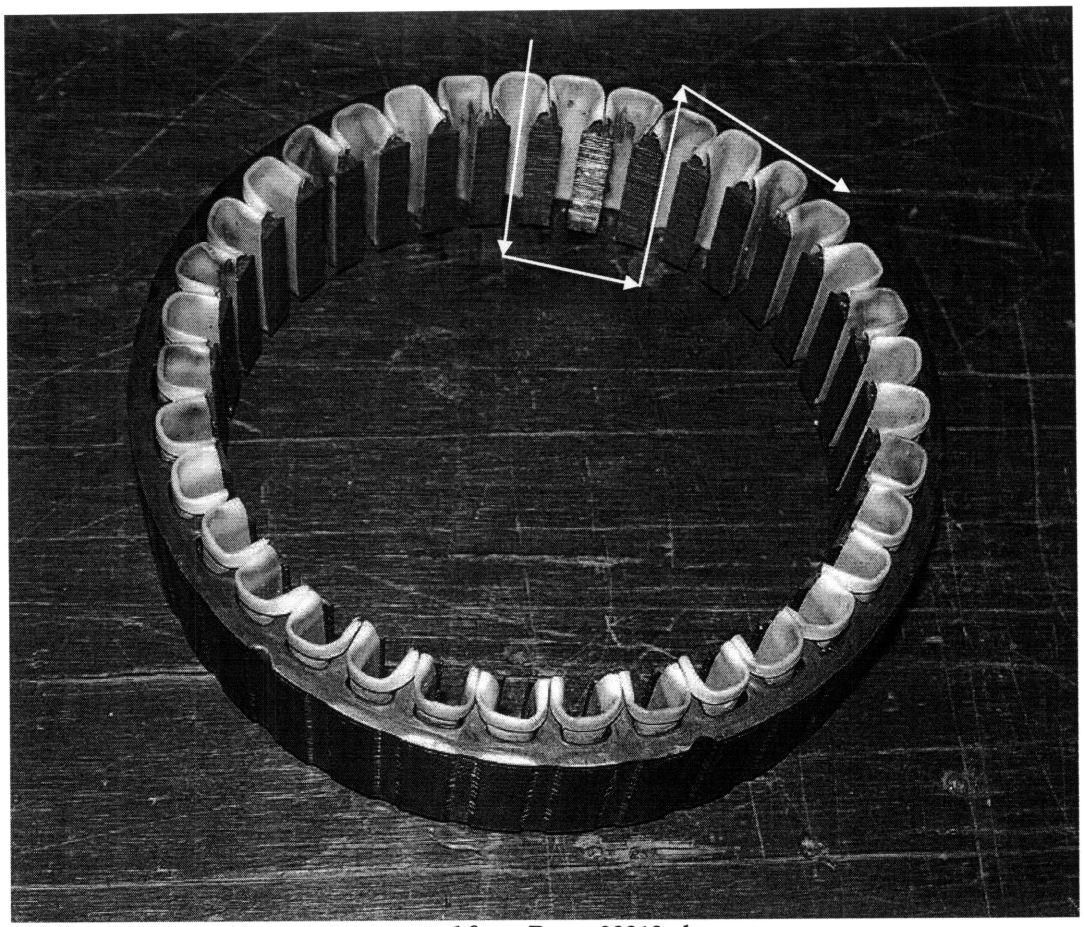

Figure 5.9 Unwound stator core removed from Remy 92319 alternator

The winding method utilized in [8] is referred to as coil winding. In this winding method, a length of wire is taken and wound in a circular coil. The total number of series-turns n is encompassed within a single coil. The coil is then split down the middle and opened such that the winding can be placed into three slots. The middle slot will consist of $n/2$ turns and the two outer slots will consist of $n/4$ turns. A second coil is placed such that one of its outer slots overlaps with the outer slot from the previous coil and all slots are then filled with $n/2$ turns. It takes six parallel coils to fill all twelve slots for each phase. Figure 5.10 shows the coil winding pattern with two parallel coils for the case where $n = 4$.

Filling each slot with $n/2$ turns requires a thinner gauge wire than what was used in the original design. A wire size that fits in the slot area and has sufficient conduction area so as to not thermally overstress the winding must be chosen. Figure 4.5 shows that in a 25°C ambient environment the windings approach 180°C. A new winding ratio with greater RMS current should at least maintain the current density of the conductors for comparable thermal performance and therefore the copper conduction area per slot and the copper packing factor need to be considered as design and manufacturing variables.

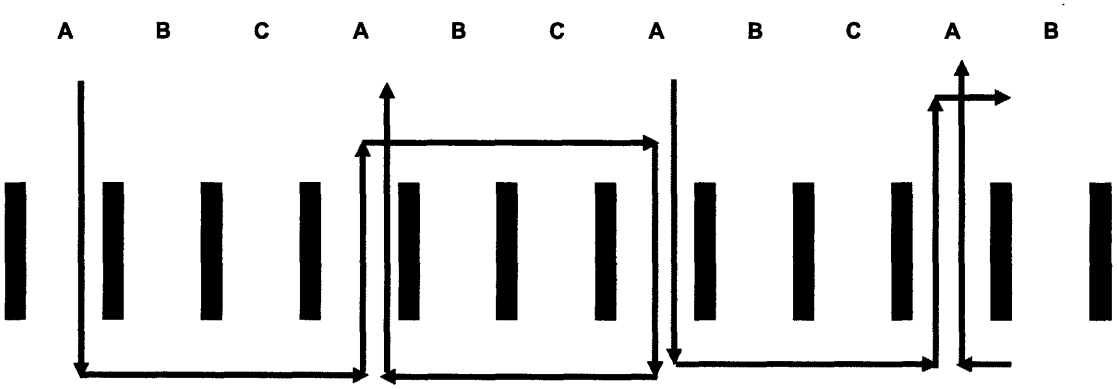

Figure 5.10 Coil winding pattern with two parallel coils

The conduction area for one armature winding A_w in the original alternator is defined as

$$A_w = \pi \frac{d_{14AWG}^2}{4} \tag{5.17}$$

where d_{14AWG} is the diameter of a 14 AWG conductor. Each slot is fitted with twelve turns thus the total conduction area per slot A_{slot} is

$$A_{slot} = 12A_w = 12\pi \frac{d_{14AWG}^2}{4} = 3\pi(64mil)^2 \approx 38604mil^2.$$

The conduction area per slot area is a measure of the slot area and can be used to determine the maximum wire gauge for the proposed number of turns.

Figures 5.6, 5.7, and 5.8 were used to set preliminary lower and upper bounds of $m = .6$ and $m = .7$ for the winding ratio. Given these bounds the number of series-turns can be determined by

$$.6 * 72 \le n \le .7 * 72 \Rightarrow 43.2 \le n \le 50.4$$

where n must be an even number integer and therefore 44 series-turns would be the lower bound and 50 series-turns would be the upper bound. Since each slot is filled with $n/2$ turns the maximum wire diameter d_{max} at each turns ratio is determined by

$$\frac{n}{2}\left(\frac{\pi d^2}{4}\right) = A_{slot} \Rightarrow d_{\max} = \sqrt{\frac{8A_{slot}}{n\pi}} \tag{5.18}$$

where $n = 44, 46, 48,$ and 50. It is also a sensible design practice to assume a packing factor less than one. This can be attributed to the packing factor of thinner gauge wire being less than that of larger gauge wire and also to an element of human error. Commercial alternators are machine wound whereas the rewound machine will be done by hand. The rewinding design from [8] was only able to fill each slot with about 90% of the total copper area of the original winding.

Table 5.1: Maximum allowable wire diameter at different turn ratios

m	$n/2$	d_{max}	AWG
44/72	22	44.84	17.5
46/72	23	43.86	17.5
48/72	24	42.93	17.5
50/72	25	42.07	18

Table 5.1 was generated to show the maximum wire diameter that could be used for each value of m, given 90% of the available slot area. Given what is shown in Table 5.1 the winding ratio that would optimize efficiency is m = 48/72. This winding ratio has the same conduction area as m = 44/72 and m = 46/72 for less RMS current. The wetted area exposed to direct airflow from the alternators cooling fan would also be greater given the two extra turns. Furthermore, the devices would operate with less thermal stress. In terms of manufacturability, this is the same number of turns per slot that was used in [8] so the capability has been proven. Finally, this winding ratio also allows for the possible use of a wave winding pattern as it can be realized as a turns per slot winding ratio of 4/6^{ths}.

A quick calculation can be used to determine the increase in conduction area from the original alternator to the new machine. In the original alternator, two parallel 14 AWG conductors carried the current in each phase, thus the conduction area A_{cond} is

$$A_{cond} = 2\pi\frac{d_{14AWG}^2}{4} = \pi\frac{d_{14AWG}^2}{2} \approx 6434 mil^2 .$$

In the new machine, six parallel 17.5 AWG conductors are carrying the current in each phase thus the conduction area A_{cond} is

$$A_{cond} = 6\pi\frac{d_{17.5AWG}^2}{4} = 3\pi\frac{d_{17.5AWG}^2}{2} \approx 8511 mil^2$$

and the relative increase in conduction area between machines is approximately 1.33.

Table 5.2: Expected increase in RMS phase current with rewound machine

RPM	$m = 1$	$m = 2/3$	Increase
1600	49.76	79.16	1.59
2000	63.09	81.66	1.29
2400	70.11	84.21	1.20
2800	76.33	96.59	1.27
3200	81.75	104.42	1.28
3600	86.19	109.71	1.27
4000	89.36	113.46	1.27
4400	90.43	116.22	1.29
4800	92.41	118.31	1.28
5400	94.63	120.61	1.27
6000	96.50	122.25	1.27

Table 5.2 was generated to show the increase in RMS phase current between the old alternator with booster diodes, denoted as $m = 1$, and the expected RMS line current of the rewound alternator, denoted as $m = 2/3$, over the operating range. This table shows that the expected increase in RMS current is less than 1.3 times the original RMS current throughout much of the operating range and thus the 1.33 times increase in conduction area should be capable of providing comparable thermal performance.

A winding ratio has now been determined based on satisfying the electrical and mechanical requirements. A series of characterization plots can be shown to quantify the expected output power improvement and the power dissipation profile of the new machine. Figure 5.11 shows the *measured* output power over the operating range of the original machine with and without booster diodes and the *expected* output power of the rewound machine. The analytical model estimates a 45% improvement over a standard three-phase rectifier and 26% improvement over a three-phase rectifier with 3rd harmonic booster diodes. Figure 5.12 shows the estimated power dissipation profile of the two power devices over the operating range based on equations (5.13) – (5.16). The power dissipation profile is a measure of the overall device efficiency in the SMR and will be used to gauge the expected temperature rise of each device.

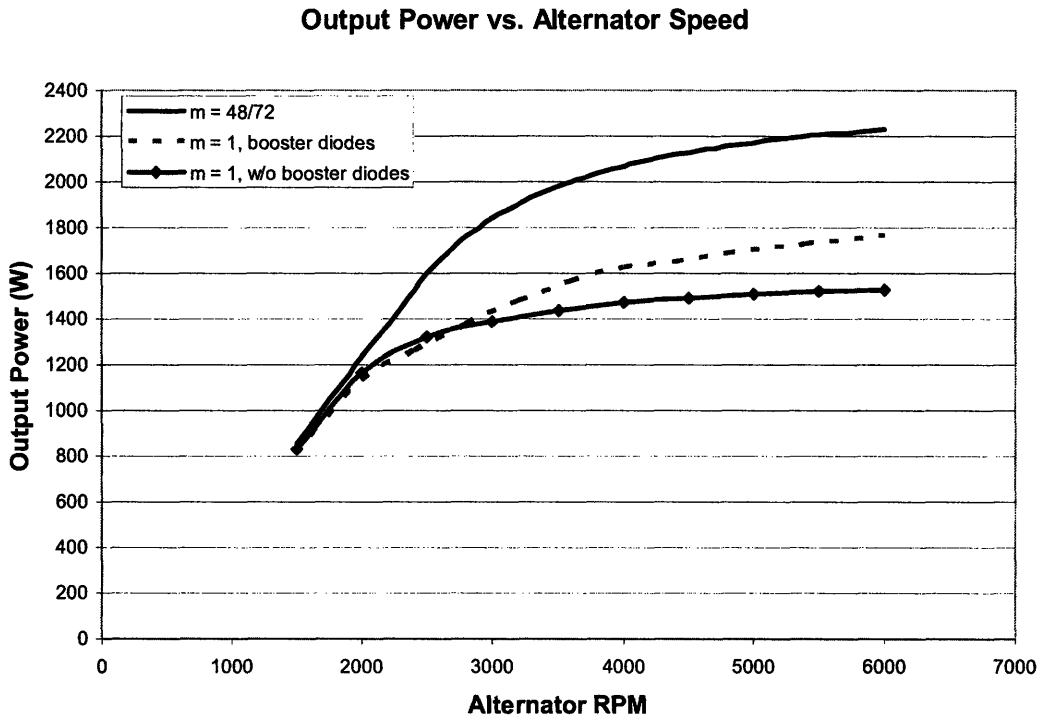

Figure 5.11 ***Expected*** **output power improvement of rewound machine over the** ***measured*** **power of the original alternator with and without booster diodes**

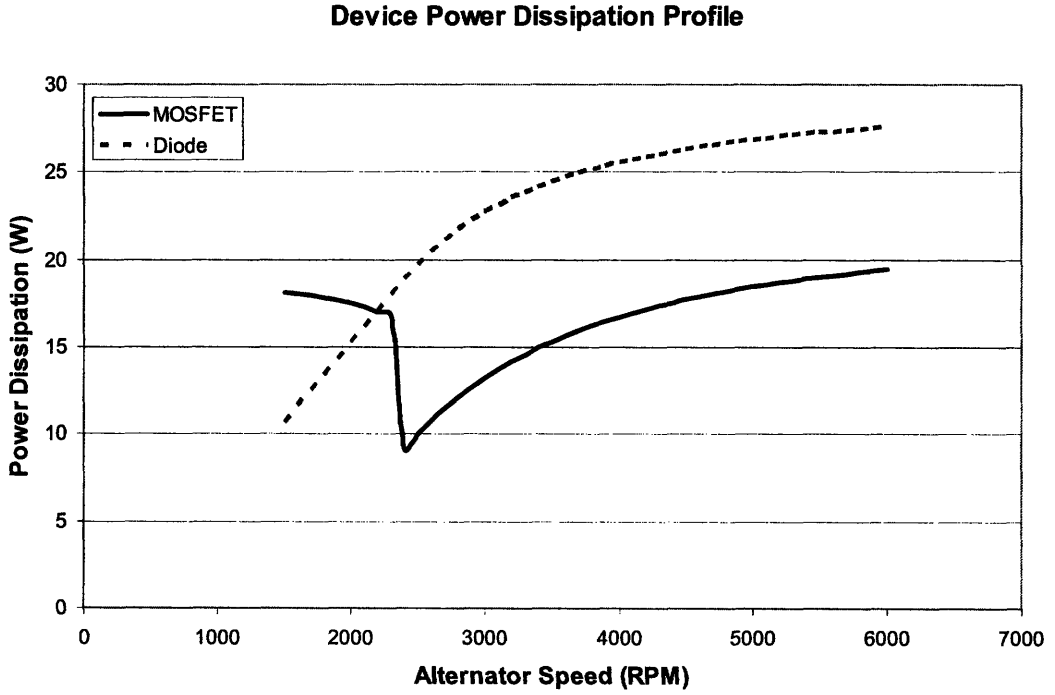

Figure 5.12 Device power dissipation over operating range at m = 2/3

Chapter 6

6. Heatsink Design

In this chapter the design of a custom heatsink for the SMR is presented. The alternator thermal model developed [3] is used as a baseline of the machine's thermal transfer capability and the device power dissipation profile from Chapter 5 is used to determine the necessary heatsink-to-ambient thermal impedance to ensure safe device operation over the operating range. The structural limitations imposed by the alternator housing and the mechanical interfaces between the heatsink and housing are discussed.

6.1 Heatsink Design Specifications

The final design element needed for the rewound machine is a heatsink. The purpose of the heatsink design is to generate a practical mechanical design that satisfies the packaging requirements and ensures safe operation for ambient temperatures up to 85°C. To achieve this we apply the alternator thermal model from [3] and use the device power

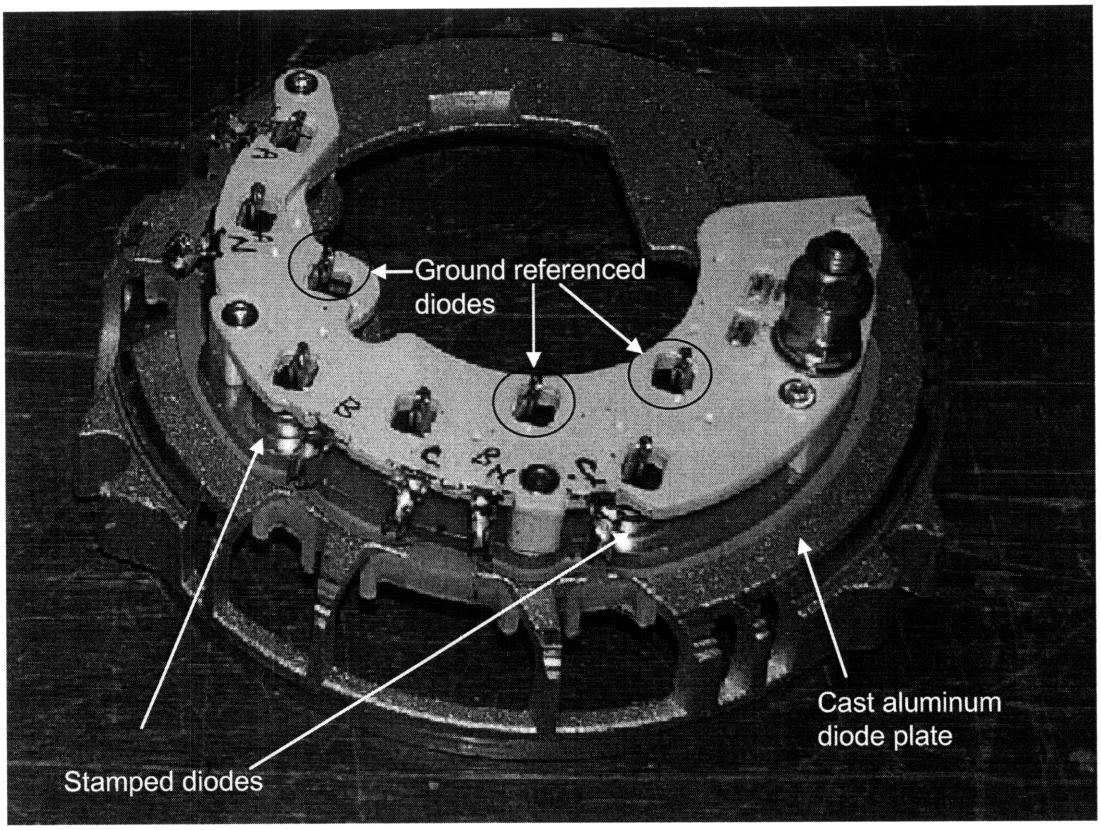

Figure 6.1 Diode plate structure

dissipation profile from Figure 5.12.

In [3] the thermal impedance with respect to ambient was established for the stator winding, diode plate, and alternator case. The diode plate with full bridge rectifier is shown in Figure 6.1. The rectifier diodes are shown hard stamped into the bus bar on the front side of the structure. The ground referenced diodes are hard stamped into the cast aluminum structure just beyond the bus bar. This cast aluminum structure is the diode plate. In the final design the bridge rectifier is removed and replaced with a custom built heatsink that sits on top of this diode plate. The experimental data in [3] showed that the thermal impedances with respect to ambient in the alternator improved at higher operating speeds allowing for more efficient operation when the power dissipation in the windings and diodes would be at its greatest. This is also evident in Figure 4.5 which plotted the temperature winding over the operating range.

The thermal characterization of the diode plate is used as an initial starting point

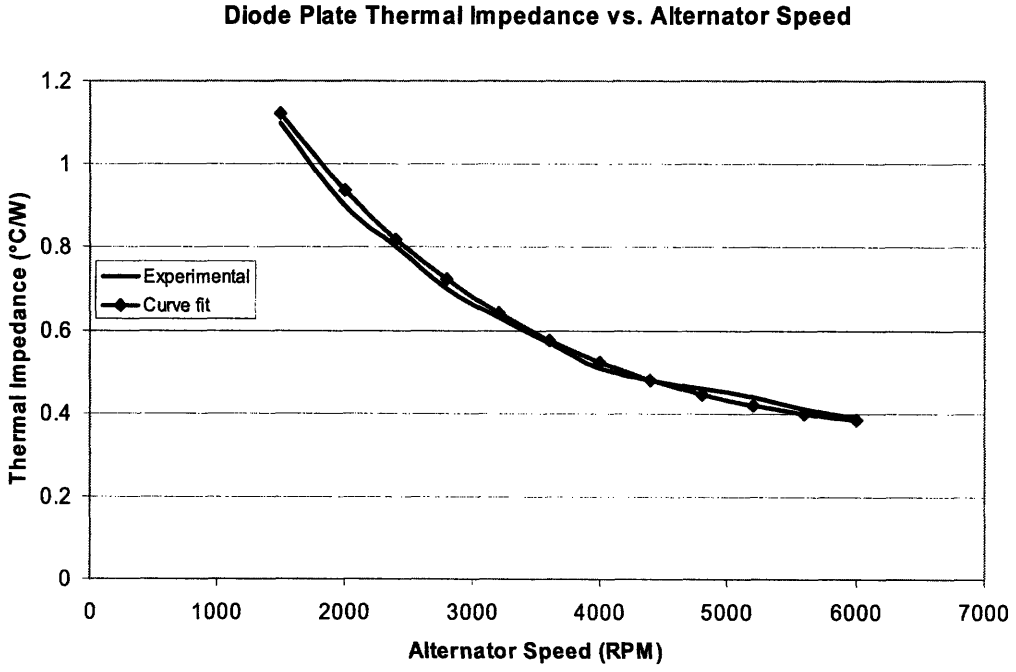

Figure 6.2 Diode plate to ambient thermal impedance with curve fit expression [3]

to determine the worst-case heatsink-to-ambient thermal impedance. Figure 6.2 plots the experimentally-obtained diode-plate-to-ambient thermal impedance over the operating range. A curve fit expression,

$$R_{th} = 2*\left[\exp\left(-\frac{5\omega}{\pi}*4.2x10^{-4}\right)+\left(\frac{5\omega}{\pi}\right)*1.87x10^{-5}\right] \quad (6.1)$$

where ω is the rotational speed of the alternator shaft, was generated and plotted alongside the experimentally obtained data to show relative accuracy of the expression. This expression can be manipulated to show what level of improvement is needed to ensure safe operation up to 85°C.

Working with the assumption that the custom heatsink will have *the same* thermal impedance to ambient as the diode plate, the power dissipation profile from Figure 5.12 is used to determine the device junction temperatures over the operating range. This device

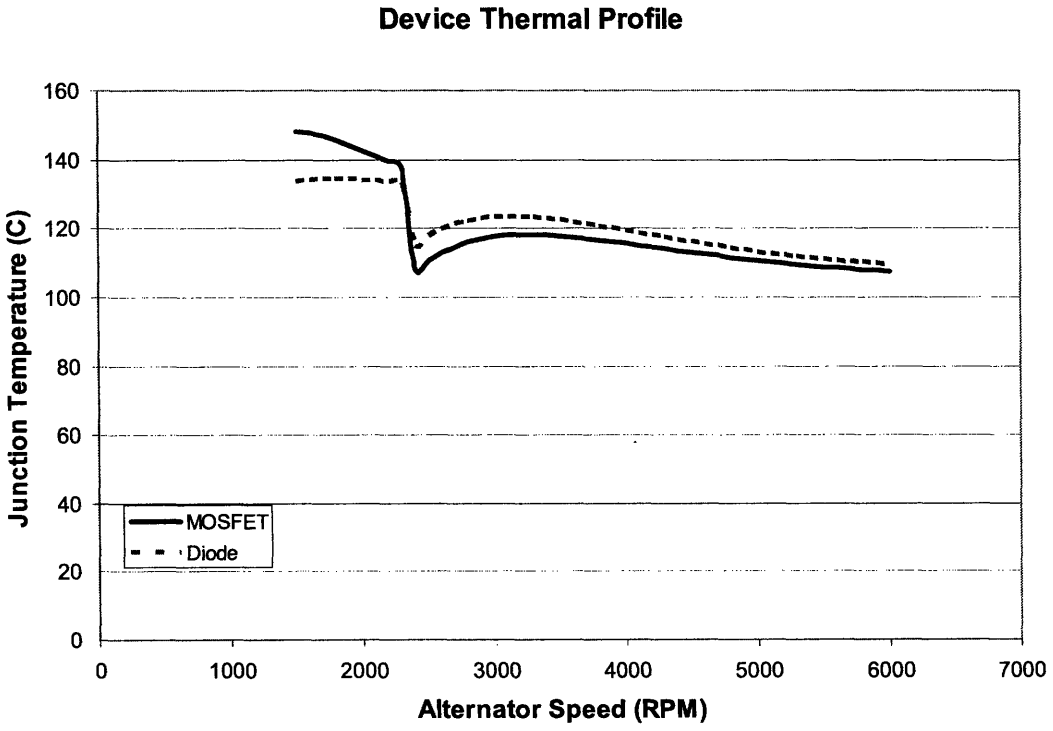

Figure 6.3 Device thermal profile at ambient of 25°C

thermal profile is presented in Figure 6.3. The plot shows that the device junction temperature for both the FET and the diode approach the de-rating temperature at lower operating speeds in a 25°C ambient environment. This is not entirely unexpected because of the MOSFET operation as a boost switch and the diode plate having higher thermal impedances at lower operating speeds. At higher speeds the devices are within the de-rating limits.

Based on Figure 6.3, the heatsink has to improve on the diode plate to ambient thermal impedance in order for the devices to operate reliably in an 85°C environment. One way that this improvement can be realized while still meeting the packaging requirements is to utilize the vertical spacing provided by the rectifier diodes in figure 6.1 and incorporate a finned heatsink into this area.

Because of the mechanical and packaging requirements, the total height availability for the heatsink and PCB was about 850 mils. The PCB required approximately 350 mils of clearance for the surface mount devices and thus 500 mils was the available heatsink height. Another mechanical requirement of the heatsink was that

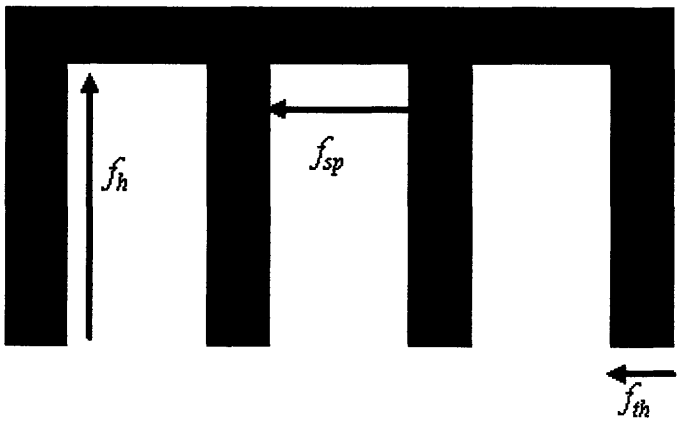

Figure 6.4 Labeled heatsink structure

the fins must be spaced so that the airflow paths lie directly in the vented openings of the alternator cover. These vented openings are approximately 160 mils wide with about 160 mils of covered space in between each opening. This dictates that the fin thickness f_{th} and the fin spacing f_{sp} must be equal to 160 mils which leaves two unknown design variables; fin height f_h and number of fins n.

The two remaining design variables were determined by calculating the effective area increase using the approximation that the heatsink is rectangular. Consider the heatsink shape with labeled fin characteristics in Figure 6.4. The effective heat sink area A_{hs} is

$$A_{hs} = (n-1)f_{sp} + 2(n-1)f_h \tag{6.2}$$

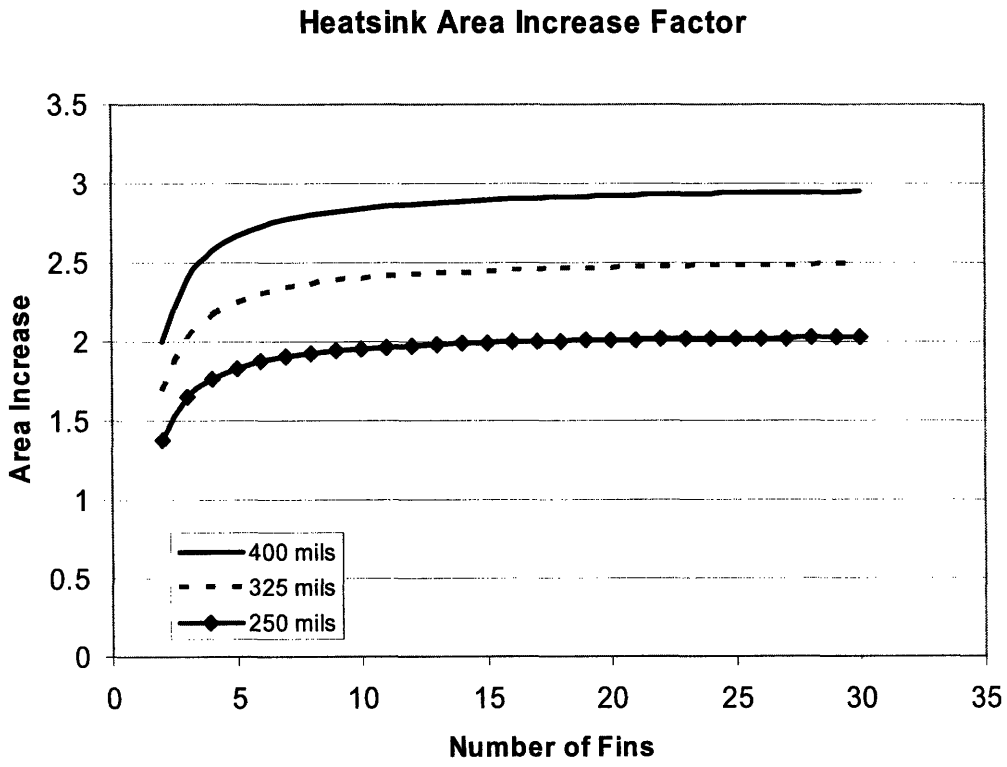

Figure 6.5 Heatsink area improvement factor at different fin heights

where n is the number of fins. Assuming that the diode plate structure is flat with no extrusions, the diode plate area A_{dp} can be expressed as

$$A_{dp} = (n-1)f_{sp} + nf_{th} = (2n-1)f_{sp}. \tag{6.3}$$

Using (6.2) and (6.3), the ratio of heatsink area over diode plate area $\frac{A_{hs}}{A_{dp}}$ can be plotted at varying fin heights to estimate how many fins would be needed to reach a point of diminishing returns. This plot is shown in Figure 6.5. The number of fins can then be compared to the available space to see whether or not that design would satisfy the packaging requirements.

The area calculations of (6.2) and (6.3) didn't account for fin inefficiency or fringing area and thus the heatsink-to-ambient thermal impedance will not necessarily improve at the same ratio as the area increase. Nonetheless, Figure 6.5 provides a proportional improvement factor and an indication of the thermal capabilities of a finned heatsink exposed to the volumetric airflow provided by the alternator cooling fans. The packaging requirements limited the total number of fins to 20-25 and so a fin height of 400 mils was chosen in hopes of achieving somewhere close to 3x improvement in thermal efficiency.

Figures 6.6 and 6.7 on the following pages show different views of the finished heatsink which was fabricated from copper using wire EDM. Figure 6.6 shows the heatink fin-side up and next to a ruler. This is done to show the fin spacing and the approximate area taken up by the heatsink. The heatsink can essentially fit into a 4" square box and is only 500 mils in height. This is a total volume of 8 cubic inches. It is also worth mentioning the tapering of the fins. Both the fin thickness and the fin spacing decrease as they approach the center. This was done to provide for easier manufacturing

of the part and optimal space utilization. Figure 6.7 shows the heatsink bolted down onto the diode plate. This is a good view for comparison with the original diode plate in Figure 6.1, and shows how that space was utilized to provide for better thermal performance.

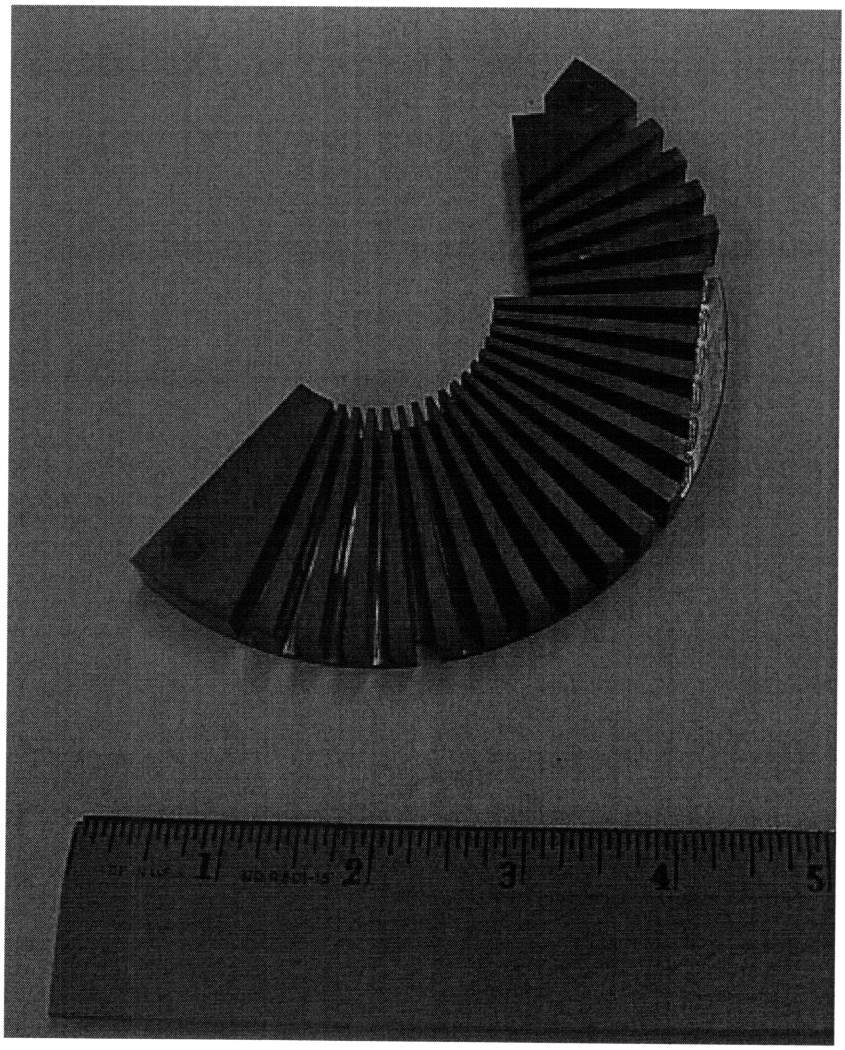

Figure 6.6 Upside down heatsink next to ruler

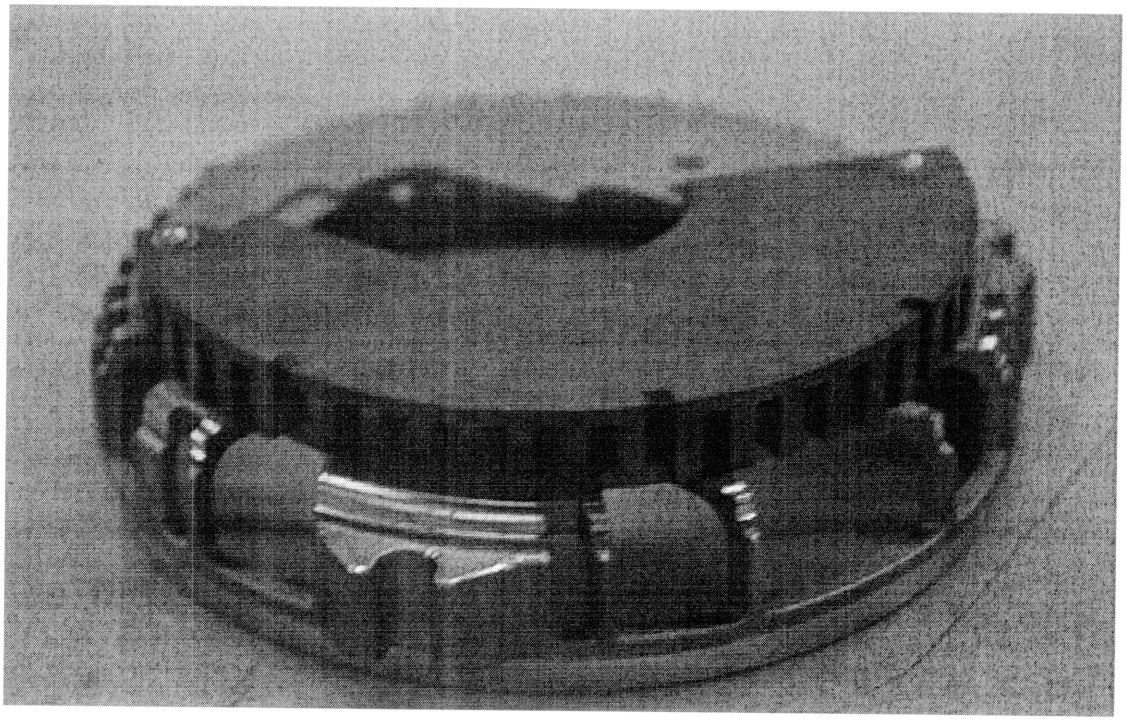

Figure 6.7 Heatsink on diode plate

Chapter 7

7. Implementation of Control Strategy

In this chapter a simple control strategy for the SMR is discussed and implemented with the use of a microcontroller. Basic functionality of the microcontroller is introduced and the control elements are discussed with respect to the microcontroller functions. The control functions, which are designed solely for the purpose of validating hardware performance, include a zero-crossing detector, speed sensor, a duty cycle modulator, and synchronous rectification. Oscilloscope captures from the SMR test runs are included. The microcontroller code for implementing the techniques shown here is listed in appendix D.

7.1 Control Theory

The control theory for the SMR-based alternator with load-matching is discussed in some detail in [1]. The design and implementation of such a control loop is demonstrated in [8, 10]. For this project the control circuitry was needed only for hardware validation. Therefore the control design was simplified to demonstrate that the packaged hardware could perform the essential SMR functions and deliver the expected output power. There were four control functions needed to validate the SMR functionality:

1. A zero-crossing detector circuit.
2. A digitally-filtered speed sensor for measuring alternator operating frequency.
3. An operating-frequency-dependent duty cycle modulator.
4. A synchronous rectifier pulse width timer.

7.2 Microcontroller

Before discussing the control functions and how they were implemented, a quick description of the microcontroller is needed to understand its capabilities and how the control functions were incorporated. The microcontroller used for this project is a Microchip PIC18F1230.

7.2.1 Oscillator

The PIC18F1230 comes with an embedded oscillator, so the use of an external crystal oscillator is not necessary. The internal oscillator was chosen because it was a simpler

design approach that saved space, and precision timing was not a necessity. The oscillator was set to operate at its fastest rate of 8 MHz which means that all instruction cycles in the microcontroller are completed in 2 MHz or 500ns. This is an important function as the resolution of the PWM switching frequency can only be realized in increments of 500ns, and all timer functions are in 2^n fractions of the instruction cycle frequency.

7.2.2 PWM Outputs

This device was designed for use in three-phase motor control applications so it has the capability of up to six PWM outputs (PWM0-5). The PWM outputs are primarily commanded by 5 control registers. There are three PWM duty cycle registers (PDC0-2), one override control register (OVDCOND), and one override state register (OVDCONS). The three PWM duty cycle registers each control one pair of PWM outputs. For example PDC0 controls PWM0 and PWM1. The PWM pairs can be set to run in either complementary or independent mode. If the PWM pairs are set to complementary mode then PDC0 directly controls the duty cycle of PWM1 and PWM0 operates with a complementary duty cycle.

When the PWM pairs are set to independent-mode operation, the OVDCOND register is used to determine whether a PWM output is controlled by its respective duty cycle register or its respective bit in the override state register. The OVDCOND and OVDCONS registers carry a bit for each of the six PWM outputs. When a PWM bit is set in the OVDCOND register the PWM is controlled by its respective duty cycle register. When a PWM bit is cleared in the OVDCOND register the PWM is controlled by its respective OVDCONS bit. These functions are utilized in the SMR to control duty cycle modulation and synchronous rectification.

7.2.3 Timer Functions

The microcontroller has two timer functions. Timer functions are basically software registers (TMR0 & TMR1) that increment every 2^n instruction cycles. Timers are simple but useful functions because they allow the processor to operate control elements at set intervals and can be used to measure a timing period or operating frequency that is considerably slower than the microcontroller oscillator speed. The timer registers are linked to interrupt flags which are set when a timer register overflows. These functions are incorporated in the SMR control system as a means of sensing the alternator angular speed and also controlling the synchronous rectification pulse width.

7.2.4 Comparator Inputs

The microcontroller is equipped to handle up to three analog comparator inputs with an internal software voltage reference. The comparator input pins are tied to the non-inverting node of the comparator and the voltage reference is tied to the inverting pin which is internal to the microchip. The comparator output pin is also internal to the microchip and is read as a digital bit on a control register. Each of the comparator outputs is linked to a corresponding interrupt flag which is set on any comparator change of state. The comparator state register must be read *and* the flag must be cleared in software to avoid false triggers. The three comparators are utilized in the SMR to indicate whether each phase is in its positive or negative current half cycle.

7.2.5 Software Interrupts

For this application the most important function of the microcontroller is the software interrupt capability. Software interrupts are subroutines that take precedence over the primary software routine. The PIC18 family is equipped with the ability to operate high priority and low priority interrupts. Both interrupts take precedence over the primary

software routine and the high priority routine takes precedence over the low priority routine. When an interrupt is triggered, a flag is set in one of the control registers. This flag must be cleared in software to avoid successive interrupts. Interrupts can be triggered by any number of events including the completion of a PWM switching cycle, a timer register overflow, and a comparator change of state. When the event occurs, the software address marker jumps to a predefined address referred to as a vector. The code within this vector is immediately executed and must be ended with a specific return from interrupt command. The address marker then jumps back to the line of code just prior to the interrupt.

7.3 Control Functions

7.3.1 Zero-crossing Detector

The zero-crossing detector is implemented by using the microcontroller comparators with a low reference voltage. It is the most important function of the control scheme because the other three functions are triggered to respond to the comparator trip. The detector is implemented using the circuit in Figure 7.1, where Q_x and D_x represent one boost switch set of the three-phase SMR and the comparator is internal to the microcontroller as discussed in 7.2.4. The resistors, capacitors, and zener diode are external components designed to filter and average the voltage at node V_x and protect the microcontroller from transient spikes.

Each of the three phases has the same comparator circuitry monitoring the MOSFET drain voltage. The comparator change of state interrupt is also enabled on each of the three comparators. When an interrupt occurs the subroutine polls the interrupt flag

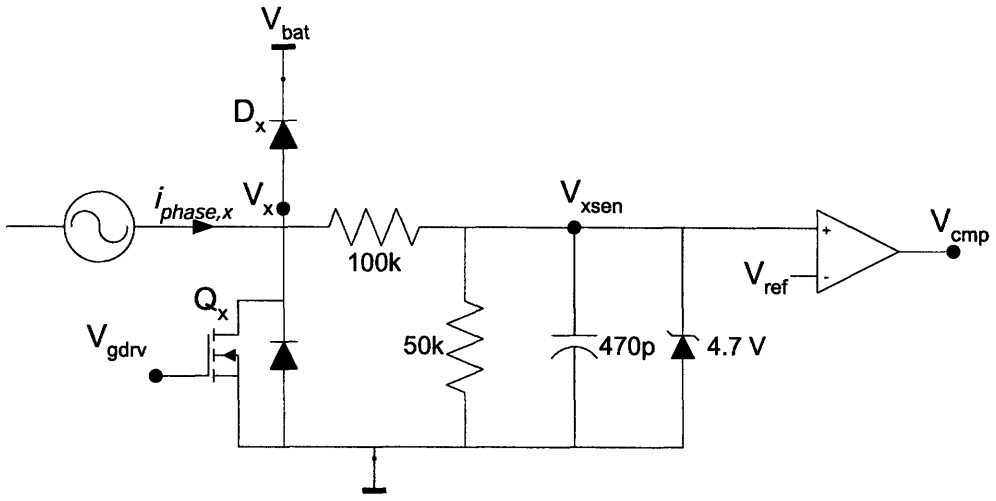

Figure 7.1 Zero-crossing detector circuit

register to see which of the three phases caused the interrupt. The interrupt routine then digitally filters and averages the timer counts to safeguard against false triggers. Finally the comparator output bit is read to determine whether the interrupt was caused by a positive going or negative going comparator trip. The comparator output bit is cleared after being read and the interrupt routine proceeds to a subsequent operation depending on the phase polarity.

7.3.2 Speed sensor

The alternator speed sensor is implemented by using a timer function with a 1:64 prescaler. This means that the timer register, TMR0, increments one count every 64 instruction cycles or 32μs. This was the simplest approach to use as it only needed one 8-bit register with no overflow to account for the entire alternator operating range, and provided for high resolution at low operating speeds. The low speed resolution is important because the SMR is operating in a load-matched condition at these speeds so the microcontroller must have the resolution and hysteresis to differentiate between speeds in order to set the appropriate duty cycle.

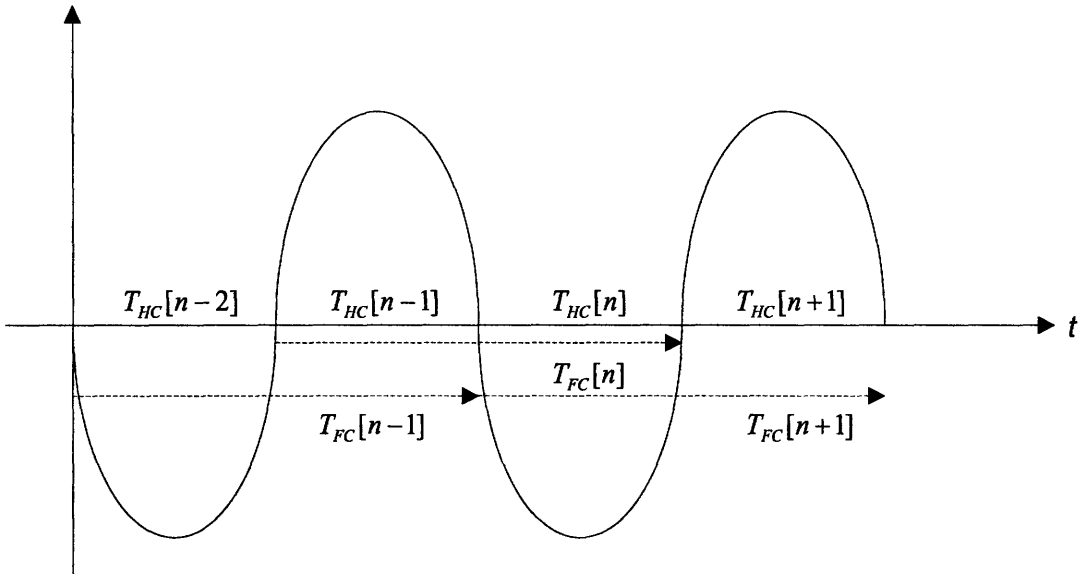

Figure 7.2 Speed sensor filter pattern

The speed sensor software routine is a high priority interrupt routine triggered off of the comparator trip interrupt. The routine can be best understood by referencing Figure 7.2. Figure 7.2 is a generic sinusoidal waveform with four discrete periods referred to as [*n* - *2*] through [*n* + *1*]. Each period has an associated number of timer counts referred to as *T[n-k]* and a subscript, *HC* or *FC*, to denote half-cycle or full-cycle timer counts. Suppose that an interrupt occurred just after period [*n*]. The number of timer counts $T_{HC}[n]$ in the TMR0 register at the time of the interrupt is placed in a holding register so that the TMR0 register can be cleared and begin incrementing again.

When the interrupt after period [*n*] occurs, information about period [*n* + *1*] needs to be calculated to so that the microcontroller can command the next PWM operation. This information is obtained by filtering and averaging known data. The filtering process chain is carried out as follows

$$T_{FC}[n] = T_{HC}[n] + T_{HC}[n-1]. \tag{7.1}$$

Next, verify that

$$T_{FC}[n-1]-5 \le T_{FC}[n] \le T_{FC}[n-1]+5\,. \tag{7.2}$$

If true then

$$T_{FC}[n+1] = \frac{T_{FC}[n]+T_{FC}[n-1]}{2} \tag{7.3}$$

$$T_{HC}[n+1] = T_{FC}[n+1]-T_{HC}[n]\,. \tag{7.4}$$

The step in (7.1) determines the most recent full cycle timer counts $T_{FC}[n]$ based on known data. In (7.2) this dataset is compared against the previous full cycle dataset $T_{FC}[n-1]$ to make sure that the two most recent full cycles are within 5 timer counts of each other. If this is not the case, then no PWM operation is performed. The full cycle information for the $[n+1]$ period is computed in (7.3) as the average of the two most recent full cycles which is a running average of the last 3 half cycle periods. Finally in (7.4) the half cycle data for the $[n+1]$ period is computed by subtracting the known half cycle data of period $[n]$ from the averaged full cycle data.

After the data for period $[n+1]$ is calculated, the data from the period $[n]$ holding registers is preserved in the $[n-1]$ holding registers. All PWM actions in the $[n+1]$ period are commanded based on the computations made in (7.3) and (7.4). When an interrupt occurs following the $[n+1]$ period, data for the $[n+2]$ period is computed based on the running data from the $[n+1]$ and $[n]$ periods.

The data averaging and filtering is done to ensure the integrity of the timer counts. Timer counts that lead to a large discrepancy between the two most recent full cycles don't result in an immediate PWM operation, and keeping a weighted average of the two most recent full-cycles ensures that a false trigger does not dominate the expected $[n+1]$ data. If the filtered speed sensor data commands a PWM operation, then the comparator output bit is read to determine whether the interrupt was a positive-going or negative-

going trigger. If it is a positive-going trigger then the routine proceeds to calculate the modulating duty cycle and if the trigger is negative-going the routine sets the synchronous rectification pulse width.

7.3.3 Speed Dependent Duty Cycle Modulation

At lower alternator speeds the maximum power operation for the machine is achieved in the load-matched state. To operate in this state a software routine is needed to modulate the MOSFET switches at some predetermined duty cycle proportional to the alternator speed. The software routine utilizes the averaged full cycle [$n + 1$] period data computed by the speed sensor routine to achieve this goal.

The computational model developed in chapter 4 calculated the optimal duty cycle at each operating speed. The duty cycle periods were then preloaded as bytes of data into an addressed table in the software code. When the full cycle timer counts for the [$n + 1$] period are computed the number of counts is used to specify an address for the table pointer, which is the mechanism for extracting data out of the table. The table pointer selects a specific duty cycle data byte from the addressed table and places that byte into a holding register. As a means of rejecting incorrect data, the information in the holding register is compared against a predefined maximum duty cycle. If the holding register contains a duty cycle period longer than the maximum duty cycle, then the PWM duty cycle register is left unchanged and the old duty cycle period is used to modulate the MOSFET in the [$n + 1$] period. Otherwise, the new duty cycle period is placed into the PWM duty cycle register and that value is used to modulate the MOSFET.

The maximum duty cycle limit is an important safety measure to ensure that the alternator does not fall into a destructive operating state. If a corrupt dataset from the speed sensor filter routine is used to calculate duty cycle, it is possible that the dataset

could specify a table pointer address that is out of range of the table. If this occurs, an invalid duty cycle period may be stored into the table latch and could result in excessive power dissipation in the MOSFET. Furthermore, if the duty cycle on period were selected greater than the MOSFET switching period ($d > 1$) then the alternator would enter into an irrecoverable state and result in destruction of the MOSFET switch.

7.3.4 Synchronous Rectification Pulse Width Timer

The final control element needed to validate the SMR hardware is a synchronous rectification pulse width timer. Synchronous rectification works by turning the MOSFET on when the phase current is in its negative half cycle so that the phase current can return from the battery negative terminal to the phase through the MOSFET's conduction channel (see figure 7.1). This is more efficient than using the MOSFET's body diode or a schottky diode as a return path.

Considering figure 7.1, when the phase current $i_{phase,x}$ first enters its negative half cycle it will return to the source through the MOSFET body diode, and the voltage V_x will go negative with respect to the ground potential. This initiates a negative-going comparator trip interrupt and subsequent speed sensor routine. During the speed sensor routine, the value of $T_{HC}[n+1]$ is computed as shown in (7.4). The $T_{HC}[n+1]$ data in combination with the second timer function and the PWM override capability is used to control the synchronous rectification pulse width.

The half cycle timer counts are placed in a holding register and the bits are right-shifted three times. This effectively divides the total number of timer counts by eight. The synchronous rectification pulse width T_{RTN} is then set with this computation:

$$T_{RTN} = T_{HC}[n+1] - \frac{T_{HC}[n+1]}{8} - 0x02. \tag{7.5}$$

where *0x02* is two timer counts. The purpose of setting the pulse width in this manner is to allow for more precise comparator interrupts and to prevent the possibility of the alternator entering a self-destructive state. Leaving the MOSFET on for the duration of the negative half cycle prevents the MOSFET drain voltage from ever going above the comparator trip point and thus prevents a positive trip interrupt. The computation in (7.5) allows the PWM to enter back into a modulating or turned-off state prior to the line current crossing back into its positive half cycle. The comparator interrupt then has a more immediate response to the positive going interrupt which allows for more precise timing and ensures that an interrupt occurs.

The PWM override and second timer function are also used in the synchronous rectification routine. The PWM OVDCOND register overrides the PWM duty cycle register so that the PWM output can be controlled by the OVDCONS register which is preset to an "all-on" condition. This method allows the MOSFET to be turned on for the duration of T_{RTN} without having to alter the data stored in the duty cycle register.

The second timer function is set to trigger a low priority interrupt whenever its register overflows and is set to increment 1:1 with the instruction cycle frequency. The TMR1 register is preset so that an interrupt occurs every time the TMR0 timer increments one count. The low priority interrupt routine then decrements the value of T_{RTN} until the value of that register becomes zero. When the value of that register equals zero, the PWM OVDCOND register is cleared and the PWM returns to nominal duty cycle control.

7.4 Oscilloscope Waveforms of Control Functions

Oscilloscope captures from the SMR are presented here to demonstrate the control functions described above. These waveforms will reference Figure 7.1, particularly the

gate drive voltage V_{gdrv}, the comparator input voltage V_{xsen}, and the comparator output voltage V_{cmp}. One important thing to note regarding the waveform captures is that the comparator output is internal to the microcontroller and not directly accessible through hardware. The method to capture this waveform was to mirror the output bit in the software register to an unused digital output pin on the microcontroller.

The first capture in Figure 7.3 is an overview of the gate drive voltage, comparator output, and synchronous rectification at 1500 alternator RPM. This is a good capture as an overview because it shows all of the essential functions. The comparator output, V_{cmp}, is initially high (indicating positive phase current) so the PWM output is modulating. The duty cycle is not distinguishable at this point because the MOSFET switching frequency is so much faster than the alternator operating speed. When the

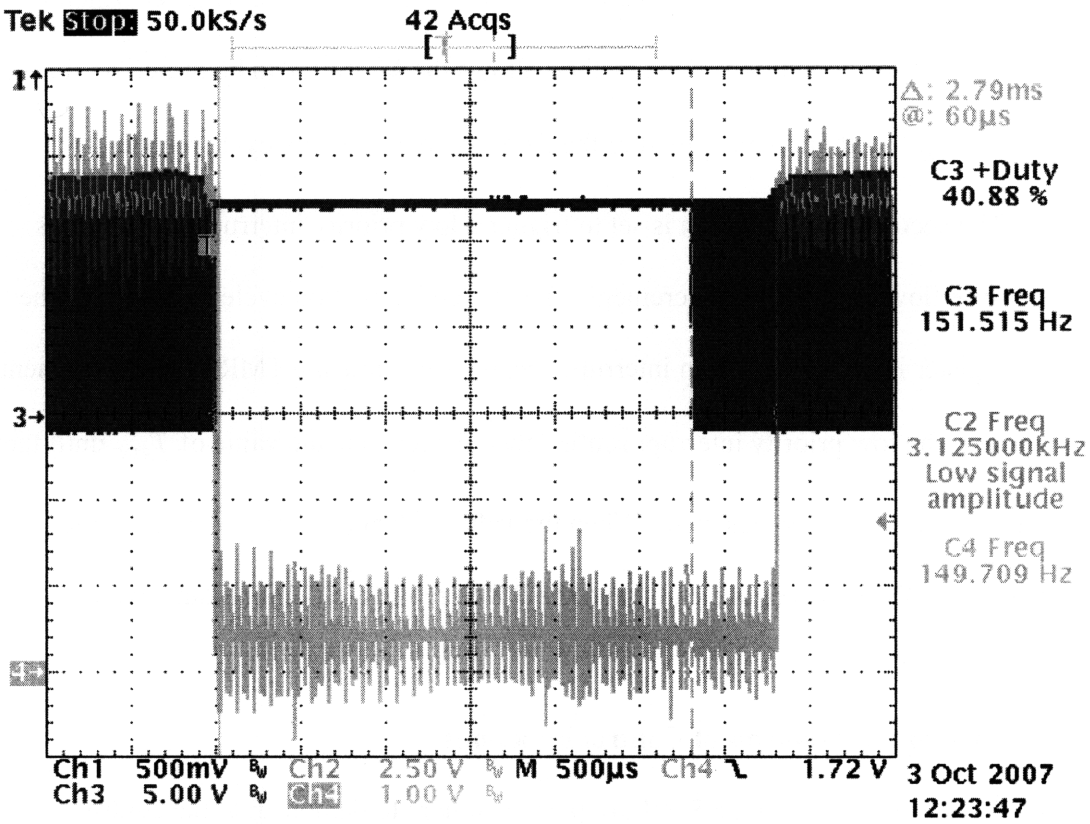

Figure 7.3 Waveform capture of gate drive voltage (Ch. 3, 5 V/div) and comparator output (Ch. 4, 1 V/div) at 1500 RPM.

comparator output voltage drives low (indicating negative phase current), the MOSFET gate drive, V_{gdrv}, turns on almost instantaneously and stays high. The MOSFET then returns to duty cycle modulation, marking the end of the synchronous pulse width, prior to the comparator output going high again.

The next capture in figure 7.4 shows the comparator input and the comparator output at 1500 alternator RPM. The comparator input shows the averaged voltage at the V_{xsen} node of figure 7.1 and the comparator output shows how the comparator responds to the input. This is intended to show that the comparator output is behaving accordingly by following the non-inverting input terminal.

Figure 7.5 is a view of the comparator input, comparator output and the gate drive

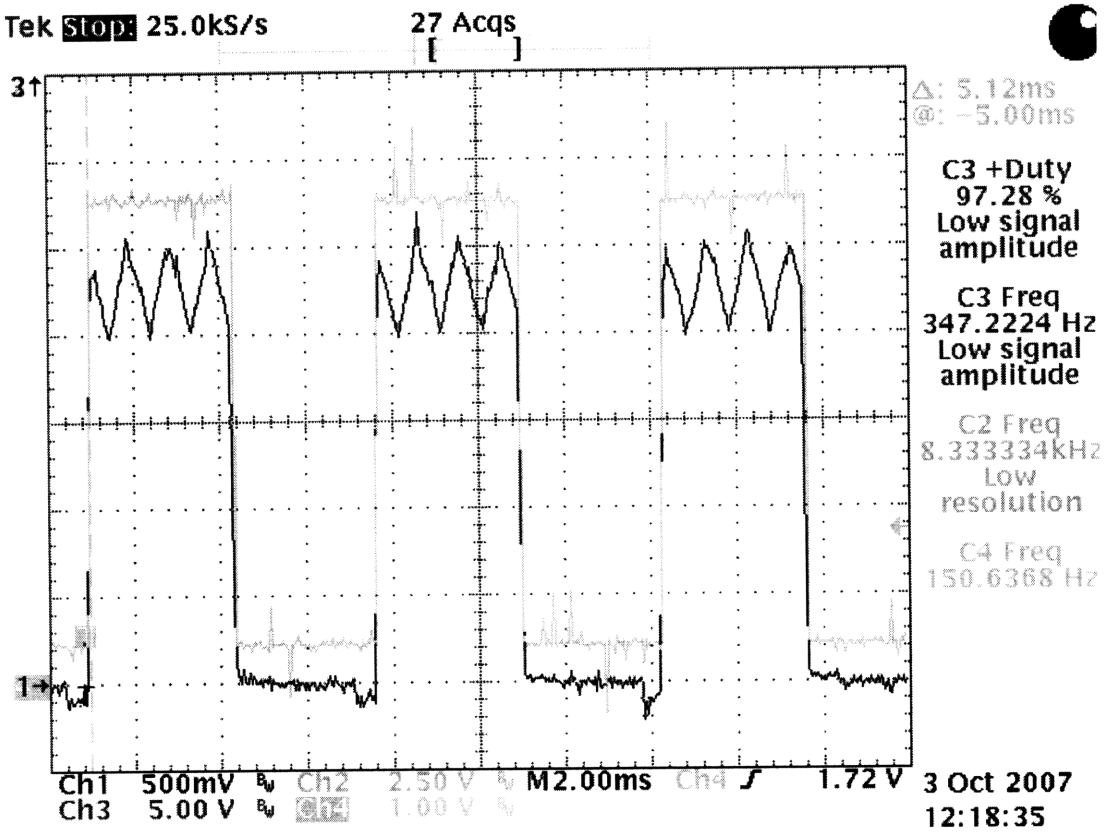

Figure 7.4 Waveform capture of comparator input (Ch. 1, 500 mV/div) and comparator output (Ch. 4, 1 V/div) at 1500 RPM.

voltage. This picture is intended to demonstrate the efficiency gain when the SMR is operating with a synchronous rectification pulse as opposed to using the MOSFET body diode to return current to the source. This picture was taken at around 2450 alternator RPM, just after the SMR left load-matched operation and the MOSFET is no longer modulating.

The relative power dissipation in the MOSFET is seen in this scope capture because the sense voltage, which is the filtered voltage of the MOSFET drain, is shown to increase considerably in magnitude when the MOSFET gate drive goes low and the phase current returns to the source through the body diode.

The final capture, figure 7.6, is an expanded view of the comparator input,

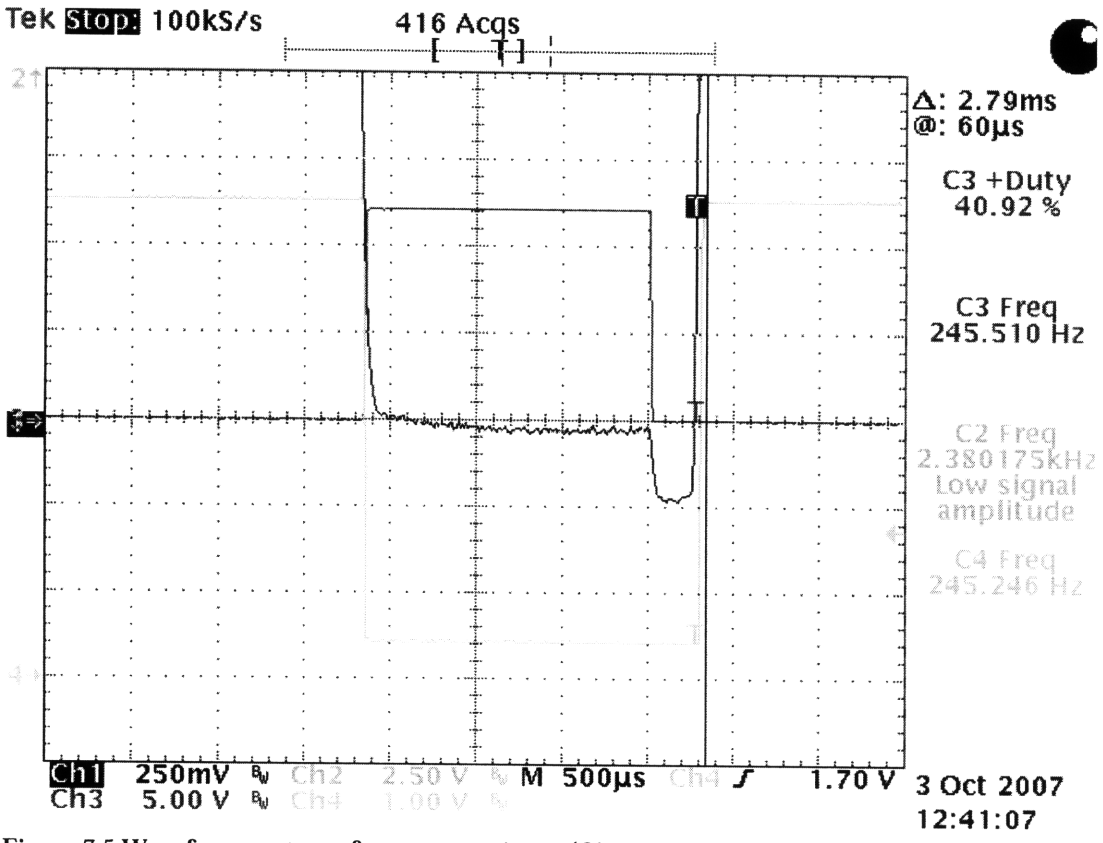

Figure 7.5 Waveform capture of comparator input (Ch.1, 250 mV/div), comparator output (Ch. 4, 1 V/div), and gate drive (Ch. 3, 5 V/div) at 2450 RPM

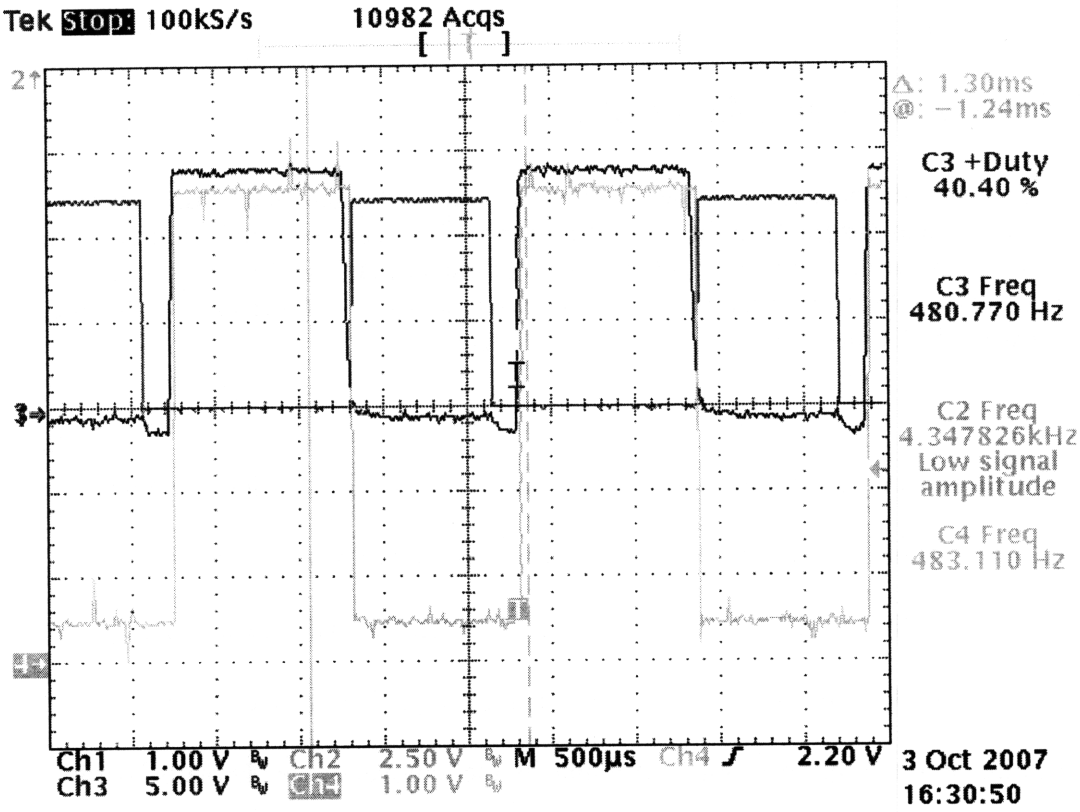

Figure 7.6 Waveform capture of comparator input (Ch. 1, 1 V/div), comparator output (Ch. 4, 1 V/div), and gate drive (Ch. 3, 5 V/div) at 4800 RPM

comparator output, and gate drive voltage during high speed operation. This capture shows the same characteristics as figure 7.5 only at higher speed operation (4800 alternator RPM). Again, the comparator output is operating accordingly as it is following the comparator input. The system is not in load-matched operation and there is no high-frequency PWM, but the MOSFET is still operating as a synchronous rectifier, turning on to return phase current. The comparator input again shows an increase in voltage when the synchronous rectification pulse ends and the MOSFET is off.

Chapter 8

8. Packaging and Assembly

In this chapter the packaging of the rewound machine and embedded SMR circuitry is presented to demonstrate that the new alternator hardware can be fitted within the same housing as the original machine. Photographs of the mechanics and details of the rewound armature, heatsink, and PCB are shown as is a side-by-side view of the fully constructed SMR machine with a commercial alternator.

8.1 Objective

The mechanical layout of the SMR circuit board and its integration into the alternator housing is a complex task encompassing a variety of undertakings. The foremost requirement is that no components are overstressed mechanically, electrically, or thermally. But for the alternator, we adopted an additional goal: We chose to package the entire circuit in the space made available by the removal of the alternator's original diode rectifier, and to use the existing alternator cooling air to cool the SMR circuit.

Every previous implementation (e.g. [8, 10]) of an SMR alternator has, to some extent, required space for the rectifier which was larger than that occupied by the diode rectifier. This complicated the process of before and after comparisons, and left the value of the work vulnerable to the claim that if space limitations are to be relaxed, better alternators can be made without the SMR. By packaging our circuit in the original housing, we can rigorously argue that any improvement is due to the new rectifier, and not the ability to occupy more volume

There are three elements of the SMR-based alternator design that are constrained by the structural limitations of the alternator housing. They are the rewound armature, the custom heatsink, and the printed circuit board (PCB). These three designs will be discussed in some detail with respect to their mechanical constraints.

8.2 Rewound Armature

The packaging constraints for an armature winding are placed primarily on the end-turns which are the segments of the conductor that exit and carry over between the stator slots. There is a height constraint imposed by the diode plate that limits how far axially the end turns can extend beyond the core and there is an area constraint imposed by the housing that limits the thickness of the end-turns. A machine wound stator core from a commercial alternator is shown in Figure 8.1 with the end-turns and termination points labeled. This armature is wave-wound with two parallel conductors per phase as described in Chapter 5. The conductor endpoints in each phase are soldered together resulting in six wire terminations for the three-phase system. All six wire leads are brought up to and terminated directly on the bridge rectifier. The wave winding pattern is advantageous in terms of packaging because the end-turns of parallel conductors lie on

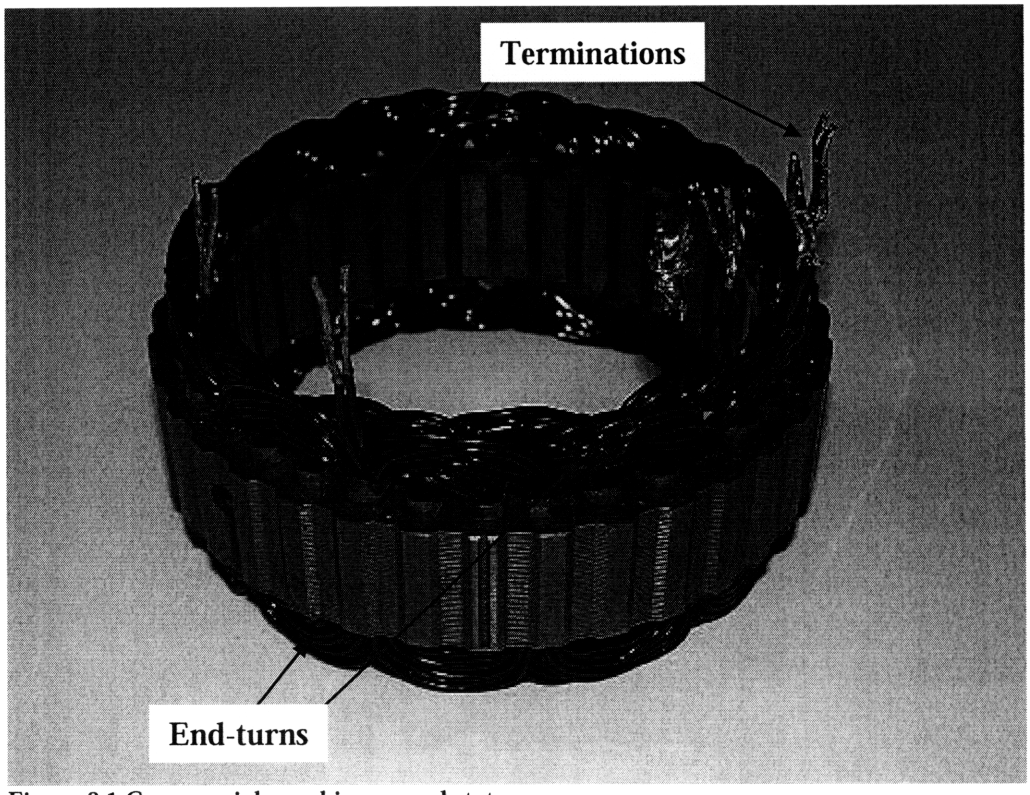

Figure 8.1 Commercial, machine wound stator core

opposite ends of the stator and because there is a limited number of wire terminations, all concentrated in the same area of the core, resulting in limited soldering. The coil-wound armature used for the SMR-based alternator does not have these characteristics.

When the armature was rewound, the coil winding pattern resulted in multiple parallel terminations that needed to be bussed together into three phase leads and a number of neutrals. Each phase consisted of six parallel conductors or twelve terminations. The six conductors are occupying slots around the entire core circumference meaning that the termination points are not concentrated in one area as in the wave-wound core. A pattern was developed to bus the six parallel leads from each

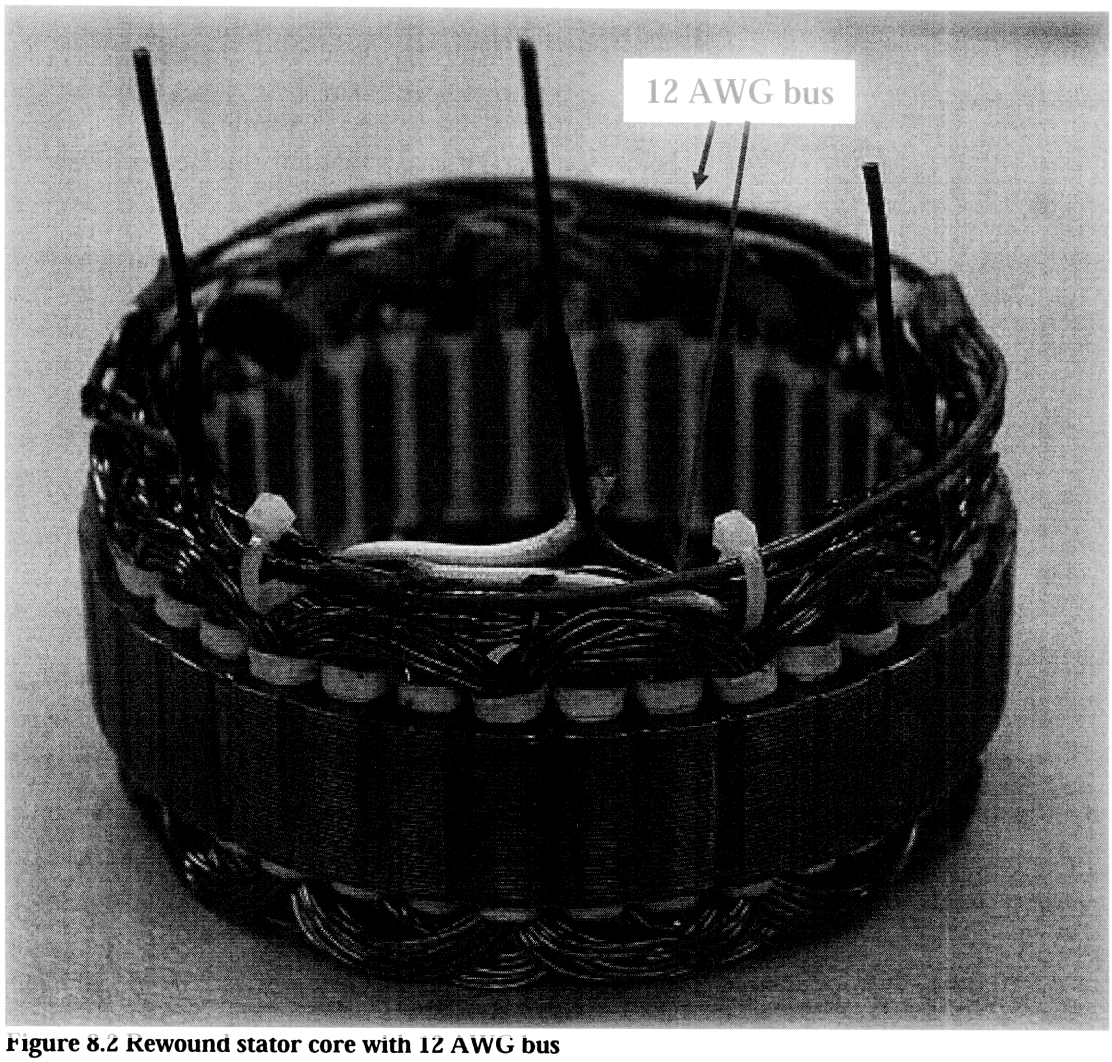

Figure 8.2 Rewound stator core with 12 AWG bus

phase around the core with one 12 AWG conductor that traversed about 270° of the core circumference. The 12 AWG conductor was secured on to the top of the end-turns with tie wraps. The neutral terminations were soldered together in groups of three (one per phase), leaving 6 neutral point connections. These 6 points were not bussed together. The rewound armature used in the SMR-based alternator is shown in Figure 8.2. The figure shows the three phase terminations, each of which is constructed by a 12 AWG bus conductor. One of the bus conductors is labeled at two different points along the circumference of the core to show how the six parallel windings are spread along the circumference.

8.3 Heatsink Packaging

The heatsink design with respect to the thermal efficiency specification was discussed in detail in Chapter 6. The spatial constraints in terms of height allocation and fin spacing were taken into consideration when trying to optimize the thermal transfer characteristics. However packaging the heatsink into the alternator also involved providing a durable ground plane connection between the cast aluminum housing and the PCB, and providing clearance for the three phase connections to extend from the armature and connect to the PCB.

The off-the-shelf alternator that was characterized in Chapter 4 utilized the aluminum housing as a ground conductor to return current from the load to the source. The ground peg where the battery connects to the alternator is a threaded insert on the top cover of the housing. In order to not alter the housing, the same ground peg would be used for the SMR-based alternator. But unlike the commercial alternator, the ground-referenced devices in the SMR are not press-fitted into the housing structure. There needed to be a reliable conductive path between the housing structure and the ground

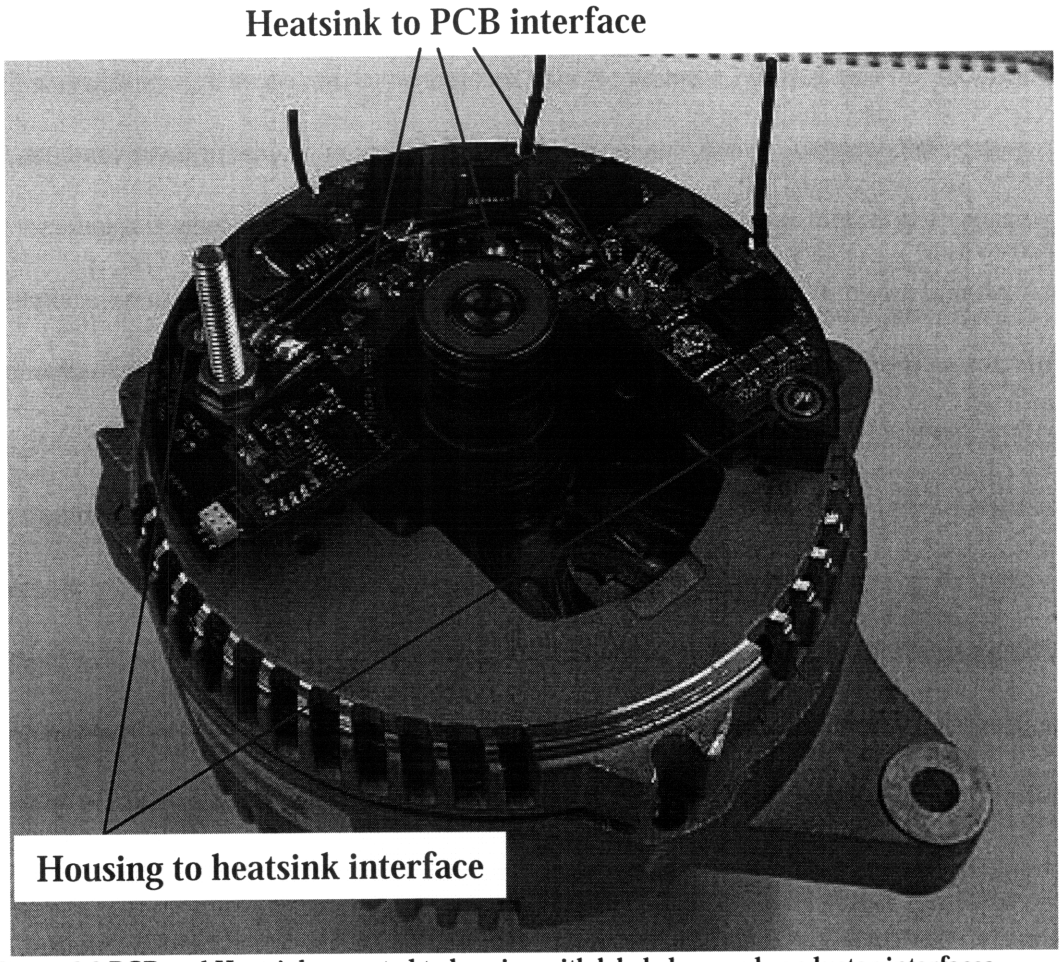

Figure 8.3 PCB and Heatsink mounted to housing with labeled ground conductor interfaces

plane in the PCB. This path required two interfaces, one between the housing and the heatsink, and another between the heatsink and PCB ground plane.

Each of these interfaces was realized with the use of brass screws. The heatsink was designed so that two 4-40 brass screws bolted the copper down onto the diode plate through threaded inserts. The copper heatsink was then threaded at three points, one at each of the three returns on the rectifier. Again, brass 4-40 screws were used as conductors between the heatsink and the PCB ground plane. Figure 8.3 is a back view of the PCB and heatsink mounted on to the diode plate. This figure shows both interfaces and the screws used to provide the return conduction path from the load.

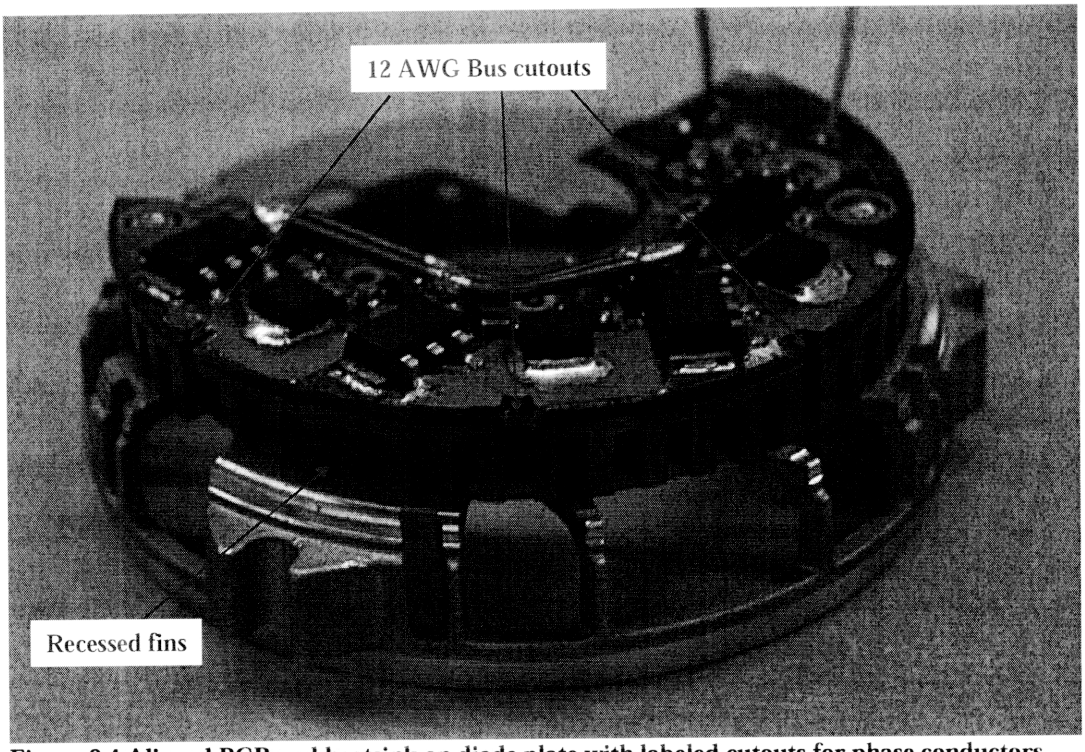

Figure 8.4 Aligned PCB and heatsink on diode plate with labeled cutouts for phase conductors

Figure 8.3 also shows the three phase leads coming up from the armature. What isn't noticeable from this view is that both the heatsink and the PCB were designed with aligned cutouts so that the 12 AWG conductors could be brought up to the PCB without having to extend radially beyond the heatsink surface. Figure 8.4 shows the heatsink and PCB on top of the diode plate from a front view. In this setup the PCB isn't secured into the heatsink but the two are aligned to show the cutout area where the three phase leads come up and solder onto the MOSFET heat spreader. This picture also shows an area where the heatsink fins are recessed back from the end of the heatsink. This is an area where the top cover of the housing is not vented and the recessed fins were meant to provide a low impedance air flow path from nearby venting.

8.4 PCB Design

In addition to the cutouts for the three phase leads and the ground plane interfaces mentioned in the previous section, there were some packaging constraints placed on the

PCB. The primary concerns dealt with the space allocation for all of the necessary devices and the available copper area given the high current application. A top view of an unpopulated PCB is shown in Figure 8.5. This a good view of the board for explaining how the board space was allocated for the power devices and also for showing the thermal via layout that was described in Chapter 3. What is evident in this figure is that the power devices, particularly the MOSFETs and their heat spreaders, take up about 50% of the total board area and are concentrated along the outer edge of the board. The positioning of the devices was done to coincide with the area closest to the vented openings in the top cover. The vented area only traverses about 180° of the diode plate circumference and provides for the most efficient heat exchange.

The control section of the board in the upper right lies in a closed area where there

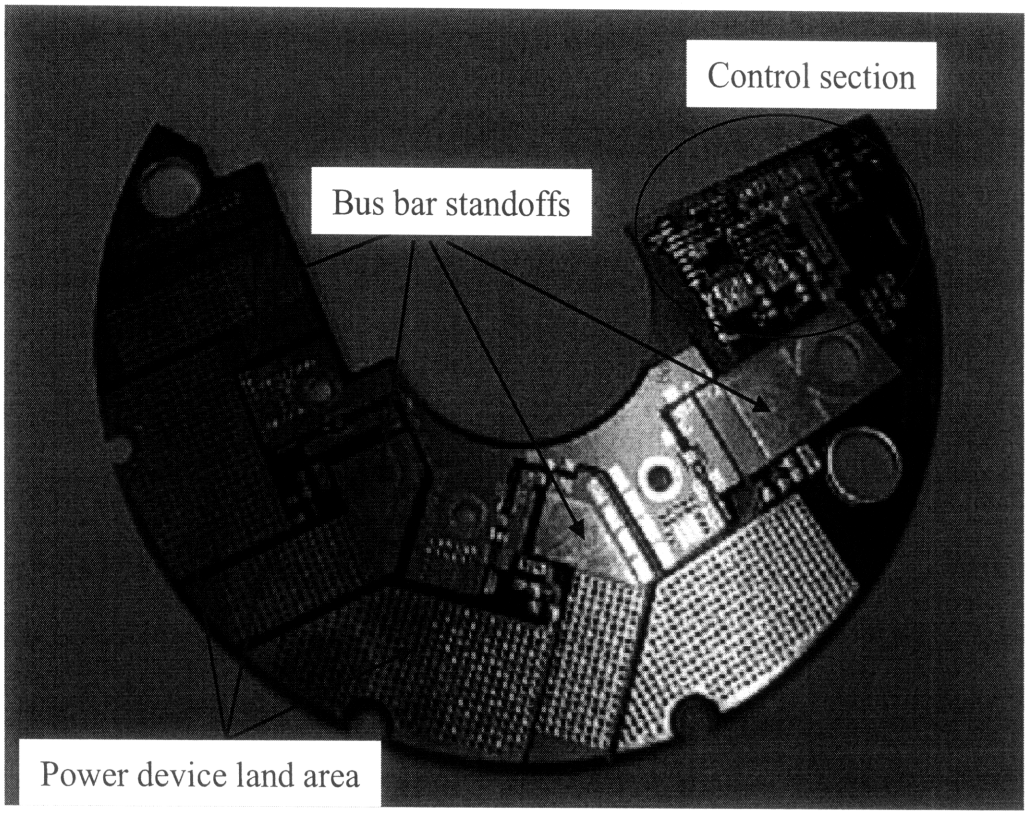

Figure 8.5 Unpopulated SMR PCB

is no direct airflow as these components do not require heatsinking. Also, if close attention is paid to Figure 8.3, one can see that the board overlaps the heatsink, which is cut away directly underneath the control section. This provided for use of the bottom side of the board to mount additional control components such as a field control MOSFET and diode. Although this control application was not implemented with the microcontroller the capability was designed into the board. A bottom view of the PCB is shown in figure 8.6. This view shows the additional field control components on the reverse side of the PCB and also shows the electrically isolating Sil-Pad™ material which was discussed in the thermal design.

Referring back to Figure 8.5, there is another detail about the PCB that is worth

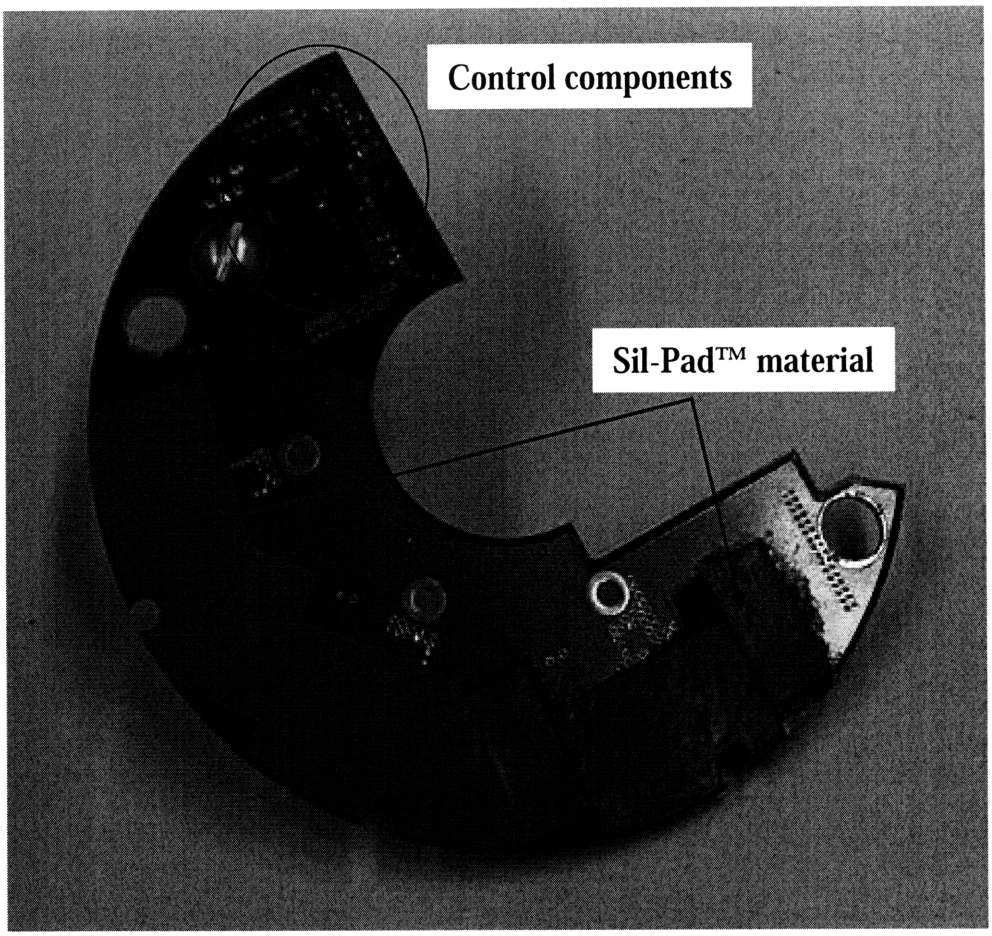

Figure 8.6 Bottom view of PCB with Sil-Pad™ material

mentioning. Because there was a limit on the available copper area internal to the PCB, a bus bar was considered for the output conductor. Placed next to the land area for the Schottky diodes were land areas for copper standoffs onto which a bus bar could be mounted. The intention was to be in close proximity to the cathode of the diode and place a small cube of copper that would make direct contact with the device. This limited the current carried through the internal copper traces. Depending on the thickness of the cube, it also provided enough clearance so that the bus bar could run directly over other surface mount devices. This is shown in Figure 8.7 which is a top view of the fully populated PCB. The bus bar is constructed with two 10 AWG conductors soldered onto the copper standoff at four different points and in position to make direct contact with the

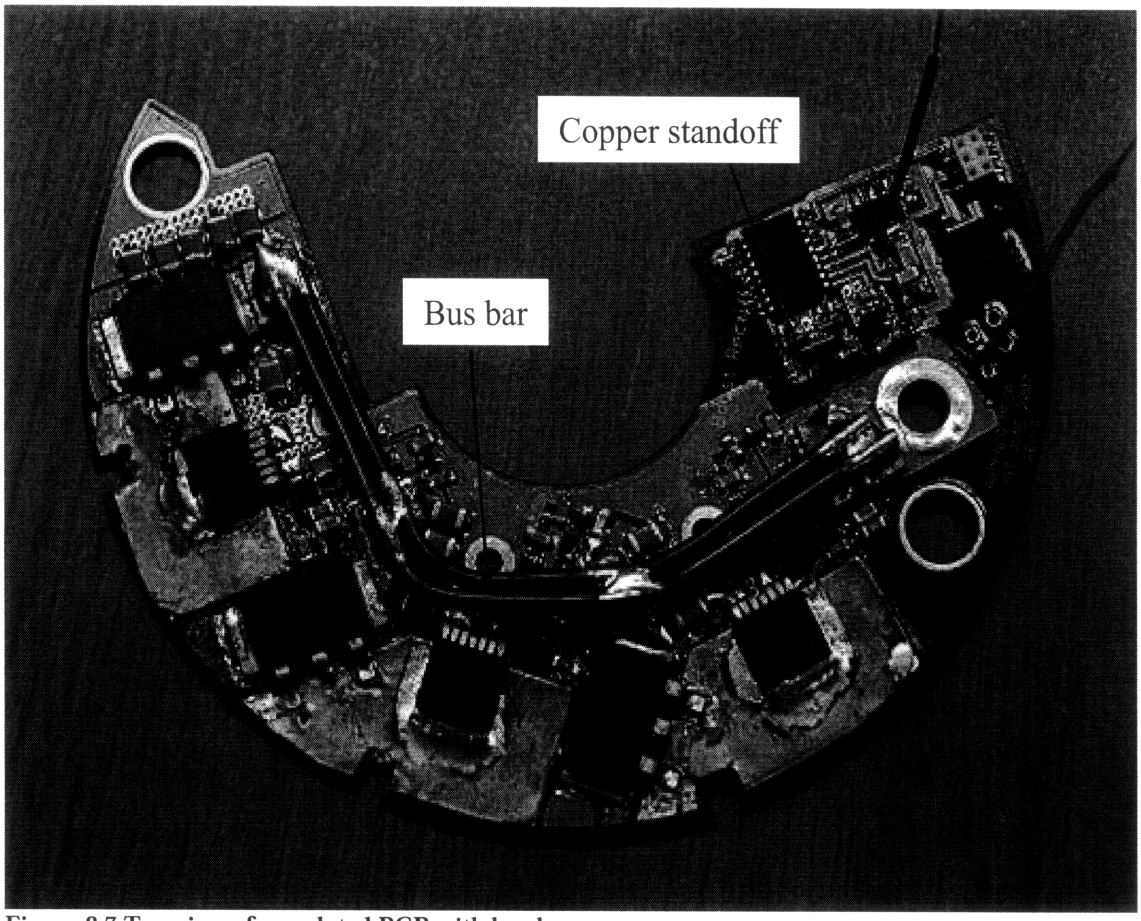

Figure 8.7 Top view of populated PCB with bus bar.

brass output peg. The copper standoffs are thick enough that the bus bar can lie over some of the output capacitors and gate drive circuitry with no risk of shorting or arcing.

8.5 Alternator Assembly

Once the design of the various elements had been completed, the final step was to assemble the machine for testing. Most of the figures in this chapter have already shown the machine in various states of assembly but a brief description of how the machine is assembled is worth mentioning. Figure 8.8, which shows the housing, the inside of the top cover, and the PCB, can be used as a reference.

The rewound stator from figure 8.2 is aligned and placed into the housing. Figure 8.8 shows that the central housing is marked to indicate the proper alignment for

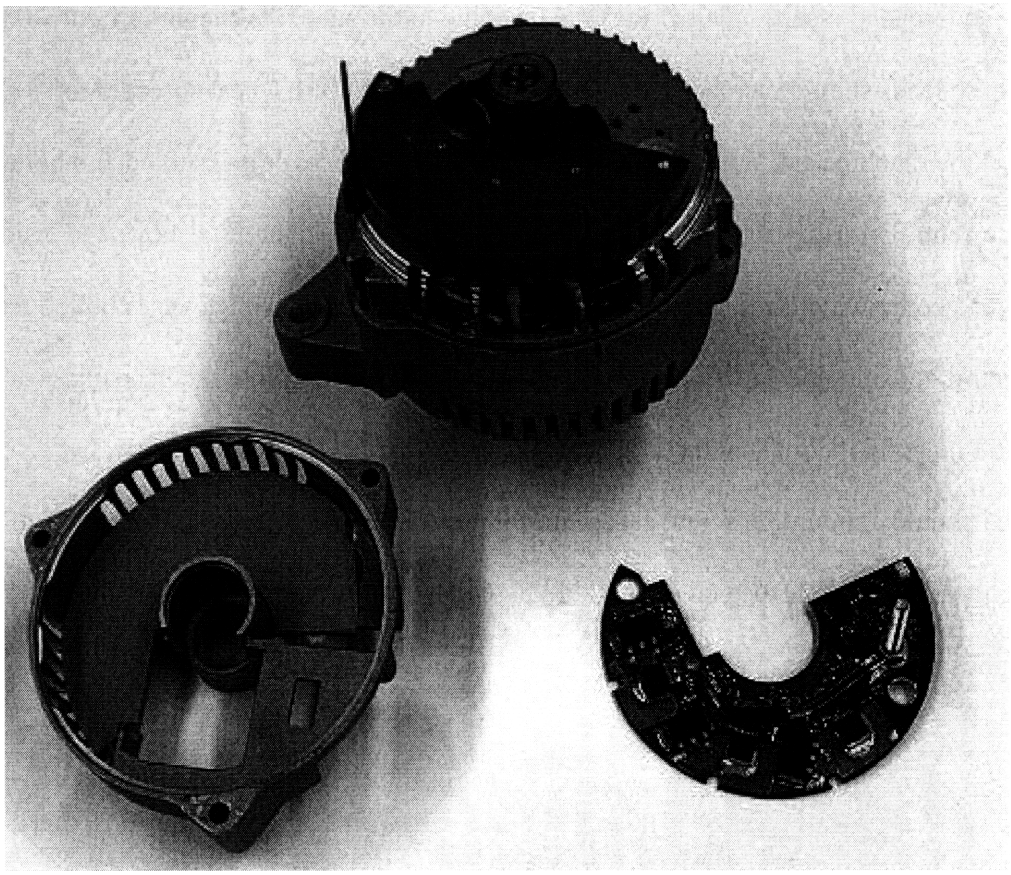

Figure 8.8 Disassembled SMR machine

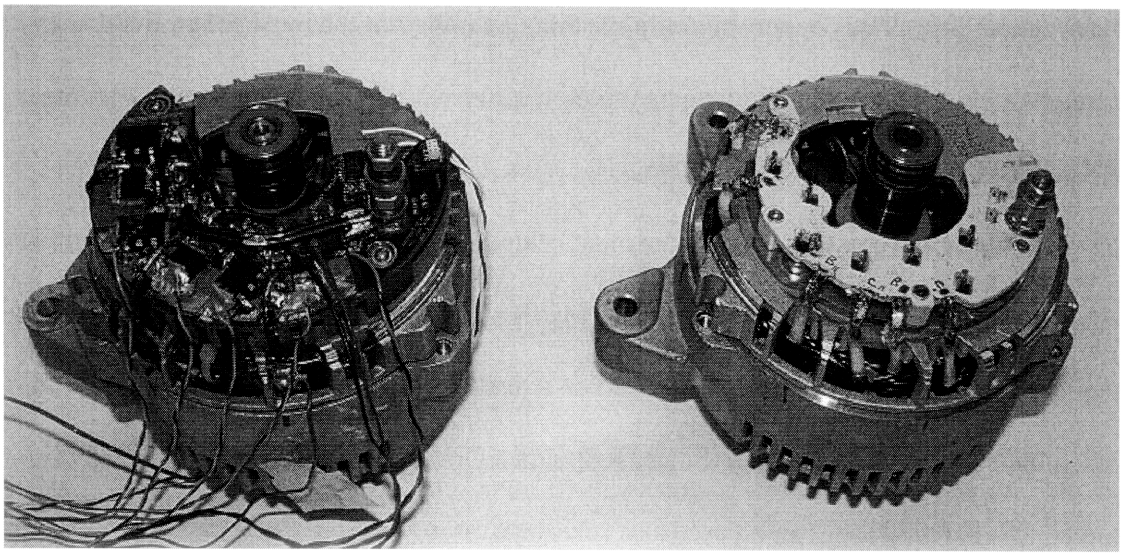

Figure 8.9 SMR machine next to commercial machine

the phase leads. The heatsink is bolted down onto the diode plate which is then aligned and placed on the central housing. The next step is to mount the PCB onto the heatsink using the threaded inserts. This brings the machine to the state it is shown in figure 8.3. The phase leads should then be soldered down onto the MOSFET heat spreader to connect the machine armature to the SMR. Finally, the end cover is installed and bolted into the central housing and the machine is fully assembled. Figure 8.8 shows the inside of the end cover which is lined with a gap-filling pad. When the end cover is bolted into the central housing, the gap-filling material compresses the PCB into the heatsink, providing a good thermal contact. This also ensures that the PCB is mechanically secured should a mounting screw back out. Figure 8.9 shows the fully assembled SMR-based alternator (minus the end cover) side-by-side with the commercial alternator, in an analogous state of disassembly.

Chapter 9

9. SMR Performance Characterization

In this chapter the assembled SMR-based alternator is run through a series of tests to characterize machine performance. The series of tests included measuring the winding resistance to validate the turns ratio and testing the machine output power capability at three field current levels. The experimental results are compared against the expected performance from the analytical models.

9.1 Objective

A series of three design goals were presented in the introductory chapter to outline what was expected of this design effort. Those goals were:

1. Increasing average output power into a fixed 14 V output at the high end operating speeds while maintaining the optimal load-matched power capabilities at lower RPM.
2. Maintaining the improved efficiency provided by the SMR over a wide range of loads.
3. Design for manufacturability; that is working with available off-the-shelf devices and implementing a circuit board layout that will not alter the physical structure or manufacturing practices of a present-day alternator design.

It has been shown throughout this thesis that the third design goal was being met. Commercial off-the-shelf components were selected and characterized in Chapters 2 and 3. Chapter 8 presented pictures of the new alternator verifying that the SMR-based machine is a form-fit replacement of the commercial alternator.

The first two goals have been analytically verified by putting forth electrical, thermal, and mechanical theory as the basis for the design choices of the SMR and the rewound machine armature. But quantitative data is still needed to establish that machine operation is consistent with theory and confirm that these two design goals are being met. Testing similar to the characterization of the commercial machine performed in Chapter 4 should be sufficient to gather the data and verify machine performance.

9.2 Stator Winding Resistance Measurement

Prior to measuring the output power characteristics of the alternator, a winding resistance measurement can be made to verify the accuracy of the turns ratio. Equation (5.2) stated that if both machines achieved the same copper area per turn then the resistance would scale as $R_{s,m} = m^2 R_{s,1}$ where $m = 2/3$. Accordingly, the new machine armature should have 4/9th the winding resistance of the commercial machine if the desired winding is achieved. Using the two machines in figure 8.9, the *line-to-line* winding resistance at different frequencies was measured for each machine with an impedance analyzer. The results are plotted in figure 9.1. The third curve is the $m = 1$ curve multiplied by 4/9. This is the ideal value of the rewound armature if the only difference between the two

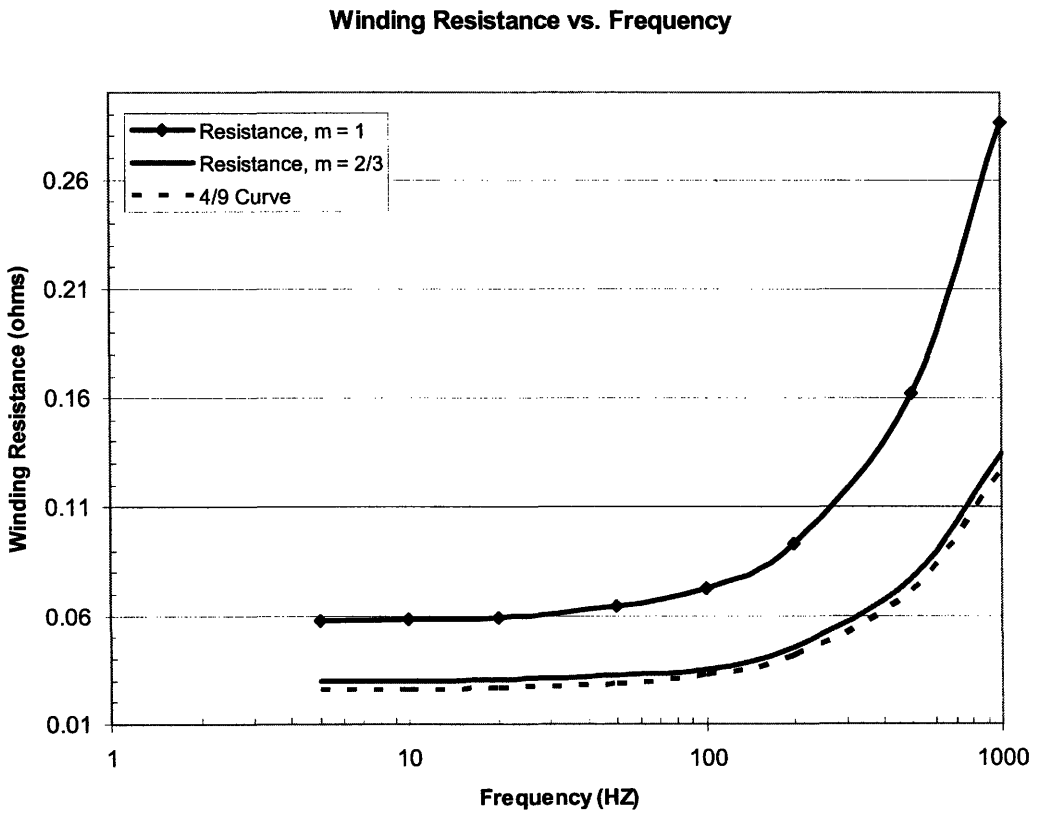

Figure 9.1 Comparison of winding resistance vs. frequency for $m = 1$ and $m = 2/3$

machines was the turns-ratio.

The plot in figure 9.1 shows that the winding resistance of the rewound machine is slightly larger than its ideal value but the error over the alternator's operating range is minimal. This small error can be attributed to the fact that the same copper packing factor was not achieved in the rewound machine and the hand winding resulted in a slightly longer winding. Nonetheless the numbers are accurate enough to validate that the correct winding ratio was achieved.

9.3 Output Power Measurements

The first design goal was to achieve increased output power at the high end operating speeds while maintaining optimal load-matched operation at low RPM. The analytical model from figure 5.11 predicted that at full (4.3 A) field current the SMR machine would average about 2229 W output power at 6000 RPM. This equates to a 26.5% improvement over the commercial alternator with third harmonic booster diodes and 45.5% improvement over the commercial alternator with a standard six diode rectifier. Note that the commercial alternator does use booster diodes.

The SMR-based alternator machine was mounted into the motor control test station shown in Figure 4.1 and tested under the same conditions (4.3 A field current, 25°C ambient) as the original Remy machine. The quantitative data collected during the test runs was compiled into a series of plots to graphically demonstrate SMR performance. The first plot shown in Figure 9.2 compares the analytical results with the experimental results to confirm that the machine behavior is consistent with theory. The analytical results were computed using the model and electromechanical parameters from Chapters 4 and 5. The experimental data is very accurate throughout the entire operating range with some deviation at the high end. The average error between the analytical and

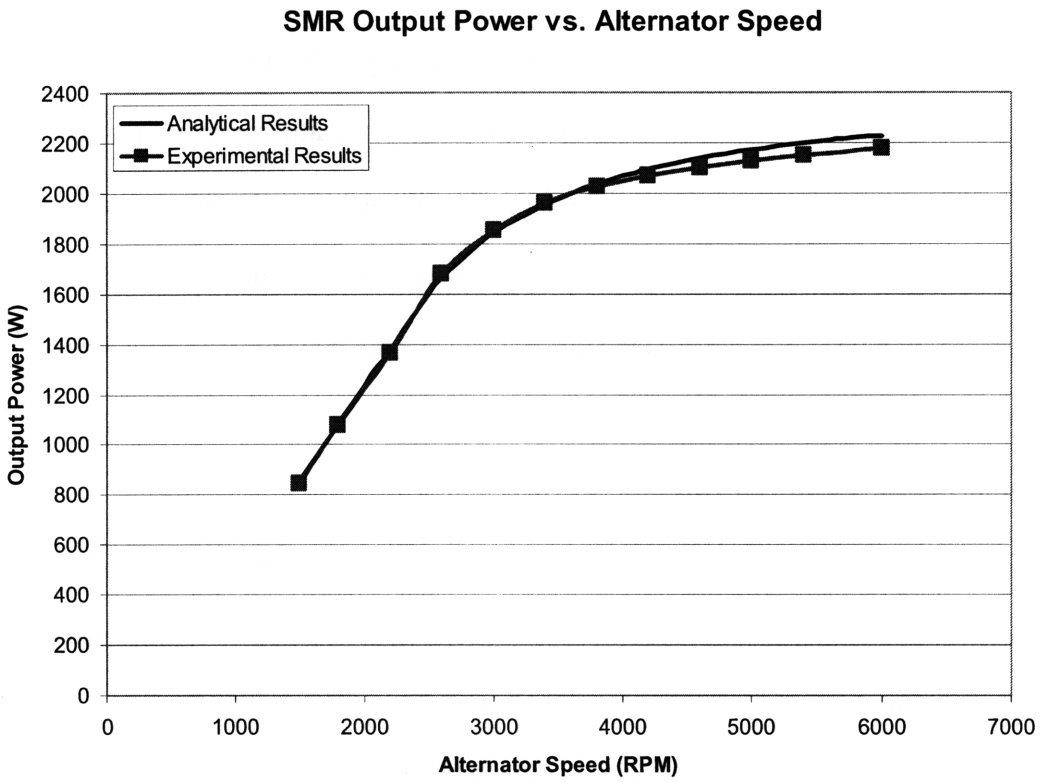

Figure 9.2 Output power comparison of analytical results versus experimental results for SMR.

experimental results is 1.24% over the operating range with a maximum deviation of 2.35% at 6000 RPM. This shows that the SMR achieved 2178 W or 97.7% of its expected output power at 6000 RPM.

The next plot, Figure 9.3, shows the experimentally measured output power improvement of the SMR machine versus the original Remy machine, with and without booster diodes. This plot validates that the number one design goal was met. There is substantial output power improvement at the high end operating speeds and load-matched operation maintaining the output power capabilities at lower RPM. Quantitatively, the SMR produced 2178 W at 6000 RPM. This equates to 42.2% output power improvement over the Remy alternator with a standard six diode rectifier and a 23.6% improvement over the Remy machine with a booster diode configuration.

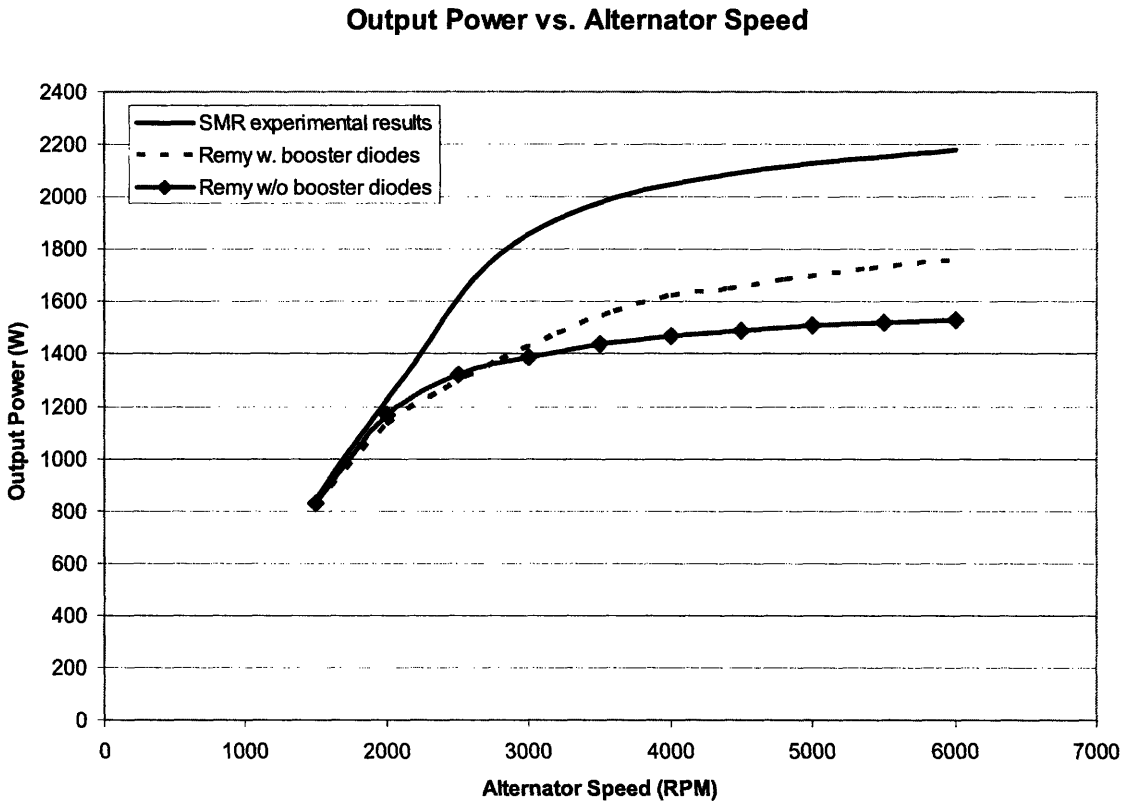

Figure 9.3 Output power comparison of SMR versus Remy with and without booster diodes

The final plot, figure 9.4, shows the output power profile of the SMR at three different field current levels. The top profile is at maximum field current of 4.3 A, the second at 3.6 A or just below 85% of maximum field, and the bottom profile at 3 A or 70% of maximum field. This plot is meant to show that the machine also demonstrates improved output power capability at less than full field, particularly at the high end operating speeds when the machine is no longer load-matched. For example, consider that the original Remy alternator with a standard six diode rectifier achieved 1531 W output at *full field current* whereas the SMR machine is capable of achieving approximately 1550 W output at *only 70%* of full field. Furthermore, the Remy alternator with additional booster diodes maxed out at 1761 W at full field whereas the SMR machine achieves over 1800 W at just under 85% of full field.

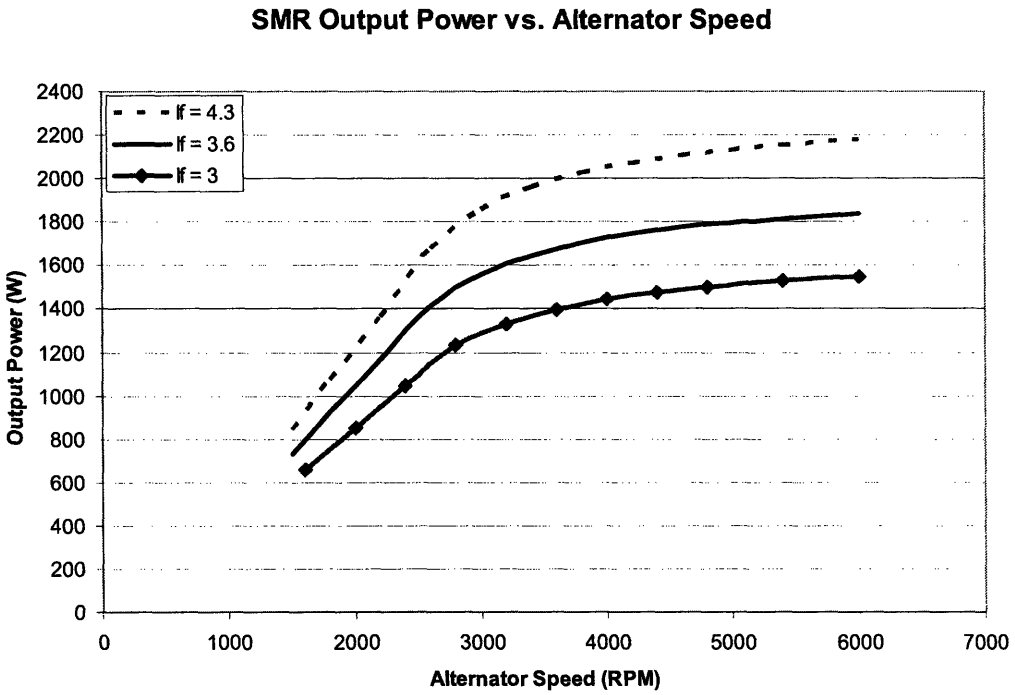

Figure 9.4 Output power comparison of SMR at 3 A, 3.6 A, and 4.3 A field current.

9.4 Temperature Measurements

The final dataset needed to fully characterize the SMR machine's performance is the operating temperature of the windings and power components. The winding temperature of the original Remy alternator with booster diodes was presented in Figure 4.5. The armature winding for the SMR-based alternator, according to the analysis presented in Chapter 5, should operate at a comparable temperature as there was a sufficient increase in copper area relative to the increase in RMS phase current.

Table 9.1: SMR Temperature Data

Alternator RPM	T_{FET}	T_{diode}	$T_{winding}$
1500	107.2	89.5	135.7
2000	116.7	108.4	157.2
2500	109.1	114.7	165.6
3000	121.9	126.6	185.1
3500	129.2	133.5	179.6

During the various test runs, attempts were made to capture the operating temperature of the windings and components but the instrumentation failed to provide a reliable readout of the data throughout the operating range. The winding temperature and case temperatures were recorded up to 3500 alternator RPM. That data is presented in Table 9.1. All temperatures are in °C.

Based on the thermal characterization performed in [3], it stands to reason that the winding temperature of the SMR-based alternator would behave very similar to that of a commercial alternator. A plot of the winding temperature up to 3500 alternator RPM is presented in figure 9.5. Included in that plot is the *expected* temperature performance of the winding throughout the operating range.

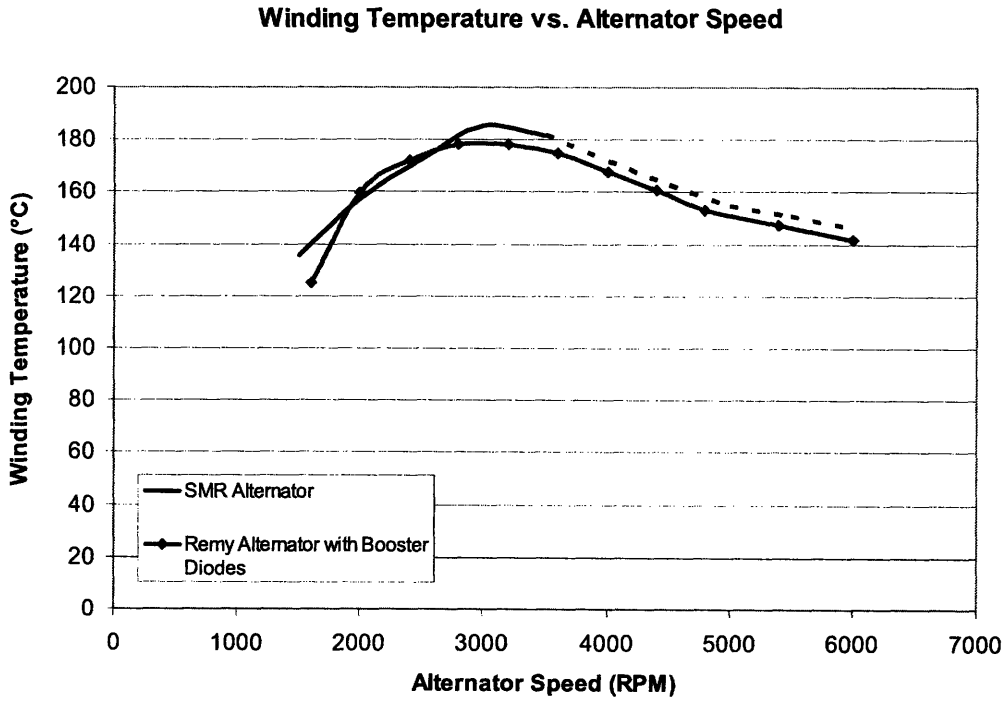

Figure 9.5 SMR winding temperature vs. Remy winding temperature over operating range. Solid line is *measured* temperature and dashed line represents *expected* temperature of SMR

Chapter 10

10. Conclusions and Future Work

In this chapter the material presented in the thesis is summarized and the major conclusions are highlighted. Recommendations for future work needed to make the SMR a fully integrated commercial product are discussed.

10.1 Thesis Summary and Conclusions

Chapter 1 presented the motivation for the design and constructions of a 14 V SMR-based alternator. Research has shown that the growing number of electrical loads in modern automobiles is approaching the output power limits of the traditional diode rectifier based alternator. In this thesis project we sought to develop a new alternator machine with increased output power capability that could be packaged into the same housing as a commercial alternator and could rely on the same manufacturing infrastructure and practices already in place. The SMR was introduced and analyzed as a theoretical basis for the new machine. The load matching concept was introduced and the design goals for the SMR were outlined.

Chapter 2 outlined the important electrical and thermal parameters for the selection of components that could be used in a 14 V SMR alternator. Based on these parameters a set of power devices and auxiliary components were selected for evaluation in a boost circuit test board. Test board specifications were generated to exercise the devices and validate their thermal and electrical capabilities.

Chapter 3 analyzed the electrical parameters and test board specifications to approximate the power dissipation in the devices. The thermal characteristics of the devices and PCB were then used to estimate the temperature rise in the devices. It was concluded that a heat spreader would be needed to conduct heat away from the MOSFET

in order to maintain the device at a safe operating temperature. A thermal transfer model was created to optimize the device temperature rise versus PCB space allocation. The devices were tested according to the test board specifications and one MOSFET-diode combination was selected to be used in the three-phase SMR alternator.

Chapter 4 investigated the performance of a Remy 92319 commercial alternator. The nominal full field current was measured at 4.3 A under laboratory conditions and used as a constant field current drive for subsequent testing. The output power capability was measured over a 1500 to 6000 alternator RPM operating range and a dataset was collected with the machine operating as a basic 6 diode rectifier and with the machine using additional third harmonic "booster" diodes. The machine constant, k, was also measured under laboratory conditions. The experimentally-obtained data was used to develop an analytical model that computed the output power capability as a function of the number of series-turns in the armature winding. A best fit curve for the analytical model was obtained by adjusting the parameter values for machine synchronous inductance and winding resistance.

Chapter 5 utilized the analytical model developed in Chapter 4 to obtain a winding ratio m that would produce an output power improvement which satisfied the design goals and didn't thermally overstress the SMR devices. It was decided to use a winding pattern consistent with the previous SMR design in [8,10]. The copper packing factor, per-turn copper area, and estimated device temperature rise were calculated at different ratios m. It was concluded that a value of $m = 2/3$ would satisfy the design goals with minimal thermal stress to the devices and the copper windings.

Chapter 6 detailed the design of a custom heatsink that would replace the rectifier structure and effectively increase the area of the diode plate in the commercial alternator

in order to provide for improved thermal performance. The structural limitations imposed by the housing and the combined height restriction of the heatsink and PCB dictated the fin characteristics of the heatsink. A CAD drawing was generated and the part was fabricated from copper using wire EDM. Pictures of the custom part are provided as well.

Chapter 7 discussed the control strategy used to verify the hardware functionality in the SMR. A PIC18F1230 microcontroller was used to implement the control strategy. The microcontroller utilized embedded comparators, timer functions, PWMs, and software interrupt capabilities to gate the MOSFETs on and off according to the polarity of the phase current and operating speed of the alternator. Oscilloscope captures from the final test runs were provided to demonstrate the functionality of control techniques implemented with the microcontroller.

Chapter 8 presented pictures of the SMR-based alternator which detailed the packaging and assembly of the new machine. The pictures focused on the sections of the machine that were replaced or redesigned: the armature winding, the heatsink, and the PCB. The photographs were used as verification that the hardware for the new machine can be packaged into an unaltered commercial alternator housing. The pictures are also used to detail the mechanical interfaces and subtleties of the new machine.

Chapter 9 provided experimental verification of the SMR-based alternator's performance capabilities. The SMR-based alternator was run through the same test methodology used in characterizing the commercial alternator. Datasets of the output power capability were recorded at 4.3 A field current and also at lower field current levels. The output data was plotted against the predicted data from the analytical model and also against the measured data from the original machine. It was verified that the

SMR machine achieved a 42.2% output power improvement over the original machine with a 6-diode rectifier and a 23.6% output power improvement over the original machine with a 6-diode rectifier plus two booster diodes. The SMR machine also achieved 97.7% of its expected output power improvement at $m = 2/3$.

10.2 Future Work

The purpose of this thesis has been to design an improved performance 14 V SMR-based alternator that can be fitted into the same mechanical housing as an off-the-shelf commercial alternator. The experimental testing conducted in Chapter 9 demonstrated that the SMR-based alternator has achieved the design goals outlined in the introductory chapter and has validated the accuracy of the analytical model developed in Chapters 4 and 5. The pictures shown in Chapter 8 have provided visual proof that the hardware needed for the new machine can be embedded into a commercial alternator housing. The next step in the alternator's development is to realize the control features implemented in the 42 V SMR alternator from [8, 10]. The machine discussed in [8, 10] featured a field current regulator, a closed loop compensator, and a load dump transient protection.

The components for the field current regulator have already been selected and the PCB layout provided the land area for the components. However, the microcontroller has not been programmed to sense the SMR output or regulate the field current by modulating the field control MOSFET. The embedded A/D converter in the microcontroller can be used to read the SMR output and provide a proportional integrator compensator. The PWM override function described in Chapter 7 can be utilized to modulate the field control MOSFET and regulate the field current by setting the duty cycle according to (4.1).

A load dump transient occurs when a heavy current load is instantaneously removed or applied to the alternator output causing the output voltage to rise or fall, respectively. In the situation where the voltage rises, it can rise to more than double the regulation set point which could cause component degradation and ultimately lead to failure. A method for handling such a transient was developed in [8, 10] where the three power MOSFETs were shorted when the output voltage went above a certain level. This is another capability that can be programmed into the microcontroller in the future.

The SMR alternator in this thesis achieved about 2178 W, 160 A output. Ultimately this may not be enough to satisfy the electrical demands of future automobiles and another design effort with newer and presumably better power components can be undertaken. The analytical and thermal models which were developed in this thesis and proven to be very accurate in predicting the performance of the SMR and its components can be used as the basis for future design work of SMR-based alternators.

Appendix A

A. Circuit Schematics

A.1. Test Board Schematic

This appendix provides a schematic diagram of the boost converter test circuit used to evaluate the components selected in Chapter 2. The schematic includes the MOSFET switch, Schottky diode, gate driver, ceramic capacitors, and a UC3823A PWM chip operating as an oscillator to provide 50% duty cycle at 100 KHz switching frequency.

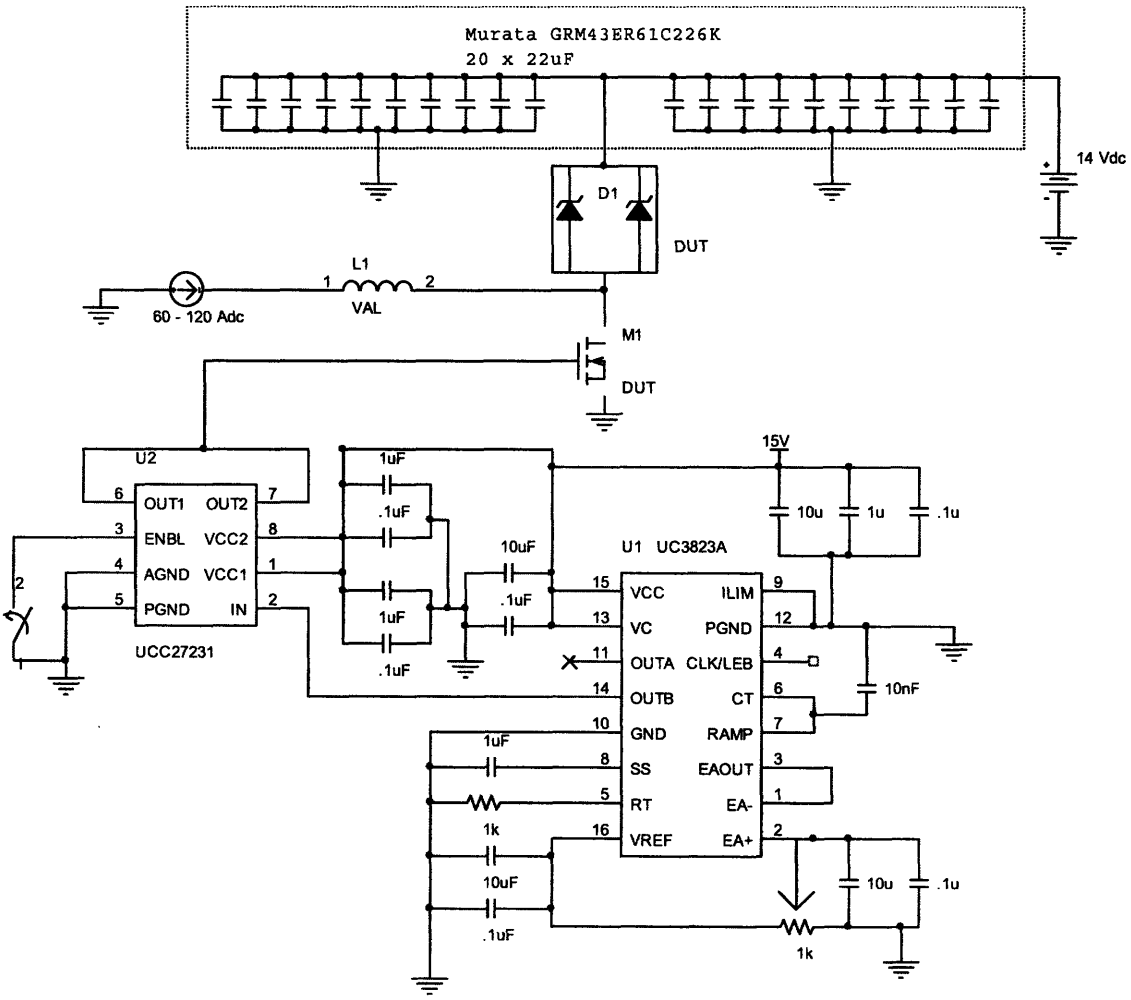

Figure A.1 Test board schematic

A.2 SMR Circuit Schematic

This appendix provides the schematic for the SMR circuit. Page 1 contains the 3-phase boost switch sets, gate drive circuits, ceramic output capacitors, and output voltage sense circuitry. Page 2 contains the zero-crossing detection circuitry and field control components. Page 3 contains the linear regulator circuitry for the three gate drivers and the microcontroller circuit.

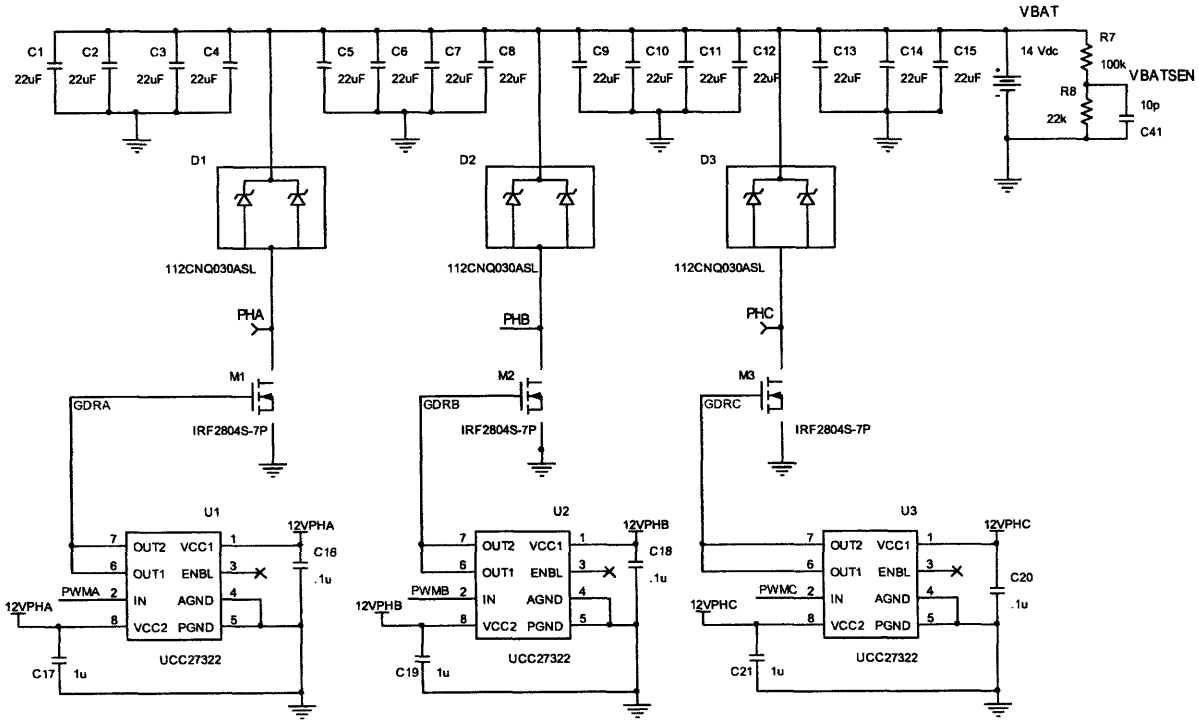

Figure A.2 SMR schematic, page 1

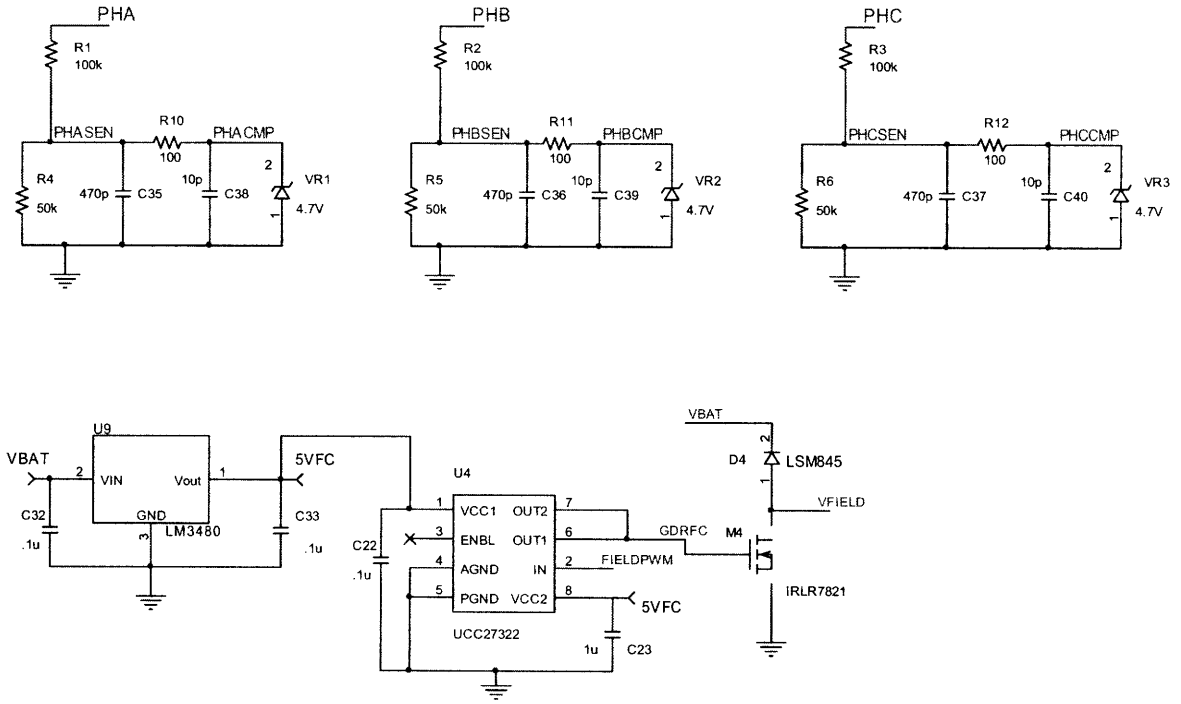

Figure A.3 SMR schematic, page 2

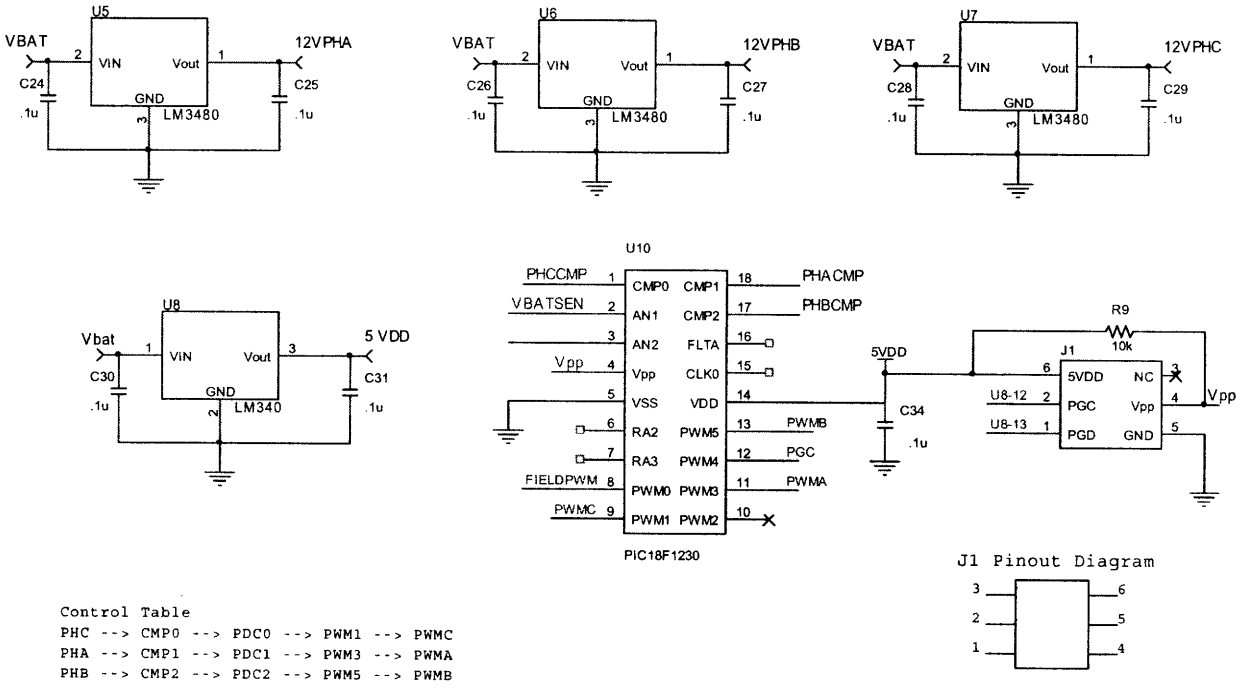

Figure A.4 SMR schematic, page 3

Appendix B

B. SMR PCB Layout

This appendix provides images of the PCB layout for the SMR prototype. The SMR prototype is a 4-layer PCB with 4oz/ft^2 outer layers and 3oz/ft^2 inner layers. The PCB layout was made using EAGLE™ Layout Editor from Cadsoft Computer, Inc. Note that images are not to scale.

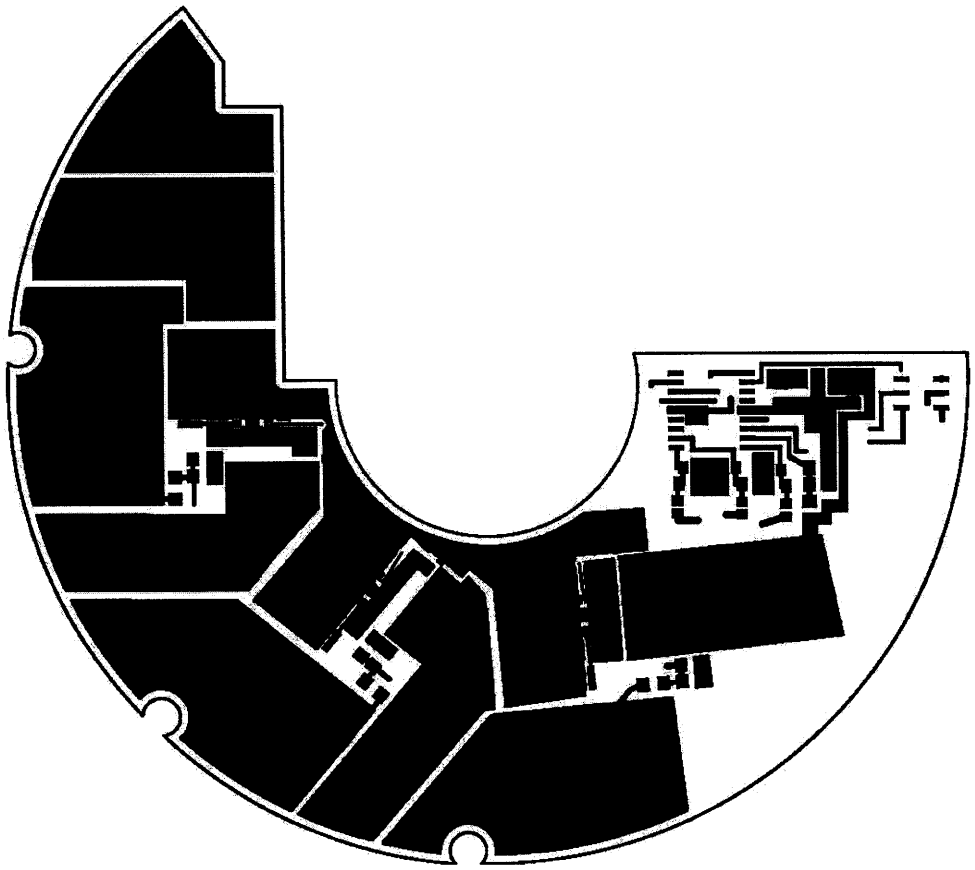

Figure B.1 Top copper layer

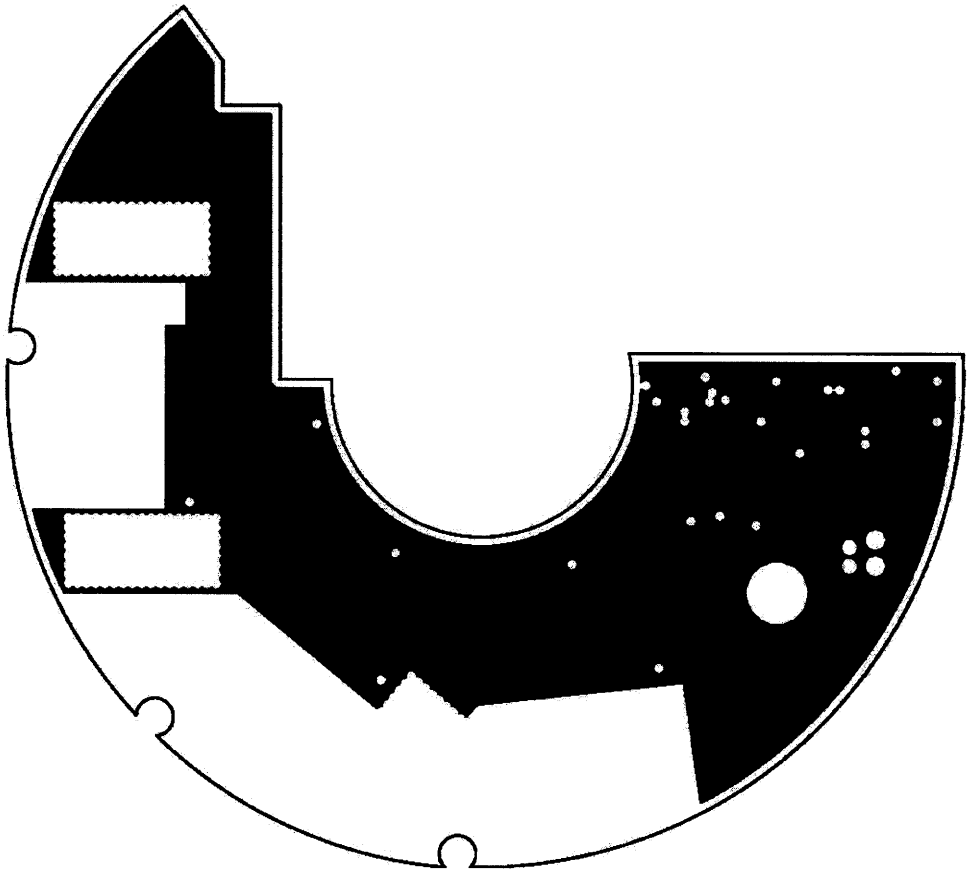

Figure B.2 Second layer

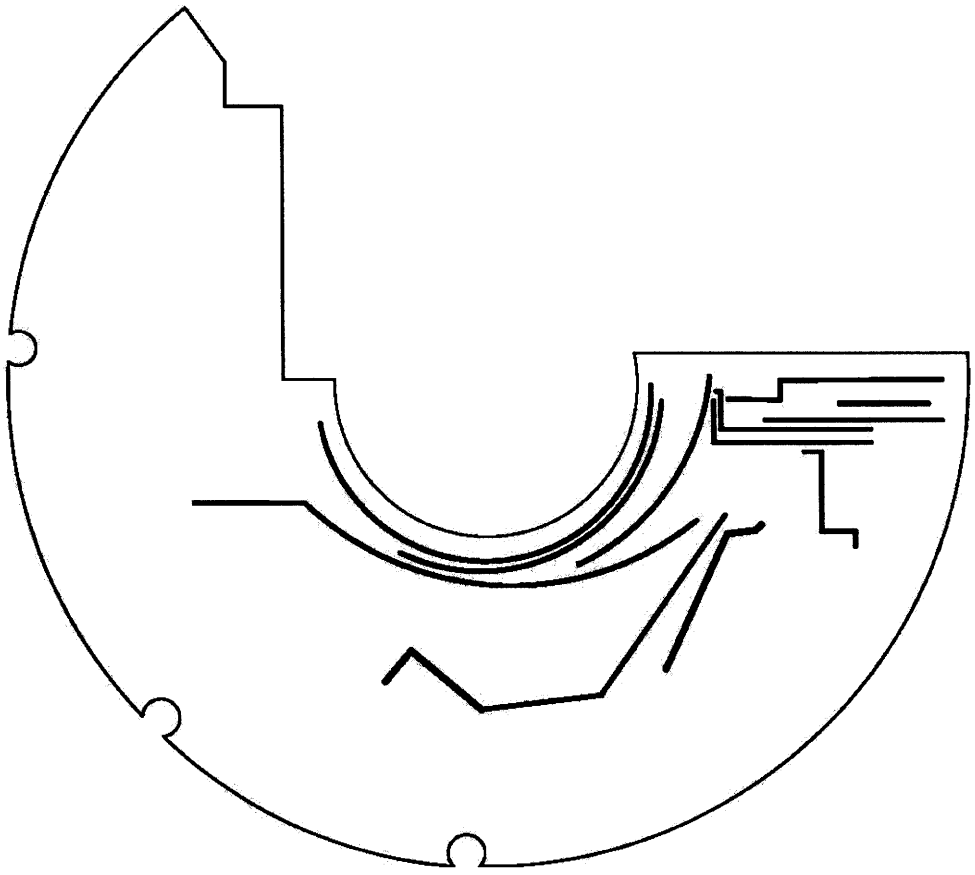

Figure B.3 Third layer

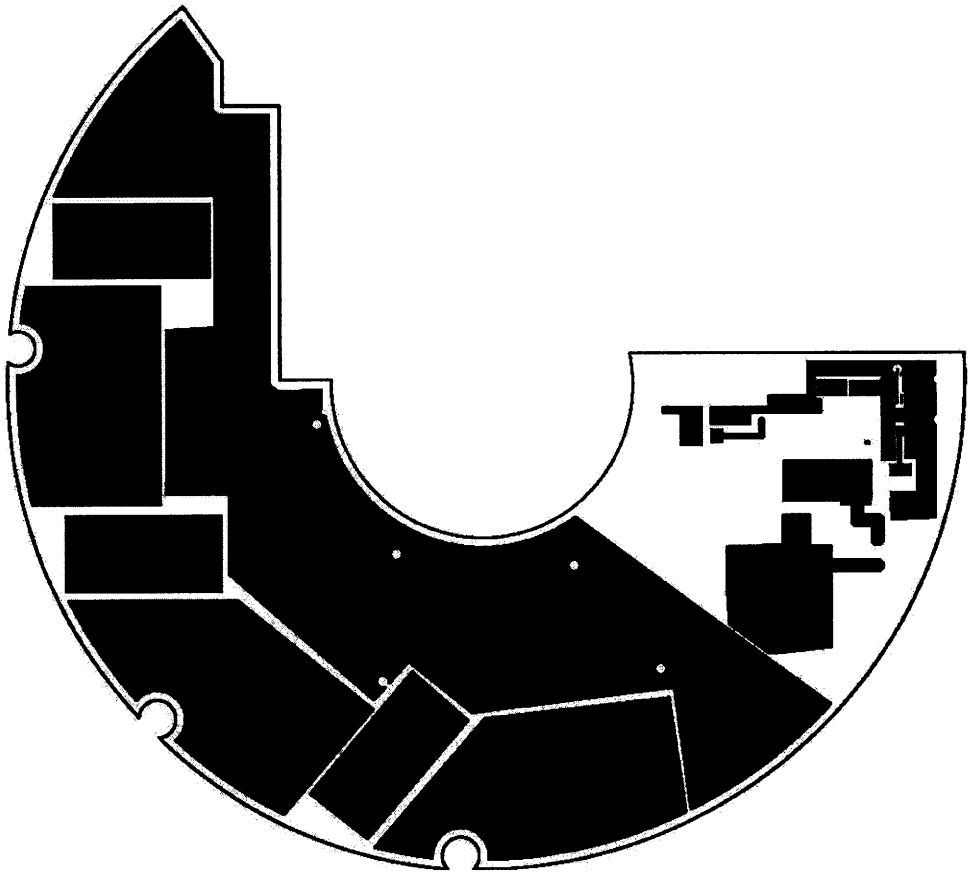

Figure B.4 Bottom layer

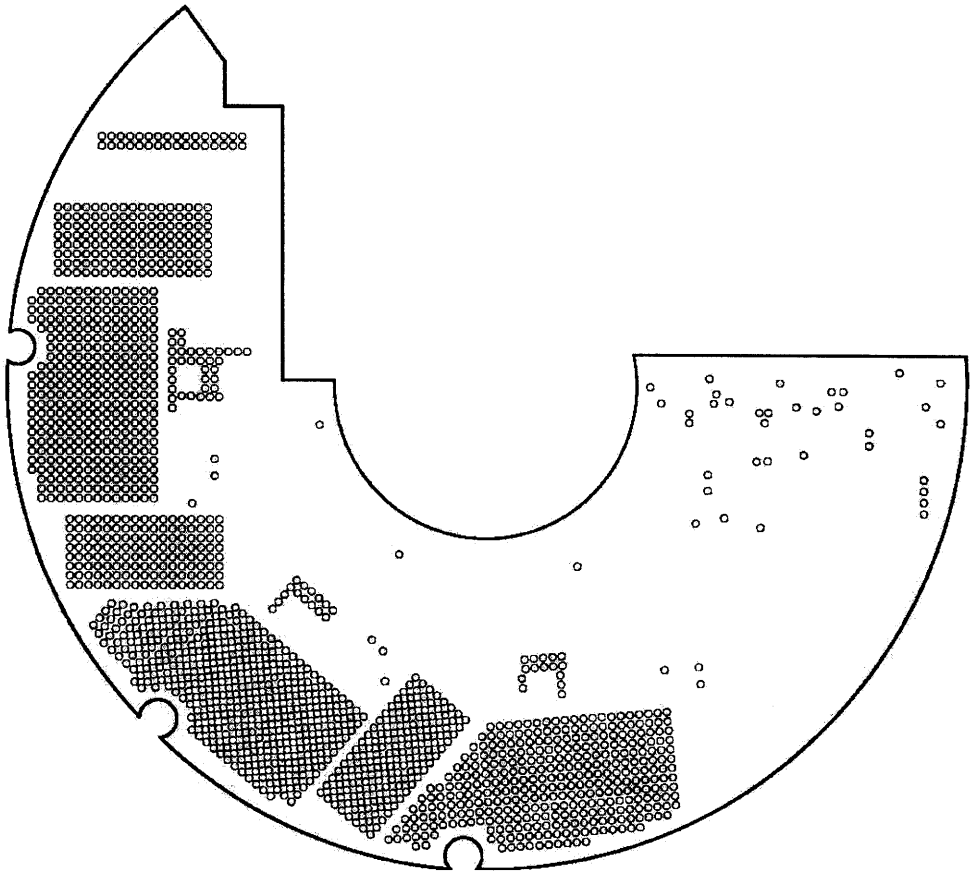

Figure B.5 PCB outline and vias

Appendix C

C. Heatsink CAD Drawings

This appendix provides 3D images of the custom heatsink designed for the SMR-based alternator. The drawings were developed with SolidWorks™ CAD software. The first drawing is a bottom view displaying the spacing and tapering of the fins. The second drawing is a top view.

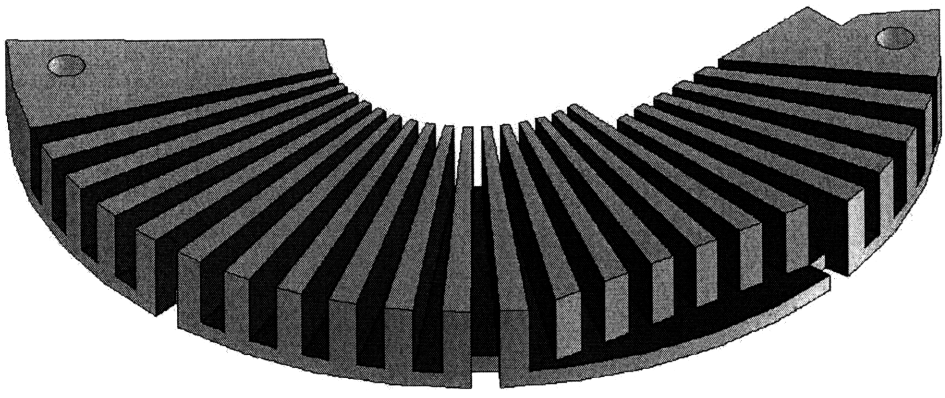

Figure C.1 Bottom view of custom heatsink

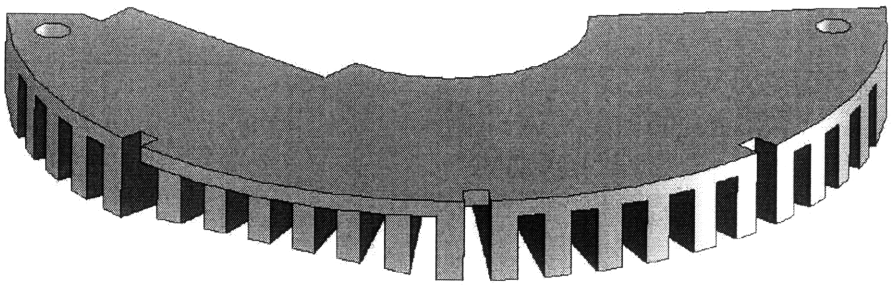

Figure C.2 Top view of custom heatsink

Appendix D

D. Alternator Computational Model

This appendix provides the MATLAB code for the alternator computational model.

```
%%% SMR Alternator Model

clear all;

%% Static Machine Parameters
m = 2/3;                    %Stator winding turns-ratio
k = .0033*m;                %Machine constant
If = 4.3;                   %Maximum field current
Ls = m^2*116.5e-6;          %Synchronous inductance
Rs = .03*m^2;               %Stator winding resistance

%% Static SMR Parameters
Vd = .5;                    %Schottky diode forward voltage drop
Rdson = .0026;              %MOSFET "on" resistance

%% Static Operational Parameters
Vo = 13.5;                  %Load voltage
Vod = (4/pi)*(Vo/2+Vd);     %Magnitude of the fundamental of EMF
                            %voltage
                            %sink from equation 4.11

%% Output Power vs. Speed Model
i = 1;                      %Index variable for loop
f(i) = 150;                 %Electrical frequency
Pmax(i) = 0;                %Initial power value at given frequency
dmax(i) = 0;                %Initial duty cycle value at given
                            %frequency


% Model runs from 150 Hz to 600 Hz (1500 rpm to 6000 rpm) in 10 Hz
% increments.  At each operating point, the alternator rpm, rotational
% frequency, peak EMF voltage, and optimal duty cycle are computed.
% Duty cycle is initially set to be either 0 or value computed by
% equation 5.12

for f= 150:10:600;
    rpm(i) = f*10;
    omega(i) = 2*pi*f;
    Vs(i) = k*If*omega(i);
    d(i) =1-((sqrt(2)*pi*k/(4*Vo))*If*omega(i));
    dmin = d(i);

    % Embedded duty cycle loop used to find optimal duty cycle
```

```
    j = 1;
    Is1(j) = 0;
    Io(j) = 0;
    Po(j) = 0;

    if dmin >=0;
        dopt(j) = dmin;
        else;
        dopt(j) = 0;
    end;

    % Duty cycle is swept from dmin to 1 in increments of .001. At each
    % point the peak phase current, average output current, and
    % output power are calculated.
    while dopt(j)<= 1;
        Is1(j) = (Vs(i)^2 - ((1-dopt(j))*Vod)^2)/(((1-dopt(j))*Vod)*Rs
                 + sqrt((omega(i)*Ls)^2*(Vs(i)^2-((1-dopt(j))*Vod)^2)+
                 Rs^2*Vs(i)^2));
        Io(j) = 3*Is1(j).*(1-dopt(j))./pi;
        Po(j) = Io(j).*Vo;
        j = j + 1;
        dopt(j) = dopt(j-1) + .001;
    end;
    % End of duty cycle loop

    % Maximum output current, output power, and the duty cycle that
    % produces those values are extracted
    [Pmax(i), jopt(i)] = max(Po);
    Imax(i) = Io(jopt(i));
    dmax(i) = dopt(jopt(i));
    Ifund(i) = Is1(jopt(i));

    % Device power dissipation at maximum output power.
    Pdiode(i) = (Imax(i)/3)*Vd;
    if dmax(i)== 0;
        Psw(i) = 0;
        else;
        Psw(i) = ((Ifund(i)*.169)-4.8)/2;
    end;
    Pfet(i) = ((Ifund(i)/2)^2)* Rdson + ((Ifund(i)/2)*sqrt(dmax(i)))^2
              * Rdson + Psw(i);

    % Temperature profile based on expected thermal transfer
    % characteristics of devices and heatsink
    Ta = 25;
    Rsa(i) = (exp(-4.2e-4*rpm(i)) + (1.867e-5*rpm(i)))*(2);
    Rjcdiode = .25;
    Rcsdiode = .85;
    Rjcfet = .5;
    Rcsfet = .96;
    Tsink(i) = 3*(Pdiode(i) + Pfet(i))*Rsa(i) + Ta;
    Tjdiode(i) = Pdiode(i)*(Rjcdiode + Rcsdiode) + Tsink(i);
    Tjfet(i) = Pfet(i)*(Rjcfet + Rcsfet) + Tsink(i);

i = i + 1;
end;
```

```
dmax = transpose(dmax);


%% Sample plot of relevant data
figure(1);
subplot(2,1,1),
plot(rpm,Pmax, 'linewidth',2);
title('Pout vs Alternator Speed, m = 2/3');
ylabel('Pout');
ylim([0 3000]);
xlabel('Alternator Speed (RPM)');
xlim([0 6000]);
grid minor;
axis on;
subplot(2,1,2),
plot(rpm,Tjdiode,rpm,Tjfet,'linewidth',2);
title('Junction Temperature vs Alternator Speed, m = 2/3');
ylabel('Junction Temperature (C)');
ylim([50 200]);
xlabel('Alternator Speed (RPM)');
xlim([0 6000]);
grid on;
axis on;
legend('Diode', 'FET');
```

Appendix E

E. PIC18F1230 Assembly Code

```
;*********************************************************************
;    Filename:          PWM
;    Date:              2.1.08
;    File Version:      1
;    Author:            Armando Mesa
;    Company:           MIT
;*********************************************************************
;    Files required:         P18F1230.INC
;                            18F1230.LKR
;*********************************************************************
      LIST P=18F1230, F=INHX32
      #include <P18F1230.INC>
;*********************************************************************
;Configuration bits
;   Oscillator Selection:
      CONFIG      OSC = INTIO1
      CONFIG      FCMEN = OFF
      CONFIG      IESO = OFF
      CONFIG      PWRT = OFF
      CONFIG      BOR = OFF
      CONFIG      WDT = OFF
      CONFIG      HPOL = HIGH
      CONFIG      LPOL = HIGH
      CONFIG      PWMPIN = OFF
      CONFIG      FLTAMX = RA7
      CONFIG      T1OSCMX = HIGH
      CONFIG      MCLRE = OFF
;*********************************************************************
;Variable definitions
; UDATA variables are only needed if low priority interrupts are used.
; UDATA_ACS variables are needed to store other special function
; registers used in the interrupt routines.

            UDATA

WREG_TEMP         RES 1
STATUS_TEMP       RES 1
BSR_TEMP          RES 1

            UDATA_ACS

Example           RES 1
SETTIME           RES 1
RTNTIME           RES 1
RTNTIMEA          RES 1
RTNTIMEB          RES 1
RTNTIMEC          RES 1
TABOFFSET         RES 1
```

```
PosDMaxL          RES 1
TABDIFF           RES 1
LowDiff           RES 1
HighDiff          RES 1
PhCTnewHC         RES 1
PhCToldHC         RES 1
PhCTnewFC         RES 1
PhCToldFC         RES 1
PhCTavg           RES 1

PhATnewHC         RES 1
PhAToldHC         RES 1
PhATnewFC         RES 1
PhAToldFC         RES 1
PhATavg           RES 1

PhBTnewHC         RES 1
PhBToldHC         RES 1
PhBTnewFC         RES 1
PhBToldFC         RES 1
PhBTavg           RES 1

IdleSpeed         RES 1
IdleCount         RES 1

;; Address of PWM duty cycle table

TABPWM            equ   0xD4

;*********************************************************************
;EEPROM data
; Data to be programmed into the Data EEPROM is defined here

DATA_EEPROM CODE  0xf00000
            DE    "Test Data",0,1,2,3,4,5

;*********************************************************************
;Reset vector
; This code will start executing when a reset occurs.

RESET_VECTOR      CODE  0x0000

            goto  Main        ;go to start of main code
;*********************************************************************
;High priority interrupt vector
; This code will start executing when a high priority interrupt occurs;
; or when any interrupt occurs if interrupt priorities are not enabled.

HI_INT_VECTOR     CODE  0x0008      ;high priority interrupt address

            bra   HighInt           ; high priority interrupt routine
;*********************************************************************
;Low priority interrupt vector
; This code will start executing when a low priority interrupt occurs.
; This code can be removed if low priority interrupts are not used.

LOW_INT_VECTOR    CODE  0x0018      ;low priority interrupt address
            bra   LowInt            ;low priority interrupt routine
```

```
;*****************************************************************
;High priority interrupt routine

; High priority interrupt routine is triggered off of
; a zero crossing of the phase current in any of the 3
; phases.  Routine reads and averages the number of
; primary timer counts and sets conditions for operation
; during ensuing half-cycle.

            CODE

HighInt:
      BTFSC       PIR1, 1
      bra         PhCTimer
      BTFSC       PIR1, 2
      bra         PhATimer
      BTFSC       PIR1, 3
      bra         PhBTimer
      BCF         PIR1, 1
      retfie

PhCTimer:
      movff       TMR0L,PhCTnewHC
      clrf        TMR0L
      RRCF        PhCTnewHC
      BCF         PhCTnewHC,7
      movf        PhCTnewHC,0
      addwf       PhCToldHC,0
      mullw       0x02
      movff       PRODL, PhCTnewFC
      movff       PhCTnewHC, PhCToldHC
      RRCF        PhCTnewFC
      BCF         PhCTnewFC,7
      movf        PhCTnewFC,0
      addwf       PhCToldFC,0
      movff       WREG, PhCTavg
      movf        PhCTnewFC,0
      subwf       PhCToldFC,0
      movff       PhCTnewFC,PhCToldFC
      BTFSS       STATUS,4
      bra         PhCLessThan
      bra         PhCGreaterThan
PhCLessThan:
      CPFSGT      LowDiff
      bra         PhCClear
      bra         PhCState
PhCGreaterThan:
      CPFSLT      HighDiff
      bra         PhCClear
      bra         PhCState
PhCClear:
      BTFSC       CMCON, C0OUT
      nop
      BCF         PIR1,1
      retfie
PhCState:
      BTFSS       CMCON, C0OUT
```

```
        bra         PhCDCycleNEG
        bra         PhCDCyclePOS
PhCDCycleNEG:
        BCF         OVDCOND,1
        BCF         PIR1,1
        BCF         PORTA, 2
        movf        PhCTnewHC,0
        mullw       0x02
        movf        PRODL,0
        subwf       PhCTavg,0
        movwf       Example
        RRCF        WREG
        BCF         WREG, 7
        RRCF        WREG
        BCF         WREG, 7
        RRCF        WREG
        BCF         WREG, 7
        subwf       Example
        decf        Example
        movlw       0x68
        CPFSLT      Example
        retfie
        movff       Example, RTNTIME
        movff       RTNTIME, RTNTIMEC
        retfie
PhCDCyclePOS:
        BSF         OVDCOND, 1
        BCF         PIR1,1
        BSF         PORTA, 2
        movf        PhCTavg, 0
        mullw       0x02
        movf        PRODL, 0
        movff       PRODH, TBLPTRH
        CPFSGT      TABDIFF
        incf        TBLPTRH
        addwf       TABOFFSET, 0
        movwf       TBLPTRL
        movlw       0x0A
        TBLRD*
        CPFSLT      TABLAT
        retfie
        movlw       0x04
        mulwf       TABLAT
        movff       PRODL, PosDMaxL
        movff       PosDMaxL, PDC0L
        retfie

PhATimer:
        movff       TMR0L,PhATnewHC
        RRCF        PhATnewHC
        BCF         PhATnewHC, 7
        movf        PhATnewHC, 0
        addwf       PhAToldHC, 0
        mullw       0x02
        movff       PRODL, PhATnewFC
        movff       PhATnewHC, PhAToldHC
        RRCF        PhATnewFC
        BCF         PhATnewFC, 7
```

```
      movf        PhATnewFC, 0
      addwf       PhAToldFC, 0
      movff       WREG,PhATavg
      movf        PhATnewFC,0
      subwf       PhAToldFC,0
      movff       PhATnewFC,PhAToldFC
      BTFSS       STATUS,4
      bra         PhALessThan
      bra         PhAGreaterThan
PhALessThan:
      CPFSGT      LowDiff
      bra         PhAClear
      bra         PhAState
PhAGreaterThan:
      CPFSLT      HighDiff
      bra         PhAClear
      bra         PhAState
PhAClear:
      BTFSC       CMCON, C1OUT
      nop
      BCF         PIR1,2
      retfie
PhAState:
      BTFSS       CMCON, C1OUT
      bra         PhADCycleNEG
      bra         PhADCyclePOS
PhADCycleNEG:
      BCF         OVDCOND,3
      BCF         PIR1,2
      movff       RTNTIME, RTNTIMEA
      retfie
PhADCyclePOS:
      BSF         OVDCOND,3
      BCF         PIR1,2
      movff       PosDMaxL, PDC1L
      retfie

PhBTimer:
      movff       TMR0L,PhBTnewHC
      RRCF        PhBTnewHC
      BCF         PhBTnewHC, 7
      movf        PhBTnewHC, 0
      addwf       PhBToldHC, 0
      mullw       0x02
      movfF       PRODL, PhBTnewFC
      movff       PhBTnewHC, PhBToldHC
      RRCF        PhBTnewFC
      BCF         PhBTnewFC,7
      movf        PhBTnewFC,0
      addwf       PhBToldFC,0
      movff       WREG,PhBTavg
      movf        PhBTnewFC, 0
      subwf       PhBToldFC, 0
      movff       PhBTnewFC,PhBToldFC
      BTFSS       STATUS,4
      bra         PhBLessThan
      bra         PhBGreaterThan
PhBLessThan:
```

```
      CPFSGT      LowDiff
      bra         PhBClear
      bra         PhBState
PhBGreaterThan:
      CPFSLT      HighDiff
      bra         PhBClear
      bra         PhBState
PhBClear:
      BTFSC       CMCON, C2OUT
      nop
      BCF         PIR1,3
      retfie
PhBState:
      BTFSS       CMCON, C2OUT
      bra         PhBDCycleNEG
      bra         PhBDCyclePOS
PhBDCycleNEG:
      BCF         OVDCOND,5
      BCF         PIR1,3
      movff       RTNTIME, RTNTIMEB
      retfie
PhBDCyclePOS:
      BSF         OVDCOND,5
      BCF         PIR1,3
      movff       PosDMaxL, PDC2L
      retfie

;*****************************************************************************
;Low priority interrupt routine
; The low priority interrupt code is placed here.
; This code can be removed if low priority interrupts are not used.


; Low priority interrupt routine is triggered off of an overflow
; in the secondary timer.  Routine monitors the pulse width of
; synchronous rectification timer and shuts MOSFETs off when
; pulse width has expired.

LowInt:
      movff       STATUS,STATUS_TEMP
      movff       WREG,WREG_TEMP
      movff       BSR,BSR_TEMP
      BCF         PIR1, 0
      setf        TMR1H
      movff       SETTIME, TMR1L
      BTFSS       OVDCOND, 3
      call        CONDA
      BTFSS       OVDCOND, 5
      call        CONDB
      BTFSS       OVDCOND, 1
      call        CONDC
      goto        Restore
CONDA:
      dcfsnz      RTNTIMEA
      BSF         OVDCOND, 3
      return
CONDB:
      dcfsnz      RTNTIMEB
```

```
      BSF         OVDCOND, 5
      return
CONDC:
      dcfsnz      RTNTIMEC
      BSF         OVDCOND, 1
      return
Restore:
      movff       BSR_TEMP,BSR
      movff       WREG_TEMP,WREG
      movff       STATUS_TEMP,STATUS
      retfie

;*******************************************************************
********
;Start of main program

; Lookup table for max duty cycle. Timer counts in high
; priority routine map to a table pointer which extracts
; a PWM duty cycle from table.

      org    TABPWM
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00
      data   0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x01
      data   0x01, 0x01, 0x01, 0x01, 0x02, 0x02, 0x02, 0x02
      data   0x02, 0x02, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03
      data   0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03, 0x03
      data   0x04, 0x04, 0x04, 0x04, 0x04, 0x04, 0x04, 0x04
      data   0x05, 0x05, 0x05, 0x05, 0x05, 0x05, 0x05, 0x05
      data   0x05, 0x06, 0x06, 0x06, 0x06, 0x06, 0x06, 0x06
      data   0x06, 0x06, 0x06, 0x07, 0x07, 0x07, 0x07, 0x07
      data   0x07, 0x07, 0x07, 0x07, 0x07, 0x07, 0x08, 0x08
      data   0x08, 0x08, 0x08, 0x08, 0x08, 0x08, 0x08, 0x08
      data   0x08, 0x08, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09
      data   0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09

TABEND
```

```
;;;; Main code - Setting all control registers for operation

Main:
      clrf        PORTB
      clrf        PORTA
      movlw       0x0C
      movwf       TRISB
                  ;RB0 = output (PWM0, Pin 8 = Field PWM)
                  ;RB1 = output (PWM1, Pin 9 = PHC PWM)
                  ;RB2 = input (CMP2, Pin 17 = PHB voltage comparator)
                  ;RB3 = input (CMP1, Pin 18 = PHA voltage comparator)
                  ;RB4 = output (PWM2, Pin 10 = Unused PWM)
                  ;RB5 = output (PWM3, Pin 11 = PHA PWM)
                  ;RB6 = output (PWM4, Pin 12 = unused PWM)
                  ;RB7 = output (PWM5, Pin 13 = PHB PWM)
      movlw       0xB3
      movwf       TRISA
                  ;RA0 = input (CMP0, Pin 1 = PHC voltage comparator)
                  ;RA1 = input (AN1, Pin 2 = VBAT sense)
                  ;RA2 = output (RA2, Pin 6 = debug output)
                  ;RA3 = output (RA3, Pin 7 = debug output)
                  ;RA4 = input (AN2, Pin 3 = unused analog input)
                  ;RA5 = input (Vpp, Pin 4 = programming voltage)
                  ;RA6 = output (CLK0, Pin 15 = Oscillator output)
                  ;RA7 = input (FLTA, Pin 16 = PWM fault input)
      movlw       0xC0
      movwf       OSCTUNE
      movlw       0xF2
      movwf       OSCCON
      movlw       0x45
      movwf       T0CON
      movlw       0x00
      movwf       TMR0L
      movlw       0x00
      movwf       TMR0H
      movlw       0x00
      movwf       PTCON0
      movlw       0x80
      movwf       PTCON1
      movlw       0x13
      movwf       PTPERL
      movlw       0x00
      movwf       PTPERH
      movlw       0x57
      movwf       PWMCON0
      movlw       0x3E
      movwf       OVDCOND
      movlw       0x3E
      movwf       OVDCONS
      clrf        PTMRL
      clrf        PTMRH
      movlw       0x04
      mullw       0x09
      movff       PRODL, PosDMaxL
      movff       PRODL, PDC0L
      movff       PRODH, PDC0H
      movff       PRODL, PDC1L
```

```
      movff       PRODH, PDC1H
      movff       PRODL, PDC2L
      movff       PRODH, PDC2H
      movlw       0x07
      movwf       CMCON
      movlw       0xA4
      movwf       CVRCON
      movlw       0x00
      movwf       T1CON
      movlw       0xD2
      movwf       TMR1L
      movlw       0xFF
      movwf       TMR1H
      movlw       0x00
      movwf       PIE1
      clrf        PIR1
      movlw       0xC0
      movwf       INTCON
      BSF         RCON, 7
      movlw       0x0E
      movwf       IPR1

      movlw       UPPER(TABPWM)
      movwf       TBLPTRU
      movlw       HIGH(TABPWM)
      movwf       TBLPTRH
      movlw       LOW(TABPWM)
      movwf       TBLPTRL
      movwf       TABOFFSET
      clrf        TABLAT

      movlw       0x2B
      movwf       TABDIFF
      movlw       0xD2
      movwf       SETTIME
      movlw       0xFF
      movwf       IdleCount
      movlw       0x68
      movwf       IdleSpeed
      movlw       0x05
      movwf       LowDiff
      movlw       0xFA
      movwf       HighDiff
      clrf        PhCToldHC
      clrf        PhCToldFC
      movlw       0x64
      movwf       RTNTIME

; Startup routine.  Up to this point all timers and
; interrupts are disabled.  Startup waits for first
; interrupt on primary phase (Phase C) to enable
; primary timer
Startup:
      BTFSS       PIR1, 1
      bra         Startup
      BTFSS       CMCON, C0OUT
      nop
      clrf        PIR1
```

```
      BSF         T0CON, 7
      movff       IdleSpeed, PhCToldHC

; CCM code polls for interrupts on Phase C.  Waits for
; a set number of successive interrupts producing the
; same number of timer counts before enabling all interrupts
CCM:
      BTFSS       PIR1, 1
      bra         CCM
      movf        TMR0L, 0
      clrf        TMR0L
      BTFSS       CMCON, C0OUT
      nop
      clrf        PIR1
      CPFSEQ      PhCToldHC
      bra         CCM
      movff       WREG, PhCToldHC
      decfsz      IdleCount
      bra         CCM
      movff       PhCToldHC, PhCToldFC
      RRCF        PhCToldHC
      BCF         PhCToldHC,7
      movlw       0x0F
      movwf       PIE1
      BSF         T1CON, 0
      bra         MainPoll

; MainPoll routine is a PWM "mirror" routine. Looks at
; PORT output of respective phase and mirrors that bit
; over to debug output
MainPoll:
      BTFSS       PORTB,1           ;PhC PWM
;     BTFSS       PORTB,5           ;PhA PWM
;     BTFSS       PORTB,7           ;PhB PWM
      bra         BitClear
      bra         BitSet
BitClear:
      BCF         PORTA,3
      bra         MainPoll
BitSet
      BSF         PORTA,3
      bra         MainPoll

;*****************************************************************
;End of program
;
            END
```

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