Choosing a Gate Dielectric for Graphene Based Transistors

by

Pei-Lan Hsu
B.S. Electrical Engineering, B.S. Physics
Massachusetts Institute of Technology, 2007

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2008

© Massachusetts Institute of Technology 2008. All rights reserved.

Author ....
Department of Electrical Engineering and Computer Science
August 15, 2008

Certified by ....
Jing Kong
Assistant Professor, Department of Electrical Engineering and Computer Science
Thesis Supervisor

Certified by ....
Jakub Kedzierski
Assistant Group Leader, MIT Lincoln Laboratory Group 88
Thesis Supervisor

Accepted by ....
Arthur C. Smith
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Students

Choosing a Gate Dielectric for Graphene Based Transistors

by

Pei-Lan Hsu

B.S. Electrical Engineering, B.S. Physics

Massachusetts Institute of Technology, 2007

Submitted to the Department of Electrical Engineering and Computer Science
on August 15, 2008, in partial fulfillment of the
requirements for the degree of
Master of Engineering in Electrical Engineering

Abstract

Much attention has recently been focused on graphene as an alternative semiconductor to silicon. Transistors with graphene conduction channels have only recently been fabricated and their performance remains to be optimized. In this thesis, different candidate gate dielectric materials are examined for use in graphene transistors. Evaporated HfO_2 is ultimately used as the gate dielectric for graphene field effect transistors (FETs) on six different graphene samples. Two types of graphene were used: graphene made from the sublimation of SiC and epitaxial graphene synthesized by chemical vapor deposition (CVD) onto nickel. Electrical performance of the graphene transistors were found to vary significantly depending on the local graphene microstructure. The gate dielectric was found to crack on thick regions of graphene but stay intact on thin regions. Dielectric charging resulted in hysteretic effects in device performance. As consistent with HfO_2 used in silicon CMOS devices, electron mobilities were lower than hole mobilities in the fabricated graphene FETs.

Thesis Supervisor: Jing Kong
Title: Assistant Professor, Department of Electrical Engineering and Computer Science

Thesis Supervisor: Jakub Kedzierski
Title: Assistant Group Leader, MIT Lincoln Laboratory Group 88

Acknowledgments

First and foremost, I acknowledge and thank everyone who worked on the graphene project at MIT Lincoln Laboratory (MIT LL): Jakub Kedzierski, Paul Healey, Peter Wyatt, and Craig Keast for design and process development, as well as Cynthia Costa and the rest of the staff at the LL Microelectronics Lab for performing the processing steps. My thesis was the culmination of everyone's contributions. My work would not have been possible without all of you.

I acknowledge and thank my thesis professor, Professor Jing Kong, as well as Alfonso Cecco, for providing CVD graphene samples and for sharing their knowledge of the graphene CVD growth process.

I acknowledge and thank Professor Walt de Heer at the Georgia Institute of Technology for providing graphene/SiC samples and for sharing his knowledge of the SiC sublimation process.

I acknowledge and thank John Hennessy for his help regarding the HfO_2 ALD process.

I acknowledge and thank Donna Lennon at MIT LL for her help and guidance regarding PMMA.

I acknowledge and thank Professor Akinwande and Annie Wang for their help and guidance regarding Parylene-C.

I especially thank my supervisor, Jakub Kedzierski, for his mentorship, guidance and patience during the course of this project. I also thank my group leader, Craig Keast, for giving me the opportunity to work on LL's graphene project.

I acknowledge and thank the MIT VI-A program, Professor James Roberge, Kathy Sullivan, and Gary Hackett for the opportunity to work at MIT LL.

I thank my family for their morale support. Finally, I extend my deepest gratitude to Stephen Hou for his encouragement and infinite understanding.

THIS PAGE INTENTIONALLY LEFT BLANK

Contents

1 Introduction **17**

1.1 Motivations for Graphene Transistors: Limitations of Silicon Technology . . 17

1.2 The Excitement about Graphene 18

1.3 Previous and Current Work to Produce Graphene 19

1.4 Previous and Current Work on Graphene FETs 20

1.5 Why Focus on the Gate Dielectric? 21

1.6 Dielectric Basics 21

1.7 The Role of Dielectrics in MISFETs and MOSFETs 22

1.8 The Disadvantages of a Large Dielectric Constant 23

2 The Dielectric Materials Search **25**

2.1 The Search on Paper: Candidate Materials 25

2.1.1 Oxides 25

2.1.2 Nitrides 26

2.1.3 Organic and Polymer Dielectrics 26

2.2 The Search by Experiment 27

2.2.1 Spin On SiO_2 28

2.2.2 Parylene-C 28

2.2.3 Polyimide 29

2.2.4 HfO_2 29

3 Fabricating Graphene Transistors Using Graphene on SiC **31**

3.1 Making Graphene on SiC 31

3.2 Fabrication Process for Transistors 32

4 Performance of Graphene/SiC Transistors with HfO_2 Gate Dielectric 35

4.1 Carbon Face Device Performance 36

4.2 Silicon Face Device Performance 39

5 Fabricating Graphene Transistors Using CVD-Grown Epitaxial Graphene 41

5.1 Synthesizing Epitaxial Graphene on Nickel via CVD Growth 41

5.2 Fabrication Process for Transistors 42

6 Performance of CVD-Grown Epitaxial Graphene Transistors with HfO_2 Gate Dielectric 45

7 Discussion: Comparing the Performance of Evaporated HfO_2 on Graphene/SiC and on CVD-Grown Epitaxial Graphene 47

8 Conclusion 49

A Tables 51

B Figures 55

List of Figures

B-1 An artist's rendition of the graphene honeycomb crystal structure. Image taken from [17]. ©Chris Ewels www.ewels.info 56

B-2 Comparing topologies of a Si MOSFET and a top-gated graphene MISFET. (A) Textbook topology of a Si metal-oxide-semiconductor field effect transistor (MOSFET). The semiconductor is Si. The dielectric is SiO_2 . Note that the source/drain contacts are highly doped regions in the Si. The gate is usually heavily doped polysilicon instead of metal. (B) Topology used for a top-gated graphene metal-insulator-semiconductor field effect transistor (MISFET). The semiconductor is the graphene. The insulator is some sort of dielectric. The metal is for the top gate. 57

B-3 Topology of a MIS capacitor used to test candidate dielectric devices. . . . 58

B-4 Spin on glass (also called flowable oxide, or "FOX") was tested in a MIS capacitor structure. (A) C-V data for $\sim 1\mu$m thick spin on glass cured at 350°C for 15 minutes. The film was much too thick to allow gate modulation at the voltages tested. (B) Optical image showing cracks in the spin on glass after curing. 59

B-5 C-V data for 100nm thick Parylene-C. The film was thin and soft, allowing probe tips to easily puncture the film during MIS capacitor testing. 60

B-6 C-V data for 90nm polyimide cured for 30 minutes at 400°C. (A) Repeated measurements on the same polyimide test capacitor showed little trace-retrace hysteresis. (B) The flat band capacitance increased continually with repeated measurements, indicating the polyimide accumulated charge during each voltage sweep. 61

B-7 C-V data for HfO_2 . (A) C-V data for 50nm evaporated HfO_2 deposited at a substrate temperature of 150°C. Hysteresis and a noticeable kink caused by charge trapping are evident. (B) C-V data for 13nm ALD HfO_2 . Very little hysteresis is visible. No significant changes to the dielectric were evident after repeated measurements. 62

B-8 Crystal structure of SiC lattice. Blue atoms represent Si, red atoms represent C (or vice versa). The lines connecting the atoms are meant to emphasize lattice structure and do not represent bonds. (A) Top view. Different layers of the same atom are arranged in a hexagonal honeycomb structure. (B) Side view. Si and C atoms form orderly stacked, hexagonally arranged layers. Image taken from [1]. 63

B-9 AFM images showing the SiC substrate step by step through the graphitization process. After the SiC is graphitized, it is transferred to MIT Lincoln Laboratory for device fabrication. Image taken from [31]. 64

B-10 Optical and AFM images of graphene grown on the C-face and Si-face of SiC. Graphene grown on the C-face appears non-uniform in brightness, whereas graphene grown on the Si-face appears much more uniform. Image taken from [31]. 65

B-11 Optical images illustrating the device fabrication process. (A) The first step is to pattern the graphene conduction channels. The channel shape is supposed to be rectangular – the rounded edges are lithographic artifacts. (B) The second step is to pattern Ti/Pt source/drain electrodes. Again, rounded edges are artifacts from lithography. (C) The third step is to deposit HfO_2 . Here, the wafer is coated with photoresist. Openings in the resist, exposing the HfO_2 , are for Al gate deposition. (D) A finished FET device. 66

B-12 AFM image a finished graphene FET. The graphene film in this device is roughly 7nm thick. 67

B-13 Composite image of a graphene/SiC sample after device fabrication. Probe marks can be seen on the Al pads. 68

B-14 Optical images of Graph_A sample C-711 after all processing steps have been finished. (A) The HfO_2 cracks were only observed on top of the graphene film and not on the SiC. (B) The Al gate metal cracked only on top of cracked HfO_2 69

B-15 Electrical data for Graph_A graphene/SiC sample C-711. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. Devices from this experiment had the lowest electron and hole mobilities. 70

B-16 Optical images of Graph_B sample C-712 before Al gate deposition and after HfO_2 deposition. Photoresist covers all areas of the wafer except an opening for the Al gate. The HfO_2 only cracks on top of the graphene and does not crack on either the SiC or on the Pt source/drain electrodes. (A) Faint cracks are visible in the HfO_2 over the graphene conduction channel. Inset: optical image of the same device prior to HfO_2 deposition showing thin regions of graphene. (B) Thick, noticeable cracks are visible over the graphene conduction channel. Inset: optical image of the same device prior to HfO_2 deposition showing thick regions of graphene. 71

B-17 Sample C-712 experienced shorting between the Al gate to the graphene conduction channel through cracks in the gate dielectric. The shorts were vaporized after current annealing the devices, which involved passing a large amount of current (roughly 10mA) from the gate to the source/drain. (A) Optical image of a device taken prior to Al gate deposition. Cracks are visible in the HfO_2 gate dielectric over the graphene conduction channel. (B) Optical image of the same device after current annealing showing black burn marks on the Al gate. 72

B-18 Electrical data for Graph_B graphene/SiC sample C-712. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. Devices from this experiment had the highest electron and hole mobilities. 73

B-19 Optical images of C-715. (A) Image of the graphene conduction channel after active area etch. (B) Image of the graphene conduction channel after Pt source/drain deposition and lift off. The graphene is visibly damaged. (C) Image of the graphene conduction channel before Al gate deposition and after HfO_2 deposition. There are visible purple-colored regions where the damaged graphene interfaced with the HfO_2 74

B-20 Electrical data for Graph_B graphene/SiC sample C-715. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. On average, the electron mobility is lower than the hole mobility. 75

B-21 Optical images of devices from Graph_C sample C-781. (A) This device has graphene missing from the conduction channel. Its electrical performance was not included in conductivity and mobility analysis. (B) This device has uniform graphene in the conduction channel. Its electrical performance was included in all data analysis. 76

B-22 Electrical data for Graph_B graphene/SiC sample C-781. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. On average, the electron mobility is lower than the hole mobility. 77

B-23 Plot showing the relationship between minimum conductivity vs. minimum cross-sectional thickness in the graphene conduction channel. The relationship suggests the thinnest graphene cross section acts as the bottleneck to charge conduction. The data also shows that thicker graphene regions conduct more current, and the linear relationship implies that each graphene sheet conducts a comparable level of current, which is given by the slope of the best fit line. 78

B-24 When looking at graphene under an optical microscope, brighter regions correspond to thicker graphene and dimmer regions correspond to thinner graphene. (A) The normalized graphene brightness (NGB) is calculated as (C_{int}-SiC_{int})/SiC_{int}, where C_{int} is the intensity (brightness) of the carbon region and SiC_{int} is the intensity of the SiC region. The intensity values are found using a histogram from a program such as Gimp. The NGB value tells how bright a graphene region is relative to its SiC background. (B) AFM measurements of graphene step heights plotted against NGB. The linear relationship confirms that brighter looking regions correspond to thicker regions of graphene. 79

B-25 Optical images comparing graphene conduction channels between a Si-face and a C-face graphene/SiC sample. (A) Device from S-767 after Pt source/drain patterning. The graphene conduction channel is barely visible. (B) Device from C-781, also after Pt source/drain patterning. The graphene conduction channel is much brighter than the graphene from S-767, indicating a much thicker graphene film. 80

B-26 Electrical data for Graph_B graphene/SiC sample C-781. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. On average, the electron mobility is lower than the hole mobility. 81

B-27 Dielectric charging effects for a device on graphene/SiC sample S-767. (A) Shifts in the minimum conduction voltage between the first and second I_d–V_g measurements. (B) Changes in charge carrier mobility between the first and second I_d–V_g measurements. 82

B-28 AFM image showing the post-anneal grain structure of the Ni used for graphene CVD. 83

B-29 Optical image of CVD graphene after it is transferred onto a 500nm oxide wafer. A prominent grain structure in the graphene is evident in the scattering of light (thin) and dark (thick) regions. 84

B-30 AFM image of CVD graphene after it is transferred onto a smooth oxide wafer. Ripples and folds in the graphene are evident, suggesting that the graphene exists as a continuous layer. 85

B-31 Optical images of the same graphene device through the various fabrication steps. (A) The graphene conduction channel is patterned. (B) Pt source/drain contacts are patterned onto the graphene. (C) A finished graphene device after HfO_2 deposition and Pt gate deposition. As was the case for graphene/SiC devices, the HfO_2 cracked on thick regions of graphene. . . . 86

B-32 Optical images of finished Graph_F devices showing cracks in the Pt/HfO_2 gate stack on thick graphene regions but not on thin regions. (A) The HfO_2 gate dielectric and Pt gate showed visible cracks on top of the graphene conduction region. Inset: optical image of the same device prior to HfO_2 deposition. The graphene conduction channel is mostly uniform, thick graphene. (B) The HfO_2 gate dielectric and Pt gate shows no visible cracks on top of the graphene conduction region. Inset: optical image of the same device prior to HfO_2 deposition. The graphene conduction channel is mostly uniform, thin graphene. 87

B-33 AFM image of a Graph_F device with mostly uniformly thin graphene. Step height measurements indicate the graphene is roughly 1.5nm thick. This is the same device shown in Figure B-32(B). 88

B-34 Electrical data for Graph_F. (A) I_d-V_g data for the different devices. V_d was held at 0.1V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. 89

List of Tables

A.1 Candidate oxides for Graphene FETs. Note that as the dielectric constant increases, the band gap decreases. All dielectric constant and band gap values taken from [63]. 52
A.2 Candidate nitrides for Graphene FETs. 53
A.3 Candidate organic and polymer dielectrics for Graphene FETs. 54

THIS PAGE INTENTIONALLY LEFT BLANK

Chapter 1

Introduction

1.1 Motivations for Graphene Transistors: Limitations of Silicon Technology

Over the past five decades, the sizes of field effect transistors (FETs) have been getting exponentially smaller, causing the number of transistors per chip to increase in accordance with Moore's Law [26]. The process has caused all aspects of the silicon CMOS transistor to scale downward in size, including not only the device's length and width but also the thickness of the gate dielectric. As the gate dielectric falls below about 1.3nm in thickness [53], direct electron tunneling creates intolerably large leakage currents, essentially turning the insulator transparent to electrons. The leakage current per transistor, multiplied by the many millions of transistors per chip, drained batteries too quickly and easily caused a chip to burn itself within seconds without adequate cooling. These complications are some of the most visible limitations to the continuation of Moore's Law [7].

In order to reduce transistor leakage current, researchers in both academia and industry have looked for years at alternative gate dielectric materials to the currently used SiO_2 . A material with a higher dielectric constant would allow an increase in the physical thickness of the gate dielectric while retaining the performance of thin SiO_2 devices.

Other researchers have looked beyond silicon altogether in the search for ever improved transistors in terms of size, speed, and application. Organic and polymer FETs have uses in flexible circuits and display technologies [35], yet its usefulness in logic is limited since the highest reported charge carrier mobilities have been well below $10\text{cm}^2\text{V}^{-1}\text{s}^{-1}$[13] (com-

pared to >1000 $cm^2V^{-1}s^{-1}$[56] for doped Si devices) and switching frequencies have been limited to about 1KHz [12]. Carbon nanotubes, which have charge carrier mobilities on the order of 10,000$cm^2V^{-1}s^{-1}$, have been successfully used in field effect transistors as well [39, 15, 28], but controlling all the relevant nanotube characteristics, such as radius, chirality, and doping, has thus far remained an unsolved problem. When a carbon nanotube becomes "unrolled", it becomes graphene. Graphene retains many of the benefits of carbon nanotubes, including high charge carrier mobilities. Thus, many researchers are now focusing on graphene for high mobility field effect transistors.

1.2 The Excitement about Graphene

Graphene is a two dimensional, single atom thick crystal of carbon arranged in a hexagonal honeycomb structure. Even though most people are unfamiliar with graphene, they are very familiar with graphite, graphene's 3D counterpart. One of the most common uses of graphite is pencil lead, which is just the repeated (and disordered) stacking of graphene layers. An artist's rendition of graphene is shown in Figure B-1.

Graphene has been a scientific thought experiment ever since the 1940s [62]. However, for decades, single layer atomic films were thought to be thermodynamically unstable and therefore not to exist. This viewpoint did not change until single-layer graphene was discovered in 2004 [43, 21][1]. Since then, researchers have found that the charge carriers in graphene have a mobility on the order of 10,000$cm^2V^{-1}s^{-1}$even at ambient temperatures [21], whereas charge carrier mobility in doped Si is only on the order of 1,000$cm^2V^{-1}s^{-1}$[56]. The electronic structure of graphene shows that the valence and conduction bands touch at the Dirac cone, resulting in graphene's ambipolar conduction capabilities (i.e. the ability to conduct both holes and electrons).

Graphene is considered to exhibit one of the highest charge carrier mobility of all materials [21]. Its intrinsically high mobility makes it a promising material for ultra fast electronics operating in the THz frequencies [21]. However, as of today, using graphene for logic devices is still a problem. As stated above, the valence and conduction bands of graphene meet at the Dirac point, which means that single layer graphene is a semimetal with no band gap. Modulating the source-drain current using the gate voltage in a graphene FET simply

[1] Researchers in the 1990s were able to deposit single-layer graphitic films, but they did not use the films for electronic purposes [45].

shifts the Fermi energy from allowing hole conduction to allowing electron conduction and vice versa, with no band gap in between. Graphene transistors thus have very low on/off current ratios – in effect the transistor is unable to turn “off”. Attempts to create a band gap in graphene are still being investigated. Some methods have already been successfully demonstrated [44, 24, 66].

1.3 Previous and Current Work to Produce Graphene

Graphene was discovered in 2004 by the mechanical exfoliation of highly oriented pyrolytic graphite (HOPG) [43]. The procedure, commonly known as the “tape method,” uses a piece of tape to repeatedly peel off layers of HOPG. Single and few-layer graphene sheets are then found in the graphitic debris. Such graphene is randomly located, limited in size from a few microns to a few hundred microns and, most importantly, unscalable for large scale electronic development.

Other methods have been attempted to produce graphene[2] in a large scale and/or predictable manner, including:

- Chemical exfoliation, which is a wet chemistry intercalation method that inserts molecules into graphite in order to separate the graphene sheets. Unfortunately, this method has thus far failed to produce single or few-layer graphene usable for device fabrication [21, 52, 60].

- Epitaxial growth of graphene by chemical vapor deposition (CVD), which involves the deposition of carbon onto a crystal template that is lattice-matched to graphene. This method was first successfully demonstrated in the 1990s [45], but the films were not applied to electronics. Recently, this method has successfully produced regions of few-layer graphene with an area of roughly 1 cm^2 [50]. Thus far, the quality of the graphene seems to be limited by the quality of the lattice-matched template. However, this method has the potential to produce large area, single to few layer graphene usable by the electronics industry.

[2]By definition, graphene is single-layer, single-crystal carbon. Multi-layered graphene is technically considered graphite. However, due to the limitations of current graphene synthesis methods, few layer graphene is still considered “graphene”. At thicknesses of 1 – 10 monolayers, few-layer graphene has been found to behave more similarly to single-layer graphene than to bulk graphite [21].

- Silicon carbide sublimation, which involves the baking of single-crystal SiC in vacuum at high temperatures (∼1400°C), sublimating Si and leaving behind a carbon rich film on the faces of the SiC crystal. The carbon graphitizes to form few-layer graphene [25, 6, 19]. The current method of SiC sublimation uses only chiplets of SiC that are a few millimeters in length and in width. Theoretically, it is possible to start with an entire SiC wafer and end with an entire wafer of graphene. Such scalability is extremely desirable, albeit still in the distant future. However, given that a 3" diameter SiC wafer currently costs about $4000 [2], making graphene in this way would be very expensive.

1.4 Previous and Current Work on Graphene FETs

The basic topology of any FET consists of a semiconductor, source, drain, gate, and gate dielectric. Graphene FETs are simply FETs with graphene as the conduction channel. The graphene rests on some sort of insulator, such as SiC (if the graphene is made by SiC sublimation) or SiO_2 on top of a silicon wafer (commonly used for exfoliated and epitaxial graphene). Unlike the textbook Si MOSFET, where the source/drain contacts are doped into a bulk piece of Si, the source/drain contacts for a graphene FET are usually thin metal films deposited directly onto the graphene itself. A comparison of the traditional Si FET topology and the graphene FET topology is shown in Figure B-2.

Successful graphene FETs have thus far mostly been demonstrated on graphene flakes obtained from mechanical exfoliation. Room temperature carrier mobilities on the order 10,000 $cm^2V^{-1}s^{-1}$have been achieved using single or few-layer exfoliated graphene [43, 23]. However, devices made from mechanically exfoliated graphene are only proof-of-concept and not suitable for industrial scale production.

Graphene FETs on SiC have also been demonstrated, but the performance is relatively poor. Published literature as of early 2008 show devices exhibiting a room temperature field effect mobility of only about 500 $cm^2V^{-1}s^{-1}$[23]. Data from graphene FETs made from epitaxial graphene have yet to be published. Thus, much work still remains to fabricate graphene FETs with high mobility in an industrially compatible manner.

1.5 Why Focus on the Gate Dielectric?

When transistors were first made, there were many different semiconductors to choose from. Silicon and germanium were both popular, and it wasn't at all clear that silicon would be the better choice [34]. However, those transistors had repeatedly exhibited non-ideal behavior and the problems were traced to the interface between the semiconductor and the gate dielectric [34]. For reliable high performance devices, the interface between the conduction channel and the gate dielectric must have minimal interface trap densities (i.e. dangling bonds) and minimal carrier scattering (to maximize mobility) [63]. Eventually, it was found that thermally grown SiO_2 provided the best gate dielectric – semiconductor interface [34, 27] due to the fact that thermal SiO_2 is produced when O_2 incorporates *into*, rather than *onto*, a Si wafer. It was partially because of SiO_2 that the electronic device industry adopted Si [27].

Thus, the choice of gate dielectric will greatly impact the behavior of graphene based FETs. Unlike traditional FETs with a Si conduction channel, FETs with a graphene conduction channel will not have the option of growing a gate dielectric such as SiO_2 , necessitating the deposition of a dielectric onto graphene. Experience from Si technology development show that deposited dielectrics usually have problematic interface layers. Charge trapping affects carrier mobility and often shifts transistor threshold voltages [56]. The choice of dielectric material and deposition technique can potentially greatly affect the performance of graphene based FETs.

1.6 Dielectric Basics

There are three types of solid state electronic materials: conductors, semiconductors, and insulators. In a conductor, electrons can move freely from one atom or molecule to another, thereby allowing charge carriers to conduct current. In contrast, a dielectric is an electrical insulator in which the opposite is true. Electrons in a dielectric can only move within, rather than between, atoms and molecules (unless the charge carrier traverses a large band gap). This forces the electrons to stretch and rotate to form dipole moments, causing the dielectric material to become polarized under an applied electric field [22]. The extent to which a material becomes polarized is a physical property of the material and is quantitatively captured by its dielectric constant. Specifically [22]:

$\vec{P} \equiv$ dipole moment per unit volume, which depends on the material and on the applied electric field $\vec{E}$,

$\vec{P} = \varepsilon_0 \chi_e \vec{E}$, where χ_e is the electric susceptibility that depends on the material's microscopic structure, and

$\mathrm{K} \equiv 1 + \chi_e$, where K is the dielectric constant of the material.

Dielectrics are commonly used as the sandwich layer between the plates of a parallel plate capacitor. An external field $\vec{E}$ causes the dielectric material to polarize, creating a polarization field $\vec{P}$ in the opposite direction of $\vec{E}$, thus effectively decreasing the $\vec{E}$ field in the dielectric. This in turn causes an *increase* in the system's capacitance: for an air filled capacitor, $C = \varepsilon_0 A/t$, where ε_0 is the permittivity of free space. For a dielectric filled capacitor, $C = K\varepsilon_0 A/t$, where K is the dielectric constant [56, 41].

1.7 The Role of Dielectrics in MISFETs and MOSFETs

In the MISFET (metal-insulator-semiconductor FET) topology, a dielectric is used as a sandwich layer between the metal gate electrode and the semiconductor. This metal-insulator-semiconductor capacitor is called the MIS capacitor for short. The most common MISFETs are MOSFETs, where the insulator is SiO_2 . Hence the name metal-oxide-semiconductor FET.

What makes the MISFET work is the MIS capacitor. Applying a voltage to the gate distorts the semiconductor's electronic band structure at the dielectric-semiconductor interface, which changes the distribution of electrical charges at that interface [56]. When the applied voltage is positive, band bending causes negative charges to accumulate at the interface. When the voltage is negative, band bending causes positive charges to accumulate at the interface. If the semiconductor is n-type, negative charges (positive voltage) represent accumulation and positive charges (negative voltage) represent inversion. If the semiconductor is p-type, positive charges (negative voltage) represent accumulation and negative charges (positive voltage) represent inversion. Depletion occurs when the system transitions from accumulation to inversion – the system has very few of either charge. It is the presence of inverted charges that allow the MISFET to conduct current, and the inversion charge is modulated by the gate voltage. Once a potential difference exists between the source and drain electrodes, applying a gate voltage of the correct polarity causes charge

inversion at the dielectric-semiconductor interface, connecting the source and drain, thus allowing the flow of current.

In the ideal situation, the amount of charge that is induced to flow depends only on the capacitance of the MIS-capacitor. Ignoring the effects of the inversion capacitance, the inversion charge is represented by the basic capacitor equation $Q = CV$, with $C = K\varepsilon_0 A/t$. An increase in C will result in a larger Q and ultimately result in a larger source–drain current even though other parameters are held constant. However, in the physical MIS capacitor system, several non-idealities exist. Accumulation of fixed charge can shift the threshold gate voltage, sometimes hysteretically. Film defects, charge traps at the dielectric-semiconductor interface, and various types of scattering mechanisms can drastically reduce charge carrier mobility, causing the source–drain current to drop.

For the past few decades, the scaling of Si technology has increased C by decreasing t. However, as t cannot be decreased without exposing the system to further quantum tunneling, researchers are looking to increase C by increasing K. Hence, the future of transistor technology will most likely incorporate high-K dielectric materials.

1.8 The Disadvantages of a Large Dielectric Constant

It has been mentioned above that the use of a high-K dielectric material for Si technology will aid in device performance by increasing the FET current while holding other parameters (voltage, capacitor area, dielectric thickness) constant. If instead a low-K material is used, then either A would increase or t would have to decrease even more, neither of which would be feasible for small, low-power circuits. However, it is important to note that high-K materials have their drawbacks.

First, dielectric materials with larger atoms (such as Hf and Ti compared to Si) generally tend to have larger higher dielectric constants, but the tradeoff is that these materials also have smaller band gaps [63]. Smaller band gaps would increase the probability of charge carrier tunneling, and this problem will offset some of the high-K gains in increased physical thickness. Second, it is now understood that the physical properties responsible for the high K are likely to degrade carrier mobility, at least for Si MOSFETs [20]. This consequence is one major disadvantage of a high-K dielectric when compared to SiO_2 for silicon CMOS circuitry.

THIS PAGE INTENTIONALLY LEFT BLANK

Chapter 2

The Dielectric Materials Search

2.1 The Search on Paper: Candidate Materials

The search for candidate dielectric materials began with an extensive literature search. The following is a brief description some of the materials that were considered. A list of investigated materials is shown collectively in Tables A.1, A.2 and A.3.

2.1.1 Oxides

Oxides are perhaps the most commonly used dielectrics in the Si CMOS industry. SiO_2 is *the* dielectric used in the CMOS device gate stacks. As the Si industry is investigating alternative high-K gate dielectric materials, much attention has stayed within the realm of oxides.

Many of the candidate oxides considered for graphene FETs have high dielectric constants (relative to SiO_2), the reason being that graphene devices will undoubtedly face the same scaling pressures as Si CMOS devices. However, there are documented problems with high-K oxides. High-K materials with larger atoms tend to have smaller band gaps relative to SiO_2 [63], offsetting some of the gains with respect to smaller leakage currents. The physical properties responsible for the high dielectric constant have been shown to degrade electron mobility in Si MOSFETs [20]. In addition, since high-K oxides require film deposition, there also usually exists a defective transition region between the oxide and semiconductor [38]. Most of the carrier degradation experienced in high-K oxides so far has been attributed to the poor quality of the dielectric film [57].

Of the many oxides available, there seems to be a consensus that hafnium oxide (HfO_2) is a very promising material. Compared to other oxides, HfO_2 has a relatively high dielectric constant (K ∼25, [63]) while simultaneously retaining a relatively large band gap (E_G ∼5.8eV, [63, 67]). Hafnium based high-K materials have been studied extensively by companies such as IBM and Intel. Intel has recently used Hf based high-K dielectrics for their 45nm technology CMOS chips, which began manufacturing in 2007 [4].

2.1.2 Nitrides

Nitrides are widely used in the Si industry. Silicon nitride (Si_3N_4) and silicon oxynitrides (SiO_xN_y) may be the most commonly used nitrides. They are often utilized as diffusion barriers, electrical insulators, protection layers, passivation layers, etch stop masks, and capacitor dielectrics [51]. Nitride-oxide and nitrided oxide gate stacks are often used to reduce leakage currents [51]. Various metal nitrides and metal oxynitrides, such as hafnium silicon oxynitride, have been considered for use in gate stacks as well [48].

2.1.3 Organic and Polymer Dielectrics

Organic and polymer dielectrics are commonly used as the gate dielectric in organic field effect transistors (OFETs), in which the semiconducting material is itself an organic or polymeric material. Most organic and polymer dielectrics have low dielectric constants (K $\leq$ 4). These dielectrics can usually be processed at low temperatures in order to be compatible with the low thermal budgets of OFET fabrication. Deposition techniques include spin-on, chemical vapor deposition, and wet chemical interactions (such as self assembled monolayers). Oftentimes, many different off-the-shelf polymers are mixed together to form usable gate dielectric materials [32].

Two organic dielectrics are especially promising on paper. The first is BCB (bisbenzocyclobutene), which has a dielectric constant of roughly 2.65 [46]. BCB is a spin-on polymer that was developed as an interconnect dielectric [9, 40]. It was later found that the material can form defect-free films that are as thin as a few tens of nanometers [9]. The cross-linked polymer is stable in ambient temperatures and against solvents. Unlike most other polymer dielectrics, which mostly allow only hole conduction, BCB has been found to allow the conduction of both electrons and holes since it lacks electron-trapping OH groups [10]. Since graphene also allows ambipolar conduction, BCB would be a promising gate

dielectric for graphene FETs.

The second promising organic dielectric is called self-assembled monolayers (SAMs). To deposit SAMs, surface interactions between the substrate and the dielectric material must ensure that only one monolayer of the dielectric is deposited. Densely packed and highly ordered SAMs of alkyl chains have been shown to form dielectric layers as thin as 2nm while simultaneously having an electron tunneling barrier of roughly 4.5eV [61, 8, 11]. SiO_2 at this thickness, in contrast, only has an electron tunneling barrier of 0.5-3eV [61]. SAMs used as gate dielectrics in Si transistors have been shown to reduce leakage currents by roughly 8 orders of magnitude [61, 8]. SAMs made from n-octadecylphosphonic acid have recently been used as the gate dielectric for organic complimentary circuits [33].

2.2 The Search by Experiment

After examining candidate dielectrics on paper, testing the physical material was necessary. Of the materials listed above, many potentially promising dielectrics were avoided. Oxides that required deposition via an O_2 plasma were not considered, since the O_2 plasma can easily damage the graphene. BCB and SAMs, although promising for OFETs, required extensive knowledge of wet chemistry and were not readily available. Materials that were not compatible with our device fabrication process, such as PMMA (which readily dissolves in acetone), were also dropped from consideration. The materials we did test were required to be compatible with our fabrication process, readily available, and its deposition process must have been innocuous to graphene.

In order to test a candidate dielectric, MIS capacitors were fabricated to see if the dielectric will successfully allow accumulation, depletion, and inversion. The test structure is shown in Figure B-3. The semiconductor is always bare p-type (100) silicon. The gate metal is usually evaporated aluminum. The test capacitor dimensions were 70μm x 70μm. The Si wafers were used out of the box with no surface cleaning or other treatments. The test capacitors ran through a high-frequency (100KHz) voltage sweep in order to find the accumulation, depletion, and inversion regions. A plot for an ideal C-V curve can be found in [56]. The dielectric materials used, as well as the test results, are discussed below.

2.2.1 Spin On SiO_2

SiO_2 has a dielectric constant of 3.9 and a band gap of roughly 8.9eV [63]. Thermally grown SiO_2 is the most commonly used gate dielectric for silicon transistors. It has also been a common gate dielectric for back-gated graphene flake devices [43, 36, 65].

SiO_2 can be deposited using a variety methods: thermal oxidation of Si, chemical vapor deposition, and spin-on, to name a few. Thermal oxidation of Si produces the best electrical performance, but this method is not applicable for growing SiO_2 on top of graphene. Plasma enhanced chemical vapor deposition is a common method of depositing SiO_2 onto an arbitrary substrate, but the oxygen plasma environment would damage the graphene. The best method available to deposit SiO_2 was thus determined to be spin-on.

Spin-on-glass was spun onto a bare Si wafer at 4000 rpm for 40 seconds and cured at 350°C for 15 minutes. Aluminum top gates were e-beam evaporated and patterned via lift off. The glass was rated to spin to a thickness of 1μm. No compatible solvent was available to allow for a thinner film. MIS capacitor C-V data is shown in Figure B-4(A). The film was much too thick – inversion was not observed in the voltage range tested (-30V to +30V). In addition, the glass cracked in several locations, shown in Figure B-4(B). We therefore concluded that spin-on-glass was not a usable gate-dielectric for graphene transistors.

2.2.2 Parylene-C

Parylene-C has a dielectric constant of roughly 3 [59]. It is an organic material that has been successfully used as gate dielectrics in OFETs, usually in thicknesses ranging from 100nm-350nm [35]. The material was available through a research group on MIT Campus [3]. 100nm of Parylene-C was deposited via chemical vapor deposition onto a bare Si wafer. Aluminum gate electrodes were evaporated through a shadow mask – no lift off process was used due to the Parylene-C sample being gold-contaminated. No post-deposition anneal was performed.

MIS capacitor C-V data for Parylene-C is shown in Figure B-5. The film was a poor dielectric for our purposes. The film was either too soft and/or thin and the probe tips easily penetrated the film. A thicker film would not have been feasible given that the dielectric constant of Parylene-C is so small – the film would need to be much too thin to compete with low equivalent oxide thicknesses. We therefore concluded that Parylene-C would not

be usable as a gate dielectric for our graphene transistors.

2.2.3 Polyimide

Polyimide has a reported dielectric constant between 2.6 and 3.3 [14, 46, 59]. Polyimide is a spin-on polymer that was used in the 1990s as an interlayer dielectric for Si circuitry [14]. Recently, it has also been used as a gate dielectric material in organic FETs at thicknesses in the range of hundreds of nanometers [30, 58]. Polyimide usually requires a curing temperature above 300°C, although certain polyimides can be cured at temperatures as low as 180°C [30, 58].

We used polyimide dissolved in a solvent. The solution was spun at 2000 rpm for 40 seconds, resulting in a 90nm thick film. The polyimide was then cured at 300°C, 350°C, and 400°C. C-V data for the films cured at 400°C is shown in Figure B-6. Trace and retrace measurements showed drastically reduced hysteresis when the film was cured at 400°C. The polyimide also appeared to charge up with each voltage sweep since the flat band capacitance increased continually with repeated measurements. Hysteresis returned after several weeks, most likely due to polyimide's natural tendency to absorb water from the air [14].

Polyimide was a very promising material. Unfortunately, attempts to spin polyimide onto a graphene/SiC sample was unsuccessful as the film would not wet the SiC surface. No other deposition method for polyimide was available. We therefore had to abandon polyimide as a usable dielectric for our graphene transistors.

2.2.4 HfO_2

HfO_2 has a dielectric constant of 25 and a band gap of roughly 5.7eV [63]. HfO_2 has long been considered a promising alternative gate dielectric by the silicon community due to its large dielectric constant and relatively large band gap. Intel has recently used Hf based high-K dielectrics for their 45nm technology CMOS chips [4].

However, of the many metal oxides known to degrade mobility by increasing optical phonon scattering, HfO_2 is amongst the worst [63]. Theoretical calculations show that for the same equivalent thickness, HfO_2 gives a mobility that is roughly 1/3 of SiO_2 [20]. HfO_2 has also been found to range from amorphous to polycrystalline, depending on deposition method and film thickness [42]. Polycrystalline dielectrics tend to break down more

easily since charge carriers can travel along the grain boundaries. Nevertheless, for low voltage applications, HfO_2 was worth testing.

We tested HfO_2 deposited using two different methods. First, 50nm of HfO_2 was thermally evaporated onto a bare Si wafer. The wafer temperature was 150°C during deposition. 100nm of aluminum was thermally evaporated and patterned for the gate. The C-V performance of the evaporated HfO_2 is shown in Figure B-7(A). Hysteresis is evident, as well as charge trapping manifested in a kink in the data. However, even so, HfO_2 successfully demonstrated charge inversion (as was expected), and its deposition (thermal evaporation) onto graphene/SiC would not have been problematic. We therefore decided to use evaporated HfO_2 as our graphene transistor gate dielectric in experiments Graph_A-C and Graph_F.

A second form of HfO_2 was tested as well. 13nm HfO_2 was deposited onto a bare Si wafer using atomic layer deposition (ALD) performed at MIT Micro Technology Laboratory. The wafer temperature was 200°C during deposition. The film underwent a 350°C nitrogen anneal for 30 minutes, 20nm platinum gate deposition and patterning, followed by a 400°C nitrogen anneal for 30 minutes. A platinum gate was used instead of an aluminum gate due to the chemical inertness of platinum [29]. The C-V performance of the ALD HfO_2 is shown in Figure B-7(B). Hysteresis is minimal and the dielectric did not seem to accumulate charge. ALD HfO_2 was the most promising dielectric we tested. We decided to use ALD HfO_2 as our gate dielectric in the experiment Graph_D.

Chapter 3

Fabricating Graphene Transistors Using Graphene on SiC

3.1 Making Graphene on SiC

The graphene films we used were grown from SiC at the Georgia Institute of Technology. Full details of the graphene growth process can be found in [25]. A brief summary of the process is given below.

The Si and C atoms in SiC are arranged as alternating layers of hexagonally packed Si and C, as shown in Figure B-8. A fresh, ungraphitized SiC wafer is cut such that one face terminates with a Si layer (named the Si-face) and the other face terminates with a carbon layer (named the C-face).

At Georgia Tech, pieces of single crystal 4H-SiC (0001) of size 3.5mm x 4.5mm x 0.3mm are heated in a vacuum chamber repeatedly at around 1400°C [31, 25]. AFM images taken at various steps of the graphitization process are shown in Figure B-9. Under these conditions, the outermost layers of Si atoms sublime, leaving behind carbon layers that form thin carbon films on both faces of the SiC crystal. The carbon films subsequently graphitize to form multiple layers of continuous, multi-crystal graphene. The layers are epitaxially ordered and stacked. The graphitization processes for the two SiC faces are different. Consequently, a given SiC sample can only have one face graphitized properly, and only the properly graphitized face is intended for device fabrication. Thus, the graphene on a graphene/SiC sample will be designated as either C-face or Si-face graphene.

Graphene on the C- and Si-faces look and behave differently. Figure B-10 shows optical and AFM images of a representative C-face and a representative Si-face sample. Under an optical microscope, the C-face has visible patches of brighter and darker regions, which correspond to thicker and thinner regions of graphene respectively. The brightness-thickness relationship is discussed further in Chapter 4. In contrast, the Si face optically appears to be much more uniform in graphene thickness. It is important to note that the AFM height variation of tens of nanometers represents not the graphene thickness, but rather the underlying roughness of the SiC. To find the graphene thickness, patterns were etched into the graphene by an O_2 plasma and AFM measurements of the step heights were taken. The graphene was found to be below 15nm in thickness.

Due to the large quantity of graphene/SiC samples produced at Georgia Tech, each sample is labeled with a number. For example, the label C-712 represents sample #712 with graphene grown on the C-face. The label S-712 represents sample #712 with graphene grown on the Si-face. Again, for each sample only one face – either the C-face or the Si-face – is intended for graphene device fabrication.

3.2 Fabrication Process for Transistors

Graphene transistors were fabricated in four separate experiments: Graph_A (sample C-711), Graph_B (samples C-712 and C-715), Graph_C (samples C-781 and S-767), and Graph_D (sample C-783). C-face graphene samples were used in all four experiments. Due to the lack of available Si-face graphene samples, a Si-face sample was used only in Graph_C. All fabricated transistors were top-gated.

After the graphene was grown at Georgia Tech, the graphene/SiC pieces were delivered to MIT Lincoln Laboratory for transistor fabrication. Since each SiC piece was only 3.5mm x 4.5mm in size, carrier wafers were required. For each wafer, a single graphene/SiC chip was epoxied along with 8 other spacer chips of equal size and thickness. The spacer chips allowed for even exposure when using a contact aligner for lithography.

To fabricate FETs with graphene conduction channels, the graphene active areas were first defined using an O_2 plasma etch. The source/drain electrodes consisted of 2nm evaporated titanium and 20nm evaporated platinum and were defined using a liftoff process. HfO_2 was blanket deposited as the gate dielectric. The gate electrode was also an evapo-

rated metal and also defined using liftoff. Patterning the HfO_2 was unsuccessful in Graph_A and was not attempted in Graph_B-D. A pictorial version of the process is shown in Figure B-11. An AFM image of a finished device is shown in Figure B-12. A composite image of a finished graphene chip is shown in in Figure B-13.

Graphene samples in all three experiments went through the same fabrication process except for the last three steps: HfO_2 deposition, HfO_2 patterning, and the choice of gate metal. Graph_A received 50nm of HfO_2 deposited at a substrate temperature of 50°C. Graph_B received 50nm HfO_2 deposited at a substrate temperature of 150°C. Graph_C received 40nm HfO_2 deposited at a substrate temperature of 100°C. Due to the chronology of events, only Graph_D received ALD HfO_2 , which was roughly 10nm thick and deposited at 200°C.[1] Graph_A-C all had 100nm Al top gates. Graph_D had a 20nm Pt top gate. An unsuccessful attempt was made to pattern the HfO_2 in Graph_A – the step included a 150°C bake that densified the HfO_2 and caused the film to crack and delaminate. HfO_2 patterning was abandoned for Graph_B-D.

[1] The film used for Graph_D was deposited at Cambridge Nanotech. This is not the same film used for the ALD C-V test capacitors, which were deposited at MIT Micro Technology Laboratory.

THIS PAGE INTENTIONALLY LEFT BLANK

Chapter 4

Performance of Graphene/SiC Transistors with HfO_2 Gate Dielectric

Finished graphene transistors were tested for field effect behavior. V_d was held at 0.5V, V_s was held at 0V, while V_g was swept from -3V to +3V. The tests were intended to demonstrate current modulation by the gate. Minimum conductivities and charge carrier mobilities were calculated. The devices tested in Graph_A-D all had their conduction channels sized to be 10μm in length and 5μm in width – they are all supposed to be "identical" devices.

Device conductivity (σ_d) was calculated from the source-drain current (I_d), the source-drain voltage (V_d), the conduction channel length (L) and width (W), and included a correction for the measured Pt series resistance. Carrier mobility was calculated as $\left(\frac{d\sigma_\mathrm{d}}{dV_\mathrm{g}}\right)(WL/C)$, where L and W are as defined above and C is the graphene-to-gate capacitance. The quantity ($d\sigma_\mathrm{d}/dV_\mathrm{g}$) was calculated from the steepest three adjacent points along each branch of the V-shaped $I_\mathrm{d} - V_\mathrm{g}$ curve. Since along each branch only one type of charge carrier (electron or hole) dominates conduction, the terms "electron mobility" will be used for the branch $V_\mathrm{g} > 0$ and "hole mobility" will be used for the branch $V_\mathrm{g} < 0$.

It should be noted that graphene is a semimetal with no band gap. The band structure of graphene implies that the material will conduct both electrons and holes, and the mobilities of both carriers should be roughly equal. The Pt source/drain contacts are also ambipolar and will inject both electrons and holes, depending on the applied voltage. The observed

graphene FET $I_{\rm d}$ - $V_{\rm g}$ curves all exhibit an ambipolar, V-shape characteristic. Negative gate voltages produce conduction dominated by holes, positive voltages produce conduction dominated by electrons. In such a circumstance, even though the source and drain contacts are designated as "source" and "drain," it is important to realize that the low-voltage contact is the electron source and the high-voltage contact is the hole source.

4.1 Carbon Face Device Performance

Graph_A devices from sample C-711 demonstrated successful gate modulation of the source-drain current. The HfO_2 film cracked extensively and delaminated in unintended areas, as shown in Figure B-14, and consequently only a handful of devices worked. Data from the functional devices is shown in Figure B-15. Minimum device currents for Graph_A ranged from $\sim 10\mu$A to $\sim 700\mu$A. Electron mobility ranged from 150 to 600 $cm^2V^{-1}s^{-1}$. Hole mobility ranged from 350 to 1050 $cm^2V^{-1}s^{-1}$.

Graph_B devices performed differently from Graph_A devices, with the only processing difference being changes to the gate dielectric. Within Graph_B, the devices made on the two separate graphene samples also performed differently. In sample C-712, the HfO_2 cracked extensively. As shown in Figure B-16, devices with thicker graphene films tended to have larger cracks. The cracks in the HfO_2 allowed the aluminum gate material to penetrate the dielectric and short directly to the graphene conduction channel for most transistor devices. In order to remedy this problem, large amounts of current (roughly 10mA) were intentionally passed from the gate to the source/drain. This sort of current annealing caused the Al shorts to vaporize, resulting in visible burn marks, as seen in Figure B-17. After the Al shorts were eliminated, the C-712 devices successfully demonstrated gate modulation of the source/drain current. Electrical data from C-712 devices are shown in Figure B-18 . Minimum conductivities ranged from 400μS to 7000μS between tested devices. Electron mobility ranged from 500$cm^2V^{-1}s^{-1}$to 4000 $cm^2V^{-1}s^{-1}$. Hole mobility ranged from 800 to 3400$cm^2V^{-1}s^{-1}$. These were the highest mobilities of all graphene devices in Graph_A-F. Sample C-715 behaved differently, however. Optical images of the active graphene regions, shown in Figure B-19, indicate that the graphene was damaged in the source/drain lithography step. Areas of the graphene seemed to have been lost in the lift off process. The HfO_2 then reacted with these damaged regions and formed large

purple-colored areas in the conduction channel. The electrical data from the C-715 devices is shown in Figure B-20. Minimum conductivities for C-715 ranged from 1100 μS to 8600μS. Electron mobility ranged from 500 to 2300cm^{2}V^{-1}s^{-1}and hole mobility ranged from 1600 to 3200cm^{2}V^{-1}s^{-1}.

Devices in Graph_C C-781 performed similarly to devices in Graph_B C-712. Relative to Graph_B, the HfO_2 used in Graph_C was reduced in thickness (from 50nm to 40nm) and deposited at a lower substrate temperature (at 100°C rather than 150°C) in order to alleviate stresses in the HfO_2 film. As a result, the Graph_C samples showed almost no visible dielectric cracking and therefore had no aluminum gate shorts. For some reason, possibly again due source/drain lift-off, many of the devices had large areas of graphene "missing" from their conduction channels, and were not included in device analysis. Only devices with mostly uniform thicknesses were analyzed. Sample devices are shown in Figure B-21. The electrical data from C-781 devices is shown in Figure B-22. Minimum conductivities for these devices ranged from 700 μS to 2700 μS. Electron mobility ranged from 700 to 2300cm^{2}V^{-1}s^{-1}. Hole mobility ranged from 1300 to 2400cm^{2}V^{-1}s^{-1}.

Graph_D, the only experiment in which the graphene sample received ALD HfO_2 , had no devices exhibit field effect behavior. All tested devices showed shorting between the graphene and Pt gate. It is so far hypothesized that the 10nm film was either too thin to fully cover the SiC surface roughness, or the film had pinholes and the Pt gate material shorted directly to the graphene and source/drain. Since Pt has a much higher melting temperature than Al, attempts to vaporize the metal shorts were unsuccessful.

The minimum source-drain conductivity for all C-face devices in Graph_B-C scaled linearly with minimum cross-sectional graphene thickness (brightness), as shown in Figure B-23.[1] Graph_A devices are not included in this analysis because graphene thicknesses were not measured for Graph_A. The large variation in observed minimum conductivities – the variation in C-781 a factor of 4, in C-715 a factor of 8, and in C-712 a factor of 17.5 – is then explained by the large variation in graphene thickness within each SiC sample. The relationship between minimum conductivity and minimum cross-sectional thickness was consistent across different graphene/SiC samples in Graph_B and Graph_C, despite changes

[1] The minimum cross-sectional graphene thickness was found by optically identifying the dimmest cross-sectional area for each device, since the thickness of a graphene film when on SiC scales linearly with film brightness as seen from an optical microscope. The relationship between the graphene optical brightness and physical thickness is shown in Figure B-24.

in the gate dielectric, suggesting that all graphene sheets, not just the ones contacting the HfO_2 , contribute to current conduction. Thus, the low on/off current ratios are not surprising, since without a band gap, the graphene layers are always conducting from source to drain. The linear relationship between minimum conductivity and minimum cross-sectional thickness implies that each graphene layer conducts a comparable level of current (given by the slope of the best fit line).

The evaporated HfO_2 used in Graph_A-C consistently experienced dielectric charging. Hysteresis was observed in all measurements. Repeated measurements on the same device both shifted the minimum conduction voltage as well as changed the charge carrier mobility, although most of these changes occurred between the first and second measurements. After the second measurement, the changes were not dramatic. Devices tested with voltages greater than +3V or lower than -3V experienced severe dielectric charging that would dissipate only after several minutes.

Charge carrier mobilities varied greatly between devices in the same graphene/SiC sample as well as between devices from different graphene samples. The lowest average electron and hole mobilities were from Graph_A, where the dielectric had densified and cracked profusely. No device in Graph_A exhibited electron mobilities higher than $600 cm^2V^{-1}s^{-1}$, and the average hole mobility was below $800 cm^2V^{-1}s^{-1}$. The second lowest average electron and hole mobilities were from C-715, where the graphene had been damaged and formed purple areas with the HfO_2 in the conduction channel. These mobilities were comparable to those from C-781, in which the dielectric did not crack or behave abnormally and in which the conduction channel had mostly uniform graphene. Devices with the highest electron and hole mobilities were from C-712 even though C-712 experienced extensive cracking in the HfO_2 and gate shorts that had to be vaporized. It is likely that the extreme levels of current and heat had annealed both the graphene and the gate dielectric, correcting defects and filling in charge traps, resulting in devices with much higher charge carrier mobilities. By comparing devices between graphene/SiC samples, it is evident that the gate dielectric must have a non-zero effect on device mobility. Even though all graphene layers conduct, inversion charge occurs only near the graphene-dielectric interface – only the layers closest to the HfO_2 gate dielectric will undergo gate modulation. Therefore, optimizing the effects from the gate dielectric is still necessary.

It is also meaningful to look at the ratio between electron and hole mobilities in the dif-

ferent devices. Since our devices contain graphene conduction channels and Pt source/drain contacts, they should theoretically exhibit symmetric mobilities for electron and holes. However, the observed mobilities have not been symmetric. Almost all devices exhibit a higher hole mobility than electron mobility, which is most likely due to the electron trapping nature of HfO_2 [37]. Graphene samples with damaged HfO_2 showed the lowest electron-to-hole mobility ratios. Devices from C-711 yielded an average electron mobility that was roughly only half the average hole mobility. Devices from C-715 also showed severe electron mobility degradation, with the average electron mobility again only half the average hole mobility. Devices from C-781, where the HfO_2 looked uniform and undamaged, showed an average electron mobility that was roughly 70% the average hole mobility, consistent with previous findings [37]. Only devices from C-712, where the graphene and HfO_2 underwent significant current anneals, showed electron mobility higher than hole mobility (by roughly 15%).

Additionally, devices on the same graphene/SiC sample exhibited markedly different mobilities. C-711 had electron and hole mobilities each vary by a factor of roughly 3 between its devices. C-781 devices had hole mobilities vary by a factor of 2 and electron mobilities vary by a factor of 3.5. C-715 devices had hole mobilities vary by a factor of 2.5 and electron mobilities vary by a factor of 4. C-712, which had the highest electron and hole mobilities, also had the largest variation, with hole mobilities varying by over a factor of 4 and electron mobilities varying by over a factor of 8. Analysis of Graph_B devices did not find carrier mobility to correlate strongly with minimal source/drain conductivity, minimal cross-sectional thickness, average graphene thickness, size of damaged graphene/ HfO_2 (both from vaporizing the Al shorts for sample C-712 and the purple HfO_2 regions for C-715). Even though the HfO_2 gate dielectric does affect carrier mobility, the effect should be more or less constant for all devices on the same graphene sample. Thus, the large variations observed on a single sample should best be explained by local variations in the graphene thickness and crystallinity.

4.2 Silicon Face Device Performance

The only Si-face sample used thus far was sample S-767, which was part of Graph_C. As shown in Figure B-25, the graphene film on S-767 (and on Si-face graphene samples in general) was much thinner and more uniform than the graphene on C-face samples.

Electrical data for S-767 devices are shown in Figure B-26. The minimum conductivities ranged from 130uS to 250uS. Electron mobilities ranged from 600 to 1050$cm^2V^{-1}s^{-1}$. Hole mobilities ranged from 900 to 1140$cm^2V^{-1}s^{-1}$.

Minimum conduction for these thinner Si-face devices are much lower than the minimum conduction levels observed for C-face devices, consistent with the observation from C-face devices that each graphene layer conducts comparable levels of current and that thinner graphene films conduct less current than thicker films. Minimum conductivity levels varied by only a factor of 2, suggesting that the graphene on the Si-face is much more uniform than the C-face.

Devices on sample S-767 experienced dielectric charging as in all the C-face devices. Shifts in the minimum conduction voltage and changes to charge carrier mobilities between the first and second I_d–V_g measurements are shown in Figure B-27. The I_d–V_g curves stabilized after the second measurement. Conductivity at voltages greater than roughly 0.5V reached a pronounced saturation, as was shown in Figure B-26. This saturation may be due to charging of the HfO_2 gate dielectric as well.

Mobility values for the devices were calculated based on the stabilized I_d–V_g curves. Mobility in the Si-face devices were much lower than C-781 even though both samples received the same dielectric. This fact suggests that either the crystallinity of the Si-face graphene is different from C-face graphene or that graphene thickness and thickness uniformity plays a role in determining carrier mobility.

Chapter 5

Fabricating Graphene Transistors Using CVD-Grown Epitaxial Graphene

5.1 Synthesizing Epitaxial Graphene on Nickel via CVD Growth

The graphene films we used were grown at the Massachusetts Institute of Technology. Full details of the graphene growth process can be found in [50]. A brief summary of the process is given below.

Epitaxial growth of a crystalline material usually requires a lattice-matched crystal template. The nickel (111) face is a lattice-matched template to graphene. 500nm of nickel is first thermally evaporated onto a 100nm thick thermal oxide wafer. The evaporated Ni film is polycrystalline. The layer of oxide prevents the Ni from forming silicide during the epitaxial growth process. A small piece (roughly 1cm^2) of the Ni-oxide-silicon wafer is placed inside a chemical vapor deposition (CVD) chamber. The Ni is first annealed at 900°C in a mixture of Ar and H_2 gas in order to increase grain sizes of the film. An AFM image of the Ni grain structure after high temperature annealing is shown in Figure B-28. The graphene grows on these grains, thus itself becoming polycrystalline, and increasing the grain sizes of the Ni template will also increase the grain sizes of the graphene film. Note that for a given Ni grain, the crystal face on which the graphene grows will not necessarily be the (111) face that is lattice-matched to graphene.

The epitaxial growth takes place at 900°C - 1000°C in atmospheric pressure. Methane is used as the carbon precursor. H_2 makes up the remaining gas. The thickness of the graphitic film depends on the partial pressure of methane. The continuity of the film depends on both the partial pressure of methane and the growth time. At the optimal pressure and growth time, a thin layer of graphitic film covers the entire Ni wafer template.

After the graphitic film is grown, it is ready to be transferred from the Ni onto an arbitrary substrate. The graphene is first top-coated with a layer of PMMA. The Ni film is then dissolved in a mild aqueous solution of HCl. This releases the PMMA with the graphitic film essentially glued to its bottom. The combination looks like a thin clear plastic film, similar to a contact lens. The PMMA is then placed onto the new substrate with the graphene in direct contact with the substrate. The top layer of PMMA is then dissolved in acetone. This completes the transfer of the graphitic film from the Ni template.

Upon analysis, the graphitic film is found to contain scattered regions of different thicknesses. Electron diffraction patterns confirm a hexagonal lattice structure [50]. An optical image of an epitaxial graphene sample is shown in Figure B-29. The graphene in the light-blue colored regions are thin, in the dark blue colored regions are thick, and in the green colored regions are even thicker. An AFM image of an epitaxial graphene sample is shown in Figure B-30. Ripples and folds visible in the graphene sheets are likely caused by the extra surface area of the polycrystalline Ni. AFM step height measurements reveal that the film is between 0.5nm and 12nm thick, similar to the C-face graphene/SiC films. It is apparent from the optical images that the graphene films exhibit a prominent grain structure, which is most likely due to the grain structure of the Ni template. Methods to increase grain size of the film are still being investigated.

5.2 Fabrication Process for Transistors

The process for fabricating transistors using epitaxial graphene is essentially the same as the process used for graphene/SiC. All transistor devices were top-gated. The same masks (and hence device topologies) were used. Most of the processing steps – patterning of the graphene conduction channel, source/drain electrode deposition and patterning, gate dielectric deposition, and gate electrode deposition and patterning – were exactly the same for the two different types of graphene. Compared to graphene/SiC, epitaxial graphene

undergoes two additional processing steps: (1) a pre-processing anneal and (2) gate dielectric patterning (which had previously only been attempted in Graph_A).

Transistors were fabricated using epitaxial graphene in Graph_F. After growth, the graphene films were transferred onto 6" Si wafers. The wafers were bare Si except for an area of size 3.5mm x 4.5mm (the same size as the graphene/SiC samples), which consists of 500nm thermal oxide. The epitaxial graphene samples were transferred onto the oxide regions. The oxide insulates the graphene from the semiconducting Si wafer underneath, in effect taking the role of the SiC in the graphene/SiC samples.

The graphene film then underwent a 20 minute 400°C anneal in Ar/H_2 gas and a 10 second 1000°C RTA in N_2 gas prior to etching the graphene active regions. The purpose of the 400°C anneal is to remove remnants of the PMMA that may be left on the graphene surface. The purpose of the RTA is to promote adhesion between the graphene film and the thermal oxide. If the RTA step is omitted, the graphene will not adhere properly to the carrier wafer and will strip away during lithography steps.

The graphene then underwent all the processing steps used for the graphene/SiC experiments. The graphene conduction channels were defined using an O_2 plasma etch. The source/drain electrodes consisted of 2nm evaporated titanium and 20nm evaporated platinum and were defined using a liftoff process. The gate dielectric used was 40nm HfO_2 evaporated with the substrate temperature at 150°C. The gate electrode was 20nm Pt. For Graph_F, pad openings were patterned into the HfO_2 . The pad process involved pad lithography and a four minute Silox etch. Since the HfO_2 was deposited at 150°C, the film did not react adversely to this processing step as it did in Graph_A. Images taken throughout the fabrication process are shown in Figure B-31.

THIS PAGE INTENTIONALLY LEFT BLANK

Chapter 6

Performance of CVD-Grown Epitaxial Graphene Transistors with HfO_2 Gate Dielectric

Finished graphene transistors were tested for field effect behavior. V_{d} was held at 0.1V, V_{s} was held at 0V, V_{g} was swept from -3V to +3V. The tests were intended to demonstrate current modulation by the gate. Minimum conductivities and charge carrier mobilities were calculated. The devices tested all have conduction channels that were sized 10μm in length and 5μm in width – they are all supposed to be "identical" devices.

As was the case for the graphene/SiC devices, the ambipolar Pt source/drain contacts can inject both electrons and holes into the graphene conduction channel. The observed graphene FET $I_{\mathrm{d}} - V_{\mathrm{g}}$ curves exhibit the usual ambipolar, V-shape characteristic. Negative gate voltages produced conduction dominated by holes, positive voltages produced conduction dominated by electrons. Conductivity and charge carrier mobility were calculated as they were for the graphene/SiC devices in Chapter 4. Again, the terms "electron mobility" and "hole mobility" are used here only loosely.

The HfO_2 in Graph_F experienced the same cracking problems as in Graph_A-C. As shown in Figure B-32, the film was observed to crack on thick regions of graphene but not on thin regions. Recall from Figure B-29 that the graphene film is multi-layer, polycrystalline and randomly oriented. Consequently, most of the devices fabricated were at least partially composed of thick graphene regions. Most of these devices experienced severe cracking of

the HfO_2 . The gate metal penetrated the dielectric through these cracks, shorting directly to the graphene. These devices did not exhibit field effect behavior.

A handful of devices did not show visible cracking of the HfO_2 . Interestingly, only one of these devices had mostly uniform thin graphene (approximately 1.5nm in thickness). An optical image of this device is shown in Figure B-32(B). An AFM image of this device is shown in Figure B-33. The other devices had thick graphene regions and experienced only slight gate shorting (most likely through invisible, hair-line cracks in the gate dielectric). The gate shorts were remedied by current annealing the devices. Attempts to current anneal devices with severely cracked HfO_2 were unsuccessful. Electrical data for the working devices are shown in Figure B-34. The minimum conductivity varied by a factor of 5, ranging from 100μS to 500μS. Electron mobilities ranged from 500 to 1400 $cm^2V^{-1}s^{-1}$. Hole mobilities ranged from 1550 to 2200$cm^2V^{-1}s^{-1}$. The hole mobility values are consistent with typical C-face devices. The electron mobility values are consistent with typical Si-face devices.

The average electron mobility is only roughly 50% of the hole mobility, which was unexpectedly low. Only sample C-711, on which the HfO_2 had densified, demonstrated an equally low average electron-to-hole mobility ratio. One possible explanation for the low electron mobilities observed is that the graphene–HfO_2 interface contains residual PMMA. PMMA has been shown to produce electron mobilities much lower than hole mobilities in organic FETs even when the semiconductor is an ambipolar material [55].

Dielectric charging was once again a problem. Hysteresis was observed in all working devices. Attempts to test the devices at voltages greater than +3V or lower than -3V caused severe dielectric charging, nearly resulting in the loss of gate modulation behavior.

Chapter 7

Discussion: Comparing the Performance of Evaporated HfO_2 on Graphene/SiC and on CVD-Grown Epitaxial Graphene

Graphene FET devices were fabricated on six separate graphene samples: five graphene/SiC samples C-711, C-712, C-715, C-781, S-767, and one CVD sample. Although the performance of the devices on any given graphene sample showed significant variations, general trends are nonetheless evident when comparing device performances across all graphene samples.

First, the yield of functioning FET graphene devices have been low and variable due to cracking of the HfO_2 . Evaporated HfO_2 tends to crack on thick regions of graphene. These thick regions are almost unavoidable since the graphene used thus far have been both multi-layer and polycrystalline, with thin and thick regions distributed randomly across the graphene sample. Cracks in the gate dielectric allow the gate metal to short directly to the conduction channel, creating resistive shorts instead of insulating gate stacks, rendering the FET devices unusable.

Second, the HfO_2 persistently exhibited dielectric charging. Repeated measurements altered charge carrier mobilities and shifted minimum conduction voltages. High fields induced by large gate voltages caused severe charging until gate modulation was almost

lost. This problem was observed for nearly all graphene devices.

Third, most graphene devices fabricated thus far have shown an asymmetry in electron and hole mobilities, even though the Dirac cone in the graphene band structure suggests that electron and hole mobilities should be roughly equal. Devices from five out of the six graphene samples (C-711, C-713, C-781, S-767, and CVD graphene) have yielded average electron mobilities ranging from 50% to 85% of average hole mobilities. Only devices in C-712, which underwent extensive current annealing, produced an average electron mobility higher than the average hole mobility (by 15%). The fact that the electron mobility is lower in most samples is likely a characteristic of the HfO_2 , which is known to reduce electron mobilities more than hole mobilities in Si CMOS devices [37].

Fourth, electron mobility seems to degrade more severely than hole mobility when the HfO_2 –graphene interface is damaged. The average electron mobility of C-711 devices was only roughly 56% the average hole mobility. The average electron mobility for C-715 was only roughly 64% the average hole mobility. Recall that sample C-711 experienced HfO_2 densification and extreme levels of cracking and sample C-715 had purple areas in the graphene conduction channel after HfO_2 deposition.

Thus, it is clear that the gate dielectric must still be optimized in order to improve the performances of graphene FETs. A pinhole-free film deposited via ALD may reduce film stress, decrease cracking and eliminate dielectric charging. Also, an adhesion promoter may be used to increase adhesion between the graphene and the gate dielectric. One possibility is to use NO_2gas, which has been successful in promoting adhesion between ALD Al_2O_3 and carbon nanotubes [18]. Both ALD Al_2O_3 and ALD HfO_2 enhanced with NO_2may be worth pursuing.

Chapter 8

Conclusion

Transistor devices with graphene conduction channels were fabricated using both graphene/SiC and CVD-grown epitaxial graphene. Evaporated HfO_2 was the gate dielectric used for all functional graphene FETs. Two problems were persistent for all the graphene devices. First, the HfO_2 exhibited noticeable charging effects. Hysteresis was evident, as was severe dielectric charging at high fields (caused by voltages > +/- 3V). Second, the HfO_2 tended to crack on thick regions of graphene but not on thin regions (with "thin" and "thick" being relative within each graphene sample). Due to the nature of graphene synthesized using current methods, thin and thick regions were randomly distributed in the conduction channel. The cracks in the gate dielectric are wide enough and deep enough to allow the metal gate to penetrate the dielectric and short directly to the graphene underneath. Gate shorting has caused low device yields, with some samples yielding only 20% functional devices.

Electrical performance of the fabricated FETs show large variations due to the local graphene microstructure. Nonetheless, general trends exist when analyzing devices from all six graphene samples. Average electron mobilities have been lower than average hole mobilities across almost all graphene samples. This asymmetry in charge carrier mobility is likely due to the HfO_2 gate dielectric rather than the graphene. Current annealing may increase both electron and hole mobility and make the two mobilities more equal.

In order to fabricate reliable, high performance devices with consistent yield, both the graphene and the gate dielectric remains to be optimized. Large-area, uniform and thin graphene will be critical to eliminating performance variations between devices. At the

same time, choosing not only a gate dielectric material but also the best deposition process will be crucial to improving device performance. Thus, the potential of graphene based electronic devices remains to be determined.

Appendix A

Tables

Table A.1: Candidate oxides for Graphene FETs. Note that as the dielectric constant increases, the band gap decreases. All dielectric constant and band gap values taken from [63].

Oxides		
Material	Dielectric Constant (K)	Band Gap (eV)
SiO_2	3.9	8.9
Al_2O_3	9	8.7
Y_2O_3	15	5.6
HfO_2	25	5.7
ZrO_2	25	5.8
Ta_2O_5	26	4.5
La_2O_3	30	4.3
TiO_2	80	3.5

Table A.2: Candidate nitrides for Graphene FETs.

Nitrides		
Material	Dielectric Constant (K)	Band Gap (eV)
BCN	2.4 [16]	data unavailable
BN (amorphous)	3.5 [5]	5.8 [5]
Si_3N_4	7.8 [64]	5.1 [63]
AlN	8.5 [54]	data unavailable

Table A.3: Candidate organic and polymer dielectrics for Graphene FETs.

Organic and Polymeric Dielectrics		
Material	Dielectric Constant (K)	Band Gap (eV)
SAMs (self-assembled monolayers)	2.4-2.7 [49]	data unavailable
BCB (bis-benzocyclobutene)	2.65 [46]	data unavailable
Parylene-C	3 [59]	data unavailable
PMMA (polymethyl methacrylate)	3.5 [59, 47]	data unavailable
Polyimide	2.6-3.3 [14, 46, 59]	data unavailable

Appendix B

Figures

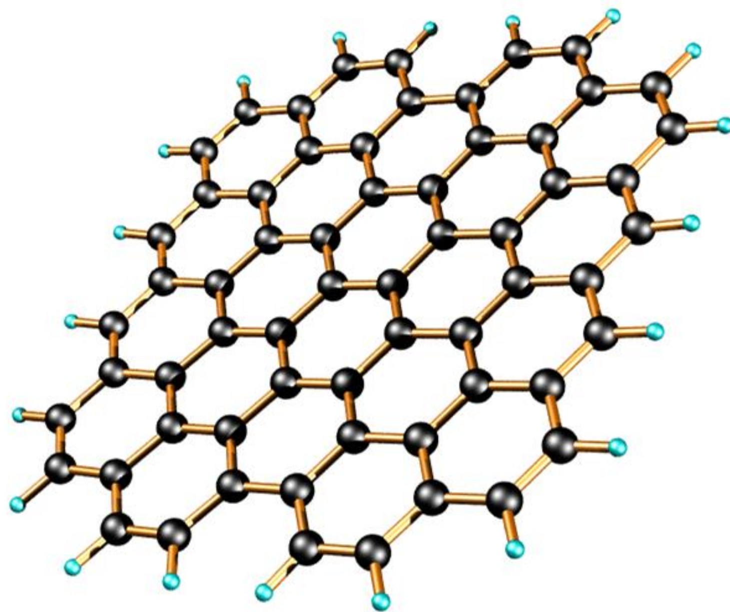


Figure B-1: An artist's rendition of the graphene honeycomb crystal structure. Image taken from [17]. ©Chris Ewels www.ewels.info

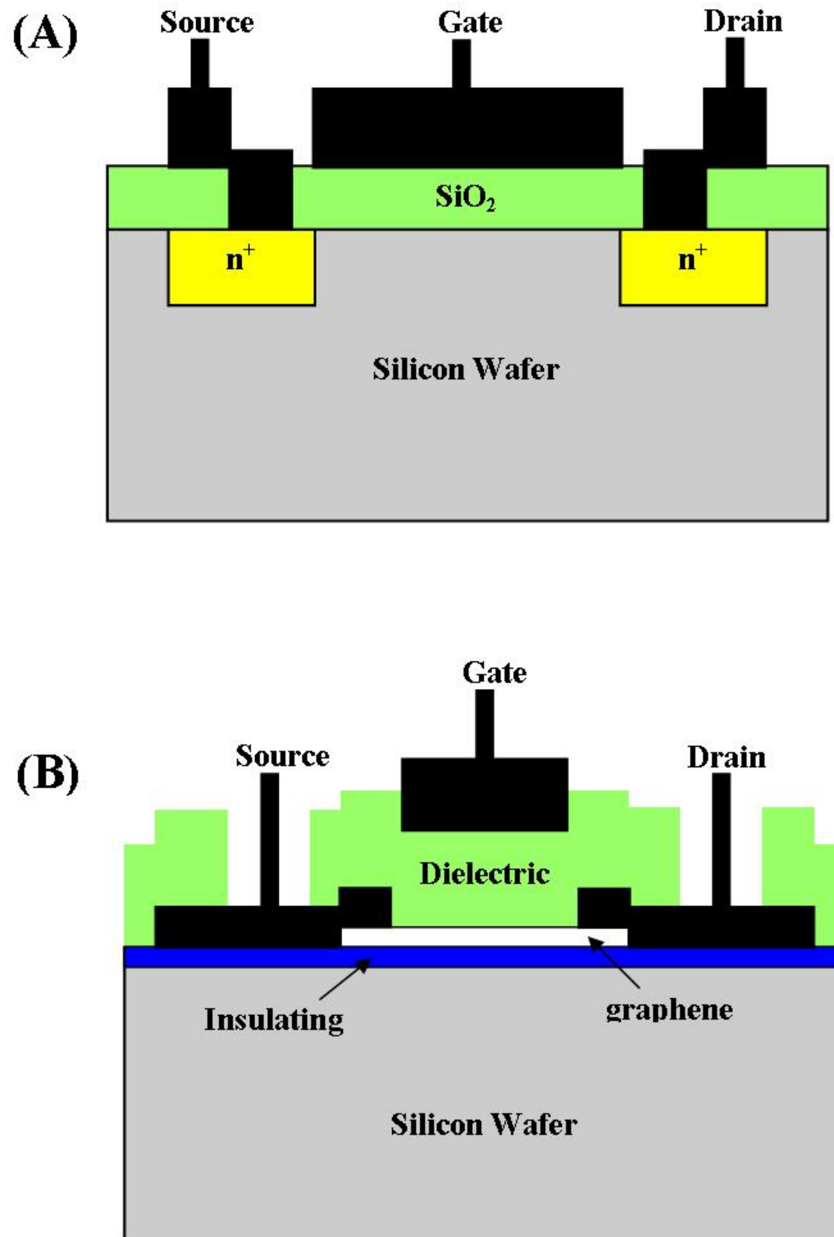


Figure B-2: Comparing topologies of a Si MOSFET and a top-gated graphene MISFET. (A) Textbook topology of a Si metal-oxide-semiconductor field effect transistor (MOSFET). The semiconductor is Si. The dielectric is SiO_2 . Note that the source/drain contacts are highly doped regions in the Si. The gate is usually heavily doped polysilicon instead of metal. (B) Topology used for a top-gated graphene metal-insulator-semiconductor field effect transistor (MISFET). The semiconductor is the graphene. The insulator is some sort of dielectric. The metal is for the top gate.

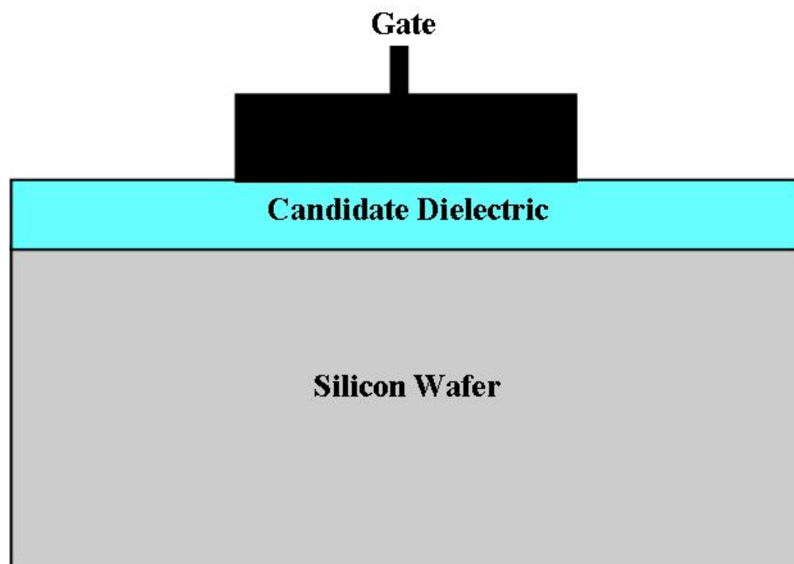
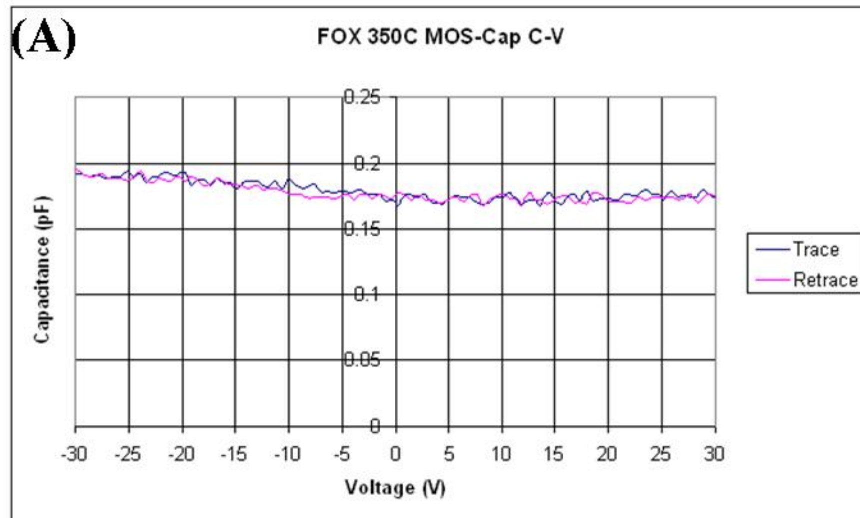


Figure B-3: Topology of a MIS capacitor used to test candidate dielectric devices.



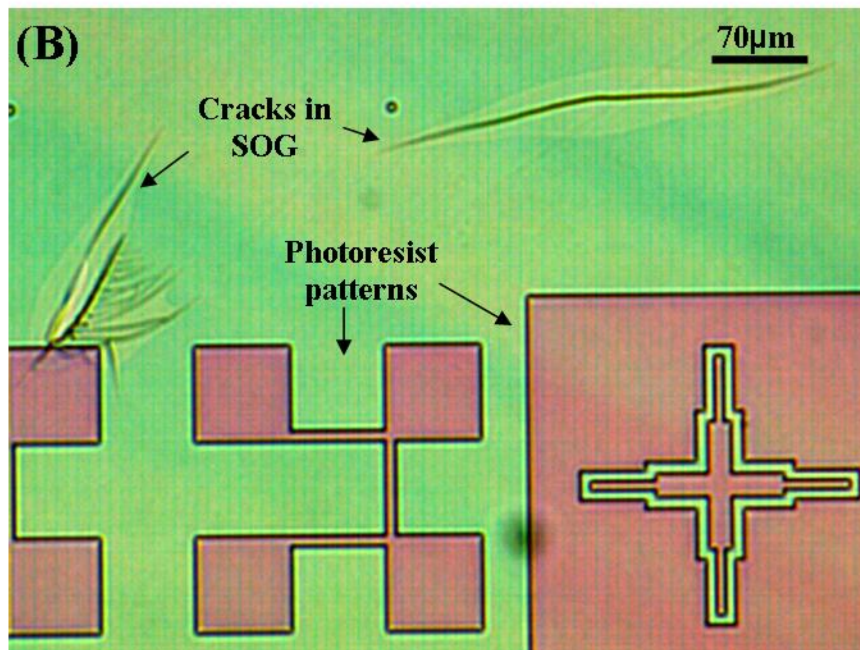


Figure B-4: Spin on glass (also called flowable oxide, or "FOX") was tested in a MIS capacitor structure. (A) C-V data for $\sim 1\mu$m thick spin on glass cured at 350°C for 15 minutes. The film was much too thick to allow gate modulation at the voltages tested. (B) Optical image showing cracks in the spin on glass after curing.

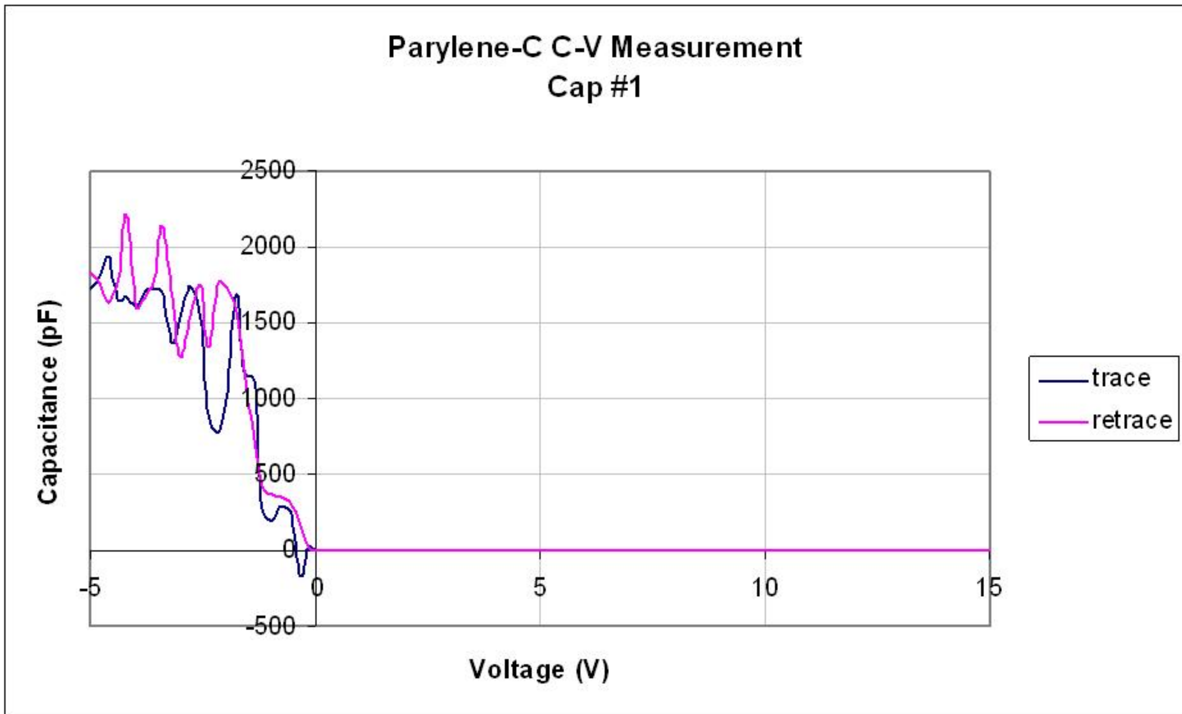
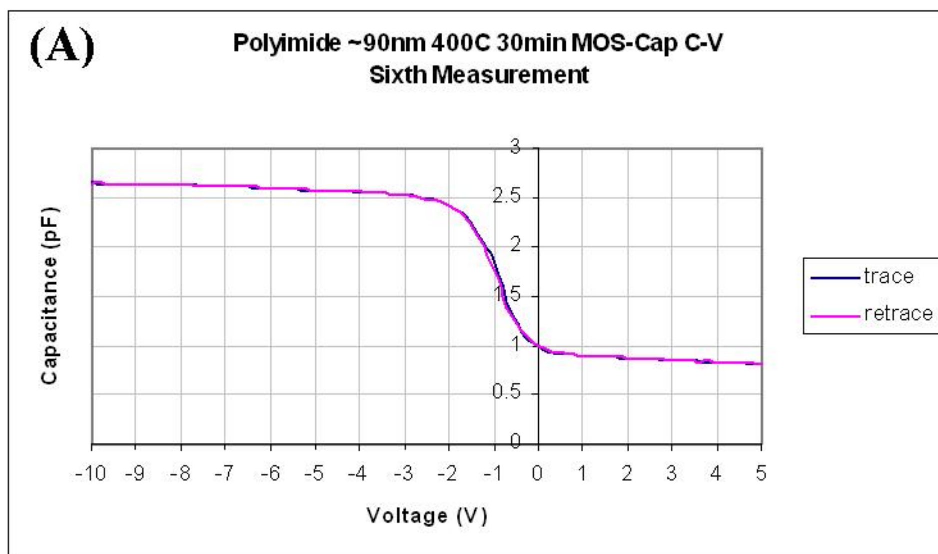


Figure B-5: C-V data for 100nm thick Parylene-C. The film was thin and soft, allowing probe tips to easily puncture the film during MIS capacitor testing.



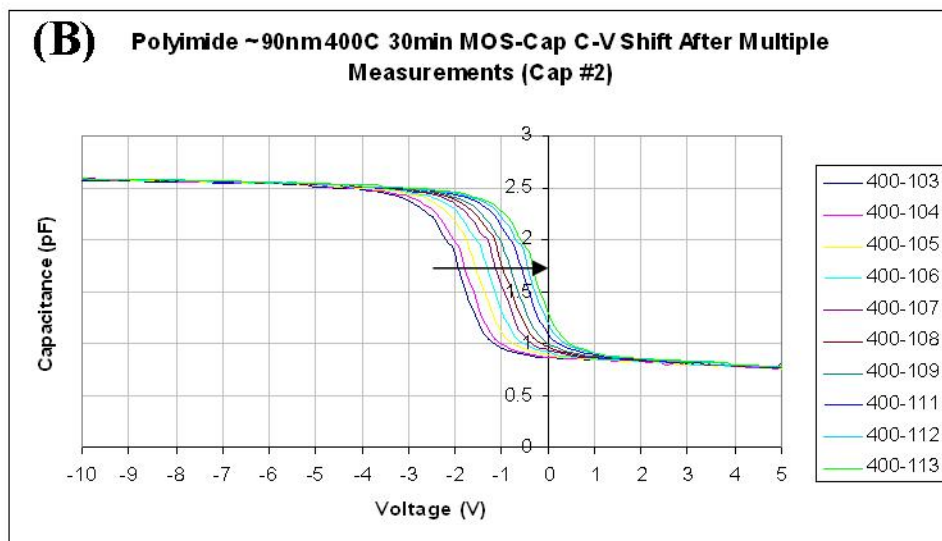


Figure B-6: C-V data for 90nm polyimide cured for 30 minutes at 400°C. (A) Repeated measurements on the same polyimide test capacitor showed little trace-retrace hysteresis. (B) The flat band capacitance increased continually with repeated measurements, indicating the polyimide accumulated charge during each voltage sweep.

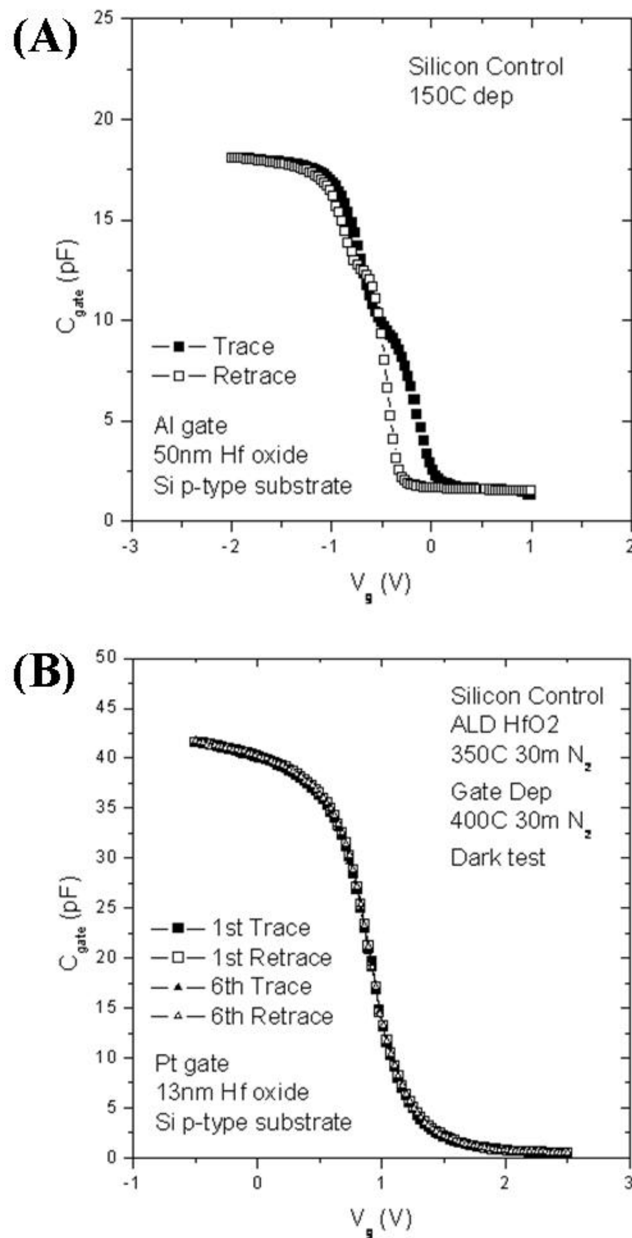


Figure B-7: C-V data for HfO_2 . (A) C-V data for 50nm evaporated HfO_2 deposited at a substrate temperature of 150°C. Hysteresis and a noticeable kink caused by charge trapping are evident. (B) C-V data for 13nm ALD HfO_2 . Very little hysteresis is visible. No significant changes to the dielectric were evident after repeated measurements.

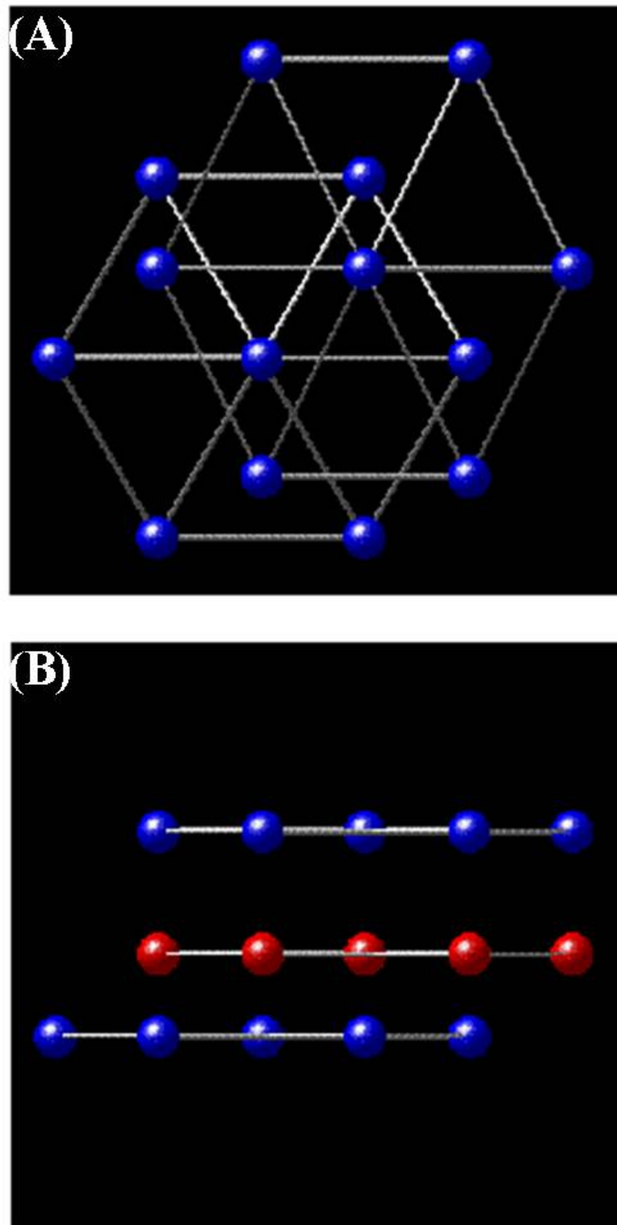


Figure B-8: Crystal structure of SiC lattice. Blue atoms represent Si, red atoms represent C (or vice versa). The lines connecting the atoms are meant to emphasize lattice structure and do not represent bonds. (A) Top view. Different layers of the same atom are arranged in a hexagonal honeycomb structure. (B) Side view. Si and C atoms form orderly stacked, hexagonally arranged layers. Image taken from [1].

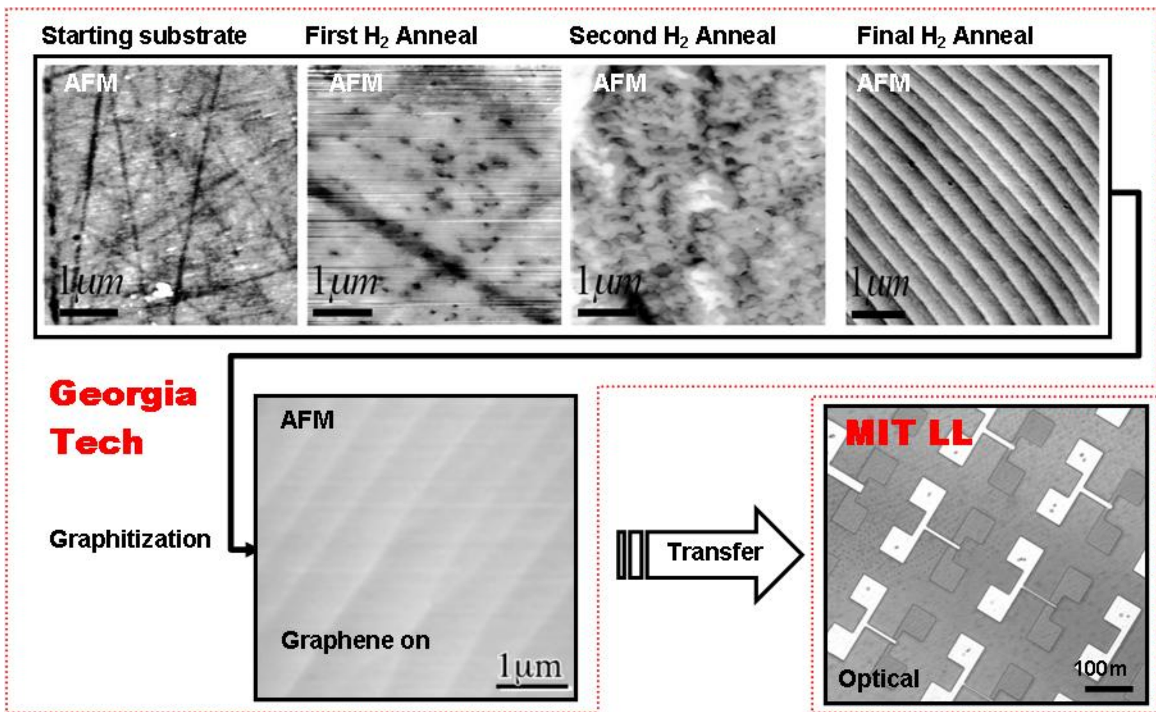


Figure B-9: AFM images showing the SiC substrate step by step through the graphitization process. After the SiC is graphitized, it is transferred to MIT Lincoln Laboratory for device fabrication. Image taken from [31].

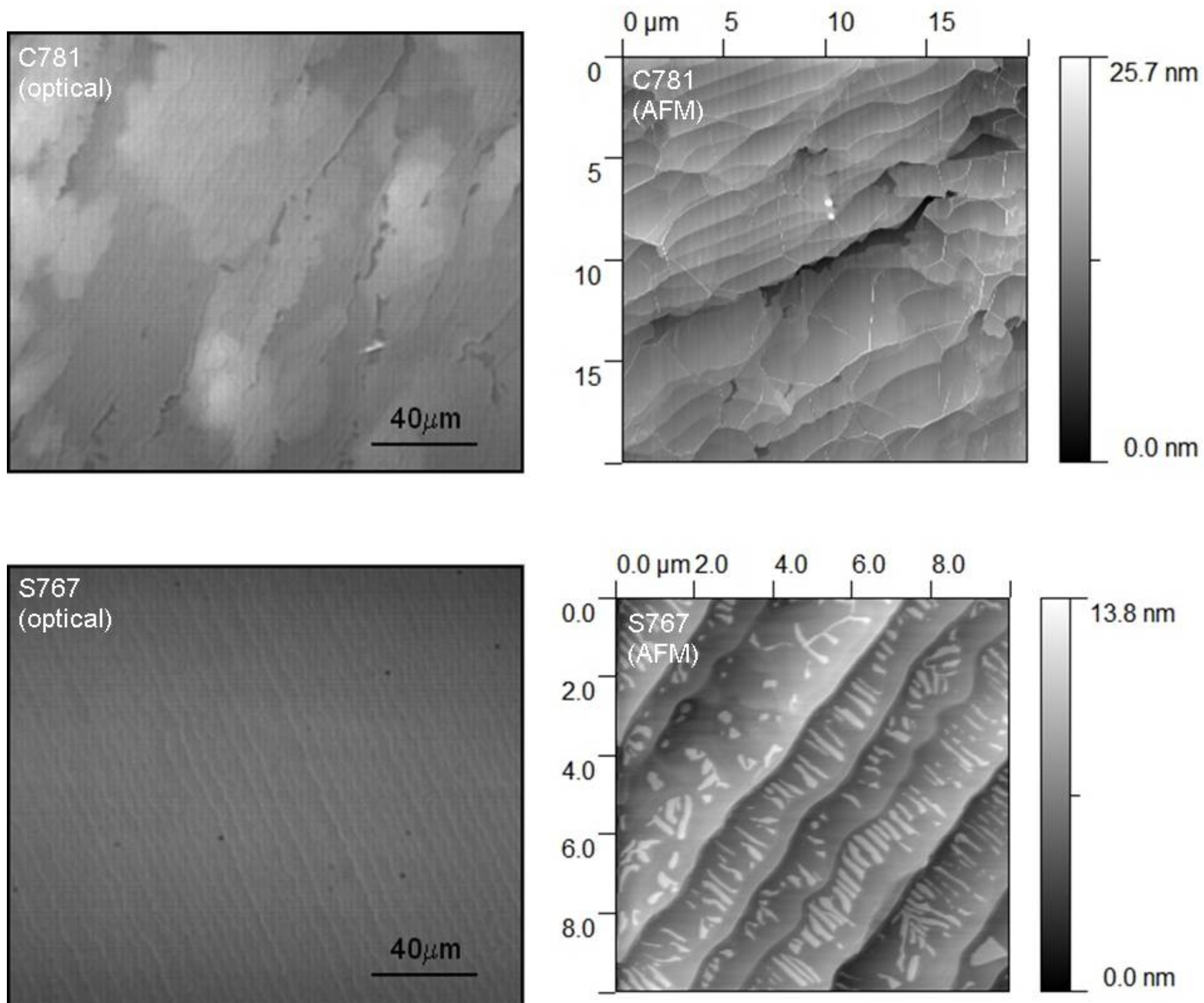


Figure B-10: Optical and AFM images of graphene grown on the C-face and Si-face of SiC. Graphene grown on the C-face appears non-uniform in brightness, whereas graphene grown on the Si-face appears much more uniform. Image taken from [31].

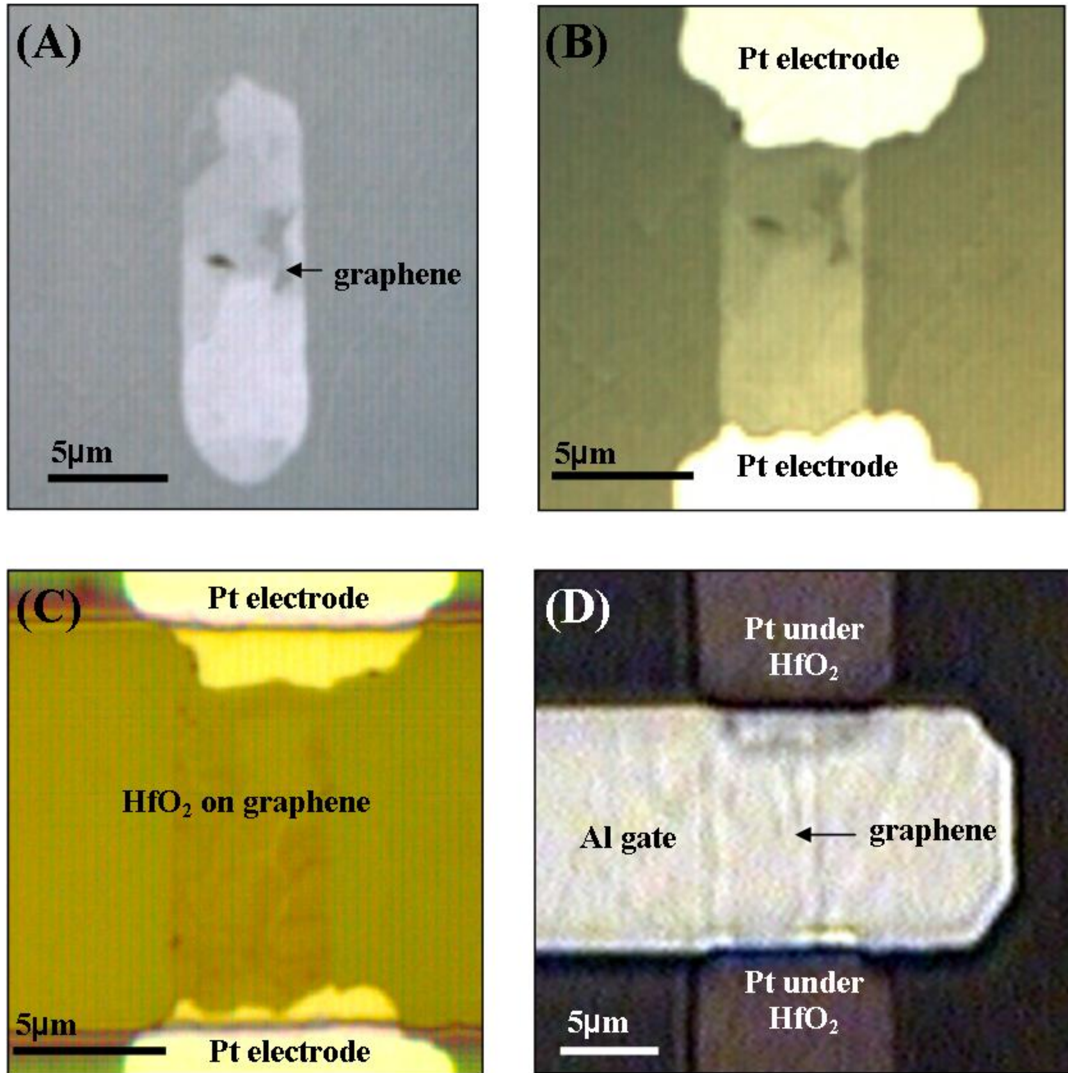


Figure B-11: Optical images illustrating the device fabrication process. (A) The first step is to pattern the graphene conduction channels. The channel shape is supposed to be rectangular – the rounded edges are lithographic artifacts. (B) The second step is to pattern Ti/Pt source/drain electrodes. Again, rounded edges are artifacts from lithography. (C) The third step is to deposit HfO_2 . Here, the wafer is coated with photoresist. Openings in the resist, exposing the HfO_2 , are for Al gate deposition. (D) A finished FET device.

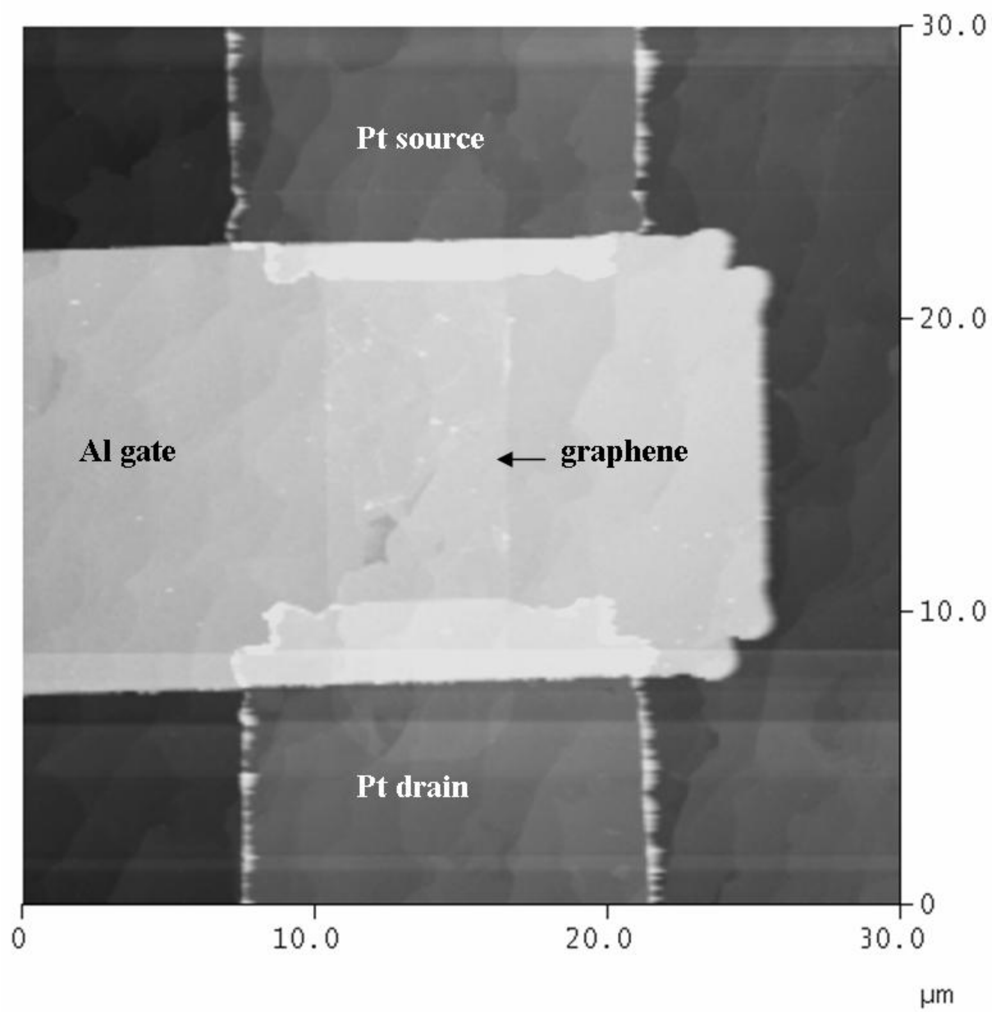


Figure B-12: AFM image a finished graphene FET. The graphene film in this device is roughly 7nm thick.

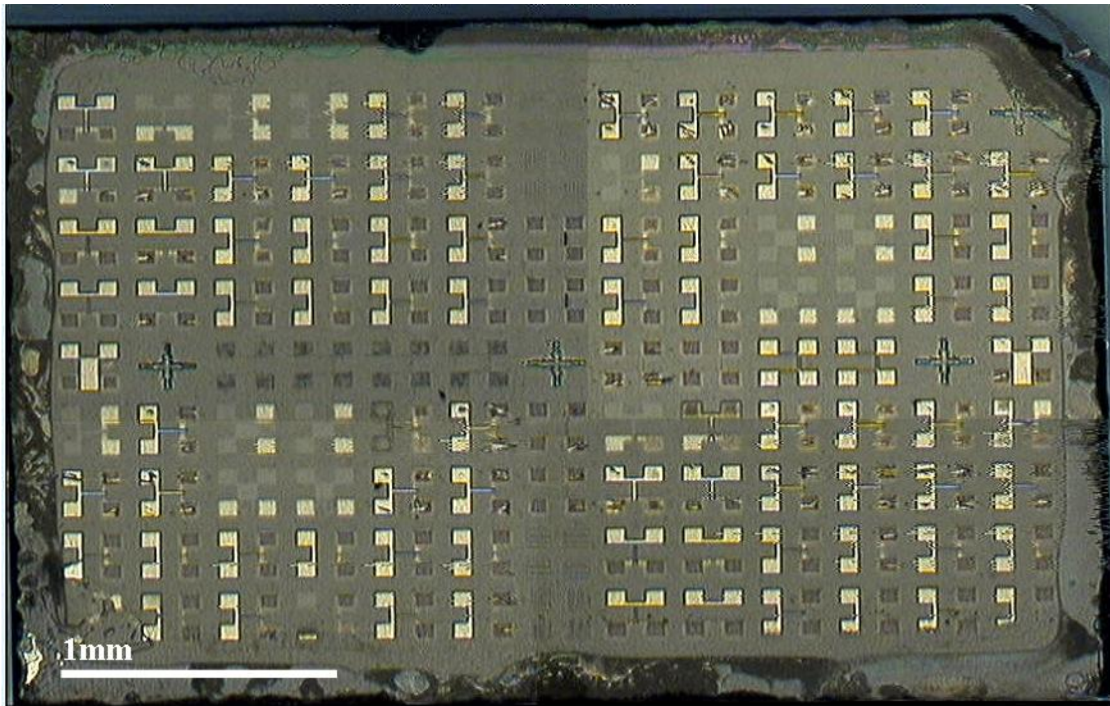
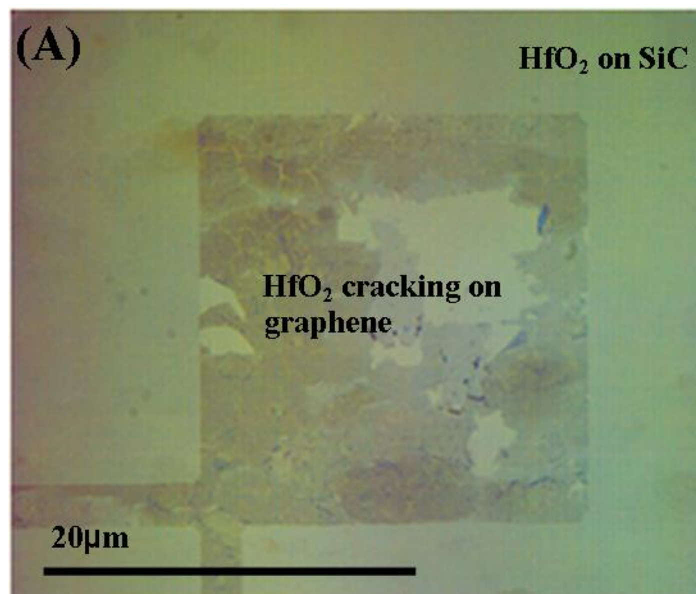


Figure B-13: Composite image of a graphene/SiC sample after device fabrication. Probe marks can be seen on the Al pads.



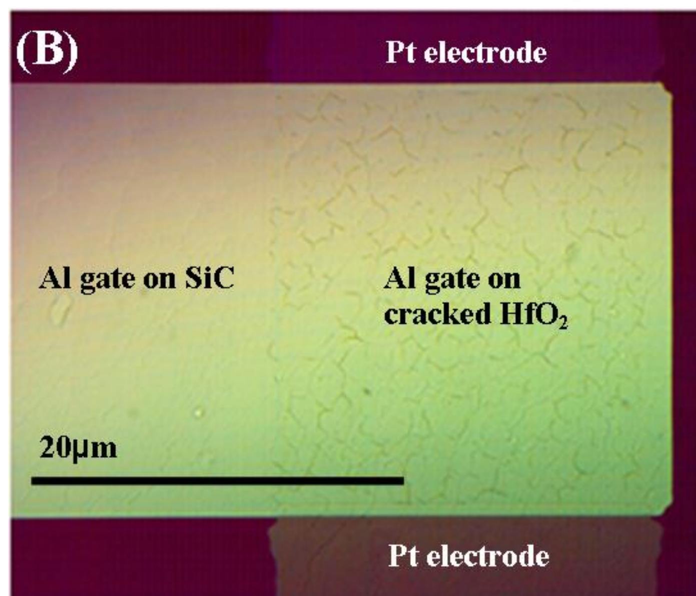


Figure B-14: Optical images of Graph_A sample C-711 after all processing steps have been finished. (A) The HfO_2 cracks were only observed on top of the graphene film and not on the SiC. (B) The Al gate metal cracked only on top of cracked HfO_2 .

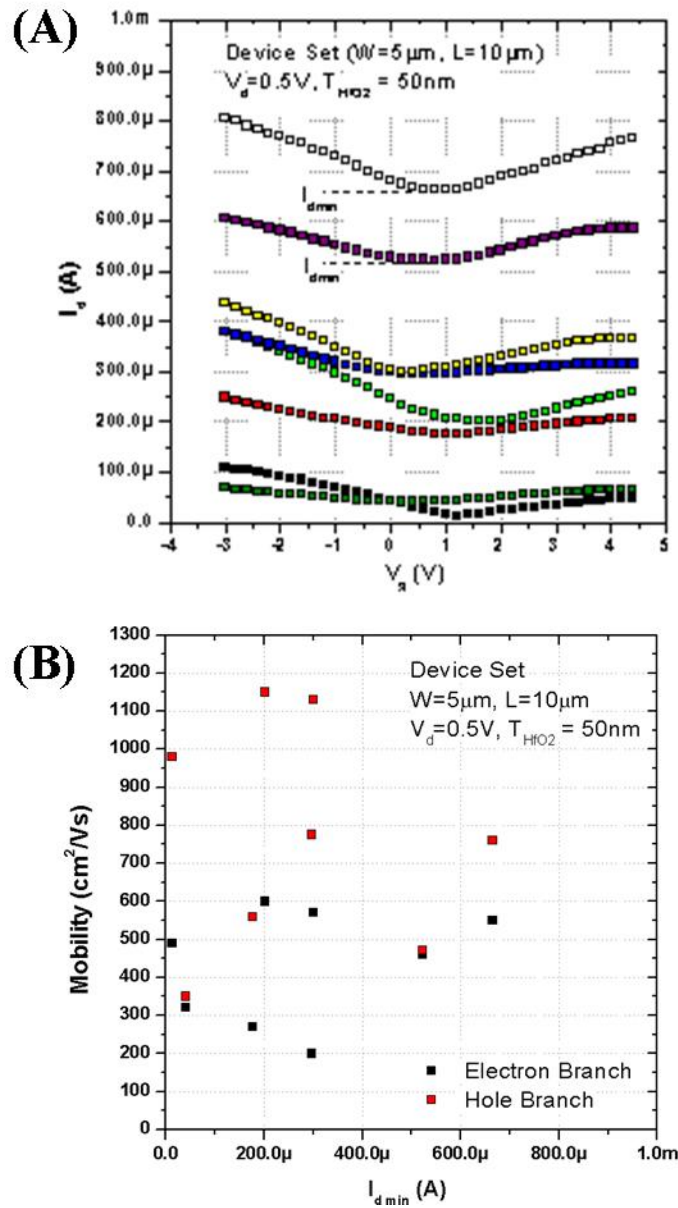


Figure B-15: Electrical data for Graph_A graphene/SiC sample C-711. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. Devices from this experiment had the lowest electron and hole mobilities.

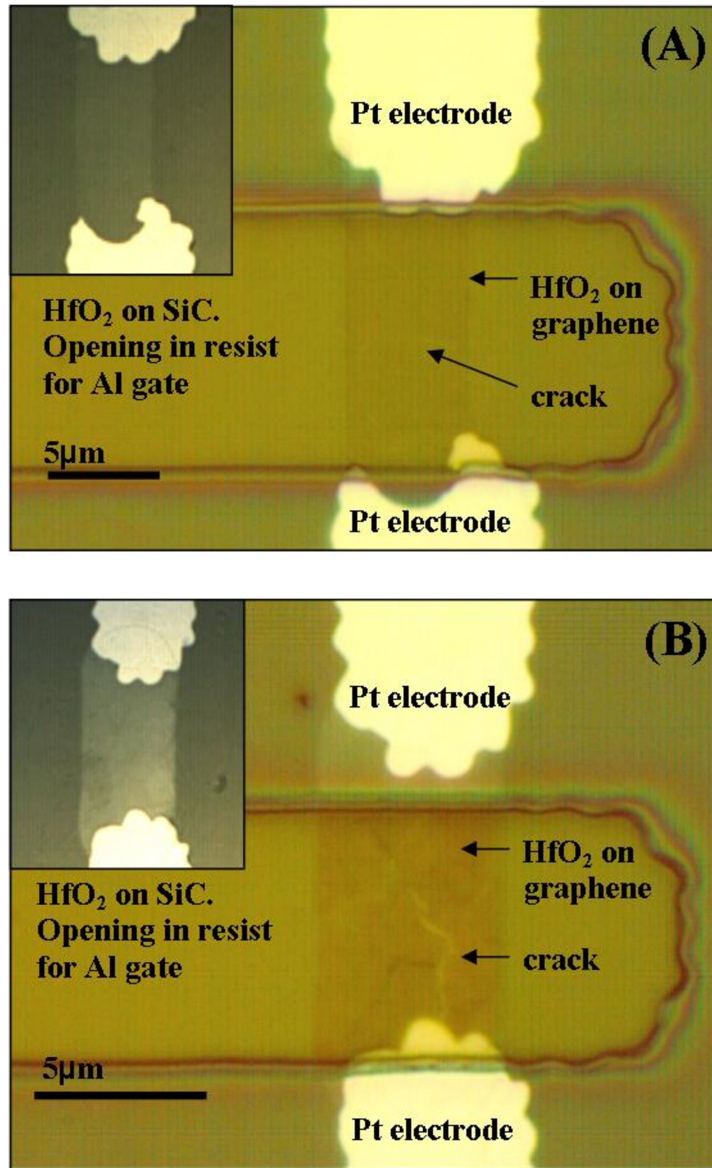


Figure B-16: Optical images of Graph_B sample C-712 before Al gate deposition and after HfO_2 deposition. Photoresist covers all areas of the wafer except an opening for the Al gate. The HfO_2 only cracks on top of the graphene and does not crack on either the SiC or on the Pt source/drain electrodes. (A) Faint cracks are visible in the HfO_2 over the graphene conduction channel. Inset: optical image of the same device prior to HfO_2 deposition showing thin regions of graphene. (B) Thick, noticeable cracks are visible over the graphene conduction channel. Inset: optical image of the same device prior to HfO_2 deposition showing thick regions of graphene.

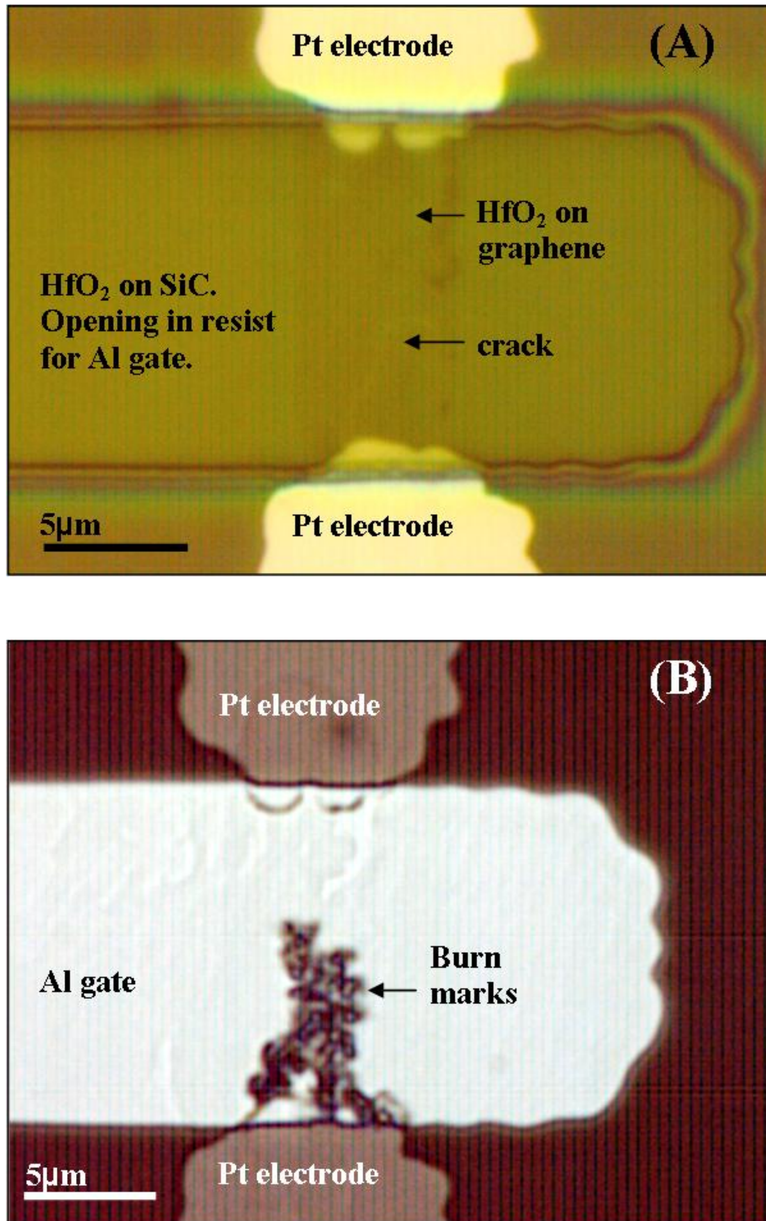


Figure B-17: Sample C-712 experienced shorting between the Al gate to the graphene conduction channel through cracks in the gate dielectric. The shorts were vaporized after current annealing the devices, which involved passing a large amount of current (roughly 10mA) from the gate to the source/drain. (A) Optical image of a device taken prior to Al gate deposition. Cracks are visible in the HfO_2 gate dielectric over the graphene conduction channel. (B) Optical image of the same device after current annealing showing black burn marks on the Al gate.

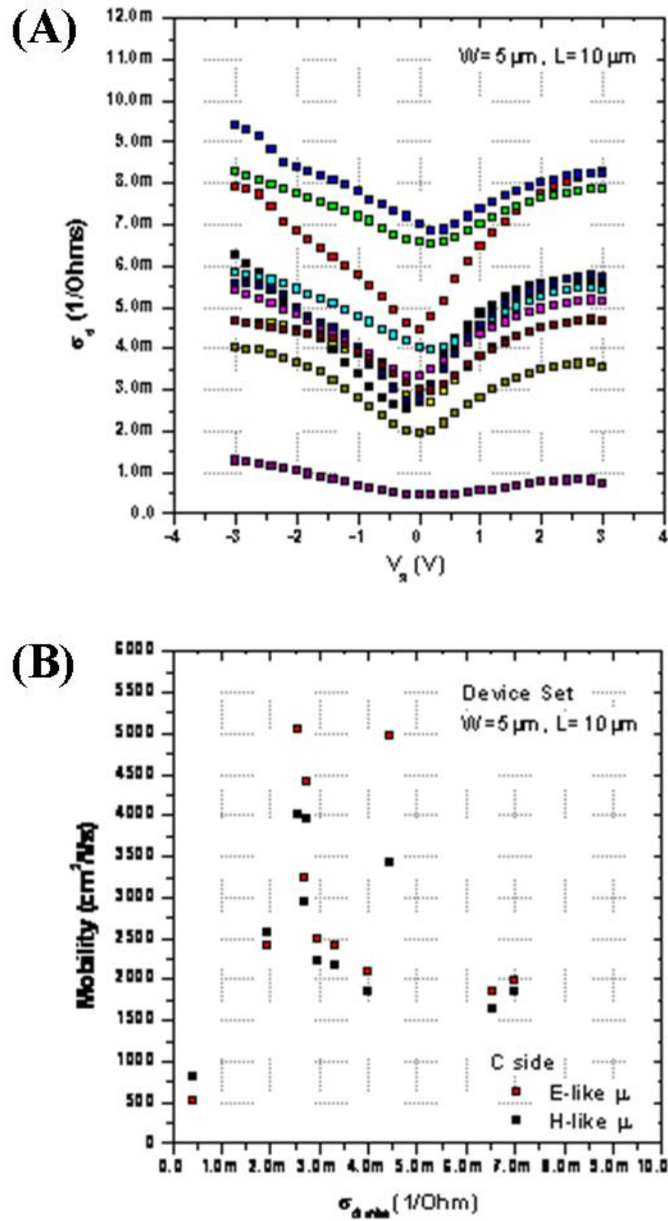


Figure B-18: Electrical data for Graph_B graphene/SiC sample C-712. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. Devices from this experiment had the highest electron and hole mobilities.

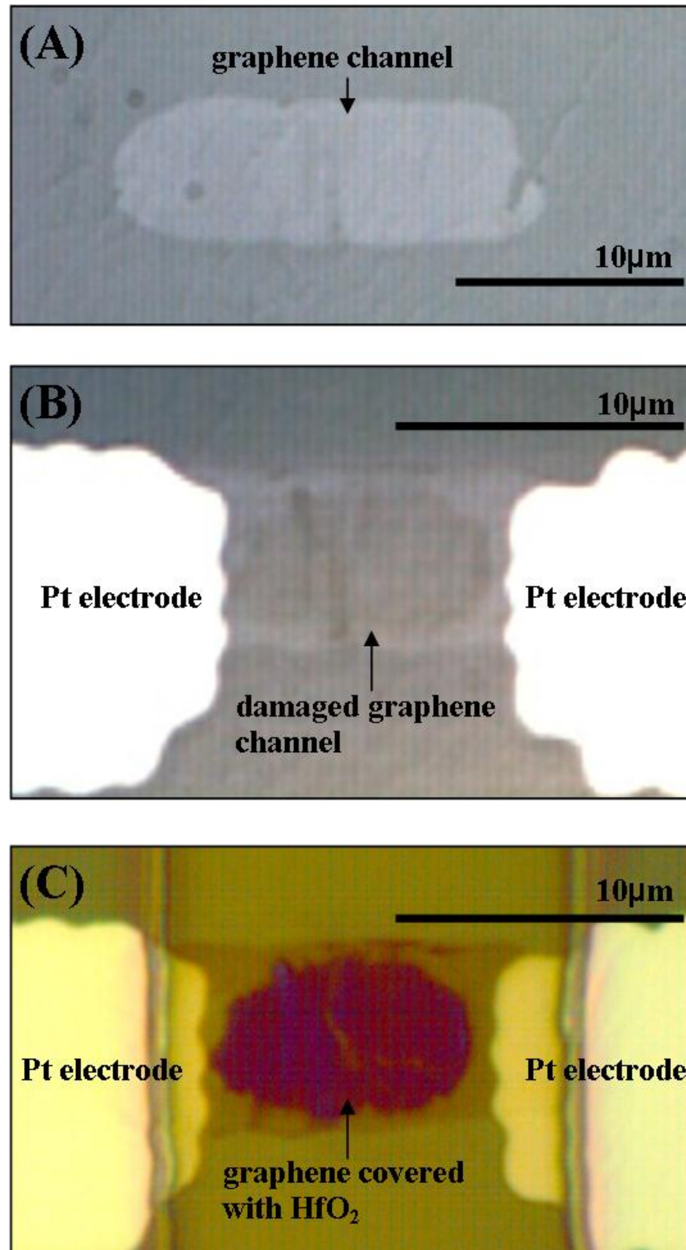


Figure B-19: Optical images of C-715. (A) Image of the graphene conduction channel after active area etch. (B) Image of the graphene conduction channel after Pt source/drain deposition and lift off. The graphene is visibly damaged. (C) Image of the graphene conduction channel before Al gate deposition and after HfO_2 deposition. There are visible purple-colored regions where the damaged graphene interfaced with the HfO_2 .

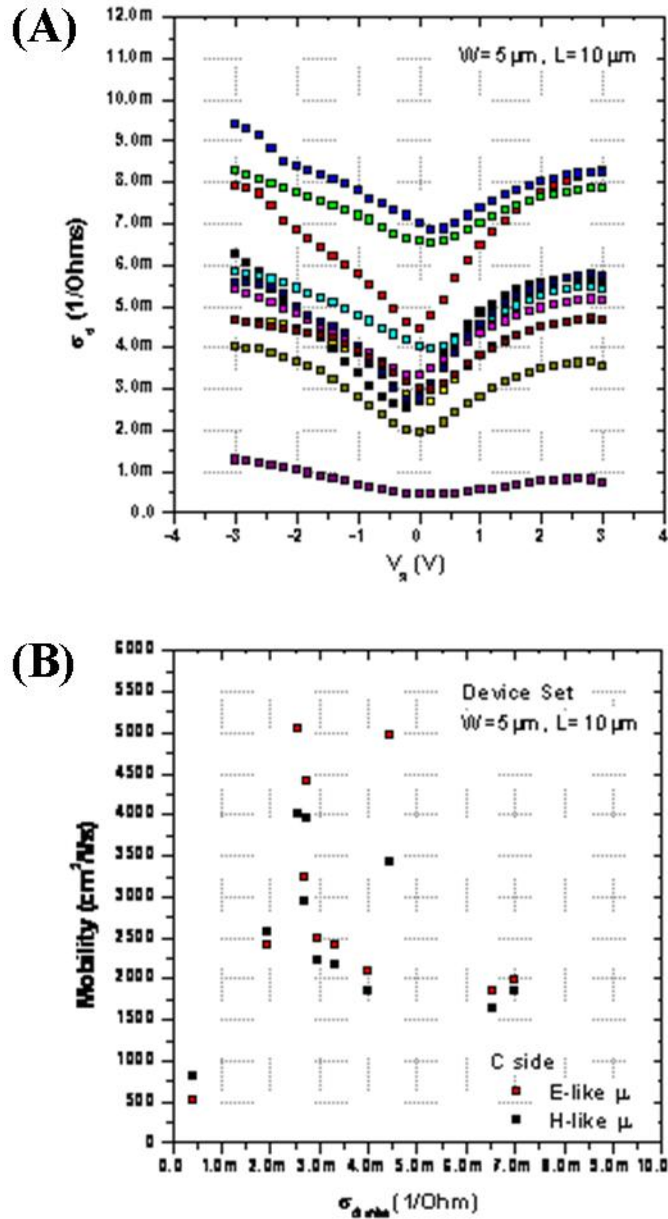
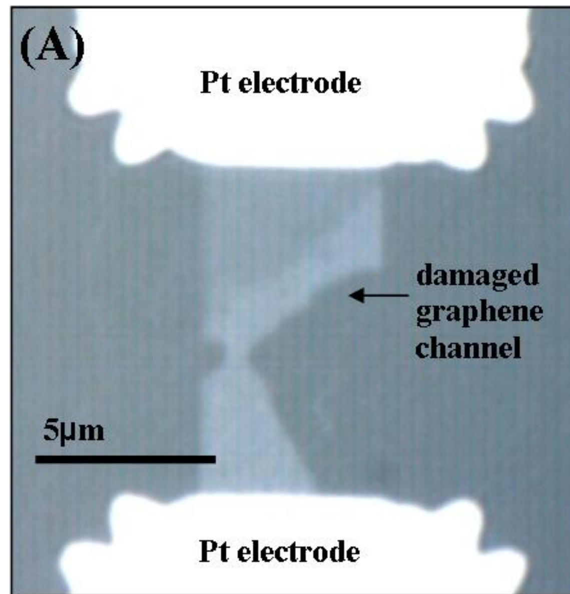


Figure B-20: Electrical data for Graph_B graphene/SiC sample C-715. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. On average, the electron mobility is lower than the hole mobility.



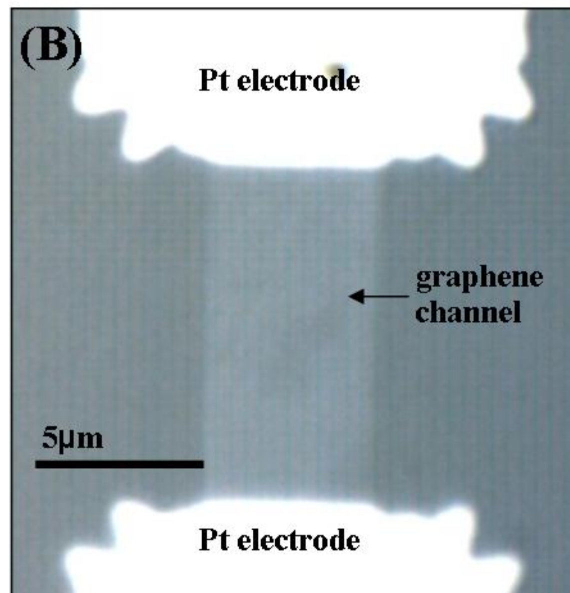


Figure B-21: Optical images of devices from Graph_C sample C-781. (A) This device has graphene missing from the conduction channel. Its electrical performance was not included in conductivity and mobility analysis. (B) This device has uniform graphene in the conduction channel. Its electrical performance was included in all data analysis.

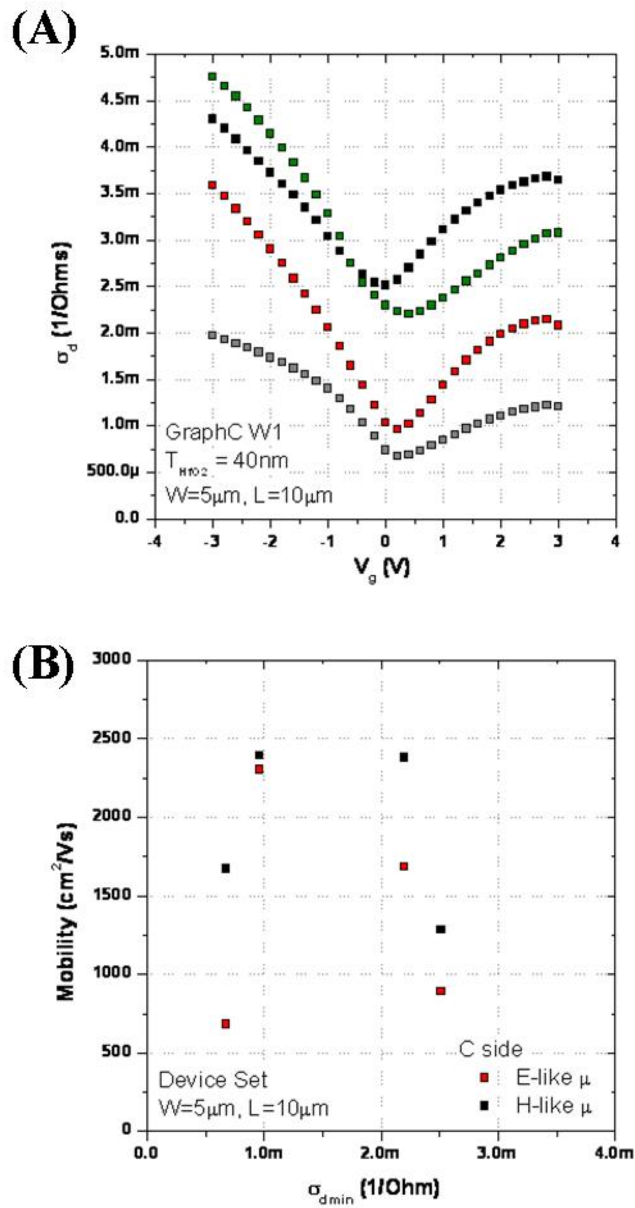


Figure B-22: Electrical data for Graph_B graphene/SiC sample C-781. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. On average, the electron mobility is lower than the hole mobility.

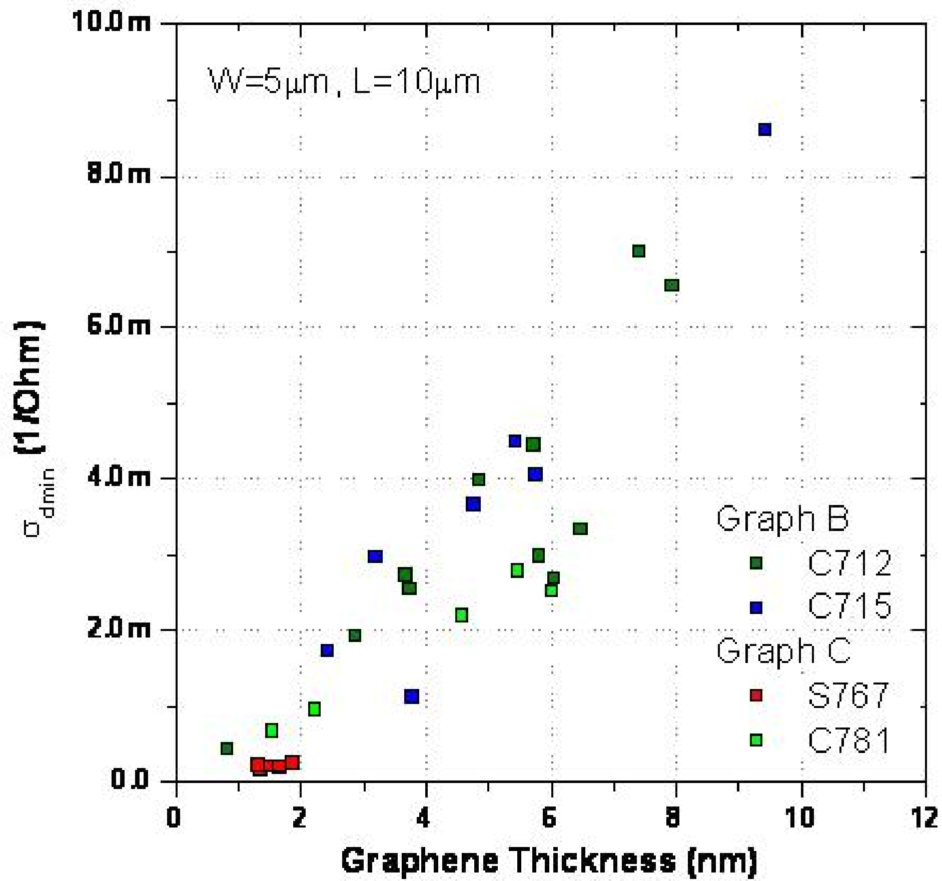
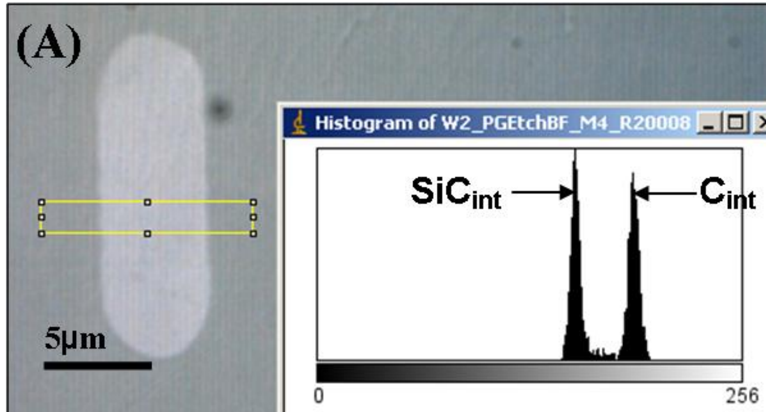


Figure B-23: Plot showing the relationship between minimum conductivity vs. minimum cross-sectional thickness in the graphene conduction channel. The relationship suggests the thinnest graphene cross section acts as the bottleneck to charge conduction. The data also shows that thicker graphene regions conduct more current, and the linear relationship implies that each graphene sheet conducts a comparable level of current, which is given by the slope of the best fit line.



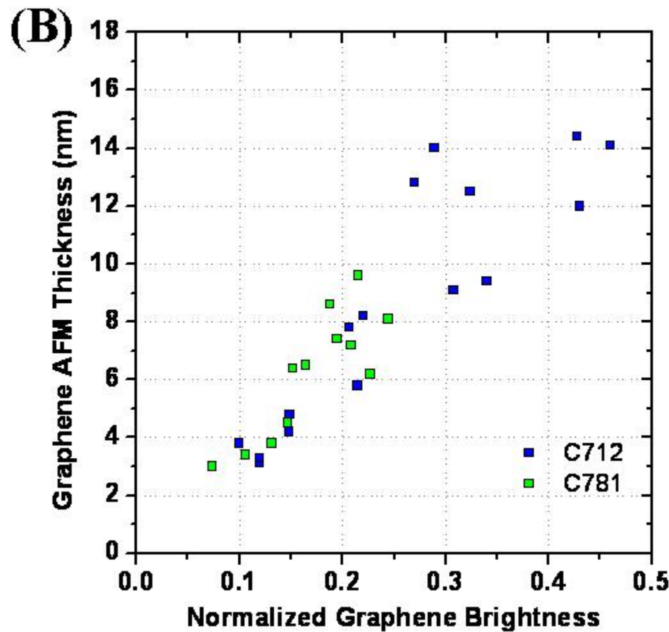


Figure B-24: When looking at graphene under an optical microscope, brighter regions correspond to thicker graphene and dimmer regions correspond to thinner graphene. (A) The normalized graphene brightness (NGB) is calculated as (C_{int}-SiC_{int})/SiC_{int}, where C_{int} is the intensity (brightness) of the carbon region and SiC_{int} is the intensity of the SiC region. The intensity values are found using a histogram from a program such as Gimp. The NGB value tells how bright a graphene region is relative to its SiC background. (B) AFM measurements of graphene step heights plotted against NGB. The linear relationship confirms that brighter looking regions correspond to thicker regions of graphene.

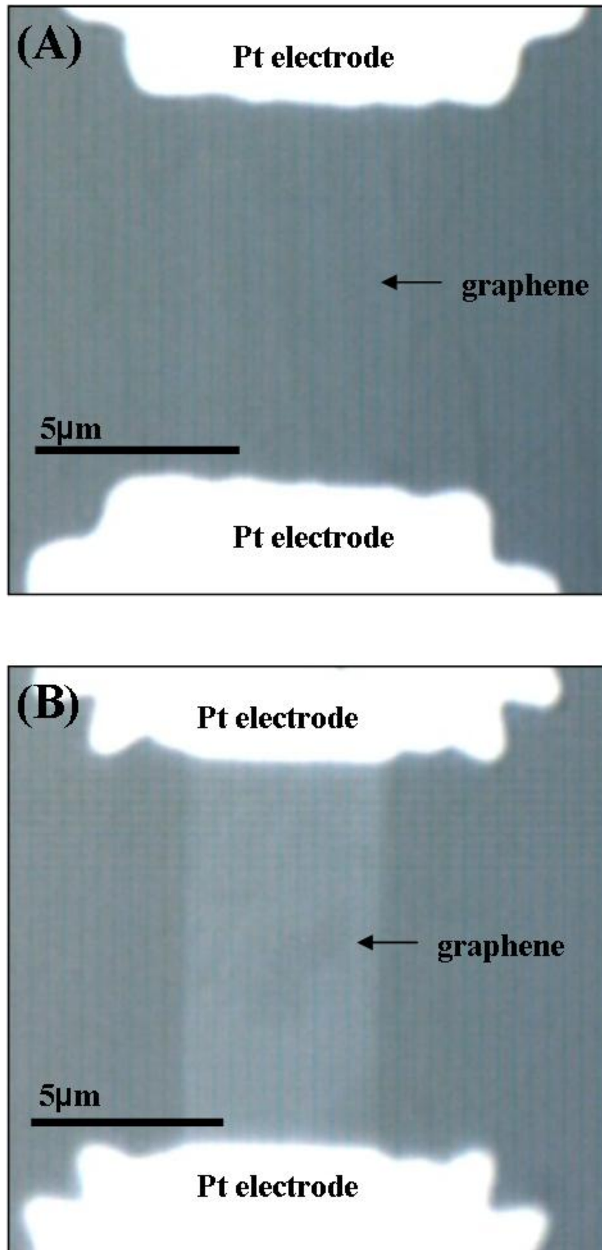


Figure B-25: Optical images comparing graphene conduction channels between a Si-face and a C-face graphene/SiC sample. (A) Device from S-767 after Pt source/drain patterning. The graphene conduction channel is barely visible. (B) Device from C-781, also after Pt source/drain patterning. The graphene conduction channel is much brighter than the graphene from S-767, indicating a much thicker graphene film.

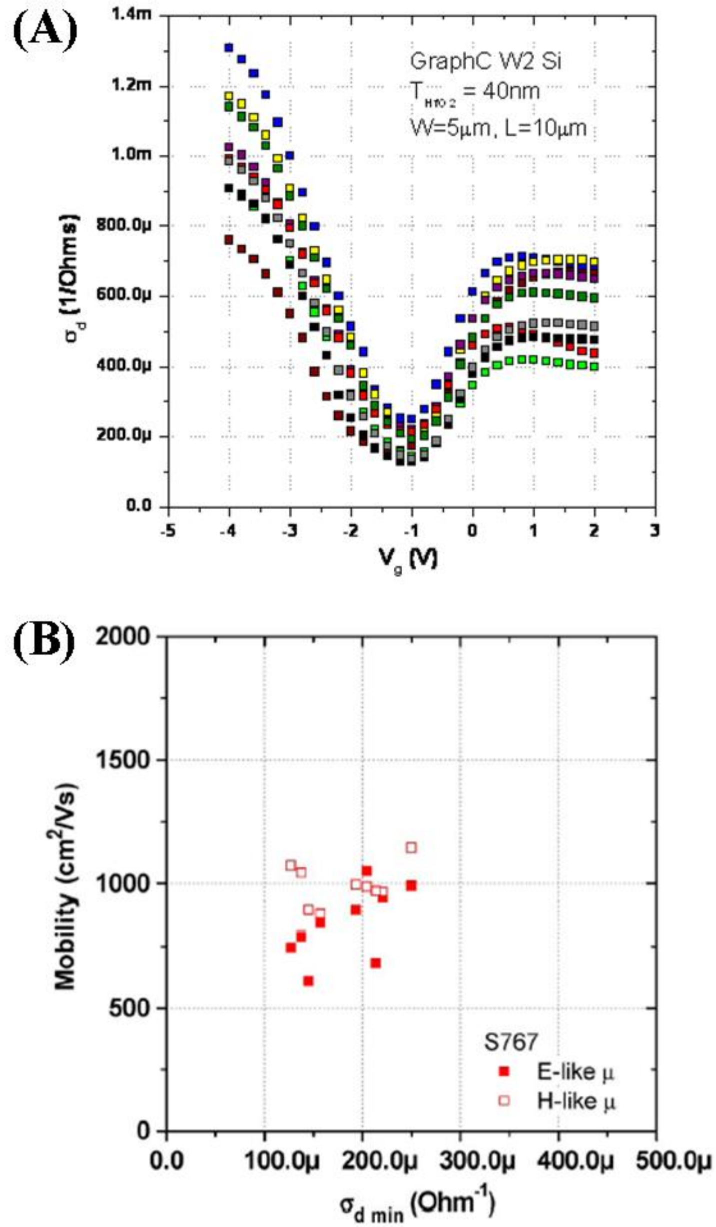


Figure B-26: Electrical data for Graph_B graphene/SiC sample C-781. (A) I_d-V_g data for the different devices. V_d was held at 0.5V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices. On average, the electron mobility is lower than the hole mobility.

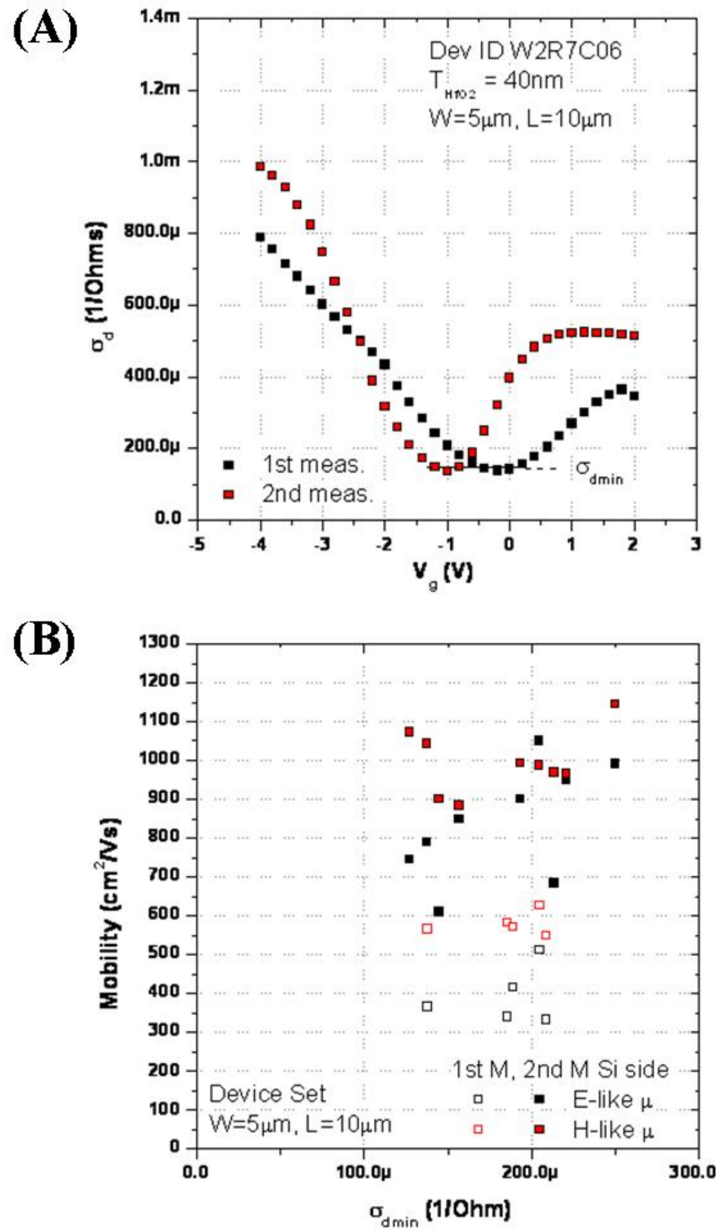


Figure B-27: Dielectric charging effects for a device on graphene/SiC sample S-767. (A) Shifts in the minimum conduction voltage between the first and second I_d–V_g measurements. (B) Changes in charge carrier mobility between the first and second I_d–V_g measurements.

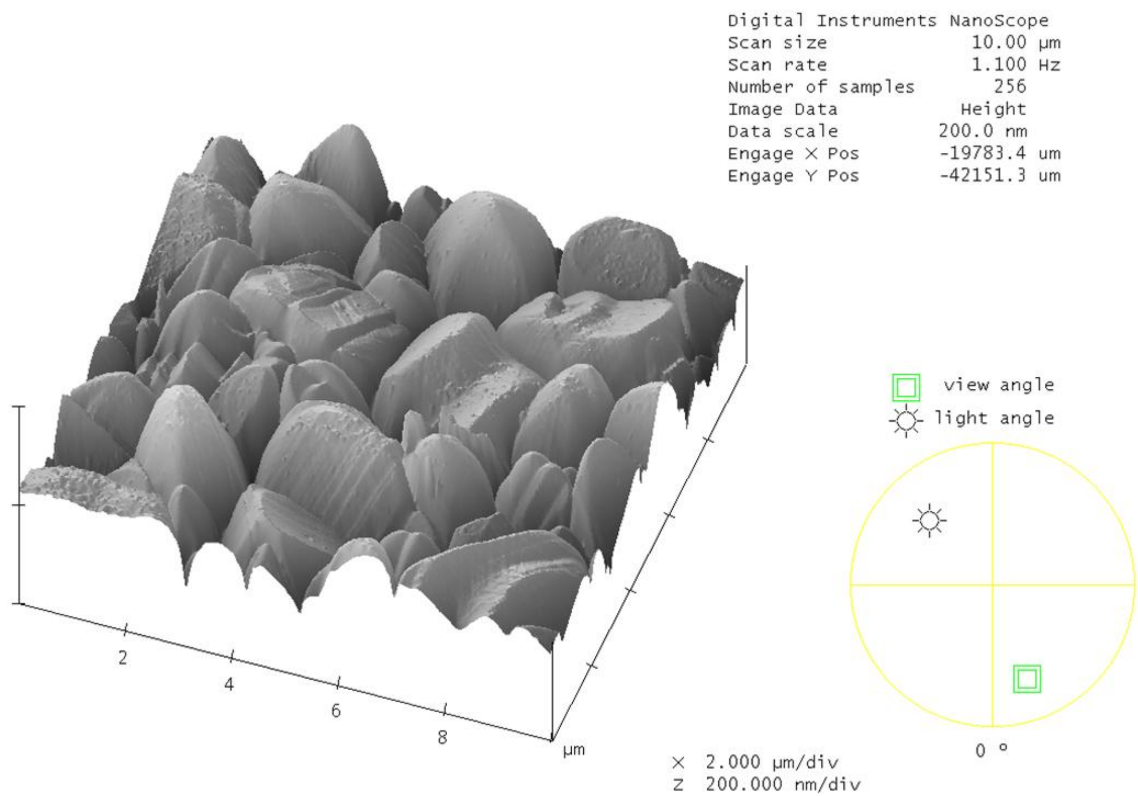


Figure B-28: AFM image showing the post-anneal grain structure of the Ni used for graphene CVD.

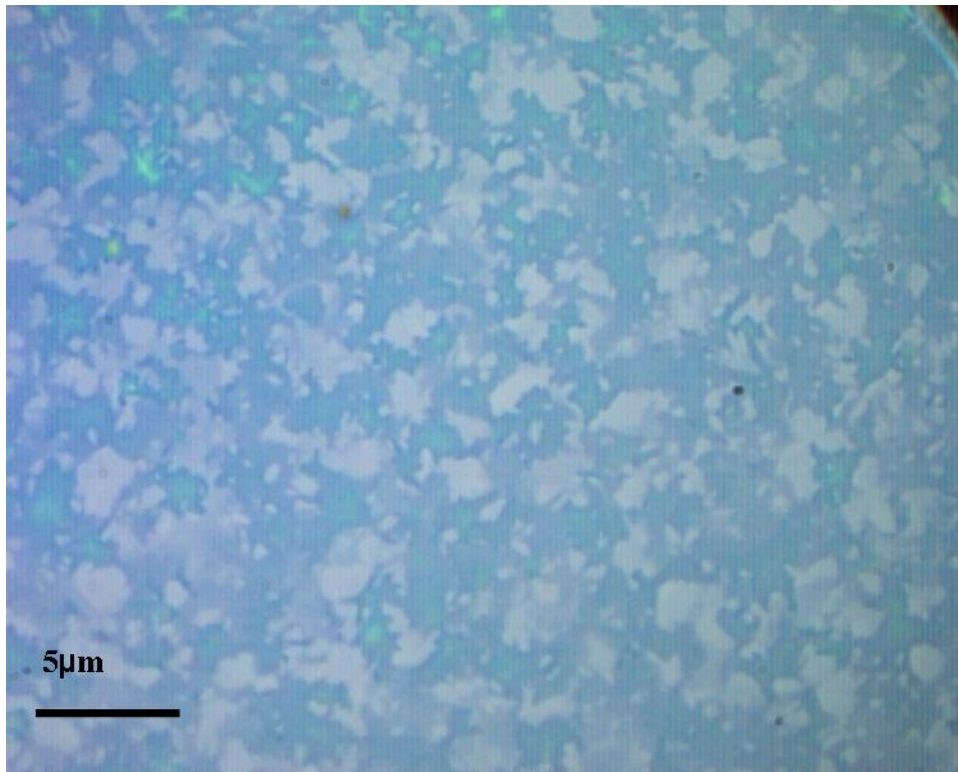


Figure B-29: Optical image of CVD graphene after it is transferred onto a 500nm oxide wafer. A prominent grain structure in the graphene is evident in the scattering of light (thin) and dark (thick) regions.

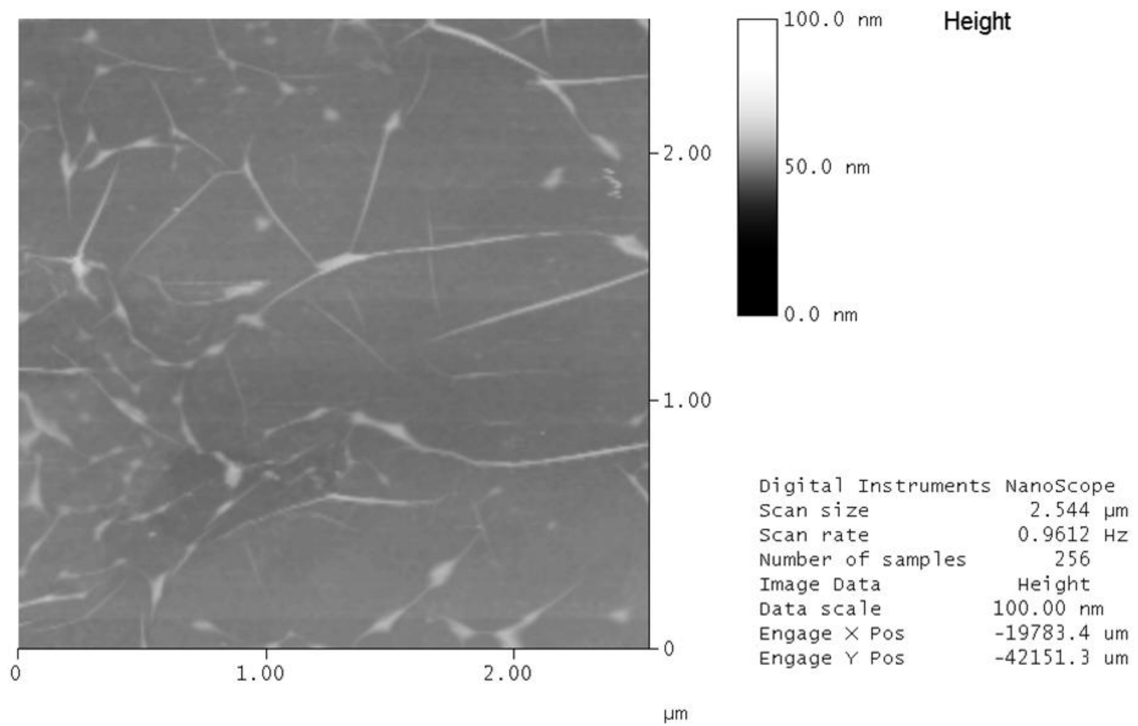


Figure B-30: AFM image of CVD graphene after it is transferred onto a smooth oxide wafer. Ripples and folds in the graphene are evident, suggesting that the graphene exists as a continuous layer.

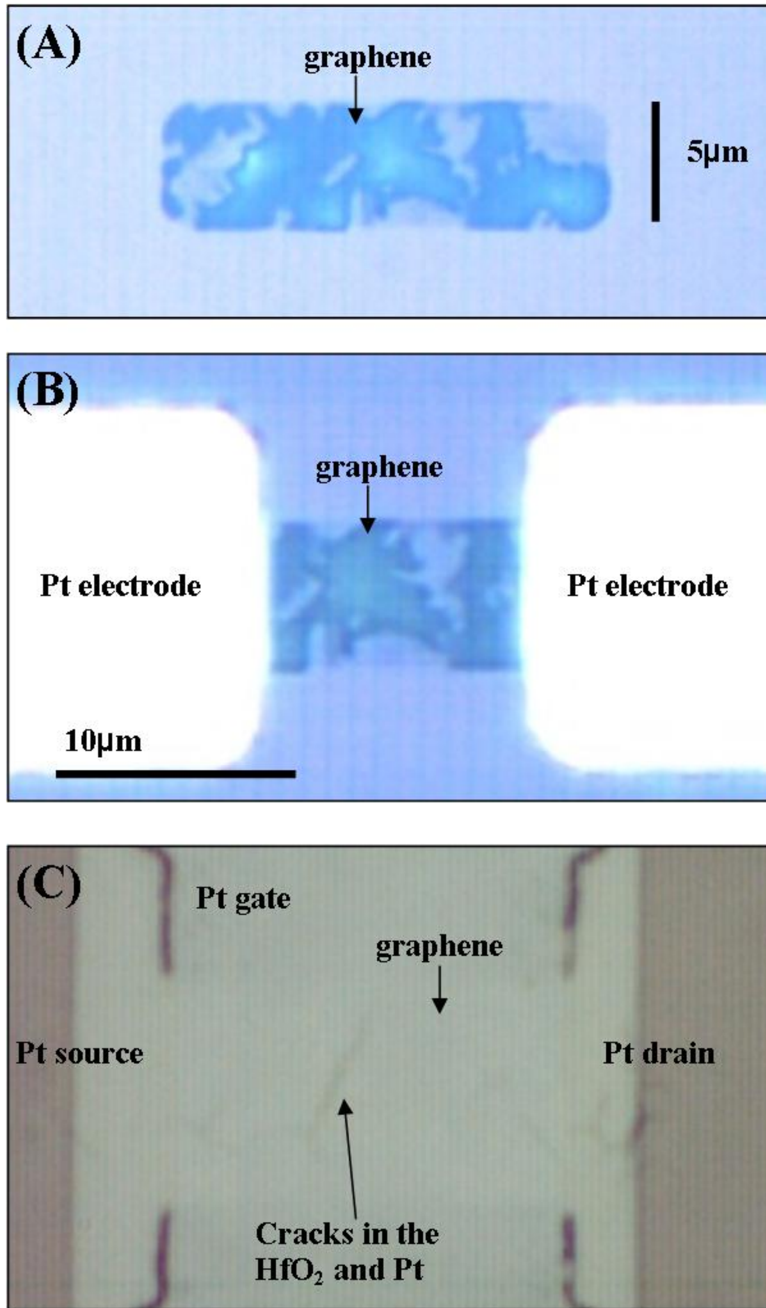


Figure B-31: Optical images of the same graphene device through the various fabrication steps. (A) The graphene conduction channel is patterned. (B) Pt source/drain contacts are patterned onto the graphene. (C) A finished graphene device after HfO_2 deposition and Pt gate deposition. As was the case for graphene/SiC devices, the HfO_2 cracked on thick regions of graphene.

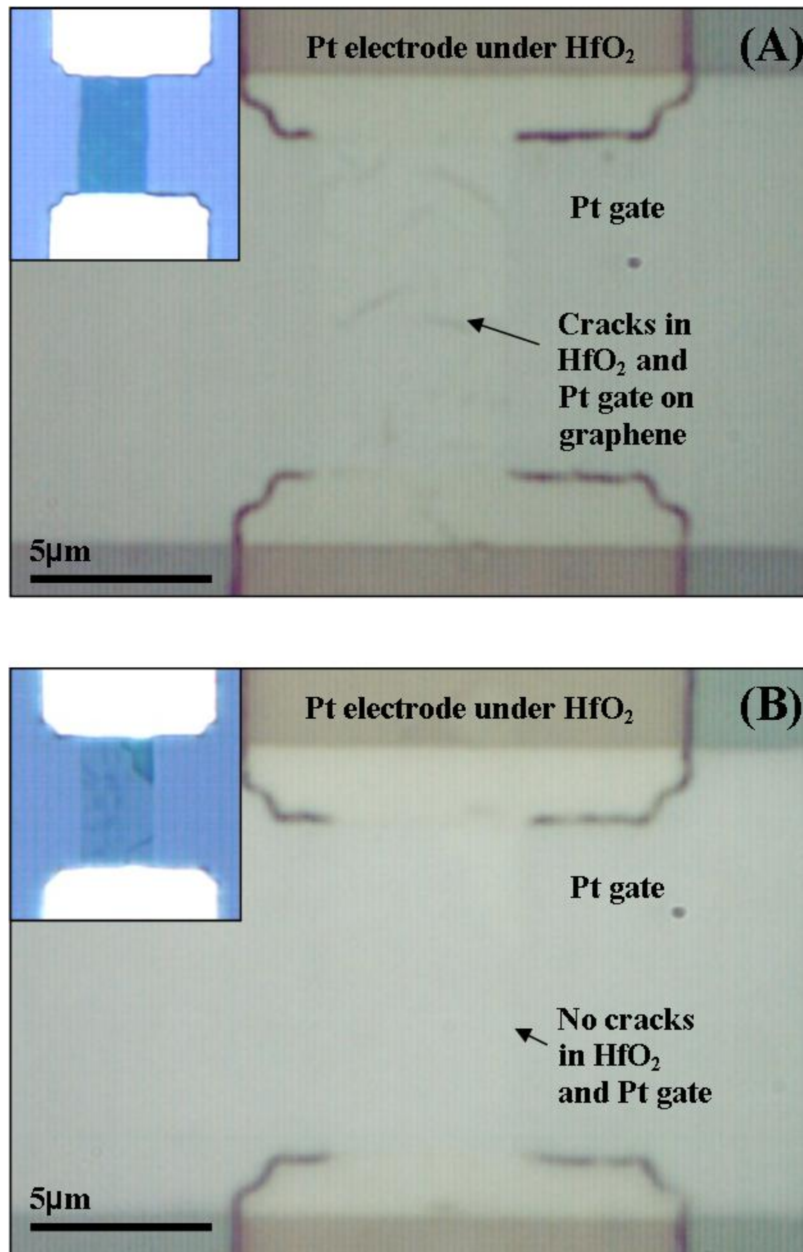


Figure B-32: Optical images of finished Graph_F devices showing cracks in the Pt/HfO_2 gate stack on thick graphene regions but not on thin regions. (A) The HfO_2 gate dielectric and Pt gate showed visible cracks on top of the graphene conduction region. Inset: optical image of the same device prior to HfO_2 deposition. The graphene conduction channel is mostly uniform, thick graphene. (B) The HfO_2 gate dielectric and Pt gate shows no visible cracks on top of the graphene conduction region. Inset: optical image of the same device prior to HfO_2 deposition. The graphene conduction channel is mostly uniform, thin graphene.

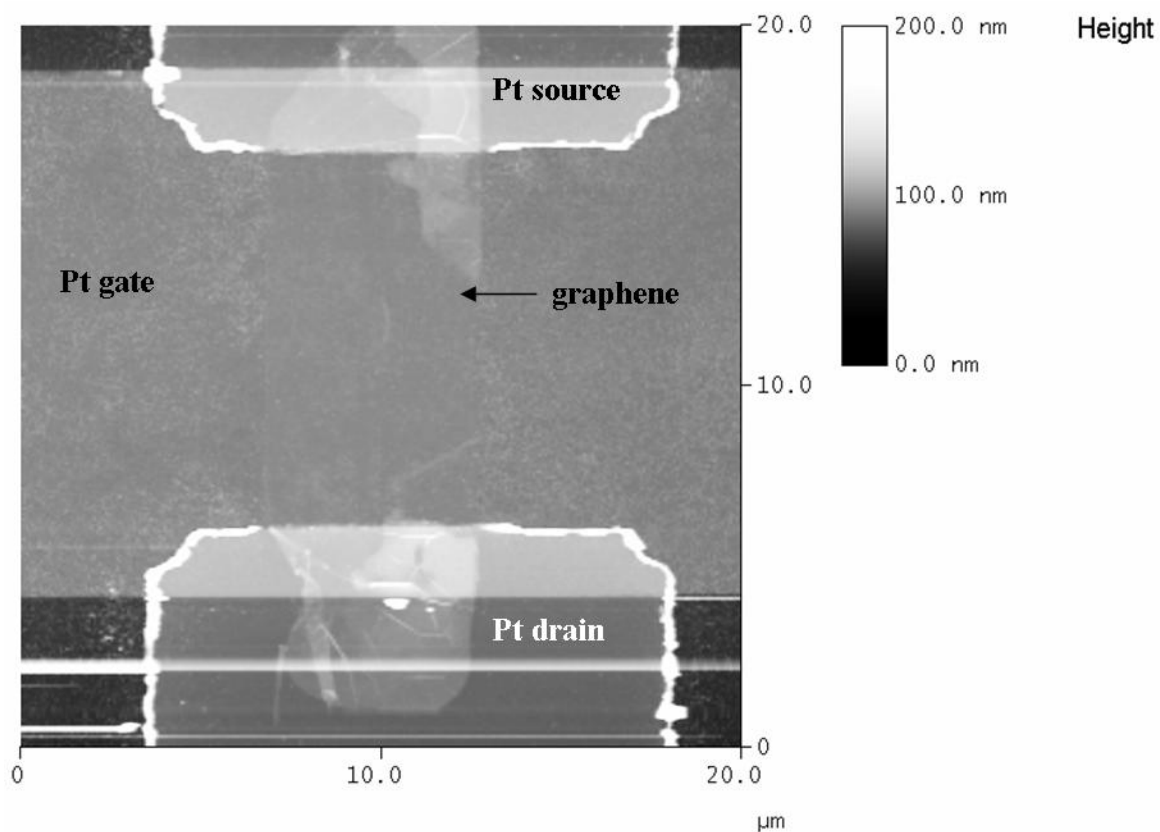


Figure B-33: AFM image of a Graph_F device with mostly uniformly thin graphene. Step height measurements indicate the graphene is roughly 1.5nm thick. This is the same device shown in Figure B-32(B).

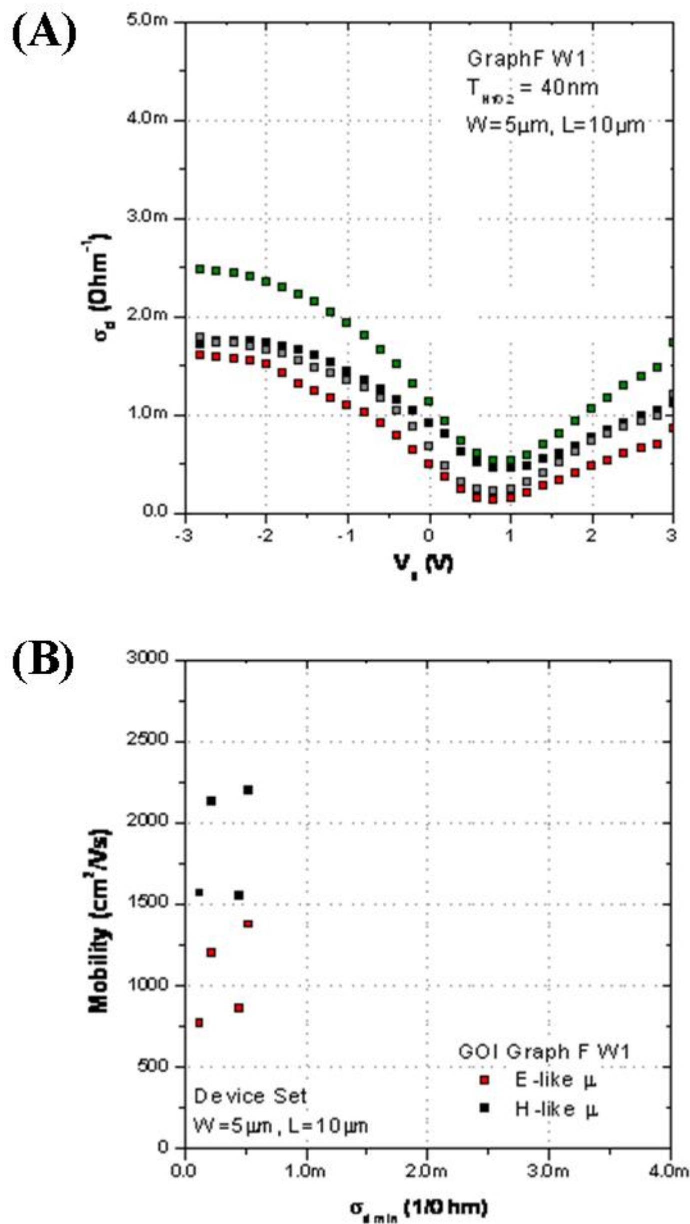


Figure B-34: Electrical data for Graph_F. (A) I_d-V_g data for the different devices. V_d was held at 0.1V, V_s was held at 0V. (B) Calculated electron and hole mobilities for the different devices.

THIS PAGE INTENTIONALLY LEFT BLANK

Bibliography

[1] web image, < http://www.ecn.purdue.edu/WBG/Introduction/Index.html>.

[2] Cree Substrate and Epitaxy Pricing Guide, February 2008.

[3] Special thanks to MIT Professor Akinwande and Annie Wang.

[4] White Paper: Introducing the 45nm Next-Generation Intel Core Microarchitecture. web document, <http://www.intel.com/technology/architecture-silicon/intel64/45nm-core2_whitepaper.pdf>, 2007.

[5] A. Bath, P.J. van der Put, J. G. M. Becht, J. Schoonman, and B. Lepley. Plasma enhanced chemical vapor deposition and characterization of boron nitride gate insullators on InP. *Journal of Applied Physics*, 70(8):4366–4370, 1991.

[6] Claire Berger, Zhimin Song, Xuebin Li, Xiaosong Wu, Nate Brown, Cecile Naud, Didier Mayou, Tianbo Li, Joanna Hass, Alexei N. Marchenkov, Phillp N. Conrad, Edward H. nd First, and Walt A. de Heer. Electronic Confinement and Coherence in Patterned Epitaxial Graphene. *Science*, 312(5777):1191–1196, 2006.

[7] M.T. Bohr, R.S. Chau, T. Ghani, and K. Mistry. The High-k Solution. *IEEE Spectrum*, 44(10):29–35, 2007.

[8] C. Boulas, J. V. Davidovits, F. Rondelez, and D. Vuillaume. Suppression of Charge Carrier Tunneling though Organic Self-Assembled Monolayers. *Physical Review Letters*, 76(25):4794–4800, 1996.

[9] Lay-Lay Chua, Peter K. H. Ho, Henning Sirringhaus, and Richard H. Friend. High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors. *Applied Physics Letters*, 84(17), 2004.

[10] Lay-Lay Chua, Jana Zaumseil, Jui-Feng Chang, Eric C.-W. Ou, Peter K.-H. Ho, Henning Sirringhaus, and Richard H. Friend. General observation of n-type field-effect behaviour in organic semiconductors. *Nature*, 434, 2005.

[11] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume. Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films. *Applied Physics Letters*, 76(14):1941–1943, 2000.

[12] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li. Large-scale complementary integrated circuits based on organic transistors. *Nature*, 403:521–523, 2000.

[13] C. D. Dimitrakopoulos and D. J. Mascaro. Organic thin-film transistors: A review of recent advances. *IBM Journal of Research and Development*, 45(1):11–27, 2001.

[14] Geraud Dubois, Robert D. Miller, and Willi Volksen. Spin-on Dielectric Materials. In Mikhail Baklanov, Martin Green, and Karen Maex, editors, *Dielectric Films for Advanced Microelectronics*, chapter 2. Wiley, 2007.

[15] T. Durkop, S. A. Getty, Enrique Cobas, and M. S. Fuhrer. Extraordinary Mobility in Semiconducting Carbon Nanotubes. *Nano Letters*, 4(1):35–39, 2004.

[16] Yoshihiro Etou, Tomoyoshi Tai, Tomohiko Sugiyama, and Takashi Sugino. Characterization of boron carbon nitride films with a low dielectric constant. *Diamond and Related Materials*, 11:985–988, 2002.

[17] Chris Ewels. web image, <http://www.ewels.info/img/science/graphite/graphene.gif>.

[18] Damon B. Farmer and Roy G. Gordon. Atomic Layer Deposition on Suspende Single-Walled Carbon Nanotubes via Gas-Phase Noncovalent Functionalization. *Nano Letters*, 6(4):699–703, 2006.

[19] C. Faugeras, A. Nerrire, M. Potemski, A. Mahmood, E. Dujardin, C. Berger, and W. A. de Heer. Few-layer graphene on SiC, pyrolitic graphite, and graphene: A Raman scattering study.

[20] Massimo V. Fischetti, Deborah A. Neumayer, and Eduard A. Cartier. Effective electron mobility in Si inversion layers in metaloxidesemiconductor systems with a high-

kinsulator: The role of remote phonon scattering. *Journal of Applied Physics*, 90(9), 2001.

[21] A.K. Geim and K.S. Novoselov. The rise of graphene. *Nature Materials*, 6:183–191, 2007.

[22] David J. Griffiths. *Introduction to Electrodynamics*. Prentice-Hall, 2003.

[23] G. Gu, Shu Nie, R. M. Feenstra, R. P. Devaty, W. J. Choyke, Winston K. Chan, and Michael G. Kane. Field effect in epitaxial graphene on a silicon carbide substrate. *Applied Physics Letters*, 90, 2007.

[24] Melinda Y. Han, Barbaros Özyilmaz, Yuanbo Zhang, and Philip Kim. Energy Band-Gap Engineering of Graphene Nanoribbons. *Physical Review Letters*, 98, 2007.

[25] J. Hass, R. Feng, T. Li, X. Li, Z. Zong, W. A. de Heer, P. N. First, E. H. Conrada, C.A. Jeffrey, and C. Berger. Highly ordered graphene for two dimensional electronics. *Applied Physics Letters*, 89, 2006.

[26] G.D. Hutcheson. The Economic Implications of Moore's Law. In H.R. Huff and D.C. Gilmer, editors, *High Dielectric Constant Materials: VLSI MOSFET Applications*, chapter 1. Springer, 2005.

[27] E.A. Irene. Sio_2 Based MOSFETS: Film Growth and Si-Sio_2 Interface Properties. In H.R. Huff and D.C. Gilmer, editors, *High Dielectric Constant Materials: VLSI MOSFET Applications*, chapter 3. Springer, 2005.

[28] Ali Javey, Ryan Tu, Damon B. Farmer, Jing Guo, Roy G. Gordon, and Hongjie Dai. High Performance n-Type Carbon Nanotube Field-Effect Transistors with Chemically Doped Contacts. *Nano Letters*, 5(2):345–348, 2005.

[29] Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee. Electrical Characteristics of Highly Reliable Ultrathin Hafnium Oxide Gate Dielectric. *IEEE Electron Device Letters*, 21(4):181–183, 2000.

[30] Yusaku Kato, Shingo Iba, Ryohei Teramoto, Tsuyoshi Sekitani, Takao Someya, Hiroshi Kawaguchi, and Takayasu Sakurai. High mobility of pentacene field-effect transistors with polyimide gate dielectric layers. *Applied Physics Letters*, 84(19):3789–3791, 2004.

[31] Jakub Kedzierski, Pei-Lan Hsu, Paul Healey, Peter W. Wyatt, Craig L. Keast, Mike Sprinkle, Claire Berger, and Walt A. de Heer. Epitaxial graphene transistors on sic substrates. *IEEE Transactions on Electron Devices*, 55(8):2078–2085, 2008.

[32] Hagen Klauk, Marcus Halik, Ute Zschieschang, Gúnter Schmid, Wolfgang Radlik, and Werner Weber. High-mobility polymer gate dielectric pentacene thin film transistors. *Journal of Applied Physics*, 92(9), 2002.

[33] Hagen Klauk, Ute Zschieschang, Jens Pflaum, and Marcus Halik. Ultralow-power organic complementary circuits. *Nature*, 445:745–748, 2007.

[34] E. Kooi and A. Schmitz. Brief Notes on the History of Gate Dielectrics in MOS Devices. In H.R. Huff and D.C. Gilmer, editors, *High Dielectric Constant Materials: VLSI MOSFET Applications*, chapter 2. Springer, 2005.

[35] Ioannis Kymissis, Akintunde Ibitayo Akinwande, and Vladimir Bulovic. A Lithographic Process for Integrated Organic Field-Effect Transistors. *Journal of Display Technology*, 1(2):289–294, 2005.

[36] Max C. Lemme, Tim J. Echtermeyer, Matthias Baus, and Heinrich Kurz. A graphene field-effect device. *IEEE Electron Device Letters*, 28(4):282–284, 2007.

[37] F. Lime, K. Oshima, M. Cassé, G. Ghibaudo, S. Cristoloveanu, B. Guillaumot, and H. Iwai. Carrier mobility in advanced CMOS devices with metal gate and Hfo_2 gate dielectric. *Solid State Electronics*, 47:1617–1621, 2003.

[38] G. Lucovsky and J.L. Whitten. Electronic Structure of Alternative High-k Dielectrics. In H.R. Huff and D.C. Gilmer, editors, *High Dielectric Constant Materials: VLSI MOSFET Applications*, chapter 11. Springer, 2005.

[39] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avourisa. Single- and multi-wall carbon nanotube field-effect transistors. *Applied Physics Letters*, 73(17):2447–2449, 1998.

[40] Michael E. Mills, Paul Townsend, Dan Castillo, Steve Martin, and Albert Achen. Benzocyclobutene (DVS-BCB) polymer as an interlayer dielectric (ILD) material. *Microelectronic Engineering*, 33:327–334, 1997.

[41] R. Nave. Polarization of dielectric, parallel plate with dielectric. web document, <http://hyperphysics.phy-astr.gsu.edu/hbase/hframe.html>.

[42] Albert V. Nguyen, N. V. a Davydov, Deane Chandler-Horowitz, and Martin M. Frank. Sub-bandgap defect states in polycrystalline hafnium oxide and their suppression by admixture of silicon. *Applied Physics Letters*, 87, 2005.

[43] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov. Electric Field Effect in Atomically Thin Carbon Films. *Science*, 306:666–669, 2004.

[44] Taisuke Ohta, Aaron Bostwick, Thomas Seyller, Karsten Horn, and Eli Rotenberg. Controlling the Electronic Structure of Bilayer Graphene. *Science*, 313:951–954, 2006.

[45] Chuhei Oshima and Ayato Nagashima. Ultra-thin epitaxial films of graphite and hexagonal boron nitride on solid surfaces. *Journal of Physics, Condensed Matter*, 9:1–20, 1997.

[46] J.L. Plawsky, R. Achanta, W. Cho, O. Rodriguez, R. Saxena, and W.N. Gill. Mechanical and transport properties of low-k dielectrics. In Mikhail Baklanov, Martin Green, and Karen Maex, editors, *Dielectric Films for Advanced Microelectronics*, chapter 4. Wiley, 2007.

[47] J. Puigdollers, C. Voz, A. Orpella, R. Quidant, I. Martín, and R. Vetter, M.and Alcubilla. Pentacene thin-film transistors with polymeric gate dielectric. *Organic Electronics*, 5:67–71, 2004.

[48] M.A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, G. Pant, B. E. Gnade, and R. M. Wallace. Ultrascaled hafnium silicon oxynitride gate dielectrics with excellent carrier mobility and reliability. *Applied Physics Letters*, 87, 2005.

[49] Maria A. Rampi, Olivier J. A. Schueller, and George M. Whitesides. Alkanethiol self-assembled monolayers as the dielectric of capacitors with nanoscale thickness. *Applied Physics Letters*, 72(14):1781–1783, 1998.

[50] Alfonso Reina, Xiaoting Jia, John Ho, Daniel Nezich, Hyungbin Son, Vladimir Bulovic, Mildred S. Dresselhaus, and Jing Kong. Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition. Submitted to Nano Letters, 2008.

[51] Yakov Roizin and Vladimir Gritsenko. Pno Structures and Oxynitrides in Modern Microelectronics: Material Science, Characterization and Application. In Mikhail Baklanov, Martin Green, and Karen Maex, editors, *Dielectric Films for Advanced Microelectronics*, chapter 6. Wiley, 2007.

[52] H. Shioyama. Cleavage of graphite to graphene. *Journal of Materials Science Letters*, 20:499–500, 2001.

[53] J.H. Stathis. Reliability limits for the gate insulator in CMOS technology. *IBM Journal of Research and Development*, 46(2/3):265–281, 2002.

[54] S. Strite and Morkoç. GaN, AlN, and InN: A review. *Journal of Vacuum Science and Technology B*, 10(4):1237–1268, 1992.

[55] Tetsuo Takahashi, Taishi Takenobu, Jun Takeya, and Yoshihiro Iwasa. Ambipolar organic field-effect transistors based on rubrene single crystals. *Applied Physics Letters*, 88, 2006.

[56] Yuan Taur and Tak H. Ning. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 1998.

[57] Akira Toriumi and Koji Kita. Material Engineering of High-k Gate Dielectrics. In Mikhail Baklanov, Martin Green, and Karen Maex, editors, *Dielectric Films for Advanced Microelectronics*, chapter 7. Wiley, 2007.

[58] K. N. Narayanan Unni, Sylvie Dabos-Seignon, and Jean-Michel Nunzi. Improved performance of pentacene field-effect transistors using a polyimide gate dielectric layer. *Journal of Physics D: Applied Physics*, 38:1148–1151, 2005.

[59] K.N. Narayanan Unni, Sylvie Dabos-Seignon, Ajay K. Pandey, and Jean-Michel Nunzi. Influence of the polymer dielectric characteristics on the performance of pentacene organic field-effect transistors. *Solid State Electronics*, 52:179–181, 2008.

[60] Lisa M. Viculis, Julia J. Mack, and Richard B. Kaner. A Chemical Route to Carbon Nanoscrolls. *Science*, 299:1361, 2003.

[61] D. Vuillaume, C. Boulas, J. Collet, J. V. Davidovits, and F. Rondelez. Organic insulating films of nanometer thickness. *Applied Physics Letters*, 69(11):1646–1648, 1996.

[62] P.R. Wallace. The band theory of graphite. *Physical Review*, 71(9):622–634, 1947.

[63] R.M. Wallace and G.D. Wilk. Materials Issues for High-k Gate Dielectric Selection and Integration. In H.R. Huff and D.C. Gilmer, editors, *High Dielectric Constant Materials: VLSI MOSFET Applications*, chapter 9. Springer, 2005.

[64] Yee Chia Yeo, Qiang Lu, Wen Chin Lee, Tsu-Jae King, Chenming Hu, Xiewen Wang, Xin Guo, and T. P. Ma. Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric. *IEEE Electron Device Letters*, 21(11):540–542, 2000.

[65] Yuanbo Zhang, Yan-Wen Tan, Horst L. Stormer, and Philip Kim. Experimental observation of the quantum Hall effect and Berrys phase in graphene. *Nature*, 438:201–204, 2005.

[66] S.Y. Zhou, G.-H. Gweon, A.V. Federov, P.N. First, W.A. de Heer, D.-H. Lee, F. Guinea, A.H. Castro Neto, and A. Lanzara. Substrate-induced bandgap opening in epitaxial graphene. *Nature Materials*, 6:770–775, 2007.

[67] W. J. Zhu, T. P. Ma, S. Zafar, and T. Tamagawa. Charge Trapping in Ultrathin Hafnium Oxide. *IEEE Electron Device Letters*, 23(10):597–599, 2002.