

**A Single Supply Wide Bandwidth 4:1 Video Multiplexer
in an 8GHz Dielectrically Isolated Complementary Bipolar Process**

by

Shan Wang

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

May 1, 1998

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Author

Department of Electrical Engineering and Computer Science
May 1, 1992

Certified by

Professor James K. Roberge
Thesis Supervisor (MIT)

Certified by

Kimo Tam
Thesis Supervisor (Analog Devices Inc.)

Accepted by

Arthur C. Smith
Chairman, Department Committee on Graduate Theses

MIT
TECHNOLOGY

0113 41233

Eng.

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ABSTRACT

A high performance monolithic 4:1 analog multiplexer implemented in an 8 GHz dielectrically isolated complementary bipolar process was designed and simulated. It is useful in many general purpose high-speed applications such as driving an $150\ \Omega$ cable or an analog to digital (A/D) converter. This switched transconductance amplifier 4:1 video multiplexer has a current mode decoder, a voltage feedback amplifier and four PNP-differential-pair input stages. It has a -3 dB small signal bandwidth of 148 MHz and a slew rate of greater than 170 V/us. It has a differential gain and a differential phase error of 0.03% and 0.03° . With -113 dB of all-hostile crosstalk and -91 dB of off isolation at 10 MHz, this multiplexer is compatible with a 10 bits A/D converter. It has a channel switching time to 0.1% of 15 ns and consumes less than 6.4 mA on a 5 V single supply voltage. The output voltage swing of this multiplexer extends to within 50 mV of each rail, providing a wide output dynamic range. It offers a high-speed disable feature allowing the output to be put into a high impedance state for multi-stages so that the off channel does not load the output bus. This shutdown feature also reduces the supply current to less than 2.6 mA.

Thesis Supervisor: James K. Roberge
Title: Professor of Electrical Engineering

Acknowledgments

The author would like to extend special thanks to Kimo Tam for his general support and guidance, without which this project could not have been a success. Additional thanks go to Professor James Roberge who helped review the drafts of this thesis, corrected mistakes, and suggested additions.

I wish to thank my family for their love and encouragement. I want to thank my friend Jean Hsu for her support. Finally, special gratitude goes to my Physics teacher Ms. Caroline Wiggin at Brookline High School, who has significantly influenced my professional goals, both past and future.

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1.0 Introduction

A video multiplexer is designed for routing one of several wideband video signals to a single output. Many multiplexers in the marketplace claim to be suitable for high quality video applications. Multiplexers for conventional video (NTSC or PAL) should have a high fidelity extending from 5 MHz to 8 MHz. High definition video requires wide-band switches operating to 20 or 30 MHz. Specifications such as crosstalk and off-isolation at these frequencies become important in order to maintain the picture quality with minimal interference from other signal paths. A desirable video multiplexer should have wide bandwidth, fast switching speed, small switching glitch, high crosstalk rejection, and high input-to-output isolation. In color video applications, distortion of the multiplexer such as differential gain and phase should be low so that the changes in contrast and color of the displayed picture are minimized. The design of the multiplexer should be compact and low-power to enable a high level of integration. A high-impedance disable output state is desirable to allow the user to connect the outputs of several multiplexers to create a multiplexer with a larger number of inputs.

The switched transconductance amplifier 4:1 analog multiplexer design described in this thesis is targeted for the video switch market. This multiplexer is implemented on Analog Devices' proprietary 8 GHz dielectrically isolated complementary bipolar process, XFCB1.5. It is based on an AD8041 operational amplifier and is able to operate on a 3 ~ 8 V single supply voltage, but is optimized for 5 V. Research shows that this multiplexer is going to be the first single-supply video multiplexer in the market.

The chip pinout of the 4:1 video multiplexer is shown in Figure 1.1. Many specifications of this multiplexer are better than or equal to many leading competitors' products.

The multiplexer has a -3 dB small-signal bandwidth of 148 MHz and a 10 ns channel switching time with a 48 mV peak-to-peak switching glitch. A similar product, MAX441, by Maxim, has a -3 dB small-signal bandwidth of 160 MHz, but its switching time is 25 ns with a switching glitch of 100 mV peak-to peak. The multiplexer's all-hostile crosstalk and off-isolation are -113 dB and -91 dB. It has a differential gain and a differential phase of 0.03% and 0.03°. The differential gain and differential phase of the MAX441 are about the same as our multiplexer, but its all-hostile crosstalk and off-isolation are both approximately 30 dB worse than ours. One of the recent Analog Devices' video multiplexer chips, the AD8174, has an input and output voltage range of ± 1.7 V and ± 740 mV from the power supplies respectively. The input voltage range of our multiplexer, however, can extend from 200 mV below the negative rail to within 1.46 V of the positive rail, and its output voltage swing can extend to within 50 mV of each rail, providing a wide output dynamic range. This 4:1 video multiplexer has a small die size of 844 μm by 872 μm , and

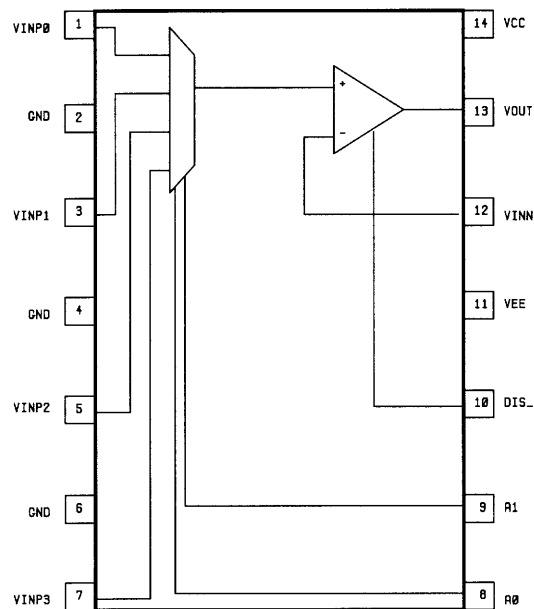


Figure 1.1 Video multiplexer chip pinout.

draws a low power supply current of 6.4 mA when it is enabled. Its power down feature reduces the supply current to 2.6 mA. It is useful in many general purpose high speed applications. For example, instead of using four slow analog to digital (A/D) converters and one digital multiplexer to digitize four video signals, one can economically use only one 4:1 video multiplexer and one fast A/D converter to accomplish the task. Its low quiescent power also makes it well suited for portable and battery powered applications where size and power are important considerations. Since the output of the multiplexer is at high-impedance when the circuit is disabled, two of these multiplexers can be wired together to produce a larger multiplexer as shown in Figure 1.2.

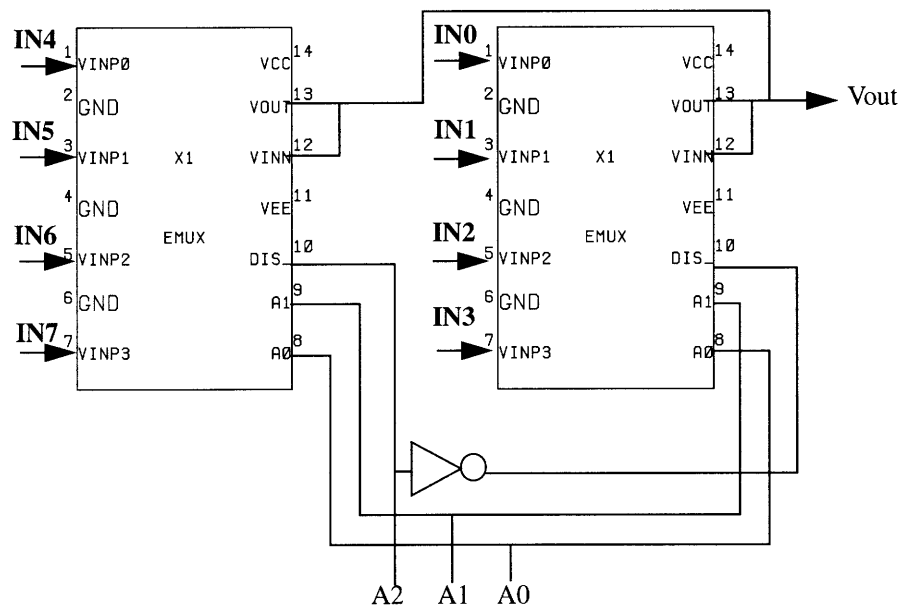


Figure 1.2 An 8:1 video multiplexer with gain of 1.

This thesis describes design techniques for the 4:1 analog multiplexer. Chapter 2 presents the overall circuit architecture and analyzes the AD8041 amplifier and several switching techniques. This is followed, in chapter 3, by circuit descriptions and discussions of several design issues of each cell of the multiplexer. It also provides a summary of

the computer simulated results and the conditions under which those results were collected. Chapter 4 discusses some issues raised in the course of the chip layout. Finally, the thesis summarizes the results and characterizes the new product.

2.0 Design Considerations

2.1 Overall Circuit Architecture

To choose a desirable multiplexer architecture, three alternative circuit techniques were considered [1]. Figure 2.1 shows the first circuit technique, where two current feedback amplifiers are configured as a 2:1 multiplexer. The disable pin of each amplifier is used as a switch. The amplifiers are connected as a gain of one, even though other non-inverting gains are possible depending upon the application. An appropriate choice of R_F allows the multiplexer to drive a high capacitive load, and low distortion is achievable using this architecture. A switched amplifier N:1 multiplexer allows only one amplifier to be on at any time and saves power, but the complete redundancy in each signal path will result in excessive die area. The switching time and glitch tend to be high since a large number of devices are changing states when an amplifier is enabled or disabled.

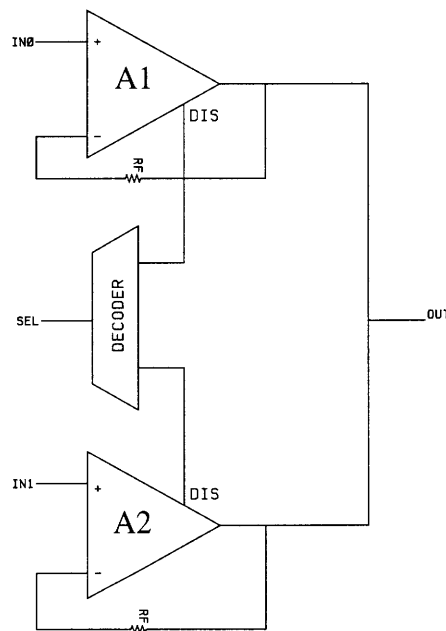


Figure 2.1 Switched amplifier 2:1 multiplexer.

The second circuit technique is shown in Figure 2.2. It is a switched open-loop buffer multiplexer whose switches (S_0 and S_1) are implemented using simple complementary emitter followers. The current sources of each switch can be shut off. For example, when switch S_0 is enabled, current sources I_1 and I_3 will provide emitter currents to transistors Q_1 and Q_3 respectively; these devices bias the bases of output transistors, Q_5 and Q_7 . In the meantime, current sources I_2 and I_4 are switched off to disable switch S_1 . This architecture can be found in Gennum's GY4102, Burr-Brown's MPC102, and Linear Technology's LT1203. Similar to the switched amplifier multiplexer, this design has a unidirectional signal path with high input impedance in any state. This type of multiplexer can be optimized for fast switching time or low glitch. The disadvantage of this architecture is that its nonzero output resistance results in a small gain error making it difficult to drive a video load. Adding a closed-loop amplifier to the output will correct this problem,

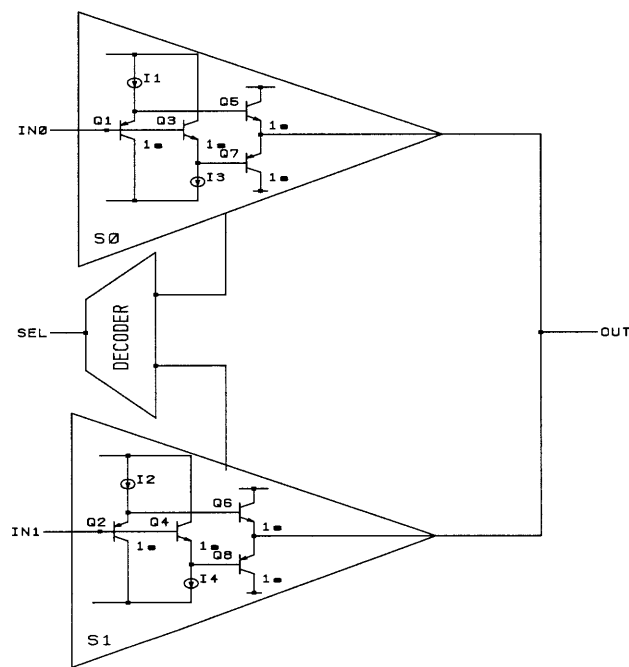


Figure 2.2 Switched open-loop buffer 2:1 multiplexer.

but the power consumption will be higher than the switched amplifier multiplexer due to the extra active switch. Offset problems may also be of concern since the signal path of the basic buffer contains unmatched NPN and PNP devices.

The third alternative circuit technique is a multiplexer with integrated input T switches [2] shown in Figure 2.3. When IN0 is selected, Q₃ is off and emitter follower Q₁, biased by current source I₁, drives the base of common-collector transistor Q₅, which is half of a differential pair formed by common-base transistor Q₇. The high gain from Q₇'s base to its collector provides a loop gain that works to equalize the base voltage of Q₆ and Q₇. When Q₄ is turned on, IN1 is isolated from the output, and Q₂ and Q₆ are both reversely biased. This T-switch structure has the advantage of bypassing both the emitter-base and the collector-base capacitances of the off transistor Q₆. However, the PNP emitter followers Q₁ and Q₂ increase the power consumption since they need high bias currents to maintain their dynamic performances and those currents are wasted through Q₃ and Q₄ when the input stage is disabled. Moreover, the input followers degrade the offset, noise and bandwidth of the circuit.

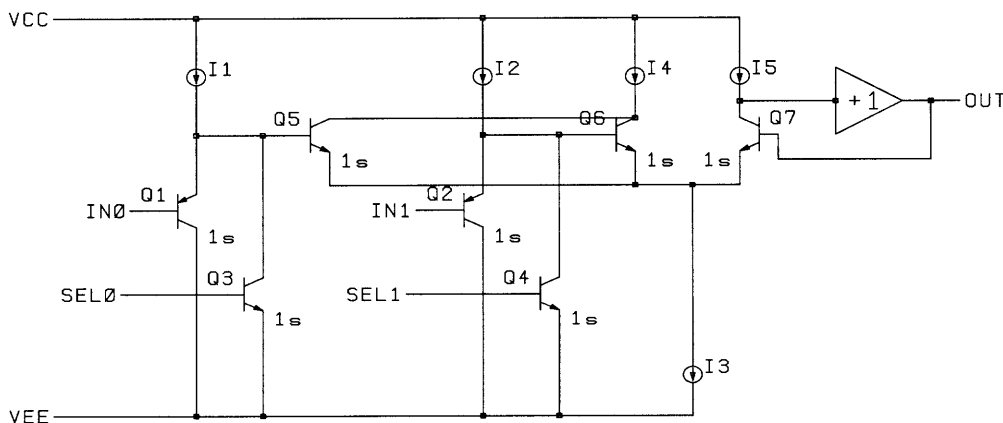


Figure 2.3 Maxim 2:1 multiplexer with integrated T switches (simplified schematic).

The 4:1 analog multiplexer described in this thesis is a switched transconductance (switched g_m) voltage feedback multiplexer. Figure 2.4 shows the block diagram of the overall circuit. A current mode decoder selects one of four transconductance input stages (GM0 ~ GM3) by steering in a fixed current I . Each GM stage is the PNP differential pair and the lower half of the folded cascode input stage of the AD8041. The selected GM stage outputs differential currents which feed into the other half of the folded cascode stage of the AD8041 operational amplifier (see Section 2.3), called amplifier A1 in the block diagram. The output of A1 is also the output of the multiplexer and can drive the common inverting input of all of the input GM stages through an optional feedback attenuator formed by R_F and R_G .

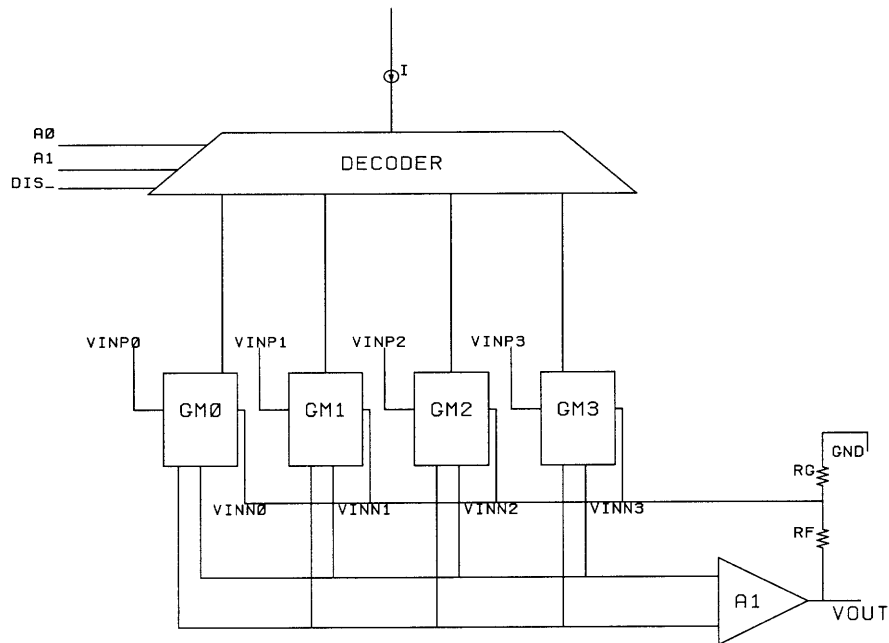


Figure 2.4 Block diagram of the switched transconductance amplifier 4:1 multiplexer.

This multiplexer topology offers high input impedance, low output impedance, low distortion, and external gain. The multiplexer's output capacitance is also low since the multiplexing function is accomplished internally. The power dissipation is minimized to a

little more than that of the operational amplifier since only one of the input stages is on at any time. Solely replicating the amplifier's input stage also makes this topology very compact in size. Since the channel switching only involves toggling a few input devices, the switching times and glitches are lower than those of a switched-amplifier multiplexer, although they may not be as good as those of a switched open-loop buffer multiplexer. This architecture inherits limitations such as the noninverting topology, and the asymmetrical expansion for an N:1 multiplexer when N is large, but they will not affect this multiplexer design.

2.2 High Frequency Processes

In the marketplace, video multiplexers are manufactured using a wide range of technologies such as CMOS, DMOS, bipolar and various combinations of the above. A multiplexer design often includes an amplifier circuit so that its output can swing very high, even rail-to-rail, without requiring a large swing at the input. The bipolar transistor's high transconductance-to-current ratio and high transition frequency f_T make it more suitable than a MOS transistor for the design of an operational amplifier. An amplifier implemented using bipolar transistors can provide high current drive and achieve a high bandwidth at low power dissipation.

The AD8041 operational amplifier, on which this multiplexer design is based, is fabricated in the XFCB (eXtra Fast Complementary Bipolar) Dielectrically-isolated (DI) process. The dielectric isolation eliminates parasitic substrate transistors and reduces high-temperature leakage and the collector-to-substrate capacitance. The XFCB process was introduced in 1993 at Analog Devices, featuring 4 GHz f_T NPN and 2.5 GHz PNP transis-

tors. The 4:1 multiplexer described in this thesis is implemented in the next generation process, known as XF1.5, which increases the speed and packing density by a factor of two.

With the improved photolithography tolerances of XF1.5, the minimum emitter width was reduced from 1.5 μm to 1.0 μm and the trench pocket of the minimum transistor was reduced from 5.5 by 19 μm to 3 by 10 μm . However the open-base breakdown voltage was reduced to 8V.

Both XFCB and XF1.5 include trimmable thin-film resistors of 100 to 1000 ohm/square with low capacitance and an extremely low voltage coefficient; low-parasitic metal-oxide-metal capacitors with a low-voltage coefficient and low-series resistance; and non-guard ringed Schottky diodes with greater than 8 V breakdowns and guard-ringed version with breakdowns over 18 V.

The XF1.5 process allows us to have devices twice as fast as those of the XFCB process; however, the speed of the amplifier does not get faster because of the change in the process. How fast the amplifier operates depends upon the compensation technique used by the circuit. Smaller parasitic capacitances benefiting from the new process have given us more phase margin and better crosstalk performance than those in the XFCB process. Since the transistor junction break down voltage is quite low in the XF1.5 process, the multiplexer will not be able to operate on $\pm 5\text{V}$ power supplies. More discussion can be found in Chapter 4 where the detailed circuit layout is described.

2.3 AD8041 Amplifier Circuit Overview

The AD8041, designed by Jeff Townsend of Analog Devices, is a low power, high-

speed, voltage feedback operational amplifier. It can operate on +3V to ± 5 V power supplies, and its input voltage range can extend from 200 mV below the negative rail to 1 V below the positive rail. Its unloaded output swings approximately rail to rail. Additionally, it features -3 dB bandwidth (gain=1) above 140 MHz, slew rate of 160 V/ μ s, and gain flatness of 0.1 dB to 30 MHz while offering a differential gain and phase error of 0.03% and 0.03 $^\circ$ on a single +5 V supply. The disable logic interface of the AD8041 is compatible with CMOS or open-collector logic. It can also be used for multiplexing by connecting the outputs of several AD8041s or for reducing power consumption.

Shown in Figure 2.5 is the simplified circuit diagram of the AD8041. It consists of a bias stage, a fully differential folded cascode input stage, a differential second gain stage with common-mode feedback, and a complementary common-emitter output stage along with a quiescent current control loop from the second stage (not shown in Figure 2.5).

This amplifier employs an NPO (negative positive zero) bias circuit that nominally results in a temperature-independent bias current. A PTAT (positively proportional to absolute temperature) current is set by Q_{44} , Q_{61} , and R_{31} . A CTAT (negatively proportional to absolute temperature) current is created by the lower emitter of Q_{74} and R_{33} . The collector current of Q_{74} sums both CTAT and PTAT currents to create an NPO current which is temperature independent to the first order. This current is then mirrored and supplied to the rest of the circuit by Q_{55} .

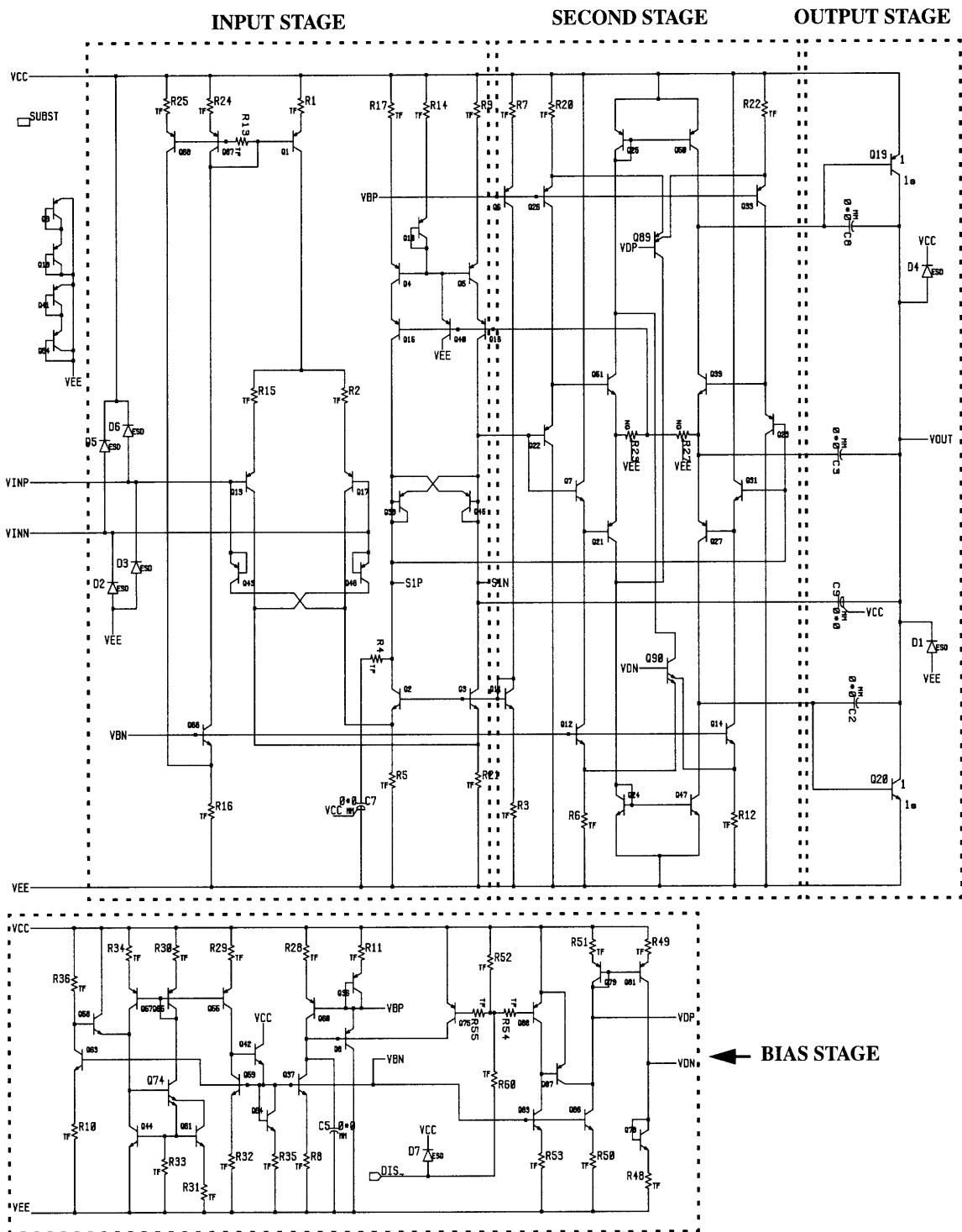


Figure 2.5 Simplified AD8041 amplifier schematic.

In the input stage, Q₄₃ and Q₄₆ provide collector-base capacitance compensation

for Q_{13} and Q_{17} . They compensate the current feed-through from C_u 's of the input devices and balance the circuit at VINN. The equation below shows the relationship between the collector current and V_{CE}

$$I_C = I_S \left(1 + \frac{V_{CE}}{V_A} \right) \left(\exp \frac{V_{BE}}{V_T} + 1 \right) \quad (2.1)$$

where I_C is the collector current of the transistor, I_S is the saturation current, V_A is the early voltage, and V_T is the thermal voltage. Since Q_{68} 's V_{CE} is higher than Q_{67} 's, the collector current of Q_{68} will be slightly higher than that of Q_{67} . Resistor R_{13} provides base current compensation by making Q_1 's base voltage slightly lower than Q_{67} 's. The bias current of the input stage is separate from the rest of the amplifier so that Q_1 can be saturated (when the input is driven near the positive supply) without disturbing the rest of the circuit. The cascode current mirrors Q_4/Q_{15} and Q_5/Q_{16} provide the active loads for the input stage. This folded cascode input stage contributes the most of the entire amplifier's voltage gain. The second gain stage converts differential inputs into two single-ended outputs. It provides common-mode feedback to the bases of Q_{15} and Q_{16} to bias the common mode level of S1P/S1N to be approximately two V_{BE} 's below the positive supply. The second stage only provides moderate gain, but its complementary common-emitter design allows the amplifier to drive a heavy load without the need of emitter followers. It allows the AD8041 to drive 50mA of output current to within 0.5V of the supply rails. The output stage of this amplifier involves several proprietary feedback loops and biasing translinear loops to control the standing current in the output devices and reduce distortion. The details of their design consideration are not discussed

here.

The compensation of the AD8041 is accomplished by capacitors C_7 and C_9 . Capacitor C_9 is used as the Miller capacitor for the second and third stages, while C_7 is used as the common-mode feedback compensation capacitor. Miller capacitors C_2 and C_8 are placed across the output devices to compensate the complementary output stage. Capacitors C_3 and C_9 allow the output impedance of the amplifier to become capacitive at a high frequency in order to reduce stability problems when driving capacitive loads. The AD8041 also has disable/power-down capability. When the input to DIS_ goes low, transistors Q_{89} and Q_{90} are turned on, and current sources such as Q_6 , Q_{26} , Q_{33} and Q_{19} are shut off. This configuration only turns off the amplifier's output while leaving the input powered. The major shortcoming of this disable technique is that it saturates many devices. When the amplifier is disabled, transistors Q_{50} , Q_{51} and Q_{47} are deeply saturated, while when the amplifier is enabled, transistors Q_{87} , Q_{78} and Q_{79} are saturated. Since a storage delay is required for the saturated transistor to remove the excess carriers from the base, while there is no change in the collector current [3], the turn-on time and turn-off time of the amplifier are very long -- 320ns and 120ns respectively. Since the AD8041 does not have a ground pin, the DIS_ logic threshold is very close (one V_{BE}) to the positive power supply, which results in a poor noise margin.

2.4 Switching Schemes

A suitable switch scheme needs to be implemented for the current mode decoder seen in Figure 2.1. The decoder should be able to select one of four transconductance

input stages quickly and steer in a fixed current I (in this case, 192 μA). In the AD8041 circuit, this current is provided by an NPO current mirror, and is separated from the rest of the amplifier's bias current so that the rest of the circuit will not be disturbed even if the current source to the input stage is saturated (when the input is driven high). A desirable switch scheme for the multiplexer should not only retain these features, but should also be fast and consume the least amount of input headroom possible with little power consumption. This section first surveys some alternative switch schemes, then covers the switching technique employed in the 4:1 video multiplexer decoder circuit. Assuming the transistor ratio is 1:N and the switching is among M channels, the total supply current and the number of devices used for steering the fixed current I are summarized for each switch scheme.

One way of switching the current is shown in Figure 2.6 where Q_1 and Q_2 form a current mirror with the area ratio 1:N so that Q_2 carries N times the current of Q_1 . Initially, control input A is tied to the V_{EE} , and Q_3 is off. Once A is brought up to one V_{BE} above the negative supply, Q_3 is turned on and quickly reaches saturation. The

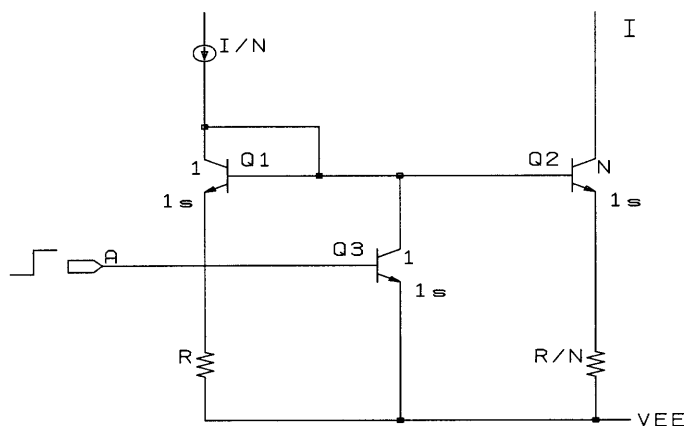


Figure 2.6 Switching scheme A.

current I/N which used to flow into Q_1 now flows into Q_3 . Since the V_{CEsat} of Q_3 is not as high as the V_{BE} of Q_1 and Q_2 , Q_1 and Q_2 will be off and conduct almost no current. This switching technique can turn Q_2 's collector current off completely and provide a sharp transient, but the problem with this type of switching is that it not only involves saturating a device, which will slow down the transient, but also wastes current, when Q_2 is off. The total supply current I_{tot} and the number of transistors n_{tot} used for an $M:1$ switching are listed below.

$$I_{tot} = \frac{I}{N} + I + \frac{I}{N} \cdot (M - 1) \quad (2.2)$$

$$n_{tot} = 3 \cdot M \quad (2.3)$$

At most, turning a high-gain transistor on using a steady-state base current is β_F times slower than the turn-on time of a diode. As i_C builds up, a larger and larger fraction of the base current goes into feeding recombination in the base so that less is available to charge the base [4]. Figure 2.7 shows a scheme where the switching can be accomplished through a current mirror by turning the controlled current I_1 on and

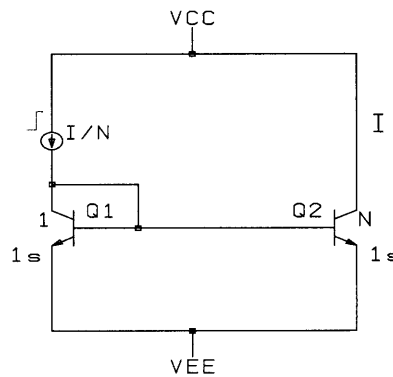


Figure 2.7 Switch current through a current mirror with an area ratio of 1:N.

off. This switching technique is faster than the previous one since it does not saturate transistors. The difficulty with this type of scheme is that the switching is strongly affected by the area ratio of the two transistors. Switching through the current mirror wastes power if the area ratio of the two transistors is 1:1. The current switches quickly when the area ratio is around 1:3 or less, but it will get slower and slower as the area ratio becomes larger. The equation below shows that the total junction capacitance at the base, due to the emitter-base junction depletion capacitance C_{je} (associated with an unit area transistor), is increased linearly with the area ratio N .

$$C_{jtot} = (1 + N) \cdot C_{je} \quad (2.4)$$

and the time needed for charging up the junction capacitance is

$$\Delta t = \frac{C_{jtot} \cdot \Delta V}{\frac{I}{N}} \quad (2.5)$$

where ΔV is approximately one V_{BE} . The switching time, as indicated in (2.5), actually goes with the square of the area ratio N . Figure 2.8 shows that the current switches within 1.7 ns through a current mirror of area ratio of 1:3, whereas in the case of an area ratio of 1:10, it takes almost 10 ns to switch. The transient time constant τ , which is $r_{e1} \cdot C_{jtot}$, also gets bigger as the area ratio increases, and the switching curve of the 1:10 case appears to be less sharp than in the 1:3 case. The total supply current and the number of transistors needed for an $M:1$ switching is listed below

$$I_{tot} = \frac{I}{N} + I \quad (2.6)$$

$$n_{tot} = 2 \cdot M \quad (2.7)$$

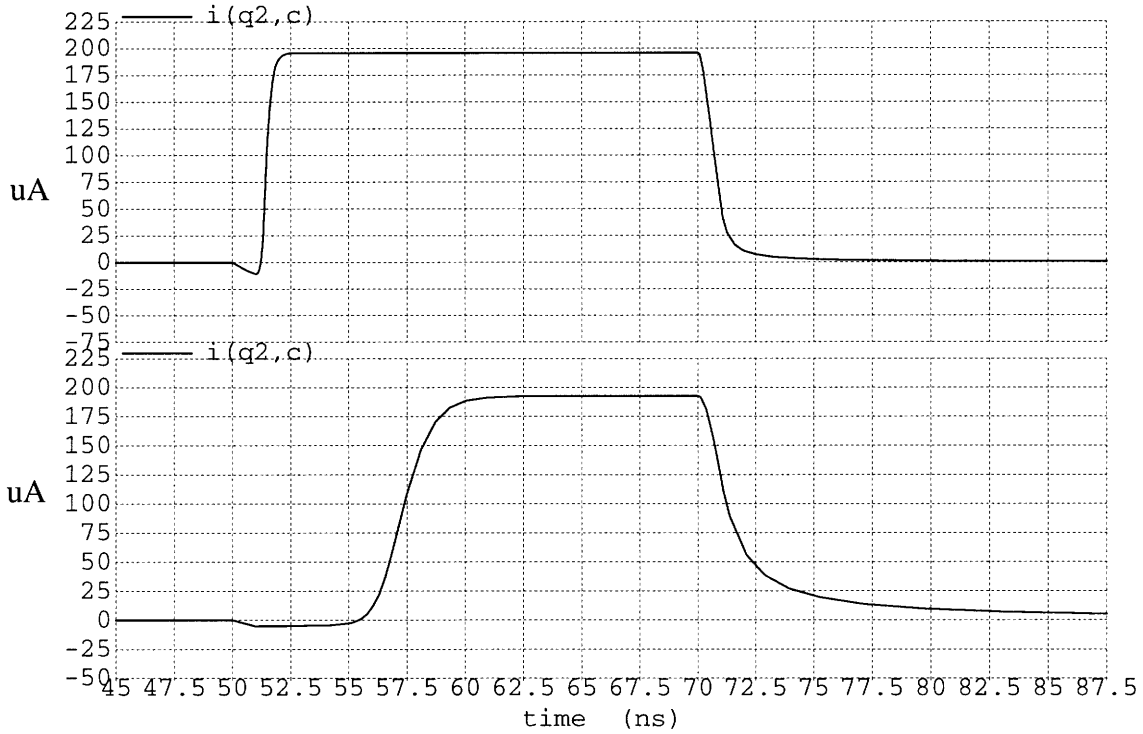


Figure 2.8 Simulated switching transient using current mirror. The first trace is the collector current of Q2 when the area ratio is 1:3, the second trace shows the collector current of Q2 when the area ratio is 1:10.

Figure 2.9 shows a scheme which looks like a combination of the schemes seen both in Figure 2.6 and Figure 2.7. Current I_1 is a controlled current source. Initially, I_1 's level is near zero and the V_{BE} of Q_2 is approximately the same as V_{BE1} , and conducts a current I . When I_1 switches from low to high, the larger voltage drop across R_1 causes V_{BE2} 's level to drop and turns Q_2 off. Replacing a simple wire with transistor Q_5 provides the base current compensation. If the voltage difference between V_{BE1} and $I_1 R_1$ is larger than $V_{CE3,sat}$, the recovery time on Q_3 will be short and the switching time will be fast. However this is not a desirable switching technique since it is not

only expensive in terms of using more devices, but also slow and wasteful for current

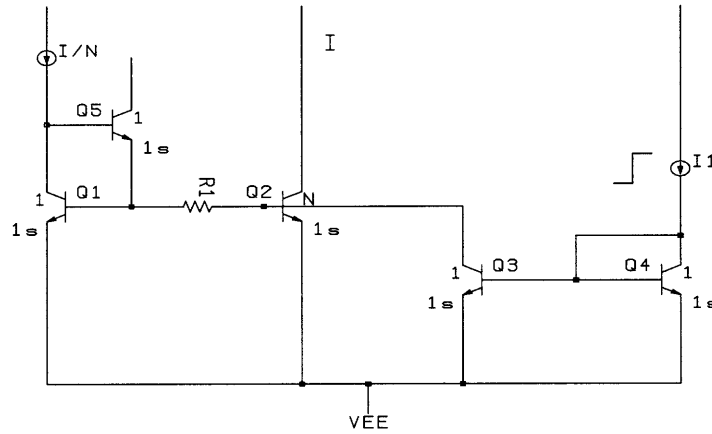


Figure 2.9 Switching scheme B.

switching. Either a high current I_1 or a large resistor R_1 is needed in order to get an adequate voltage drop across R_1 and ensure a fast switching speed. The total supply current and the transistor count for an $M:1$ switching are shown below

$$I_{tot} = \left(\frac{I}{N} + I \right) + (M - 1) \cdot 2I_1 \quad (2.8)$$

$$n_{tot} = 3 \cdot M + 2 \quad (2.9)$$

Finally, an alternative scheme considered is an ECL (emitter-coupled logic) gate as seen in Figure 2.10. Both currents in Q_1 and Q_2 are functions of V_{id} , the difference between V_p and V_n . As shown in Figure 2.11, for input voltage differences of greater than several hundred millivolts, the collector currents become nearly independent of V_{id} since all the current is flowing in one of the transistors [5]. An ECL gate allows the current to be switched quickly and efficiently. Moreover, multi-channel switching can

be implemented easily by adding more transistors to the common emitter node.

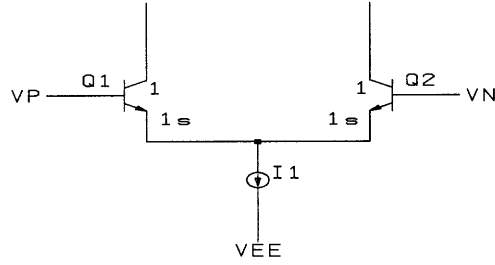


Figure 2.10 Simple emitter-coupled logic (ECL) circuit.

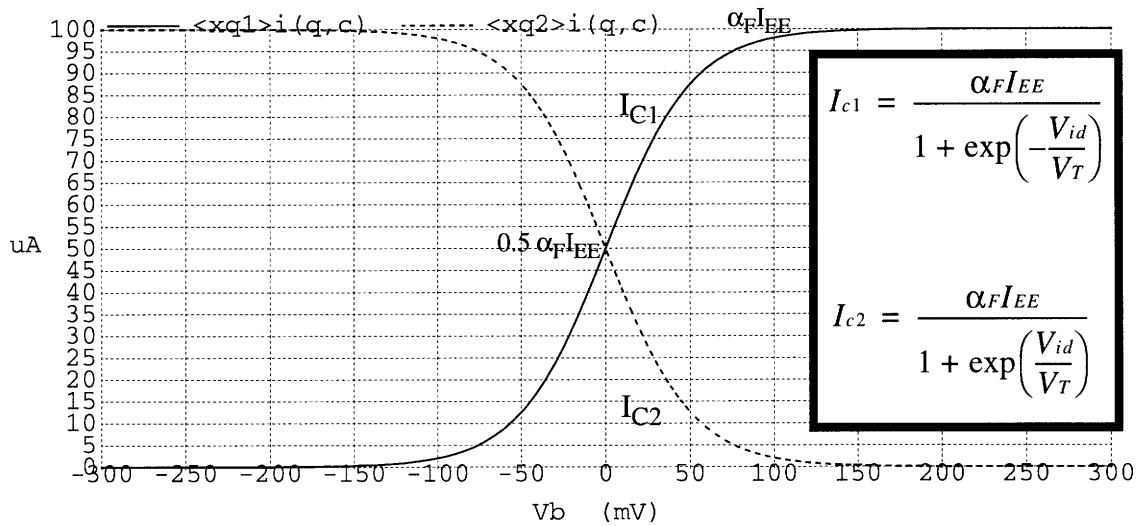


Figure 2.11 Emitter-coupled pair collector current as a function of differential inputs.

The simple ECL circuit leads to the scheme shown in Figure 2.12, where Q_2 and Q_3 form an ECL current switch. Initially, A, B, C and D are tied to V_{EE} , and $Q_3 \sim Q_6$ are off. Transistors Q_1 and Q_2 form a current mirror with an area ratio of 1:1. Transistor Q_2 is on and carries I/N . Each resistor has IR/N mV across it. When A is raised to V_{BE} , $Q_3 + N \cdot (IR/N)$ mV above the negative supply, an $(N-1)IR/N$ mV differential voltage is created between the bases of Q_3 and Q_2 . The current which flowed into Q_2 is quickly shut off. In the meantime, approximately N times Q_1 's collector

current, I , is steered into Q_3 . Transistors $Q_4 \sim Q_6$ conduct no current since their bases are still tied to the V_{EE} . Notice that a resistor, rather than a current source, is used

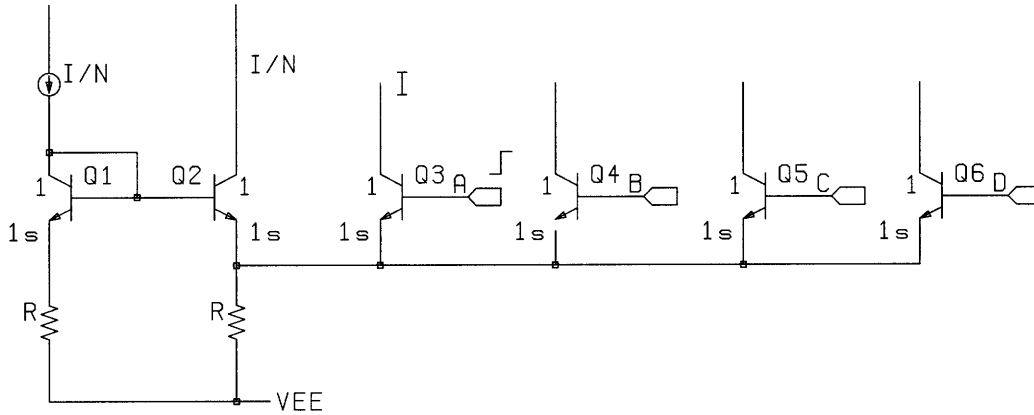


Figure 2.12 Combine current mirror and ECL gates to switch among multi-channels.

between the end of the emitter and the negative rail. This design avoids wasting headroom, since the current source consumes at least one V_{CE} plus a voltage across the emitter degeneration resistor, while a resistor alone consumes much less. This current switch has the same speed and simplicity benefits as an ECL and can be extended to a Single-Pole-X-Throw current switch by expanding the number of emitter-coupled transistors. The total supply current and the number of transistors needed for an $M:1$ switching are shown below. Further study of this switching scheme shows that Q_1 , and Q_2 and Q_1 's emitter degeneration resistor R , are not necessary for the current switch unless Q_2 's collector current can be used for another purpose, such as disabling the switch.

$$I_{tot} = I + \frac{2 \cdot I}{N} \quad (2.10)$$

$$n_{tot} = M + 2 \quad (2.11)$$

Other existing switching techniques for multi-channel switching using ECL gates

are also considered. Figure 2.13 shows a scheme which uses stacked ECL gates to select the current. This is a fast and efficient design, but it cannot be used here, since it alone consumes at least three V_{CE} 's (above 600 mV) of headroom in doing the 4:1 switching.

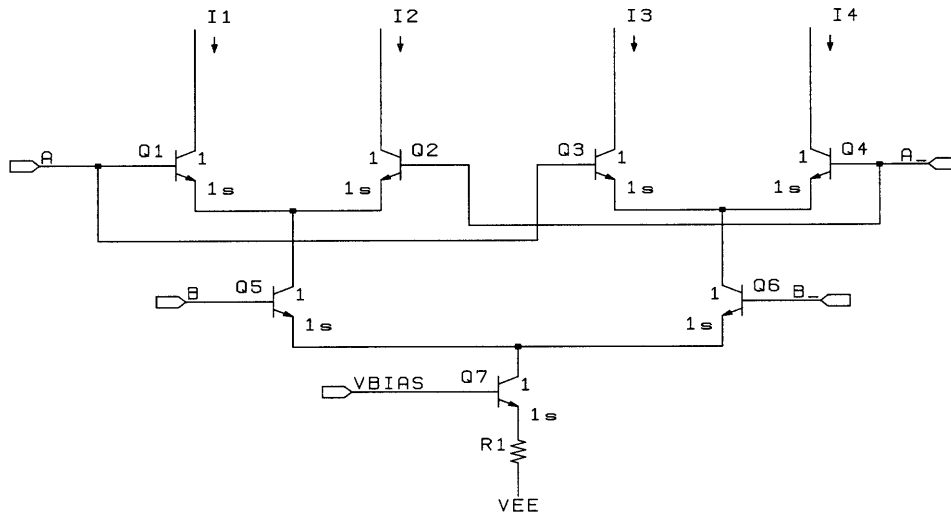


Figure 2.13 Stacked ECL gates.

Ideally, an ECL gate should have a switching delay close to $1/2\pi f_T$. However, Figure 2.14 shows that a major delay will result if we consider the parasitic capacitance in the circuit. According to the following equation:

$$\Delta t = \frac{C}{I} \cdot \Delta V \quad (2.12)$$

With a given C and I , the greater the change in voltage across the capacitor, the longer the switching time will be. In Figure 2.14, the voltage across the capacitor swings from 1.4V to 4.4V, a change of 3V, when V_3 switches from low to high making the base of Q_1 swing 5 V. The computer simulation results are attached in Figure 2.15 to show this delay. By keeping the voltage swings in the ECL small, the size of the stored charge is correspondingly smaller. Further experimentation indicates that the currents switch fairly rapidly and cleanly when the differential voltage between the base of Q_1 and the

base of Q_2 is around 200mV. If the differential voltage is much higher than this value, the transient delay will increase; if the differential voltage is more than 100mV lower than this value, then the current switching will not be complete.

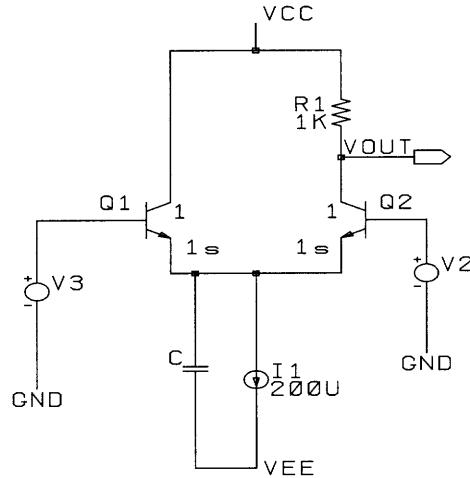


Figure 2.14 Emitter-coupled pair with emitter capacitance.

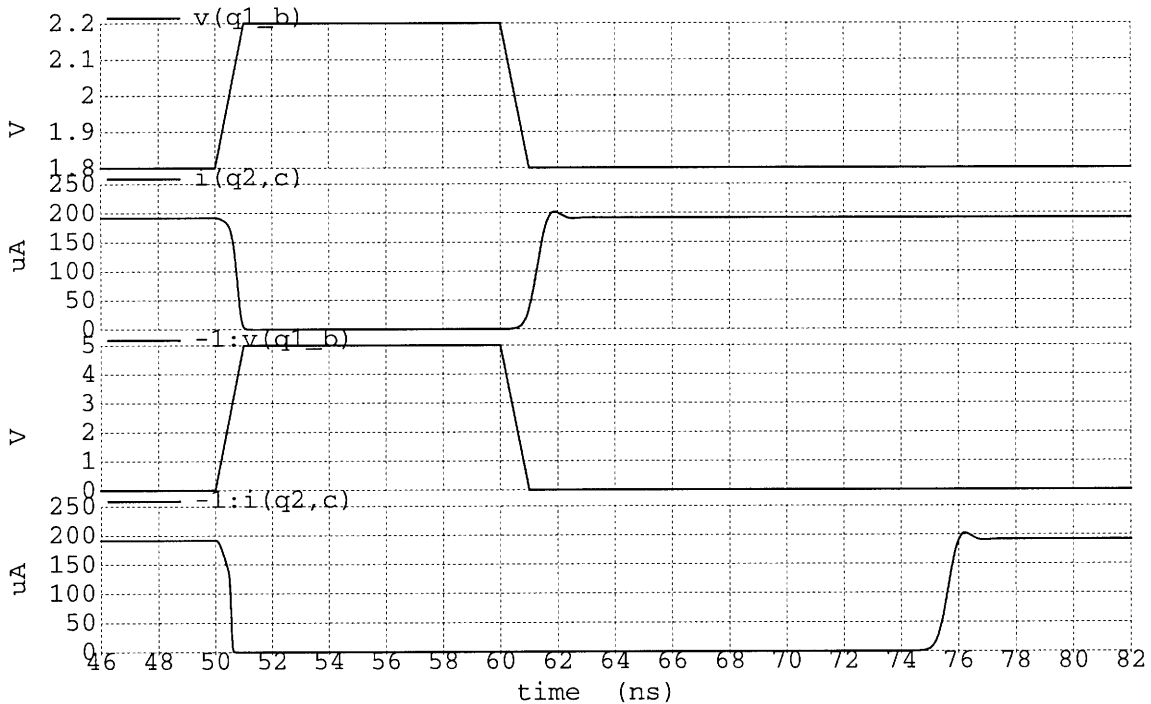


Figure 2.15 Switching speed variations due to the parasitic capacitance and the differential voltage size. The top trace shows a step changes of 400 mV on V_3 , and the second trace shows the output voltage transient due to this change; the third trace shows a step change of 5 V on V_3 , and the bottom trace indicates that the output voltage transient experiences a major delay due to this large change of voltage.

Based on the previous studies, a suitable switching scheme has been identified. The decoder of the 4:1 video multiplexer will use the switching technique that is similar to the one shown in Figure 2.12. Since this decoder sources rather than sinks current into the multiplexer's input stage, NPN transistors in Figure 2.12 will be replaced by PNP transistors. Also, in order to maintain the ECL gate's switching speed, the differential voltage swing is kept to within several hundred millivolts for the ECL gates governing the current steered into the input stage. The voltages across the two resistors are also held to about 400 mV to allow large input headroom.

3.0 Circuit Descriptions

3.1 Multiplexer Block Diagram

Figure 3.1 shows the block diagram of the 4:1 switched transconductance voltage feedback multiplexer. It is composed of four major parts: the current mode decoder cell (NMDF1), the four copies of the folded cascode input cell (INPTNEW), the common bias cell (NBIAS), and the common output amplifier cell (NMAIN). Among the fourteen pins of the multiplexer, four are positive input pins (VINP0 ~ VINP3) separated by ground pins (GND's) to avoid the coupling of the inputs in the lead frame; the negative input terminals of all four input cells are tied to a common negative input pin (VINN) so that the number of pinouts is reduced by three; the rest of the pins are assigned to the positive power supply (VCC), the negative power supply (VEE), the channel-select logic inputs (A0 and A1), the active-low disable input (DIS₋), and the common output (VOUT).

The circuit operation is as follows. When DIS₋ is held high, the chip is enabled. Depending on the voltage levels of the logic inputs, the decoder steers a fixed current into one of the four transconductance input stages. The signal at the positive terminal of this selected input cell is amplified through the output amplifier by an amount determined by the feedback configuration from the output to the common negative input. Bringing the DIS₋ low reduces the supply current for the amplifier and turns the output of the amplifier into a high impedance. In disable mode, signals applied to A0 and A1 have no effect on the operation. The following sections describes the detailed circuit structure and the operational principle of each cell.

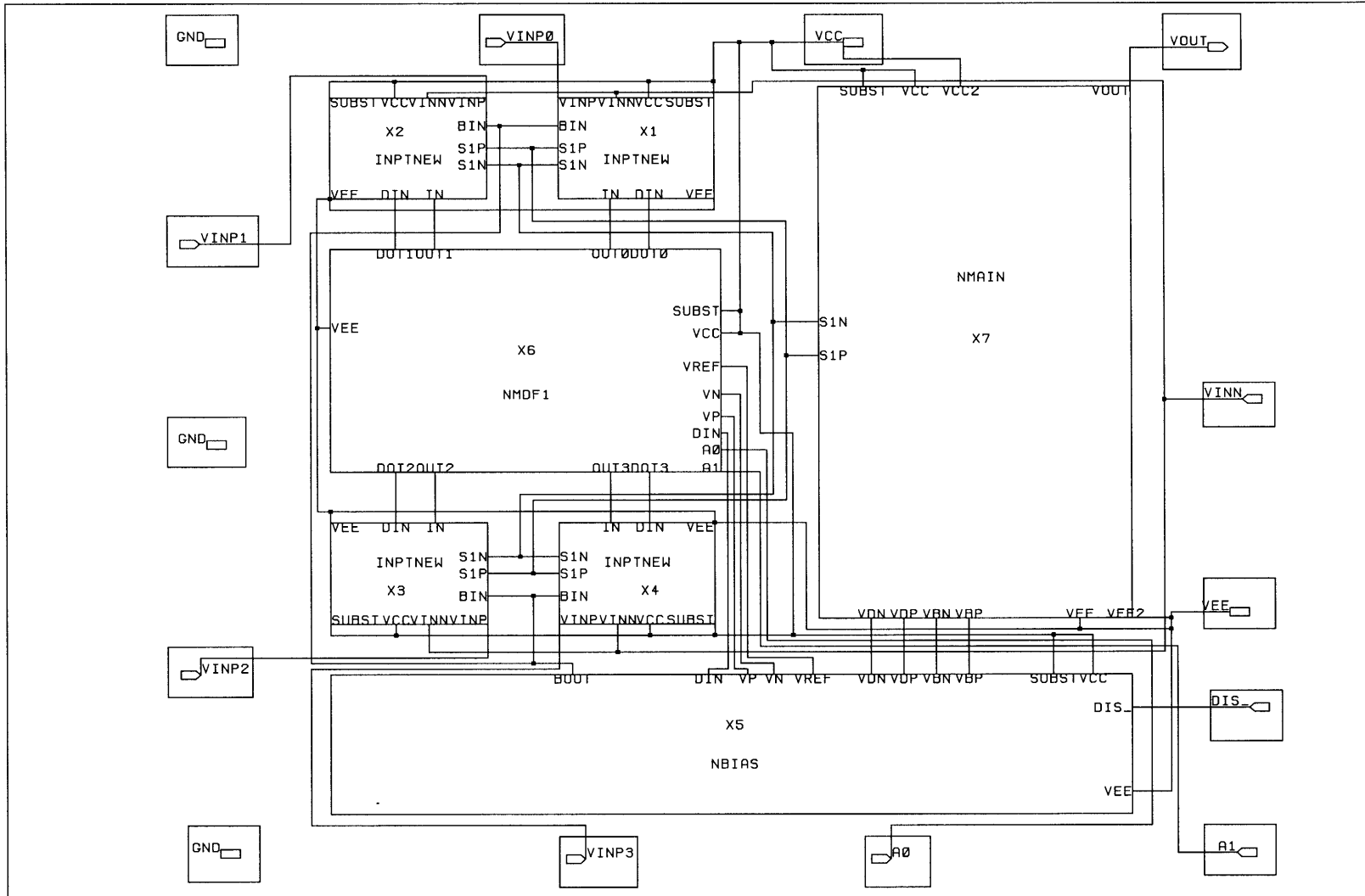


Figure 3.1 The actual block diagram of 4:1 video MUX chip.

3.2 The Biasing Cell

Figure 3.2 shows the circuit diagram of the biasing cell of the 4:1 video multiplexer. Some similarities exist between this biasing cell and that of the AD8041 seen in Figure 2.5. Like the AD8041, R_{36} , Q_{63} and Q_{58} form a start-up circuit, and a PTAT (positively proportional to absolute temperature) current is set by Q_{44} , Q_{61} , Q_{42} , and R_{31} . A CTAT (negatively proportional to absolute temperature) current is created by the lower emitter of Q_1 in combination with R_{33} , R_{37} , and R_{38} . The collector current of Q_1 adds together both CTAT and PTAT currents to create an NPO current which is temperature independent to the first order. This current is then mirrored and supplied to the rest of the circuit by Q_{65} . Current mirrors of this biasing cell all have their emitters degenerated as in the AD8041, because the current of a highly degenerated current mirror ($R_E * I_E > 4V_T \sim 100 \text{ mV}$) is determined primarily by resistor ratios rather than by the ratios of the emitter area, which may be subject to matching problems. Setting the current ratios using emitter degeneration also allows transistors to have a smaller geometry, resulting in lower C_u and higher output impedance. Finally, all of the current sources' base currents are compensated in a fashion similar to that of AD8041 by connecting to transistors such as Q_{12} before they are mirrored out, so that the accuracy of the supplied current is maintained.

As Section 2.3 points out, the disable function of the AD8041 saturates many transistors and is very slow. The disable circuit has been redesigned for the new biasing cell, and many other new features, such as a logic reference voltage and two extra reference voltages, have been added to help the multiplexer to achieve the desired performance. This section provides detailed descriptions of these new designs.

Designing a decoder and a disable circuit involves constructing a temperature independent logic reference voltage and developing a fast and efficient switching scheme. A desirable logic reference voltage must be set at a fairly constant level, which will not be affected by a change of temperature. Figure 3.2 shows the circuitry that generates a reference voltage V_{REF} with a low temperature coefficient. Transistor Q_6 mirrors an NPO current into the band-gap-referenced biasing circuit that supplies both Q_7 's base current and Q_{11} 's collector current. The V_{REF} is the sum of the voltage drops across R_3 and the V_{BE} of Q_{11} . Since the collector current can be written as

$$i_C = I_S e^{(qV_{BE})/(kT)} = AT^3 e^{(qV_{go})/(kT)} e^{(qV_{BE})/(kT)} = AT^3 e^{(q(V_{BE} - V_{go}))/(kT)} \quad (3.1)$$

where A is a constant that depends on transistor type and geometry, q is the charge on an electron, k is Boltzmann's constant, T is the temperature, and V_{go} is the width of the energy gap extrapolated to absolute zero divided by the electron charge [6]. Solving Eqn. 3.1 for V_{BE} yields

$$V_{BE} = \frac{kT}{q} \ln \frac{i_C}{AT^3} + V_{go} \quad (3.2)$$

The partial derivative of V_{BE} with respect to temperature at constant i_C is

$$\frac{\partial}{\partial T} V_{BE} = \frac{k}{q} \ln \frac{i_C}{AT^3} - \frac{3k}{q} = \frac{V_{BE} - V_{go}}{T} - \frac{3k}{q} \quad (3.3)$$

The quantity $(V_{BE} - V_{go})/T$ is $-1.5 \text{ mV}/^\circ\text{C}$ at $T = 300 \text{ K}$ for the typical V_{BE} value of 0.7 V in XF1.5 process. As Figure 3.2 shows, the current of R_3 , decided by the Widlar current source, is PTAT. By choosing the values of R_3 , R_4 and R_2 and the area ratio

SUBST □

Biasing Cell

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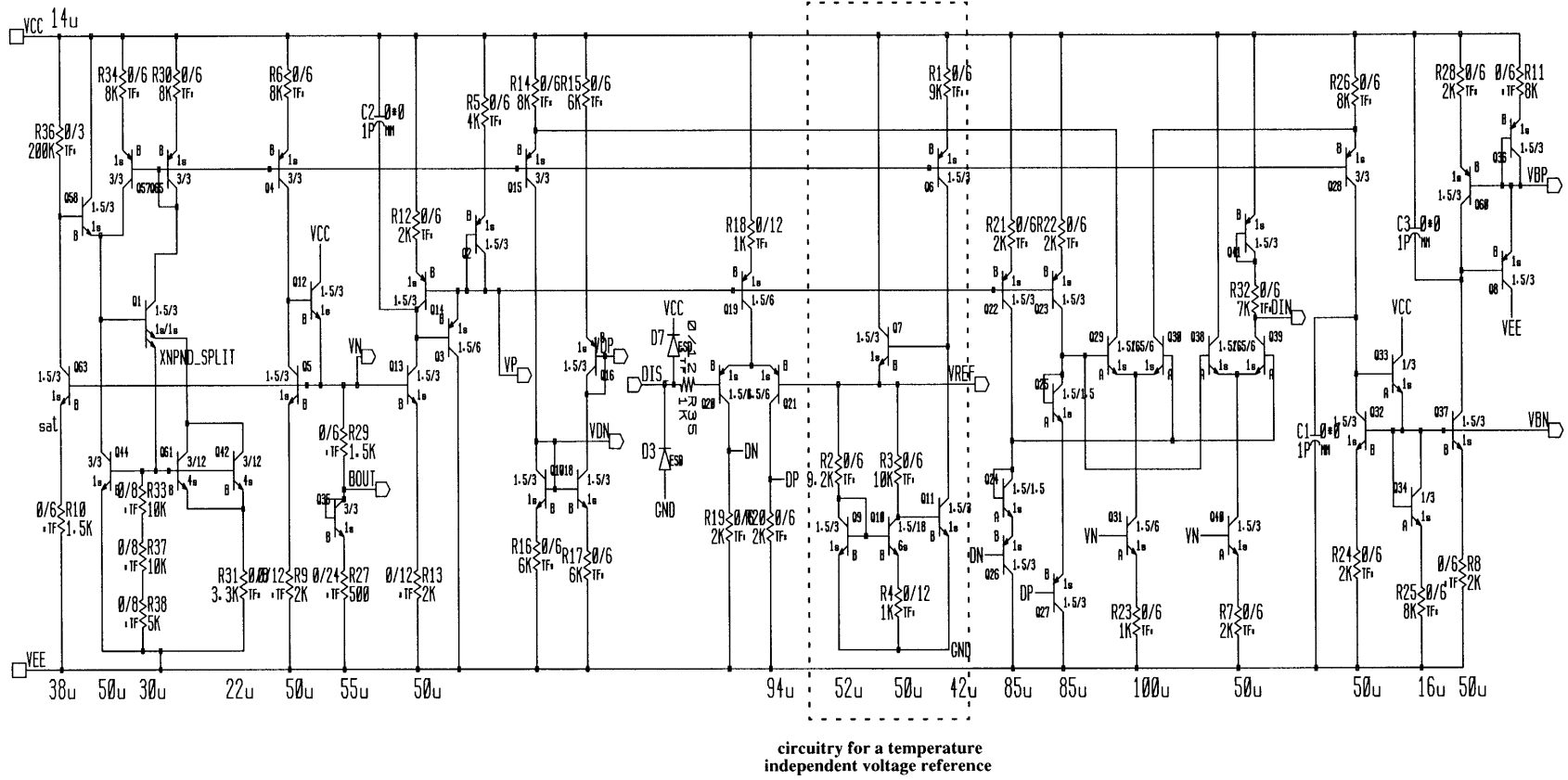


Figure 3.2 Biasing cell schematic.

of Q_{10} to Q_9 as shown in the circuit, V_{REF} is set to be nominally 1.27V above ground at room temperature and has a temperature coefficient of 30 $\mu\text{V}/^\circ\text{C}$. This reference voltage level is ready for a low power application, such as 5 V TTL, and 3 V or 5 V CMOS. Note that a TTL threshold voltage also changes with temperature. Figure 3.3 plots the simulated temperature dependence of V_{REF} and other biasing current levels of the multiplexer using nominal models. It shows that V_{REF} varies only 7 mV in the temperature range of -50°C to 150°C . Since V_{REF} is only a logic reference, rather than a precise one, a 7 mV variation is a satisfactory result. If on the other hand this reference voltage is set by only two diode-connected transistors, its voltage level will still be approximately 1.3 V at the room temperature, although in the range of -50°C to 150°C the voltage will change by almost 600 mV, rather than by just 7 mV. Setting V_{REF} at a higher level involves using three V_{BE} 's or one V_{BE} and a much larger resistor and a higher power. These alternatives are impractical since they will result in a voltage variation much greater than 7 mV, and the big resistor will require a large area.

The biasing of the output amplifier is separated from the biasing of the rest of the logic circuits of the multiplexer to prevent the disturbance of the amplifier by the logic circuitry. As in Figure 3.2, V_{BP} and V_{BN} are two biasing voltages for temperature independent NPN and PNP analog current sources of the output amplifier while V_P and V_N are two biasing voltages for the decoder and the disable circuit. Among the rest of the input and output terminals of the biasing cell, $DIS_$ serves as the logic input to the disable circuit; $BOUT$ provides a sloppy reference voltage for all of the four input stages (Section 3.4 explains its function); DIN connects to the decoder and helps to turn off the input stages when the multiplexer is disabled; V_{DP} and V_{DN} connect to the output

amplifier and switch to about 1 V below the positive supply and 1 V above the negative supply, respectively, to disable the amplifier.

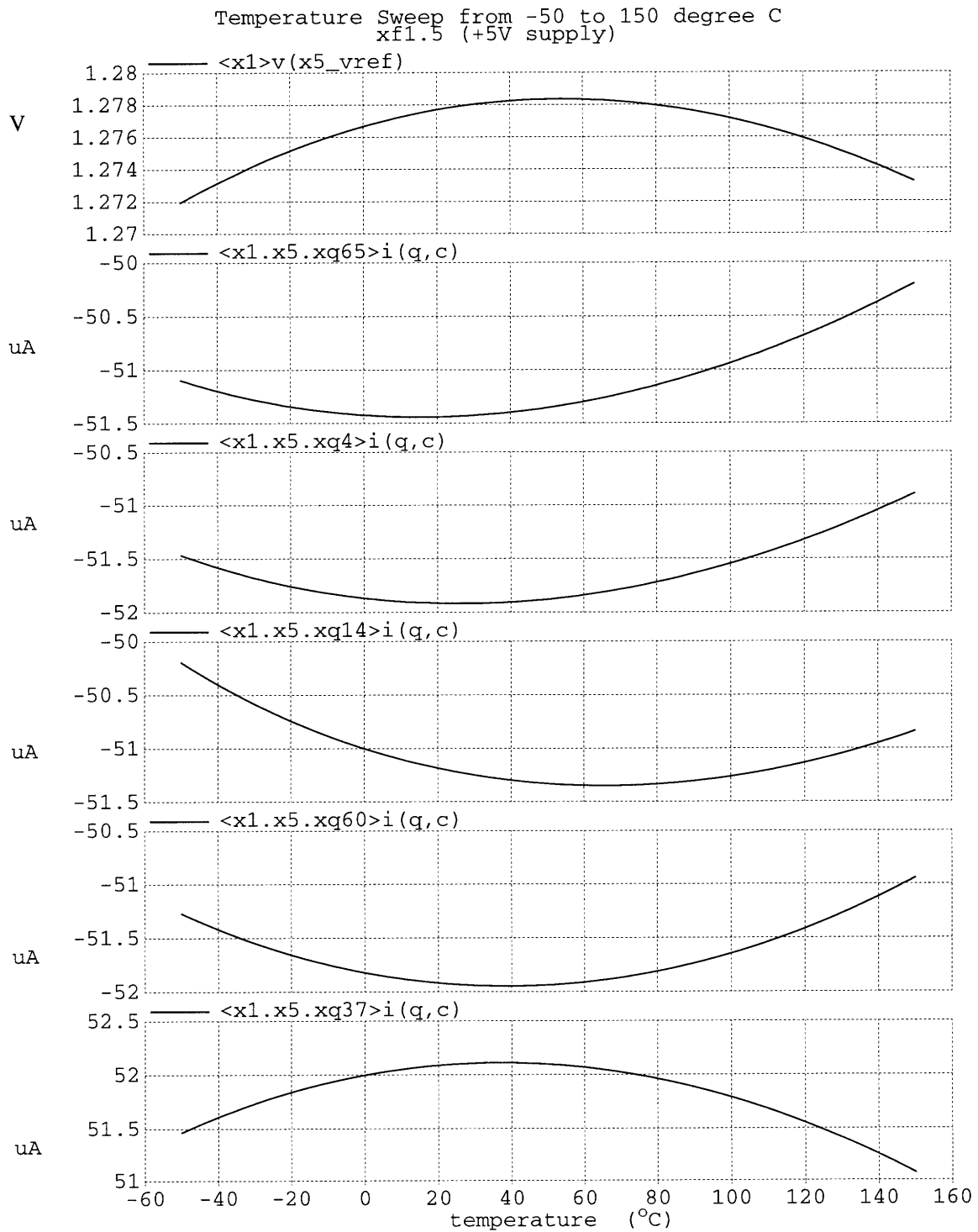


Figure 3.3 Vref and other biasing currents change with temperature.

Referring again to Figure 3.2, the disable circuit operation can be explained as follows. When $DIS_$ is held high, the multiplexer is enabled. The PNP transistor Q_{21} of the ECL gate conducts current and keeps node DP 200 mV above node DN. Their voltage levels are both shifted up by two V_{BE} 's through transistors Q_{25}/Q_{27} and Q_{24}/Q_{26} so that current sources Q_{31} and Q_{40} will not be saturated. The resulting voltages are applied to the correspondent terminals of the ECL gates formed by Q_{29}/Q_{30} and Q_{38}/Q_{39} . The 200 mV differential voltage will cause all of the currents supplied by Q_{31} and Q_{40} to flow through Q_{29} and Q_{38} , and nearly no current to flow in Q_{30} and Q_{39} . On one hand, Q_{29} 's 100 μ A collector current flows through R_{14} , dragging the emitter voltage of Q_{15} down by 400 mV and putting it in cutoff. Without an active current source, VDP and VDN are driven close to the supply rails (due to leakage current, they are about 500 mV from their respective supply rails). On the other hand, raising $DIS_$ also raises DIN close to the positive supply rail and enables all the input stages. Since no current flows in Q_{30} , current source Q_{28} will be in normal operation so that VBN and VBP supply the correct biasing reference voltage to the output amplifier, keeping it enabled.

To disable the multiplexer, $DIS_$ is driven to a voltage that is lower than the logic reference voltage V_{REF} (1.27 V). This time Q_{20} conducts, and DN is lifted 200 mV higher than DP. This differential voltage causes the ECL gates formed by Q_{29}/Q_{30} and Q_{38}/Q_{39} to tilt in the other direction letting Q_{30} and Q_{39} conduct currents. Since there is no current in Q_{29} , Q_{15} will turn on and supply current to Q_{17} to make the voltage VDN. This current is then mirrored through Q_{18} to set the voltage level on VDP. Current source Q_{28} is put in cutoff in a fashion similar to Q_{15} of the enable case.

This results in driving VBN and VBP close to the supply rails and disabling the output amplifier. The voltage developed across R_{32} and Q_{41} (DIN) is used to disable all input stages of the multiplexer.

Two 1 pF capacitors C_1 and C_2 are added to both the amplifier circuit's biasing and the logic circuit's biasing respectively. Capacitor C_1 is connected to the negative supply from Q_{32} 's collector, and C_2 is connected to the positive supply from the collector of Q_{14} . This helps to stabilize the feedback bias circuits. In the case where the power supplies are disturbed, those capacitors will help the appropriate collectors track the variations on the supplies and maintain the correct biasing level.

3.3 The Decoder Cell

Figure 3.4 shows the logic flow of the decoder. This current mode decoder can quickly select one of four transconductance input stages and steer a fixed current into the selected stage. As discussed in section 2.4, the desired switching scheme for the decoder design is ECL gates. The voltage swing in an ECL gate is considerably smaller

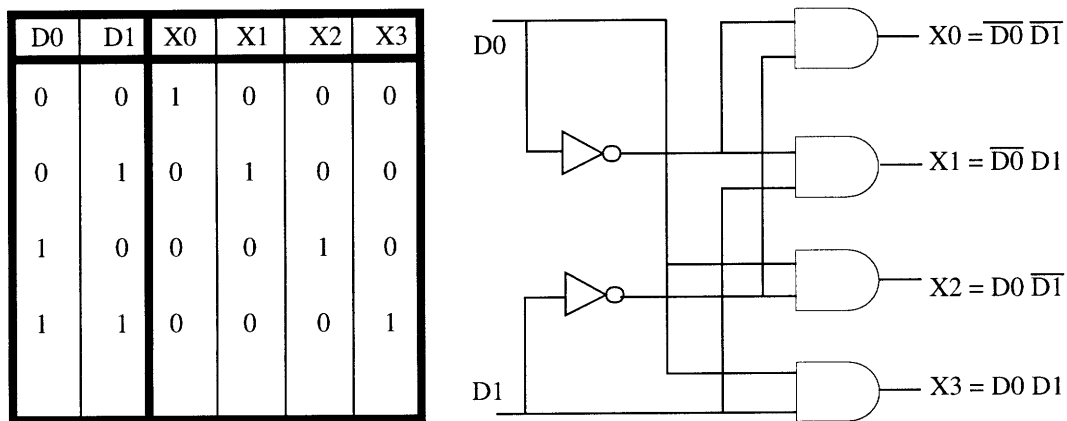


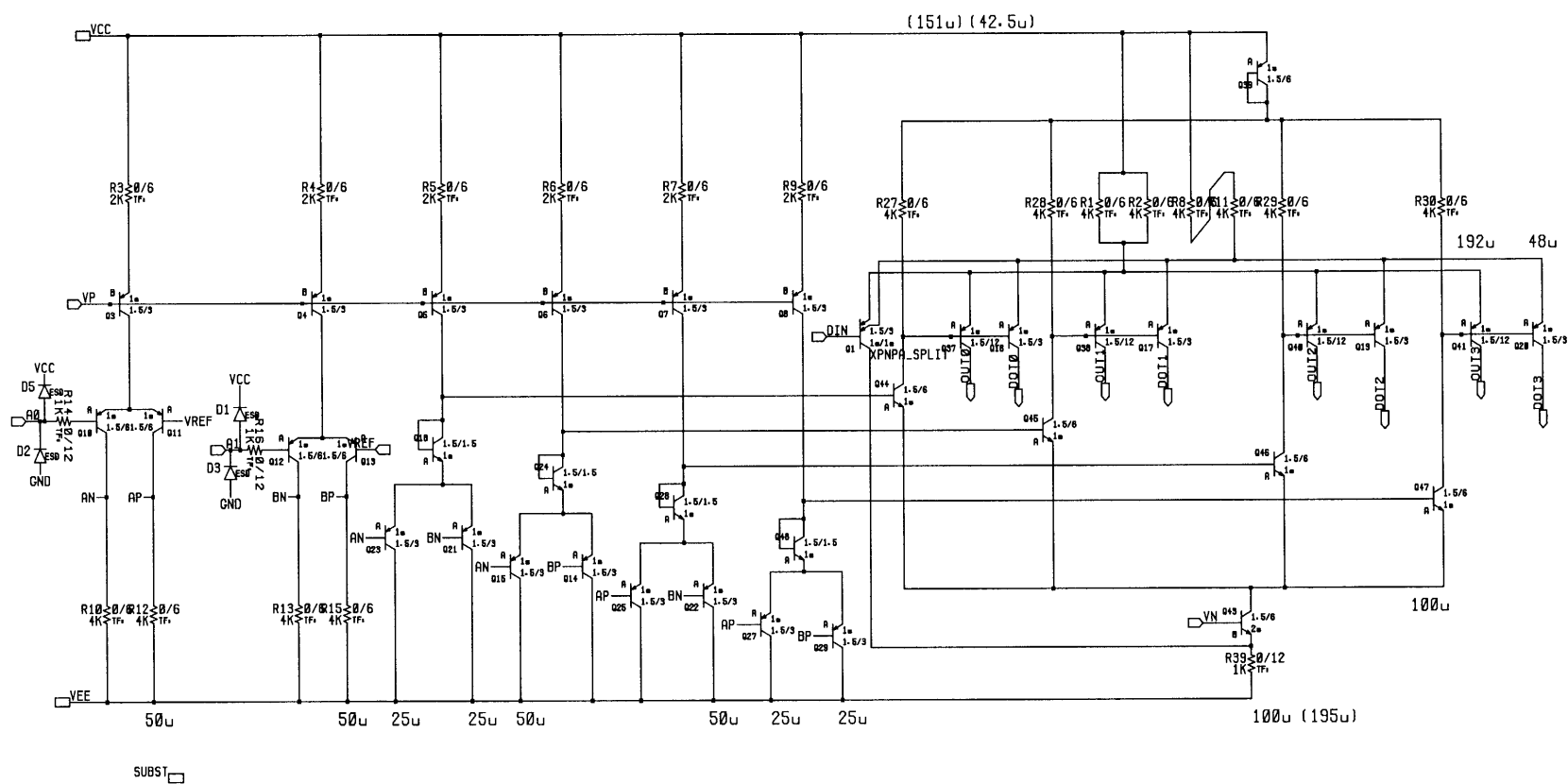
Figure 3.4 Decoder's truth table and logic diagram.

than it is for the other logic gates, and the transfer characteristic is sharper. To create a multiple-input ECL gate, one can add more input transistors to the common emitter node. A single stage can produce both inverted and noninverted outputs. The trade-off between power consumption and switching speed is taken into consideration throughout the decoder design.

As shown in Figure 3.5, the decoder circuit of the 4:1 video multiplexer has two logic input terminals, A0 and A1, which are directly accessible to the user. Among the rest of the input and output terminals, DIN is a disable input that is controlled by the disable circuit in the biasing cell (see Figure 3.2); VREF is the logic reference voltage that is generated by the band-gap-reference circuit in the biasing cell; VP and VN also come from the biasing cell providing biasing voltages for the logic circuit; OUT0 ~ OUT3 are connected to four input stages respectively, and the selected one will provide a fixed current of 192 uA into a selected input stage; DOT0 ~DOT3 are also connected to the input stages, and the selected one will supply 48 uA of current to the selected input stage (detailed descriptions on their functionality can be found in Section 3.4).

The decoder circuit is composed of four groups of ECL gates. The first group consists of two ECL gates formed by PNP transistor pairs Q_{10}/Q_{11} and Q_{12}/Q_{13} . The bases of Q_{11} and Q_{13} are connected to VREF. The bases of Q_{10} and Q_{12} are connected to logic inputs A0 and A1, respectively. Voltage levels at A0 and A1 are compared with the reference voltage VREF. As an example, assuming that A0 and A1 are both logically 1 (eg. voltage levels are at positive supply), currents generated by Q_3 and Q_4 will be steered into Q_{11} and Q_{13} . There will be almost no current flowing into Q_{10} and Q_{12} . Complementary voltages AN/AP and BN/BP are generated. Both AP and BP will

Decoder Cell



have voltage levels of 200 mV above those of AN and BN. Since no current is flowing in either R_{10} nor R_{13} , both AN and BN will be at voltage levels close to the negative supply. Using 200 mV swings at the collectors of Q_{10} and Q_{12} prevents saturating these devices when A0 and A1 are at 0 V and the multiplexer is on a single supply ($V_{EE} = \text{GND}$). The first group of ECL gates buffers the input logic voltages and limits the swings of the internal nodes.

The combinations of AN/AP and BN/BP are handled by the second group of four AND gates formed by PNP transistor pairs Q_{23}/Q_{21} , Q_{15}/Q_{14} , Q_{25}/Q_{22} , and Q_{27}/Q_{29} . These AND gates perform the actual 2:4 decoding. Diodes Q_{18} , Q_{24} , Q_{28} and Q_{48} are used to raise the common-mode levels at the bases of $Q_{44} \sim Q_{47}$ to prevent Q_{43} from being saturated.

The third group of ECL gates consists of four NPN transistors $Q_{44} \sim Q_{47}$. They take the level shifted new voltages from the second group of ECL gates as their inputs and decide which transistor will take over Q_{43} 's collector current. This group of ECL gates is also integrated with the fourth group of ECL gates whose topology is similar to the circuit technique shown in Figure 2.12. This last group forms a direct interface between the decoder and the input stages. It consists of a PNP double-emitter device Q_1 ; the two emitters are joined by two groups of PNP transistors -- $Q_{37}/Q_{38}/Q_{40}/Q_{41}$ and $Q_{16}/Q_{17}/Q_{19}/Q_{20}$. Transistors from each group are also paired as Q_{37}/Q_{16} , Q_{38}/Q_{17} , Q_{40}/Q_{19} , and Q_{41}/Q_{20} , so that each pair of transistors can share a common base voltage supplied by the third group of ECL gates. This base voltage is set by a diode connected PNP transistor Q_{39} and one of the four resistors $R_{27} \sim R_{30}$. In our example, Q_{43} 's collector current will flow through Q_{47} since the base voltage of Q_{47} is the highest of

the four transistors. As a result, there will be an approximately 400 mV voltage drop across R_{30} and one V_{BE} drop across Q_{39} . There will be almost no voltage drop across the other three resistors ($R_{27} \sim R_{29}$). Notice that Q_1 's base is tied to DIN, which is generated from the biasing stage and sits close to the positive supply unless the circuit is disabled. Since the PNP transistor pair's (Q_{41}/Q_{20}) base voltage level is about 600 mV lower than DIN and 400 mV lower than other transistor pairs (Q_{37}/Q_{16} , Q_{38}/Q_{17} and Q_{40}/Q_{19}), Q_{41} and Q_{20} will conduct currents and source them to select a desired input channel.

The simplified drawing seen in Figure 3.6 shows that Q_{41} and Q_{20} actually acquire their collector currents through a structure that is similar to a current mirror. The equation below shows the relationship between the collector current of Q_{41} and other circuit parameters.

$$V_T \cdot \ln \frac{I_{C39}}{I_{S39}} + I_{C39} \cdot R_{30} = V_T \cdot \ln \frac{I_{C41}}{I_{S41}} + I_{C41} \cdot R_1 \parallel R_2 \quad (3.4)$$

where I_{C39} and I_{C41} are collector currents of Q_{39} and Q_{41} , I_{S39} and I_{S41} are the saturation currents of Q_{39} and Q_{41} , V_T is the thermal voltage. Since I_{S39} and I_{S41} are directly proportional to the area of Q_{39} and Q_{41} , making Q_{41} twice as large as Q_{39} and keeping the value of R_1/R_2 half of R_{30} , Q_{41} can mirror 192 uA of current (not 200 uA because of the α loss from emitter current to collector current). A similar concept also applies to Q_{20} .

Voltage DIN is applied to the base of the double-emitter PNP transistor Q_1 to help turn off the input stages and save power when the multiplexer is disabled. As discussed in Section 3.2, DIN is raised close to the positive supply rail when the circuit

is enabled. Its voltage level is sufficiently high that we can ignore its existence in the fourth group of ECL gates while the multiplexer is enabled. However, when the multiplexer's disable input is selected, DIN will be more than one volt below the positive supply, and become the lowest input among those of the fourth group of ECL gates. This voltage enables Q_1 to have a collector current of more than 195 μA , which is approximately the sum of its two emitter currents. This current flows into R_{39} . Current through R_{39} increases, raising the voltage on the emitter node of Q_{43} . This causes Q_{43} to turn off so that the decoder can save power, rather than wasting the collector current of Q_1 .

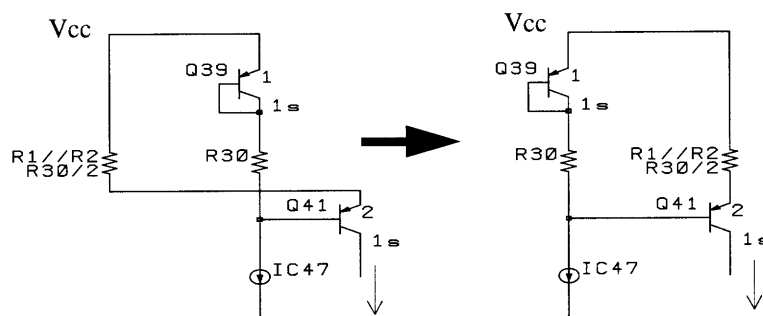


Figure 3.6 A simplified equivalent circuit showing the decoder topology.

Two design questions drew the author's attention -- how much more input headroom the decoder consumes, and how the decoder affects the channel crosstalk. These questions are related; a trade-off has to be made between them during the design. The original AD8041 input stage has a resistor of 130 Ω at the current location of R_1/R_2 (or R_8/R_{11}) and it consumes about 25 mV of headroom. Even though a carefully selected switching scheme is employed in the decoder design, the original headroom is still lowered by almost 400 mV. This is due to the replacement of the previous 130 Ω resistor

with a 2 K Ω resistor (R_1/R_2). A 2 K Ω resistor is used here because it has to maintain an 1:2 relationship with $R_{27}/R_{28}/R_{29}/R_{30}$, which are all 4 K Ω resistors (equation 3.1), so that the current sourced out of the decoder will be 192 μ A. Using a smaller resistance value for $R_{27} \sim R_{30}$ will increase the leakage currents flowing into the unselected input stages. This causes the gm's of the unselected input stages to be not negligible and worsens the DC channel crosstalk. Increasing those resistor values will lessen the leakage current, but more input headroom will be wasted. There is one advantage; as discussed in Section 3.2, more emitter degeneration (400 mV vs. 25 mV) will make transistors such as Q_{37} better current sources.

3.4 The Input Cells

The 4:1 video multiplexer contains four identical transconductance input cells. The input cell is designed to minimize the inter-channel crosstalk and maximize the off isolation. During the design process, two versions of this cell are investigated. The first part of this section analyzes the trade-off of these two versions of the design. This is followed, in the second part, by a discussion of the schematic of the actual input cell.

The first version of the input cell design, seen in Figure 3.7 is similar to the PNP differential pair of the AD8041 folded cascode input stage (Figure 2.2). The non-inverting terminal V_{INP} is the input to the cell and V_{IN} is the inverting feedback terminal. Terminal IN is the tail current input terminal of the cell and is connected to a corresponding current output terminal (OUT_0 , OUT_1 , OUT_2 , or OUT_3) of the decoder. Terminal FD_0 and FD_1 are the current output terminals of the input cell, feeding dif-

ferential currents to the other half of the folded cascode stage in the amplifier.

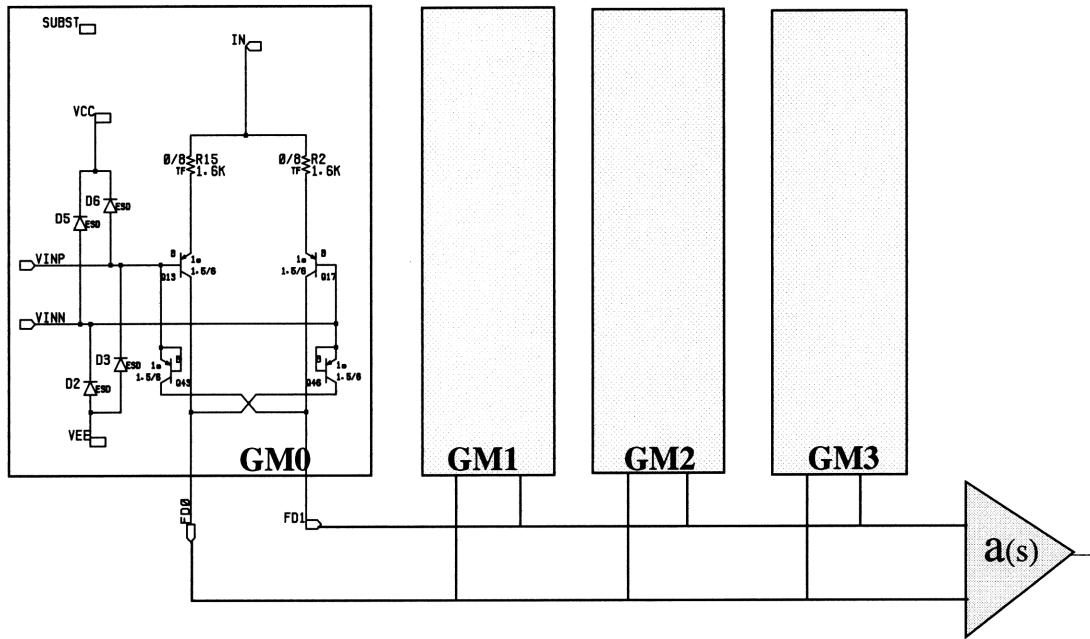


Figure 3.7 The first version of input stage design.

One component of the crosstalk can be modeled using the following equation:

$$Crosstalk = \frac{Ym(off)}{gm(on)} = \frac{(Cu_{13} - Cu_{43}) \cdot s + \frac{q \cdot Ic_{13(off)}}{k \cdot T}}{\frac{gm_{13}}{gm_{13} \cdot R_{15} + 1}} = R_{15} \cdot gm_{13(off)} \cdot \left(\frac{(Cu_{13} - Cu_{43}) \cdot s}{gm_{13(off)}} + 1 \right)$$

where C_{u13} and C_{u43} are the collector-base junction capacitances of Q_{13} and Q_{43} respectively, s is $j\omega$, V_T is the thermal voltage, $I_{c13(off)}$ is the leakage collector current of Q_{13} when this input channel is unselected, g_{m13} is the value of the transconductance of Q_{13} of the selected input channel, and $g_{m13} / (g_{m13} R_{15} + 1)$ is approximately $1 / R_{15}$. If Q_{13} and Q_{43} are perfectly matched, the difference between C_{u13} and C_{u43} will be zero. For a leakage current of 2 pA, the crosstalk is calculated to be -188 dB and

independent of frequency (the all-hostile crosstalk will be $-188\text{dB} + 20\log 3$, which is -178.5dB). However, the computer simulation seen in Figure 3.8 shows that the crosstalk is not only frequency dependent, but also C_u -matching dependent. The first trace in Figure 3.8 shows an inconsistency with the previous ideal-case hand-calculation (-80dB vs. -178dB at 10MHz) due to parasitic capacitances such as C_{cs} and C_{je} . The second trace shows the mismatch among Q_{13} , Q_{43} , Q_{17} , and Q_{46} by 6fF in the input stage will significantly worsen the crosstalk performance by almost 28dB at 10MHz . Because of parasitic capacitances due to wiring and capacitor-mismatching, high-pass conduction paths will exist among unselected inputs or between the unselected inputs and the output. It is true that a careful layout can reduce the coupling due to wiring parasitics although it will not entirely eliminate it; however, as shown in the rest of this section, the capacitor-mismatching dependence can be eliminated if an alternative design is used.

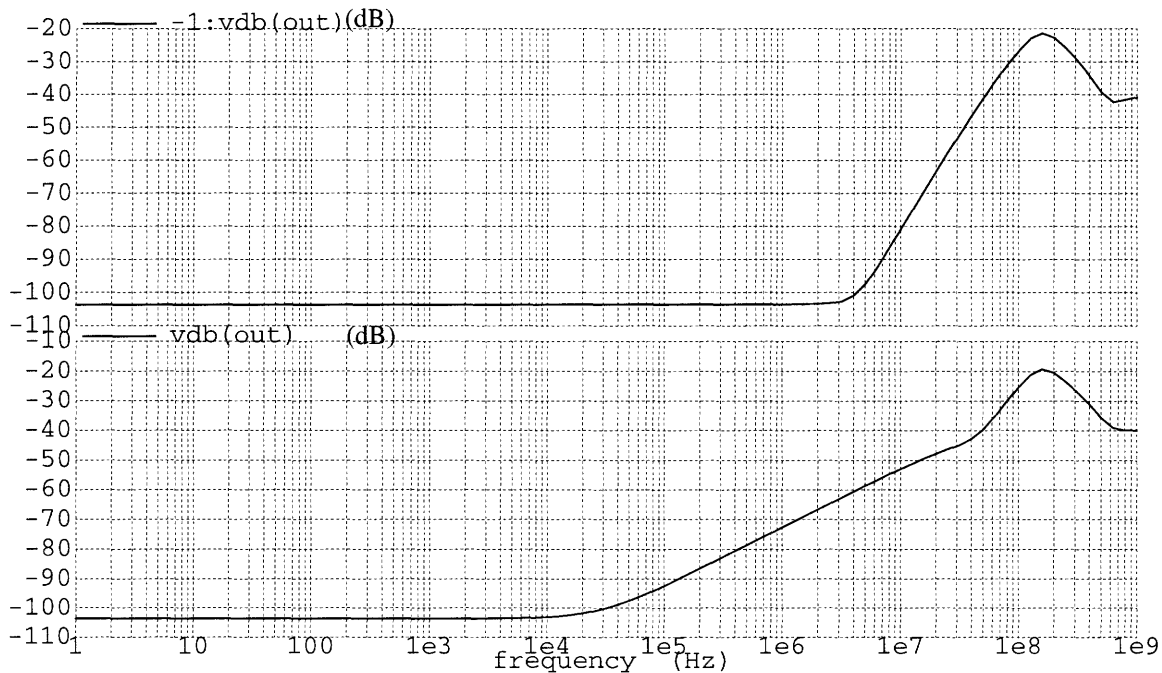


Figure 3.8 All-hostile crosstalk from the first version of the input cell design. The top trace represents the perfectly matching condition of the input transistors. The bottom trace shows the 6fF mismatch.

The second version of the input cell design is shown in Figure 3.9. This is also the actual input cell design used for the 4:1 video multiplexer. Comparing Figure 3.9 with Figure 3.7, the difference is that the second version design not only has the PNP differential pair of the input stage, but it also includes the folded cascode. Terminals S1P and S1N are now the current outputs of the cell. A current input terminal DIN connects to the corresponding current output terminal (DOT0, DOT1, DOT2, or DOT3) of the decoder. Terminal BIN carries the sloppy voltage reference generated by the biasing stage (discussed in section 3.2) and is used to help deselect the input stage. Even though this alternative design uses more hardware than the previous design, it has many desirable features, such as low crosstalk and convenient shutdown, with little extra power consumption.

When an input stage is unselected, its IN and DIN will draw no current. The base voltage of Q₁₁ drops below the reference voltage BIN. Because of the ECL connection among Q₁/Q₂/Q₃, Q₂ and Q₃ will stop conducting currents. The double-emitter device Q₁ conducts a current of only 20 uA altogether. Since there is no other current flowing in the rest of the circuit, this 20 uA will be the only supply current consumed by the unselected input stage. The following equation shows the current injected into the amplifier by the unselected input stage through terminal S1P/S1N:

$$i_o = \frac{\frac{1}{g_{m1}} \parallel (R_{21} \parallel R_4)}{\frac{1}{g_{m1}} \parallel (R_{21} \parallel R_4) + \frac{1}{C_{je} \cdot s}} \cdot \frac{V_{id}}{\frac{1}{(C_{u13} - C_{u43}) \cdot s + g_{m13(off)}}} \quad (3.6)$$

where g_{m1} and g_{m13} are the transconductances of Q₁ and Q₁₃, C_{je} is the emitter-base junction depletion capacitance of Q₂/Q₃, C_{u13} and C_{u43} are collector-base junction

Input Cell

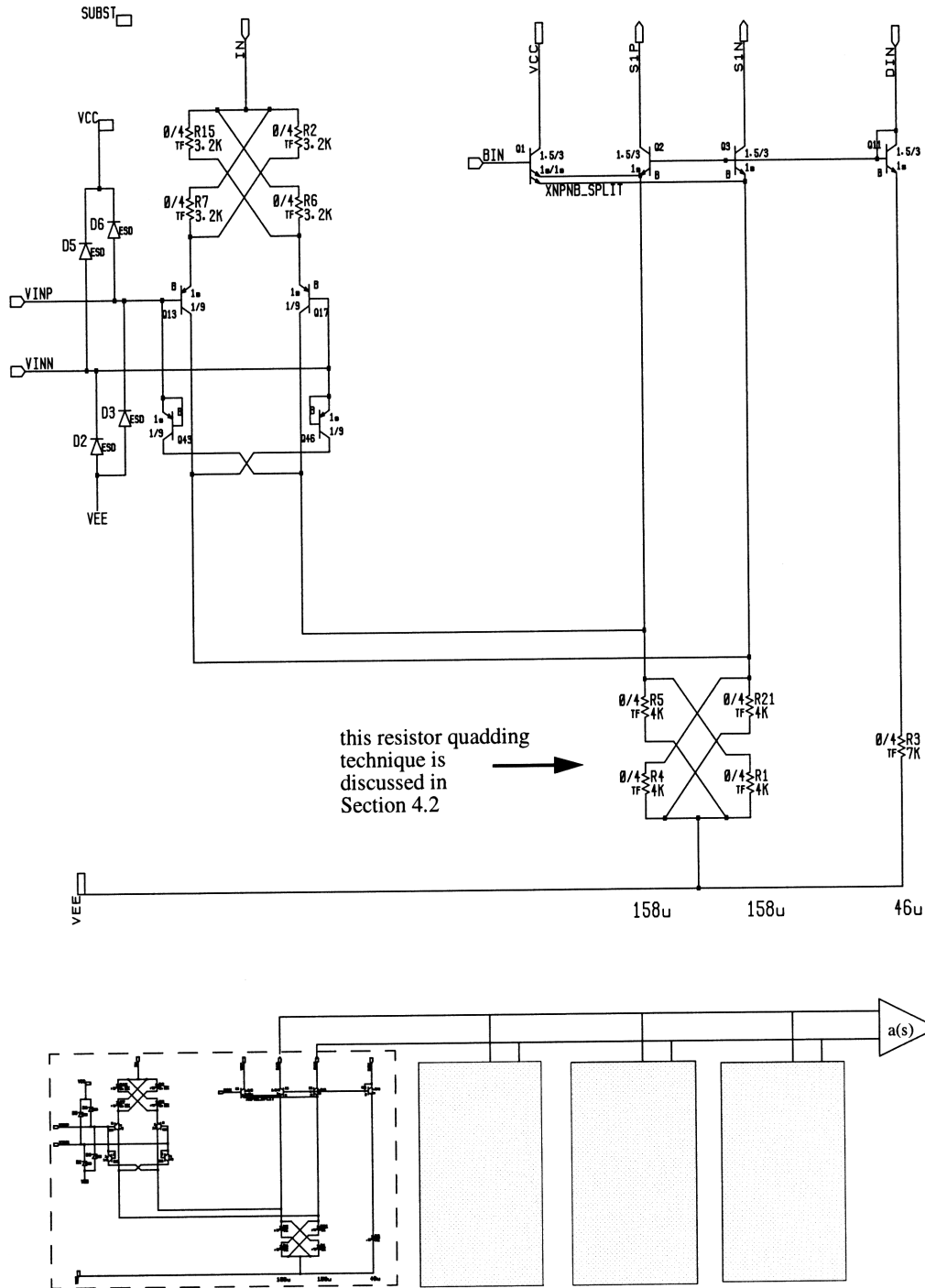


Figure 3.9 Input cell schematic.

capacitances of Q_{13} and Q_{43} , s is $j\omega$, v_{id} is the differential voltage applied to the VINP terminal. An equivalent small signal circuit is proposed in Figure 3.10 to show the derivation of the equation (3.6). The representation of $Y_{m(off)}$ (also written as i_o / v_{id})

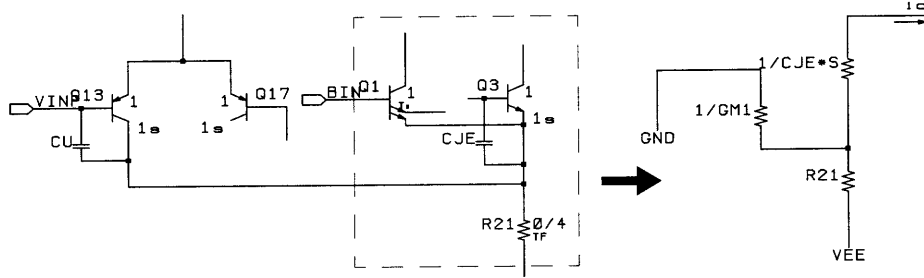


Figure 3.10 Simplified circuit shows the derivation of Eqn. (3.3).

in Eqn. (3.7) is found using Eqn. (3.6) for the unselected input cell. To solve for the crosstalk, we have

$$Crosstalk = \frac{Y_{m(off)}}{g_{m(on)}} = (p(s) \cdot s) \cdot (k \cdot s + 1) \quad (3.7)$$

where g_m is the equivalent transconductance of the selected input stage, given as

$$g_{m(on)} = \frac{g_{m13}}{g_{m13}R_{15} + 1} \quad (3.8)$$

where g_{m13} is the transconductance of Q_{13} . $p(s)$ in Eqn. (3.7), represented as

$$p(s) = \frac{C_{je} \cdot (R_{15} \cdot g_{m13(off)}) \cdot \left(\frac{1}{g_{m1}} \parallel (R_{21} \parallel R_4) \right)}{C_{je} \cdot s \cdot \left(\frac{1}{g_{m1}} \parallel (R_{21} \parallel R_4) \right) + 1} \quad (3.9)$$

C_{je} , R_{21} , g_{m1} , and $g_{m13(off)}$ are parameters belonging to the unselected input stage, while R_{15} is from the selected input stage, C_{je} is the emitter-base junction depletion capacitance

of Q_2/Q_3 , g_{m1} and g_{m13} are transconductances of Q_1 and Q_{13} . k in Eqn. (3.4) is given as

$$k = \frac{C_{u13} - C_{u43}}{g_{m13(off)}} \quad (3.10)$$

where C_{u13} and C_{u43} are collector-base junction capacitances of Q_{13} and Q_{43} of the unselected input cell. The calculation shows that $p(s)$ has a pole at 50 GHz. When comparing Eqn. (3.7) with Eqn. (3.5), because of the extra multiplicative term s in Eqn. (3.7), the calculated crosstalk is seen to be very small and the match between Q_{13} and Q_{43} becomes noncritical. The simulation shows that the crosstalk has dropped from -85 dB to -114 dB, a significant improvement. However, the computer simulated crosstalk is still higher than the hand calculation. This suggests that the crosstalk has a different contributor which we have not been able to discover.

In the input cell design, the input PNP differential pairs seen in Figure 3.11 are worthy of attention. The equivalent RC network is shown in Figure 3.12.

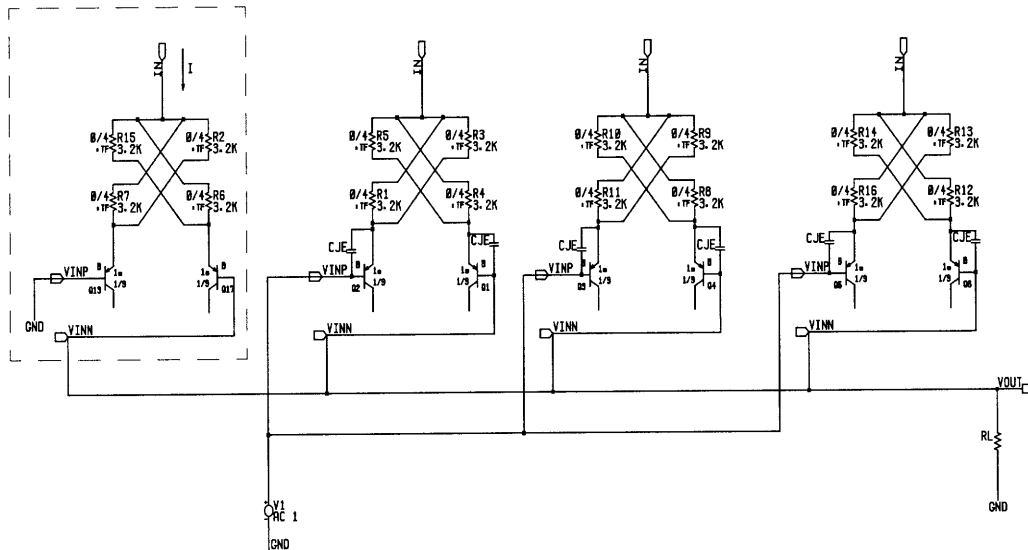


Figure 3.11 Circuit used for all-hostile crosstalk calculation.

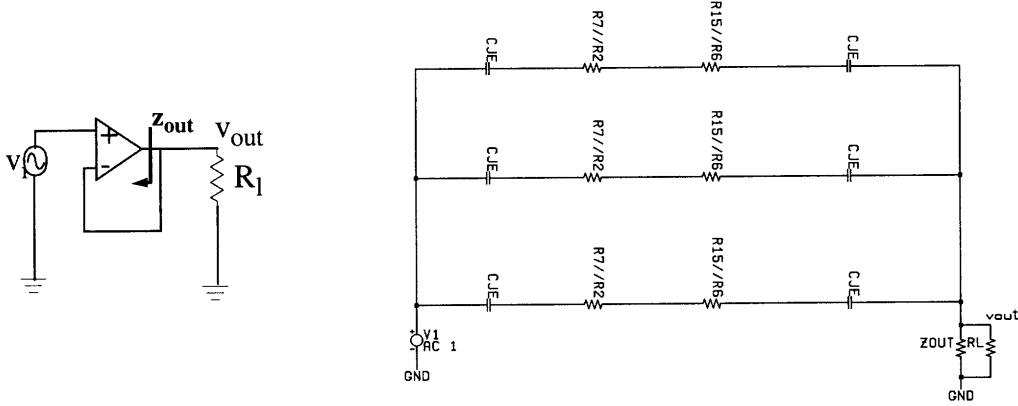


Figure 3.12 RC network representation of the unselected input stages of Figure 3.11.

Since the value of $R_{15}//R_6$ is the same as $R_7//R_2$, the equation shown below gives the relationship between the input and the output of the RC network seen in Figure 3.12.

$$V_{out} = \frac{3z_{out}(s)}{z_{out}(s) + 2(R_{15} \parallel R_6) + \frac{1}{0.5C_{je} \cdot s}} \cdot v_i \quad (3.11)$$

Here $z_{out}(s)$ is the frequency-dependent output impedance of the multiplexer, R_{15} and R_6 are resistors from the unselected input stage, C_{je} is the emitter-base junction capacitance of the PNP transistors Q_{13}/Q_{17} of the unselected input cell. The load resistance R_L is ignored in Eqn. (3.11) since it is in parallel with $z_{out}(s)$ which is very small. Eqn. (3.11) is further rearranged giving

$$\frac{V_{out}}{v_i} = 3 \cdot \frac{z_{out}(s) \cdot C_{je} \cdot s}{2 + C_{je} \cdot (z_{out}(s) + 2(R_{15} \parallel R_6)) \cdot s} \quad (3.12)$$

when ω is within the multiplexer's operational range, Eqn. (3.12) simplifies to:

$$\frac{V_{out}}{V_i} = 3 \cdot \frac{z_{out}(s) \cdot C_{je} \cdot s}{2} \quad (3.13)$$

Eqn. (3.13) is also the expression for the all-hostile crosstalk of the multiplexer. At 10 MHz, using the simulated results of $z_{out}(s)$ and C_{je} , the all-hostile crosstalk is hand-calculated to be -114 dB which matches the computer simulation.

The validity of this crosstalk model can be verified by exploring the form of $z_{out}(s)$. Figure 3.13 shows the circuit used for calculating $z_{out}(s)$. $z_{out}(s)$ can be written as

$$z_{out}(s) = \frac{V_{test}}{I_{test}} = \frac{1}{g_{m70} \cdot a(s)} \quad (3.14)$$

where v_{test} is the test voltage applied at the output, i_{test} is the test current collected at the output, g_{m70} is the transconductance of Q_{70} , $a(s)$ is a frequency-dependent voltage gain. If we write $z_{out}(s)$ as $R + Ls$ where R and L are fitted to the simulated $z_{out}(s)$ as 7 m Ω and 11.14 nH, respectively, the all-hostile crosstalk can be modeled as shown in Figure 3.14 and Eqn. (3.13) can be written as

$$\frac{V_{out}}{V_i} = 3 \cdot \frac{(R + Ls) \cdot C_{je} \cdot s}{2} \quad (3.15)$$

Computer simulated results of both the simulated all-hostile crosstalk and the calculated RLC network model of the crosstalk are presented in Figure 3.15 and Figure 3.16 respectively. A comparison of these two plots shows that we have correctly modeled the multiplexer's crosstalk.

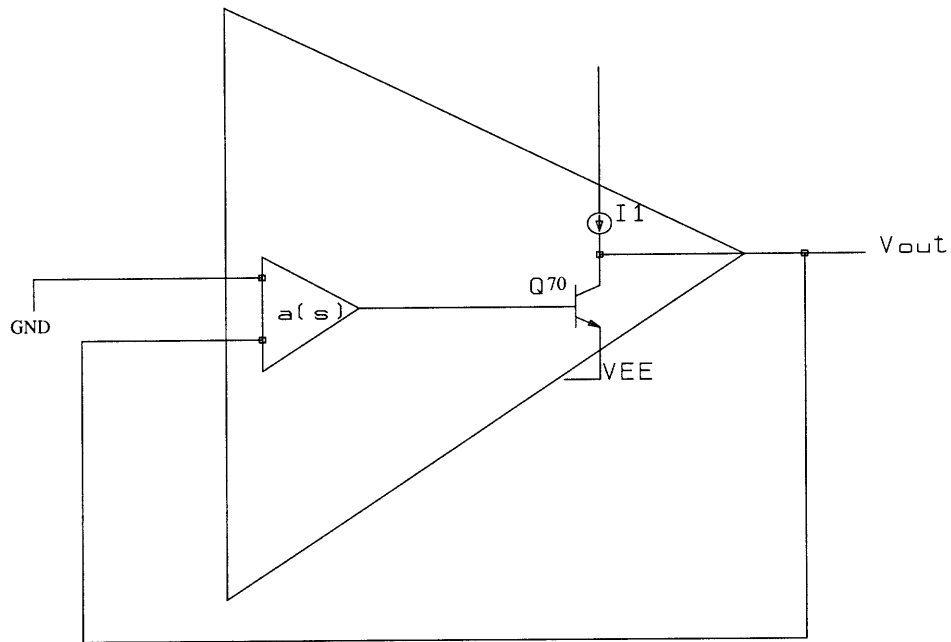


Figure 3.13 Circuit for output impedance calculation.

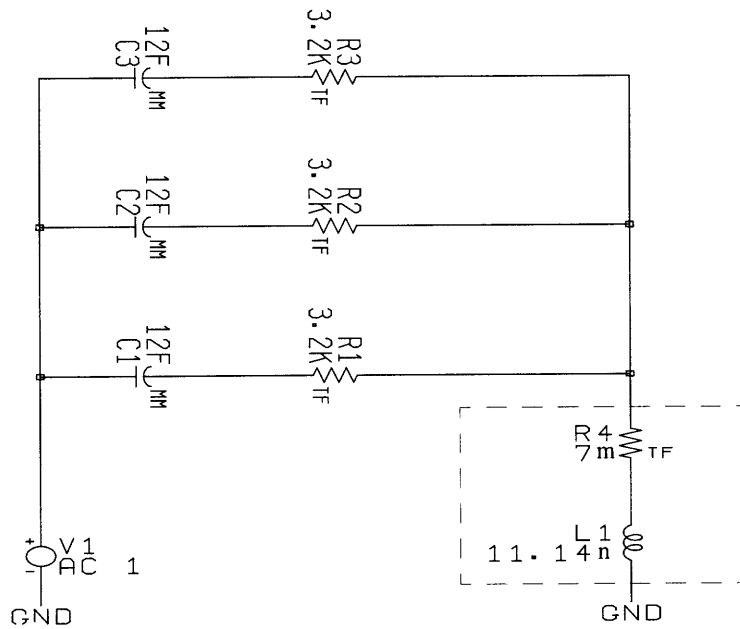


Figure 3.14 RLC network model for crosstalk calculation.

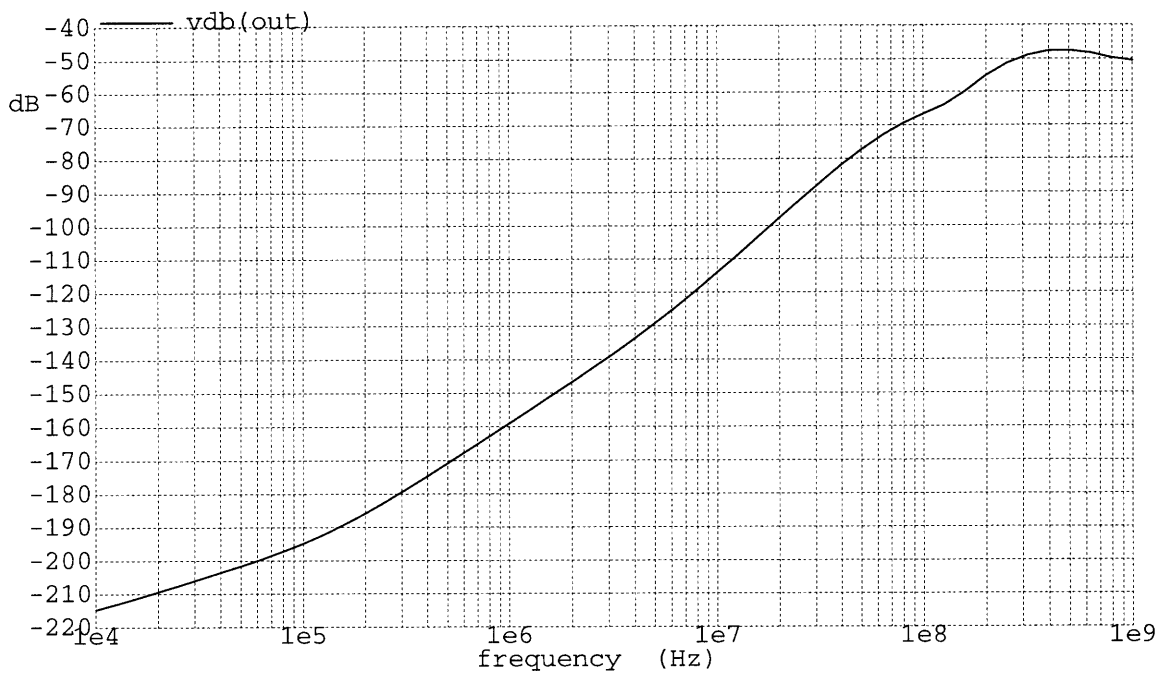


Figure 3.15 Magnitude of the all hostile crosstalk.

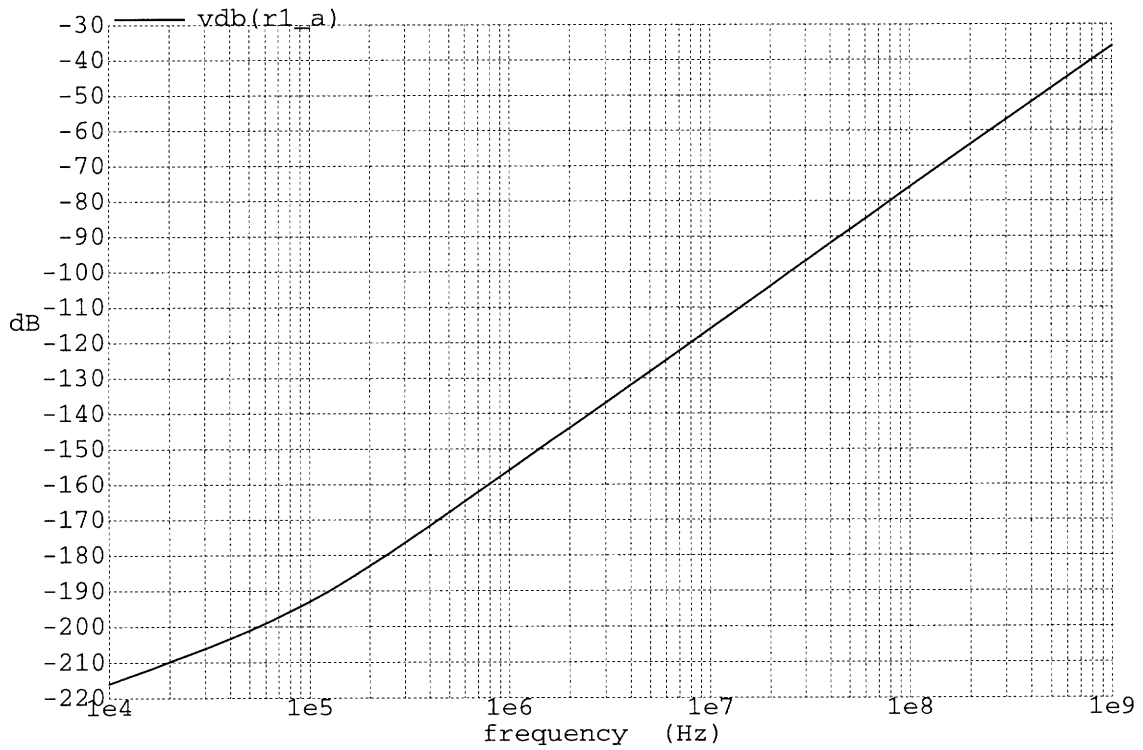


Figure 3.16 Simulation of the crosstalk's RLC model.

The off isolation of the multiplexer also improves in the second version of the input cell design. Figure 3.17 shows the circuit used for the off isolation calculation. To test the multiplexer's off isolation, chip disable is selected. This turns off all the input stages and the output amplifier and causes the output impedance to be very high. The output impedance is ignored since it is in parallel with the load resistance R_L .

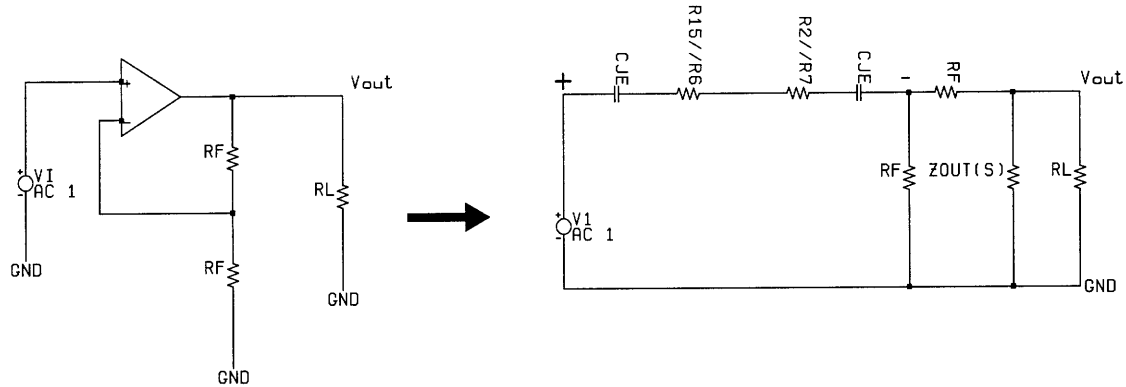


Figure 3.17 Circuit diagram for calculating off isolation.

The above figure leads to an equation to solve for the off isolation. After rearranging all the terms and simplifying the equation, we have

$$Offisolation = \frac{V_{out}}{V_i} = R_L \cdot \frac{R_F}{4 \cdot \left(R_F + \frac{R_L}{2} \right)} \cdot C_{je} \cdot s \quad (3.16)$$

where C_{je} is the emitter-base junction depletion capacitance of Q_{13}/Q_3 . At a frequency of 10 MHz, using 150Ω for R_L and $1 \text{ K}\Omega$ for R_F , the off isolation is calculated to be -98 dB, which is close to the simulated result -91dB.

There is another advantage to using the second version of the design. In the first version, all the input cells are tied together and connected to the low impedance nodes of the output amplifier, whereas the second version design ties all the input cells to the high impedance nodes of the amplifier and adds the parasitics to the dominant pole.

Circuit layout and packaging can also affect the crosstalk performance. Chapter 4 will discuss these issues in detail.

Finally, from Figure 3.18, we derived the expression for the input headroom. It gives

$$V_{EE} + (R_{21} \parallel R_4) \cdot (I_{C3} + I_{C13}) + V_{CE13} - V_{EB13} < V_{IN} < V_{CC} - (R_1 \cdot I_1) - V_{EC37} - (R_2 \parallel R_7 \cdot I_{C13}) - V_{EB13} \quad (3.17)$$

Substituting values for all the terms in Eqn. (3.17), the input headroom is solved at 27 °C to be

$$V_{EE} - 0.2V < V_{IN} < V_{CC} - 1.46V \quad (3.18)$$

where V_{CC} and V_{EE} are positive and negative supplies respectively.

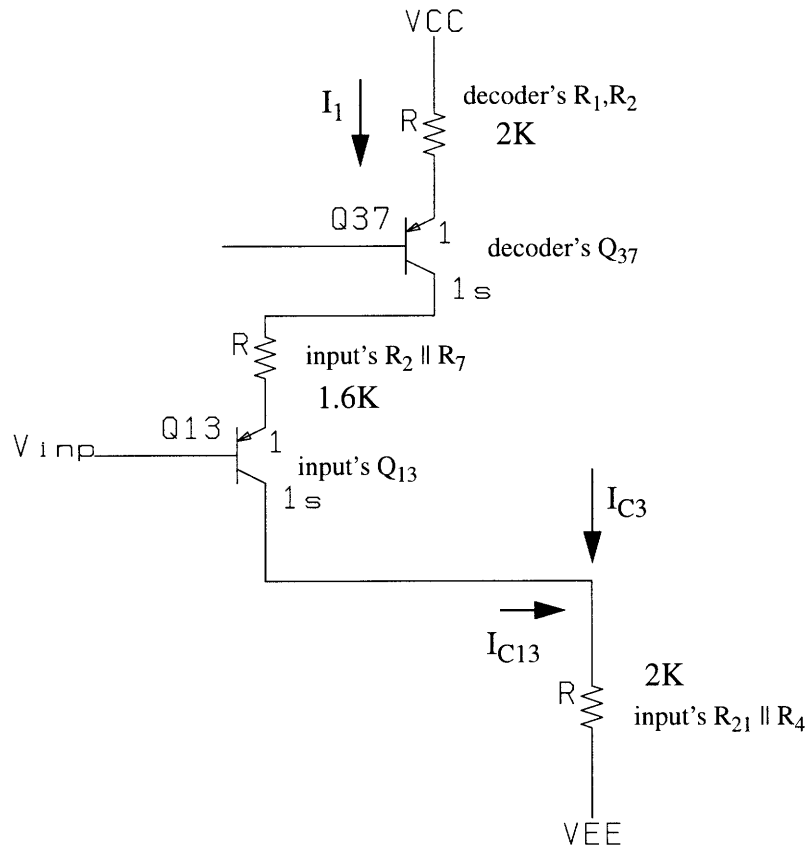


Figure 3.18 Input voltage range.

3.5 The Output Amplifier

The simplified schematic of the output amplifier is presented in Figure 3.19. This amplifier is similar to the operational amplifier AD8041 except for some minor changes to accommodate the multiplexer's operation. The design theory of this cell has been dis-

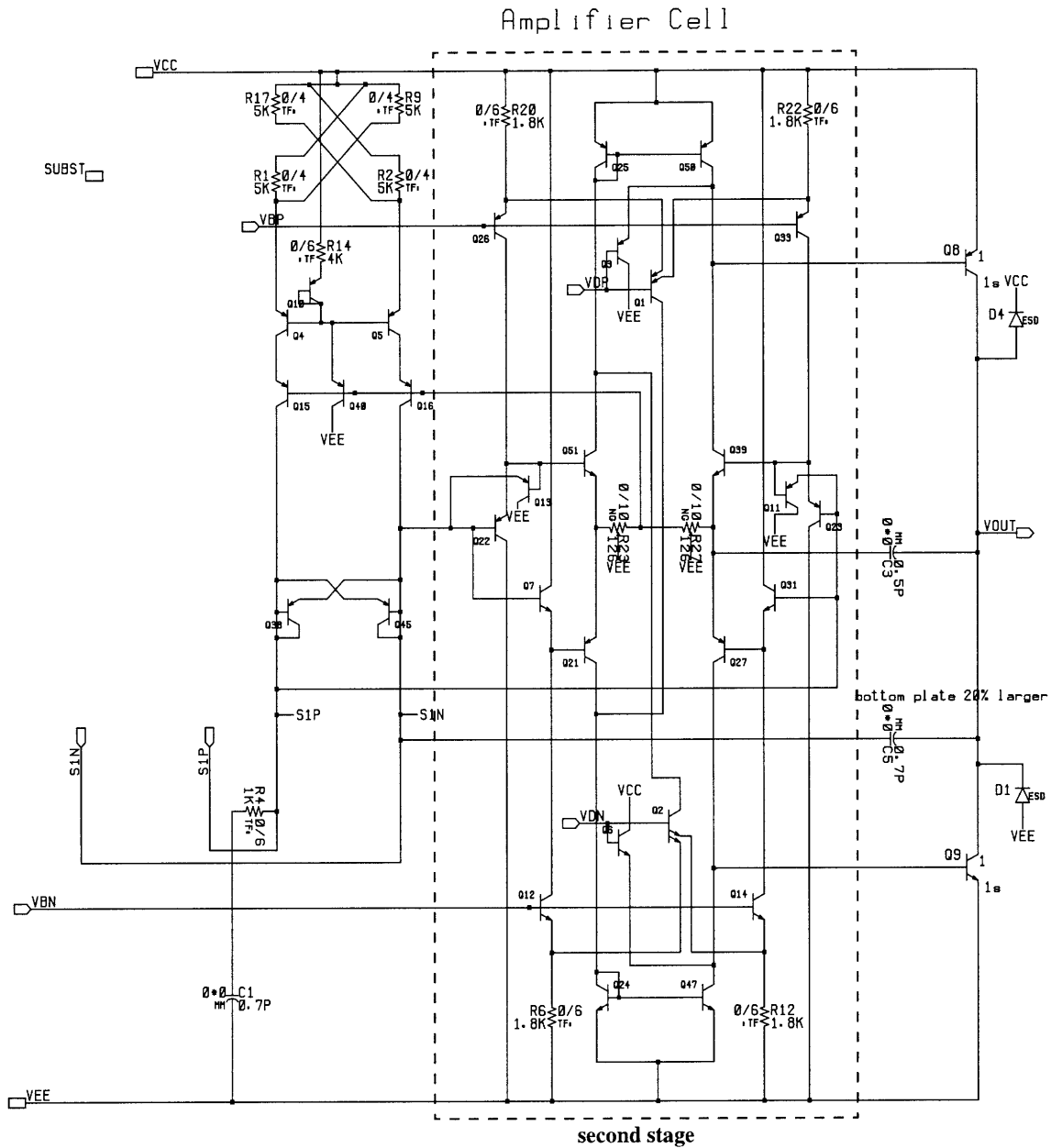


Figure 3.19 Simplified output amplifier schematic.

cussed in Section 2.3. The inputs VBP and VBN are voltages delivered by the biasing cell

which are used by the current sources of the amplifier to produce temperature independent bias currents; VDP and VDN are voltages from the biasing cell which help to turn off the amplifier when the chip is disabled; SIP and SIN are the differential current inputs to the output amplifier. The output terminal of the amplifier is also the output of the multiplexer.

As discussed before, most of the operational features of the AD8041 amplifier are desirable except for its slow disable function. The multiplexer's amplifier design has used several circuit techniques to address that problem. When the AD8041 is disabled, currents will keep on flowing through Q_{50} and Q_{47} . However, since the output devices have lost their base currents, the collector nodes of Q_{50} and Q_{47} will drop and lead both transistors into saturation. To prevent this from happening, clamp transistors Q_3 and Q_6 are added to catch the collector nodes and stop them from dropping too low.

Clamp Q_3 's base and emitter are tied to VDP and the Q_{50} 's collector respectively; clamp Q_6 's base and emitter are connected to VDN and the Q_{47} 's collector in a similar fashion. When the amplifier is enabled, VBN and VBP are both about 900 mV away from the supply rails, and VDN and VDP are approximately 400 mV from the supplies. Because of the ECL connection between the double-emitter PNP transistor Q_1 and Q_{26}/Q_{33} (the same style is also used by Q_2 , Q_{12} and Q_{14}), transistors Q_1 and Q_2 are off and all current sources of the amplifier are in normal operation. Clamps Q_3 and Q_6 are in cutoff since the output devices are conducting the right amount of currents and VDP/VDN are both close to the supply rails.

When the amplifier is disabled, VDP and VDN will have voltage levels of about 1 V from the supply rails, while both VBP and VBN are pushed close to the supplies (400 mV away from each rail). Again, due to the ECL connections, currents are quickly steered

into Q_1 and Q_2 . Current sources of the amplifier are all turned off and the operation is disabled. Currents collected at the emitters of Q_1 and Q_2 are dumped into Q_{25} and Q_{24} respectively and mirrored through Q_{47} and Q_{50} to pull down the bases of the output devices. The collector voltage of Q_{50} and Q_{47} will drop again, but this time, since they are also tied to the emitters of Q_3 and Q_6 , both Q_3 and Q_6 are turned on. The collectors of Q_{50} and Q_{47} are caught at one V_{BE} below V_{DP} and V_{DN} respectively, which are about 250 mV away from the supplies; thus those transistors are not saturated.

In addition, PNP transistors Q_{13} and Q_{11} are included in the second stage of the AD8041 amplifier to protect transistors from being severely reverse biased. Since most of the voltages in the AD8041's second stage are not well defined during the disable, simulation shows that Q_{22} and Q_{23} can be reverse-biased by more than 3 V when the amplifier is shut down. As discussed in Section 2.2, the XF1.5 process has a BV_{EBO} of only 4.5 V. When a transistor is reverse-biased by more than 3 V, it could experience a harmful stress which would cause β degradation and ultimately damage the device. Two transistors, Q_{13} and Q_{11} , are connected to the bases of Q_{22}/Q_{51} and Q_{23}/Q_{39} respectively. When the amplifier is enabled, those two transistors are off and reverse-biased by about 700 mV, and the rest of the amplifier circuit operates normally. Once the amplifier is shut down, Q_{13} and Q_{11} will be forward biased by about 400 mV. They will not conduct currents since their V_{BE} 's are still low, but they will define the V_{BE} 's of Q_{22} and Q_{23} so that they can only be reverse-biased by about 400 mV during the disable.

3.6 Computer Simulation Results

The operation and performance of the multiplexer circuit were verified by ADICE5 (an Analog Devices simulation tool). The results listed in Table 1 and the plots presented in this section are simulation results in the absence of layout parasitics. The effects of these parasitics are discussed in Chapter 5.

Table 1: Video MUX Specifications (@27°C, $V_{CC}=5V$, $R_L=2K$, $G=1$, $V_{out,dc}=2.5V$)

Parameter	Conditions	Simulation Results	Units
<i>Dynamic Performance</i>			
-3dB Bandwidth (small signal)	$G=1$	148	MHz
Phase Margin	$G=1$	63	degree
-3dB Bandwidth(large signal)	2 V _{pp}	50	MHz
Bandwidth for 0.1dB Flatness	$G=2$, $R_l=150\text{ohm}$, $R_f=1k$	12.7	MHz
Slew Rate	V_o starts at 1V	170	V/us
positive edge	$V_o = 2V$ step	200	V/us
negative edge			
Rise Time (10% - 90%)	V_o starts at 1V	9.4	ns
Fall Time (90% - 10%)	$V_o = 2V$ step	7.2	ns
Settling Time to 0.1%	V_o starts at 1V	25	ns
	$V_o = 2V$ step		
<i>Switching Characteristics</i>			
50% logic to 10% output settling	switching steps 1 V step at output	4	ns
50% logic to 90% output settling	switching steps 1 V step at output	9.7	ns
50% logic to 99.9% output settling	switching steps 1 V step at output	15	ns
Turn-on Time	0V->2.5V at output	20.2	ns
50% logic to 90% output settling			

Table 1: Video MUX Specifications (@27°C, V_{CC}=5V, R_L=2K, G=1, V_{out,dc}=2.5V)

Parameter	Conditions	Simulation Results	Units
Turn-off Time 50% logic to 90% output settling	3.5V->0 at output	52.7	ns
Channel Switching Glitch	ground all inputs	48	mVpp
<i>Power Supply</i>			
+PSRR	DC	114	dB
-PSRR	DC	119	dB
Quiescent Current (enabled)	V _s =± 2.5V no load	6.37 / 6.20	mA
Quiescent Current (disabled)	V _s =± 2.5V no load	2.6 / 2.5	mA
<i>Output Characteristics</i>			
Output Voltage Swing	G=2, R _f = 1K, V _s =± 2.5 V	V _{EE} + 0.04 to V _{CC} - 0.04	V
Output Current	V _{out} =0.5 V, 4.5 V, R _I =10 Ω	50	mA
Short Circuit Current		-158 / 120	mA
Output Resistance (enabled) (disabled)	DC	10 20	mΩ GΩ
Output Capacitance	Disabled	6.4	pF
<i>Input Characteristics</i>			
Input Voltage Range		V _{EE} - 0.2 to V _{CC} - 1.46	V
Input CMRR	R _f =1K, R _I =100 Ω DC	-101	dB
Input Offset Voltage	from hand calculation, 1σ	2	mV
<i>Distortion/Noise Performance</i>			
Differential Gain	f=3.58MHz, V _s =± 2.5V, R _L =150 Ω	0.03	%

Table 1: Video MUX Specifications (@27°C, V_{CC}=5V, R_L=2K, G=1, V_{out,dc}=2.5V)

Parameter	Conditions	Simulation Results	Units
Differential Phase	f=3.58MHz, V _s =±2.5V,R _L =150 Ω	0.03	degree
All Hostile Crosstalk	10 MHz	-114	dB
Off Isolation	R _l =100, f=10MHz, G=2, R _f =1K, single channel	-91	dB
Input Voltage Noise	10 MHz	15.2	nV/ Hz ^{1/2}
Total Harmonic Distortion	10 MHz sin of 2Vpp	-62	dB
Operating Temperature Range		-50 to 150	°C

Figure 3.20 shows that the multiplexer's unity-gain frequency is 90 MHz, and the phase margin is 63°. Figure 3.21 shows the multiplexer's -3 dB small signal bandwidth is at 148 MHz. Its slew rate is shown in Figure 3.22.

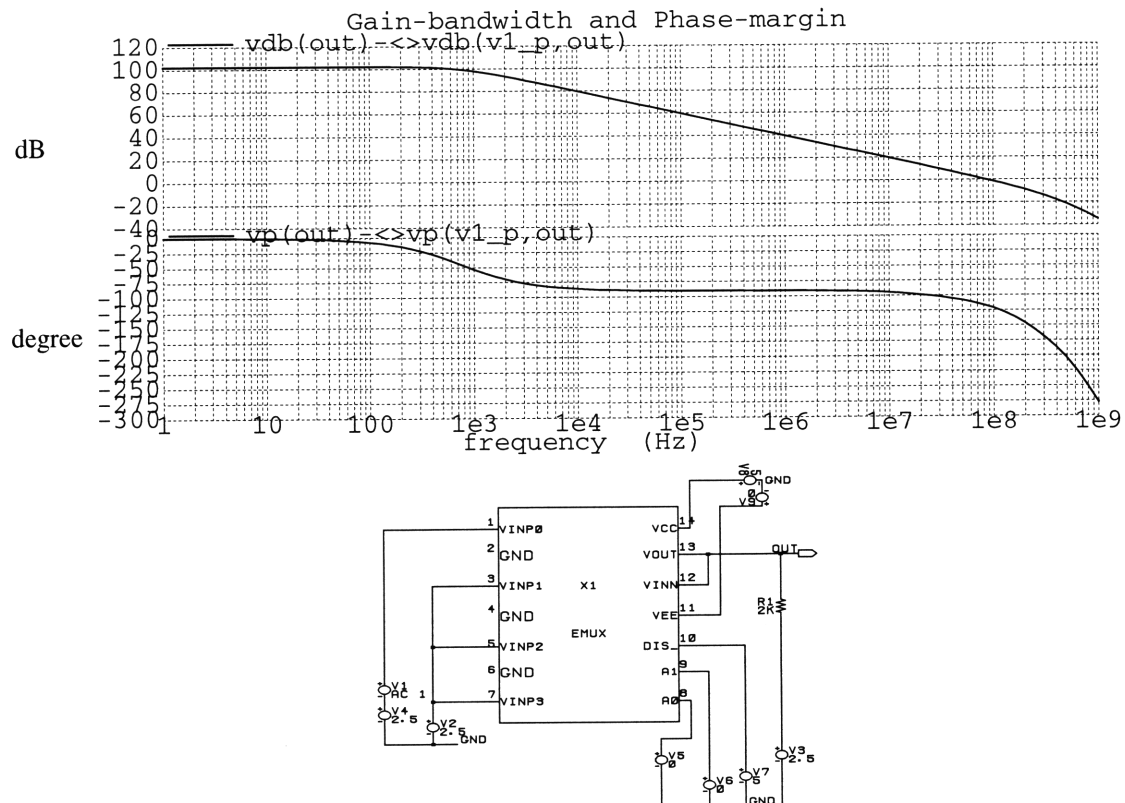


Figure 3.20 Open-loop gain and phase, and their test circuit.

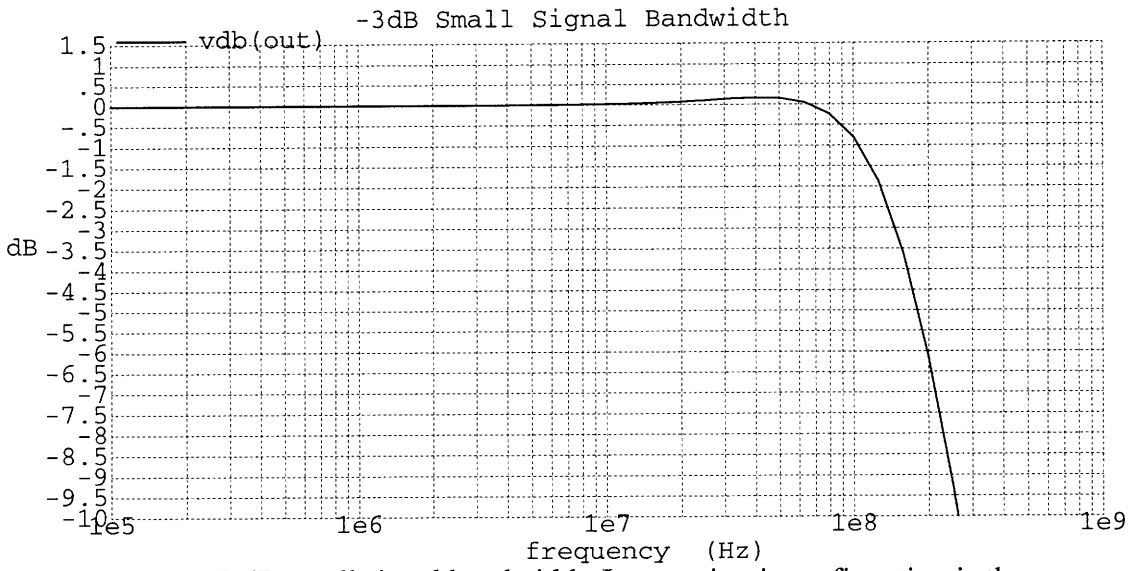


Figure 3.21 -3 dB small signal bandwidth. Its test circuit configuration is the same as shown in Figure 3.20.

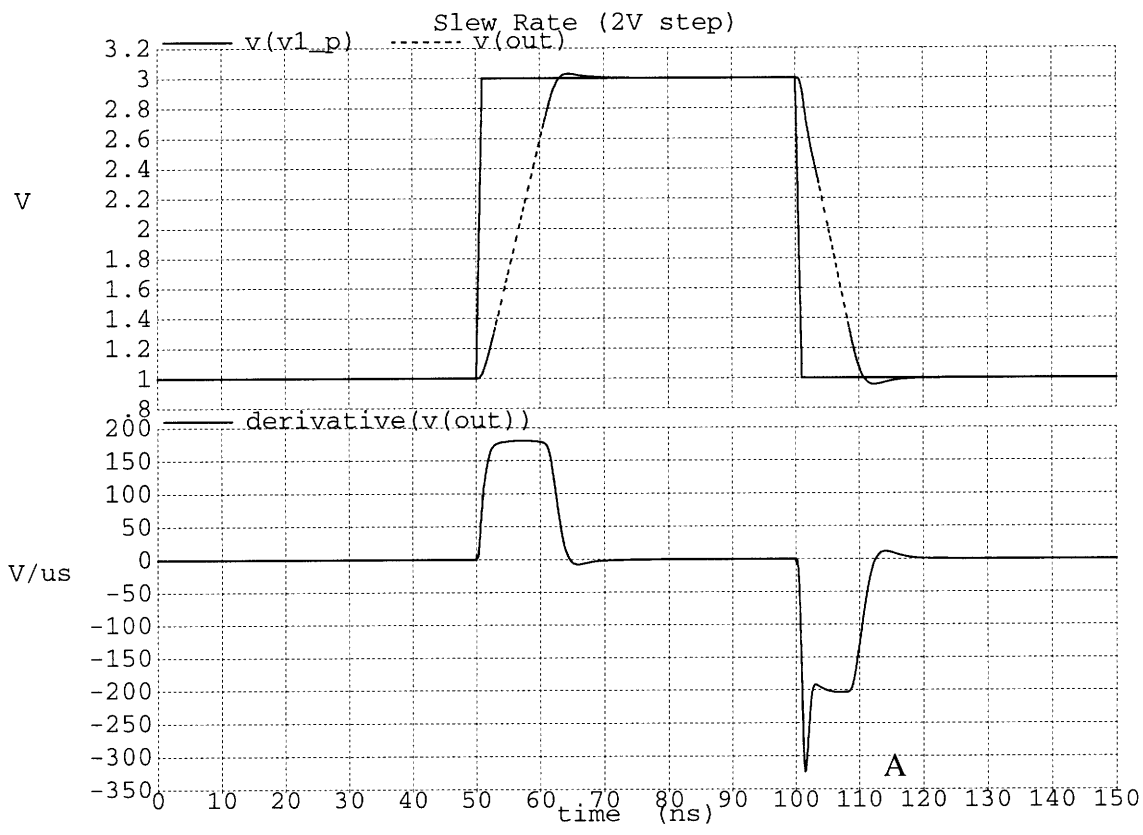


Figure 3.22 Slew Rate. The peaking “A” shown in the second trace is due to the discharging of the parasitic capacitances at the common emitter node of the input PNP differential pair transistors.

The channel switching and circuit disable are simulated as is seen in Figure 3.23. Figure 3.24 zooms in the switching transient, showing that the switching is 90% completed within 10 ns. This switching speed is slew limited by the amplifier. Figure 3.25 shows that the disable transient will last about 53 ns. Figure 3.26 indicates that the switching glitch is within 48 mV peak-to-peak. This glitch is simulated by switching the multiplexer from channel to channel while keeping all channels at the same DC voltage level (eg. 2.5 V for our case).

Differential gain and phase are simulated using NSTC (National Television Standards Committee) standard (sweep the DC input voltage from - 0.3 V to 0.7 V at a fixed frequency 3.58 MHz). Figure 3.27 shows the differential gain is 0.03% and the differential phase is 0.03° . The all-hostile crosstalk and off isolation have been discussed in Section 3.4. Figure 3.28 and Figure 3.29 present the simulation results of their magnitude and phase. At 10 MHz, the all-hostile crosstalk is shown to be -114 dB, and the off isolation is -91 dB.

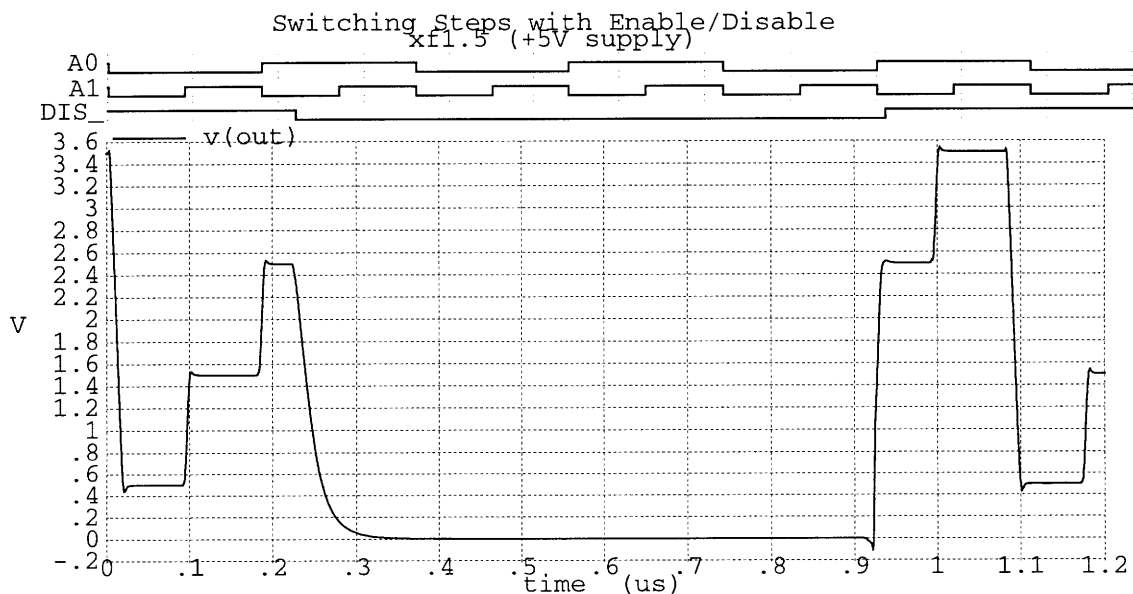


Figure 3.23 Switching Steps with Enable and Disable.

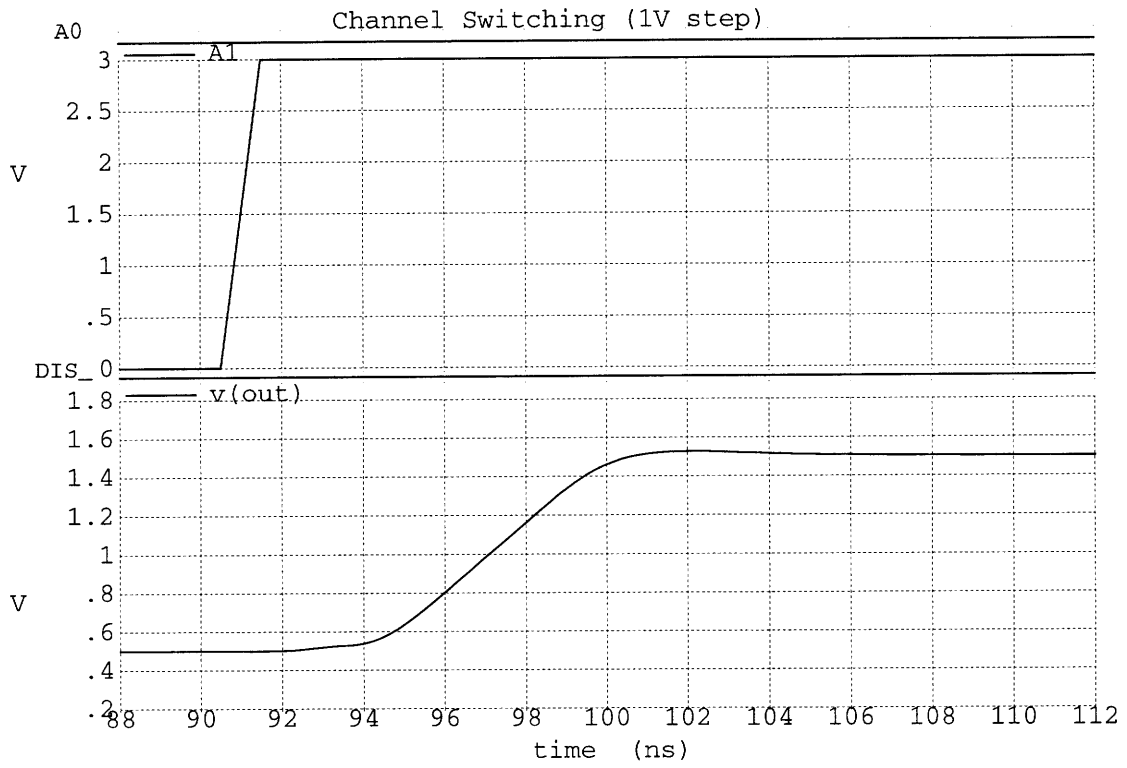


Figure 3.24 Channel switching time.

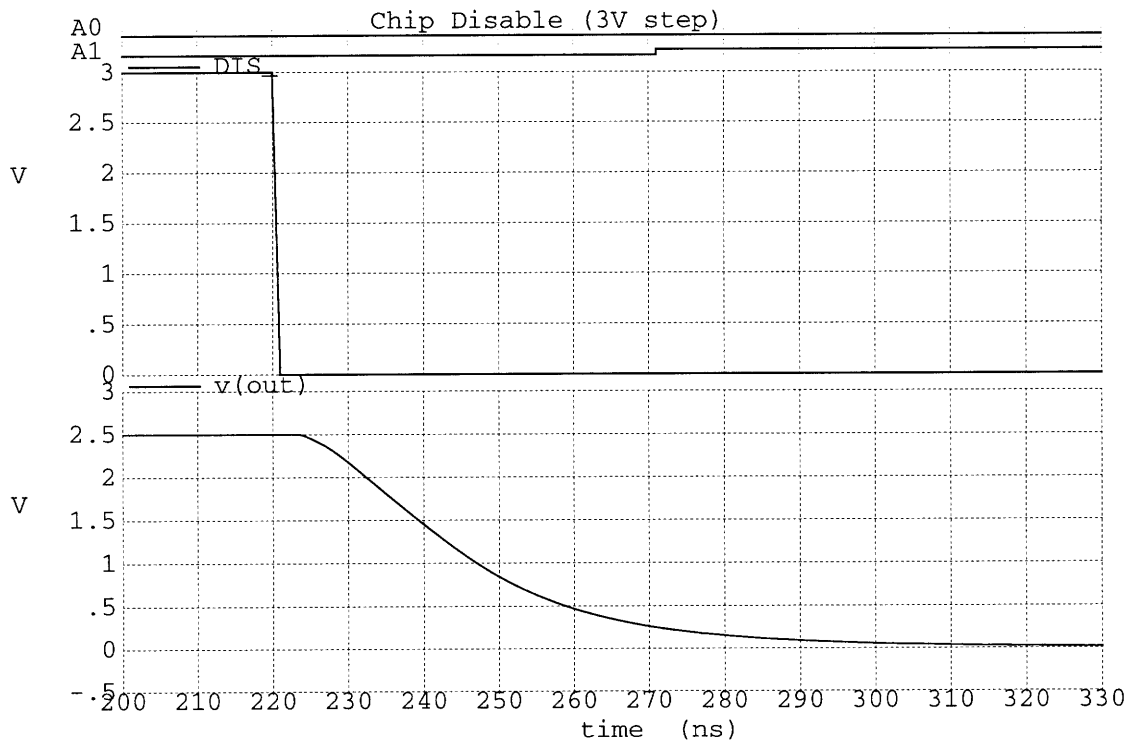


Figure 3.25 Disable transient.

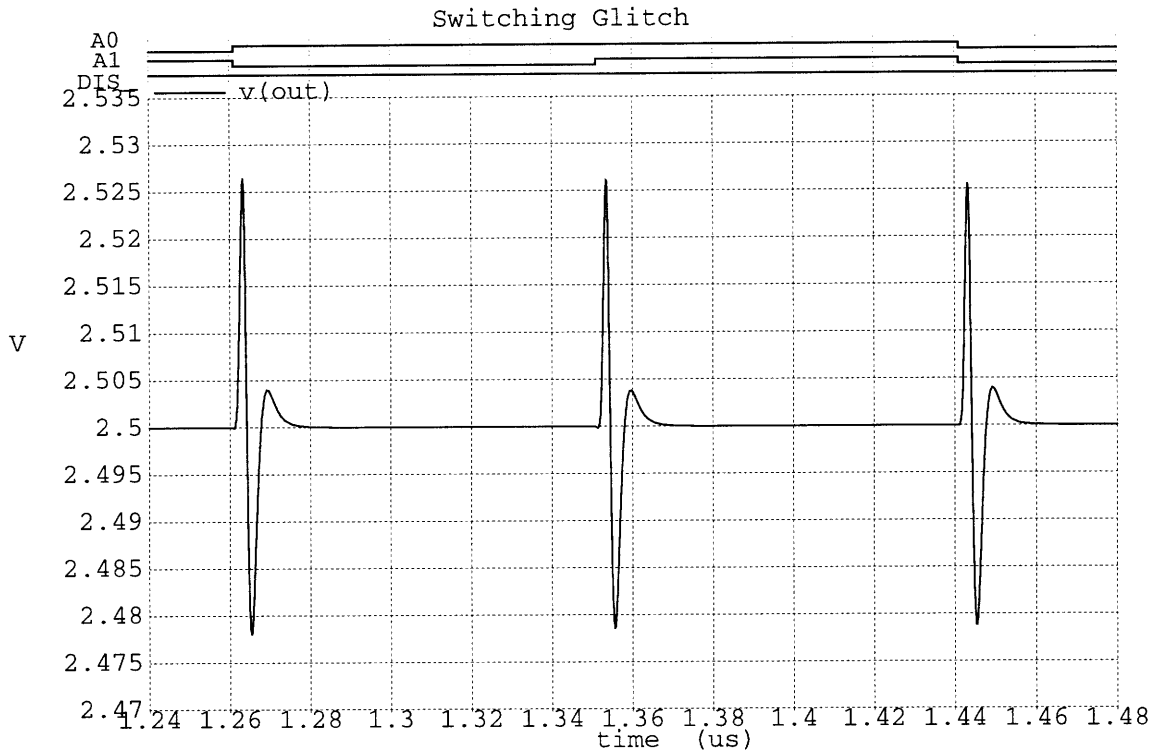


Figure 3.26 Channel switching glitch.

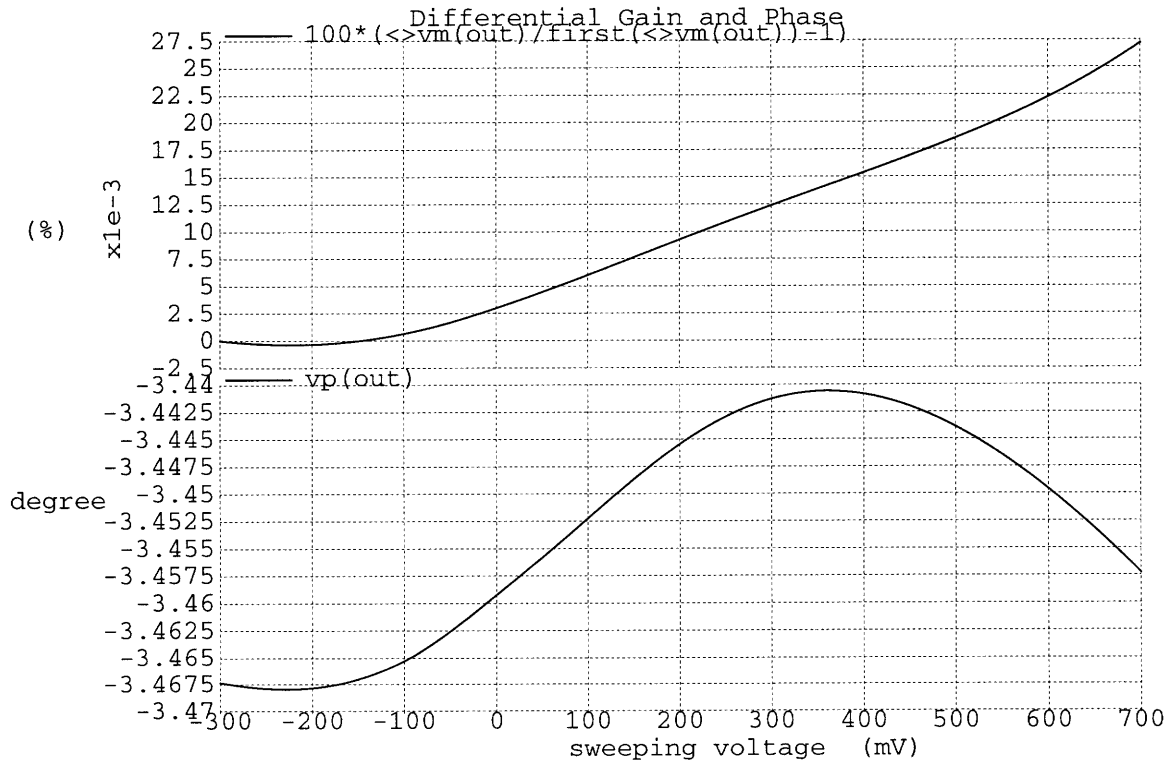


Figure 3.27 Differential gain and differential phase error.

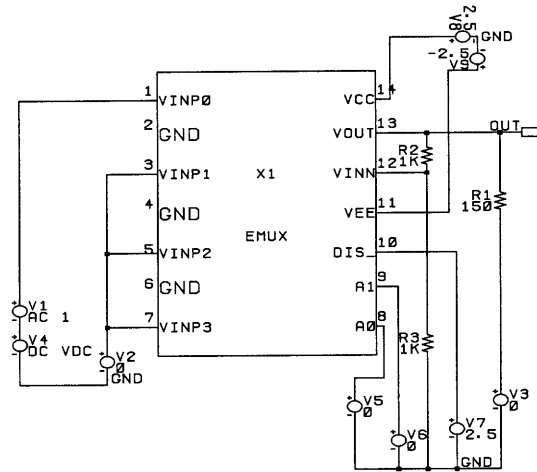


Figure 3.27.1 Test circuit for differential gain and differential phase error.

Simulation commands (in XADICE5):

```
>freq 3.58meg
>sweep vdc from -0.3 to 0.7
>go
```

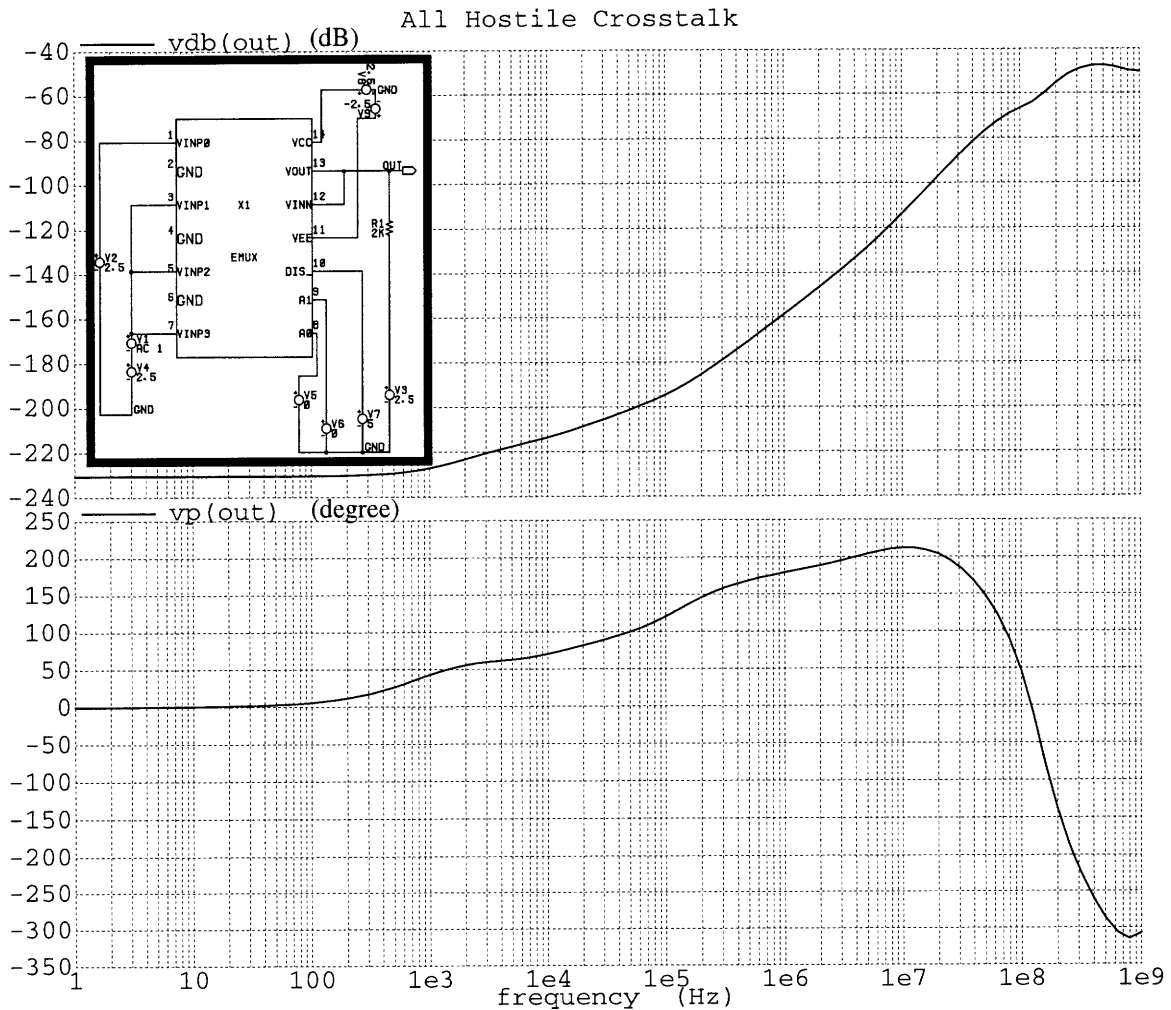


Figure 3.28 Magnitude and phase of all hostile crosstalk.

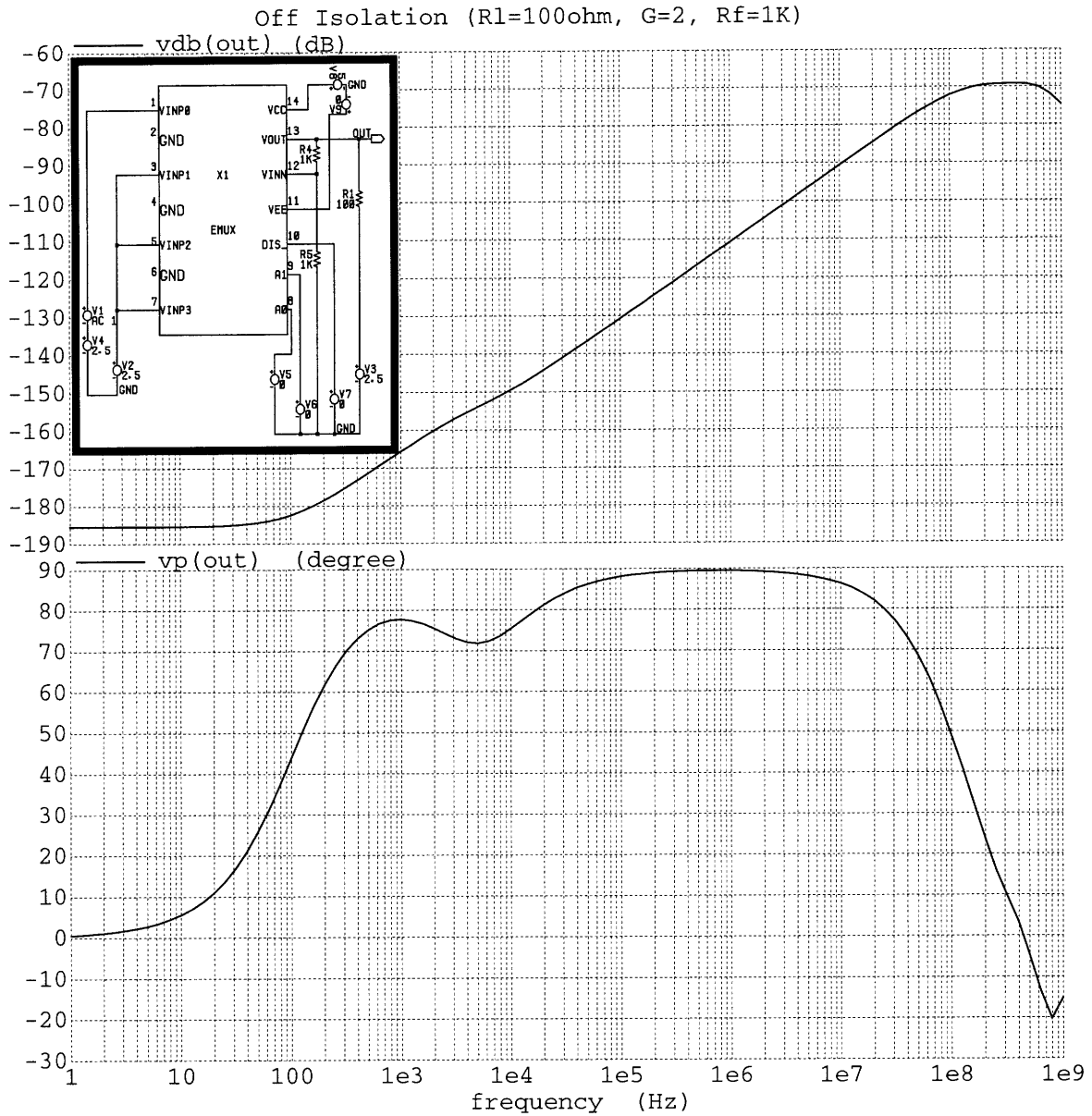


Figure 3.29 Magnitude and phase of off isolation.

The input noise is $15 \text{ nV/Hz}^{1/2}$ as shown in Figure 3.30. This is mainly due to the thermal noises contributed by R_{15}/R_6 , R_2/R_7 , R_5/R_1 , and R_{21}/R_4 from the input stage. The output resistance while enabled is simulated to be $10 \text{ m}\Omega$, as seen in Figure 3.31, matching closely the calculated result from Eqn. (3.15). The actual value will be larger than this due to the additional bond wire and lead frame resistances (estimated to be about $3 \text{ m}\Omega$). The disabled output resistance is shown in Figure 3.32 to be $20 \text{ G}\Omega$.

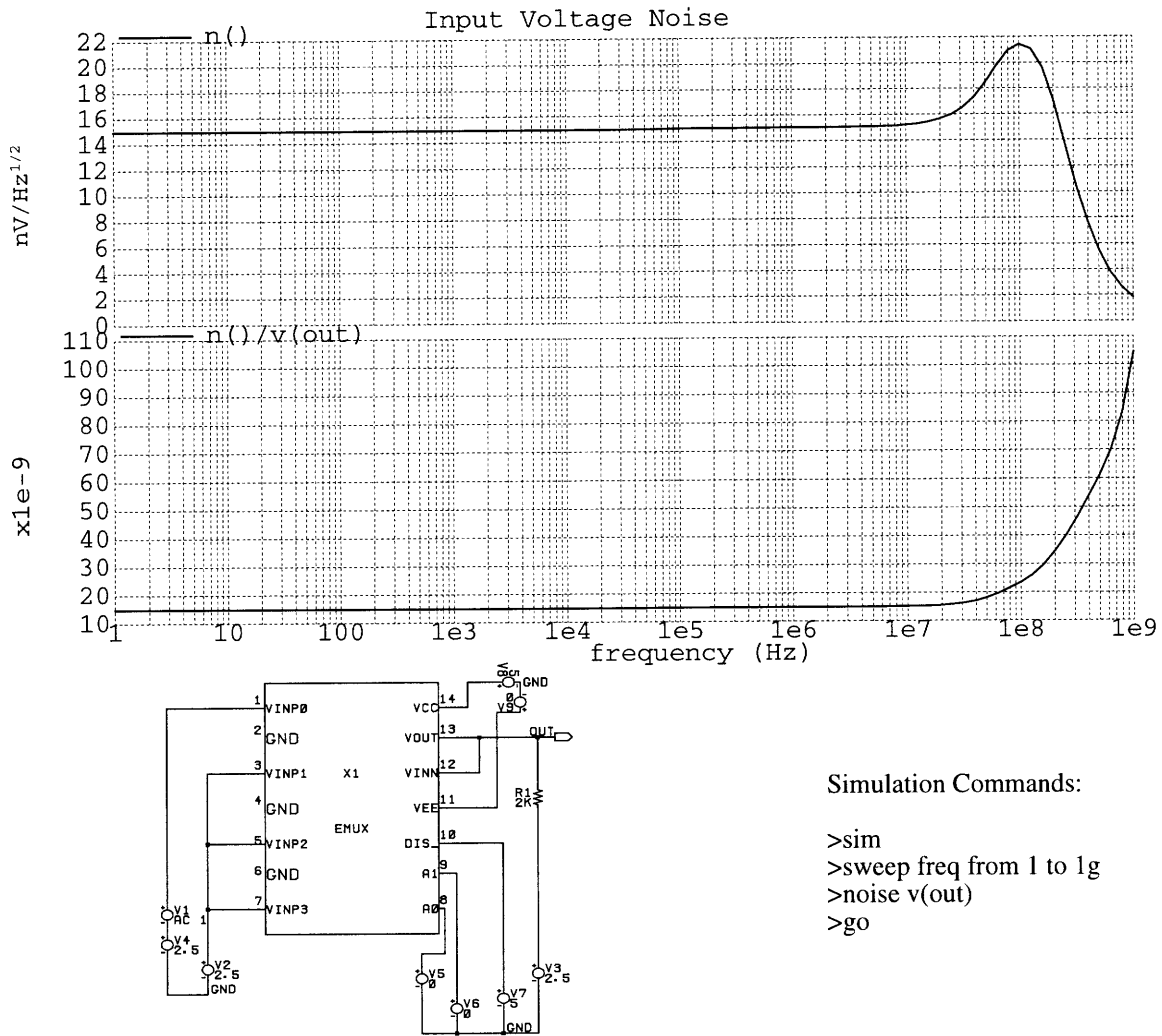


Figure 3.30 Input voltage noise.

To calculate the effective output capacitance when the multiplexer is disabled, the following equation can be used:

$$z = \frac{R}{RCs + 1} \quad (3.19)$$

where R is the DC value of the disabled output resistance, C is the output capacitance, z is the output impedance at any frequency. Reading out values from Figure 3.32, R is 20 GΩ, z / Ω is 80 dB at 2.5 MHz. The output capacitance is then solved to be 6.4 pF.

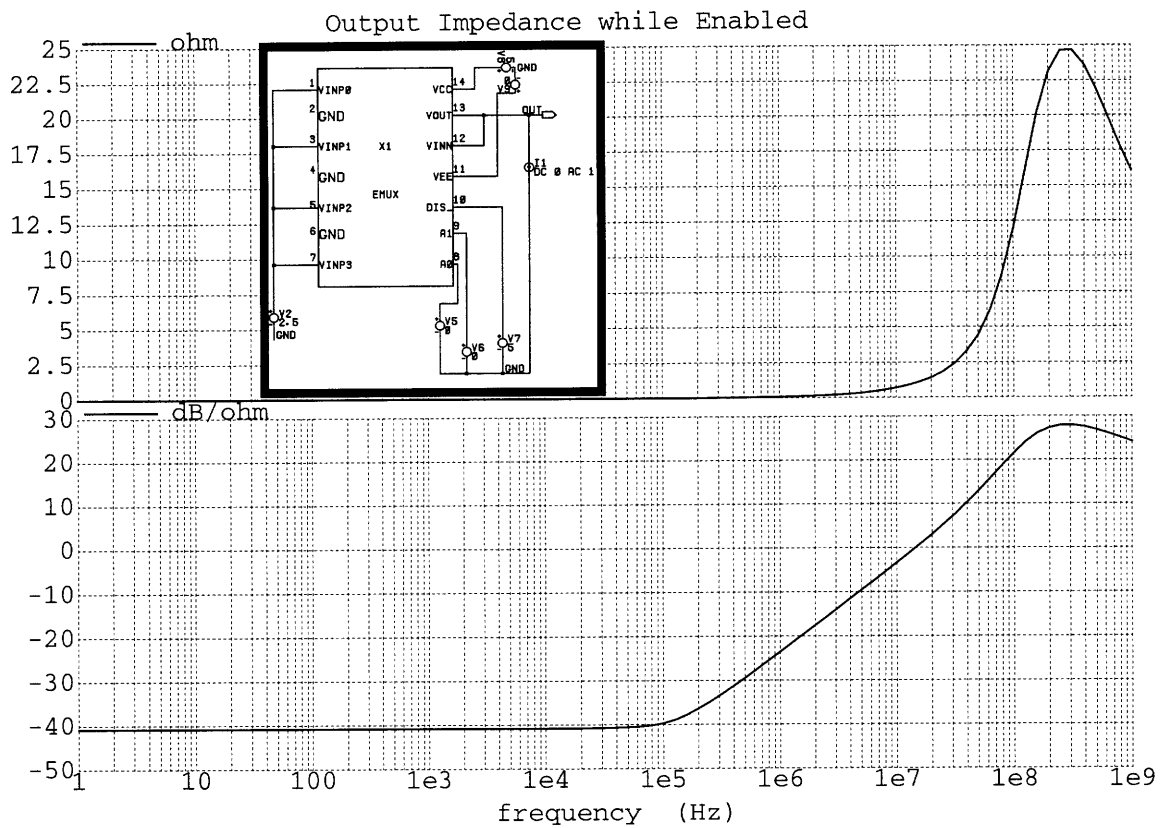


Figure 3.31 Output impedance of the MUX while enabled.

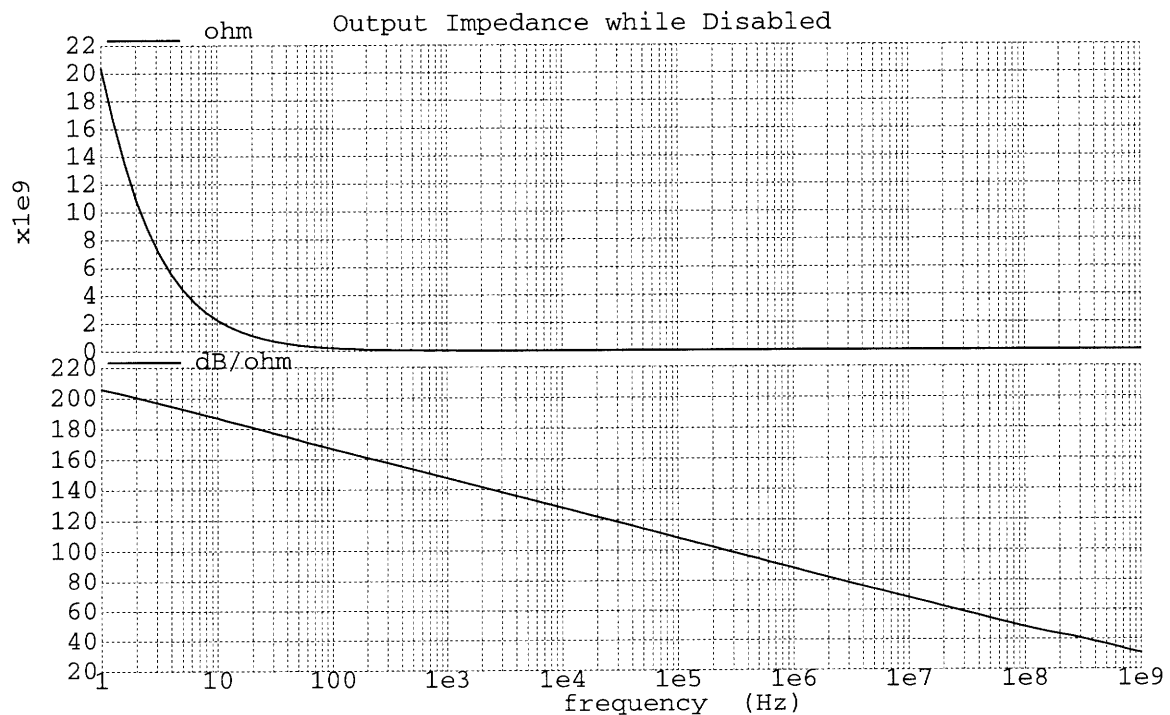


Figure 3.32 Output impedance of the MUX while disabled.

The total harmonic distortion (THD) is simulated in Figure 3.33. The first, second, third and fourth harmonics are -6.12 dB (0.494 V), -69 dB (3.55×10^{-4} V), -77.2 dB (1.38×10^{-4} V) and 106.9 dB (4.5×10^{-6} V) respectively. The THD is calculated below

$$THD = 20 \times \log \frac{\sqrt{(3.55 \times 10^{-4})^2 + (1.38 \times 10^{-4})^2 + (4.5 \times 10^{-6})^2}}{0.494} = -62dB \quad (3.17)$$

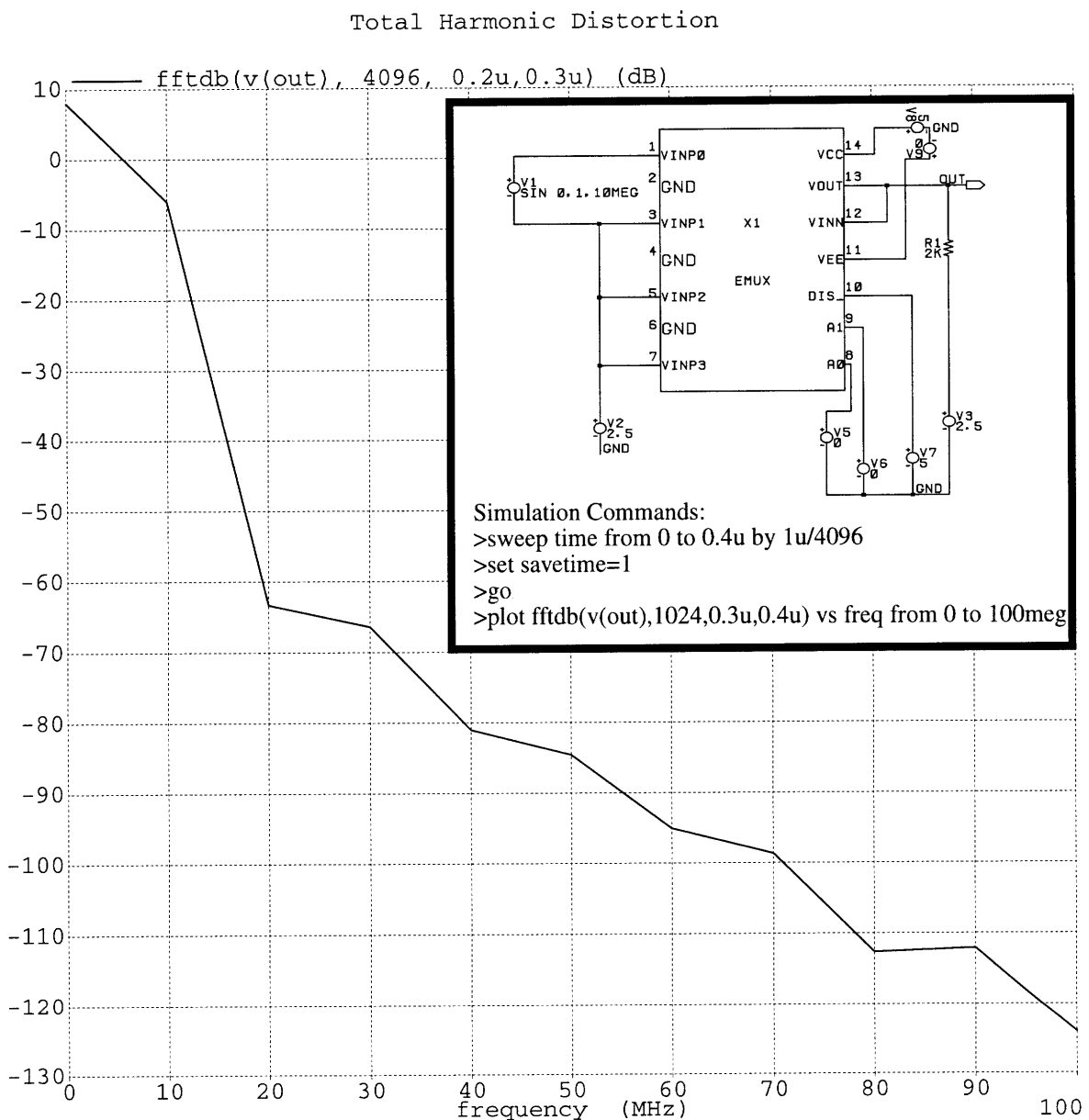


Figure 3.33 Total Harmonic Distortion.

4.0 Circuit Layout

4.1 Calculation of the Input Offset Voltage

One of the important aspects of the performance of a multiplexer is its input offset voltage. This parameter places the lowest limit on the values of DC voltage that can be accurately detected and amplified by the circuit. Offset voltage is a random parameter with a mean value that should usually be designed to be very near zero. The input offset voltage of the multiplexer can be shown to be primarily dependent on the offset voltage of the first stage, since the voltage gain of the first stage is reasonably high. This offset arises from randomly occurring mismatches between the device pairs making up the first stage of the multiplexer (including the input cell and first part of the amplifier cell), and is best described by a probability distribution with ideally zero mean and some standard deviation. The parameter of interest is the standard deviation of the offset voltage, which will dictate the limit one can place on the offset voltage of production units being tested while maintaining an acceptable yield. The information available at the design stage is the distribution of mismatches in resistor values. Transistor mismatch is of a secondary concern due to the level of degeneration and the expected V_{BE} mismatch.

A simplified first stage schematic diagram is shown in Figure 4.1. In this analysis we will simplify the problem by considering each device pair mismatch independently and superposing the results.

First consider a mismatch between Q_1 and Q_2 and between R_1 and R_2 . Assuming I_1 and I_2 are identical, we have

$$V_{OS1} + V_{EB1} + I_1 R_1 - I_2 R_2 - V_{EB2} = 0 \quad (4.1)$$

where V_{OS1} is the offset voltage, V_{EB} is the emitter-base voltage of a transistor. (4.1) leads

to

$$V_{OS1} = V_T \ln \frac{I_{S1}}{I_{S2}} + \frac{I}{2} \cdot (R_2 - R_1) = V_T \ln \left(1 + \frac{\Delta A}{A} \right) + \frac{I R_1}{2} \cdot \frac{\Delta R}{R_1} \quad (4.2)$$

where $\Delta A / A$ and $\Delta R / R_1$ are the fractional mismatch in the transistor areas A_1 and A_2 , and in the resistor values, R_1 and R_2 . Eqn. (4.2) can be further simplified and written as

$$V_{OS1} = V_T \left(\frac{\Delta A}{A} \right) + \frac{I R_1}{2} \cdot \frac{\Delta R}{R_1} \quad (4.3)$$

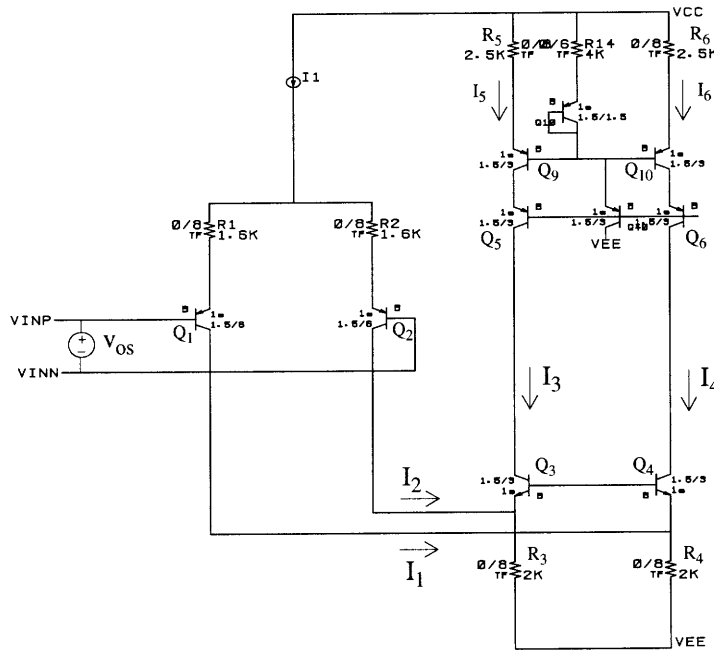


Figure 4.1 Circuit for input offset voltage calculation

Since V_{BE3} and V_{BE4} are well matched (1σ delta V_{BE} is 290 μ V for the given emitter size) [7], we only consider mismatches in R_3 and R_4 . The difference between R_3 and R_4 , ΔR , will require a difference in current $\Delta I = I_2 - I_1$, to make $I_3 = I_4$. The offset contribution of R_3 and R_4 is:

$$V_{OS2} = V_T \ln \left(\frac{I_2}{I_1} \right) + (I_2 - I_1) \cdot R_1 = V_T \ln \left(1 + \frac{\Delta I}{I_1} \right) + \Delta I \cdot R_1 \quad (4.4)$$

The following equation summing currents through R3 and R4 gives:

$$R_3 \cdot (I_2 + I_3) = R_4 \cdot (I_1 + I_4) \quad (4.5)$$

Now introducing $k = I_3 / I_1$, which is approximately 1.65, we have

$$[(1 + k) \cdot I_1 + \Delta I] \cdot R_3 = (1 + k) \cdot I_1 \cdot (R_3 + \Delta R) \quad (4.6)$$

Simplifying Eqn. (4.6), we have

$$\frac{\Delta I}{I_1} = \frac{(1 + k) \cdot \Delta R}{R_3} \quad (4.7)$$

and the substitution of (4.7) in (4.4) yields

$$V_{OS2} = (1 + k) \cdot (V_T + I_1 R_1) \cdot \frac{\Delta R}{R_3} \quad (4.8)$$

The final consideration is the mismatch between R₅ and R₆. We find

$$R_5 I_5 - V_{BE8} = R_6 I_6 - V_{BE10} \quad (4.9)$$

Assuming Q₉ and Q₁₀ match well, and $I_6 = I_5 + \Delta I$, then

$$\frac{\Delta I}{I_5} = \frac{\Delta R}{R_5} \quad (4.10)$$

and the offset voltage can be written as

$$V_{OS3} = V_T \left(\frac{\Delta I}{I_1} \right) + \Delta I \cdot R_1 = \frac{\Delta R}{R_5} \cdot I_5 \cdot \left(\frac{V_T}{I_1} + R_1 \right) \quad (4.11)$$

The total input offset voltage is then the sum of the three components:

$$V_{OS} = V_{OS1} + V_{OS2} + V_{OS3}$$

$$V_{OS} = \left[V_T \left(\frac{\Delta A}{A} \right) + \frac{I R_1}{2} \cdot \frac{\Delta R}{R_1} \right] + \left[(1+k) \cdot (V_T + I_1 R_1) \cdot \frac{\Delta R}{R_3} \right] + \left[\frac{\Delta R}{R_5} \cdot I_5 \cdot \left(\frac{V_T}{I_1} + R_1 \right) \right] \quad (4.12)$$

(1st term) (2nd term) (3rd term)

For a given set of mismatches, this expression will give the input offset voltage. However, the information of interest is the distribution of the observed offset voltages over a large number of samples. Assuming the mismatch factor $\Delta A / A$ is negligible compared with $\Delta R / R$, if each of the distributions of the mismatch factors $\Delta R / R_1$, $\Delta R / R_3$, and $\Delta R / R_5$ is regarded as an independent random variable with normal distribution, then the standard deviation of the distribution for V_{OS} is calculated by taking the square root of the sum of the squares of the individual contributions.

The standard deviation in the distribution of thin film resistor matching in the XF1.5 process is resistor-length and resistor-width dependent, and in general, resistor-width matches much better than length. Thus we have $\Delta R = \Delta L(R_{\text{square}} / W)$, and its value is 0.44% for our resistors [8]. We obtain, with $I = 192 \text{ uA}$, $R_1 = 1.6 \text{ K}\Omega$, $V_T = 26 \text{ mV}$, $I_1 = 96 \text{ uA}$, $k = 1.646$, $I_5 = 62 \text{ uA}$

$$\sigma_{V_{OS}} = \sqrt{(0.722)^2 + (2.079)^2 + (0.463)^2} \cdot 10^{-3} \text{ V} = 2.248 \text{ mV} \quad (4.13)$$

(1st term) (2nd term) (3rd term)

Terms in Eqn. (4.12) and Eqn. (4.13) correspond to each other. The largest single offset contribution is thus the mismatch in the resistors R_3 and R_4 (shown as the second term in Eqn. (4.13)).

4.2 Techniques for Minimizing the Input Offset Voltage

To minimize the input offset voltage, several design techniques are applied at the circuit layout level. The schematic of each cell has been drawn to highlight these layout techniques. As shown in Section 4.1, there are three major contributors to the input offset voltage -- the mismatch between R_1 and R_2 , between R_3 and R_4 , and between R_5 and R_6 , seen in Figure 4.1. Equation (4.13) shows that the largest single offset contribution is the mismatch between R_3 and R_4 . A basic objective in the design of the multiplexer is the minimization of the mismatch between those resistors and input devices.

The observed random distribution of the mismatches between two nominally identical resistors or transistors is primarily the result of two factors. One of those factors is the variation in the location of the edges of the resistor or transistor resulting from the limited resolution of the photolithographic process itself. The second factor is the variations in sheet resistance and junction depth of the implanted and diffused regions across the wafer resulting from nonuniform conditions during the predeposition and / or diffusion of the impurities. This causes resistance and transistor parameters to vary with distance across the die. Since the photolithographic resolution limits the attainable matching, using resistors or transistors with geometries which are large in comparison with the resolution becomes an important step. A fixed amount of edge location uncertainty will have less effect on a wider and longer resistor than on a smaller resistor, so matching will improve. Similarly, the matching of I_S observed in bipolar transistors improves as the emitter size is made larger. The process-related gradients across the die can be partially alleviated by the use of appropriate geometries which cause the device mismatch to be insensitive to the process gradients.

In agreement with the above arguments, the input transistors and resistor pairs of the input stage are resized to overcome the resolution limitation, and a common centroid geometry is employed by several resistor pairs to tolerate process gradients. As shown in Figure 3.8, the input cell's transistors Q_{13} , Q_{17} , Q_{43} and Q_{46} are all resized from $1.5 \text{ } \mu\text{m} / 6 \text{ } \mu\text{m}$ to $1 \text{ } \mu\text{m} / 9 \text{ } \mu\text{m}$ (width / length) to improve their R_b 's. The resistors' length stays the same, their width is cut in half, and the number of resistors is doubled, so that the total area occupied by the resistors is not changed, but the matching is improved. Since the standard deviation of the resistor width is much smaller than that of the length, cutting resistors' width in half will not have much effect on the matching (assuming the width is still larger than the minimum). To keep the length the same, the resistor value needs to be doubled, requiring another identical resistor to be put in parallel with it to maintain the original resistance in the circuit. This allows us to replace the resistor pairs with the cross-connected segments of a quad of resistors. In a geometric sense, the centroid of both composite devices lies at the center of the structure. In Figure 3.8, resistor pairs R_{15} and R_2 are changed into $R_{15} // R_6$ and $R_2 // R_7$, and their dimensions are changed from $8 \text{ } \mu\text{m}$ wide by $12.8 \text{ } \mu\text{m}$ long to $4 \text{ } \mu\text{m}$ wide by $12.8 \text{ } \mu\text{m}$ long. Thus the mismatch due to process gradients is minimized while the overall area is kept unchanged. A similar technique is applied to resistor pairs $R_5 // R_1$ and $R_{21} // R_4$, as well as to resistor pairs $R_{17} // R_{62}$ and $R_9 // R_1$ in Figure 3.18 of the amplifier cell. The improved input offset voltage is calculated to be around 1.8 mV .

4.3 Technique for Improving the Current Mirror's Accuracy

Base to emitter voltage matching is critical for those current mirrors whose emitters are not degenerated. Since XF1.5 process's minimum width Metal1 and Metal2 wires

are narrow, their resistances are relatively high. Metal1 has a sheet resistance of $48 \text{ m}\Omega/\text{square}$, and Metal2's sheet resistance is $31 \text{ m}\Omega/\text{square}$. As shown on the left of Figure 4.2, if the power supply is directly connected to the emitters of the current mirror, the modeled wiring resistance R between two emitters will become important since it might introduce offset to V_{BE} matching which in turn will affect the mirrored current. A simple calculation shows that it takes about 51 squares of Metal1 (approximately 2.5Ω) to offset the mirrored current by 10% if this metal wire is also part of the supply line and holds a nominal current of 1 mA.

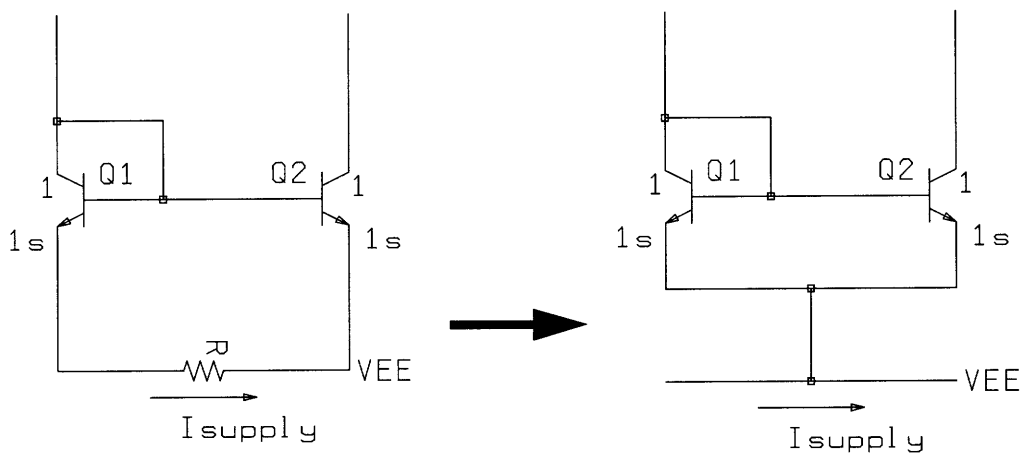


Figure 4.2 Method for improving the current mirror's precision.

One way to improve the precision of this type of current mirror is to lay out the circuit as shown on the right of Figure 4.2. By tying Q_1 and Q_2 's emitters together before connecting them to the power supply, the supply current flowing to other parts of the circuit will no longer flow between Q_1 and Q_2 's emitters. Thus the offset voltage introduced by the metal wire is minimized and the collector current of Q_1 is precisely mirrored to Q_2 . This layout technique is applied to the current mirrors Q_{25}/Q_{50} and Q_{24}/Q_{47} of the ampli-

fier cell seen in Figure 3.19, and to the NPO current generator Q_{44}/Q_{61} of the biasing cell seen in Figure 3.2.

The same idea is applied to improve the resistors' match in the input cell seen in Figure 3.9 where R_1/R_4 are tied together before connecting to the negative supply. This layout can also be found in the amplifier cell seen in Figure 3.19 where R_{17}/R_9 are joined before they are connected to the positive supply.

Finally, since nearly 75% of the supply current of the amplifier is dissipated at the output stage, the power supplies of the rest of the amplifier cell have been separated from the power supplies of the output stage so that they do not need to carry the large load current of the output devices during the normal operation, and the disturbance due to the activities at the output stage is minimized.

4.4 Device Sizing and Layout Arrangement

Devices are sized to optimize the circuit performance while using the least amount of area possible. Section 4.2 describes one of the sizing strategies where resistor pairs are sized to improve their matching without consuming any extra area. This section discusses several other strategies adopted in the design.

Typically, the larger the components in value and in chip area, the tighter the matching will be. Hence, high precision and small chip area are often conflicting objectives and trade-offs must be considered. As shown in the biasing cell (Figure 3.2), the decoder cell (Figure 3.5), and the amplifier cell (Figure 3.19), the current sources of the logic circuit and the current sources of the amplifier are sized to be $1.5 \text{ um} / 3 \text{ um}$ (W/L), 4.5 times the minimum size $1 \text{ um} / 1 \text{ um}$, and all the current sources' transistors are

located in close proximity on the chip. This allows transistors to track closely and minimize the variations during the fabrication process. In the decoder cell, resistors $R_{27}/R_{28}/R_1/R_2/R_8/R_{11}/R_{29}/R_{30}$ are all of the same size and placed close to each other for better matching, so that the sourced current from the decoder will be consistent from channel to channel.

As discussed in Section 3.5 (see Figure 3.19), transistors Q_3 and Q_6 are used to prevent Q_{50} and Q_{47} from getting into saturation in disable mode. Since the emitters of Q_{50} and Q_{47} are fixed to the power supply, and their collector voltages are equal to one V_{EB} above the disable voltage V_{DP} and V_{DN} , a small V_{EB} is desirable for Q_3 and Q_6 to keep Q_{50} and Q_{47} away from saturation. The base-emitter voltage of Q_3 and Q_6 is

$$V_{EB} = |V_{BE}| = V_T \cdot \ln \frac{I_C}{I_S} \quad (4.14)$$

where I_S is proportional to the emitter area. For a given I_C , a larger transistor will have a smaller V_{EB} , but because of the logarithmic relationship between V_{EB} and $1/I_S$, the impact of the area on the value of V_{EB} is not great. Trade-offs need to be made between the size of the transistor and the value of the V_{EB} . As illustrated in Figure 3.19, the amplifier design chooses to size both Q_3 and Q_6 to be $1.5 \text{ } \mu\text{m} / 12 \text{ } \mu\text{m}$, achieving a V_{EB} of 780 mV and allowing 250 mV of emitter-collector voltage for both Q_{50} and Q_{47} .

From the discussion in Section 2.3, we know that the NPO bias circuit of the bias cell generates temperature independent bias currents for the entire multiplexer. To ensure this NPO circuit's accuracy, a very long resistor (200 squares, $25 \text{ K}\Omega$) has been divided into three resistors -- R_{33} ($10 \text{ K}\Omega$), R_{37} ($10 \text{ K}\Omega$), and R_{38} ($5 \text{ K}\Omega$), so that the resistance

can be cleanly defined. A long transistor (24 μm in length) is also cut into four smaller ones, each having a length of 6 μm . They are also quadded for better matching.

All input pins and the output pin of the multiplexer (VINP0 ~ VINP3, VINN, A0, A1, DIS_ and VOUT) are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. The logic inputs A0, A1 and DIS_'s ESD devices are connected to the positive power supply and ground. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7 V, as may occur with loss of the multiplexer's power supplies while signal source is still present. Between the logic input pin (eg. A0, A1 and DIS_) and the input transistor, a 1 $\text{K}\Omega$ resistor is inserted to protect the input transistors' base-collector junction from strongly forward biasing during an ESD event, in which case current will go through ESD diodes rather than the B-C junction.

5.0 Conclusion

A single supply wide bandwidth 4:1 video multiplexer implemented in an 8 GHz dielectrically isolated complementary bipolar process has been designed and simulated. Its fast switching speed, small switching glitch, high crosstalk rejection, and high input-to-output isolation make it very competitive against other leading products in the video switch market. Its low quiescent power also makes it well suited to portable and battery powered applications.

This switched transconductance amplifier 4:1 analog multiplexer is compact in size. The circuit layout shows that its die size is 844 μm by 872 μm . A file which contains all the parasitic capacitances associated with the circuit was extracted from the layout. It was then attached to the original multiplexer's schematic and all circuit performances were resimulated. Most of the simulations were confirmed as be consistent with previous results. However, the crosstalk rejection was found to vary from channel to channel. A thorough study of the parasitic capacitors attached to all four input nodes showed that the problem was due to the capacitive couplings between the unselected input channel and the emitters of the input PNP transistor pair (Q_{13} / Q_{17}) of the selected channel. After rerouting the input wire and eliminating those capacitive couplings, as shown in Figure 5.1, the crosstalk rejection became uniform for all four input channels.

Work could be continued on this thesis in a number of areas. First, in addition to the previously discussed parasitic file extracted from the circuit layout, a simulation pack-

age consisting of the parasitic resistances, capacitances and inductances associated with each of the fourteen pins of the 4:1 multiplexer could be designed and attached to the original schematic. The simulation results on parameters such as CMRR and PSRR will then be more realistic than those simulated without the package.

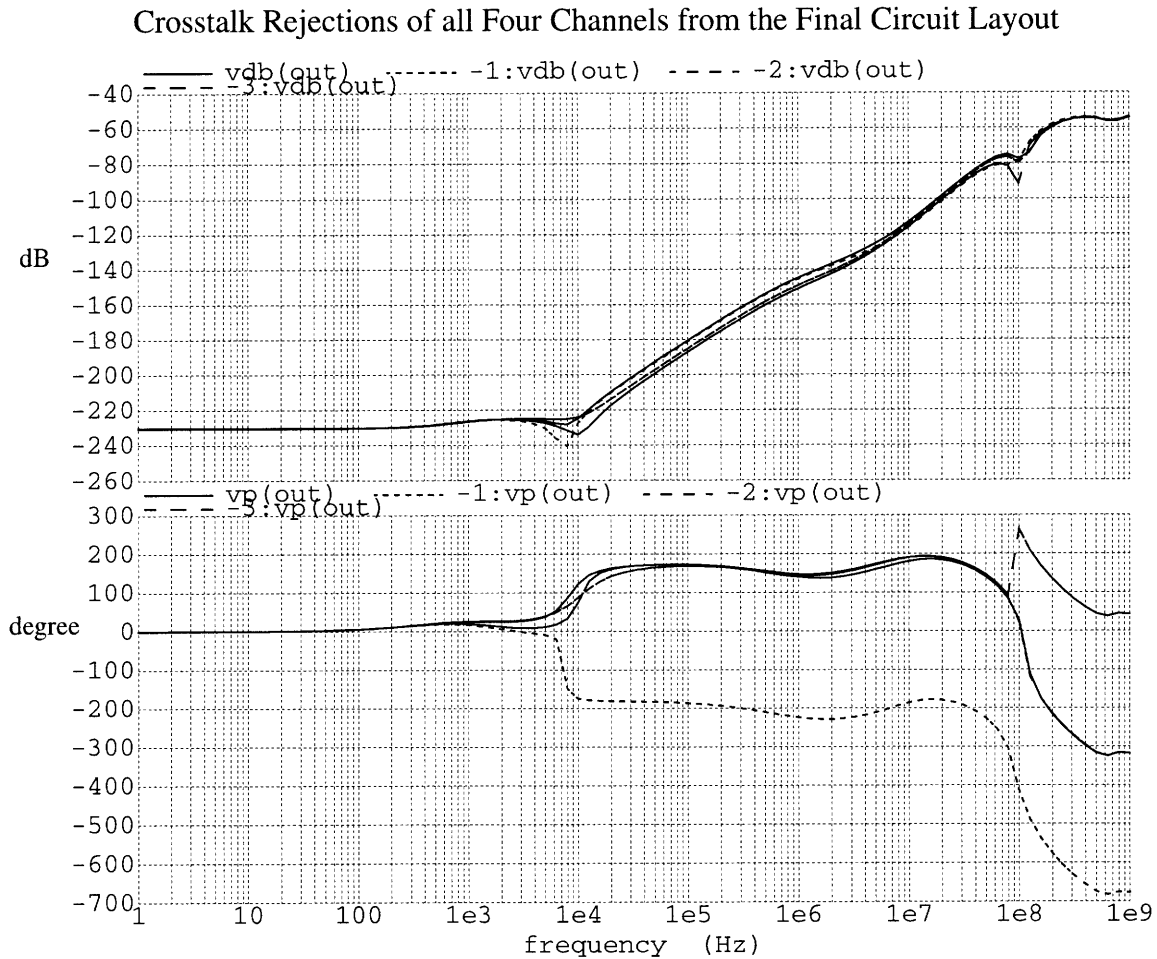


Figure 5.1 Magnitude and phase of the crosstalk rejection of each input channel from the circuit layout.

A second facet of the work that needs to be continued is the chip fabrication and debugging / characterizing of the resulting wafer. Since the entire circuit layout has been completed and its functionality has been verified, this multiplexer design is ready to be sent for manufacturing at any time. Our multiplexer chip can easily reuse the AD8174's

circuit board for its lab testing because its pinout arrangement is very similar to the AD8174's. These remaining tasks that need to be accomplished in order to make this video multiplexer a reality are challenging, yet will be ultimately rewarding.

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