Miniaturizing Microvias for Multi-Chip Modules

by

Paul Gerard Puskarich

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

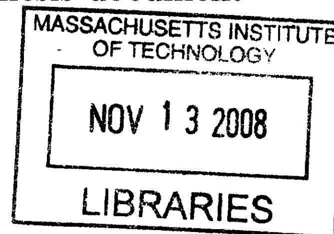
Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2008

© Paul Gerard Puskarich, MMVIII. All rights reserved.
The author hereby grants to MIT permission to reproduce and distribute publicly paper and electronic copies of this thesis document in whole or in part.



Author ....
Department of Electrical Engineering and Computer Science
May 23, 2008

Certified by ....
John J. Le Blanc
Principal Member Technical Staff, Draper Laboratory
Thesis Supervisor

Certified by ....
Thomas W. Eagar
Professor of Materials Engineering and Engineering Systems, MIT
Thesis Supervisor

Accepted by ....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

ARCHIVES

Miniaturizing Microvias for Multi-Chip Modules

by

Paul Gerard Puskarich

Submitted to the Department of Electrical Engineering and Computer Science
on May 23, 2008, in partial fulfillment of the
requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science

Abstract

Electronics packaging is continually migrating toward denser packaging. This encompasses a push toward multilevel die, denser metallization, and smaller microvias. In this thesis we investigate the miniaturization of laser-drilled microvias in polyimide dielectric for chips-first multi-chip module (MCM) technology. The challenge is to produce increasingly smaller microvias and package more microvias into a given area without sacrificing electrical performance. Principally, this means a microvia must maintain certain minimum electrical resistance and mechanical adhesion to the conducting layers. The thesis encompasses the following research:

1. Investigating the state of the art in laser-drilled polyimide microvias.
2. Designing and fabricating test structures with microvias, in which the state of the art is pushed in microvia size and/or aspect ratio.
3. Measuring the contact resistances of laser-drilled microvias in a Kelvin structure configuration.
4. Developing finite element models of Kelvin structures to estimate the contact resistance of miniature microvias.

The experimental results of this thesis prove that microvias with approximately 19 μm diameter and 10 mΩ contact resistance can be reliably fabricated for chips-first MCM technology.

Thesis Supervisor: John J. Le Blanc
Title: Principal Member Technical Staff, Draper Laboratory

Thesis Supervisor: Thomas W. Eagar
Title: Professor of Materials Engineering and Engineering Systems, MIT

Acknowledgments

For their contribution to the success of this thesis, I thank my supervisors, John Le Blanc and Professor Thomas Eagar, as well as my colleagues at Draper Laboratory: Andrew Mueller, Michael Holm, Caroline Bjune, Wenbi Lai, Ed Judd, and Antonio Montiero. Their guidance and support over the past year has been invaluable.

This thesis was prepared at The Charles Stark Draper Laboratory, Inc., under Independent Research & Development Contract 21810-001.

Publication of this thesis does not constitute approval by Draper or the sponsoring agency of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

Permission is hereby granted to the Massachusetts Institute of Technology to reproduce any or all of this thesis.

Paul Puskarich

Contents

1 Introduction **15**

1.1 Multi-chip modules 15

1.2 Miniaturizing microvias for MCMs 16

1.2.1 Research scope 17

1.2.2 Thesis outline 17

2 Multi-Chip Modules **19**

2.1 Advantages of MCM technology 20

2.2 Disadvantages of MCM technology 21

2.3 Types of MCM technology 21

2.3.1 MCM-D 21

3 Microvias **27**

3.1 Categories of vias 27

3.2 Definition of structure 29

3.3 Draper's microvia challenges 29

3.3.1 Technology roadmap 30

4 Microvia Analysis and Test Results **33**

4.1 Experimental plan for miniaturizing microvias 33

4.1.1 Design of test vehicles 34

4.2 Microvia formation 35

4.2.1 Oxide back-etch results 35

4.2.2 Cross-sections 37
4.3 Contact resistance 44
4.3.1 Measurement using Kelvin structures 44
4.3.2 Thermal shock cycling 47

5 Finite Element Modeling **51**
5.1 Microvia model geometry 52
5.2 FEM parameters 52
5.3 Contact resistance results 54
5.3.1 Comparative analysis 58

6 Conclusion **61**
6.1 Contribution of research 62

List of Figures

1-1 Cutaway view of (a) an IC package and (b) an MCM. (Not to scale) . 16

1-2 Cross-section view of (a) an MCM and (b) microvias within the HDI. (Not to scale) 16

2-1 A complete MCM package [1]. 20

2-2 Bare ICs placed within an example MCM by Draper Laboratory [9]. . 23

2-3 First level lamination with windowpane [9]. 24

3-1 Cross-section of a typical metallized via. 28

3-2 Three categories of vias: blind, buried, and through-hole. 28

3-3 General microvia structure and definitions. Courtesy of Draper Laboratory. 29

4-1 Microscope images of (a) the top of a 34 μm laser-drilled hole and (b) the bottom of the whole, showing the silicon oxide before back-etching. 36

4-2 Thickness of SiO_2 oxide as a function of laser aperture. 37

4-3 Standard process microvias (5 μm copper plating, 12.5 μm polyimide adhesive) created with different laser aperture diameters. 38

4-4 Ext-A Microvias. 10 μm copper plating; 12.5 μm adhesive; laser apertures 14 μm, 18 μm, 24 μm, 34 μm. 39

4-5 Ext-B Microvias. 5 μm copper plating; 7 μm adhesive; laser apertures 14 μm, 18 μm, 24 μm, 34 μm. 40

4-6 Ext-C Microvias. 10 μm copper plating; 7 μm adhesive; laser apertures 14 μm, 18 μm, 24 μm, 34 μm. 41

4-7 Ext-D Microvias. 5 μm copper plating; 4 μm adhesive; aser apertures 14 μm, 18 μm, 24 μm, 34 μm. 42

4-8 Kelvin structure for monitoring the contact resistance of microvias. (a) Model for the setup of the four-probe measurement. (b) Magnified image of an actual Kelvin structure used in the test vehicles. 45

4-9 Kelvin structure measurements for the four test vehicles. The die-level measurements for the 14 μm and 18 μm microvias are absent because the values were greater than 20 mΩ, and thus the microvias were rejected as failures. 46

4-10 Kelvin structure measurements for test vehicle Ext-A taken during thermal shock analysis. 49

4-11 Kelvin structure measurements for Ext-B taken during thermal shock analysis. 49

4-12 Kelvin structure measurements for Ext-C taken during thermal shock analysis. 50

4-13 Kelvin structure measurements for Ext-D taken during thermal shock analysis. 50

5-1 CAD drawing of a Kelvin structure for finite element analysis. 51

5-2 Magnified view of a microvia cross-section and its corresponding CAD drawing to be modeled. 52

5-3 Mesh elements of a Kelvin structure generated using finite element analysis. 53

5-4 Electric potential gradient of Kelvin structure modeled using finite element analysis. 54

5-5 Finite element model of contact resistance as a function of laser aperture for Ext-A. The die-level measurements for the 14 μm and 18 μm microvias are absent because the values were greater than 20 mΩ, and thus the microvias were rejected as failures. 56

5-6 Finite element model of contact resistance as a function of laser aperture for Ext-B. 56
5-7 Finite element model of contact resistance as a function of laser aperture for Ext-C. 57
5-8 Finite element model of contact resistance as a function of laser aperture for Ext-D. 57
5-9 Finite element model contact resistance as a function of aluminum test die thickness for test vehicle Ext-D. 59

List of Tables

3.1 International Technology Roadmap for Semiconductors — Near-term Years, 2006. 31

4.1 Draper Laboratory microvia dimensions. 34

4.2 Test vehicle parameters. 34

4.3 Microvia Diameter Measurements (μm) 43

5.1 Measured and modeled contact resistance values for die-level and upper-level microvias. 55

Chapter 1

Introduction

The electronics industry continuously demands smaller, lighter, faster, and lower cost packaging. Electronics packages are expected to accommodate several integrated circuits (ICs) with high I/O pin counts and fine pitch die pads, all within a minimal footprint. The progression of the multi-chip module (MCM) industry is fueled by the need for package size reduction and for increased complexity.

1.1 Multi-chip modules

MCMs are the next stage of evolution for microelectronics packages. A typical electronics package contains a single silicon chip, while an MCM contains multiple chips, as shown in Figure 1-1. An MCM is a specialized electronic package where multiple ICs, semiconductor dies, and other modules are packaged in such a way as to facilitate their use as a single surface mounted device.

On the MCMs studied for this research, the IC dies are connected to each other through a High Density Interconnect (HDI) layer. HDI is typically comprised of several layers of conducting materials (that consist of the signal, power, and ground connections), separated by dielectric material, glued together by adhesive, and connected by microvias, as illustrated in Figure 1-2. The advancement of MCM technology encompasses a push toward multilevel dies, denser metallization, and smaller microvias. Miniaturizing microvias is the main focus of this thesis.

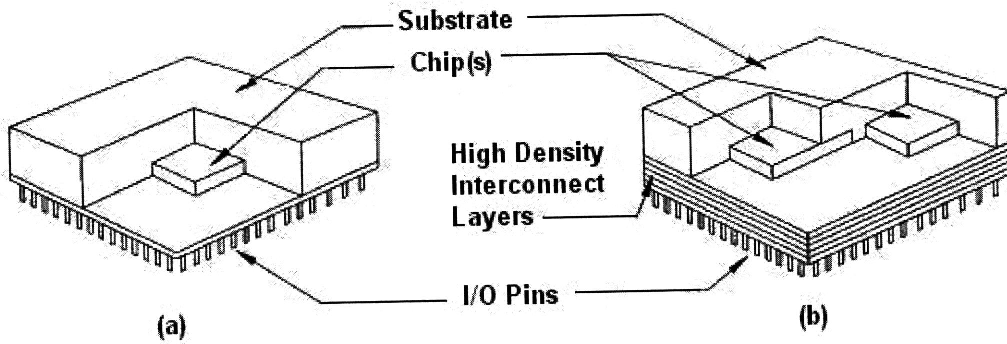


Figure 1-1: Cutaway view of (a) an IC package and (b) an MCM. (Not to scale)

1.2 Miniaturizing microvias for MCMs

A laser-drilled microvia is a critical MCM structure that allows for high density routing between different conduction layers in a package. Microvias are a principal feature of MCMs, along with thin dielectrics and interconnect lines and spaces. Microvias, in general, can be formed by various processes, including photolithography, photodefining dielectrics, reactive ion etching, and laser ablation. The laser-drilled microvias that this thesis studies are fully defined using laser laser drilling, metallization, photolithography, and etching.

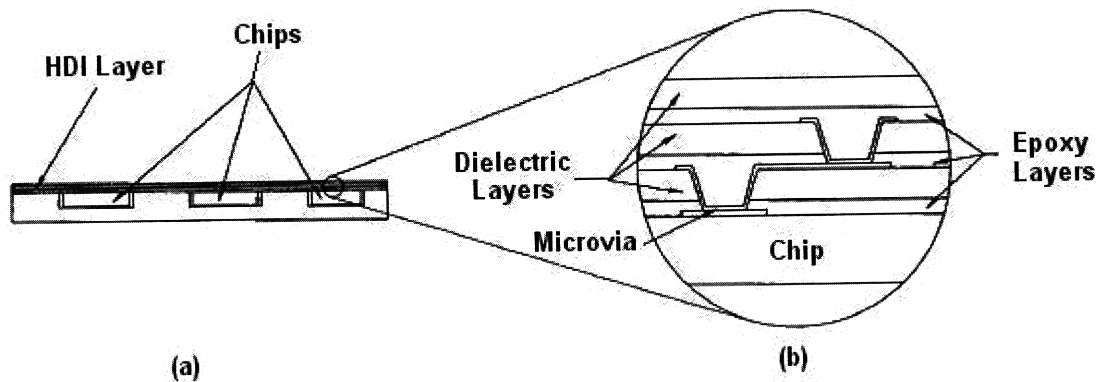


Figure 1-2: Cross-section view of (a) an MCM and (b) microvias within the HDI. (Not to scale)

1.2.1 Research scope

This thesis will look at miniaturization of laser-drilled microvias in polyimide dielectric for chips-first MCM technology. This thesis will describe why smaller microvias are a priority for MCMs and then present a plan to develop smaller microvias, focusing on via formation and electrical performance.

1.2.2 Thesis outline

Chapter 2 introduces MCM technology and the projected direction of the MCM industry. Chapter 3 presents microvias, their role in MCM packages, their fabrication process, and Draper Laboratory's motivations for miniaturizing them. Chapter 4 describes the plan for testing smaller microvias and analyzes the microvias for electrical performance and mechanical adhesion. Chapter 5 presents results from finite element models that were created to determine the contact resistances of microvias in a Kelvin structure configuration and compares the modeled values to the measured values from Chapter 4. Chapter 6 concludes the experimental results and finite element analysis and proposes the future direction of microvias for Draper Laboratory.

Chapter 2

Multi-Chip Modules

A multi-chip module (MCM) is a single electronics package that encloses multiple integrated circuits (ICs). Multi-chip packaging of bare (unpackaged) ICs represents a rapidly growing technology that is revolutionizing the electronics industry. MCM technology replaces the discrete packaging of individual IC elements, which are much larger than the dies they enclose, with monolithic structures that interconnect two or more bare dies. Eliminating separate IC chip packages can achieve a 5-to-1 to 10-to-1 reduction in substrate area [2].

Within the MCM package, silicon dies containing ICs may be stacked vertically on a ceramic or silicon substrate and separated by layers of dielectric; the dies are internally connected by fine wires that are buried in the package. A single MCM can contain several IC chips (e.g., specialized processor, DRAM, flash memory, etc.) combined with passive components (e.g., resistors and capacitors) all mounted on the same substrate base. A complete MCM can perform all or most of the functions of an electronic system, such as the ones used in handheld devices. The MCM can then be mounted on a PCB in the same way as any other surface mounted device. Figure 2-1 depicts how compactly an MCM can be assembled. This is particularly valuable in space-constrained environments like handheld devices as it reduces the complexity of the PCB and overall design.

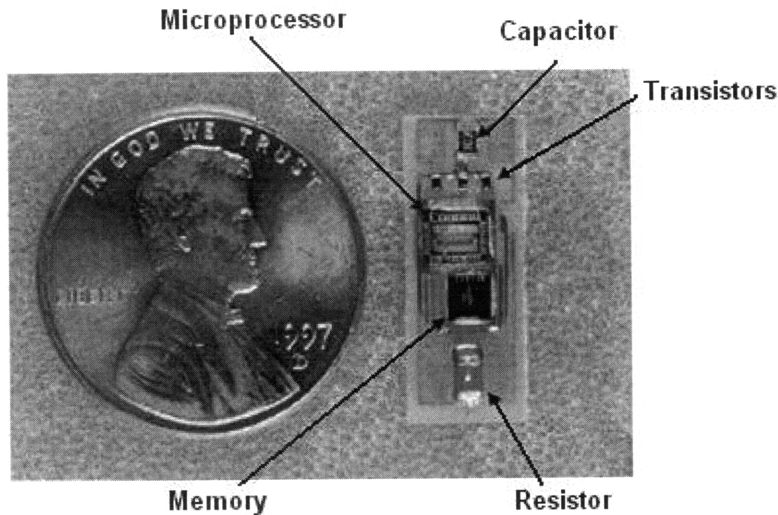


Figure 2-1: A complete MCM package [1].

2.1 Advantages of MCM technology

MCM technology offers numerous advantages over mounting individually packaged components directly onto the PCB. Removing individual dies from their packages allows for shorter interconnect distances and for the dies to be placed closer to each other, thereby allowing for considerable reduction in overall size and weight. Also, shorter interconnects between dies allow for better electrical properties, and the impedance of the system is easier to control. There is also a reduction in power supply inductance, capacitance loading, cross talk, power consumption, and power loss.

Further advantages of MCM technologies arise from using a smaller system. Since MCMs result in a smaller overall package when compared to individually packaged components that perform the same function, the resulting I/O pin count to the system board is significantly reduced. Decreasing the number of interconnects between components and boards improves reliability.

MCMs are also advantageous for mixing analog and digital functions without serious limitations. Further, different IC technologies (e.g., GaAs, SiGe) can be integrated in the same package.

2.2 Disadvantages of MCM technology

Although there are many benefits of MCMs, there are also some drawbacks. The most important problem is the lack of availability of ICs in bare die form. Further, the sequential build-up technique that MCM manufacturers such as Draper employ decreases the yield of fabrication since any defective chip in the package will result in a non-functional MCM, even if all other dies in that same package are functional. There are also thermal drawbacks. Power dissipation in a confined module is an issue. Without individual die packages, a single MCM package has to be able to remove heat generated by all the ICs.

2.3 Types of MCM technology

MCMs are classified according to the technology used to create the HDI substrate. The three major technologies used to fabricate substrates for MCMs are MCM-L, composed of metal traces on stacked organic laminate sheets; MCM-C, metal patterned and interconnected on co-fired ceramic layers; and MCM-D, electroplated and patterned metal layers alternating sequentially with laminated dielectric thin films. Of the three MCM technologies, Draper Laboratory employs the MCM-D packaging process.

2.3.1 MCM-D

The combination of superior materials and thin film technology enables MCM-D to dominate other types of MCM as the clear leader in packaging density and circuit speed. Feature sizes can be smaller than 10 μm, which is an order of magnitude more than possible with either MCM-L or MCM-C [3]. The MCM-D fabrication processes are similar to those used in the manufacture of ICs in that all of the features are photolithographically defined.

In MCM-Ds, the conducting layers are deposited on a base substrate of usually ceramic but also silicon. The metal deposition is normally done by electroplating.

After the deposition process, the metallized surface is patterned by applying a photosensitive resist that, after exposing and developing, functions as an etch resist. All metal not covered by the resist is removed.

After the patterning of one layer, a dielectric coating can be applied. Microvia holes in the dielectric are opened by laser drilling and new layers can be added. For the dielectric, Draper Laboratory uses 12.5 μm DuPont™Kapton polyimide film. Spin-deposited polymers such as polyimide, and chemical vapordeposited silicon oxides, nitrides, and oxynitrides can also be used for dielectric. The conductors are usually electroplated copper, aluminum, or gold.

Generally, MCMs are assembled using a "chips last" approach in which the interconnect layer is created first (not necessarily high density), and then the dies are subsequently attached to the interconnect structure by wire bonding or flip chip attachment. Draper Laboratory practices an alternative assembly approach known as "chips first." In a chips-first design, the chips are placed first, before the HDI layer is deposited. Silicon chips are placed onto the substrate and held in place by adhesives. Each layer of the HDI is laid atop the chip and substrate.

This "chips first" approach was invented by General Electrics Corporate Research and Development (GE CR&D) [5] [6], and has subsequently been practiced by other organizations as well [7]. Draper practices the GE CR&D HDI process with a license agreement from Lockheed/Martin. There are, however, some distinct process variations practiced by Draper [8].

Die thinning

When building MCMs with a chips-first scheme, it is critical to ensure that the surfaces of all the dies are at the same level. As commercial dies come in a variety of thicknesses, we begin our process by thinning the dies to 150 μm. The thinning of dies is a mechanical grinding process, done using Logitec PM2a Precision Lapping and Polishing Equipment. The thinning is done using a coarse grit for removing most of the silicon and a fine grit to minimize polishing damage in the last 102 μm of removal. Thickness variations are $+/-3$ μm.

Die placement

Accurate die placement and the ability to maintain that placement accuracy are critical to the MCM process. The die attach must not allow the movement of dies during the placement and cure cycles or the laser drill computer files will not align to the dies later in the process.

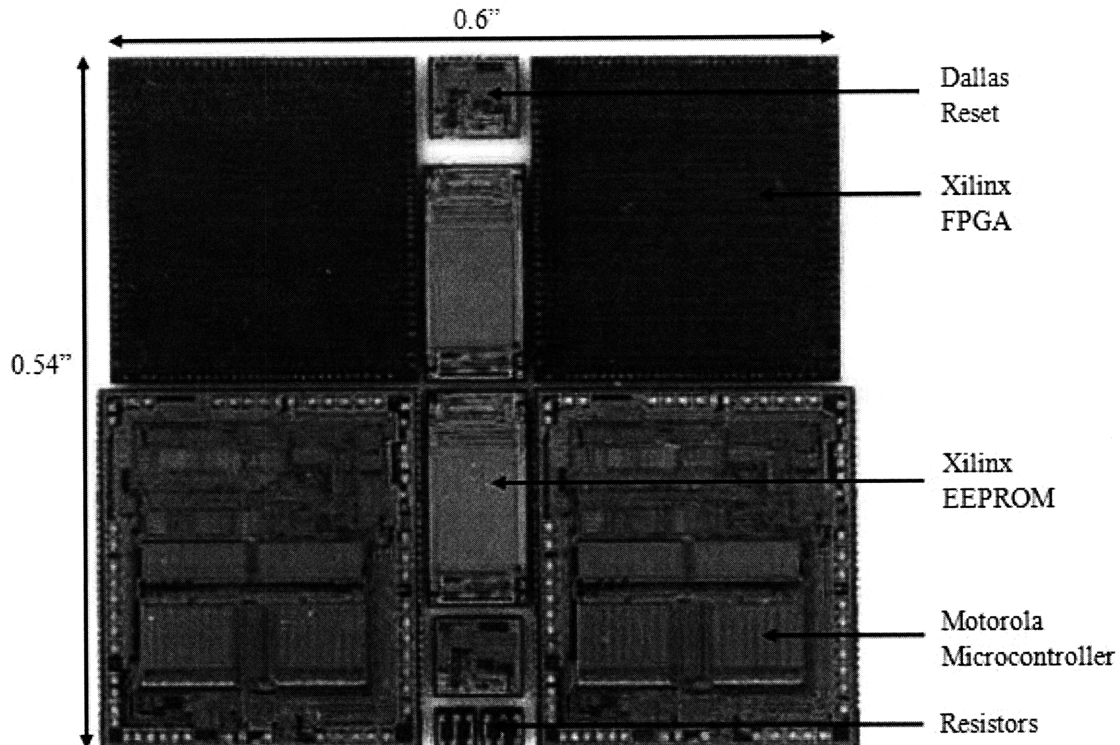


Figure 2-2: Bare ICs placed within an example MCM by Draper Laboratory [9].

Multiple modules are placed on a single substrate and diced out later in the process. To facilitate dicing, the dies are typically arranged to fit the minimum footprint in a rectangular box. Figure 2-2 shows a set of die for an MCM that have been placed and are ready for lamination.

First lamination

At this stage in the MCM assembly process, the surfaces of the dies are coplanar, as they are all thinned to the same thickness, but the entire module is not. From a sheet

of 130 μm Kapton HN that has been coated with 25 μm of the R/flex 1000 adhesive, a windowpane is cut which has an opening for all of the dies, with a 75 μm clearance around the dies [8]. This is then placed onto the substrate with the die protruding though the openings. The thickness of this windowpane matches the thickness of the die and gives the entire module a coplanar surface on which to build. A sheet of 12.5 μm Kapton HN coated with 12.5 μm R/flex 1000, which will serve as the first dielectric layer, is placed on top of the windowpane and die level. The entire stack is subsequently laminated together, as seen in Figure 2-3.

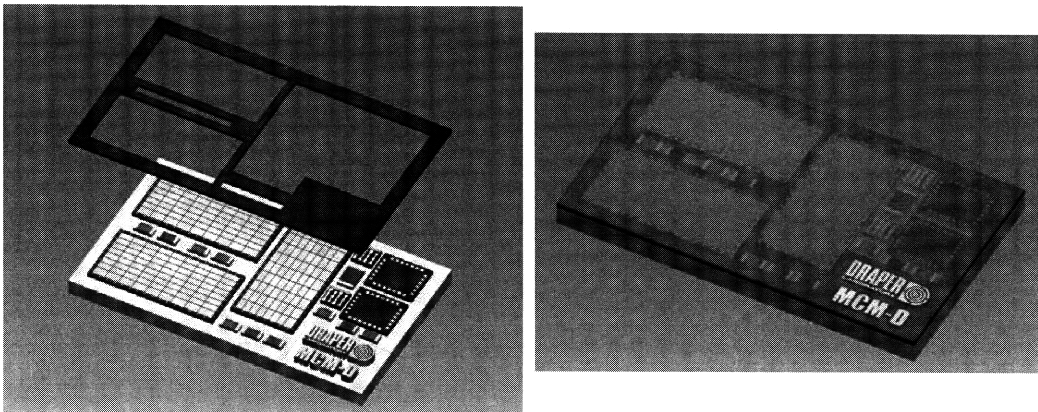


Figure 2-3: First level lamination with windowpane [9].

Microvia formation

Laser ablation drilling is a technique used to form holes in the dielectric for microvias. The inherent flexibility of the laser process makes it possible to control hole depth, diameter, and sidewall slope.

Microvias are formed by punching with multiple pulses, using enough laser power to remove dielectric, while not damaging the underlying die pad or capture pad. Because the dies are accurately placed, and the placement accuracy has been maintained through lamination, a simple alignment step is performed and holes are drilled in accordance with a CAD file of die pad coordinates. The resultant holes have a conical shape with a top width of 40 μm, tapering down to a bottom width of 30 μm.

The ablation process leaves behind a large amount of soot. Though much of this

can be washed away, an oxygen plasma cleaning step ensures the total removal of laser ablation soot. It is critical to remove all organic contamination from the bottom of the holes prior to metallization.

Metallization

The critical process in the metallization of the modules is the removal of the native oxide film on the die pads. The majority of integrated circuits have aluminum bond pads. Aluminum readily oxidizes and self-passivates. To remove the native oxide we use an argon back-etch. It is difficult to measure the amount of aluminum oxide that is removed as the oxide quickly reforms. Draper Laboratory routinely includes an oxidized Si wafer and measure the SiO_2 etch rate as a process metric.

The conductor metal is a Ti/Cu/Ti structure. The titanium layers act as both an adhesion enhancer and a diffusion barrier [10]. An initial plating seed layer is sputtered onto the modules, consisting of 1000 Å of titanium and 2000 Å of copper. Then, an additional 5 μm of copper is electroplated onto the modules in a copper sulfate plating bath. The structure is capped off with another 1000 Å of titanium.

The metal interconnect pattern is defined using standard semiconductor processes. Positive photoresist is spun onto the modules and a glass mask is aligned. Because the surface is relatively planar, 50 μm line widths are easily maintained.

Upper level interconnect

Upper level interconnect is fabricated by repeating the lamination, laser drilling, and metallization steps as described above. Typically, all interconnect traces are confined to the area directly above the die to allow for a minimum module area. Draper Laboratory presently builds modules with up to five levels of interconnect.

The configuration of the top layer is application specific, which may entail any of the following steps: soldering components on the surface, attaching solder-bumps to the module and flipping it into the next level of integration, or wire bonding from pad to pad.

Chapter 3

Microvias

The sequential buildup assembly technique is necessary to make high-density and cost-effective MCMs. Sequential buildup is done by adding a minimum of one layer of dielectric to the multi-layer core of an MCM package. A microvia, as drawn in Figure 3-1, is a metallized hole that goes through one of the dielectric layers on an MCM. According to the Institute for Interconnecting and Packaging Electronic Circuits (IPC), holes smaller than 150 μm in diameter on an MCM qualify to be called microvias. Plating the hole with copper creats a conductive path between circuits on different layers of an MCM. Microvias are dominating future generations of electronic products because they provide for increased density on a smaller substrate. Most of the products that use microvia technology are mobile phones, ASICs, notebook computers, and other handheld products.

3.1 Categories of vias

The three categories of vias for electronics packages, as illustrated in Figure 3-2 are the following:

1. *Blind vias* are located on the outer layer of the top and bottom of the circuit board and are formed to such a depth as to make contact with the first inner layer. The depth of these holes usually does not exceed one aspect ratio (hole diameter).

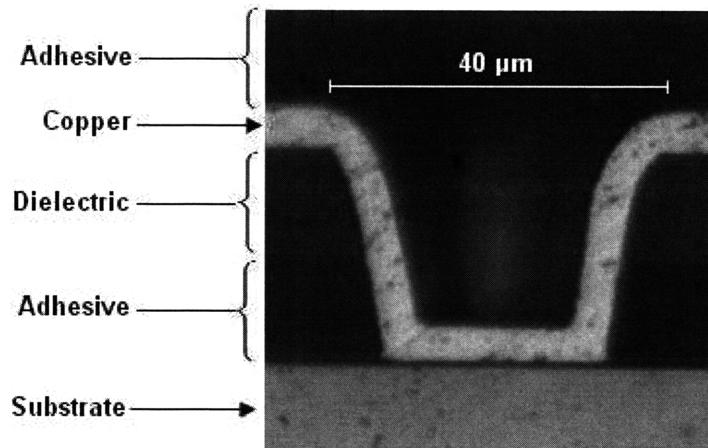


Figure 3-1: Cross-section of a typical metallized via.

2. *Buried vias* are plated within the core of the circuit board or MCM without access to the surface on either side of the board. These holes are formed before the board is laminated. The inner-layer material has the holes created by a through-hole processing method. The inner layers may be stacked several layers high during this hole-formation process.

3. *Through-hole vias* are formed though the entire thickness of the board. These vias are used as interconnects or as mounting locations for components.

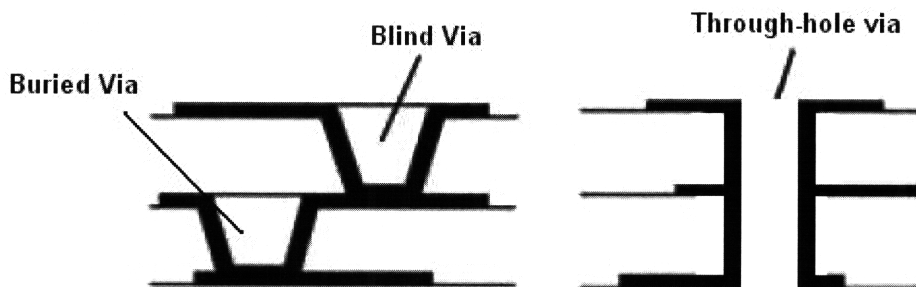


Figure 3-2: Three categories of vias: blind, buried, and through-hole.

This thesis focuses on blind and buried vias that are small enough (less than 150 μm diameter) to be referred to as microvias. Blind and buried microvias are formed to reclaim "real estate," to accommodate fine I/O pitch, to redistribute circuits

from the chip to the internal layers of the MCM, to reduce MCM layer count and size, and to enhance electrical performance.

3.2 Definition of structure

Figure 3-3 defines the general structure of microvias. Draper's working assumptions for microvias include the following: minimum bond pad spacing is 5 μm, minimum capture pad spacing is 12.5 μm, and the capture pad shall be bigger than the via top by 5 μm.

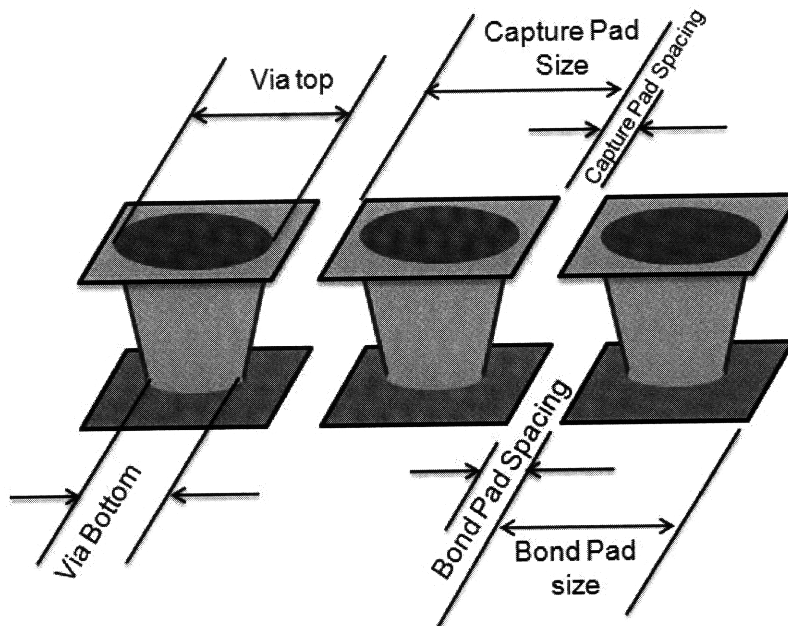


Figure 3-3: General microvia structure and definitions. Courtesy of Draper Laboratory.

3.3 Draper's microvia challenges

Draper's technical vision for the MCM-D process is to reduce the MCM interconnect geometry in order to connect to the I/O pins of new die and to keep pace with the International Technology Roadmap for Semiconductors. Increases in the total gates on new ICs require higher I/O pin counts as well as finer pin pitch. Also, faster

rise-times, as well as the need for signal integrity, require an increasing number of power and ground pins. These factors drive the need for more layers in multi-layer MCM packages, which in turn, drive the need for miniaturized microvias.

The many advantages to miniaturizing microvias include the following: (1) much smaller die pads can be used, saving on board size and weight; (2) more chips can be placed in less space or on a smaller MCM, which results in a low cost; and (3) electrical performance improves, because parasitic capacitance is increased due to smaller microvia length and diameter and inductance is reduced due to the shorter pathway created by the microvia, especially compared to a through-hole via. With these motivations, this thesis investigates reducing the diameter of laser-drilled microvias by more than fifty percent.

3.3.1 Technology roadmap

The International Technology Roadmap for Semiconductors (ITRS), which exists to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, forecasts the minimum microvia geometries for the upcoming generation of microelectronics. The die bond pads of the new memories and FPGAs are decreasing in size; therefore smaller diameter microvias are needed to access consecutive bond pads. A subset of the most recent ITRS predictions from 2006 are listed in Table 3.1.

The final row of Table 3.1 lists the maximum microvia top diameter and is formulated based on the ITRS forecast for die pad pitch. The calculation accounts for the pitch, subtracts 5 μm for assumed spacing between die pads, and subtracts another 5 μm to allow for the entire microvia to land on the die pad.

The ITRS roadmap and expectations for die pad size will be the driving forces in Draper's push for smaller vias.

Table 3.1: International Technology Roadmap for Semiconductors — Near-term Years, 2006.

ITRS Technology Roadmap	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*
Wire bond — single in-line (μm)	40	40	35	35	30	30	25
Two-row Staggered Pitch (μm)	50	45	45	40	40	35	35
Three-tier Pitch (μm)	55	50	50	45	45	40	40
Maximum Microvia Top Diameter (μm)	30	30	25	25	20	20	15

Chapter 4

Microvia Analysis and Test Results

Microvia contact resistance and reliability are highly important to electronic systems and devices. Typically several thousand microvias reside within one MCM, and there may be several MCMs within one electronic device, such as a computer or radar guidance system. If one of these thousands of microvias should happen to fail, then the entire system could potentially fail. Therefore, the reliability of an individual microvia must be extremely high.

This chapter details the plan for fabricating smaller microvias in Section 4.1 and then analyzes the test results in Section 4.2.

4.1 Experimental plan for miniaturizing microvias

Presently, Draper Laboratory can reliably fabricate microvias with top and bottom diameters of 40 μm and 30 μm, respectively; microvias with diameters of 30 μm and 20 μm have been fabricated experimentally, as listed in Table 4.1. The purpose of this thesis is to measure and to understand the electrical properties of microvias as the diameters are further reduced to 20 μm and smaller.

The challenge is to produce increasingly smaller microvias and to package more microvias into a given area without sacrificing electrical and mechanical performance. Principally, this means a microvia must maintain certain electrical resistance and mechanical adhesion to the next conducting layer. This research aims to assess the

Table 4.1: Draper Laboratory microvia dimensions.

	Top (μm)	Bottom (μm)	Aspect Ratio	Depth (μm)
Standard	40	30	0.7	25
Experimental	30	20	1	25
Proposed	20	10	Varied	Varied

viability of fabricating smaller microvias and to identify a combination of laser apertures, copper plating thickness, and dielectric adhesive thickness for achieving reliable microvia connections.

4.1.1 Design of test vehicles

To determine the viability of fabricating and using smaller microvias, four test vehicles were created and subjected to microvia diagnostics. Each test vehicle was comprised of Kelvin structures with varying parameters for microvia formation, as outlined in Table 4.2. The three process variables that we examined were the following: laser aperture diameter, polyimide adhesive thickness, and copper plating thickness.

Table 4.2: Test vehicle parameters.

Test vehicle	Laser aperture (μm)	Copper plating (μm)	Adhesive (μm)
Ext-A	14, 18, 24, 34	10	12.5
Ext-B		5	7
Ext-C		10	7
Ext-D		5	4

The standard process parameters for microvias fabricated at Draper Laboratory are as follows: 34 μm laser aperture, 5 μm copper plating, and 12.5 μm R/flex adhesive. For this research, microvias were laser-drilled on each test vehicle with aperture diameters of 14 μm, 18 μm, 24 μm, and 34 μm. Test vechicle Ext-A was laminated with the standard 12.5 μm R/flex adhesive, while the other test vehicles were laminated with thinned adhesive layers. Ext-B and Ext-C were laminated with 7 μm R/flex adhesive, and Ext-D was laminated with 4 μm R/flex adhesive. Ext-A

and Ext-C were plated with 10 μm copper, while Ext-B and Ext-D were plated with the standard 5 μm copper.

4.2 Microvia formation

In order to test the viability of the microvias in the four test vehicles, we monitor the microvias throughout their formation. First, experiments were done to investigate the oxide back-etch rate of small diameter, high aspect ratio microvias. Second, samples of miniature microvias were fabricated with standard process parameters and cross-sectioned to confirm suitable laser drilling and metallization steps. Next, the contact resistances of the Kelvin structures in the test vehicles were measured. Finally, the four test vehicles were subjected to liquid-to-liquid thermal shock cycling (-50°C to $+125$°C). After 1,000 thermal shocks, the test vehicles were cross-sectioned to reveal post-processing geometries and to search for possible failure modes.

4.2.1 Oxide back-etch results

For small microvias to suitably adhere to pads, an important step in the microvia formation process is the removal of all organic contamination from the bottom of the laser-drilled holes prior to metallization. Reactive ion etching with an oxygen plasma is used to remove organic contaminants after laser drilling.

Next, argon back-etching is used to remove the native oxide at the bottoms of the laser-drilled holes. The back-etch process to remove oxide is a 100 Watts RF Argon plasma at 3 mTorr. A Filmetrics F40 microscope-based measurement system was used to measure the thin film thickness of the oxide at the bottoms of the laser-drilled holes. Spectral analysis of reflections from the top and bottom of the oxide thin film provides the thickness.

Experiments were conducted to measure the back-etch rate of small diameter, high aspect ratio microvias. Test samples of polyimide dielectric were laminated on oxidized silicon wafers, laser-drilled with a variety of hole sizes, back-etched, and then examined to measure the thickness of silicon oxide removed from the bottom of

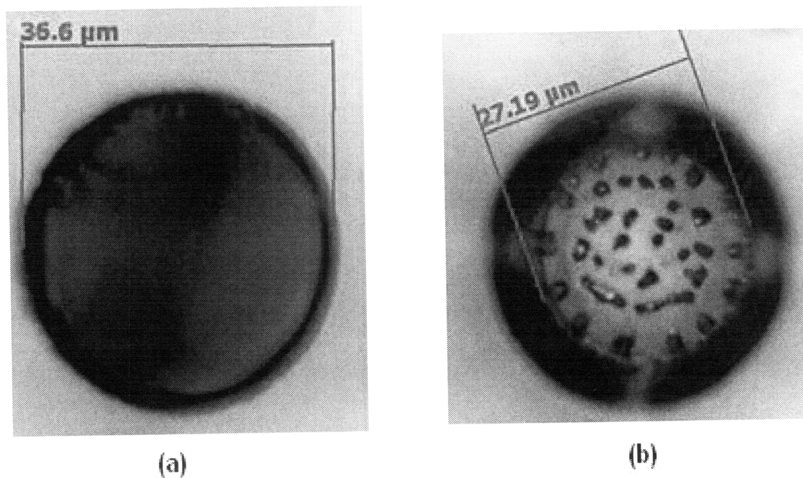


Figure 4-1: Microscope images of (a) the top of a 34 μm laser-drilled hole and (b) the bottom of the whole, showing the silicon oxide before back-etching.

the holes. Figure 4-1 shows microscope images of the top and bottom of a 34 μm aperture laser-drilled hole. The bottom of the hole shows the silicon oxide present before back-etching.

The experiments were performed to monitor the back-etching of smaller microvias. Removal rates of SiO_2 can be correlated with removal rates of native oxides such as Al_2O_3 on metal die pads. Whereas the oxidized wafers had an SiO_2 layer thickness of 10,000 Å, the Al_2O_3 oxide that develops on aluminum die pads generally reaches only 20 Å. Further, the back-etch rate of SiO_2 is much slower than the back-etch rate of Al_2O_3.

Figure 4-2 shows the thickness of the SiO_2 oxide as a function of laser aperture. that is removed after reactive ion etching. The thickness of the SiO_2 oxide immediately after laser drilling is approximately 10,000 Å. As seen in Figure 4-2, back-etching the microvias removes approximately 1,000 Å of SiO_2 oxide. This data reveals that even with the smallest diameter microvias in a sample with the highest aspect ratio (i.e., thickest polyimide and glue), we were still able to back-etch oxide at the bottom of the microvias. Proper back-etching assures that microvias can adequately adhere to the pads and establish electrical connections.

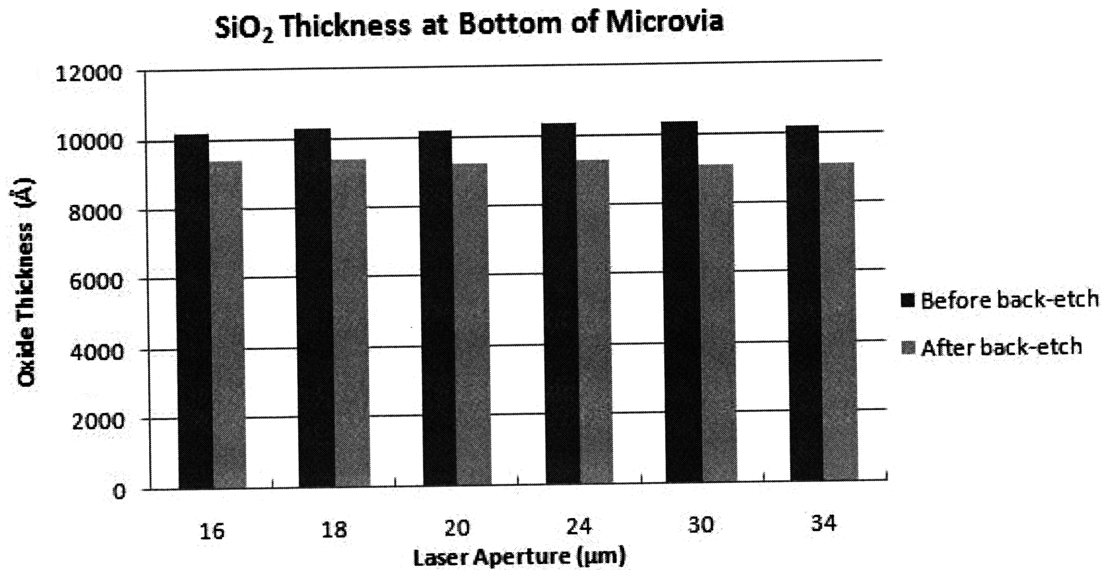


Figure 4-2: Thickness of SiO_2 oxide as a function of laser aperture.

4.2.2 Cross-sections

The standard process samples and experimental test vehicles, both with miniature microvias, are cross-sectioned to confirm proper laser drilling and metallization steps. Cross-sectioning is useful for analyzing the physical structure of microvias and for ensuring mechanical contact is made with the die level.

Cross-sectioned microvias are obtained by cutting the entire substrate with a diamond saw just before the edge of a row of microvias. This is followed by grinding to the edge of a microvia and carefully polishing to the center of the microvia.

Figure 4-3 exhibits the cross-section images of miniaturized microvias fabricated with standard process parameters (5 μm copper plating, 12.5 μm polyimide adhesive). Laser apertures are varied to create vias with different diameters. As seen in the 12 μm and 14 μm microvias, as the aperture is reduced below 16 μm, the plated sidewalls begin to converge and the microvias become more filled.

Figures 4-4 through 4-7 are cross-section images of the microvias in the four test vehicles. Table 4.3 lists the measured microvia diameters after the three process stages: laser drilling, reactive ion etching, and copper electroplating.

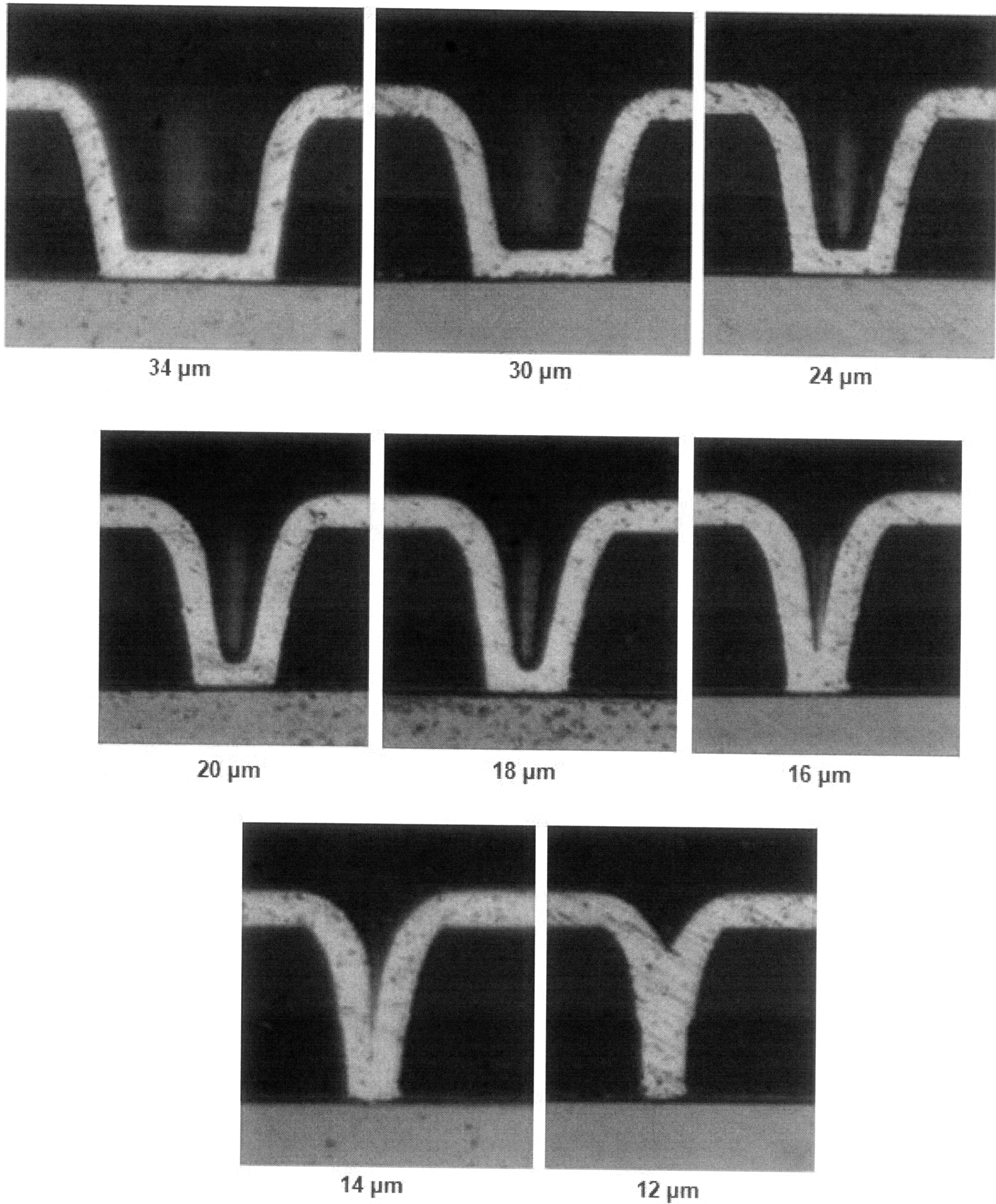


Figure 4-3: Standard process microvias (5 μm copper plating, 12.5 μm polyimide adhesive) created with different laser aperture diameters.

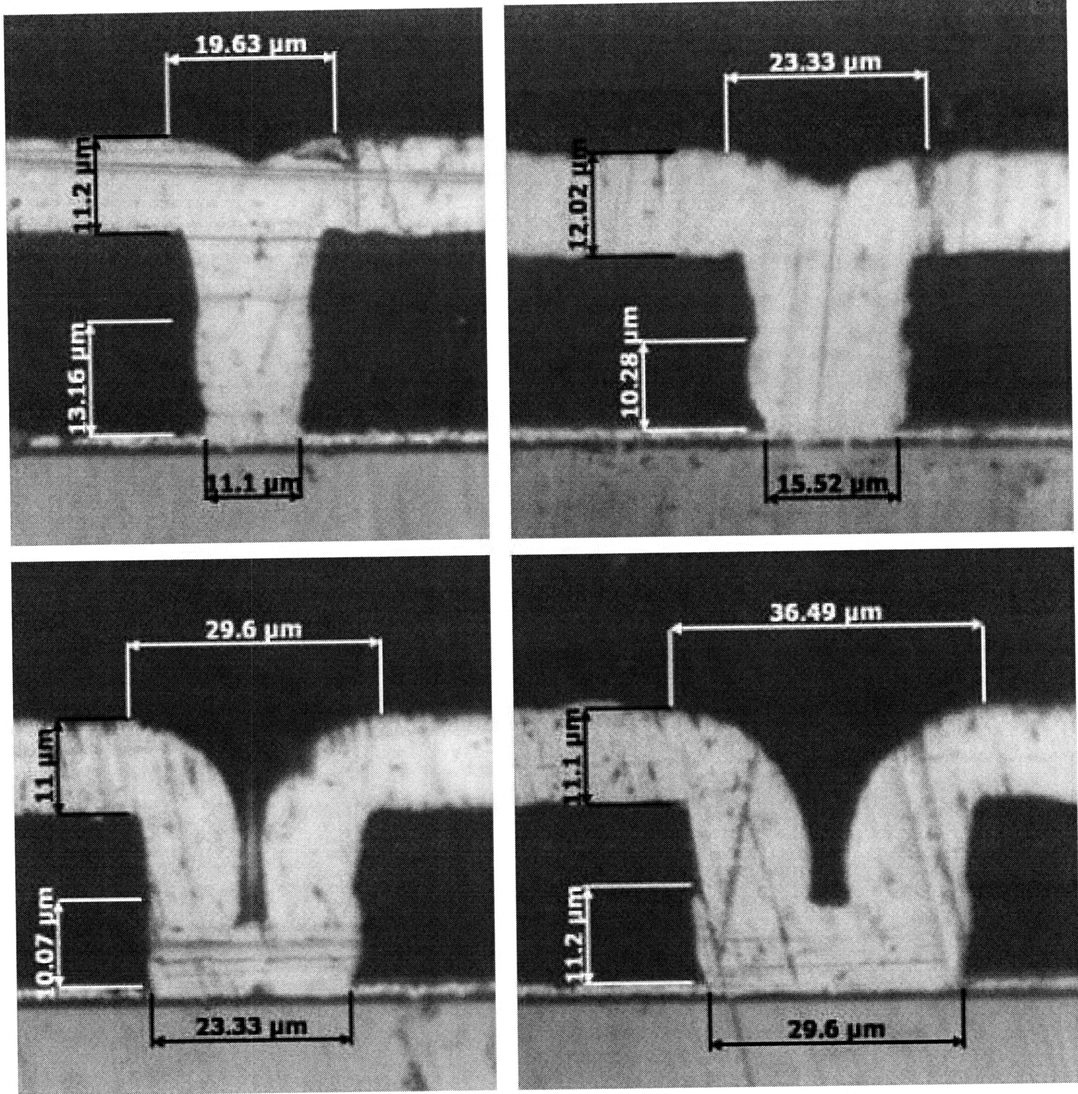


Figure 4-4: Ext-A Microvias. 10 μm copper plating; 12.5 μm adhesive; laser apertures 14 μm, 18 μm, 24 μm, 34 μm.

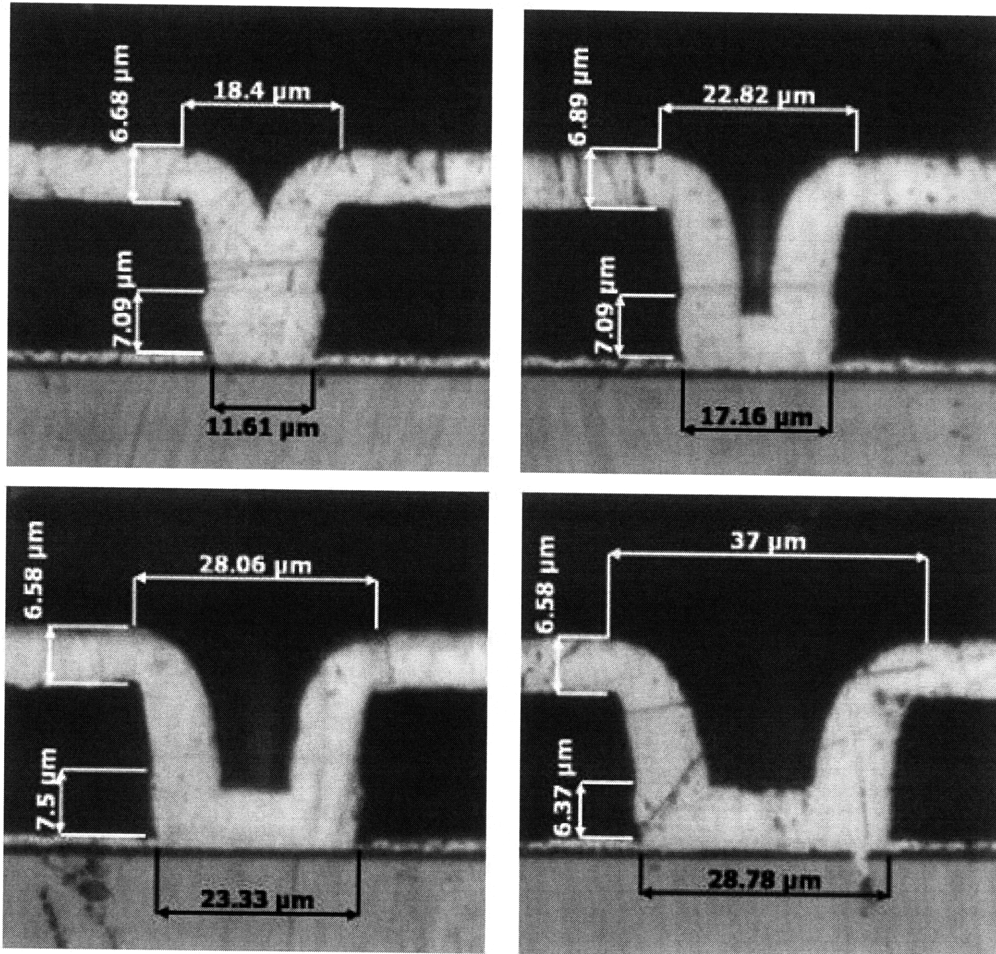


Figure 4-5: Ext-B Microvias. 5 μm copper plating; 7 μm adhesive; laser apertures 14 μm, 18 μm, 24 μm, 34 μm.

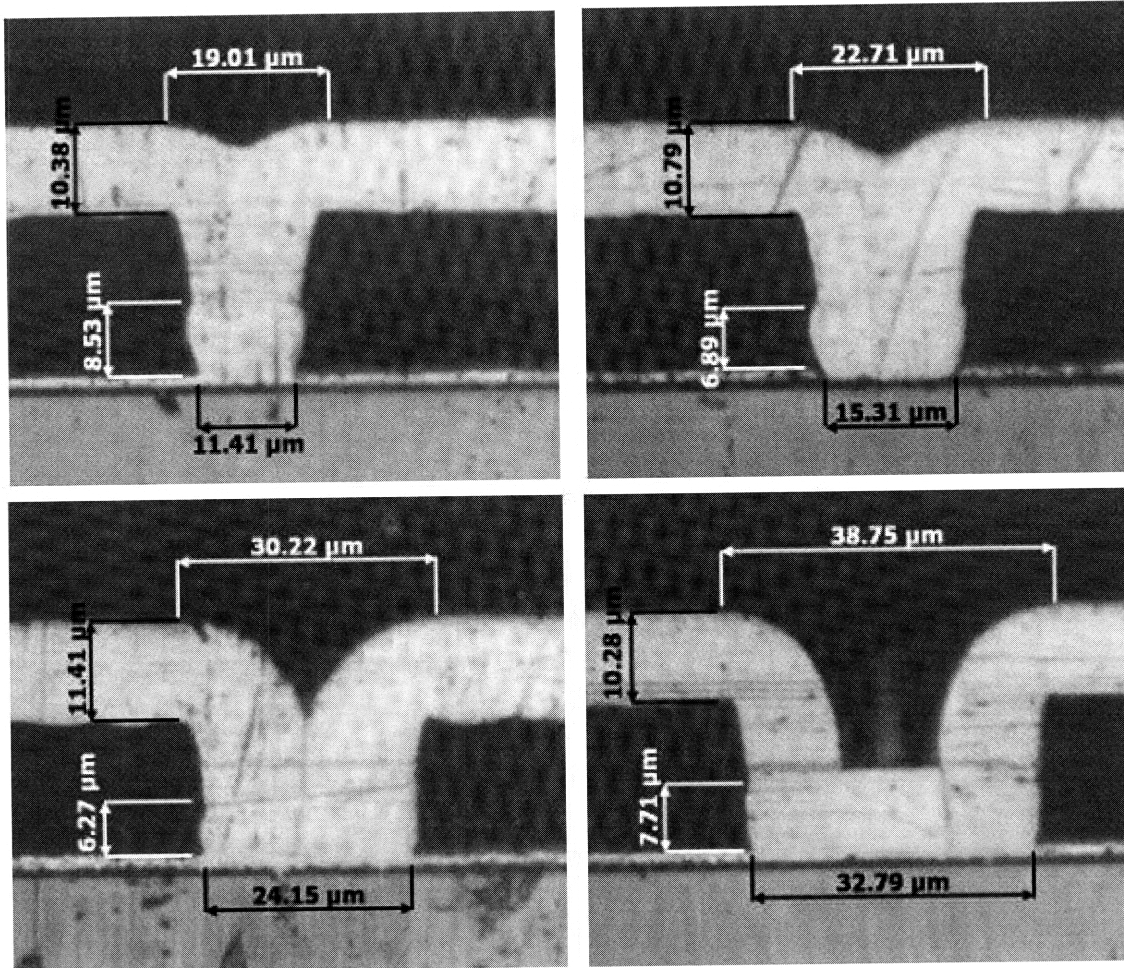


Figure 4-6: Ext-C Microvias. 10 μm copper plating; 7 μm adhesive; laser apertures 14 μm, 18 μm, 24 μm, 34 μm.

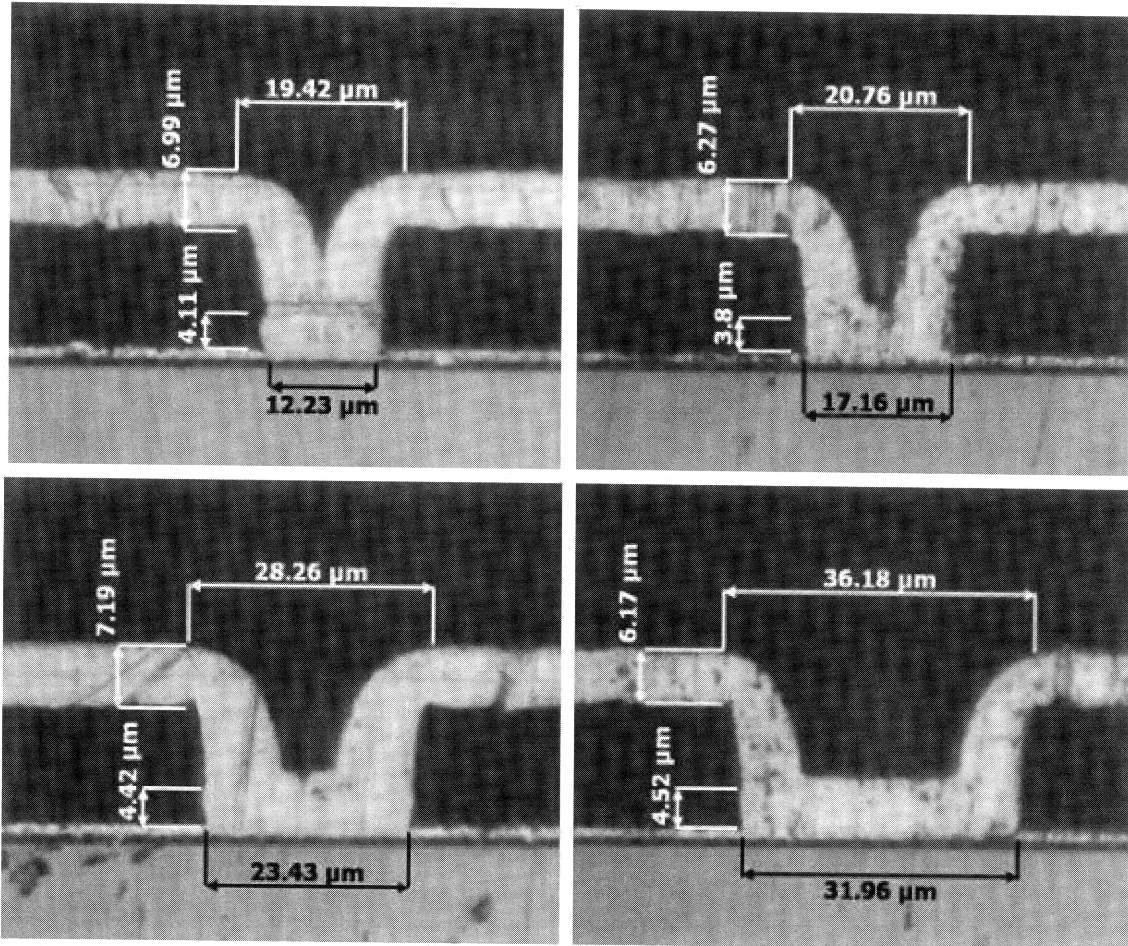


Figure 4-7: Ext-D Microvias. 5 μm copper plating; 4 μm adhesive; aser apertures 14 μm, 18 μm, 24 μm, 34 μm.

Table 4.3: Microvia Diameter Measurements (μm)

Ext-A: 10 μm Copper, 12.5 μm Dielectric Adhesive

Laser Aperture		Laser Drilled Hole Before RIE	Laser Drilled Hole After RIE	Electoplated Microvia Cross Section
14	Top	18.77	20.68	19.63
	Bottom	7.83	12.78	11.10
18	Top	24.43	25.21	23.33
	Bottom	12.16	17.54	15.52
24	Top	30.70	31.55	29.60
	Bottom	19.37	24.59	23.33
34	Top	38.39	38.92	36.49
	Bottom	28.92	33.50	29.60

Ext-B: 5 μm Copper, 7 μm Dielectric Adhesive

Laser Aperture		Laser Drilled Hole Before RIE	Laser Drilled Hole After RIE	Electoplated Microvia Cross Section
14	Top	19.28	19.44	18.40
	Bottom	8.32	11.83	11.61
18	Top	23.39	24.74	22.82
	Bottom	12.36	16.18	17.16
24	Top	30.85	31.11	28.06
	Bottom	19.29	23.73	23.33
34	Top	39.54	40.57	37.00
	Bottom	27.53	32.04	28.78

Ext-C: 10 μm Copper, 7 μm Dielectric Adhesive

Laser Aperture		Laser Drilled Hole Before RIE	Laser Drilled Hole After RIE	Electoplated Microvia Cross Section
14	Top	19.52	20.32	19.01
	Bottom	8.09	10.87	11.41
18	Top	23.46	24.58	22.71
	Bottom	14.93	16.22	15.31
24	Top	30.65	31.15	30.22
	Bottom	21.18	23.16	24.15
34	Top	39.72	40.29	38.75
	Bottom	30.96	31.15	32.79

Ext-D: 5 μm Copper, 4 μm Dielectric Adhesive

Laser Aperture		Laser Drilled Hole Before RIE	Laser Drilled Hole After RIE	Electoplated Microvia Cross Section
14	Top	19.24	20.03	19.42
	Bottom	8.83	11.26	12.23
18	Top	23.62	24.78	20.76
	Bottom	13.10	17.03	17.16
24	Top	29.26	30.88	28.26
	Bottom	19.90	23.89	23.43
34	Top	39.07	39.69	36.18
	Bottom	29.80	32.57	31.96

4.3 Contact resistance

Though we track several process metrics—laser-drilled hole diameter, back-etch rate, hole diameter enlargement after back-etching, copper plating thickness, and polyimide adhesive thickness—contact resistance is the key to a reliable microvia process.

The contact resistance at the interface between two touching conductors arises from two properties characteristic of all contacting surfaces: surface roughness and surface contamination. Because the surface irregularities are large on an atomic scale, the true area of contact is only a small fraction of the apparent area of contact, thus causing a constriction in the lines of current flow between the two conductors. Further, the surfaces are usually contaminated with a film such as a layer of oxide, which if not removed, can add to the contact resistance both by reducing the area of true metallic contact and by introducing a film resistance.

4.3.1 Measurement using Kelvin structures

For this research, microvia contact resistance is monitored using Kelvin structures. A Kelvin structure, as depicted in Figure 4-8, is a four-probe measurement in which a cross is built on separate interconnect levels with a microvia joining the two arms in the center. Resistance is measured by supplying a fixed current to one side of the circuit and measuring a voltage on the other side. As the only thing common to both arms of the circuit is the joining microvia, the contact resistance can be deduced by Ohm's Law ($R = V_{Measure}/I_{Input}$).

At first level, we construct silicon die with 1 μm aluminum metallization atop which to build Kelvin structures. Kelvin structures are also constructed on all upper levels, thus yielding information on the integrity of the entire module's fabrication. Figure 4-8 (b) shows a sample of an actual Kelvin structure that was used for measuring microvia contact resistance. The tops of the microvias can be seen in the top left, center, and bottom right of the cross structure.

The contact resistance results of the Kelvin structure measurements are graphed in Figure 4-9. A reliable microvia must maintain a certain electrical resistance and me-

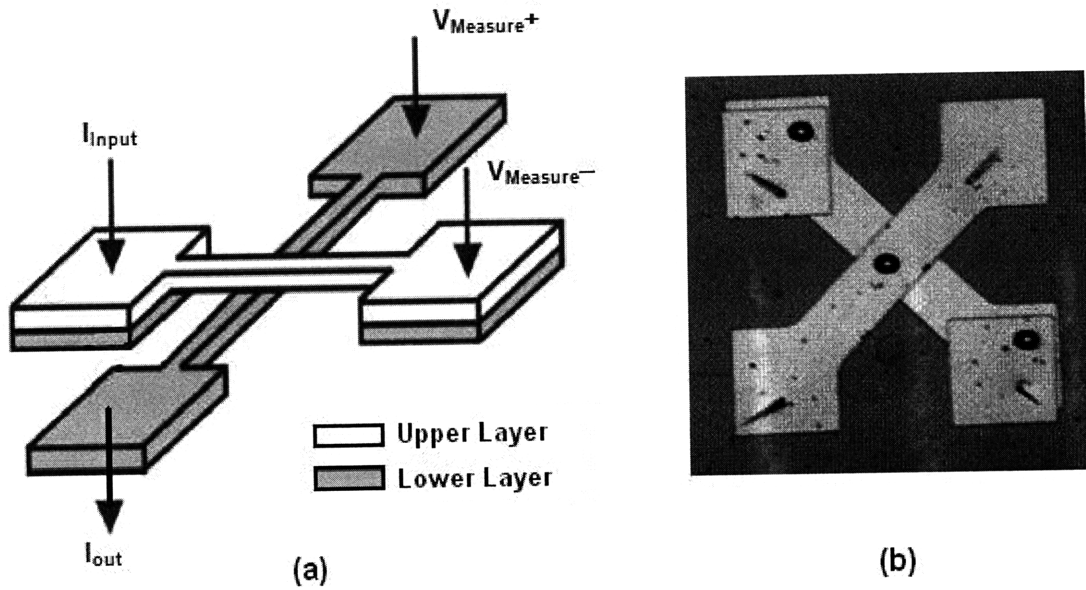


Figure 4-8: Kelvin structure for monitoring the contact resistance of microvias. (a) Model for the setup of the four-probe measurement. (b) Magnified image of an actual Kelvin structure used in the test vehicles.

chanical adhesion to the next conducting layer. For standard size microvias, Draper Laboratory rejects microvias with contact resistances greater than 10 mΩ as having failed. For the purpose of this research, miniaturized microvias with contact resistances greater than 20 mΩ are considered to have failed.

The die-level measurement values for the 14 μm and 18 μm microvias of Ext-A are absent because the values were greater than 20 mΩ, and thus the microvias were rejected as failures. The microvias of Ext-D have the lowest contact resistance values for all size microvias. Thus, according to these results, the Ext-D microvias are preferable for their low contact resistance and minimal geometry (i.e., thin 5 μm copper plating and thin 4 μm adhesive).

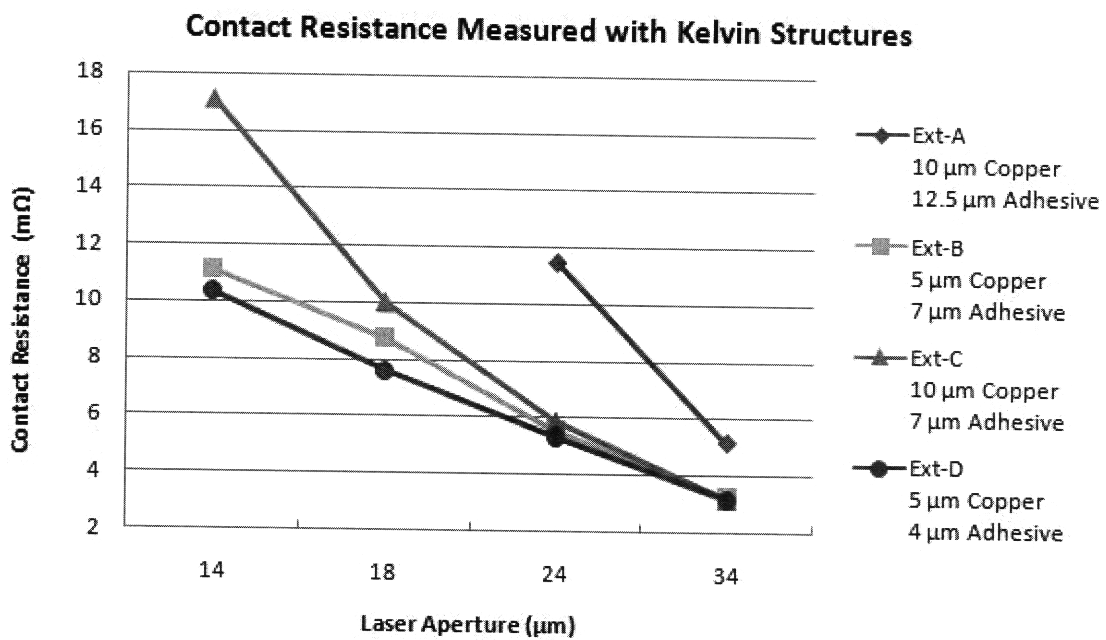


Figure 4-9: Kelvin structure measurements for the four test vehicles. The die-level measurements for the 14 μm and 18 μm microvias are absent because the values were greater than 20 mΩ, and thus the microvias were rejected as failures.

4.3.2 Thermal shock cycling

During the MCM-D fabrication process, the copper plated microvias are subjected to large thermal stresses, resulting from the thermal excursions induced during processing. Following deposition, the microvia layer, including Kapton polyimide and adhesive surrounding the copper microvia, is elevated in temperature and pressure. The Kapton and adhesive layers expand at higher rates than the copper, placing a large tensile stress on the microvia. Previous analysis performed at Draper Laboratory has shown that the stresses far exceed the elastic limit of the copper, the microvia plastically deforms, and a large tensile/shear debonding force is incurred at the microvia/pad interface. The microvia is also loaded in shear due to the in-plane expansion of the Kapton, which is relatively less constrained at high temperatures, when the adhesive softens.

For this research, the four test vehicles were subjected to 1,000 liquid-to-liquid thermal shocks (-50°C to $+125$°C) to test for fatigue. The contact resistances of all the Kelvin structures were monitored at intervals of 200 shocks. Standard process microvias (34 μm laser aperture, 5 μm copper, 12.5 μm adhesive) will survive 800 liquid-to-liquid thermal shocks.

Contact failures

This research will not attempt to explain the failure mechanisms of microvias, however according to previous research, possible reasons for failure include the temperature and coefficient of thermal expansion mismatch of the copper microvia, Kapton polyimide, and adhesive [13].

The effect of the Kapton thickness is important. Thinner Kapton acts as a strain relief for the expanding adhesive, reducing the constrained pressure that is acting on the copper. The adhesive thickness is also important. Thicker adhesive places more strain on the microvia. Furthermore, the effect of the microvia sidewall angle is also an important factor. As the angle relaxes from vertical, more bending moment is induced, increasing the stress on the copper. Therefore, a microvia with thin

Kapton, a thin adhesive layer, and nearly vertical sidewalls is the more robust design if consideration is limited to the existing materials.

Overall, it was concluded that minimization of the Kapton and adhesive layer thicknesses is advisable and significantly reduces the stress on the copper via.

Results of thermal fatigue experiments

Figures 4-10 through 4-13 show satisfactory survival rates for all but some of the smallest microvias. The results confirm that thinner metal and dielectric adhesive, as used for Ext-D, are the favorable parameters for microvias to survive thermal fatigue.

Therefore, the most desirable microvia parameters to use in future MCM processes are the microvias from test vehicle Ext-D (5 μm copper, 4 μm adhesive). By inspecting the survival rate of the 14 μm Ext-D microvia as a function thermal shocks in Figure 4-13, we see that only one of the fifteen microvias failed after 400 thermal shocks. All other 14 μm microvias survived until 800 thermal shocks, at which point five of the fifteen failed. Further testing will need to be done to verify whether the single failure was an anomaly. Presuming all 14 μm Ext-D microvias can reliably survive 600 thermal shocks, then that specific microvia structure (14 μm laser aperture, 5 μm copper, 4 μm adhesive) could be classified as a successful candidate for implementation in future MCMs.

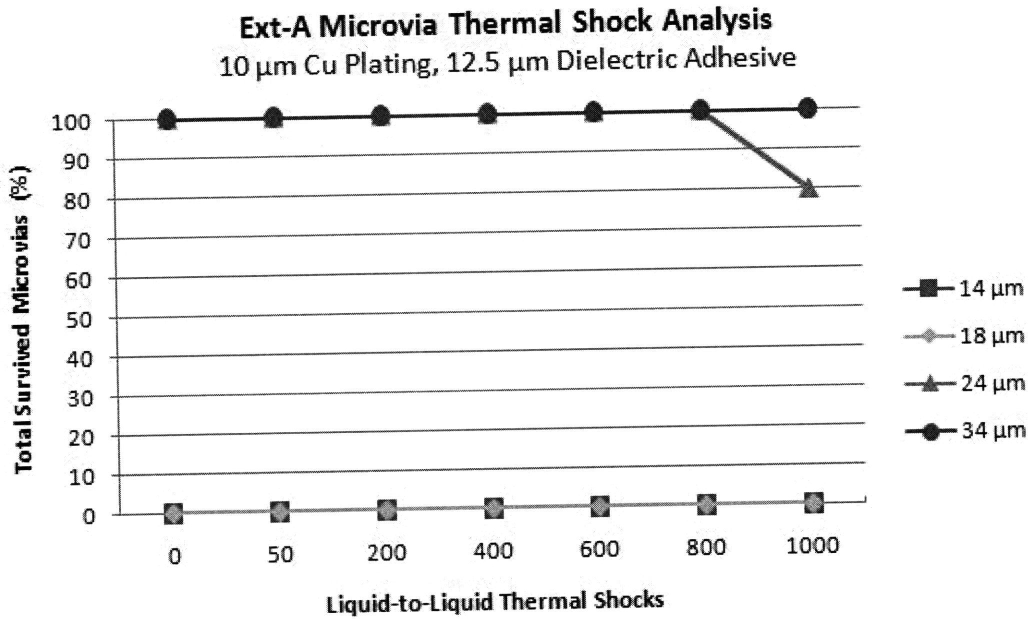
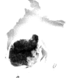


Figure 4-10: Kelvin structure measurements for test vehicle Ext-A taken during thermal shock analysis.



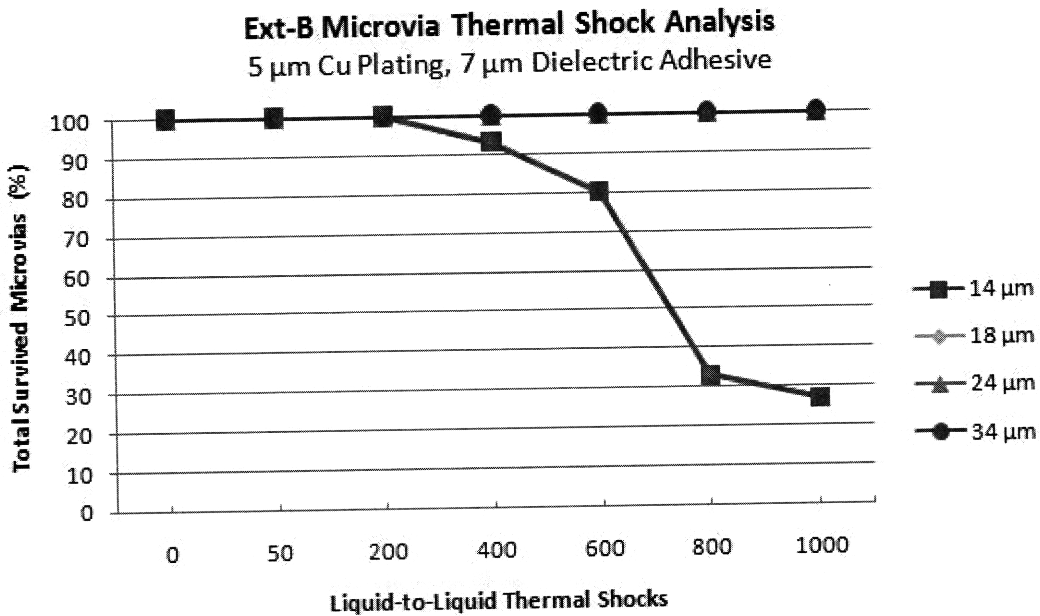


Figure 4-11: Kelvin structure measurements for Ext-B taken during thermal shock analysis.

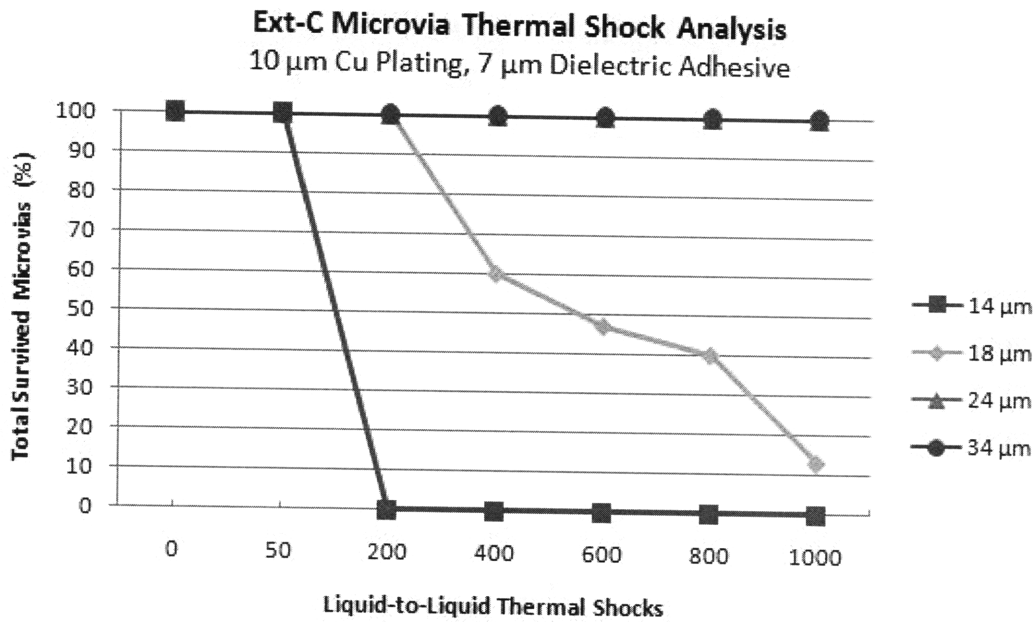


Figure 4-12: Kelvin structure measurements for Ext-C taken during thermal shock analysis.

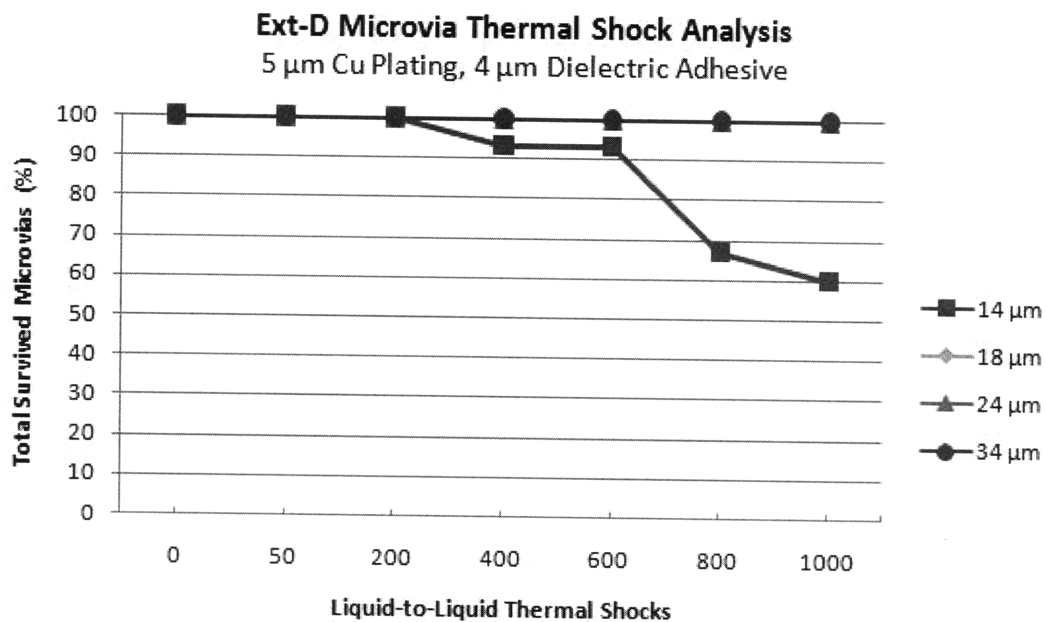


Figure 4-13: Kelvin structure measurements for Ext-D taken during thermal shock analysis.

Chapter 5

Finite Element Modeling

The contact resistances of miniaturized microvias in thin film polyimide is calculated using a finite element model (FEM) and compared to the experimental contact resistance measurements from Chapter 4. The models incorporate the entire Kelvin structure, as shown in the CAD drawing in Figure 5-1.

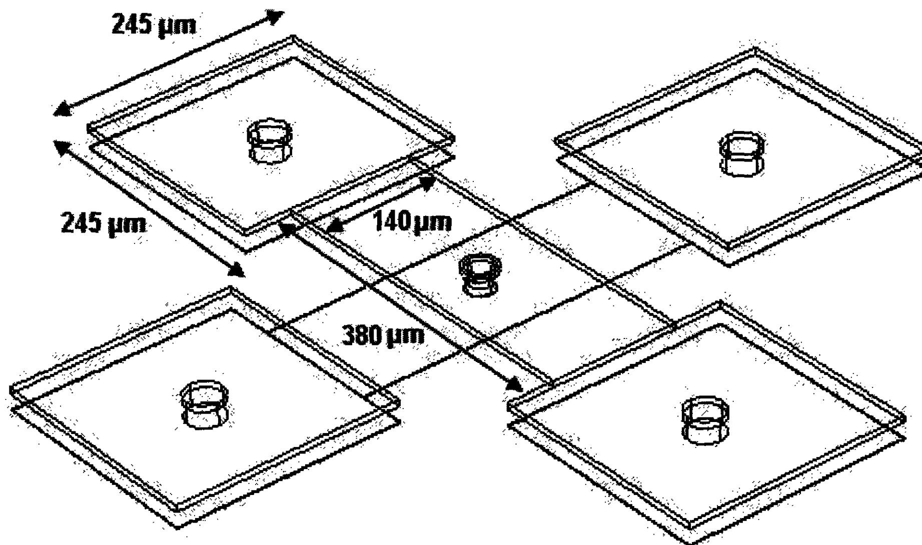


Figure 5-1: CAD drawing of a Kelvin structure for finite element analysis.

5.1 Microvia model geometry

The dimenions of the microvias used for the finite element models were determined by measuring the cross-section images of the test vehicles presented in Table 4.3. Figure 5-2 shows the cross-section of a 34 μm microvia and its corresponding model.

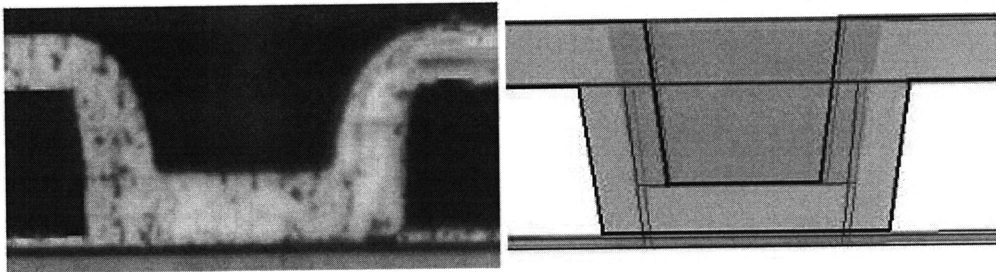


Figure 5-2: Magnified view of a microvia cross-section and its corresponding CAD drawing to be modeled.

The geometry of the Kelvin structure itself also mimics the dimensions of the actual Kelvin structure. The die pads of the Kelvin structure were 245 μm by 245 μm, and the connecting bridges were 380 μm by 140 μm. Further, the models also accounted for the different Kelvin structure heights due to the varying copper thickness and adhesive thickness of the test vehicles. The bottom level of the Kelvin structures serve as the die-level metallization, which was set to 1 μm aluminum for all models.

5.2 FEM parameters

The commercial software package COMSOL was used to create the model and to calculate the resistance of the different contact geometries. The predefined environment for generalized electrostatic cases was selected. The partial differential equation (PDE) used was $-\nabla \cdot (\sigma \nabla V) = Q$, where V is the electric potential, σ is the conductivity, and Q is the current source. The current source Q is defined by $\nabla \cdot \mathbf{J}_0$ where $\mathbf{J}_0$ is the density of an external current, so that the total current density is given by $\mathbf{J}_{tot} = \mathbf{J} + \mathbf{J}_0 = \sigma \mathbf{E} + \mathbf{J}_0$, where $\mathbf{E} = -\nabla V$ is the electric field.

The boundary conditions used in the models were set for insulating boundaries $-\mathbf{n} \cdot \mathbf{J} = 0$ (i.e., the normal component of the current density is zero) and for fixed potential boundaries $V = V_0$.

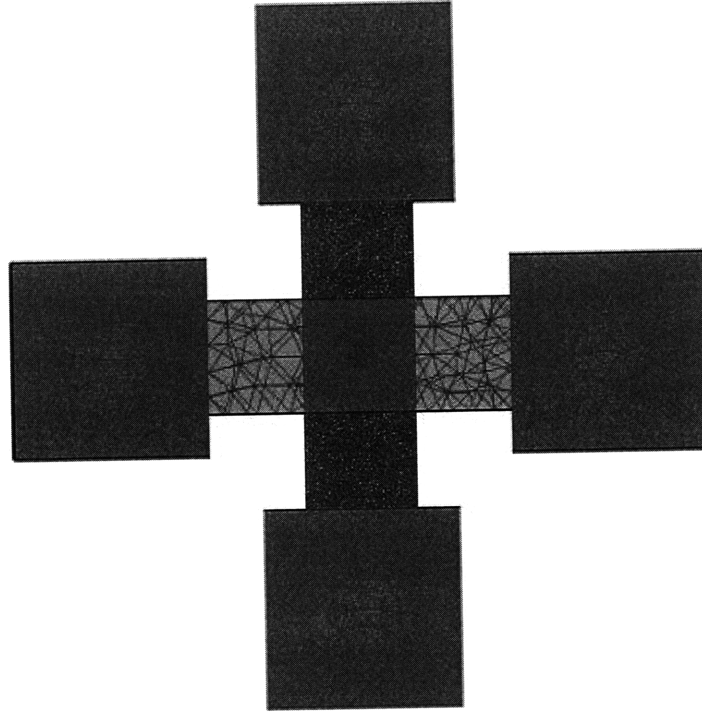


Figure 5-3: Mesh elements of a Kelvin structure generated using finite element analysis.

Finite element meshing, as shown in Figure 5-3, was performed using quadratic Lagrange elements and a smoothing algorithm for element quality improvement. Mesh densities were varied from extremely fine to extra coarse settings as limited by the specific microvia geometry. The number of used elements varied from approximately 60,000 to 200,000. The stability of the FEM solutions was verified by solving the models using different mesh densities. In general, the finer meshes yielded solutions nearer to the measured values.

The initial conditions for the models were achieved by supplying a 1 mA current into one of the pads and setting its neighboring pad to ground (electric potential, V_0=0). After solving the model by applying the PDEs to the mesh elements, post-processing can be done to measure the resulting voltage across the remaining two

pads. The electric potential gradient over all boundary layers of the Kelvin structure was observed for each model, an example of which can be seen in Figure 5-4. Finally, the contact resistance was deduced by applying Ohm's Law ($R = V_{Measure}/I_{Input}$).

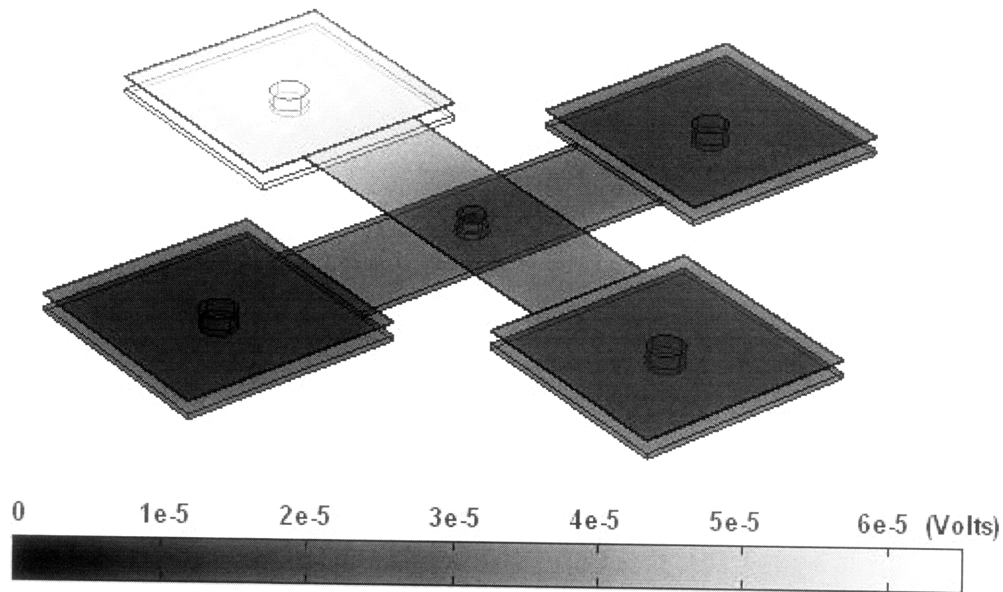


Figure 5-4: Electric potential gradient of Kelvin structure modeled using finite element analysis.

5.3 Contact resistance results

Table 5.1 lists the contact resistance values for die-level and upper-level microvias that were measured from Chapter 4 and calculated with the finite element models. The contact resistances are also graphed according to test vehicle in Figures 5-5 through 5-8.

Table 5.1: Measured and modeled contact resistance values for die-level and upper-level microvias.

Ext-A: 10 μm Copper, 12.5 μm Dielectric Adhesive

Laser Aperture (μm)	Contact Resistance (mΩ)					
	Die-Level			Upper-Level		
	Measured	Modeled	Error	Measured	Modeled	Error
14	220.5	10.10	95.4%	4.9	4.37	10.7%
18	46.7	7.20	84.6%	3.0	2.44	18.5%
24	11.1	4.00	64.0%	1.7	1.24	26.8%
34	4.7	2.90	38.3%	1.0	0.90	10.1%

Ext-B: 5 μm Copper, 7 μm Dielectric Adhesive

Laser Aperture (μm)	Contact Resistance (mΩ)					
	Die-Level			Upper-Level		
	Measured	Modeled	Error	Measured	Modeled	Error
14	10.8	9.41	12.8%	4.8	3.73	22.3%
18	8.0	7.14	10.7%	3.2	2.58	19.2%
24	5.5	5.38	2.2%	2.2	1.89	14.1%
34	3.1	3.04	1.9%	1.2	1.12	7.0%

Ext-C: 10 μm Copper, 7 μm Dielectric Adhesive

Laser Aperture (μm)	Contact Resistance (mΩ)					
	Die-Level			Upper-Level		
	Measured	Modeled	Error	Measured	Modeled	Error
14	19.1	8.88	53.5%	3.7	3.46	6.5%
18	10.3	7.02	31.8%	2.3	2.24	2.5%
24	5.6	4.18	25.4%	1.4	1.11	21.0%
34	3.1	2.66	14.3%	0.8	0.74	7.6%

Ext-D: 5 μm Copper, 4 μm Dielectric Adhesive

Laser Aperture (μm)	Contact Resistance (mΩ)					
	Die-Level			Upper-Level		
	Measured	Modeled	Error	Measured	Modeled	Error
14	10.1	8.85	12.4%	4.6	3.14	31.7%
18	7.4	6.32	14.5%	3.1	2.22	28.4%
24	5.3	4.06	23.4%	2.0	1.20	39.8%
34	3.1	2.60	16.1%	1.2	0.90	24.6%

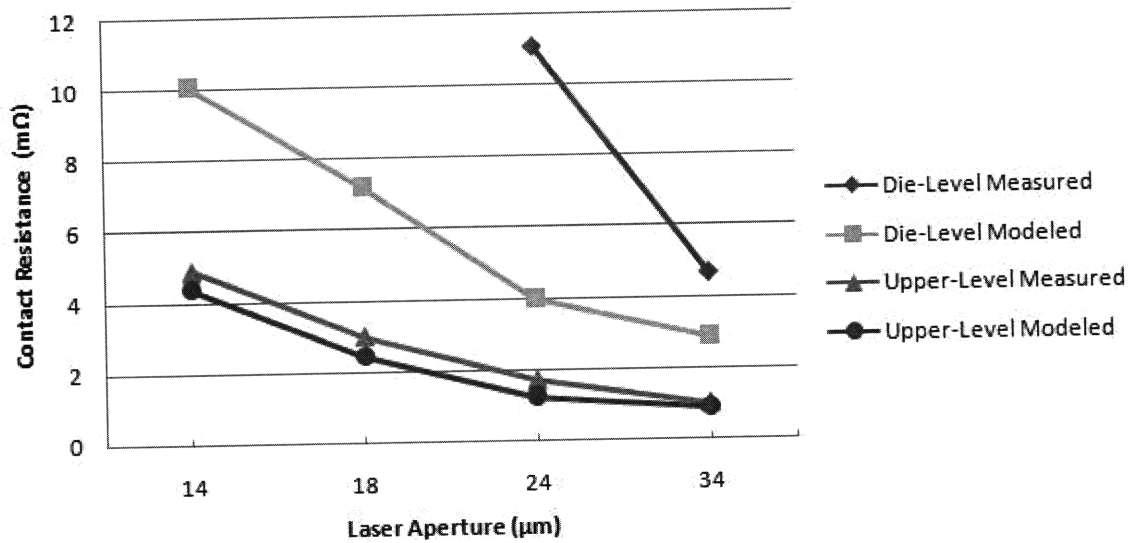


Figure 5-5: Finite element model of contact resistance as a function of laser aperture for Ext-A. The die-level measurements for the 14 μm and 18 μm microvias are absent because the values were greater than 20 mΩ, and thus the microvias were rejected as failures.

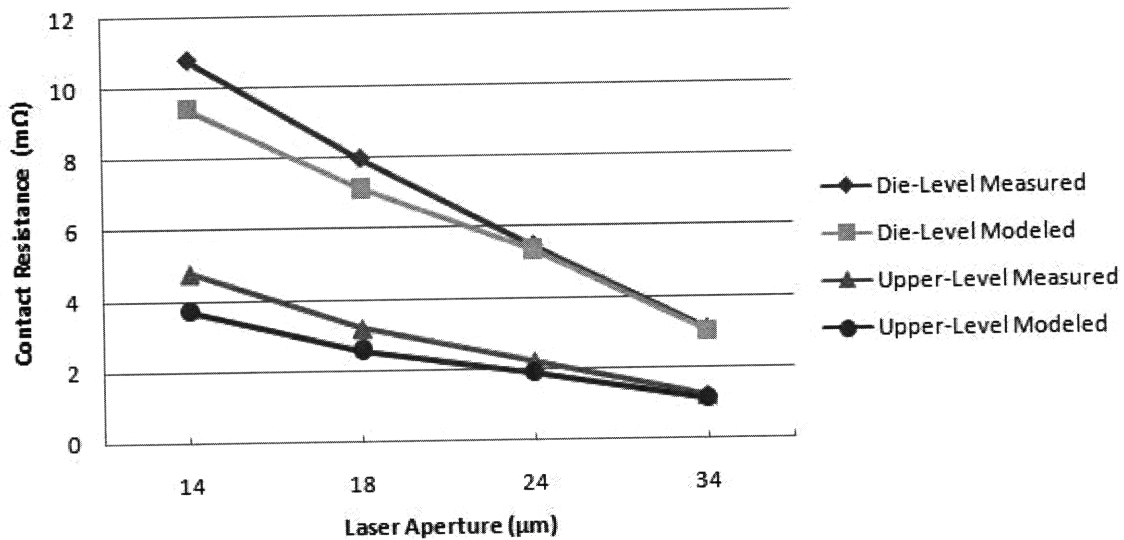


Figure 5-6: Finite element model of contact resistance as a function of laser aperture for Ext-B.

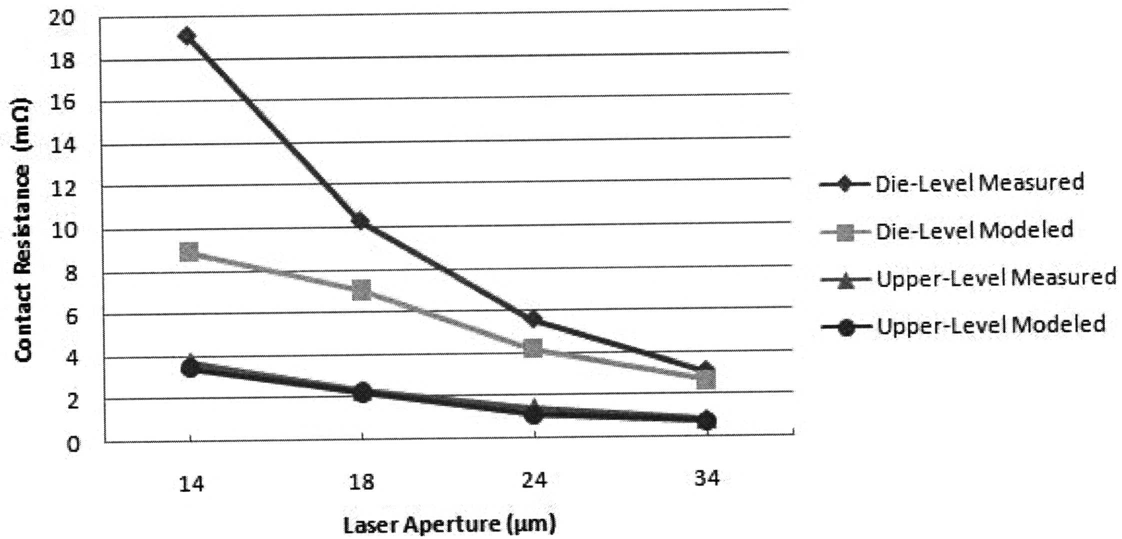


Figure 5-7: Finite element model of contact resistance as a function of laser aperture for Ext-C.

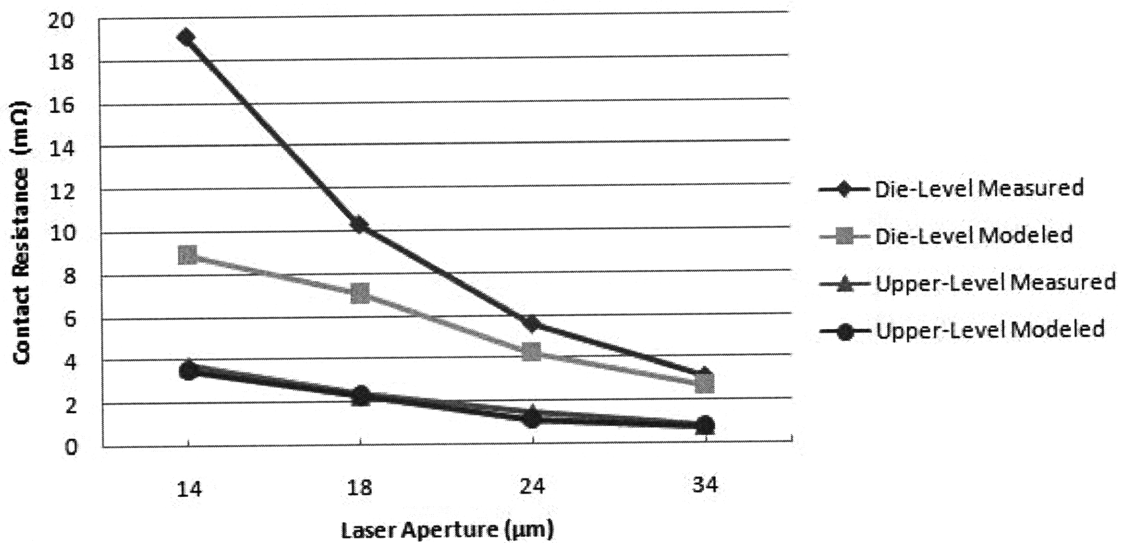


Figure 5-8: Finite element model of contact resistance as a function of laser aperture for Ext-D.

5.3.1 Comparative analysis

Overall, the FEM for test vehicles Ext-B and Ext-D yielded contact resistances nearest to the measured values. Both of these test vehicles were electroplated with 5 μm of copper. On the otherhand, the contact resistances modeled by test vehicles Ext-A and Ext-C diverged most from the measured values. There are a couple possible explanations for these differences.

Electroplating stress

First, since this research considers a microvia to be failed if the measured contact resistance is greater than 20 mΩ, the 14 μm and 18 μm microvias of test vehicle Ext-A were considered failed. Thus, the high values of contact resistance of these microvias were deemed inconclusive. A possible explanation for the discrepancy in the other microvia values of Ext-A and Ext-C is the 10 μm copper plating. Previous analysis performed at Draper Laboratory revealed that the electroplating bath for thicker layers of copper stresses the wafer and causes the wafer to bow on the ends. This sort of stress during plating could affect the structural integrity of the microvia or even cause certain microvias to fail, both of which would influence the measured contact resistance.

Microvia geometry

For all test vehicles, the FEM generates contact resistance values that are less than the measured values. This uniform difference could be attributed to the microvia geometry used by the FEM. Despite using exact dimensions as taken from cross-sections for the FEM, the model geometry is still idealized. Actual microvias contain a more interesting geometry, including non-linear sidewalls, bulging at the base into the adhesive layer, thickness variation across a wafer, and so forth. If the models were to include such details, the resulting contact resistance calculations may improve.

Test die metallization

The error between the measured and modeled values could also be attributable to variance in the thickness of the die-level aluminum metallization. In general, Draper Laboratory assumes that the test die metallization is a 1 μm uniformly thick layer of aluminum. Cross-sectioning reveals that the metallization is not uniformly 1 μm thick across a wafer and certainly not uniform from wafer to wafer. Therefore, in addition to the three process parameters that were varied in the test vehicles—laser aperture, plating thickness, and adhesive thickness—another process parameter that had been examined with the FEM was the aluminum test die metallization.

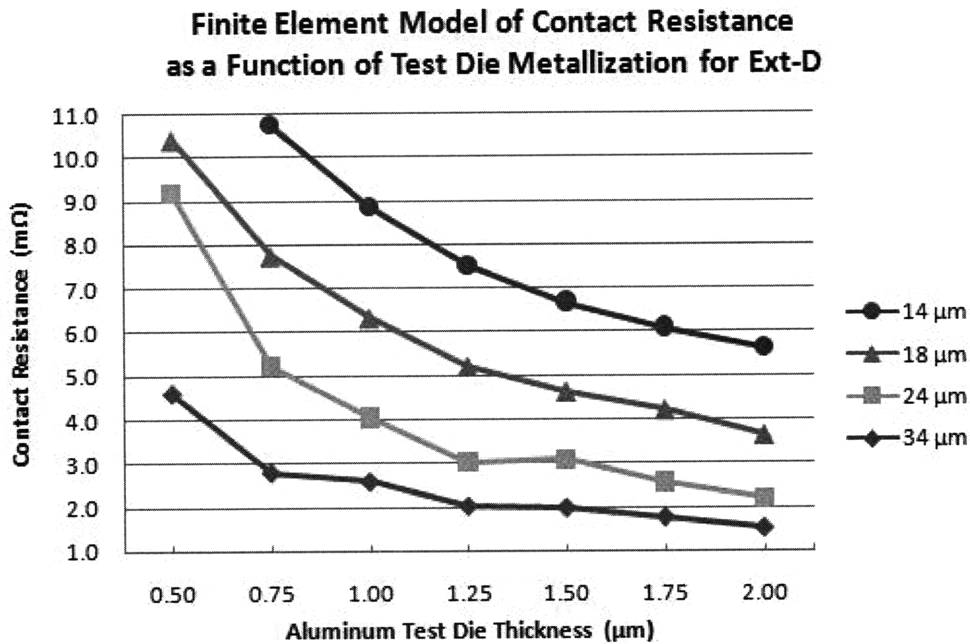


Figure 5-9: Finite element model contact resistance as a function of aluminum test die thickness for test vehicle Ext-D.

Figure 5-9 graphs the FEM contact resistance of microvias from test vehicle Ext-D as a function of aluminum test die thickness. As we would expect, the contact resistance decreases as the aluminum test die metallization becomes thicker. However, as the metallization thickness varies $+/-\ 0.25\mu$m, the modeled contact resistance can vary from 1 mΩ to 2 mΩ depending on laser aperture.

Chapter 6

Conclusion

In this thesis we investigated the miniaturization of laser-drilled microvias in polyimide dielectric for chips-first MCM technology.

By analyzing the microvia formation in Section 4.2, we verified that the argon plasma could back-etch oxide at the bottom of even the smallest diameter microvias in a sample with the highest aspect ratio (i.e., thickest polyimide and glue). This result assured that microvias can adequately adhere to the die pads and establish electrical connections.

The Kelvin structure contact resistance measurements of the four test vehicles presented in Section 4.3 tested the electrical performance of the varying size microvias and revealed some interesting results. The 14 μm and 18 μm microvias of Ext-A (10 μm copper, 12.5 μm adhesive) were rejected as failures, which was surprising because the Ext-A microvias had the thickest layer of copper. The failues could possibly be attributed to stress on the wafer during electroplating. On the other hand, the microvias of Ext-D (5 μm copper, 4 μm adhesive) had the lowest measured contact resistance values for all size microvias when compared with the other test vehicles. The contact resistance experiments further included liquid-to-liquid thermal shocks to test for fatigue. The results showed that the microvias of Ext-D performed best and confirmed that thinner metal and dielectric adhesive are more favorable during thermal fatigue.

Based on the results of Chapter 4, the Ext-D microvias were deemed most prefer-

able for implementation into future MCMs assembled by Draper Laboratory because of their low contact resistance, minimal size (i.e., smallest diameter, thinnest plating, and thinnest adhesive), and longest thermal shock survival.

6.1 Contribution of research

The foremost contribution of this thesis was the finite element model that calculates the contact resistance of microvias in a Kelvin structure configuration. The model was tailored to the specific geometry of each microvia, as measured by the cross-section results in Section 4.2.2. The model yields solutions that were in many cases within 0.5 mΩ of the measured contact resistance values. The accuracy of the model's solutions is influenced by the accuracy of the model's predefined geometry. If the geometries were to include details such as rounded corners, non-linear sidewalls, and surface roughness, the resulting contact resistance calculations may further improve. Nevertheless, the finite element model presented herein is the most accurate model Draper Laboratory has to estimate the contact resistance of microvias.

Overall, this research proved that Draper Laboratory can fabricate reliable microvias with smaller diameters (19 μm) than it had ever fabricated before. The smaller diameter microvias will allow Draper Laboratory to assemble MCMs that can accommodate advanced IC dies with higher I/O pin counts and smaller die pads.

Bibliography

[1] Tanner Labs (A Division of Tanner Research, Inc.), "Multi-Chip Modules," http://www.tanner.com/Labs/research/technologies/mcm/default.htm

[2] W. Daum, W.E. Burdick, Jr., R.A. Fillion (GE Corporate Research & Development Center), "Overlay High-Density Interconnect: A Chips-First Multichip Module Technology," *IEEE*, April 1993.

[3] N.A. Blum, H.K. Charles, Jr., and A.S. Francomacaro, "Multichip Module Substrates," *Johns Hopkins APL Technical Digest*, Vol. 20, No. 1, 1999.

[4] J. Wolf (Fraunhofer IZM), B. Bottoms, B. and Chen-Chairs (Productronica), "Packaging Roadmap: The impact of miniaturization," *iNEMI International Electronics Manufacturing Initiative*, November 14, 2007.

[5] L.M. Levinson, C.W. Eichelberger, R.J. Wojnarowski, and R.O. Carlson (GE Corporate Research & Development Center), "High-Density Interconnects Using Laser Lithography," *Proceedings of the 1988 International Symposium on Microelectronics*, pp. 301-306, 1988.

[6] L.E. Roszel (T.I.), W. Daum (G.E. CR&D), "MCM Prototyping Using Overlay Interconnect Process," *Proceedings of the 1992 IEEE Multi-Chip Module Conference*, pp. 36-39, 1992.

[7] T.M. Schaefer, J.J. Kacines, B.A. Randall, L.E. Roszel, G.J. Fokken, D.Walter, D.J. Schwab, L. Mowatt, and B.K. Gilbert, "A Chips-First Multichip Module Implementation of Passive and Active Test Coupons Utilizing Texas Instruments

HDI Technology," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Part B, Vol.19, No.2, May 1996.

[8] A. Dineen, G.V. Ives (Draper Laboratory), "Method of Fabricating a Laminated Substrate Assembly Chips-First Multichip Module," *U.S. Patent 5,564,181*, October 15, 1996.

[9] J.J. LeBlanc, R.P. Tumminelli, M.C. Singleton, E.P. Ayers, J.F. Haley, G.V. Ives, A.D. Dineen (The Charles Stark Draper Laboratory, Inc.), "Process for Fabricating Dense, Chips-First MCMs with Thinned Die," *HD International*, 2001.

[10] J.H. Das, J.E. Morris, "Metal Diffusion in Polymers," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Part B, Vol.17, No.4, November 1994.

[11] G. Norberg, S. Dejanovic, and H. Hesselbom, "Contact Resistance of Thin Metal Film Contacts," *IEEE Transactions on Components and Packaging Technologies*, Vol.29, No.2, June 2006.

[12] J. Santander, M. Lozano, A. Collado, M. Ullan, and E. Cabruja, "Accurate Contact Resistivity Extraction on Kelvin Structures with Upper and Lower Resistive Layers," *IEEE Transactions on Electron Devices*, Vol.47, No.7, July 2000.

[13] A.S. Prabhu, D.B. Barker, and M.G. Pecht, "A Thermo-Mechanical Fatigue Analysis of High Density Interconnect Vias," *Advances in Electronice Packaging*, ASTM EEP 10-1, Vol.10, pp.187-216, 1995.

[14] Comsol Incorporated, Comsol multiphysics modelling software, 2007.

[15] I. Grosse, J. DiTomasso (University of Massachusetts), "Finite Element Modeling and Analysis of MCM High Density Interconnect Vias," *Final Technical Report*, RL-TR-96-109, June 1996.