A Regulated, Charge-Pump CMOS DC/DC Converter for Low-Power Applications

by

Jooyoun Park

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of

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Abstract

A regulated, low-power charge-pump DC/DC converter implemented in CMOS technology has been designed and extensively simulated in HSPICE. The charge-pump circuit is able to generate both positive and negative voltages. The converter consists of a charge-pump circuit operated at 500kHz from a +5V supply and a pair of op-amps which function as the regulation mechanism. The desired output voltages, +7.5V and -2.5V, are generated by the op-amps where the charge-pump supplies the rail voltages beyond the nominal V_{SS} of 0V and the nominal V_{DD} of +5V. Given a 2mA load, the target output voltages of -2.5V and +7.5V are reached to within 1 mV, with an output ripple $\leq$ 2mV. The efficiency of the converter pair is 51%.

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/Jooyoun Park

ASSIGNMENT

Draper Laboratory Report Number T-1303

In consideration for the research opportunity and permission to prepare my thesis by and at The Charles Stark Draper Laboratory, Inc., I hereby assign my copyright of the thesis to The Charles Stark Draper Laboratory, Inc., Cambridge, Massachusetts.

Jooyoun Park Date

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Chapter 1

Introduction

1.1 The Need for On-Chip Power Converters

The demand for low-power applications and the proliferation of battery-powered devices have resulted in a steady decrease in the supply voltages of integrated circuits (ICs). The power savings that result from a decrease in the supply voltage has been one of the prime motivators for current research efforts which focus on the development of circuit topologies that can operate with 1.2V or lower supplies.

There is, however, a limit to which supply voltages can be lowered before performance is adversely affected, particularly in analog designs. Care must be taken such that an across-the-board lowering of the voltages will not result in some subcircuit being placed out of its range of functionality. In mixed-signal IC's, for example, where analog and digital circuits coexist on the same substrate, the problem of circuits requiring different operating voltages emerges: digital circuits can often operate at lower voltages than analog circuits. A similar situation arises in any chip where all of the subcircuits do not share the same minimum operating voltage. In such ICs how does one minimize power consumption?

One idea is to power the chip with several supply levels. This will decrease the aggregate power consumption; however, the cost of manufacturing a product which incorporates such a chip will increase since several external supplies will be required. The current trend in chip design is to move away from multiple supplies in favor of one. Given one low voltage supply, how does one generate the requisite voltages for all the different subcircuits? One solution, which will be explored in this thesis, is to use on-chip DC-DC converters.

As more functional subcircuits are integrated on a single chip, and as devices become smaller and more densely packaged, on-chip power converters will become increasingly necessary. A piece of consumer electronics currently in development that addresses the issue of integrating multiple supply rails on-chip is the InfoPad terminal being developed at the University of California at Berkeley. The InfoPad is a hand-held personal communication system whose electronics require the generation of +5V, -17V, +12V and +1.5V, all from a single 6V battery. This battery is responsible for powering the baseband circuitry, the encoder/decoders for data compression, the A/D and D/A converters, the spreader and despreader for spread spectrum RF communication, the RF transceiver, and the flat-panel display [1].

1.2 Motivation for a Regulated CMOS Charge-Pump DC-DC Converter

In lowering manufacturing costs and making devices lightweight, an on-chip DC-DC converter is preferable to one that is off-chip. Discrete off-chip components tend to add to the cost, size and weight of a device. Among the currently available IC processes, the implementation of a DC-DC converter in CMOS is desirable since CMOS is currently the technology of choice for low-power design. The popularity of CMOS is largely due to the ease in designing circuits with minimal static power dissipation. In the interest of minimizing size and cost, the DC-DC converter presented in this thesis will not make use of off-chip magnetic elements such as inductors or transformers. Instead, off-chip capacitors will constitute the only external elements. A charge-pump, which requires only capacitors and integrated switches, will thus be used as the primary voltage conversion mechanism.

In order for the charge-pump to function as a voltage regulator, the circuit must be controlled by a feedback mechanism. The regulation scheme that will be featured in this thesis will be one that takes advantage of the regulation capabilities of an op-amp. Other control schemes exist such as linear feedback regulation; the research group that supports

this thesis has implemented a working, charge-pump converter that is controlled by a linear regulator. This thesis will also discuss Pulse-Width Modulation (PWM) and Pulse-Frequency Modulation (PFM) as alternative control schemes that can be used for applications with design specifications different from that of the converter featured in this thesis.

1.3 Outline of Thesis

The following is a list of topics presented in this thesis:

- **Chapter 2** discusses the specifications of the converter.
- **Chapter 3** features an analysis of the charge-pump.
- **Chapter 4** features an analysis of the Op-Amp regulator, along with simulation results of the complete charge-pump/regulator circuit.
- **Chapter 5** discusses PWM and PFM as alternative control schemes.
- **Chapter 6** is the conclusion.

Chapter 2

Design Specifications and Methods

2.1 Performance Goals

To aid in the investigation of the charge-pump regulator using the op-amp control scheme, a set of nominal specifications was established:

Output Voltage	+7.5V, -2.5V
Current Output	2mA nominally (varies from 1.5mA to 2.5mA)
Clock Input	2MHz±30%
Supply Voltages Provided	+5V nominally (varies from 4.75 to 5.25V), 0V
Reference Voltage Supplied	+2.5V
Power Supply Rejection	-14dB, from DC to 40kHz
Load Regulation	10mV/mA, from DC to 40kHz
Output Ripple	Less than $5mV_{pp}$
Time to Reach 90% Output	Less than 50ms
Efficiency	Greater than 40%

Table 2.1: Design Specifications

The above specifications are not those of a typical converter. One prominent atypical figure is the efficiency requirement: Most commercial power converters have an efficiency of at least 90%. In such high-efficiency converters, the power consumed by the converter itself is small compared to that delivered to the load. In contrast, the charge-pump that is featured in this thesis drives a relatively light load (~2mA), and will thus be considerably lower in efficiency than most commercial power converters. According to one study, a conventional charge-pump may require about 6mA to operate at no load [2]. As a consequence, the amount of power needed to operate the converter circuit itself would be comparable to the amount of power it needs to deliver, resulting in lower efficiency.

2.2 Design Method

The complete power converter, which consists of the charge-pump and its regulation circuit, was extensively simulated in HSPICE using Level 49 models for a high voltage process. The converter's performance measurements consisted mainly of transient simulations, from which the output voltage, output ripple, power supply rejection, load regulation, rise time and efficiency can be determined.

A monolithic form of the converter was not fabricated at the time of the writing of this thesis.

Chapter 3

Voltage Generation: A CMOS Charge-Pump

3.1 Overview of Charge-Pump Circuits

Charge-pumps are widely used in both analog and digital electronics. They perform the voltage conversion by storing charge on a capacitor and then changing the reference of one of its terminals; the capacitor is referenced to either terminal depending on a step-up conversion or a polarity inversion. The shuttling of charge into and out of the charge transfer capacitors is effected by transistor switches operated at frequencies typically between hundreds of kilohertz up through tens of megahertz.

Charge-pumps are often used as voltage doublers for the purpose of generating bias voltages. For example, they are incorporated in flash memory cells and EEPROMS so that the requisite bias voltages can be generated for erasing and programming operations [3],[4]. Such bias generators tend to require minimal (if any) voltage regulation; often the charge-pumps are run in an open-loop fashion. Most of the references for charge-pump circuits in the current literature focus on the bias-generation function and not on its use as a regulated voltage supply; they do not drive heavy loads but rather gates. The focus of this thesis, however, will be on a regulated charge-pump DC-DC converter that will function as a power supply.

3.2 Description of Charge-Pump Circuit Under Study

Among the various charge-pumps featured in the literature, the one that was chosen for this thesis is a topology analyzed by C. Wang and J. Wu [2]. One of the advantages of this charge-pump is that it does not involve the driving of large storage capacitors (0.1μF-1μF) by a clock buffer. The loading of clock buffers produces large transient switching currents which would interfere with the operation of the circuit the converter is powering, in addi-

tion to decreasing the efficiency. Hence, rather than driving the charging capacitors directly (which is a common scheme found in several papers), this charge-pump utilizes transistor switches in switching the references of the storage capacitors from either V_{DD} or GND. This topology is capable of generating both positive and negative voltages, and is not limited to a particular IC process.

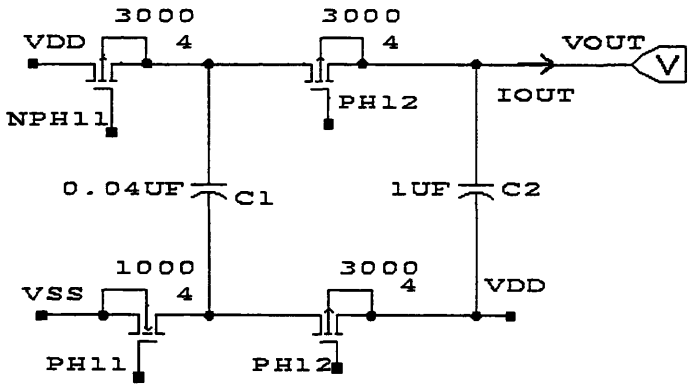


Figure 3.1: Positive Voltage Generator

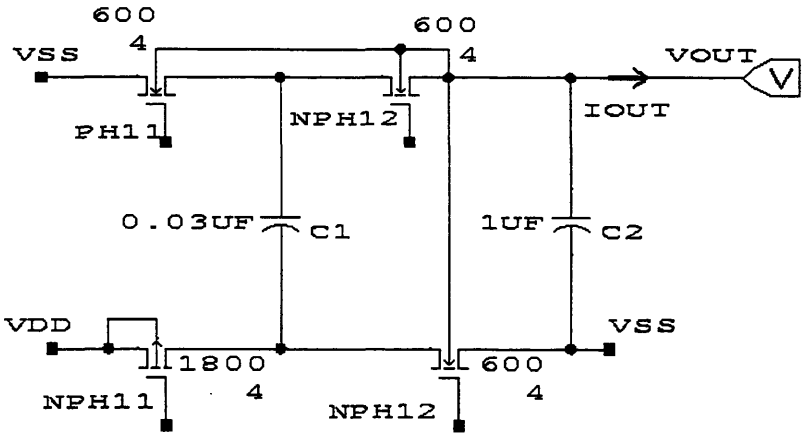
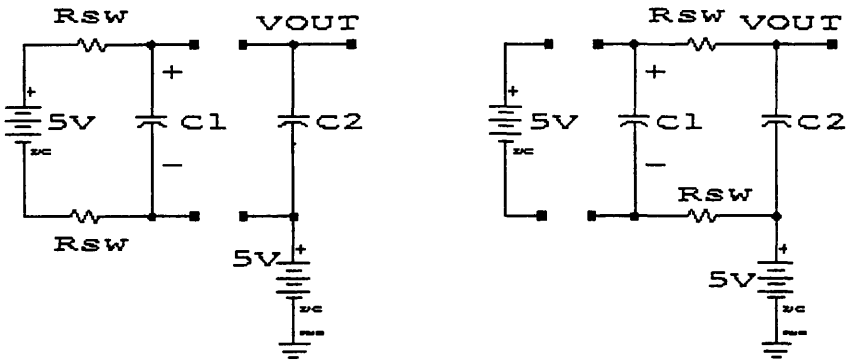


Figure 3.2: Negative Voltage Generator

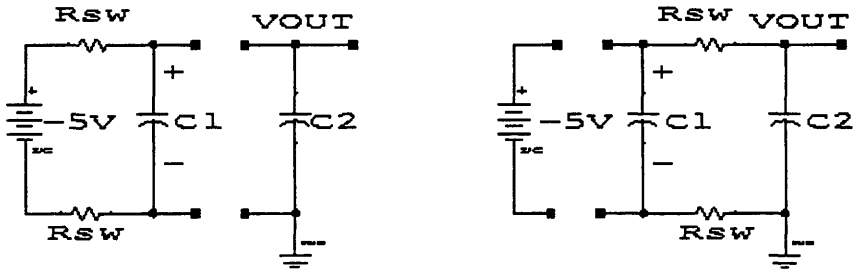
3.2.1 Operation of the Charge-Pump

The charge-pump circuit is able to step-up voltages or invert them by charging a capacitor on a fraction, D, of the switching period, T, and then stacking the capacitor on either V_{DD} or GND for a time (1-D)T. The following figures illustrate this process:



(a) 0 < t < DT (b) DT < t < T

Figure 3.3: The Two Switching Phases of Positive Voltage Generation



(a) 0 < t < DT (b) DT < t < T

Figure 3.4: The Two Switching Phases of Negative Voltage Generation

3.2.2 Dynamic (Transient) Response

The transient response is useful for determining the dynamic characteristics of the charge-pump as it reaches its steady-state voltage. The transient behavior was captured through average equations [10]. Averaged circuits models are a common means of characterizing high frequency switching DC/DC converters. The average of a variable is taken over one period, T, where the values of the variable when the switches are on and off are weighted in the average by the duty ratio, D, and its complement, 1-D, respectively. The variable that is averaged is one that is subject to the constraint equations imposed by Kirchoff's voltage and current laws: KVL and KCL. Since KVL and KCL are linear and time-invariant, their forms are not changed by averaging. In the analysis that follows, the averaged variables that are used to arrive at a closed-form expression for the output voltage are the currents through the charge transfer capacitors, $C_1 dV_{C1}/dt$ and $C_2 dV_{C2}/dt$.

Looking at Fig. 3.5, the expressions for dV_{C1}/dt and dV_{C2}/dt were derived:

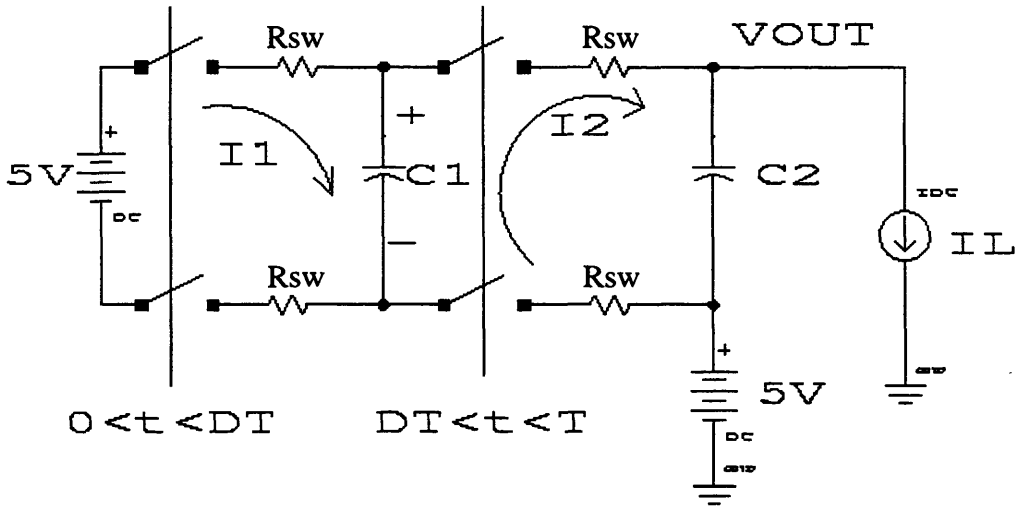


Figure 3.5: Positive Voltage Generator Used in Deriving the Average Equations

• **Calculating dV_{C1}/dt:**

For $0 < t \leq DT$,

$$V_{DD} - R_{sw}C_1dV_{C1}/dt - V_{C1} - R_{sw}C_1dV_{C1}/dt = 0$$

$$2R_{sw}C_1dV_{C1}/dt = V_{DD} - V_{C1} \tag{3.1}$$

For $DT < t \leq T$,

$$V_{C2} = R_{sw}C_1dV_{C1}/dt + V_{C1} + R_{sw}C_1dV_{C1}/dt$$

$$2R_{sw}C_1dV_{C1}/dt = V_{C2} - V_{C1} \tag{3.2}$$

Averaging (3.1) and (3.2) leads to an expression for $d\langle V_{C1}\rangle/dt$, where $\langle . \rangle$ denotes an averaged variable:

$$2R_{sw}C_1d\langle V_{C1}\rangle/dt = D(V_{DD} - \langle V_{C1}\rangle) + (1-D)(\langle V_{C2}\rangle - \langle V_{C1}\rangle)$$

$$d\langle V_{C1}\rangle/dt = [-\langle V_{C1}\rangle + (1-D)\langle V_{C2}\rangle + DV_{DD}]/(2R_{sw}C_1) \tag{3.3}$$

• **Calculating dV_{C2}/dt:**

For $0 < t \leq DT$,

$$C_2dV_{C2}/dt = -I_L \tag{3.4}$$

For $DT < t \leq T$,

$$C_2dV_{C2}/dt + I_L = C_1dV_{C1}/dt$$

$$C_1dV_{C1}/dt = (V_{C1} - V_{C2})/2R_{sw}$$

$$C_2dV_{C2}/dt = -I_L + (V_{C1} - V_{C2})/2R_{sw} \tag{3.5}$$

Averaging (3.4) and (3.5) leads to an expression for $d\langle V_{C2}\rangle/dt$:

$$C_2d\langle V_{C2}\rangle/dt = -DI_L - (1-D)I_L + (1-D)(\langle V_{C1}\rangle - \langle V_{C2}\rangle)/2R_{sw}$$

$$d\langle V_{C2}\rangle/dt = [(1-D)\langle V_{C1}\rangle - (1-D)\langle V_{C2}\rangle - 2R_{sw}I_L]/(2R_{sw}C_2) \tag{3.6}$$

The final expression for the output voltage of the charge-pump is

$$V_{OUT} = \langle V_{C2} \rangle + V_{DD} \tag{3.7}$$

and the average equations (3.3) and (3.6) are

$$d\langle V_{C1} \rangle/dt = [-\langle V_{C1} \rangle + (1-D)\langle V_{C2} \rangle + DV_{DD}]/(2R_{sw}C_1)$$

$$d\langle V_{C2} \rangle/dt = [(1-D)\langle V_{C1} \rangle - (1-D)\langle V_{C2} \rangle - 2R_{sw}I_L]/(2R_{sw}C_2)$$

Combining the equations for $d\langle V_{C1} \rangle/dt$ and $d\langle V_{C2} \rangle/dt$, an expression for the average voltage across C_2, $\langle V_{C2} \rangle$, was obtained. The d/dt operator was replaced by the complex frequency, s, using the Laplace transform:

$$\langle V_{C2}(s) \rangle = \frac{D(1-D)V_{DD} - 2R_{sw}I_L + 4R_{sw}^2C_1I_Ls}{4R_{sw}^2C_1C_2s^2 + [2R_{sw}C_2 + 2R_{sw}C_1(1-D)]s + D - D^2} \tag{3.8}$$

Evaluating $\langle V_{C2}(s) \rangle$ for s = 0 and substituting it into (3.7) results in a expression for the steady-state voltage:

$$V_{OUT} = 2V_{DD} - \frac{2I_LR_{sw}}{D(1-D)} \tag{3.9}$$

To illustrate the dynamic characteristics of the charge-pump, the following nominal values were substituted into (3.8):

- $D = 0.25$
- $R_{sw} = 30\Omega$
- $V_{DD} = 5V$
- $I_L = 2mA$
- $C_1 = 0.04\mu F$
- $C_2 = 1\mu F$

which resulted in the following expression for $\langle V_{C2}(s) \rangle$:

$$\langle V_{C2}(s) \rangle = \frac{0.818 + 2.88\times10^{-7}s}{1.44\times10^{-10}s^2 + 6.18\times10^{-5}s + 0.188}$$

which was entered into MATLAB to determine the pole-zero locations, and the step (Fig. 3.6) and frequency (Fig. 3.7) responses. The zero was at 2.84×10^6 rad/sec; the poles were at 3.06×10^3 rad/sec and 4.26×10^5 rad/sec.

According to the step response (Fig. 3.6), where the input was stepped from 0 to V_{DD}, the system can be modeled as a single-pole system to a first-order approximation with the low pole at 487 Hz dominating the response with the damped, exponential rise. The dominant pole approximation, where the following relation must be satisfied,

$$P_2/P_1 >> 10 \tag{3.10}$$

holds for this system since the ratio of second pole, P_2, to the first pole, P_1, is 139. Hence, the transient response can be modeled as a dominant pole effect rather than an overdamped second-order system. From the phase plot (Fig. 3.7), the charge-pump is stable.

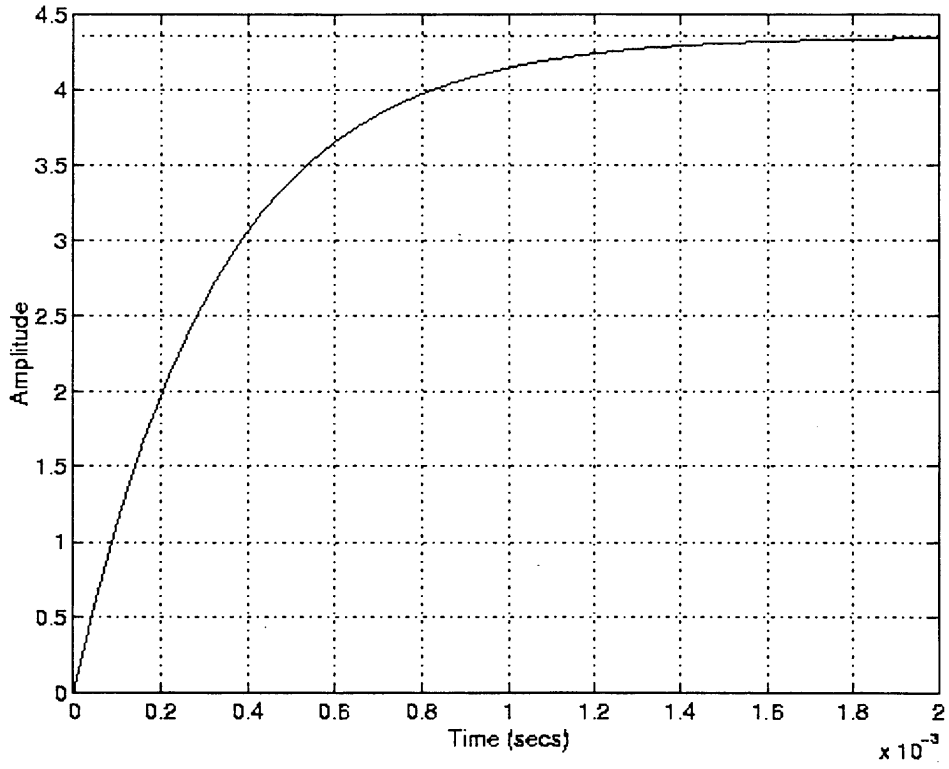


Figure 3.6: Transient Response of Charge-Pump: $<V_{C2}> = V_{OUT} - V_{DD}$

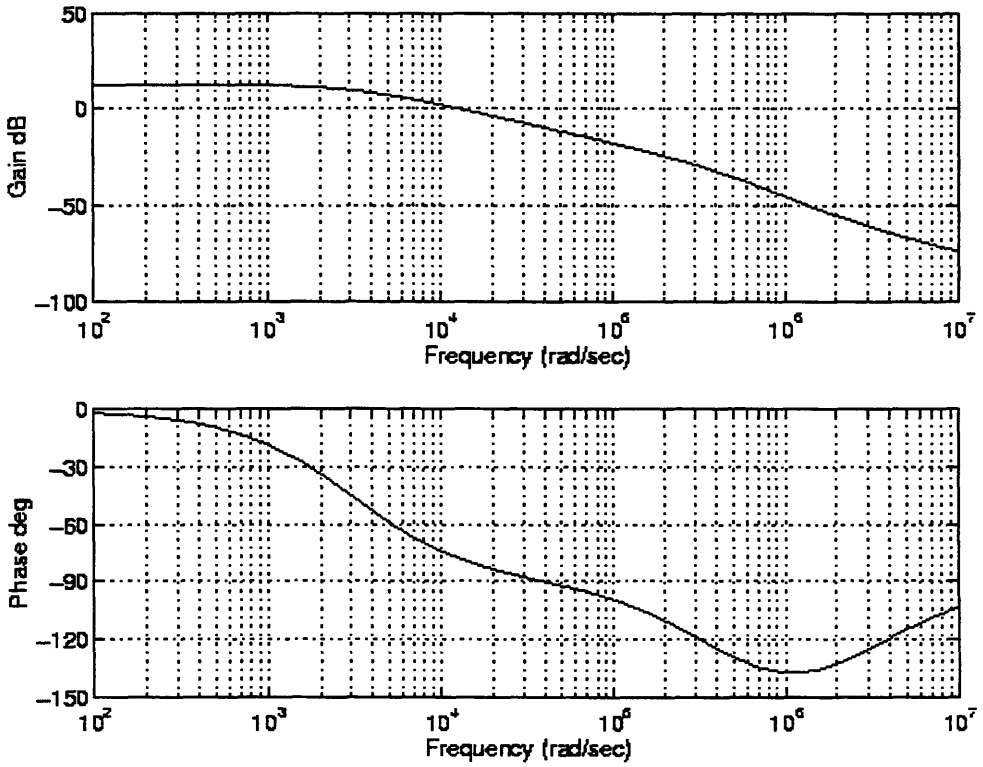


Figure 3.7: Bode Plot of $<V_{C2}>$: V_{OUT}-V_{DD}

3.2.3 Clock Speed and Capacitors

The choice of capacitor sizes for the charge-pump is directly related to the clocking of the switches. There is an inverse relation between the switching frequency and the size of the charge-transfer capacitors. Given a 2MHz clock, it is difficult to optimize the efficiency of the charge-pump because of the dynamic switching losses. Thus, the clock frequency was divided down to 500kHz. The clock was not divided down further since the power converter's switching frequency had to be several times greater than the operating frequency of the circuit it was powering, which, in this case, was at 20kHz. Keeping the

switching frequency at least an order of magnitude above the operating frequency of the circuit being powered facilitates supply filtering.

In dividing the clock, a cascade of two divide-by-2 Moebius counters [5] was used in lowering the 2MHz switching frequency by a factor of 4 to 500kHz.

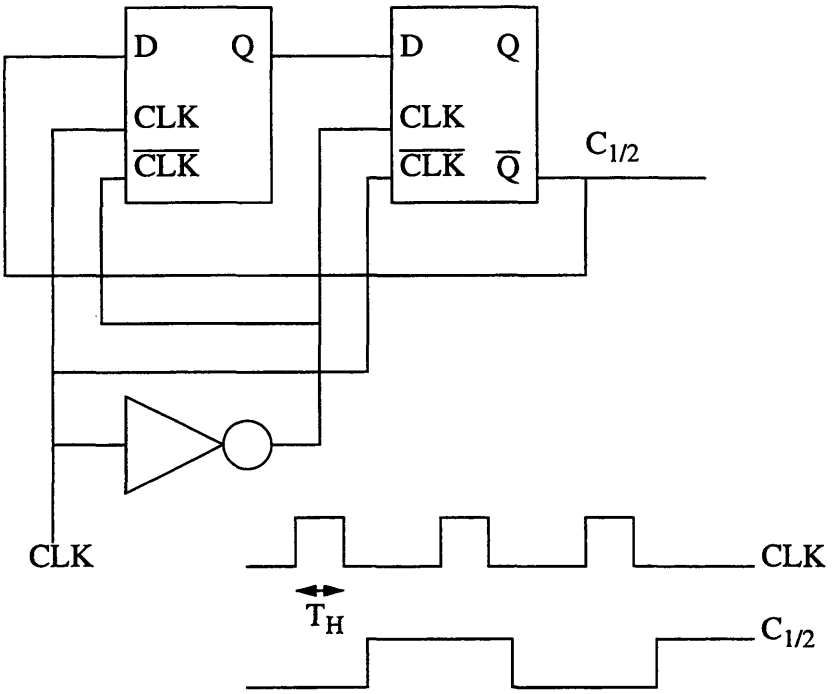


Figure 3.8: Moebius Counter (f/2 generation)

As shown in Fig. 3.8, the Moebius counter can take a clock signal, CLK, with an arbitrary pulse width, T_H, and produce an output clock that is exactly half of the input frequency with a 50% duty ratio. The circuit is composed of two D-registers [6].

After choosing a clock frequency of 500kHz, the capacitor sizes were chosen. In the paper where this charge-pump was analyzed, both of the capacitors, C_1 and C_2 (as shown in Fig. 3.5), had a value of 1μF, and the clock was approximately 20kHz at full loading.

The values of the charge-transfer capacitor, C_1, and the output capacitor, C_2 are related to the switching frequency and the output ripple, respectively. Since the switching frequency was 500kHz, the value of capacitor C_1 was divided by a factor of 500kHz/20kHz, or about 25, from 1μF to 0.04μF. This value for C_1 is an approximation and can vary between 0.01μF and 1μF, depending on the efficiency and the rise time.

The value of the output capacitor, C_2, was unchanged because of the ripple spec. At a switching frequency of 500kHz, the amount of charge per cycle delivered to the 2mA load at steady-state is $Q = I_L T = (2mA)(2\mu s) = 4x10^{-9}$ coul. For a ripple voltage, V_r, less than 5mV, C_2 needs to be at least $Q/V_r = 0.8\mu F$. Thus, C_2 was set at 1μF.

The capacitor values are large enough such that they have to be external components. It may be possible, with considerable silicon area, to break down the charge-pump into many smaller charge-pumps with capacitors that are all integrated. Although this option eliminates the need for external capacitors, it may result in a considerably less efficient converter. Because an integrated capacitor always has a stray capacitance to ground, an external capacitor is preferable. In one study, the maximum efficiency possible with a poly-metal capacitor was 50%, whereas an efficiency of 97% was achieved with an external capacitor under certain load conditions [7].

3.2.4 Switch Resistances

The equivalent resistances, R_{sw}, of the switching transistors can be determined according to the desired output voltage as defined by (3.9). For a given R_{sw}, the width-to-length ratio, W/L, of the transistors can be calculated from the following equation which assumes, at steady-state, that the transistors are operating in the triode region, neglecting the second-order effects [2].

$$R_{sw} = \frac{L}{\mu C_{ox} W (V_{GS} - V_T)} \tag{3.11}$$

3.2.5 Auxiliary Circuits Required for Operation of the Charge-Pump

In order to minimize short-circuit currents, the switches were operated in a "break-before-make" fashion, where the switches were opened and closed using non-overlapping clock phases.

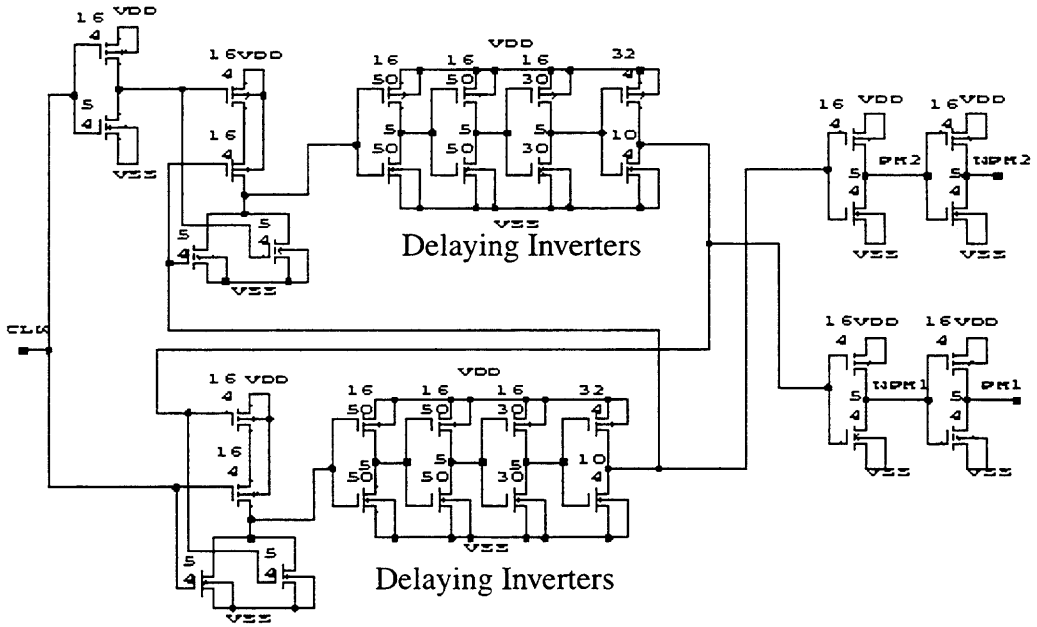


Figure 3.9: Break-Before-Make Circuit

This "break-before-make" circuit can be used to generate pulses with arbitrarily small duty-ratios by inserting delaying inverters [8].

When the charge-pump's output voltage increases beyond V_{DD} = +5V, the switching transistors need a gate voltage that is equal to or greater than the output voltage to shut off the transistor [2]. Otherwise, the transistor will remain on all the time, resulting in considerable short-circuit power loss. An analogous situation holds for the negative voltage generator, where the gates need to be biased at or below the output voltage of -2.5V to completely turn off. Hence, a level shifter is needed in each case, which generates a bias voltage for the gates of the transistor switches that is equal to the output voltage. In order to prevent latch-up, a startup circuit is required for the +7.5V generator. The startup circuit provides the voltage for the level shifter until the output voltage of the +7.5V generator reaches +5V.

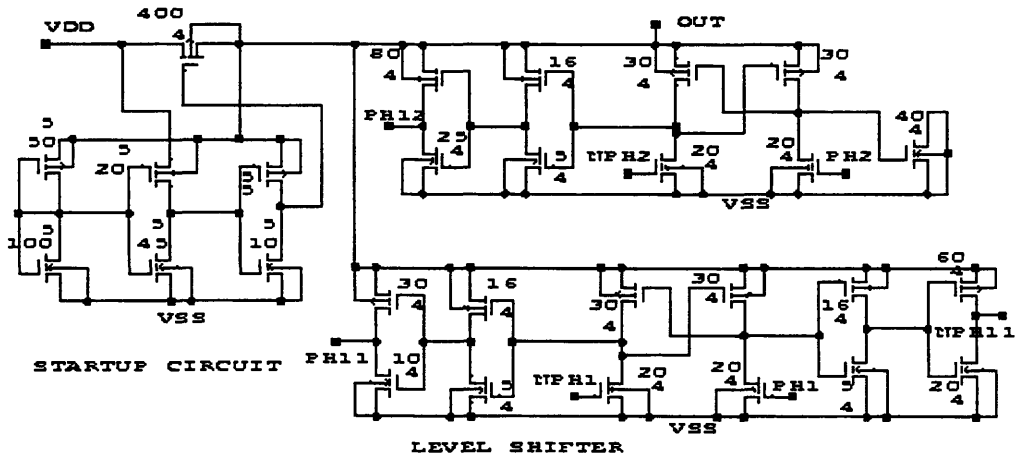


Figure 3.10: Startup-Circuit and Level-Shifter for Positive Voltage Generator

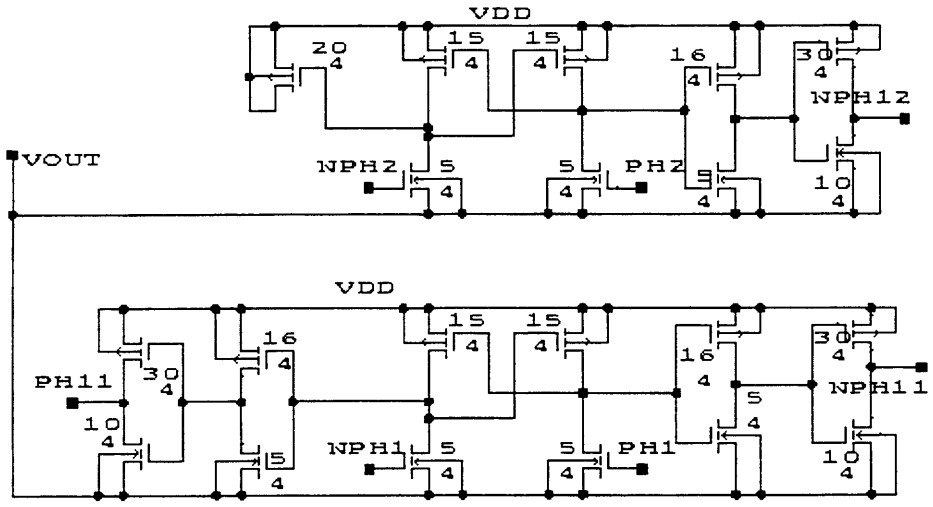


Figure 3.11: Level-Shifter for Negative Voltage Generator

Chapter 4

Output Regulation: Op-Amp Regulator

4.1 Operation of Regulator

One of the ways to generate a regulated voltage is to use an op-amp regulator. This method of regulation takes advantage of the inherent power-supply rejection and load regulation properties of an op-amp.

With an op-amp regulator, the charge-pump is run in an open-loop fashion. The steady-state output voltage is not the target voltage but a value close to a multiple of the supply voltage. In the case of the +7.5V generator, the charge pump reaches about $2V_{DD}$ at steady-state; for the -2.5V generator, the expected steady-state voltage is $-V_{DD}$. The output voltage from the charge-pump is then used as one of the supplies of an op-amp circuit which, in turn, generates the target voltage.

The output of the charge-pump voltage has to be high enough such that the supply terminals and the output voltage of the op-amp are far enough apart to ensure that the op-amp is operating in a region where all of its transistors are in saturation. Otherwise, the op-amp will track the power supply and load variations. In the transient simulations, the output of the charge-pump was at least +9.25V for the +7.5V generator circuit and more negative than -4.6V for the -2.5V generator.

The +7.5V generator circuit (Fig. 4.1) consists of a 3x, non-inverting op-amp circuit that is followed by a unity-gain buffer included in the feedback loop. The inclusion of the buffer is central to decreasing the output impedance of the op-amp circuit, enabling it to drive 2mA with a load variation of 1mA. Similarly, the -2.5V generator circuit (Fig. 4.2) consists of an inverting op-amp circuit followed by a unity gain-buffer included in the feedback loop.

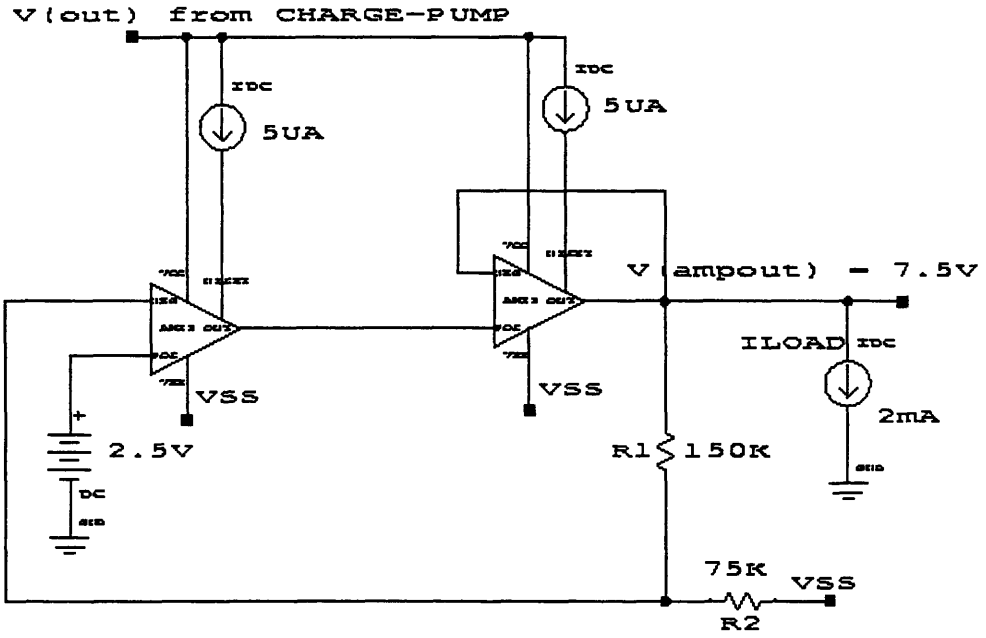


Figure 4.1: Op-Amp Circuit for Positive Voltage Generation (+7.5V)

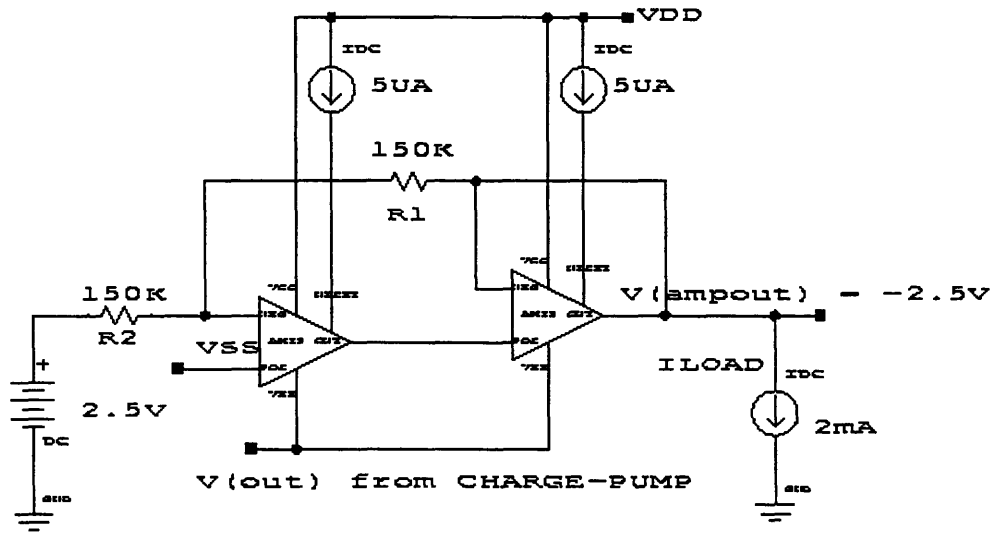


Figure 4.2: Op-Amp Circuit for Negative Voltage Generation (-2.5V)

4.2 Power Supply Rejection Estimate

In order to gauge how much regulation can be expected with the op-amp regulator under specific bias conditions (supply, output voltage, load) with a particular op-amp, power supply rejection (PSR) measurements were performed via HSPICE simulation. The charge-pump was replaced by an ideal supply for the purpose of estimation. The voltages and bias conditions used were:

- +7.5V Generator: Supply Voltages: +9.25V, 0V; Output Voltage: +7.5V
- -2.5V Generator: Supply Voltages: +5V, -4.6V; Output Voltage: -2.5V

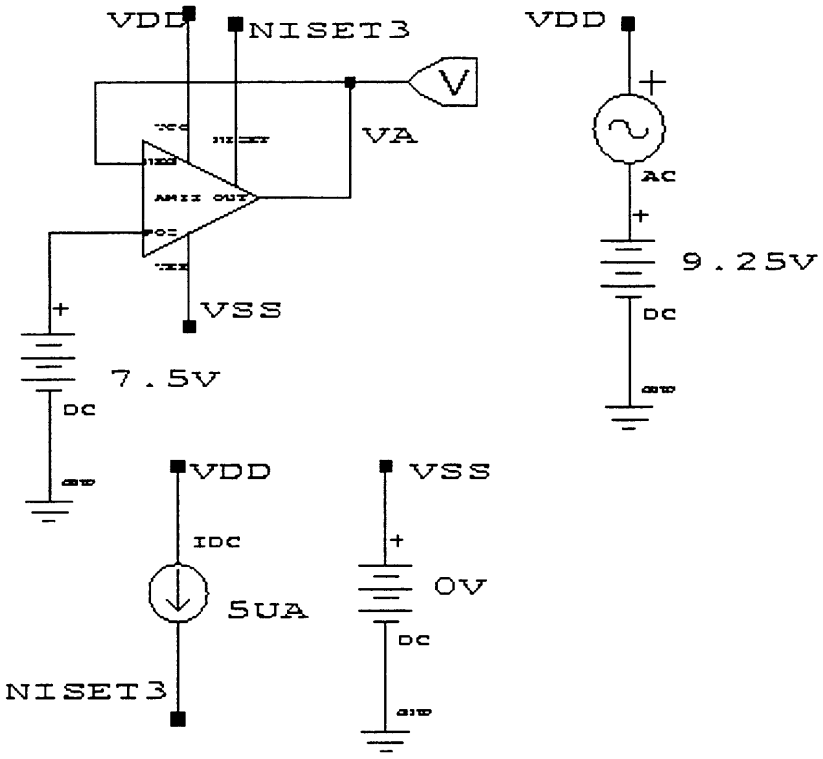


Figure 4.3: Test Circuit Used in Simulation of PSR for +7.5V Generator

In the test circuit shown in Fig. 4.3, the op-amp was biased such that output voltage was the target voltage. To model power supply variations from the charge-pump output, an ideal sinusoidal source with an amplitude of 1V was attached to the positive terminal (or

the negative terminal, in the case of the -2.5V generator). The supplies were ideal DC sources. A frequency sweep was then performed, resulting in a bode plot relating the output voltage normalized to 1V as a function of frequency.

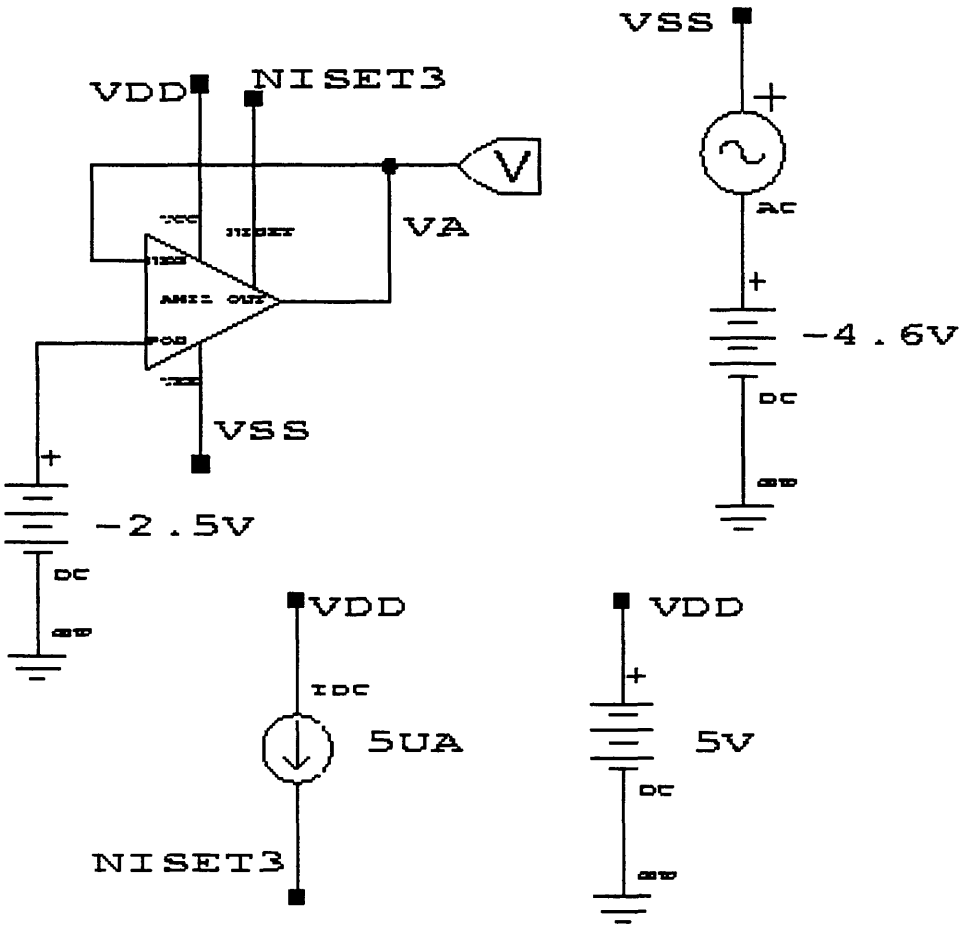


Figure 4.4: Test Circuit Used in Simulation of PSR for -2.5V Generator

The results of the power supply rejection simulations (Figs 4.5 and 4.6) provides an estimate that the supply rejection as required by the specs, -14dB from DC to 40kHz, should be comfortably met using the op-amp regulator.

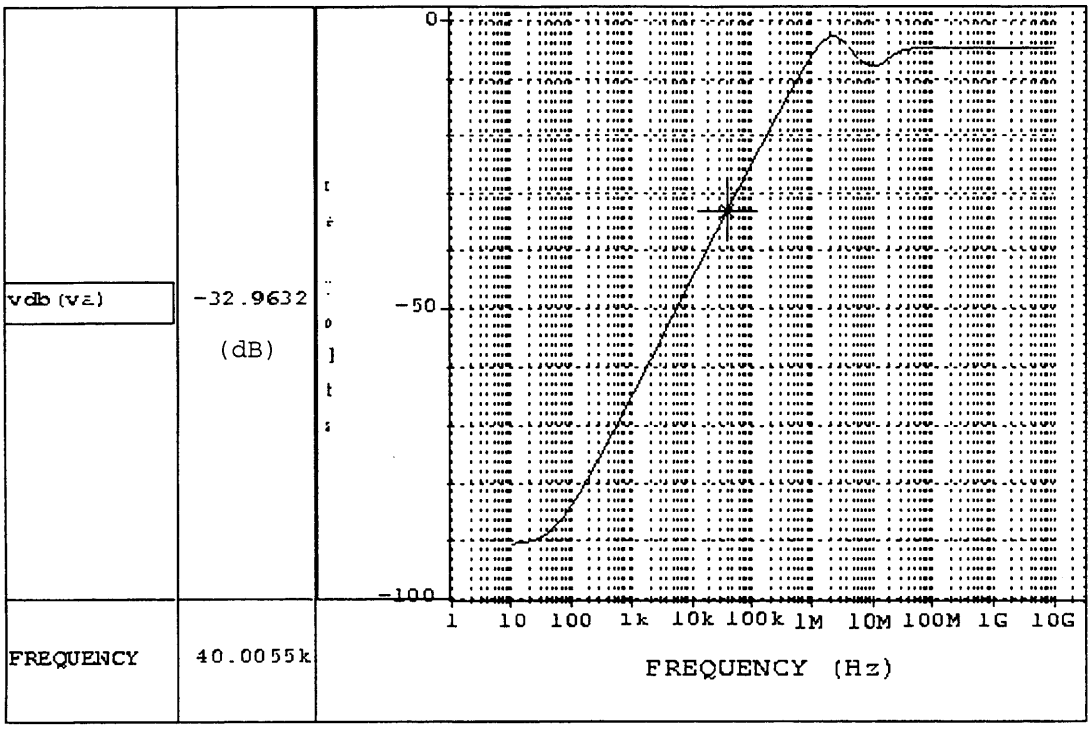


Figure 4.5: Estimated Power Supply Rejection: +7.5V Generator

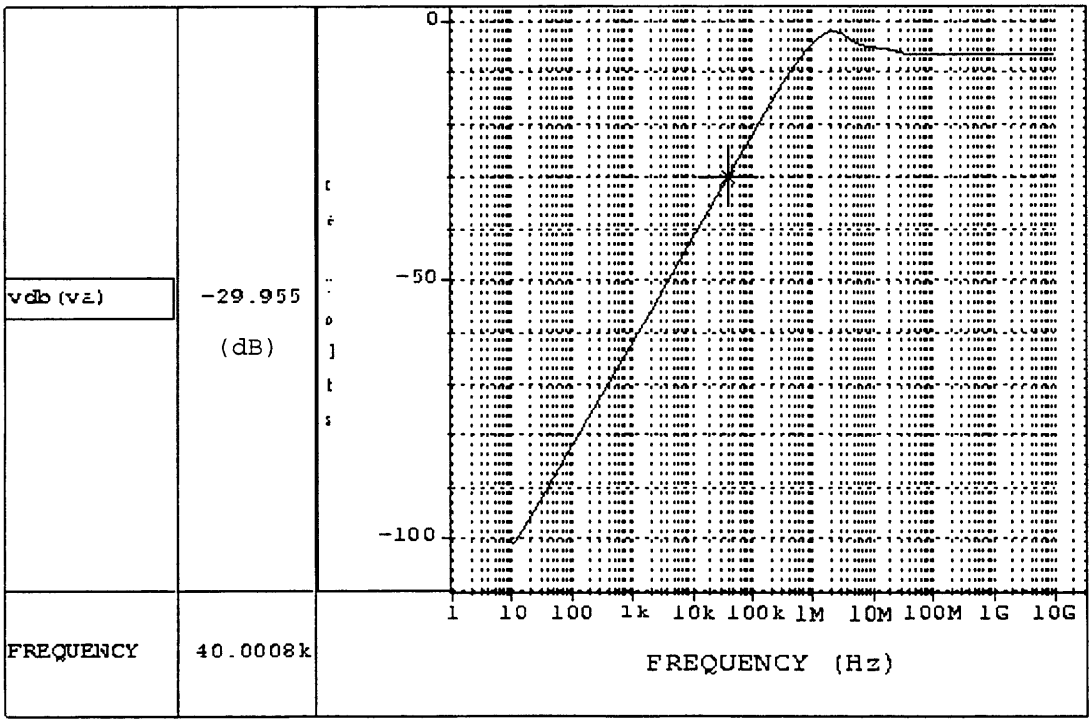


Figure 4.6: Estimated Power Supply Rejection: -2.5V Generator

4.3 Load Regulation Estimate

The capacity for load regulation was estimated using an ideal load that varied sinusoidally at 40kHz from 1.5mA to 2.5mA. The supply voltage provided by the charge-pump was modeled as an ideal source, as in the case of the PSR simulations. The operating voltages and bias conditions for the op-amp circuit were the following:

- +7.5V Generator: Supply Voltage: +9.25V, 0V; Output Voltage: +7.5V
- -2.5V Generator: Supply Voltage: +5V, -4.6V; Output Voltage: -2.5V

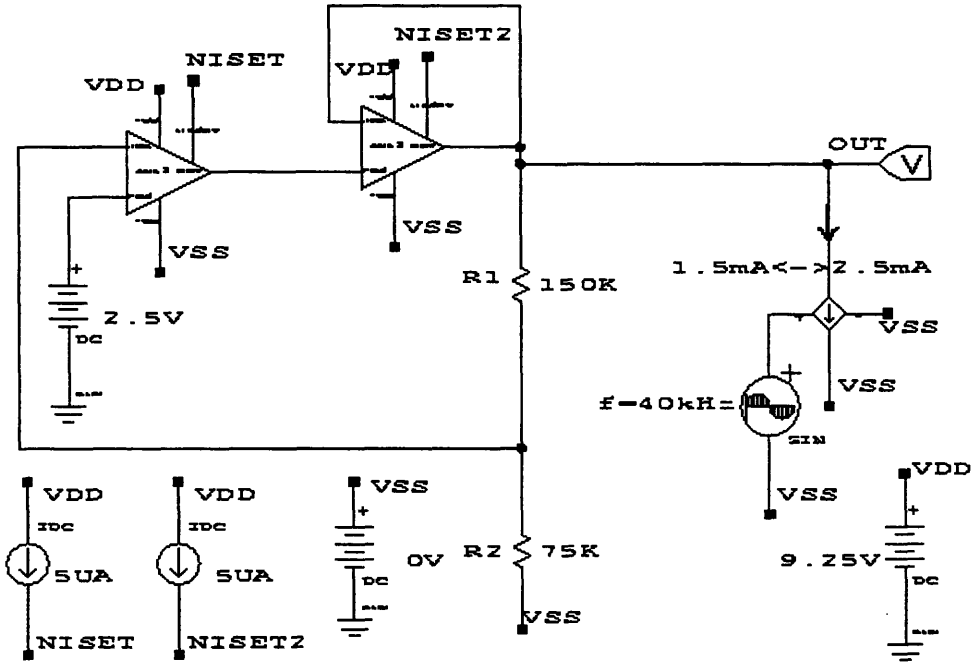


Figure 4.7: Test Circuit for Simulating Load Regulation +7.5V

According to the simulation results (Figs. 4.9, 4.10) it was estimated that the +7.5V and the -2.5V generators would have load regulation capabilities around 6mV/mA and 3mV/mA, respectively, which are within the 10mV/mA max. specification.

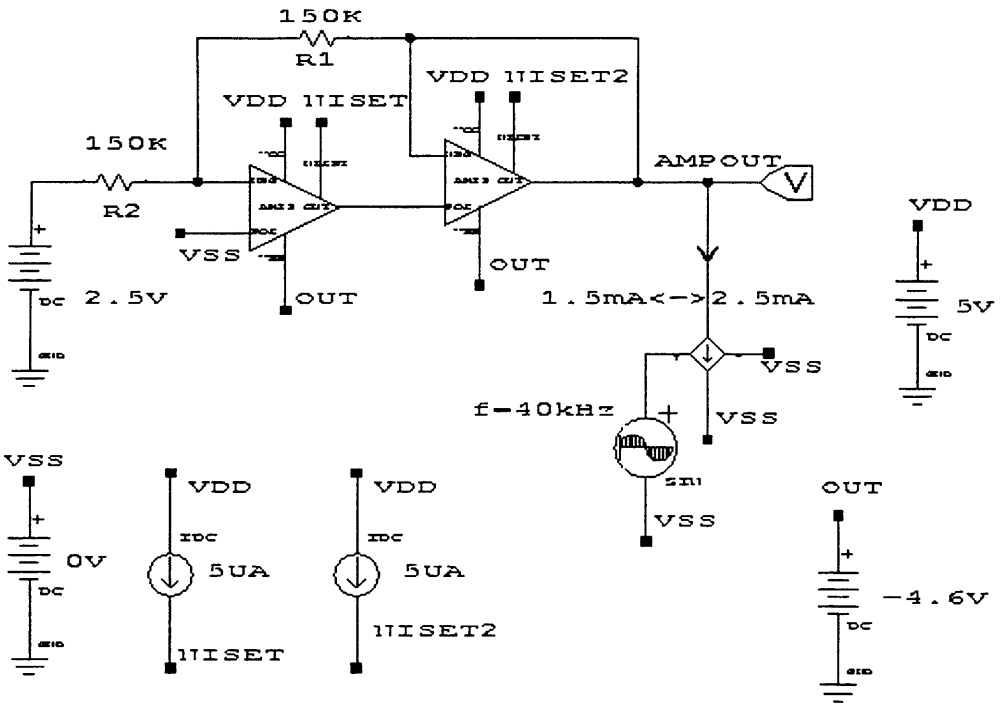


Figure 4.8: Test Circuit for Simulating Load Regulation: -2.5V

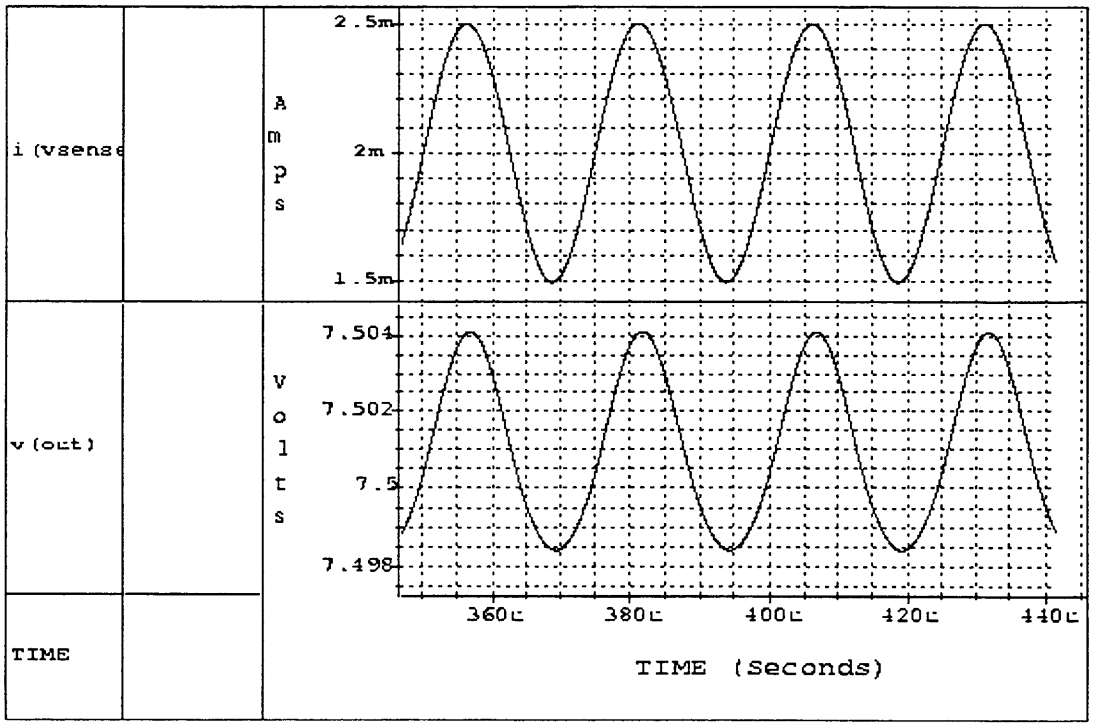


Figure 4.9: Estimated Effect of Load Variations on +7.5V Generator Output

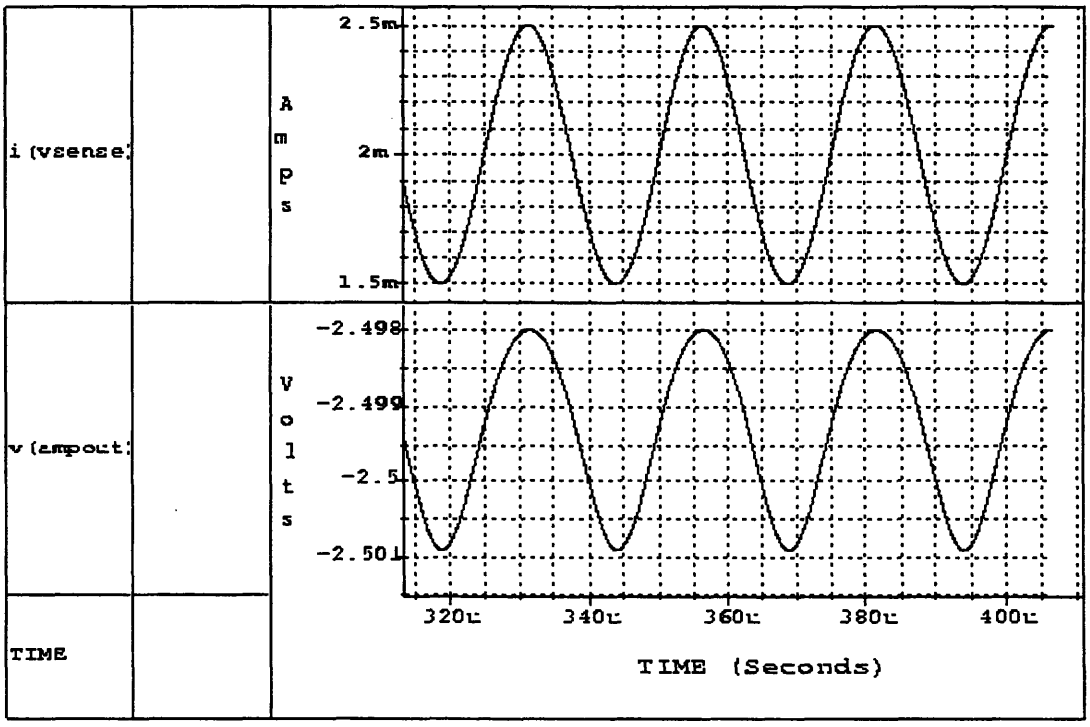


Figure 4.10: Estimated Effect of Load Variations on -2.5V Generator Output

4.4 Simulation Results: Transient Measurements of Complete Converter

4.4.1 Simulations Under Nominal Conditions

Transient response measurements were performed with HSPICE for the complete converter circuit which consists of the charge pump, the auxiliary circuits (break-before-make circuit, level-shifter, startup circuit), and the op-amp regulator. The +7.5V and -2.5V converters are featured in Fig. 4.11 and Fig. 4.12, respectively.

The nominal conditions under which the simulations took place are defined below:

- clock frequency: 500kHz
- V_{DD}: +5V
- Load: 2mA

From the plots of the transient response, one can extract the output voltage, the ripple, the efficiency, power supply rejection and load regulation. The latter two were simulated with a modified circuit with the appropriate sinusoidally varying circuit element (voltage source or load).

The plots use the following voltage and current variables:

- `v(ampout)` : Output of the Op-Amp regulator (the target voltage)
- `v(out)` : Output voltage of the unregulated charge-pump
- `v(vdd)` : Supply voltage, V_{DD}
- `i(vsense)` : Load current
- `i(vivdd)` : Current drawn from V_{DD}
- `average(i(vivdd))` : Average of the total current drawn from V_{DD} (used in efficiency calculation)

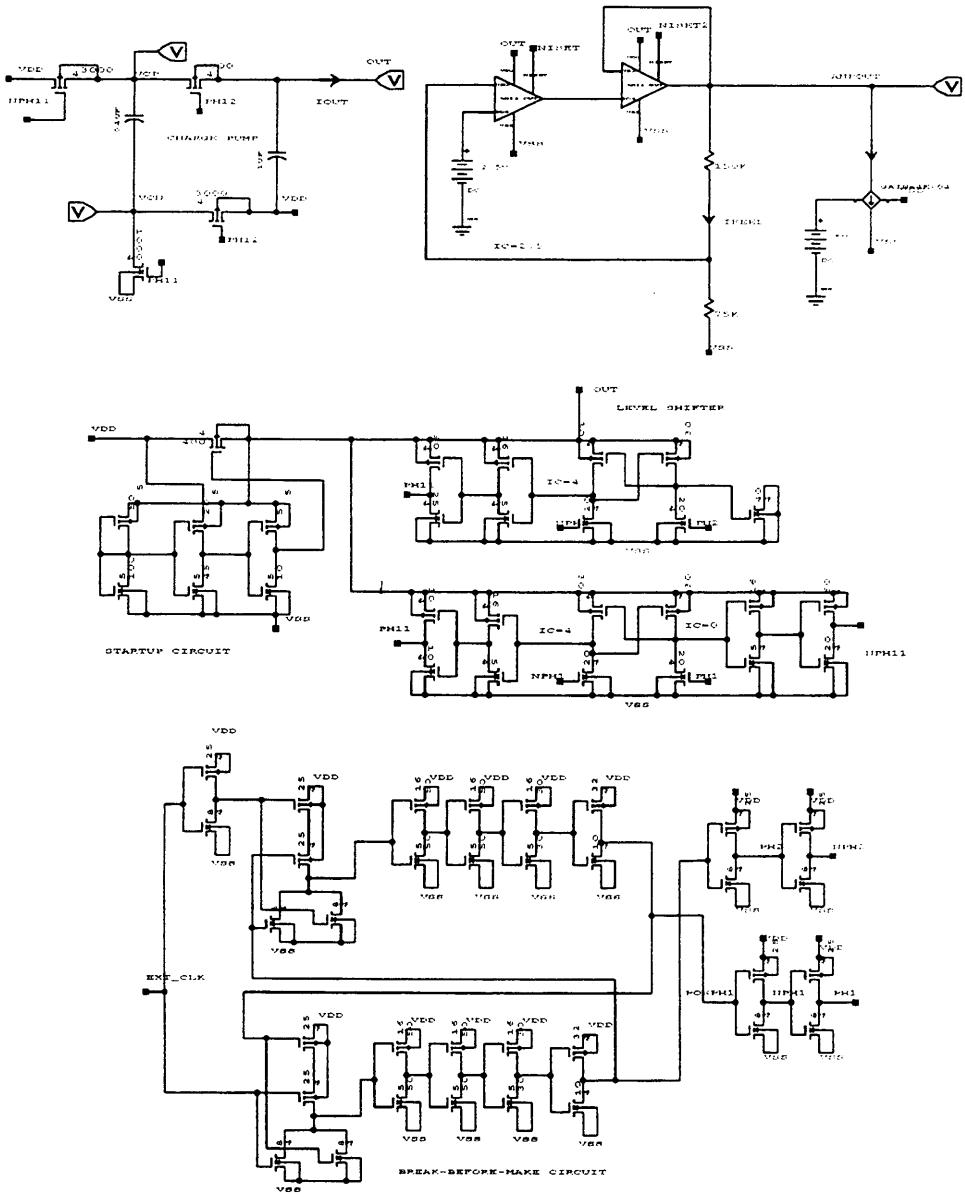


Figure 4.11: Complete Converter/Regulator Circuit for +7.5V Generation

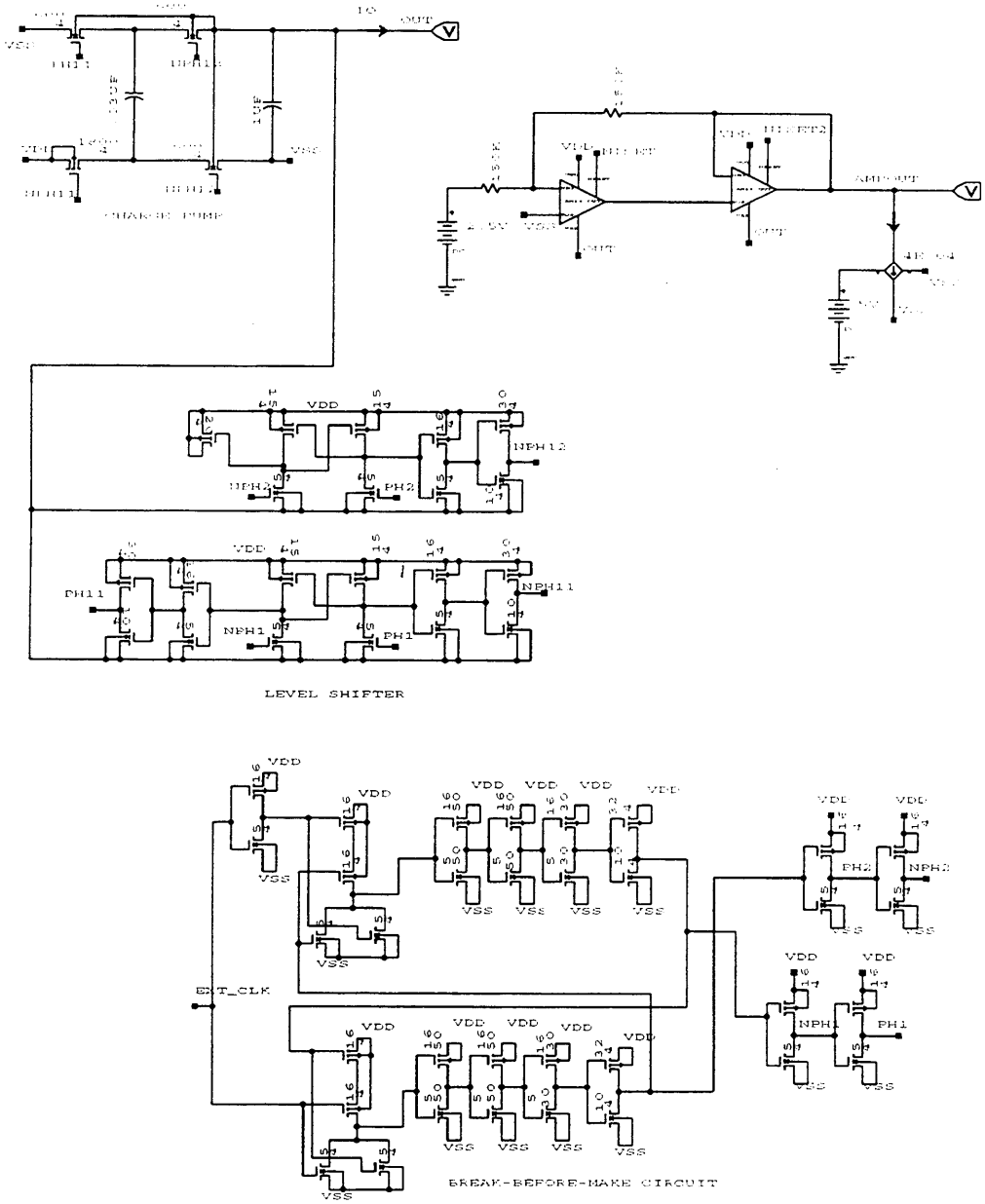


Figure 4.12: Complete Converter/Regulator Circuit for -2.5V Generation

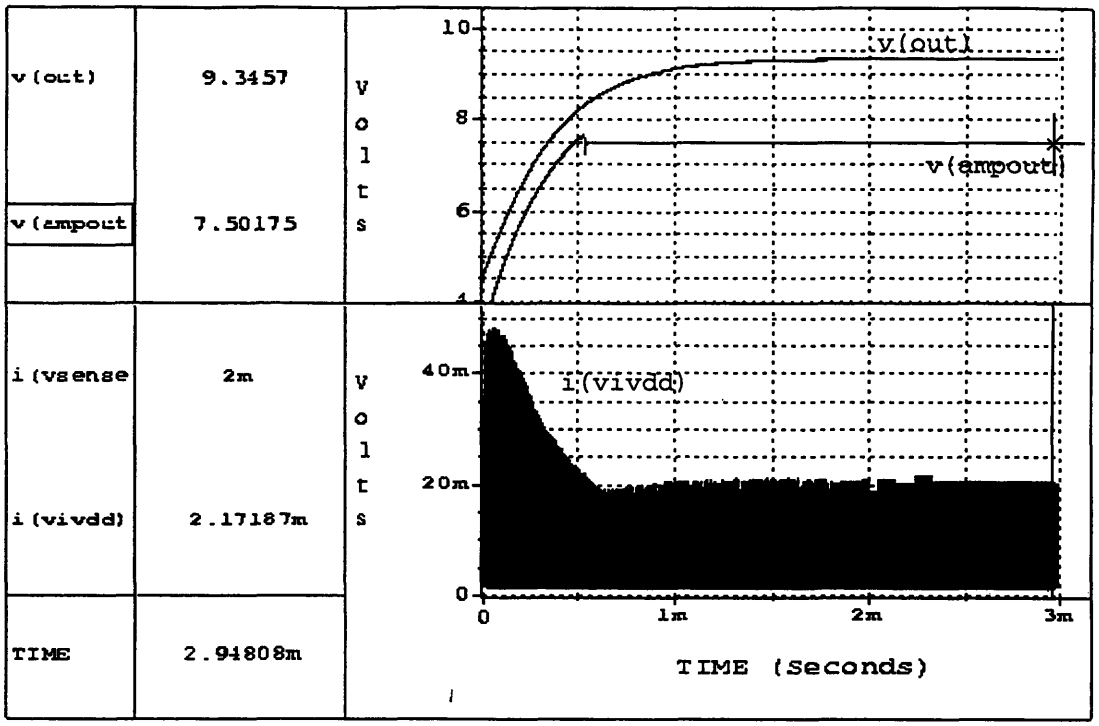


Figure 4.13: +7.5V Regulator Simulation: Nominal Conditions

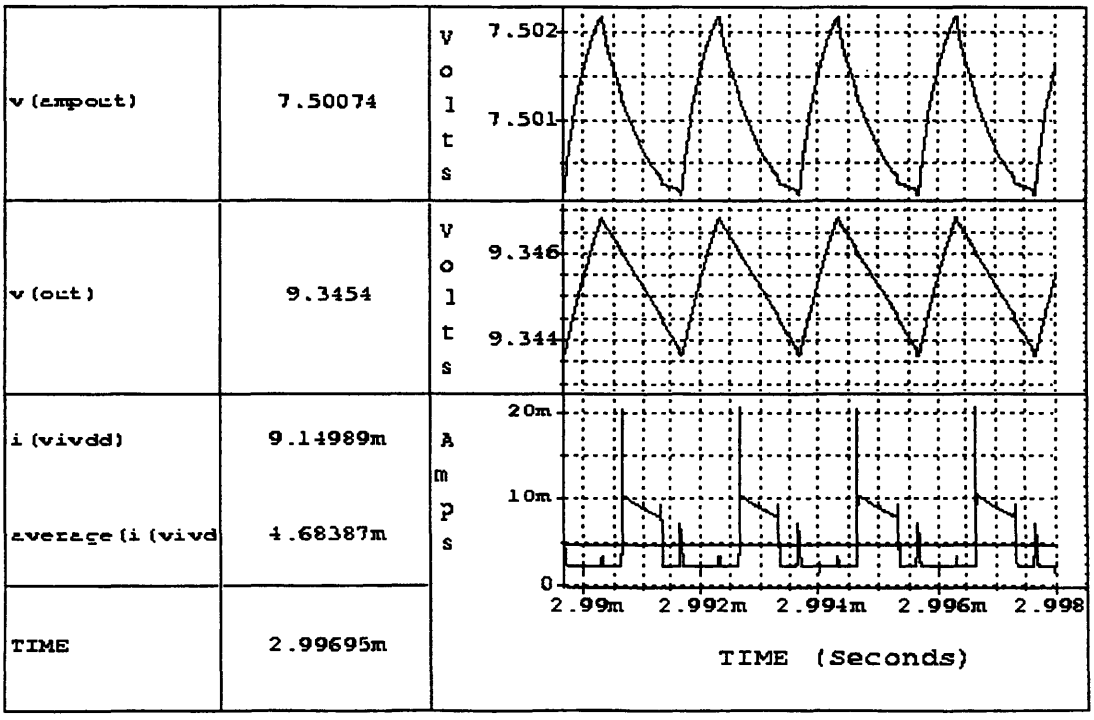


Figure 4.14: Steady-State Voltages and Currents for Fig. 4.13

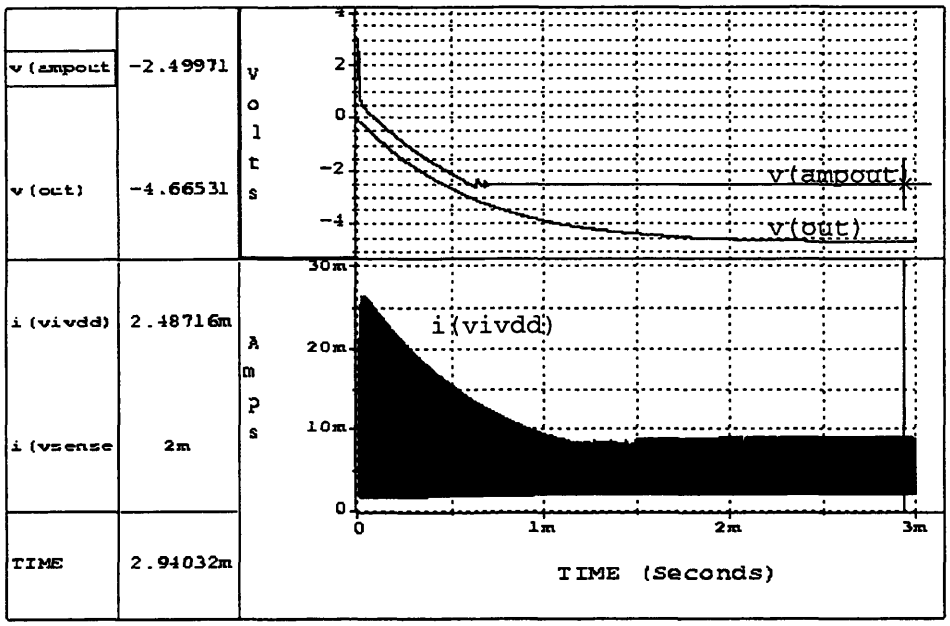


Figure 4.15: -2.5V Regulator Simulation: Nominal Conditions

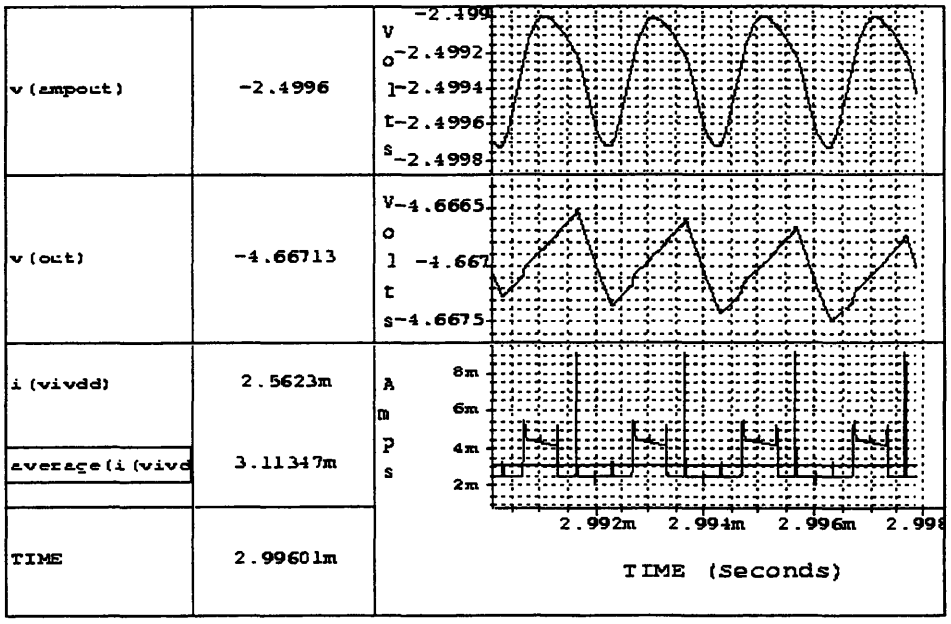


Figure 4.16: Steady-State Voltages and Currents for Fig. 4.15

From the plots of the +7.5V generator (Figs. 4.13, 4.14), the output voltage is +7.501V, the ripple voltage is 2mV and the efficiency is 64%. These values meet the required specifications summarized in Chapter 2.

From the plots of the -2.5V generator (Figs. 4.15, 4.16) the output voltage is -2.499V, the ripple voltage is 0.7mV, and the efficiency is 32%. The efficiency is drastically lower for the -2.5V generator since it is a step-down converter.

In actuality, the amount of charge delivered to the output capacitors of the +7.5V converter and the -2.5V converter are similar; the difference in the output voltages stems from where the voltage across the output capacitor is referenced. The stark disparity in the efficiencies between the +7.5V and -2.5V converter should be examined more closely since the two converters operate in the same manner. The efficiencies for the +7.5V and -2.5V converter were calculated according to the canonical definition of efficiency, which is the ratio of the output power to the input power. In the case of the +7.5V converter, the output voltage included the +5V offset from the supply since the output capacitor was referenced to it. For the -2.5V converter, only 0V was referenced. Hence, the fact that the +7.5V generator has twice the efficiency of the -2.5V converter is only due to the inclusion of the +5V offset in the step-up conversion.

An efficiency figure that may be more useful in evaluating the converter would be to conceptually combine the +7.5V and -2.5V converters, assuming that the magnitude of the output voltage is 10V while keeping the output current at 2mA. The input voltage would remain at +5V and the current drawn from the 5V supply would be the sum of the currents drawn by the +7.5V and the -2.5V converters. Calculating (10V)(2mA) results in 20mW for the output power; calculating (5V)(7.797mA) results in 38.99mW for the input power. Calculating the ratio of the output power to the input power results in an efficiency of 51%.

4.4.2 Power Supply Rejection Simulation

The power supply rejection (PSR) capabilities of the complete converter was simulated under the following conditions:

- Clock frequency: 500kHz
- V_{DD}: +5V±0.25V @ 40kHz
- Load: 2mA

From the plots of the +7.5V generator (Figs. 4.17, 4.18), the power supply rejection is -21.9dB and the average steady-state voltage is about 7.50V. These values meet the specifications in Chapter 2.

Similarly, from the plots of the -2.5V generator (Figs. 4.19, 4.20), the power supply rejection is -28.0dB and the average steady-state voltage is about -2.50V. These values also meet the specifications.

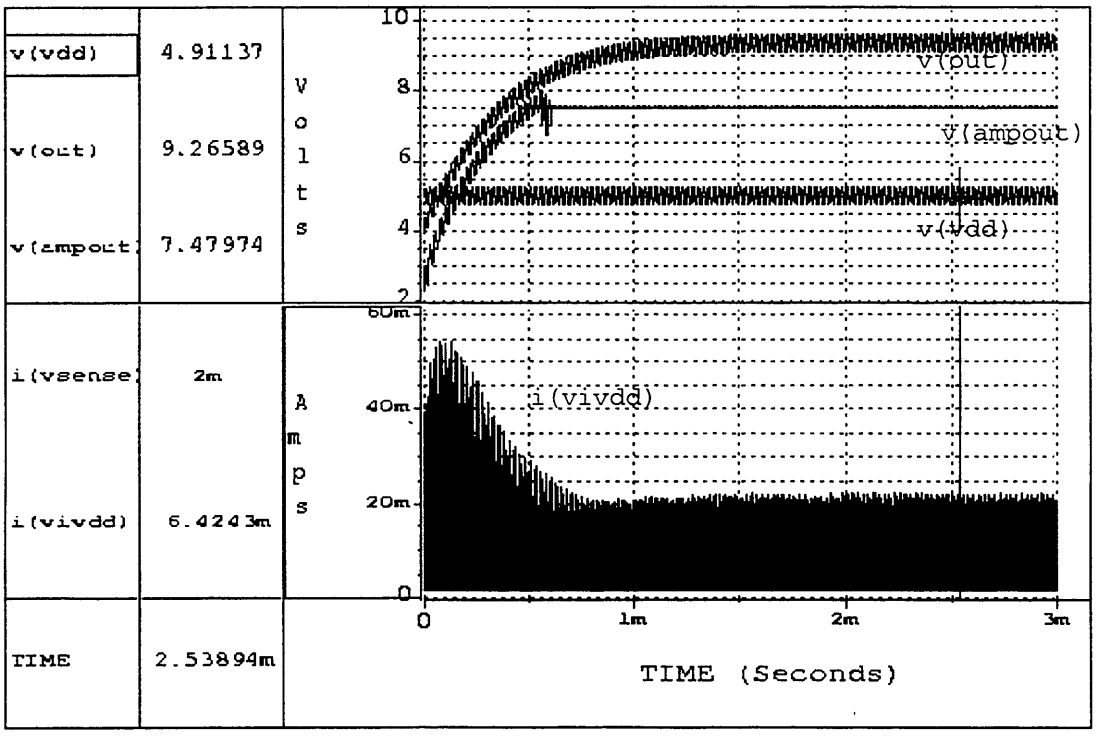


Figure 4.17: +7.5V Regulator Simulation: Power Supply Rejection

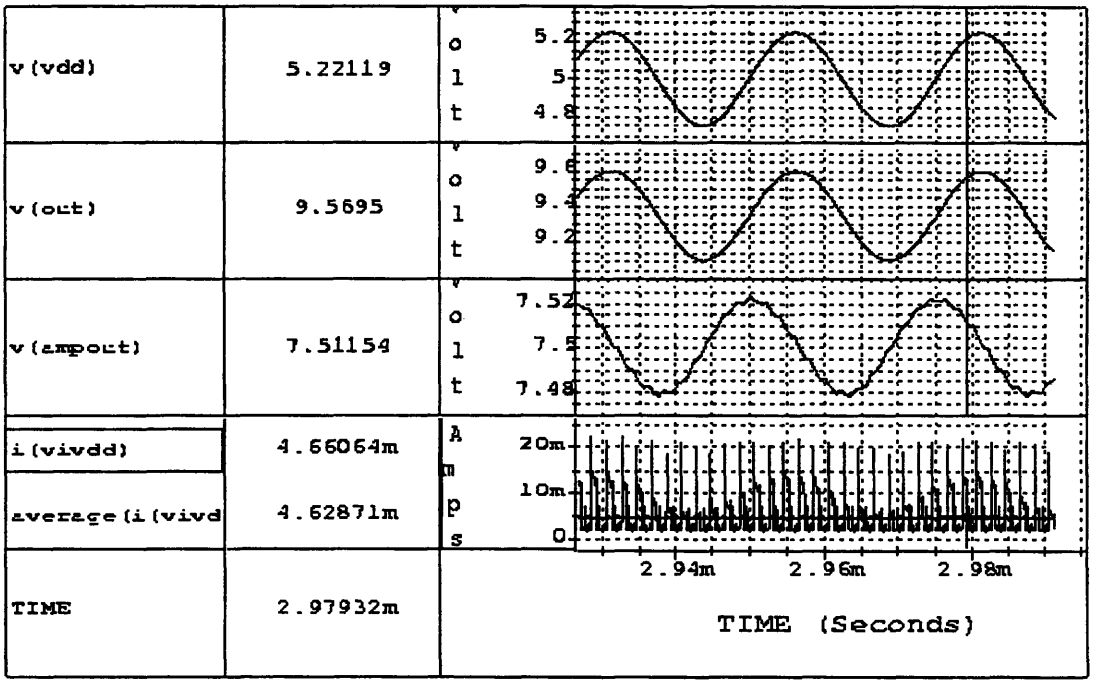


Figure 4.18: Steady-State Voltages and Currents for Fig. 4.17

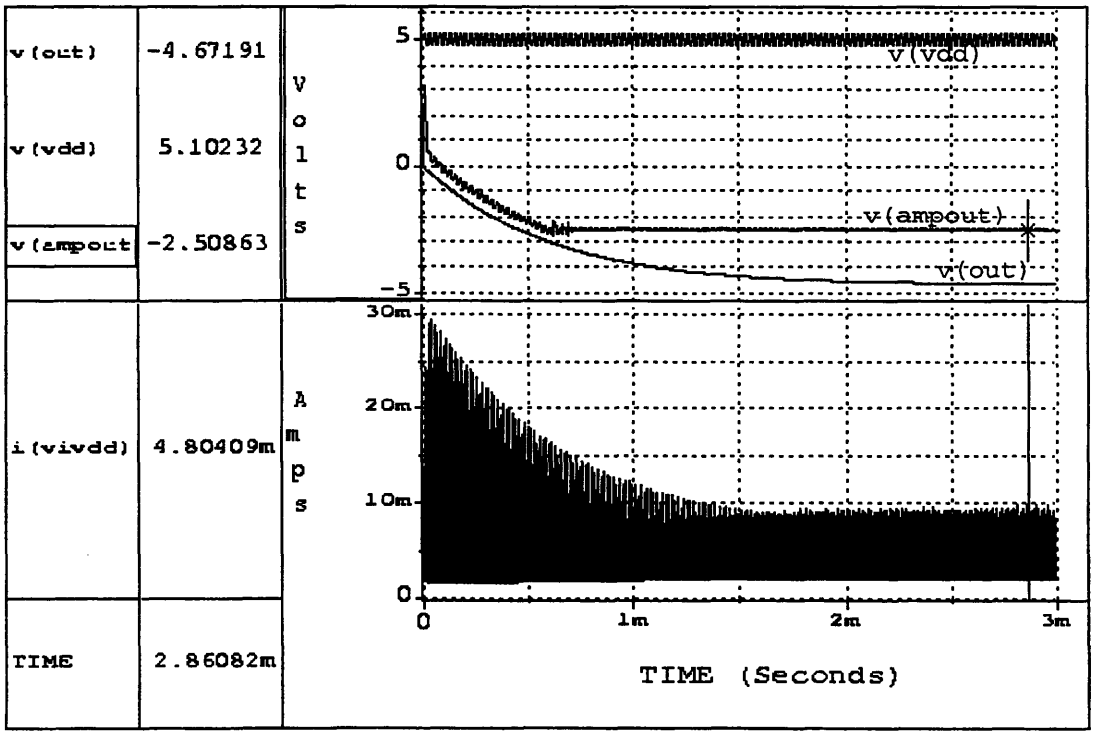


Figure 4.19: -2.5V Regulator Simulation: Power Supply Rejection

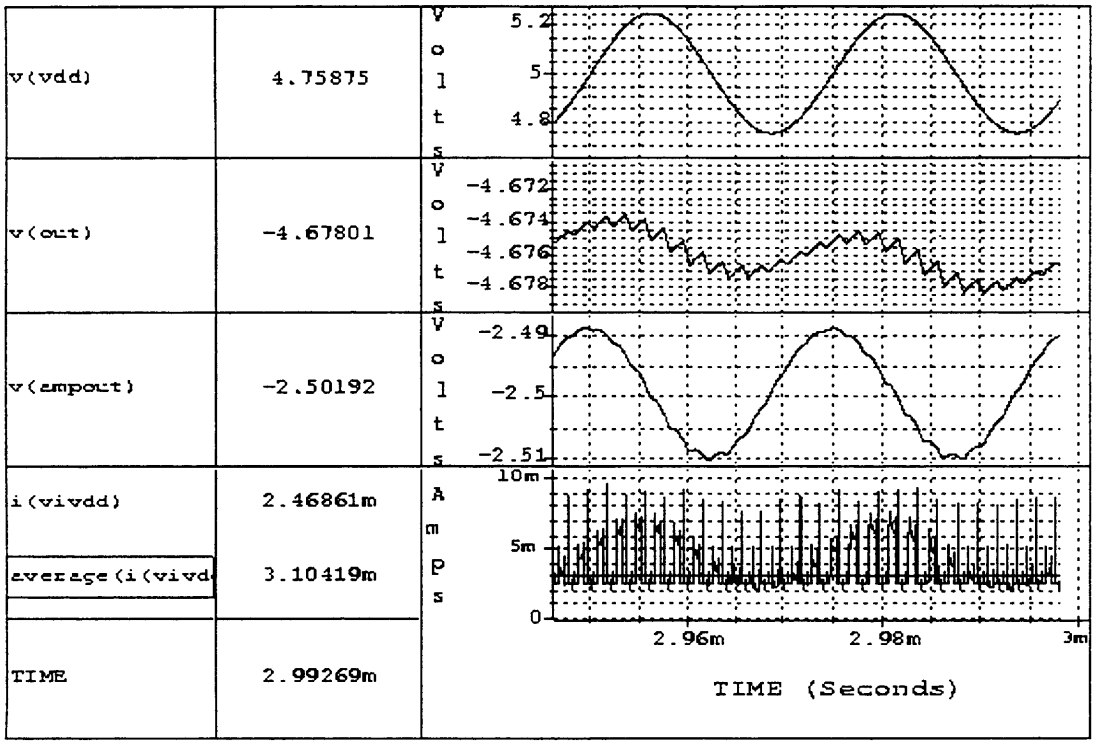


Figure 4.20: Steady-State Voltages and Currents for Fig. 4.19

4.4.3 Load Regulation Simulations

Load regulation simulations were performed where the regulator drove a sinusoidally varying load under the following conditions:

- Clock Frequency: 500kHz
- V_{DD}: +5V
- Load: 1.5mA<->2.5mA @ 40kHz

The plots of the +7.5V generator (Figs. 4.21, 4.22), indicate that the load regulation is 7mV/mA; the average steady-state voltage is approximately +7.50V. From the plots of the -2.5V generator (Figs. 4.23, 4.24), the load regulation is 4mV/mA and the average steady-state voltage is about -2.50V. These values meet the 10mv/mA specification.

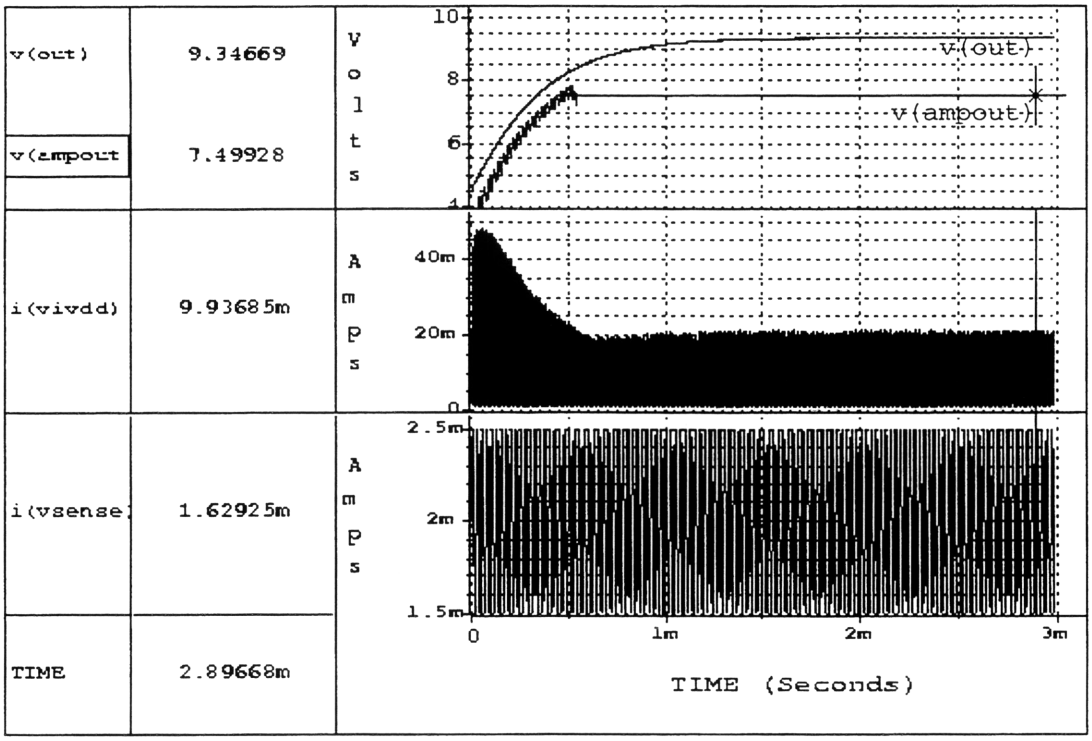


Figure 4.21: +7.5V Regulator Simulation: Load Regulation

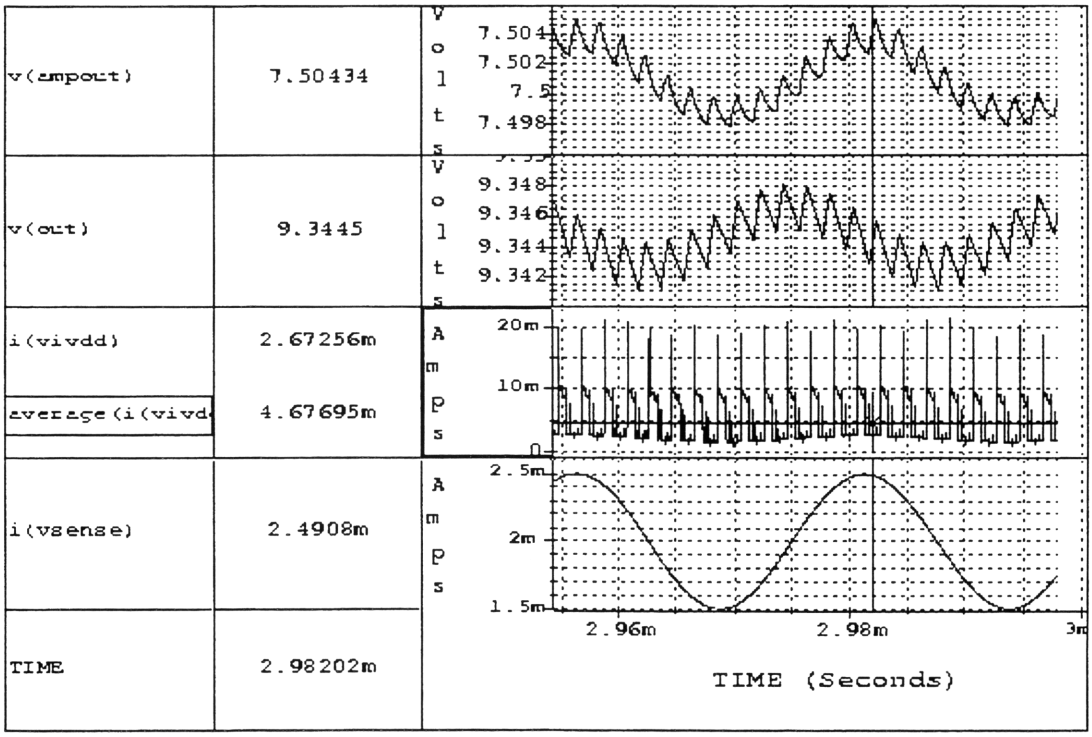


Figure 4.22: Steady-State Voltages and Currents for Fig. 4.21

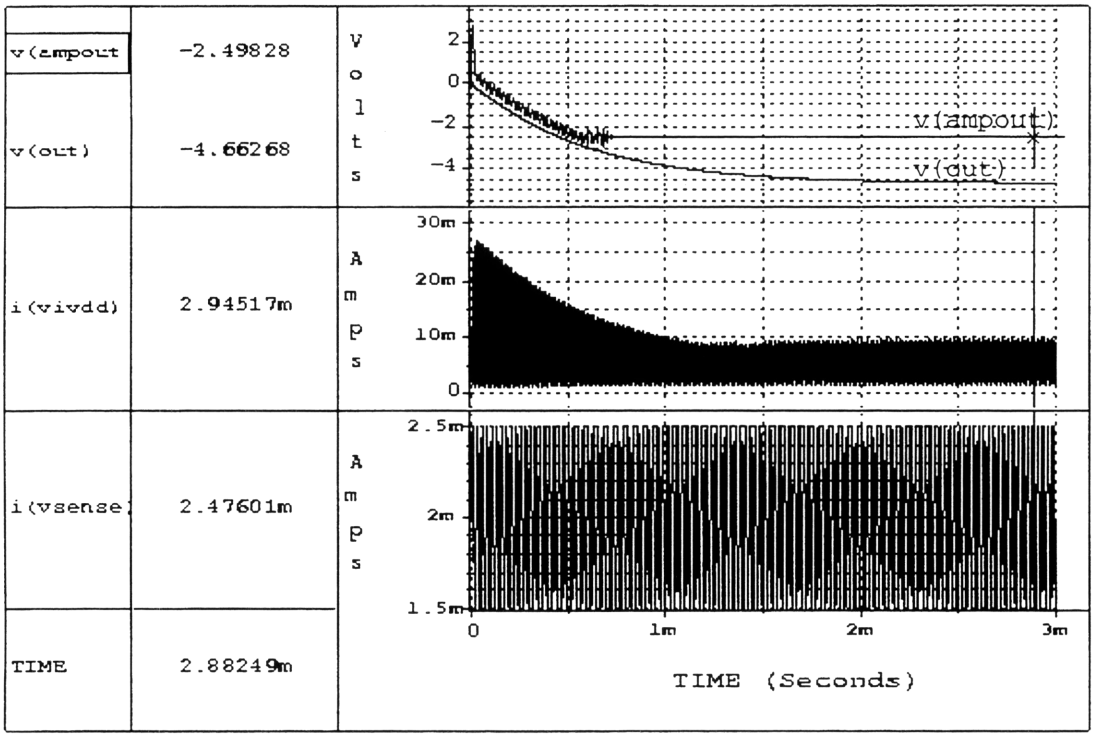


Figure 4.23: -2.5V Regulator Simulation: Load Regulation

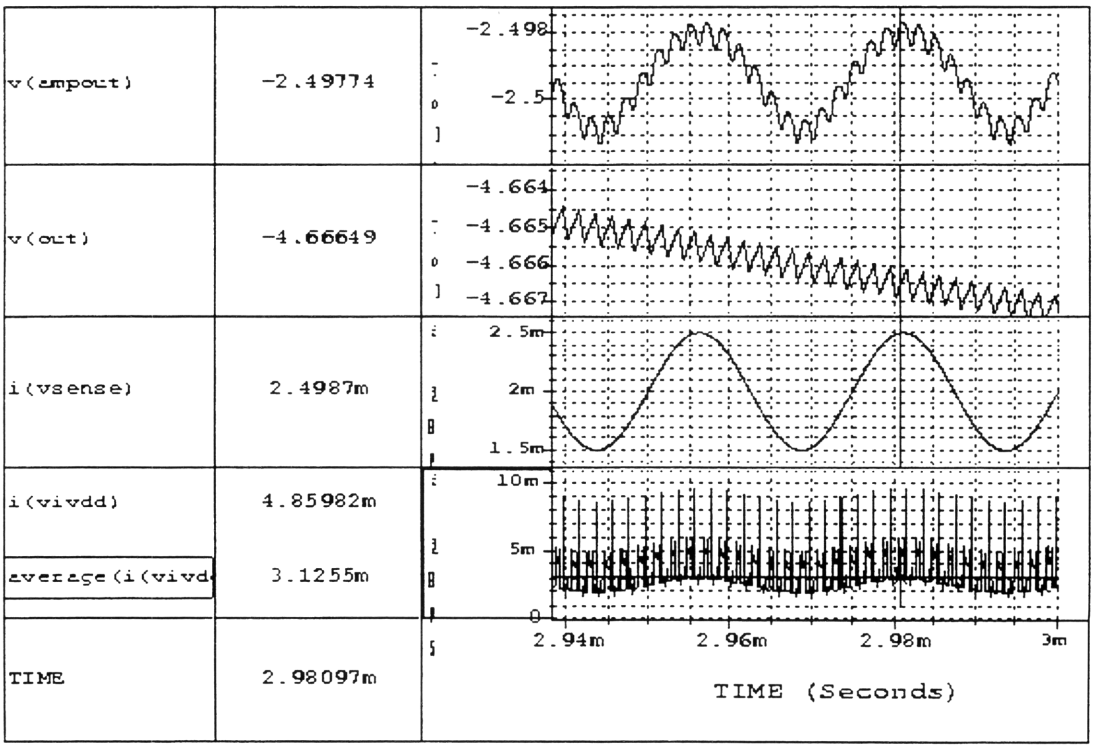


Figure 4.24: Steady-State Voltages and Currents for Fig. 4.23

4.4.4 Summary of Transient Response Results

The voltage regulators for +7.5V and -2.5V generation met all of the specifications with the exception of the efficiency specification for the -2.5V regulator. A modified efficiency calculation which combines the figures for the +7.5V and -2.5V converters resulted in an efficiency of 51% for both converters, which may provide a better sense of the actual efficiency regardless of polarity. The complete converter circuit can be further optimized by changing transistor sizes and op-amp bias currents to improve the efficiency.

Characteristics	Specifications	+7.5V Regulator	-2.5V Regulator
Output Voltage	+7.5V, -2.5V	+7.501V	-2.499V
Ripple Voltage	< $5mV_{pp}$	$2mV_{pp}$	$0.7mV_{pp}$
Power Supply Rejection	-14dB from DC to 40kHz	-21.9dB @ 40kHz (estimated: -33.0 dB)	-28.0dB @ 40kHz (estimated: -30.0dB)
Load Regulation	10mV/mA from DC to 40kHz	7mV/mA @ 40kHz (estimated: 6mV/mA)	4mV/mA @ 40kHz (estimated: 3mV/mA)
Efficiency	> 40%	64%	32%

Table 4.1: Comparison of Transient Measurements and Specifications

Chapter 5

Other Output Regulation Schemes

5.1 Pulse Width Modulation

A common way of controlling the output characteristics of a power converter is to use a Pulse-Width Modulation (PWM) control scheme. A PWM controller consists of a saw-tooth generator and a comparator comparing some form of the output voltage with the sawtooth waveform to determine the appropriate pulse width of the switching clock. The input to the comparator is often the output of an integrator which is useful for constructing a system whose steady-state error must be zero.

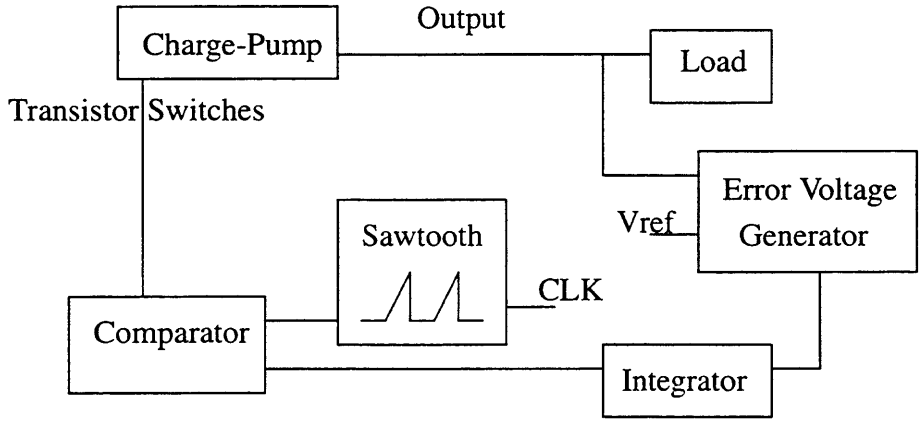


Figure 5.1: Block Diagram for PWM-Controlled Charge-Pump

For the DC/DC converter featured in this thesis, a PWM controller may be implemented. However, this converter will not be as robust as the op-amp regulator under different operating conditions (e.g. power supply and clock frequency variations). Early on, a PWM controller was studied and the main problems that were encountered in its effective implementation were the following: 1) dependence on the switching frequency; 2) awk-

ward algebraic tricks required to prevent op-amp saturation; and 3) poor power supply rejection.

Dependence on Switching Frequency

The sawtooth waveform is dependent on the switching frequency. It is generated by charging a capacitor where the time constant of charging is much longer than the switching period; the peak voltage, V_p, of the sawtooth waveform is $V_p = IT/C$. Therefore, a change in the switching frequency will cause a change in the peak voltage of the sawtooth waveform, which in turn changes the slope, and hence affects the pulse-width for a given comparator trip voltage that is fed from the integrator. A circuit to minimize the dependence on switching frequency was designed, but it was not robust over the 2Mhz$\pm$30% frequency range. A circuit that can generate a sawtooth waveform whose peak voltage is a constant with respect to frequency needs to be developed further if PWM is to be used in this particular application.

Algebraic Tricks to Prevent Op-Amp Saturation

The supplies that were given were 0V and +5V and the output voltages were -2.5V and +7.5V; a +2.5V reference was provided. Since the numbers that were given were multiples of 2.5, some minor algebraic manipulation were required to come up with the correct relations between 1) the output voltage, 2) the error voltage, and 3) the input to the comparator such that the control loop could force the system to converge upon the correct output voltage without saturating the op-amps that are involved.

The issue of saturating op-amps comes up since the system is referenced to +2.5V and the PWM control scheme would utilize a simple integrator, which inverts signals to a neg-

ative voltage. Given a 2.5V offset in the system, some amount of algebraic manipulation was necessary to generate an appropriate error voltage from the output of the integrator to be used as the comparator tripping voltage on the sawtooth waveform. Hence, it was very convenient that the system reference was +2.5V and the output voltages were multiples of it. If the desired output voltage was 8.25V, for example, there would have been difficulty generating the correct error voltages and keeping the amplifiers, which are biased with respect to 2.5V, from saturating to either supply voltage.

Poor Power Supply Rejection

The PWM controller had an integrator which integrated the error to zero at steady-state. The integrator required another off-chip capacitor since its response had to be about an order of magnitude slower than the 40kHz power supply variations. It was observed that the PWM converter could not handle a 40kHz variation in the power supplies; after 20mS, there were no signs that the transient was dying out; the converter followed the V_{DD} variations regardless of the size of the capacitor on the integrator. Making the capacitor large had the effect of dampening the rise of the voltage to its specified output value rather than filtering out the supply variations. When the capacitor was made too large, regulation did not occur at all.

In general, the PWM scheme may be more efficient than an op-amp regulator for lighter loads since the width of the pulses are not set and can become arbitrarily small. However, the PWM scheme investigated here for this set of specifications (frequency = 2MHz $\pm$ 30%; 40kHz V_{DD} variations) is not a robust design; a very specific operating point (sawtooth trip-point at steady-state, a frequency-independent sawtooth peak), needs to be established before it can be made to regulate. The PWM controller is not easily con-

figurable as a result. The difficulties that are outlined above render it an unattractive control scheme for the present application.

5.2 Pulse Frequency Modulation

Another way of regulating a DC/DC converter is by means of Pulse-Frequency Modulation (PFM) where the clock is turned on and off. PFM systems can be implemented with a comparator that compares the output voltage and then decides to either keep the clock on or to turn it off. This control scheme takes up the least power since the controlling block is a simple latch comparator [9] rather than two op-amps (Op-Amp controller) or a sawtooth generator, integrator and comparator (PWM).

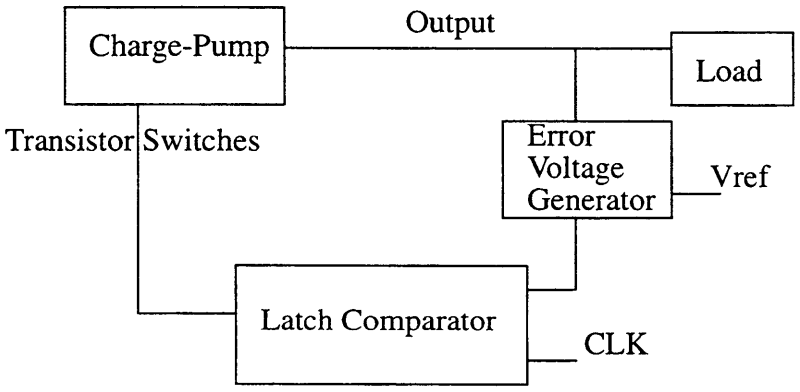


Figure 5.2: Block Diagram for PFM-Controlled Charge-Pump

For the purposes of the specific DC/DC converter featured in this thesis, a pulse-frequency modulator was not an appropriate means of regulation for the following reason: A PFM converter generates different frequencies from the frequency of the clock being turned on and off by the latch comparator. This on/off frequency is a function of the load; hence in a system where the load constantly changed, many different on/off frequencies

would be produced. For a system that is sensitive to the frequencies generated by its power supply, such as a demodulator, a PFM converter is not advisable.

The benefits of a PFM converter is that it can be operated over a variety of frequency ranges; the 2MHz$\pm$30% specification for the clock would not noticeably affect the performance of the converter. Moreover, since the PFM converter is turned off and on, its efficiency would be higher at light loads compared to other control schemes that were discussed. Its static dissipation would be lower than the other regulation schemes as well.

Chapter 6

Conclusion

The performance of a DC/DC converter consisting of a charge-pump circuit and an op-amp regulation scheme were analyzed. The specifications were comfortably met, with the exception of optimum efficiency. Relying on the regulation properties of an op-amp enabled the system to be decoupled; the charge-pump operated independently of the op-amp. As a result, the target voltage is essentially generated independently of the charge-pump's behavior. This simplifies designing the converter for an arbitrary voltage.

Other control schemes can be used, such as a linear feedback regulator, which controls the gate biases of the switching transistors accordingly. In PWM, the pulse width is modulated; in PFM, the pulse is either turned off or on. Perhaps the most noticeable difference between the op-amp regulation schemes and those mentioned above is the decoupling of the voltage generation function from its regulation mechanism. One of the possible reasons why PWM was difficult to implement effectively was since the control loop directly controlled the charge-pump, the poles of the system might have moved, leading to poor power supply rejection. Because the steady-state and transient properties are a function of the load, it may not be a robust design scheme to have a controller directly control the output since the operating points will change with changing loads.

For a simple concept, the op-amp regulator, for this particular application, seems to be the best control scheme given the set of specifications in Chapter 2.

References

[1] A. Stratakos, S. Sanders, and R. Brodersen, "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System," *Proc. IEEE Power Electronics Conf.*, pp. 619-626, 1994.

[2] C. Wang and J. Wu, "Efficiency Improvement in Charge Pump Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 6, pp. 852-860, June 1997.

[3] C. Calligaro, R. Gastaldi, P. Malcovati, and G. Torelli, "Positive and Negative CMOS Voltage Multiplier for 5V-Only Flash Memories," *Proc. IEEE 38th Midwest Symposium on Circuits and Systems*, Vol. 1, pp. 294-297, 1995.

[4] K. Sawada, Y. Sugawara, and S. Masui, "An On-Chip High-Voltage Generator Circuit for EEPROMS with a Power Supply Voltage below 2V," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 75-76, 1995.

[5] M. Shoji, *CMOS Digital Circuit Technology*, pp. 306-307, Prentice-Hall, Englewood Cliffs, NJ, 1988.

[6] N. Weste and K. Eshragian, *Principles of CMOS VLSI Design*, pp. 319-320, Addison-Wesley, New York, Second Edition, 1993.

[7] P. Favrat, P. Deval, and M. Declercq, "A New High Efficiency CMOS Voltage Doubler," *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 259-262, 1997.

[8] L. Casey, J. Ofori-Tenkorang, and M. Schlecht, "CMOS Drive and Control Circuitry for 1-10 MHz Power Conversion," *IEEE Transactions on Power Electronics,* Vol. 6, No. 4, pp. 749-758, Oct., 1991.

[9] J. Ho and H. Luong, "A 3V, 1.47mW, 120MHz Comparator for Use in a Pipeline ADC," *Proc. IEEE Asia Pacific Conf. on Circuits and Systems*, pp. 413-416, 1996.

[10] J. Kassakian, M. Schlecht, and G. Verghese, *Principles of Power Electronics,* Addison-Wesley, Reading, Massachusetts, 1991.