XXVI. CUSTOM INTEGRATED CIRCUITS

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1. CONVERSION OF ALGORITHMS TO CUSTOM INTEGRATED CIRCUITS[1]

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The conversion of algorithms to custom integrated circuits is seen as a set of transformations through a set of representatives, starting from a high-level functional description (e.g., microcode) through architecture, logic, gate, circuit, device, and layout specifications. The design problem consists of establishing an initial architecture (including the utilization of space/time tradeoffs to establish the desired degree of parallelism), then designing each module of the resultant architecture. We obtain the designs for these cells either from a library of previous designs, from a program that can generate a given type of cell (e.g., programmed logic array, register file, or finite-state machine), or by interactive use of a layout language. Our research has led to the development of layout programs that provide for the representation of types in terms of variables of the design that can be bound by the user. Thus, logical dependence of PLAs and ROMs can be specified, as well as connection points and device (e.g., length and width) parameters. In this way, design of any cell naturally leads to a parametrized representation that can be utilized for a single design or retained for additional instantiations in other projects. We have also developed both logic and layout optimization techniques for use with these programs.

Earlier work on switch-level unit-delay logic simulators for MOS circuits has

been extended and has led to the development of a new theory of MOS digital systems. Because MOS circuits provide for unique (capacitive) memory that is not explicitly represented in the design, and because of the use of bilateral devices and precharged busses, earlier theories appropriate to TTL logic are inappropriate, and this new fundamental theory is required. In addition, although we had earlier devised two design rule checkers, based on different representations, we are now designing special hardware to perform this task that should provide a speedup of at least two orders of magnitude.

At the level of circuit representation, we have started on work to extract an equivalent circuit from a layout in a form appropriate for timing and circuit simulation. We have also made a theoretical investigation of delays through interconnect networks that has been shown to provide accurate bounds on measured delays, and a new theory of the analog design of digital circuits is providing new equivalent circuits capable of bounding the circuit waveforms of MOS digital circuits.

Finally, a prominent part of our work is concerned with compilation techniques. Formalisms for the representation of functional specifications have been interpreted to provide complete designs of state machines, including data paths (registers and ALUs), control, and the instantiation of multiple processors where required for speed.

References

1. J. Allen and P. Penfield, Jr., "VLSI Design Automation Activities at M.I.T.," IEEE Trans. on Circuits and Systems (in press).