

Chapter 3. Novel Superconducting Tunneling Structures

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3.1 Project Description

Sponsor

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In this program we seek to examine the superconducting Josephson behavior in short-channel electronic structures where interference effects can take place. Additionally, our hybrid superconducting-semiconducting structure represents the first attempt at Josephson coupling via resonant tunneling. A significant consequence of this approach is that the energy scale for modulating the Josephson coupling is set by the quantum confinement levels and not the intrinsic semiconducting gap voltage.

Our device uses a thin vertical Si membrane ($< 1000\text{\AA}$) as a degenerate semi-conducting weak link between the superconducting source and drain electrodes which lie on either side. This structure is in many ways an electrical analogue of a Fabry-Perot interferometer. The membrane defines a vertical quantum well in which the charge carriers can interfere with each other (either constructively or destructively), thus creating a resonant tunneling structure between the source

and drain for both the Cooper pairs (i.e., the Josephson channel) and the normal quasiparticle (i.e., electron) channel. A separately applied gate voltage biases the levels within the semiconducting well, and ideally will modulate the Josephson current by varying the wavelength of the tunneling particles. Previous efforts on such hybrid Josephson devices have not utilized either resonant tunneling or quantum confinement, and their lack of gain arises from the significant mismatch between the semiconducting and superconducting gap energy scales.² A key motivation for our devices is that the energy scale is set by quantum confinement, and can be tuned separately from either of the gap energies. For Si well widths in the range of $500\text{-}1000\text{\AA}$, the energy levels separation in the well can be more comparable to the superconducting gap energy, i.e., many times smaller than the semiconducting gap.

Recent progress has now validated our basic device geometry in uniformly doped low-mobility Si:P. We are now progressing to fabricate the devices on doped high-mobility epitaxial layers grown on Si wafers at IBM. Higher mobilities will increase the characteristic lengths for the carriers in the semiconducting well, thereby better enabling internal interferences.

A schematic of the device geometry is shown in figure 1. More details of the fabrication process and progress will be published elsewhere.³ The primary aspects of the fabrication are described here. The originating wafer is $< 110 >$ Si, phosphorous-doped via ion implantation to yield

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² A.W. Kleinsasser, T.N. Jackson, G.D. Pettit, H. Schmid, J.M. Woodall, and D.P. Kern, *IEEE Trans. Mag.* MAG-25(2): 1274 (1989), and references within.

³ K. Early, G.E. Rittenhouse, J.M. Graybeal, and Henry I. Smith, "Sub-100 and sub 10-nm-thick Membranes Aniso-

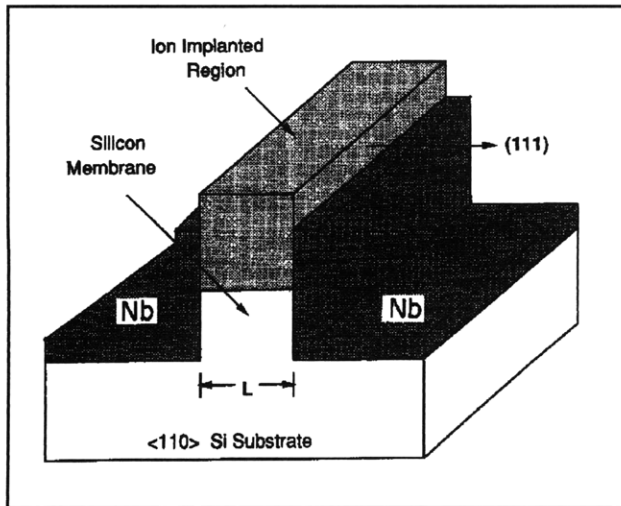


Figure 1. Schematic of the planar device structure. The vertical membrane consists of two etch pits separated by a length $L \leq 1000\text{\AA}$. The typical height for the vertical membrane is $\approx 3000\text{\AA}$.

$1 \times 10^{19} \text{ cm}^{-3}$ carriers at low temperature. A 300\AA Si_3N_4 layer is used as an etchant mask, with the membrane defined by aligning a mask stripe along either the $[\bar{1}1\bar{2}]$ or $[11\bar{2}]$ crystalline axis. The membrane fabrication is done via wet etching, using a potassium hydroxide/isopropyl alcohol solution which is well known for its highly anisotropic etching of Si. Because of the wafers' crystallographic orientation, the resultant terminating (111) planes are perpendicular to the wafer surface and form the walls of the vertical membrane structure. Such processing yields atomically-smooth surfaces which possess a significantly higher degree of parallelism and a significantly lower surface defect density than could be obtained by reactive-ion-etching (RIE) or other energetic processes. The niobium counterelectrodes are subsequently deposited, and source-

drain isolation is obtained by planarization followed by a chlorine RIE etch.

The electrical results of such devices fall into two categories. Those with wall thicknesses (denoted L in figure 1) greater than roughly 1000\AA displayed no Josephson currents, and showed current-voltage (I - V) characteristics consistent with superconducting-insulator-normal (SIN) metal behavior. The thin "insulating" layer is presumably a Schottky barrier at the Nb/Si interface, whereas the lack of a Josephson current reflects the fact that the device thickness L is significantly greater than the proximity-induced superconducting coherence length ξ_N in the Si ($\xi_N \approx 65\text{-}100\text{\AA}$ at 4.2K for these low-mobility devices). However, devices with membrane thicknesses comparable to 600\AA displayed finite Josephson currents, and fine I - V behavior consistent with SNS behavior. The I - V s are shown as a function of temperature for one device in figure 2. The product of the critical current and the high-bias device resistance $I_c R_n$ was as high as 0.4 meV at low temperatures, consistent with the best previous results on Nb/Si/Nb devices. Careful examination of the device characteristics plus imaging with a high-resolution STEM ruled out the existence of any Nb shorts over the top of the membrane. Additionally, modulation of the critical current versus applied magnetic flux was entirely consistent with the device geometry.

The next step for this work is to fabricate these devices using high-mobility Si. Note that conventional uniformly doped Si cannot provide the necessary characteristic lengths as its mobility is too low. Therefore, we are turning to chemical-vapor deposited epitaxial layers of Si/Si:B grown on (110) oriented wafers which can have mobilities approaching $10^4 \text{ cm}^2/\text{V}\cdot\text{sec}$. This work is presently underway.

tropically Etched in (110) Silicon," submitted for publication; G.E. Rittenhouse, Henry I. Smith, and J.M. Graybeal, "A Silicon Weak-Link Josephson Junction Using a Vertical Membrane Structure," forthcoming.

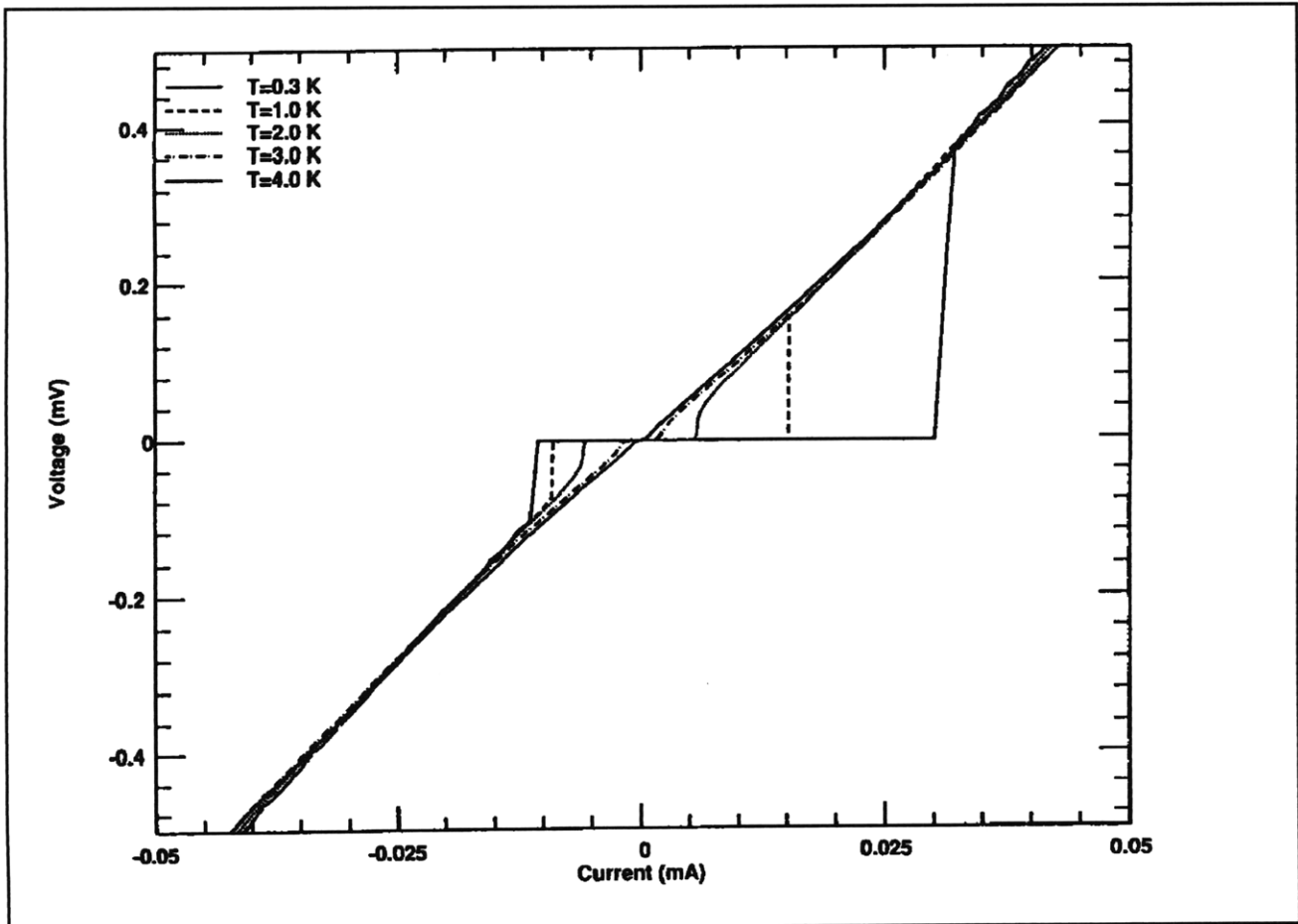


Figure 2. Current-voltage characteristics of one device versus temperature. Note presence of a finite Josephson current.



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