

ELECTRONIC AUTOMATION OF A REMOTELY DEPLOYABLE
SEAWATER SAMPLING DEVICE

by

Jonathan N. Betts

Submitted to the Department of Earth, Atmospheric and Planetary
Sciences, Massachusetts Institute of Technology, and to the
Department of Chemistry, Woods Hole Oceanographic Institute in
partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE
in Oceanography

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ABSTRACT

A microcomputer-based controller for an oceanographic instrument was designed, prototyped and converted to mass-producible form. The instrument is intended to be tethered at sea, submerged, for periods of up to one year. At a predetermined time during its deployment, it opens a trace-metal clean sample vessel, allowing the vessel to fill with seawater. The instrument then seals the vessel, and waits to be picked up by a ship. Multiple units, programmed to open in succession, can be tethered at one site.

The controller consists of a microprocessor, a real-time clock I.C., motor driving circuitry, motor movement feedback circuitry, micropower management and a wireless serial communications interface, all mounted on two custom printed circuit boards.

The device is designed to withstand the pressure at 100 meters depth, and includes provisions for increasing this, in the future, to 5000 meters.

Initial tests in a laboratory tank were successful. A long-term open-ocean deployment is planned for the near future.

Thesis Supervisor: Dr. Edward A. Boyle, Professor of Chemical
Oceanography

Acknowledgments

The design of the time-series sampling unit that is the focus of this thesis was all but finished before I entered the project. I have merely contributed technical assistance in one aspect of the device: the electronics. Any use of the word "we," if not signifying the community of oceanographers, certainly refers to the other people in the Chemical Oceanography Laboratory at MIT who have been involved in the project: Prof. Ed Boyle, who conceived of and initiated the project, Dr. Rob Sherrell, who contributed important early design guidance, and Jory Bell, who, besides contributing most of the design, has also done most of the work, including all of the mechanical fabrication and the software.

It is with pleasure that I describe the produce of my co-workers' efforts, but also with concern -- do not mistake my acts of description with their acts of creation.

In addition, I would like to acknowledge the contributions of those people who, although not directly involved in the project, have in one way or another made this thesis possible. Dr. Bill Jenkins at WHOI read the manuscript on rather graciously short notice. Tyana Caplan kept me spiritually and physically intact in spite of the deleterious forces of graduate school existence. Beth Sackett lifted my spirits untiringly. Prof. John Edmond gave me the travel opportunity that provided enough distance from my previous project to see that I wanted to do this one. Julian Sachs pointed out to me at a crucial

moment what I had said under my breath but not realized "I want to do the electronics for the sampler." Patty Marcus and Mary Ellen Higgins typed in many a requisition under the most unreasonably narrow time constraints. And last but not least, my plants, who grew inspiringly.

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Introduction

One can easily see the need for time-series data for oceanic properties such as temperature and flow rate because they are so plausibly linked to tangible factors as seasonal variations, storms and diurnal cycles. Not until recently, however, has significant interest in time-series chemistry data developed. Trace metal time series, in particular, have gone largely unstudied due both to the difficulty of collecting individual samples, and to a general lack of awareness that valuable information was present.

Recent studies of, for example, lead concentrations¹, iron-dependent, ocean-productivity patterns² and Cu, Ni, Cd, Al and Mn concentrations³, have turned up surprisingly rapid variations in the concentrations of oceanic trace metals. Our surprise highlights our current ignorance of the forces behind these short-term changes, motivating further study.

Much stands to be gained from a deeper understanding of time-variability of marine trace-metals. Lead dynamics trace key cycles of particles formation and destruction in the water column⁴ with importance not only to the understanding of the disposition of pollutants entering the ocean, but also to the understanding of the ocean as a whole, of its "biogeochemical cycles". Iron fluctuations may have important biological implications, and furthermore, understanding the nature of the fluctuations may also help reveal

patterns of other elements whose deposition to the ocean is largely aeolian.

Unfortunately, the cost of ship time and the large amount of effort required of qualified researchers prohibit the frequent visits to a single site needed to collect a time series. Some recent efforts have been directed toward the construction of devices capable of taking multiple samples at a given site while unaccompanied, but none so far have come to fruition. It is the goal of this project to provide such a device to the oceanographic community.

We know of only two previous attempts to construct such a device. One was by a group at Woods Hole which was working on a sampler for vertical profiling as part of the WOCE project, and which was thought to have been adaptable to time series measurements as well. The design was based on pumping seawater into tri-laminate bags using a peristaltic pump. The project was terminated by NSF because its schedule and specifications became incompatible with the WOCE project.

The other device exists in planning stages only. Dr. Ken Bruland and co-workers began the design of a system based on concentrating certain trace-elements of interest on a resin, eliminating the need to store and bring back any actual water samples. Time series would be gathered by pumping the seawater through several resin columns in sequence.

Even if these devices are completed, each has serious limitations that are overcome in the design of the time-series sampler presented here. The integrity of samples collected by the Woods Hole device depends on the perfect cleaning of the sample containers, and on not contaminating the sample containers during assembly of the device prior to deployment. This is because no provision is made for flushing the sample containers at the time of sample collection. Also, surfaces that are not trace-metal clean are in direct contact with the surrounding seawater.

The Bruland device, by virtue of its concentrating the samples, may be more tolerant of minor contamination of the sample columns. But its concentration scheme is very species specific. The samples from a given deployment would only apply to a few elements, limiting possible collaborations, and reducing the chances of following up on new results.

During the design process we constrained ourselves to the requirements that our sampler be:

- free of any exposed surfaces that are not trace-metal clean
- capable of flushing the sample container just prior to collection with several volumes of the same water it is about to sample

- resistance to contamination during set-up, deployment, and retrieval.
- unlikely to fail catastrophically
- inexpensive enough that the loss of a mooring -- not an uncommon occurrence -- would not ruin a P.I. financially

With these in mind, we settled on the design depicted in figure 1. Each sample is collected by a separate, autonomous unit, eliminating the chance of a catastrophic failure. The sample container, a commercially available, 250 ml plastic bottle is opened and closed by unscrewing and screwing its cap by rotary motion. The bottle is the only surface that the water sample contacts. The bottle is simple to insert and remove from the sampler. The sample remains sealed in the same container while waiting to be picked up at sea as while waiting in the lab for analysis.

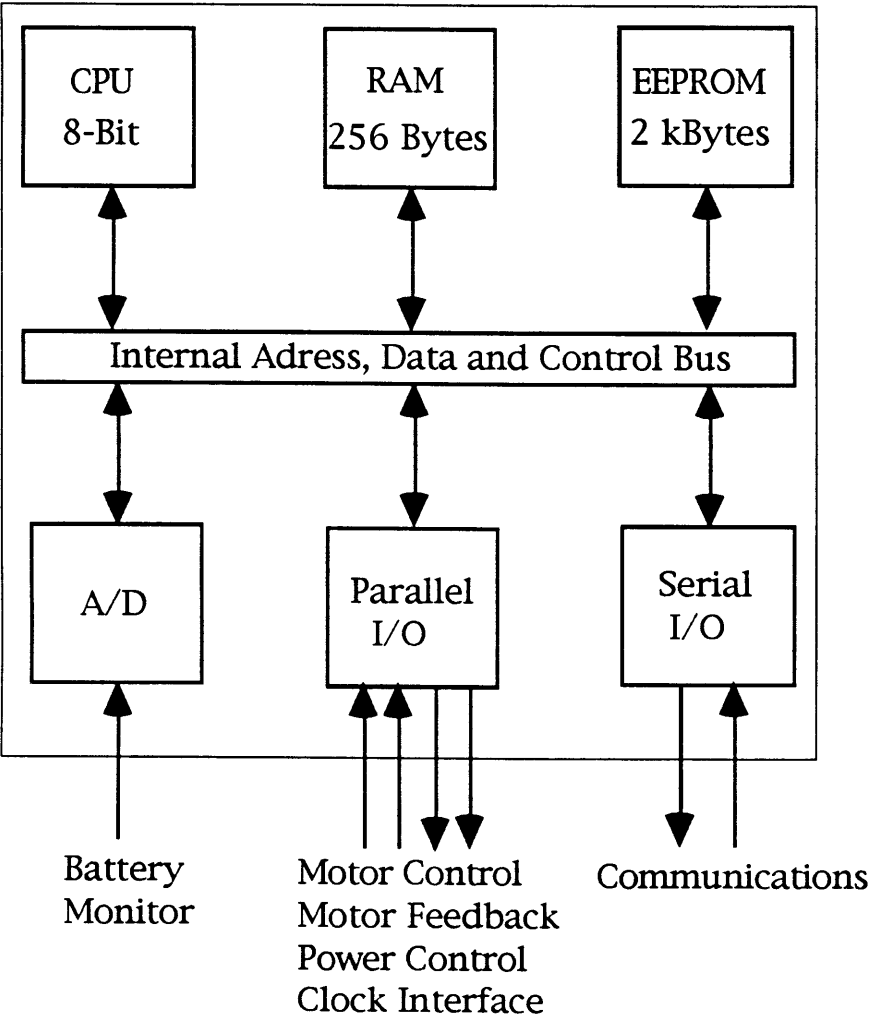
The sample enters the bottle by gravity. Upon deployment, the bottle is filled with distilled water. When the bottle is opened, the distilled water rises out buoyantly, drawing in seawater, which mixes with the distilled water inside. Subsequently, a mixture of distilled water and seawater rises out. Thus, more than just the original distilled water leaves the bottle; several volumes of seawater enters, mixes and then exits, thoroughly flushing the bottle.

The exterior surfaces of the sampler modules are made entirely of plastics known to be trace-element clean: high-density polyethylene, ultra-high molecular weight polyethylene and Teflon™. The whole module can be leached in an acid solution to scour metals from its liquid-contactable surfaces. To avoid a metal connector on the sampler exterior, information is passed into and out of the unit using an oscillating magnetic field.

The cost is kept low by the sampler's freedom from the complexity of a centralized design. Of course many sampler modules are required for a single deployment, but each one is inexpensive enough (< \$700), that an array of, for example, 21 units still costs far less than the P.I.'s salary during the deployment period. The cost is further minimized by eliminating the need for a pressure casing through the use of Fluorinert™ liquid⁵ to compensate for water pressure in the cavities occupied by the motor and the electronics.

Microcontroller

The internal architecture of the MC68HC811E2 single-chip microcontroller, and its connections to the rest of the system are shown in simplified form below:



The 8-bit central processing unit (CPU), executes instructions stored in the 2048-byte EEPROM. Operating variables and return addresses are stored in the 256-byte RAM. Communications, both for development (down-loading of programs) and for normal operation

(setting opening times and verifying sample collection) are mediated by the serial communications interface. Through the parallel interface, the processor controls the motor power and direction, turns off system power, and communicates with the real-time clock. The timer/counter unit does in hardware the high-speed task of motor-pulse counting which would otherwise place undue demand on the software. The voltage levels of the battery for the electronics (9 volt) and the batteries for the motor (two 6 volt banks) are monitored using the 8-bit analog-to-digital converter.

Timing and Reset

The schematics in figure (2) show the processor clock oscillator and reset generator, both implemented using parts of the same CD74HC16M hex Schmitt trigger. The clock oscillates at 8 MHz, which the processor divides down to 2 MHz and uses as its fundamental timing signal; thus all processor operations occur in multiples of 500 nS, with most instructions executing in 1.5 to 5 μ S.

When the power management circuitry first delivers 5 V power to the processor upon wake-up, the capacitor in the reset circuit is discharged, holding the input of the Schmitt trigger high, and thus its output low. This low signal places the processor into its “reset” state, setting each internal status bit to a known initial state. The processor remains inactive and the rest of the system has time to stabilize before C1 finally charges enough that it reaches the lower input-voltage threshold of the Schmitt trigger, forcing reset high.

Real-Time Clock

Made by Harris Semiconductor Corp., the ICM7170 real-time clock chip is in some ways the heart of the sampler electronics. During the long periods at sea, the only activity in the sampler is the faint but stable pulse of the 7170's 32,768 Hz crystal oscillator, and the CMOS logic counting these pulses.

The 7170 contains counters for 100th's of seconds, second, minutes, hours, days, months and years. For each counter there is a corresponding alarm register. When the counters all equal their associated alarm registers, the "interrupt" output pin is pulled to ground potential, triggering the power management circuitry to wake up the rest of the sampler's electronics system.

The microprocessor programs the alarm registers of the 7170 according to the time and date it receives via the magnetic link. When the processor shuts down, the address, data and control outputs it uses to communicate with the 7170 (see fig. C-1) all fall to ground potential. While it is necessary that all of the 7170's inputs be at either ground or Vdd for it to achieve its ultra-low-power mode, its "chip select" input in particular must be held at Vdd, its logical "false" state. For this reason, Q1 was added to invert the sense of the processor output before it reaches the "chip select" input.

This is important to the graceful sequencing of the power-up transition as well. Upon reset, the outputs used by the processor to

control the 7170 all drive low. The "RD" (read) and "WR" (write) inputs on the 7170 are therefore both driven "true". If the chip select signal were not inverted, a potentially damaging conflict would result. Before the processor enables the chip select, it places both "RD" and "WR" high.

Power Management Circuitry

Introduction

While the sampling unit is at sea, it spends most of its time waiting in its ultra-low-power standby mode, in which it draws less than a thousandth of its normal operating current. The power management circuitry switches between power modes, providing a solid 5 V supply to the entire system in normal mode, and a special 3 V supply to itself and to the real-time clock in standby mode. The bulk of the 12 μA standby current is drawn by the wake-up receiver, which operates continuously, directly from the 9 V battery. Another 3 μA or so are drawn by the real-time clock. The power management circuitry itself consumes only about 0.6 μA .

Circuit Description

The logical center of the power management circuitry (see fig. XXX) is the 74HC73 JK flip-flop, which functions as a 1-bit memory. It holds the state of the system: a "0" on its Q output signals full-power mode, while a "1" puts the system in standby.

The 74HC73's output controls the MAX667, a 5 V regulator chip with the ability to shut off its output and also to cease its own internal current consumption. While on, it steps down the 9 V battery input to 5 V, at up to 100 mA (although the system draws only about 11

ma of 5 V power). When the MAX667 is off, it draws only about 0.1 μA .

Once the 5 V output from the MAX667 falls, D1 is no longer forward biased, and so the 74HC73 and the real-time clock chip can no longer derive their power from that source. Instead, the voltage regulator comprised by Q1, Q2 and Q3 provides a trickle of current at about 3 V. This lower voltage reduces the amount of current drawn by the real-time clock chip.

The special 3 V regulator was designed especially for this purpose, since the lowest-current regulator currently available in chip form (which is, coincidentally, the MAX 667) draws an undesirable 4 μA while providing its regulated output. The custom 3 V regulator draws only about 0.25 μA .

This regulator functions as follows. The base-emitter drop of Q1 serves as a voltage reference. Ignoring Q3 for the moment, we see that current is fed to the regulator through 10 M Ω resistor R1. This current pulls up the voltage on the emitter of Q1, the collector of Q2 and on the divider formed by R2 and R3. It continues to rise until it reaches about 3.5 V, when the voltage across both R2 and the base-emitter junction of Q1 reaches 0.40 V. Q1 then turns on and conducts enough current that the voltage drop across R4 starts to turn on Q2. The current through the collector of Q2 competes for the original current through Q1 and the voltage divider, preventing the voltage

across the divider from rising, and completing the negative feedback loop.

The voltage at the collector of Q2 is thus regulated at 3.5 V. When the 9 V battery is at the end of its life, it provides only 6 V, leaving only 2.5 V across R1. Of the resultant 0.25 μA , 0.15 μA flows into the voltage divider and 0.04 μA through Q1 to keep 0.4 V across R4. This leaves a disposable current of only 0.06 μA , far less than the 2-3 μA needed to power the clock. The output current is increased by the addition of Q3 in emitter follower mode. With its gain of 50, provides up to 3 μA , while also dropping the voltage to about 3.0 V. This is a worst case. With a 7 V battery input the regulator can provide up to 8 μA .

Despite the changes in current through the regulator, voltage stability is maintained by the function of R4. Since most of the current through Q1 (40 nA) flows through R4, and only a small fraction through the base of Q2 (about 1 nA), changes in the current demand on Q2 do not significantly affect the current through Q1. The collector-emitter voltage of Q1 is of course constant. The only remaining variable to affect the base-emitter voltage of Q1 is temperature. The temperature coefficient of the base-emitter voltage is about -2.1 mV/°C⁶. The regulator is unlikely to encounter ocean waters higher in temperature than the 25 °C at which it is calibrated. The minimum temperature anticipated is 1 °C, which would increase the output voltage of the regulator to about 3.4 V -- still low enough to maintain reduced current consumption of the

real-time clock chip and to allow the "wake-up stun" system to function (described next).

Inputs to the 74HC73 circuit are either "wake" signals (from the wake-up receiver and the real-time clock chip) or "sleep" signals (from the microprocessor). To minimize the possibility of spurious inputs, especially spurious "sleep" inputs, which could ruin the sampler's prospects of taking a sample, the inputs to the 74HC73 are low-pass filtered with 100 pF capacitors to ground and 1 M Ω series resistors.

The sensitivity of the wake-up receiver causes it to respond to the voltage transients on the 9 V supply that result from shutting off the 5 V regulator, waking up the system immediately after every attempt to put it to sleep. The solution to this is to disable the wake-up input of the 74HC73 for a few seconds whenever the system is put to sleep. When "sleep" is brought high by the microprocessor, voltage divider R5-R6 presents 3.75 V to the anode of D2, charging C1 up to about 3.3 V. Due to the presence of D3, the "wake" input to the 74HC73 can no longer go below about 3.0 V, preventing a wake-up. Within a few seconds, however, R7 discharges C1 to less than about 1.8 V, allowing the 74HC73 input to reach its logical "low" threshold of about 1.5 V (1.7 V at 1 °C, as discussed above), and the system can once again respond to legitimate wake-up stimuli.

The data receiver (see fig. C-5) is powered from the 9 V battery without an intervening regulator since it requires a minimum of 6 V

to operate the TLE2037 amplifier. This receiver draws too much power to operate continuously, so its 9 V battery connection is switched on by the presence of the 5 V supply. Since the 5 V supply falls quickly at first, then lingers near the turn-on voltage of Q2, the 5 V is divided by two before reaching the base of Q2. While the switch is off, R3 prevents any leakage through Q2 from turning on Q3 and wasting battery power.

Wake-Up Call Receiver

Introduction

The default state of the sampler system is a nearly complete shut-down of the electronics. In this quiescent state, current is drawn only from the 9 V battery, and only about 12 μA . After derating the 500 mAH capacity of the 9 V 50% to account for the effects of pressure and low temperatures (advice of engineer at Duracell Corp.), the battery would last about 3 years. However, the bulk of the electronics must be on for some periods, and during these, about 25 mA are consumed. The battery will reach its designed lifetime of one year providing that the main electronics are on for less than 50 hours.

In order to maintain such a low standby power, even the data receiver, which draws about 7 mA, must remain off. This prevents one from using this receiver to give instructions to the sampler prior to a mission, and querying the sampler for a report after a mission.

Circuit Description

The wake-up call receiver uses so little power by sacrificing bandwidth - it operates at 16 Hz. At the heart of the receiver is an incredibly well-designed new op-am from Maxim⁷, the MAX406, which uses only 1.2 μA of current, despite its relatively high bandwidth of 20 kHz.

The first stage of the receiver is the diode detector which is biased at approximately mid-supplies. The input capacitor provides DC isolation from the L-C tank which oscillates about ground. The capacitor from the cathode to ground, C1 charges immediately through the diode when the input voltage rises, but must discharge passively through R1 when the voltage falls, since the diode is reverse biased at these times.

The time constant formed by R1 and C1 is very long (5 mS) compared to the time between peaks of the 100 kHz carrier (0.1 mS) so the voltage on C1 follows only the amplitude trend of the carrier - a 16 Hz modulation.

The design of this receiver is complicated by the need to run the detector diode at such low current (0.5 μ A) and at such a low voltage (6 μ V input) both of which reduce its efficiency and require higher amplifier gain. The detector must be run at such a low voltage because all of the amplification must be done at subsequent stages (at 16 Hz) rather than before the diode (at the 100 kHz carrier frequency) due to the effects of limited supply current on amplifier bandwidth.

The need for high gain brings out a weakness of all CMOS op-amps: high input noise. The resonant input tank (see figure C-5) provides enough selectivity (Q =ca. 40) that the noise is low at the input of the receiver, but after the noisy, high-gain amplifier stage (1000x), the

broad-band noise is greater than the 16 Hz signal at the maximum receiver range. To remedy this, a 16 Hz band-pass filter follows the amplifier stage. The filter has a Q of 10 (the maximum possible without using exotic, high precision capacitors) and also boosts the gain an additional factor of 10. The broad-band noise after the amplifier is about the same amplitude as at the input, but signal is now 10 times greater, or about 3 or 4 times the noise.

The final stage is a sampling window comparator, the Linear Technology⁸ LTC1042, which is a reasonably high-power comparator nested within a circuit that turns it on only 0.4 % of the time. The chip draws 2.5 mA for 80 μ S every 0.2 s, averaging to 1.0 μ A overall current consumption. The comparator itself has the handy and unusual ability to trigger its output when the input exceeds the reference voltage in *either* direction, positive or negative. The half-width of this window is set by the voltage divider on pin 5 to be 20 mV. The output of the comparator is connected to the "Wake" input of the power management circuitry (see figure C-3, and section IV.3), waking up the rest of the circuit.

Since both positive and negative swings can exceed the window, the 16 Hz modulation creates, each second, 32 opportunities for triggering the comparator. The comparator sampling at 5 Hz beats rapidly enough with 32 Hz that it requires a maximum of 2 samples to encounter the signal at ≥ 0.717 of its peak amplitude.

The maximum response time, then, is 0.4 s plus the time needed for the band-pass filter to pump up to near its full-amplitude output. Since the filter has a Q of 10, it reaches $1-1/e$ of its maximum within 10 cycles⁹, or 0.625 s, bringing the total response time to 1.025 s. The control-unit software waits a conservative 3 s for a reply from the samplers.

Data Receiver

Introduction

Whenever the full electronics system is powered up in response to a signal from the wake-up call receiver, the sampler begins listening using the data receiver. If no broadcast is heard from the control unit within 3 seconds, the processor, to conserve power, issues the "sleep" signal to the power management circuitry.

If the wake-up call appears to be valid, the data receiver is further used by each sampler to listen for its unique address, indicating its turn to either receive instructions (before being put in ocean) or tell how successfully it sampled (after being removed). If does not hear its address within 3 minutes, it sleeps. The addressing scheme is needed to avoid communications conflicts, since all the samplers transmit and receive using the same carrier frequency.

The communications format is standard asynchronous serial characters at 1200 Baud, interpreted by the UART built into the 68HC811 processor. The system is limited to half-duplex (one way at a time) operation due to the lack of selectivity of the receivers.

Circuit Description

Broadcasts are picked up by the receiver using a small, commercially wound coil. Unlike typical radio broadcasting and receiving, the

technique employed here is essentially a weakly coupled transformer. When the oscillating magnetic field of the transmitting coil overlaps spatially with the receiving coil, it induces a voltage, however small, in the receiving coil.

The dominant source of selectivity for the receiver is the Q (about 40) of the L-C tank formed by the receiving coil and a 10 nF capacitor in parallel with it. The receiver is tuned by adjusting a threaded ferrite cap atop the coil. The operating frequency is about 100 kHz.

The first stage amplifier is biased at mid-supplies, and isolated from the DC ground potential of the receiving coil by a 10 nF capacitor. This first stage amplifies the input by a factor of 100. Because the input signal ($20 \mu\text{V}$ at the maximum range of 1.5 m) is smaller than the input noise amplitude of most low-power op-amps, a bipolar, ultra-low-noise device is used here: the TLE2037, which is identical to the industry standard OP-37 (except cheaper).

The second stage provides another factor of 100 of gain, and also operated the detector. A CA3130 was chosen due to its high bandwidth, low power consumption of 0.5 mA^{10} , and its ability to drive its output near ground. Its non-inverting input is biased at 0.6 V by the drop across D1. Its output splits into two channels. Each charges a capacitor through a diode. With no input signal, the voltage across each capacitor is approximately zero, since each output diode drops about same voltage as the input bias diode lifts. In the

presence of a signal, the positive swings on the output of the op-amp charge the capacitors to the voltage at the peak of the wave form, while on the negative swings the diodes are reverse biased so the capacitors must discharge passively through their paralleled resistors.

The key difference between the two output channels lies in the time constant of the passive discharge phase. C1 discharges with a time-constant of 200 ms which, at 1200 Baud, is 240 bit times, or 24 characters. This channel follows the long-term amplitude trend of the signal and is used to set the threshold of the comparator (next stage). The time-constant of C2 (47 μ S) is much longer than the period of the carrier (10 μ S), which is therefore smoothed out, but much shorter than one bit time of the data stream (833 μ S).

The signal present on C2 is a copy of the transmitted serial wave form except that its amplitude can vary over orders of magnitude depending on the proximity of the transmitter. It must be converted to a digital signal of constant amplitude compatible with the UART on the 68HC811. The voltage on C1 traces the amplitude of the signal on C2. The center of the voltage divider R1-R2 is thus midway between the positive and negative peaks of the signal on C2.

The final stage is made up of one half of a CA5260 functioning as a comparator. Its CMOS output stage allows it to drive digital logic directly. The comparator outputs a logic "low" when the signal on C2 is greater than the voltage from C1's voltage divider, and *vice versa*.

Thus a logic "low" indicates the presence of carrier, a logic "high", its absence. Since the idle state of a standard serial logic line is "high", the default is no RF, and thus no wasted power.

The transmitter-receiver system cannot function in a manner that is completely transparent to the communications protocol. That is, the system could not be inserted in place of a wire in an arbitrary place in a 1200 Baud serial communications system. This is because the receiver has to be sufficiently general to accommodate a wide range of input amplitudes, and it "forgets" the amplitude setting of any transmitter after about 24 characters worth of quiet. During quiet times, the receiver essentially calibrates itself for signals at the amplitude of the background noise -- and so it picks up that noise. When real data begins to be received, the UART is generally in the middle of processing a garbage character from the noise stream and not able to synchronize on the incoming character. Therefore, each time communications are resumed after a quiet period, a dummy character followed by a character-long pause must be sent ahead of the real data to re-calibrate the receiver and reset the UART.

Despite the wide dynamic range of the detector circuit, a gain control feedback is needed because the dynamic range of the incoming signal is even greater. The other half of the CA5260 monitors the voltage on C1 as an indicator of whether the signal is in danger of exceeding the voltage range of the amplifiers. When the voltage exceeds mid-supplies, the output of the CA5260 begins to rise, turning on the BSS138 field effect transistor (FET). The FET is connected directly

across the input L-C tank, so when the FET conducts, it reduces the input voltage to the receiver. The impedance of the L-C tank rises to about 10 k Ω at resonance, so the 10 Ω on-resistance of the BSS138 FET is capable of reducing the input signal amplitude by a factor of 1000. This is important in the range 0-10 cm only, but it simplifies constraints on transmitter placement.

Motor Interface and Transmitter

Introduction

The motor interface consists of (1) the motor driver circuitry, which controls the intensity and polarity of power going to the motor, (2) the transmitter for the wireless link, which uses the same driver components, but in a different way than the motor does, and (3) the pulse detector, which informs the processor how quickly, if at all, the motor is turning.

Motor Driver and Transmitter

The antenna coil and motor are connected in parallel, except that the antenna circuit also includes a $1.0 \mu\text{F}$ series capacitor. Under the DC drive conditions used to power the motor, no current flows through the capacitor, so no power is wasted in the antenna. While transmitting, the driver is switching polarity at 100 kHz, and so the capacitor impedance drops to about 1.5Ω while the impedance of the motor, with its inductance of $125 \mu\text{H}$, rises from 2.4Ω to 80Ω . The inductance of the transmitting coil is about $33 \mu\text{H}$, or about 20Ω at 100 kHz, so roughly 80% of the power goes to transmitting. The 20% dissipated in the motor does no harm because the power (about 0.5 W) is negligible, and the polarity oscillates so rapidly that no net movement can occur.

Current to the motor and antenna coil is switched using four power transistors in an H-bridge configuration (see figure C-6). An H-bridge allows the voltage on the motor antenna to be completely reversed even though the driver circuitry uses a power supply providing only one polarity. When the motor is powered in the bottle-closing direction, the upper-left-hand transistor and the lower-right-hand transistor are on (conducting) and the other two are off. The opposite is true when the bottle is opening.

Ground is supplied to the H-bridge through a 0.05 ohm resistor, which drops only about 100 mV under full load (motor stalled), so motor operation is unaffected, but 100 mV is sufficient signal for the pulse detector circuit (see section IV.7, and figure C-7).

Positive voltage is supplied to the H-bridge from the voltage doubler circuit. Depending on the state of the "double" signal from the processor, the voltage doubler circuit provides either 6 V or 12 V to the H-bridge. A logical high on the "double" line turns on Q1, which turns on Q2, which puts 6 V on the gate of the N-channel MOSFET Q3. This forces Q3 into conduction, connecting the negative terminal of battery bank #2 to the positive terminal of battery bank #1, and thus elevating the positive terminal of battery bank #2 to 12 V. This also increases the gate voltage on Q3 to 12 V, improving its conductivity. In reality, the voltage doubler increases the voltage by a bit more than a factor of two since without the doubling, the current is forced to flow through the Schottkey diodes, D1 and D2, which drop about 0.4 V at 2 A. With the doubler active, the only

drop is across the MOSFET, which drops only $2 \text{ A} \times 0.1 \text{ } \Omega = 0.2 \text{ V}$.
The final ratio is then $11.8/5.6$ or about 2.1.

Gate Drive Considerations

The power transistors comprising the H-bridge are HEXFETs (a kind of MOSFET or Metal Oxide Semiconductor Field Effect Transistor). FETs are controlled by the voltage on their gates. Since they require virtually no gate current at steady state, very little power is required of the gate drivers, provided they can overcome the gate capacitance quickly enough. If they were to switch the FET too slowly, excessive power would be dissipated in the FET, potentially destroying it, since at intermediate resistances it shares the load with the motor or antenna coil.

The gate capacitances of the N- and P-channel devices comprising the Si9942DY are about 160 pF and 340 pF, respectively¹¹. The HCMOS outputs of the 74HC27, which are capable of about 4 mA drive the gates of the N-channel devices. At this current, it takes about 20 nS to charge the gate to the 5 V it requires in order to be fully "on." Assuming the worst case -- that the FET conducts with the same resistance as the motor ($2.4 \text{ } \Omega$) at all intermediate gate voltages, and that the "Double" signal is high, supplying 12 V to the motor H-bridge -- about 2.5 A will flow during switching, causing 15 W to be dissipated in the FET itself. Since the maximum power dissipation of the Si9942DY package is 2 W and the N-channel device resides in only one half of this package, the FET must switch only 1/15 of the

time, i.e., once every 300 nS or at a maximum rate of 3.3 MHz. This is far greater than the fastest switching required by the system, which is the 100 kHz transmitter carrier frequency.

The gates of the P-channel devices are pulled to ground by the 2N3904 transistors, which supply a more-than-ample 60 mA. The gates are pulled positive by the 1 k Ω collector-pull-up resistors on the 2N3904's. The time required for the 1 k Ω resistor to charge the 340 pF gate capacitance to 5 V, given a 12 V source, is about 9 nS.

Given a 6 V source, however, it takes two R-C time constants, i.e., 640 ns, to bring the gate voltage to $1 - e^{-2} \times 6$ V or 5.2 V. Fortunately, at 6 V, the power dissipated during switching is only 3.75 W at worst case, so the maximum switching frequency is $1 / (3.75 \times 640 \text{ nS})$ or 420 kHz -- still well above the 100 kHz carrier frequency.

These thermal designs are made more conservative by the fact that the electronics operate in Fluorinert™ liquid, which has a greater capacity than air to remove heat from electrical components⁵.

Selecting between Motor and Antenna

The logic responsible for mediating between motor and antenna driving resides in the 74HC27 triple, three-input NOR gate chip. To operate the motor, either the "close" or "open" output is brought low by the microprocessor, depending on the motor direction desired. Since at least one input to G1 is high, its output is low, which leaves

the other inputs to G2 and G3 enabled. The serial-data output of the 68HC811 idles high, preventing via D1 the transmitter oscillator from oscillating, and forcing its output low. All other inputs being low, G2 and G3 act simply as inverters of the "close" and "open" signals respectively, driving the active-high inputs to the H-bridge. That is, with the exception that, when the "close" output on G2 is active, G3 is disabled. This prevents both directions from being enable simultaneously by accident, burning out the H-bridge, and also serves the antenna driving function (described next).

To operate the transmitter, both "close" and "open" are brought low simultaneously. G1 prevents the motor from closing; since all of G1's inputs are low, its high output forces G2 and G3 to be in their true states, with their outputs low and the H-bridge off. When the serial-data line goes low, two things happen: G1 no longer disables the H-bridge and the transmitter oscillator begins toggling its output. When the oscillator output is low, both "close" and "open" are enabled, so "close" wins, and current flows through the antenna from left to right. When the oscillator output is high, "close" is disabled, so the "open" signal from the microprocessor takes effect, forcing current through the antenna from right to left.

As long as the serial-data line is low, the H-bridge will toggle at 100 kHz, broadcasting energy to the control unit.

Motion Feedback

Introduction

To know when the sample bottle is open, closed, stuck closed, etc., the program refers to output from a circuit that detects current pulsed from the motor. This method is not as exact as one using some form of absolute position feedback, such as a magnetic or optical encoder on the motor shaft. The benefit of the pulse detector is that it requires only one, low-cost, 8-pin integrated circuit and a few associated passive components, while a shaft encoder would require additional, and rather challenging mechanical engineering and would increase the size and complexity of the sampler mechanism.

Circuit Description

The pulse-detection circuitry (figure C-7) senses the pulse in current created by the motor during the change-over from one armature coil to the next. This current passes through the $0.05\ \Omega$ resistor that connects ground to the H-bridge, creating a small voltage drop.

These roughly $600\ \mu\text{V}$ peak-to-peak pulses are low-pass filtered through R1 and Ci to remove noise from the brushes. Next, C2 and R2 form a high-pass filter that serves three functions. It allows the DC level to float up from just above ground, where the $0.05\ \Omega$ resistor is, to approximately 4.5 V where the amplifiers are biased.

The filter also functions to remove asymmetries between the individual brushes in the motor. If the filter frequency is set below 1.6 kHz, the larger pulses force the smaller ones below zero-crossing, preventing them from being detected. Finally, the filter prevents the low-frequency swings due to variations in load from saturating the amplifier.

The first amplifier provides a gain of 1000, bringing the 600 μV input up to 0.6 V peak-to-peak. The 100 pF capacitor in the feedback provides another low-pass filter. The capacitor coupling to the next op-amp provides additional high-pass filtering, and removes any differences between the bias voltages of the first and second op-amps.

The second op-amp functions as a comparator. The resistor network, R3-R4-R5 provides about 4.5 V to the inverting input of the op-amp from the bottom of R4, and, from the top of R4, the same voltage plus about 25 mV to the 1 M Ω resistor biasing the non-inverting input.

With no motor movement, and thus no signal at the output of the first op-amp (except noise, which is much less than 25 mV) the output of the second op-amp; remains positive since its non-inverting input is at a higher voltage than its inverting input. Since the CA5260 has CMOS outputs, its positive output drives all the way to the positive supply rail, providing a logical high output to the microprocessor.

When the motor moves, the non-inverting input receives 300 mV negative-going pulses, which exceed the 25 mV offset, and drive the output low. The processor counts these negative going pulses via its timer/counter subunit in order to keep track of how far the shaft has rotated. Each pulse represents about 1/700 of a revolution of the motor-gearbox output shaft.

Due to various factors, the output is not perfectly proportional to motor movement at all times. For example, the high-pass filtering causes the ratio of pulses to movement to double when loading decreases the shaft speed to less than half of its free-running rate. This is because each edge, both rising and falling, of the slowed input signal then produces an individual pulse. Also, when the motor is moving at near stall, parasitic vibrations and catching and slipping produce a large number of false pulses.

Fortunately, an accurate integration of the pulses to form an exact motor position is not needed. At either end of the screw's travel (see appendix D), a stop is reached - either the bottle is fully closed or bottom of the screw abuts the 2nd triangle - and the motor stalls completely. When the pulses cease for long enough, the processor assumes that the end stop has been reached. The circuit is accurate enough (within a factor of two) to get a rough idea of where the screw is, however, so if pulses cease prematurely, the processor can attempt to unstick the screw by pulsing the motor power, or, as a last resort, doubling the motor voltage (see section IV.6).

Appendix A: Development and Testing

Schematics for the electronics were composed, and the printed circuit board patterns were laid out using CAD/CAM programs on the Macintosh.

The original hand-wired prototypes of the electronics were done using 0.1" grid, single-side plated perf board, with connections made by soldered lengths of 30 AWG wire-wrap wire.

The printed circuit boards were fabricated by PSI Manufacturing Co. of St. Helens, Oregon. The designs were transmitted to PSI via modem, in Gerber-format files. The design rules used were 0.012" lines and spaces, 0.035" holes. For compactness, surface-mount integrated circuits were used wherever commercial availability conveniently permitted.

The components were hand-soldered to the printed circuit board using a 0.016" tip set at 550 °F and 28 AWG solder with 62% Sn, 2% Ag. Before soldering, the components were secured in place using cyanoacrylate gel. Soldering was done under a 6X stereo microscope.

The software was written in Micro-C, available from Dunfield Development Systems, P.O. Box 31044, Nepean, Ontario, Canada K2B 8S8.

No tests have yet been conducted in natural waters. The hand-wired prototype was larger than would fit into the sampler module. For testing, a connector was added to the sampler module so that the motor could be operated by the electronics remotely. The system successfully operated in a tank of water in the laboratory, with the electronics connected from outside the water by two wires.

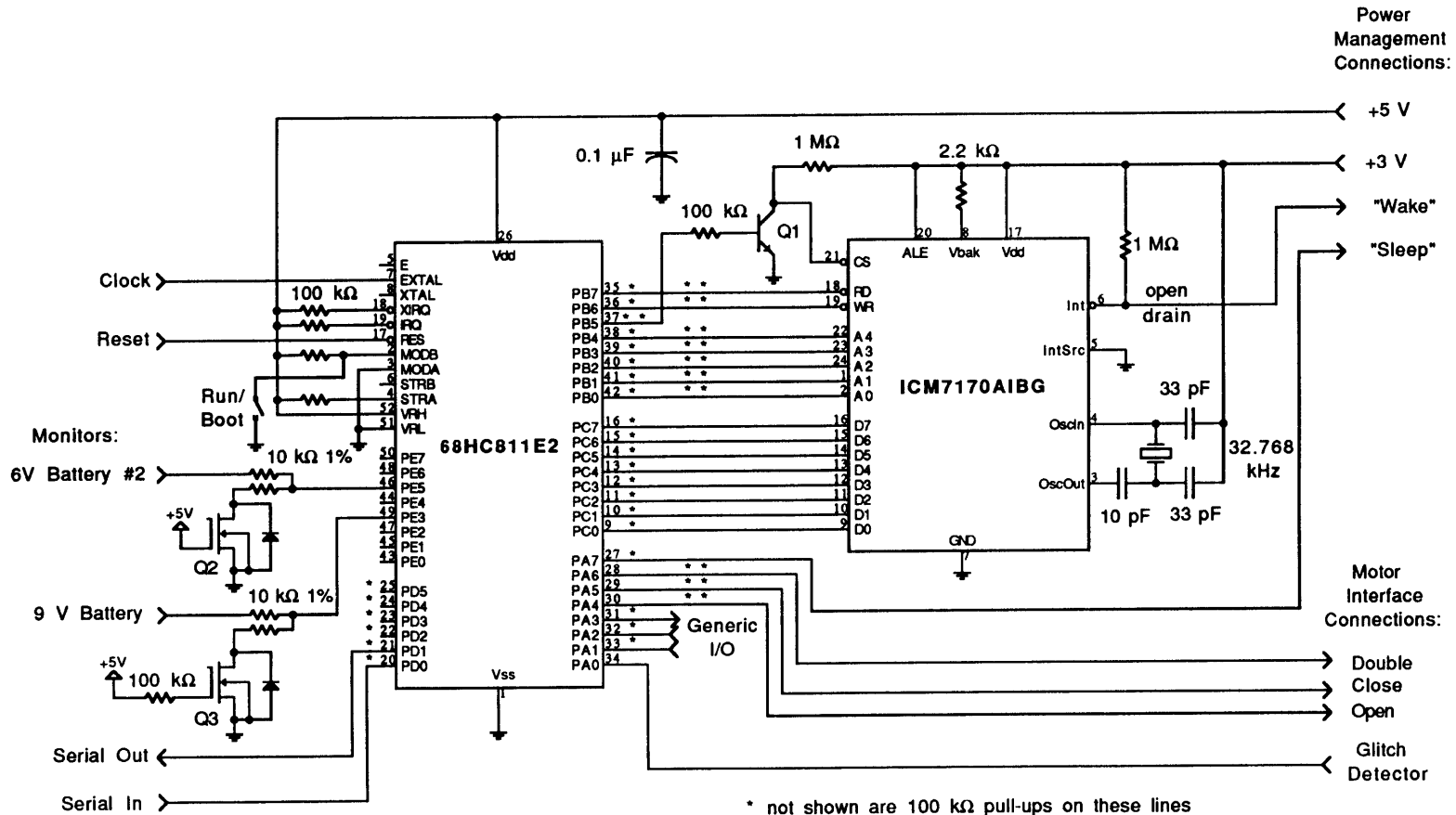
Appendix B: Electronic Parts, Suppliers and Prices						
Part Number	Description	Mgfr	Distr.	# per circuit	Cost each	Cost of 1 circuit
TLE2037D	OP-37 low noise op amp, 8-pin DIP	TI	Newark	1	\$1.860	\$1.86
CA3130E	CMOS high-speed op amp	Harris	Mauser	1	\$1.680	\$1.68
CA3260E	dual CMOS op amp	Harris	Digikey	2	\$2.200	\$4.40
MAX406CSA	micropower CMOS op amp	Maxim	Arrow	2	\$6.000	\$12.00
LTC1042CS	sampling window comparator	LT	Gerber	1	\$2.550	\$2.55
MAX667	voltage regulator w/ shutdown	Maxim	Bell	1	\$4.900	\$4.90
CD74HC73M	HCMOS JK flip flop	Harris	Gerber	1	\$0.320	\$0.32
CD74HC27M	HCMOS triple, three-input NOR gate	Harris	Gerber	1	\$0.245	\$0.25
74HC14	HCMOS hex Schmidt input inverter	Harris	Mauser	1	\$0.380	\$0.38
MC68HC811E2FN	HCMOS microprocessor with EEPROM	Motorola	Hamilton	1	\$15.300	\$15.30
ICM7170IBG	real-time clock IC	Harris	Falcon	1	\$7.500	\$7.50
Si9942DY	Dual, complementary, HEXFETs	Siliconix	Sterling	3	\$3.000	\$9.00
766-141-R100K	resistor network, 100 kΩ, SO-14 pkg.	CTS	Digikey	2	\$1.301	\$2.60
260-1M	thick-film chip res., 0805 pkg, 1MΩ	TransOhm	Mauser	10	\$0.030	\$0.30
260-100K	thick-film chip res., 0805 pkg, 100kΩ	TransOhm	Mauser	19	\$0.030	\$0.57
260-10K	thick-film chip res., 0805 pkg, 10kΩ	TransOhm	Mauser	9	\$0.030	\$0.27
260-1K	thick-film chip res., 0805 pkg, 1kΩ	TransOhm	Mauser	5	\$0.030	\$0.15
260-100	thick-film chip res., 0805 pkg, 100Ω	TransOhm	Mauser	1	\$0.030	\$0.03
260-4.7K	thick-film chip res., 0805 pkg, 4.7kΩ	TransOhm	Mauser	1	\$0.030	\$0.03
260-2.2K	thick-film chip res., 0805 pkg, 2.2kΩ	TransOhm	Mauser	2	\$0.030	\$0.06
260-6.8K	thick-film chip res., 0805 pkg, 6.8kΩ	TransOhm	Mauser	1	\$0.030	\$0.03
260-47K	thick-film chip res., 0805 pkg, 47kΩ	TransOhm	Mauser	1	\$0.030	\$0.03
880-0101	wirewound resistor, 0.1 Ω	Clarostat	Allied	2	\$1.740	\$3.48
10F300 - 20MΩ	carbon comp, 1/8W resistor, 20MΩ	Allen-Brad	Newark	2	\$0.590	\$1.18
10F300 - 10MΩ	carbon comp, 1/8W resistor, 10MΩ	Allen-Brad	Newark	6	\$0.590	\$3.54
10F300 - 2.7MΩ	carbon comp, 1/8W resistor, 2.7MΩ	Allen-Brad	Newark	1	\$0.590	\$0.59
290-1.0M	metal-film chip res., 1206 pkg, 1.0MΩ	TransOhm	Mauser	2	\$0.050	\$0.10
290-100K	metal-film chip res., 1206 pkg, 100kΩ	TransOhm	Mauser	1	\$0.050	\$0.05
290-12.1K	metal-film chip res., 1206 pkg, 12kΩ	TransOhm	Mauser	5	\$0.050	\$0.25
290-10K	metal-film chip res., 1206 pkg, 10kΩ	TransOhm	Mauser	5	\$0.050	\$0.25
P 4.99K F	metal-film chip res., 1206 pkg, 5.0kΩ	Panasonic	Digikey	1	\$0.053	\$0.05
290-1.5K	metal-film chip res., 1206 pkg, 1.5kΩ	TransOhm	Mauser	1	\$0.050	\$0.05
PCC104B	ceramic chip cap., 1206 pkg, 0.1 μF	Panasonic	Digikey	8	\$0.528	\$4.22
140-CC501B103K	ceramic chip cap., 0805 pkg, 0.01 μF	XICON	Mauser	9	\$0.190	\$1.71
PCC102CG	cer. chip cap. NPO TC, 0805 pkg, 0.001 μF	Panasonic	Digikey	2	\$0.264	\$0.53
PCC101CG	ceramic chip cap., 0805 pkg, 100 pF	Panasonic	Digikey	4	\$0.168	\$0.67
PCC273BG	ceramic chip cap., 0805 pkg, 0.027 μF	Panasonic	Digikey	2	\$0.240	\$0.48
PCC330CG	ceramic chip cap., 0805 pkg, 33 pF	Panasonic	Digikey	2	\$0.152	\$0.30
PCC150CN	ceramic chip cap., 0805 pkg, 15 pF	Panasonic	Digikey	1	\$0.144	\$0.14
PCC100CN	ceramic chip cap., 0805 pkg, 10 pF	Panasonic	Digikey	1	\$0.144	\$0.14
PCC470CG	cer. chip cap., NPO TC, 0805 pkg, 47 pF	Panasonic	Digikey	1	\$0.152	\$0.15
PCC103B	cer. chip cap., XR7 TC, 1206 pkg, 0.01 μF	Panasonic	Digikey	3	\$0.184	\$0.55
P4920	monolithic ceramic cap, 1.0 μF	Panasonic	Digikey	1	\$0.748	\$0.75
PCT2476	tantalum chip capacitor, 10V, 47 μF	Panasonic	Digikey	2	\$1.748	\$3.50
PCT1686	tantalum chip capacitor, 6.3V, 68 μF	Panasonic	Digikey	1	\$1.748	\$1.75
PCT1226	tantalum chip capacitor, 6.3V, 22 μF	Panasonic	Digikey	1	\$1.348	\$1.35
PCT2106	tantalum chip capacitor, 10V, 10 μF	Panasonic	Digikey	1	\$1.248	\$1.25
PCT3105	tantalum chip capacitor, 16V, 1.0 μF	Panasonic	Digikey	4	\$0.524	\$2.10
TK1227	adjustable inductor, 470 μH	TOKO	Digikey	1	\$2.050	\$2.05
S1012-36-ND	header strip, right angle, 36 position	Sullins	Digikey	0.5	\$1.110	\$0.56
278-502	wire for transmitter coil, 1 ft.	unknown	Radio Shak	6	\$0.048	\$0.29
C2016W-X-ND	hook-up wire, 22 AWG, 1 ft.	Card	Digikey	1	\$0.037	\$0.04
1N5820GI	Schottkey diode, 3 Amp cont.	Gen Instr	Digikey	2	\$0.512	\$1.02
FMMT3904	NPN transistor, SOT-23 pkg.	Zetex	Digikey	7	\$0.210	\$1.47
FMMT3906	PNP transistor, SOT-23 pkg.	Zetex	Digikey	3	\$0.263	\$0.79
BSS138ZX	N-channel MOSFET, SOT-23 pkg.	Zetex	Digikey	3	\$0.630	\$1.89
NC26-32.768	32768 Hz crystal	Fox	Cronin	1	\$0.300	\$0.30
276-1122	low-power detector diode (1N914 type)	unknown	Radio Shak	1	\$0.099	\$0.10
ZC2800E	Schottkey diode, SOT-23 pkg.	Zetex	Digikey	2	\$0.581	\$1.16
BAS16ZX	Si diode, single, SOT-23 pkg.	Zetex	Digikey	1	\$0.225	\$0.23
BAW56ZX	Si diode, dual, com. anode, SOT-23 pkg.	Zetex	Digikey	1	\$0.338	\$0.34
BAV99ZX	Si diode, dual, series, SOT-23 pkg.	Zetex	Digikey	1	\$0.300	\$0.30
TOTAL						\$103.87

Appendix B, continued: Electronic Parts Suppliers

Distributor	Address	Phone Number	Contact
Allied	7410 Pebble Dr. Ft. Worth, TX 76118	800-433-5700	Annie
Arrow	50 Horseblock Rd., Brookhaven, NY 11719	508-658-0900	Jeff
Bell		508-474-8880	Gary
Cronin/Fox	5570 Enterprise Pkwy, Ft. Meyers, FL 33905	813-693-1554	Jack
Digikey	701 Brooks Ave. S., Thief River Falls, MN 56701	800-344-4539	any
Falcon	Connecticut	203-878-5272	Tom
Gerber	128 Carnegie Row, Norwood, MA 02062	617-769-6000	Mike
Hamilton	10 D Centennial Dr., Peabody, MA 01960	508-332-3701	Brian
Mauser	12 Emery Ave, Randolph, NJ 07869	800-346-6873	any
Newark	10 G Roessler Rd., Woburn, MA 01801	508-683-0913	Charlie
Radio Shack	Central Square, Cambridge, MA	547-7332	any

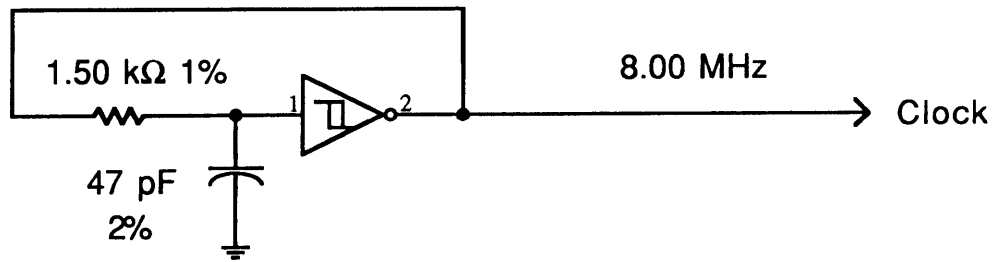
Appendix C: Schematic diagrams of the sampler electronics.

Figure C-1: Microprocessor and Real-Time Clock

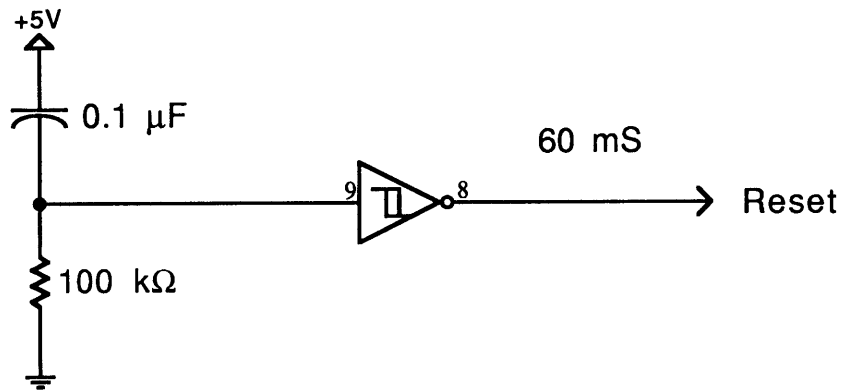


* not shown are 100 kΩ pull-ups on these lines
 ** these outputs drive low on power-up

Figure C-2: Microprocessor Clock and Reset



74HC14:
GND=3,5,7
+5V=11,13,14



I_{CC} , this page = 2.7 mA

Power to Communications Board:

Figure C-3: Power Management System

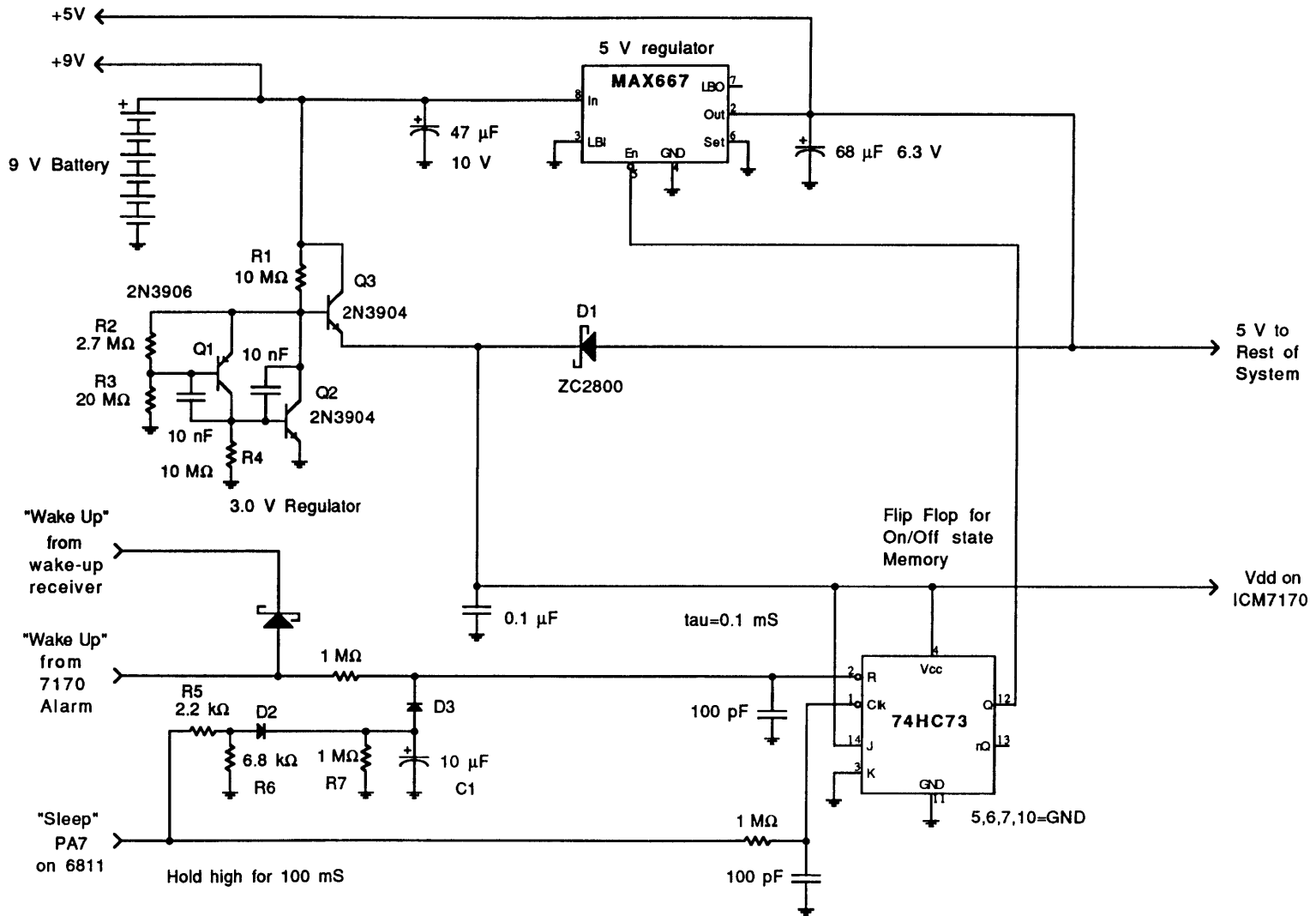
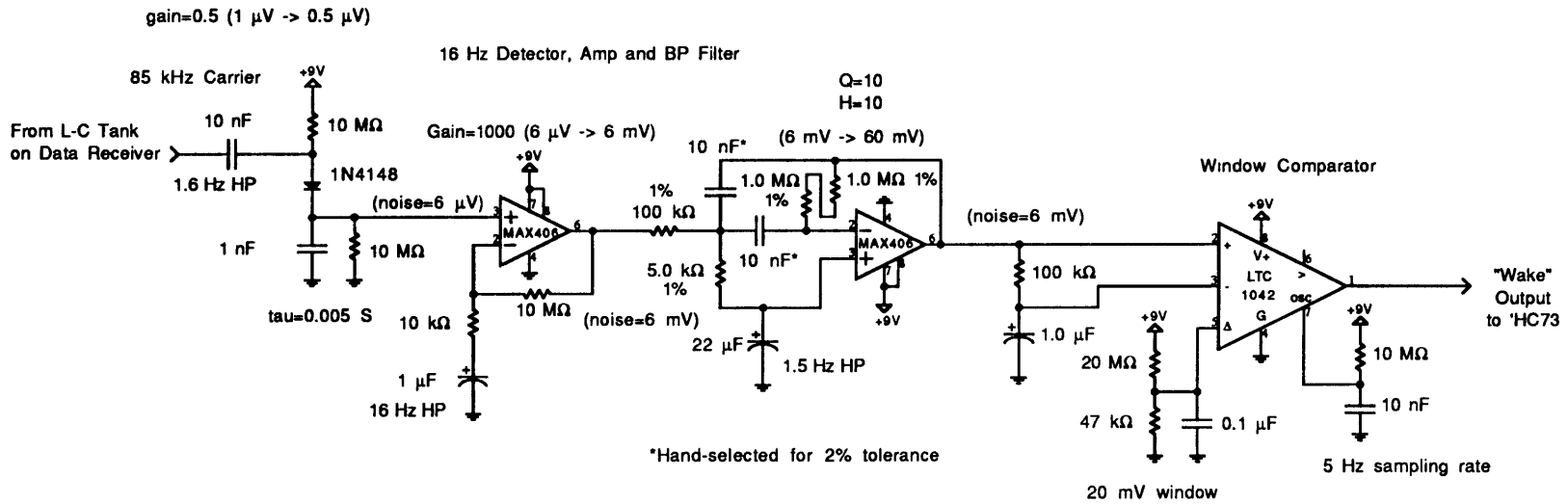
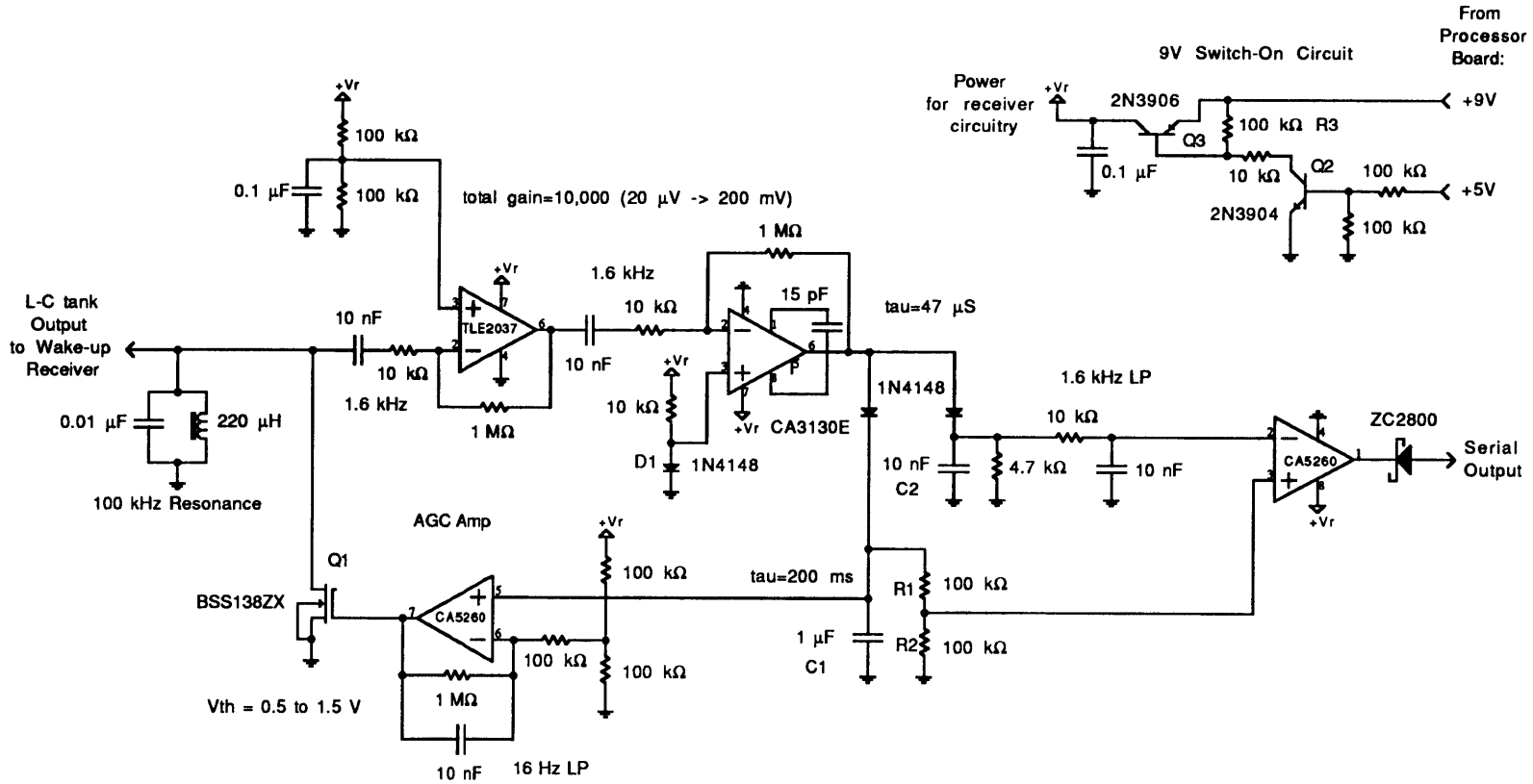


Figure C-4: Wake-Up Receiver



Complete Circuit Current Consumption: 6.5 μA

Figure C-5: Magnetic Data Receiver



Transmitter Oscillator

Figure C-6: Motor Interface and transmitter Circuitry

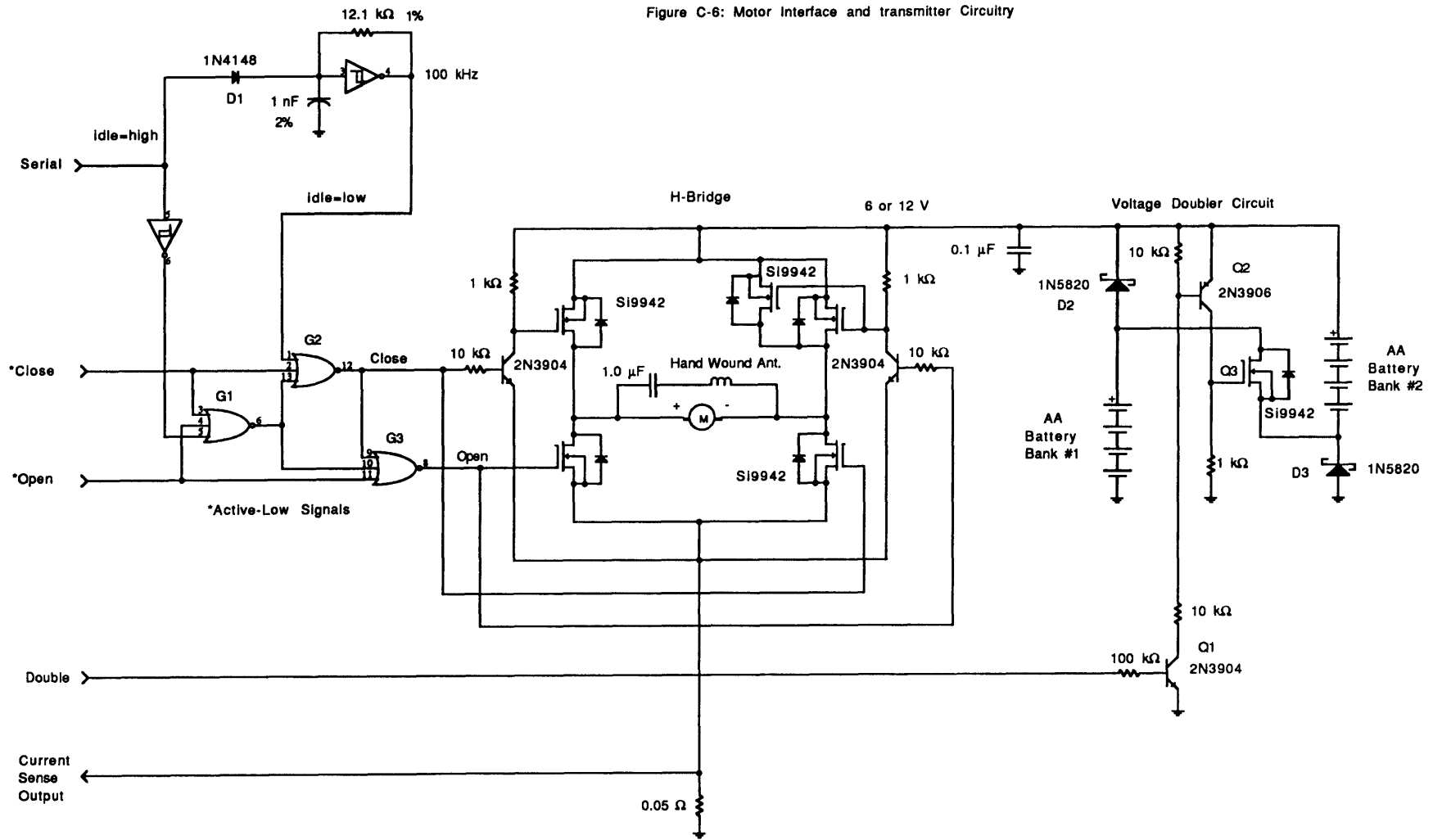
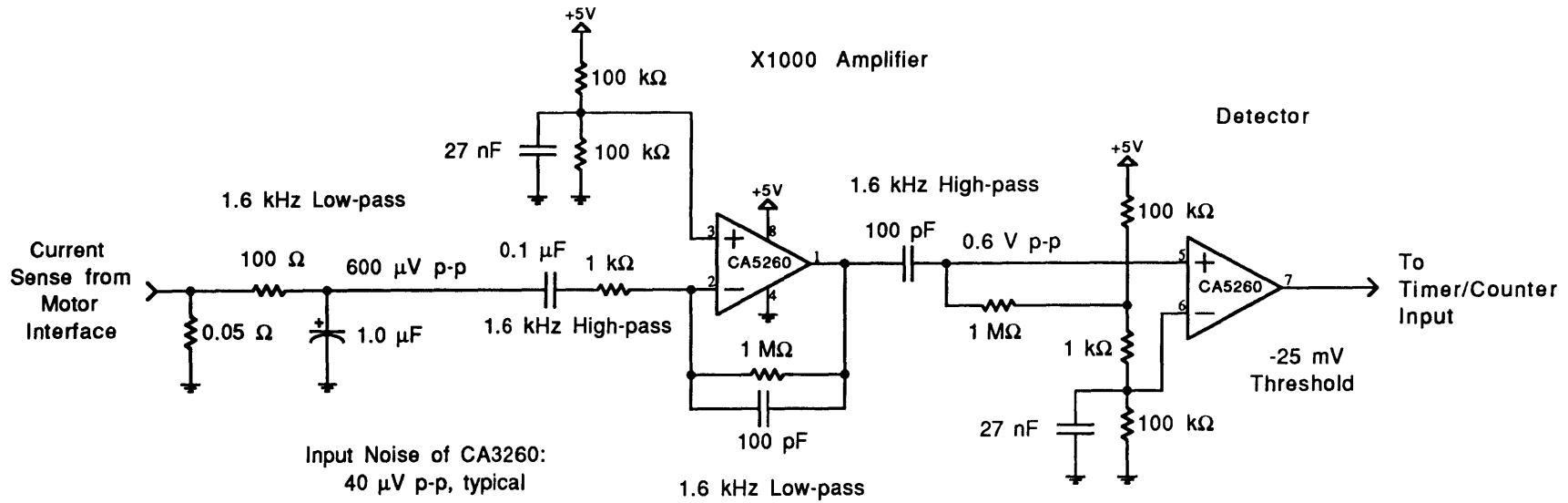
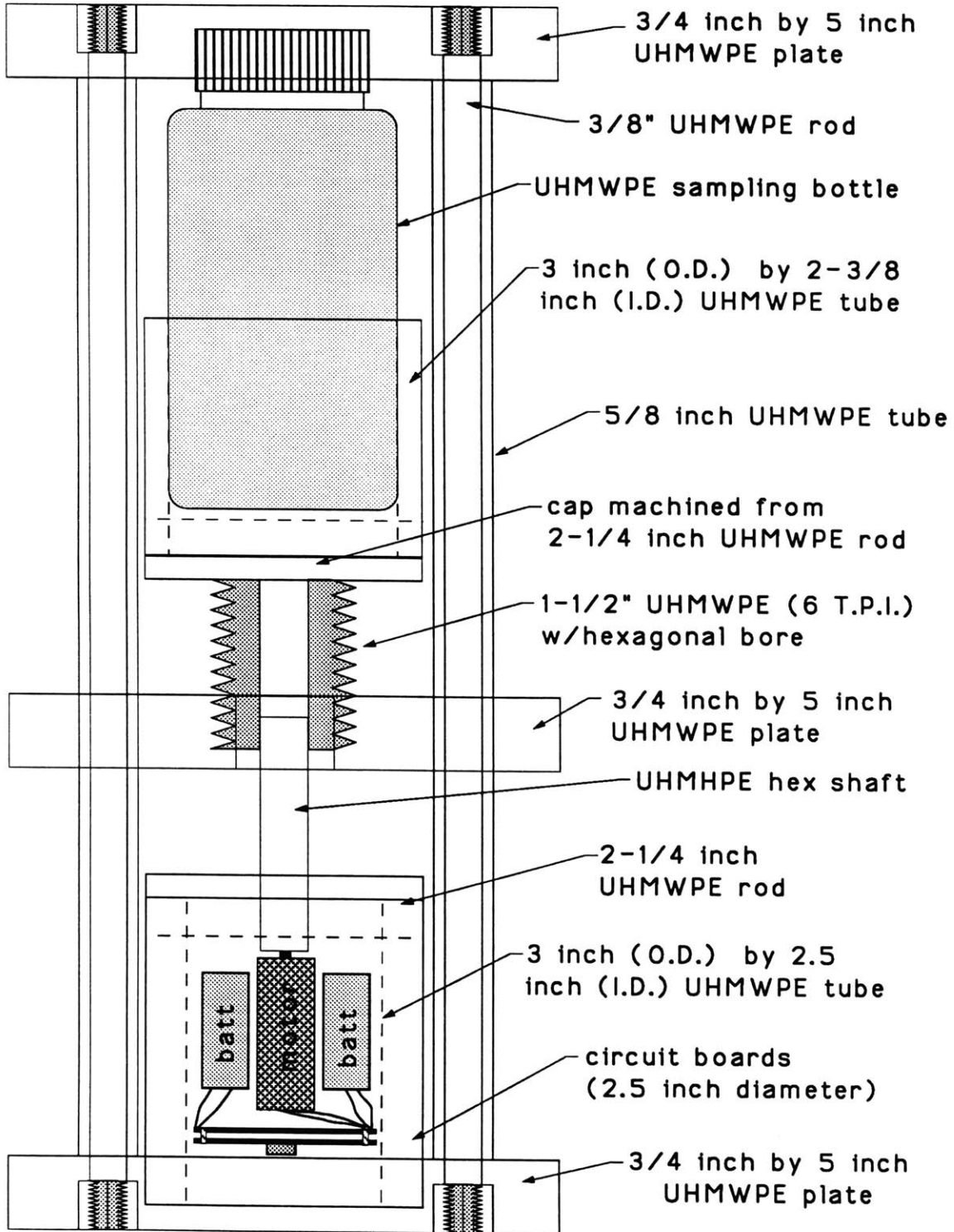


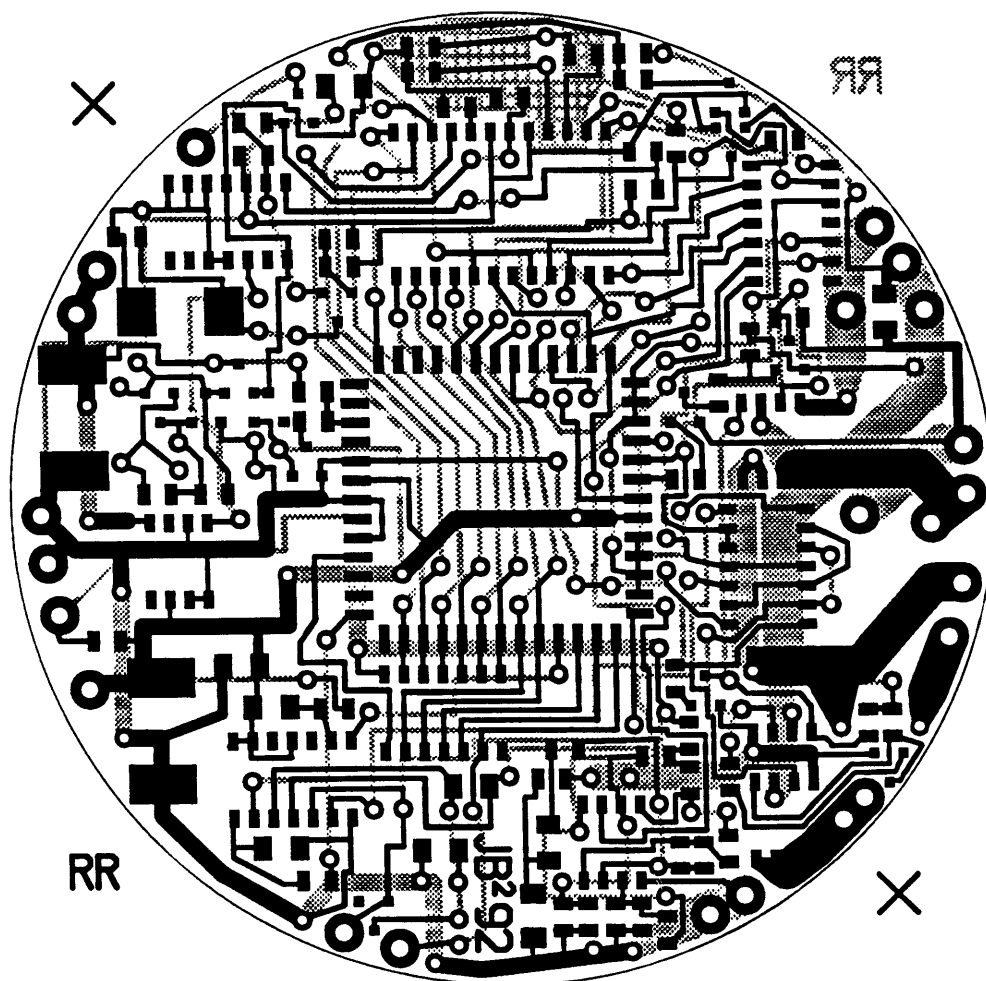
Figure C-7: Motor-Speed Detector Circuitry



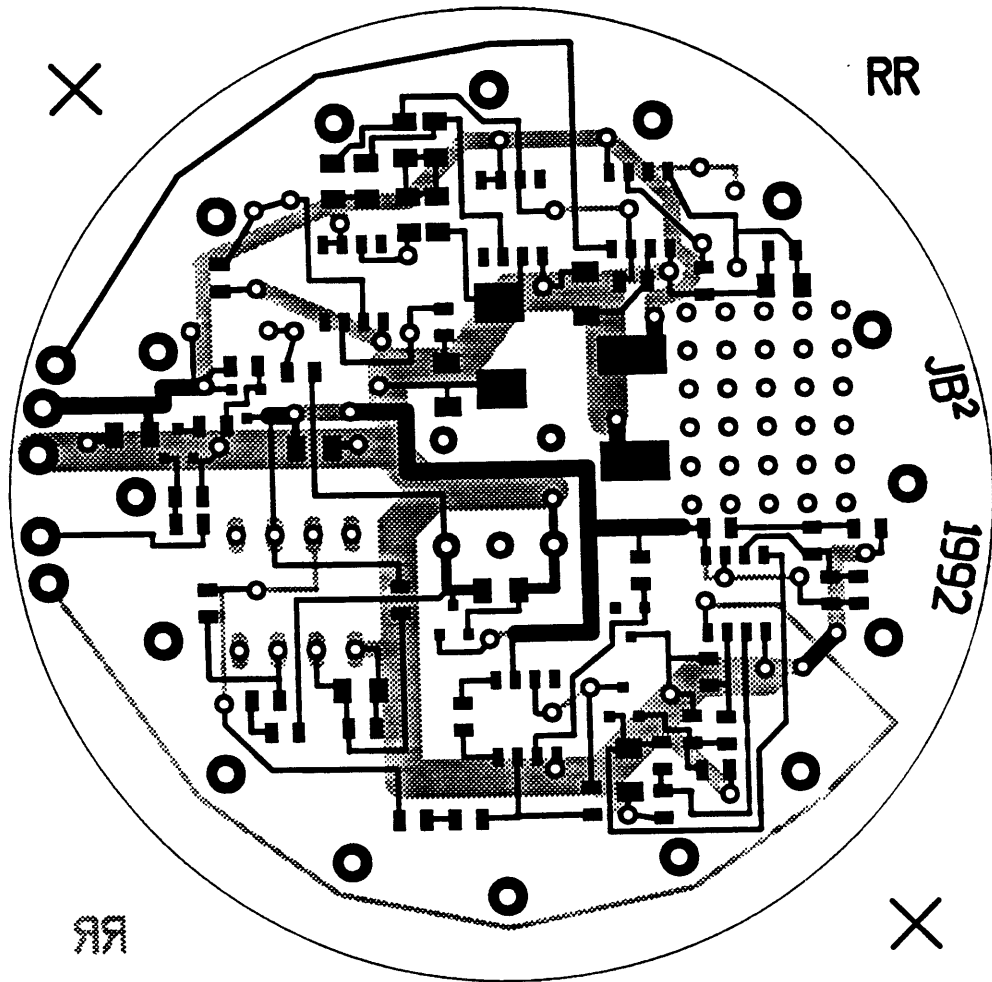
appendix d: sampler unit hardware



Appendix E: Images of printed circuit boards.



Component side X-ray view of main sampler electronics printed circuit board. Scale: 2X.



Component side X-ray view of printed circuit board for the magnetic communications circuitry. Scale: 2X.

References

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- ⁷1992 *New Releases Databook*. Maxim Integrated Products, Inc. 120 San Gabriel Dr., Sunnyvale, CA 94086. (408) 737-7600.
- ⁸*Linear Data Book*, 1990. Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95038. (408) 432-1900.
- ⁹Natarajan, Sunjaran, 1987. *Theory and Design of Linear Active Networks*, New York, New York: Macmillan.
- ¹⁰*Linear and Telecom ICs*, 1991. Harris Semiconductor Corp., 1301 Woody Burke Rd., Melbourne, FL 32902. (407) 724-3000.
- ¹¹*Little Foot Series Product Databook*. Siliconix Inc., 2201 Laurelwood Road, Santa Clara, CA 95056. (800)-988-8000.