Hole Transport in Strained SiGe-Channel MOSFETs: Velocity in Scaled Devices and Mobility Under Applied Mechanical Strain

By

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Abstract

Since the 90 nm CMOS technology node, geometric scaling of CMOS has been supplemented with strain to boost transistor drive current. Future CMOS technology nodes (i.e. beyond the 32 nm node) will require more significant changes to continue improvements in transistor performance. Novel CMOS channel materials and device architectures are one option for enhancing carrier transport and increasing device performance. In this work strained SiGe and Ge are examined as a means of increasing the drive current in deeply scaled CMOS. As part of this work a novel high mobility strained-Ge on-insulator substrate has been developed, and the hole transport characteristics of short channel and asymmetrically strained-SiGe channel p-MOSFETs have been explored.

A thin-body biaxial compressive strained-Si/strained-Ge heterostructure on-insulator (HOI) substrate has been developed, which combines the electrostatic benefits of the thin-body architecture with the transport benefits of biaxial compressive strain. A novel Germanium on Silicon growth method and a low temperature bond and etch-back process have been developed to enable Ge HOI fabrication. P-MOSFETs were also fabricated using these substrates and the hole mobility characteristics were studied.

The hole mobility and velocity characteristics of short channel biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs on-insulator have also been examined. Devices with gate lengths down to 65 nm were fabricated. The short channel mobility characteristics were extracted and a 2.4x hole mobility enhancement relative to relaxed-Si was observed. The measured hole velocity enhancement is more modest at about 1.2x. Band structure and ballistic velocity simulations suggest that a more substantial velocity improvement can be expected with the incorporation of added longitudinal uniaxial compressive strain in the SiGe channel.

The hole mobility characteristics of biaxial strained SiGe and Ge p-MOSFETs with applied uniaxial strain are also studied. The hole mobility in biaxial compressive strained SiGe is already enhanced relative to relaxed Si. It is observed that this mobility enhancement increases further with the application of <110> longitudinal uniaxial compressive strain. Since hole mobility and velocity are correlated through their dependence on the hole effective mass, a mass driven increase in mobility with applied uniaxial strain should result in an increase in velocity. Simulations have also been performed to estimate the hole effective mass change in asymmetric strained SiGe. Finally the piezoresistance coefficients of strained SiGe are extracted and found to be larger than in Si.

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Chapter 1

INTRODCUTION

1.1 Thesis Introduction

Since the 90 nm CMOS technology node dimensional scaling has been supplemented with strain to increase transistor drive current [1-2]. The tensile and compressive strain introduced into the Si channel improves the electron and hole transport properties respectively, resulting in higher transistor drive currents [3-7]. The virtual source velocity extracted from state-of-the-art devices by A. Khakifirooz et al [124] reveals a dramatic increase in hole velocity with the introduction on uniaxial compressive strain in Si, Figure 1.1. As dimensional scaling of CMOS continues, less area will be available to incorporate the channel stressors needed to enhance carrier transport and to contact the source/drain regions of the transistor leading to an increase in the extrinsic device resistance. While incorporating addition strain into the Si channel in deeply scaled CMOS presents a practical limitation, a more fundamental limit exists. The velocity enhancement provided by uniaxial compressive strain Si is expected to saturate with increasing strain. Figure 1.2 helps illustrate how aggressive scaling of dimensional parameters at the 32 nm node has resulted in limited space available to incorporate channel stressors and to contact the source/drain regions [25][27]. Future CMOS technology generations will require further innovation to overcome these limitations and to realize improvements in transistor performance. Several technologies are currently being explored as options for improving transistor performance in the deeply scaled regime. Novel channel materials are being examined as a means of increasing drive current through improvements in carrier transport properties [8-10]. More sophisticated device

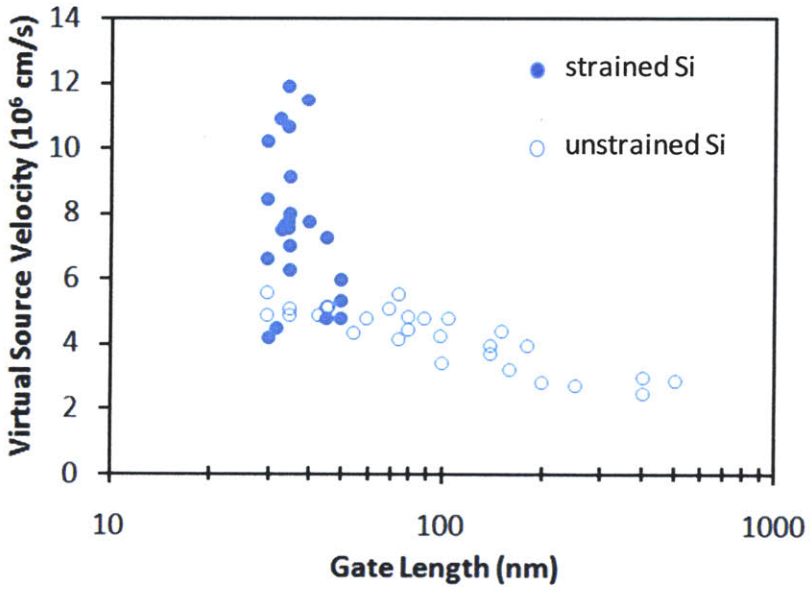


Figure 1.1 The virtual source velocity (υ_{xo}) versus gate length in state of the art uniaxial-strained and relaxed Si devices. Results from [124].

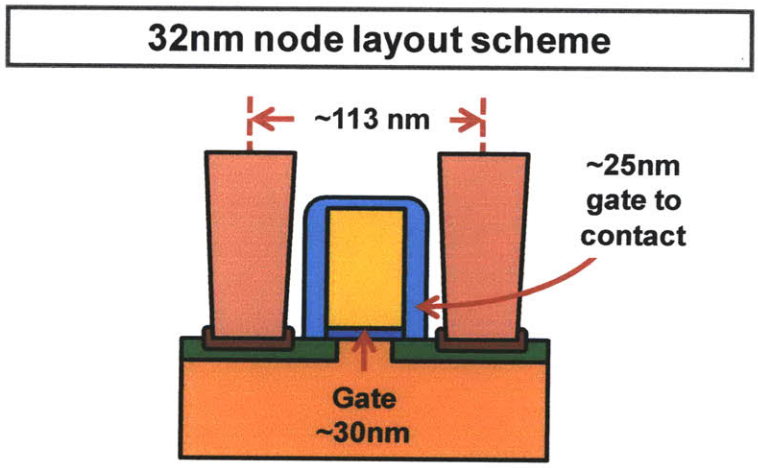


Figure 1.2 Intel's 32 nm CMOS technology node layout scheme. Continued dimensional scaling of CMOS has resulted in a very tight layout. Beyond the 32 nm technology node spatial constraints may make it difficult to contact the source/drain region and incorporate channel stressors, which can lead to reverse scaling effects. Replacing the Si channel with a high mobility material is an option available to realize drive current gains in deeply scaled MOSFETs. Dimensions from [25][27].

architectures, like ultrathin-body FETs, fin-FETs, and nano-wire FETs, are also being explored in an attempt to maintain electrostatic integrity in deeply scaled devices [11-14]. To continue to realize improvements in device density, 3D integration is also being considered [15-16].

In this work strained-SiGe and strained-Ge are examined as alternative channel materials for deeply scaled p-MOSFETs. The hole transport improvement provided by biaxial compressive strained-SiGe and strained-Ge has been well documented [9][17][18]. Hole mobility gains of over 10x have been realized in long channel biaxial compressive strained-Ge channel p-MOSFET relative to relaxed-Si [9][26]. The hole mobility performance of short channel p-MOSFETs has been examined [19-24], but the transport performance is not as impressive due to measures taken to maintain electrostatic integrate at smaller gate lengths (i.e. halo, extension, and body doping implants). These measures disrupt the strain and increase the number of coulombic scattering centers in the channel. This makes it difficult to understand the fundamental limit of the transport improvement that can be realized with biaxial compressive strained-SiGe.

As part of this work a novel biaxial compressive strained Ge on-insulator substrate, which is called Ge Heterostructure on Insulator (Ge HOI), has been developed. This substrate combines the electrostatic benefits of the thin-body architecture with the high hole mobility characteristics of strained-Ge. This is advantageous in the deeply scaled regime where maintaining electrostatic integrity is critical and improvements in carrier transport are needed.

The transport performance gains of biaxial compressive strained-SiGe in short channel p-MOSFETs are also examined. The hole mobility and velocity of short channel p-MOSFETs are measured and the transport performance evaluated. Unlike hole mobility, the hole velocity characteristics of short channel biaxial compressive strained-SiGe p-MOSFETs have yet to be explored. Hole velocity is a more appropriate transport measure in nano-scale MOSFETs. The goal

is to determine if the impressive mobility gains observed in fully-strained biaxial compressive strained-SiGe translates into an equally impressive velocity gain at shorter gate lengths. Subsequently, alternative strain configurations are theoretically explored to determine improved strain distributions for increasing carrier velocity.

The influence of additive <110> longitudinal uniaxial compressive strain on the hole mobility characteristics of initially biaxial strained-SiGe p-MOSFETs is also examined. Additive uniaxial compressive strain is applied via mechanical bending to biaxial compressive strained-SiGe p-MOSFETs and the corresponding change in mobility examined. Hole mobility and velocity are positively correlated through their dependence on the hole effective mass, and therefore any mass driven change in mobility with applied uniaxial strain is expected to result in a change in velocity. Simulations have been performed to determine if the observed change in mobility with applied uniaxial strain is a mass driven effect. If this is the case, then the hole velocity characteristics of short channel biaxial compressive strained-SiGe p-MOSFETs should also benefit from the addition of <110> uniaxial compressive strain component.

1.2 Thesis Outline

In chapter 2 the origins of carrier transport enhancement in strained SiGe and Ge will be discussed. The influence of improvements in transport metrics on device performance will also be discussed. In chapter 3 the development of strained-Ge HOI will be presented. A novel Ge on Si growth method and low temperature bond process will be discussed. Measurements of the strain and Ge percentage before and after substrate fabrication will also be presented. This chapter will conclude with hole mobility results for strained-Ge HOI. In chapter 4 the hole mobility and velocity characteristics of short channel biaxial compressive strained-SiGe p-MOSFETs will be examined. The optimal strain configuration for improving hole velocity will also be investigated.

In chapter 5 the hole mobility characteristics of biaxial compressive strained-SiGe with additive uniaxial strain will be examined. The mechanism driving the observed change in mobility will also be investigated. This thesis will conclude with chapter 6 where the conclusions and contributions of this work will be discussed. Additional detailed information on the Ge HOI, SSDOI, and short channel device fabrication will be provided in the appendices.

Chapter 2

THESIS BACKGROUND

2.1 Introduction

In this chapter, background material essential to understanding hole transport in strained SiGe and Ge p-MOSFETs will be discussed. First an introduction into the material properties of Si, SiGe, and Ge will be provided. Then the mechanism for introducing strain into Si, SiGe, and Ge will also be discussed. Following this the strain impact on the valence band structure will be reviewed. How these strain induced changes impact carrier transport will also be presented. Carrier transport in the context of strained SiGe and Ge p-MOSFETs will then be reviewed. Finally, carrier transport in nano-scale MOSFETs will be discussed.

2.2 Si, SiGe, and Ge material properties

Small changes in the lattice constant of Si, SiGe, and Ge can result in significant changes to their electrical properties. Silicon has a lattice constant of 5.432 Å. The lattice constant of Germanium is 4.1% larger at 5.655 Å. Vegard's law provides a linear interpolation for the lattice constant of Silicon Germanium alloys [28]. The Ge fraction dependent lattice constant, a(x), is given by

$$a(x) = x \cdot a_{Ge} + (1 - x)a_{Si} \qquad \text{Equation 2.1}$$

where x, $a_{Ge,}$ and a_{Si} are the Ge fraction in the silicon germanium, the lattice constant of Si, and the lattice constant of Ge respectively. Pseudomorphic growth of $Si_{1-y}Ge_y$ on a relaxed $Si_{1-x}Ge_x$ layer, where $y < x$, causes the in-plane $Si_{1-y}Ge_y$ lattice to stretch and take on the lattice constant of the underlying relaxed $Si_{1-x}Ge_x$ substrate. This introduces biaxial tensile strain into the lattice matched

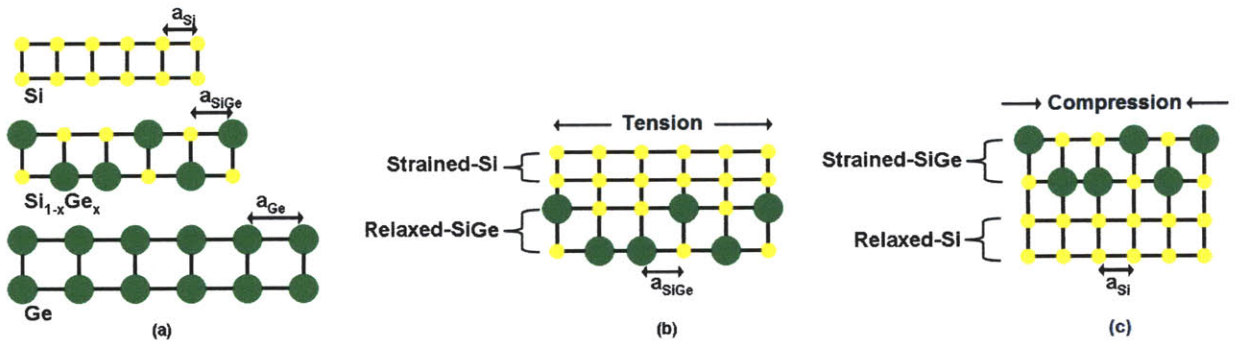


Figure 2.1 (a) A depiction of the relative size difference between the relaxed lattice spacing in Si, $Si_{1-x}Ge_x$ and Ge. (b) A depiction of the method by which biaxial tensile strain is introduced into Si (i.e. pseudomorphic growth of Si onto relaxed-$Si_{1-x}Ge_x$). (c) A depiction of the method by which biaxial compressive strain is introduced into $Si_{1-y}Ge_y$ (i.e. pseudomorphic growth of $Si_{1-y}Ge_y$ onto relaxed-$Si_{1-x}Ge_x$).

$Si_{1-y}Ge_y$ layer. By varying the Ge fraction in the relaxed $Si_{1-x}Ge_x$ layer the strain in the $Si_{1-y}Ge_y$ layer can be adjusted. Compressive strain can also be introduced into $Si_{1-y}Ge_y$ similarly through pseudomorphic growth on a relaxed Si or relaxed $Si_{1-x}Ge_x$ substrate where $y > x$. The equilibrium lattice constant of $Si_{1-y}Ge_y$ is greater than that of Si or $Si_{1-x}Ge_x$ and thus it experiences biaxial compression to conform to the smaller lattice constant of the underlying material. In Figure 2.1 a ball and stick depiction of the relaxed Si, SiGe, and Ge lattices are presented as well as diagram depicting the means by which tensile and compressive strain are introduced into Si and SiGe respectively.

As mentioned the strain in $Si_{1-y}Ge_y$ can be tuned by varying the Germanium fraction in the underlying $Si_{1-x}Ge_x$ substrate. The amount of in-plane strain present in the biaxial strained-$Si_{1-y}Ge_y$ layer is given by

$$\varepsilon = \frac{a_y}{a_x} - 1 \qquad \text{Equation 2.2}$$

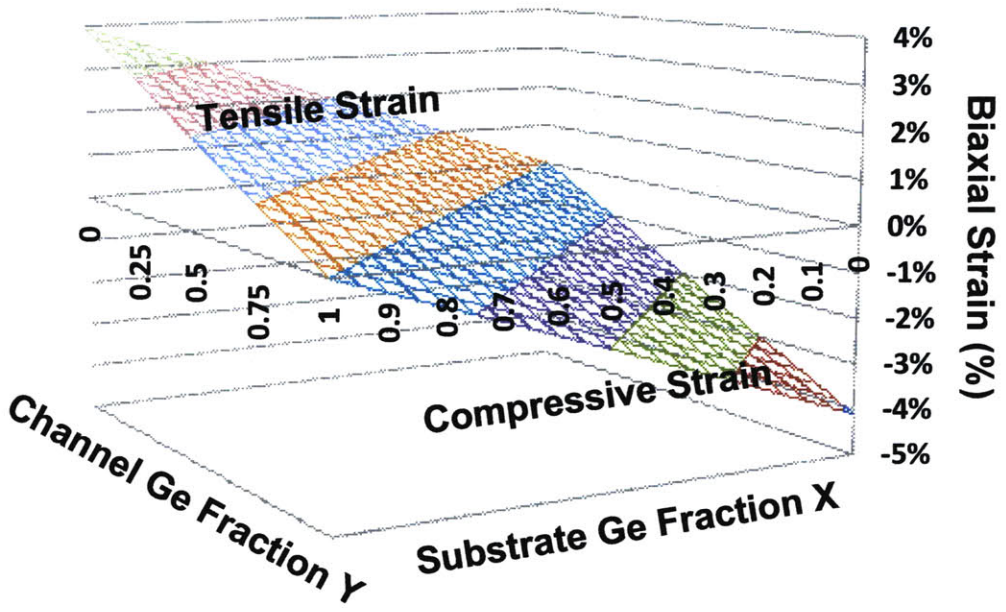


Figure 2.2 A 2D map of the biaxial strain in $Si_{1-y}Ge_y$ pseudomorphic to relaxed $Si_{1-x}Ge_x$, where $0 < Y < 1$ and $0 < X < 1$. Y is the channel Ge fraction and X is the substrate Ge fraction.

where ε is the amount of strain present in the $Si_{1-y}Ge_y$ layer, a_y is the lattice constant of $Si_{1-y}Ge_y$, and a_x is the lattice constant of the underlying relaxed $Si_{1-x}Ge_x$ substrate. A negative strain value indicates biaxial compressive strain and a positive value indicates that biaxial tensile strain is present in the strained layer. In Figure 2.2 a 2D contour map of the strain present in biaxial strained-$Si_{1-y}Ge_y$ pseudomorphic to relaxed-$Si_{1-x}Ge_x$ is plotted, where y and x both range from 0 to 1 (i.e. pure Si to pure Ge). Notice that when $x > y$ tensile strain is present in the $Si_{1-y}Ge_y$ layer, when $y > x$ compressive strain is present in the $Si_{1-y}Ge_y$ layer, and when $y = x$ no strain is present in the $Si_{1-y}Ge_y$ layer.

2.2.1 Y/X notation introduced

Throughout this work the Y/X biaxial strain notation will be used. Y represents the channel Ge percentage, and X is the substrate Ge percentage. This notation provides information about the channel Ge composition and the amount of strain present in the channel. For example, a 60/30 structure would consist of a strained $Si_{0.4}Ge_{0.6}$ layer pseudomorphic to a relaxed $Si_{0.7}Ge_{0.3}$ layer, which if we refer to Figure 2.2, has about -1.2% biaxial compressive strain in the $Si_{0.4}Ge_{0.6}$ layer. This notation will prove useful since knowing both the channel Ge percentage and strain are critical in understanding the potential transport benefits of the material.

2.2.2 Methods for introducing uniaxial strain into Si and SiGe

The three dominant methods for introducing uniaxial strained into Si and SiGe involve using a stress liner, an embedded material stressor, or though 1D strain relaxation of a biaxial strained material [1-5][29]. Compressive stressors are highly stressed films which deform the underlying materials through stress transfer. This technology has been used since the 90 nm technology node, where tensile stress liners have been used to stretch the NMOS channel to improve electron transport and compressive stress liners used in PMOS devices to compact the channel and improve hole transport in Si [5]. Embedded material stressors have also been used to strain Si [1-2]. With the embedded stressor technology, the stress is mostly transferred to the flanking material adjacent to the embedded stressor. In state of the art logic p-MOSFETs embedded SiGe source/drains are utilized to introduce compressive strain into the Si channel. The SiGe in the source/drain region is pseudomorphic to the underlying and surrounding relaxed Si, which puts the SiGe under compressive stress. At shorter gate lengths the compressive stress is transferred into the channel improving hole transport. A similar technology exists where $Si_{1-y}C_y$ is utilized as the embedded source/drain material to benefit electron transport in NMOS devices

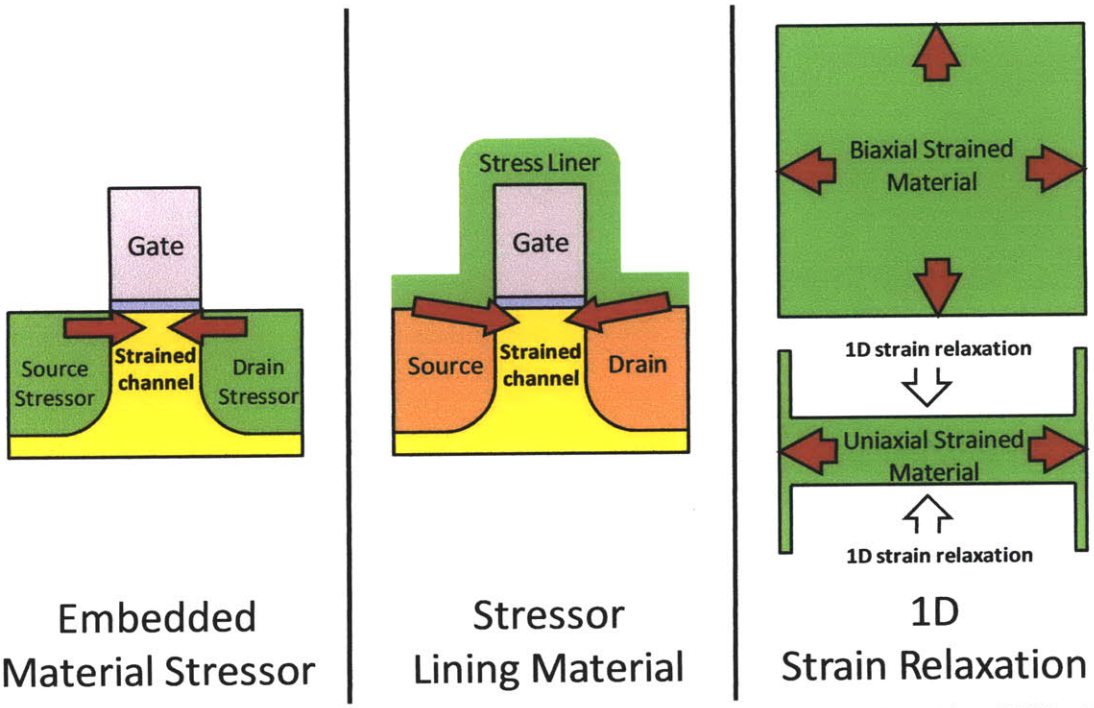


Figure 2.3 A depiction of three common methods used to introduce uniaxial strain into Si and SiGe. The red arrows indicate the strain direction.

[135][136]. Since SiC possesses a smaller lattice constant than Si it is under tensile strain when pseudomorphic to relaxed Si. At shorter gate length this tensile strain is transferred into the Si channel benefiting electron transport. Relaxing the strain in biaxial strained material has also proven to be an effective means of realizing a uniaxial strain configuration [29]. This method involves taking a biaxial strained material and patterning it into a long slender bar. In this scenario the strain along the length of the bar is anchored and maintained, while the transverse strain along the shorter dimension relaxes providing a uniaxial strain distribution. In Figure 2.3 a schematic is provided of the various mechanisms by which uniaxial strain can be introduced into Si or SiGe. In the next section we will see how strain impacts the valence band structure of SiGe.

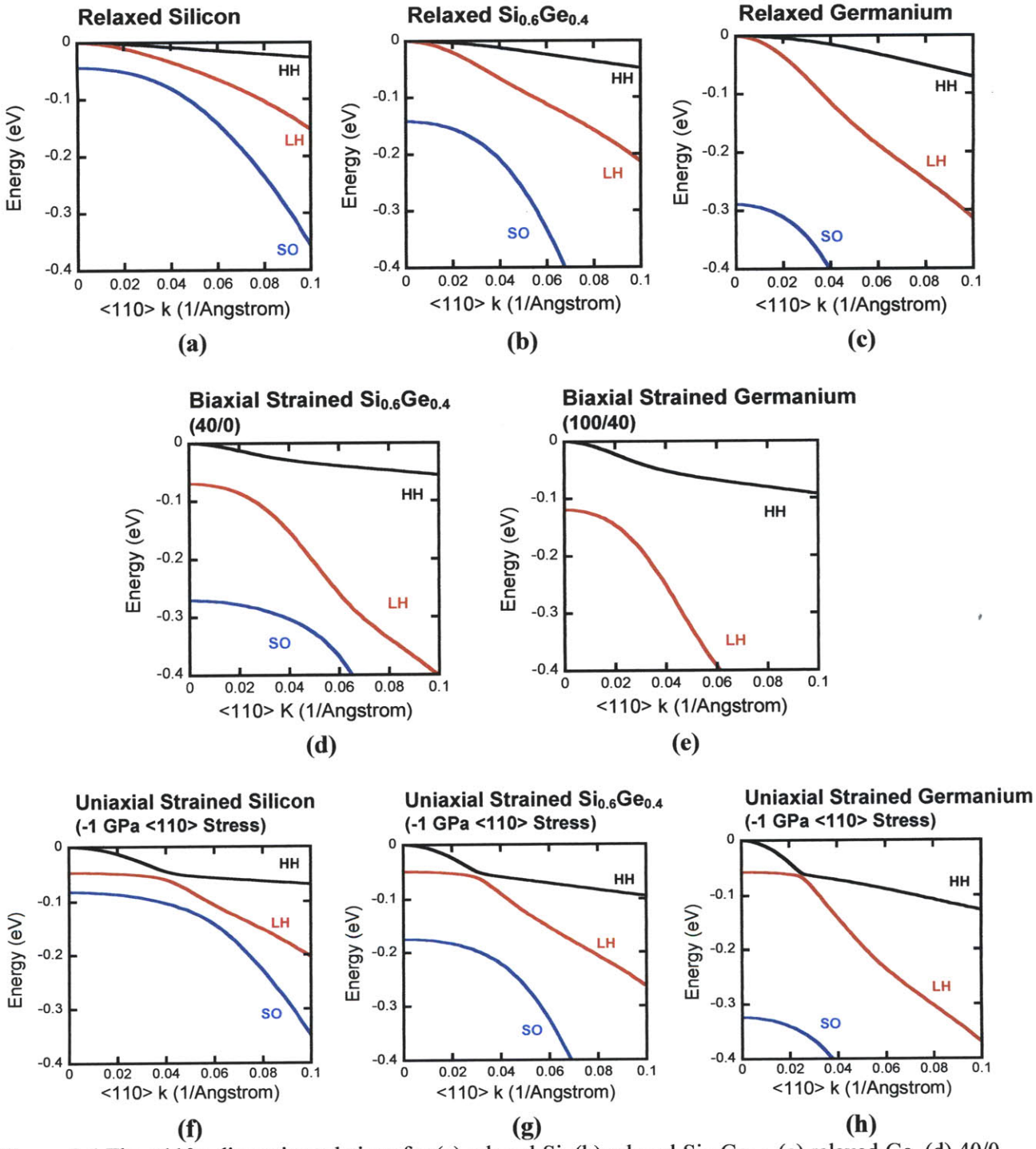


Figure 2.4 The <110> dispersion relations for (a) relaxed-Si, (b) relaxed-$Si_{0.6}Ge_{0.4}$, (c) relaxed-Ge, (d) 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$, and (e) 100/40 biaxial compressive strained-Ge are also plotted. The <110> dispersion relations for uniaxial strained (f) Si, (g) $Si_{0.6}Ge_{0.4}$, and (h) Ge, each with -1GPa of applied <110> stress are also plotted. The dispersion relation calculations were performed in nextnano3 [30].

2.3 Impact of strain on the valence band structure

Strain modifies the lattice spacing in a crystal, changing the periodic potential of the lattice, and thus altering the valence band structure. The impact of strain on the valence band structure depends heavily on the type of strain applied to the lattice. Biaxial and uniaxial strain each impact the valence band structure differently.

The Energy-momentum vector (E-k) relations can be calculated for Si, SiGe, and Ge using the 6x6 k·p method [30][36-38]. The kp method utilizes material parameters and knowledge of the strain distribution in the material to calculate the shape of the valence bands. The unstrained valence band structure of Si, SiGe, and Ge are similar in that the heavy hole (HH) and light hole (LH) bands are degenerate at the gamma point, while the split off (SO) band is separated in energy. In Figure 2.4 (a), (b), and (c) the valence band dispersion relations are plotted along the <110> direction on (100) oriented relaxed Si, $Si_{0.6}Ge_{0.4}$, and Ge. In this analysis and work we examine the <110> transport direction since this is the conventional orientation in state of the art MOSFETs. Alternative transport directions have been studied as a means to improving carrier transport relative to the <110> transport direction in relaxed Si [31-35].

The addition of biaxial strain to SiGe and Ge strongly impacts the shape and spacing between the bands [26][39-45]. In Figure 2.4 (d) and (e) the E-k dispersion relation for 40/0 biaxial compressive strained $Si_{0.6}Ge_{0.4}$ and 100/40 biaxial strained Ge are plotted. The addition of biaxial compressive strain warps and separates the HH, LH, and SO bands. Biaxial compressive strain in Si cannot be introduced via pseudomorphic growth on SiGe and thus is not plotted. In Figure 2.4 (f), (g), and (h) the E-k dispersion relations for uniaxial strained Si, $Si_{0.6}Ge_{0.4}$, and Ge with -1 GPa of uniaxial compressive stress applied along the <110> direction are plotted respectively. Uniaxial

strain also warps and separates the valence bands. By comparing uniaxial and biaxial strain we can see that biaxial strain is more effective at separating the bands in energy while uniaxial strain is more effective at warping the bands. In the next section we will see how the strain induced band splitting and warping of the valence bands impact hole transport.

2.4 Carrier transport in strained Si, SiGe, and Ge

The strain induced valence band changes discussed in the previous section have a significant impact on the carrier transport properties of Si, SiGe, and Ge. To develop an understanding of how strain impacts hole transport we begin by introducing the Drude model for carrier mobility [46], μ, which is given by

$$\mu = \frac{q\tau}{m^*} \qquad \text{Equation 2.3}$$

where τ is the relaxation time and m* is the carrier effective mass. From equation 2.3 we see that the effective mobility is strongly influenced by changes in the effective mass and relaxation time. The carrier effective mass is given by

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k^2} \qquad \text{Equation 2.4}$$

where ħ is plank's constant and E(k) is the dispersion relation [47]. Equation 2.4 indicates that as the curvature of E(k) increases the carrier effective mass is reduced. Due to the non-parabolic nature of the strained valence bands, extracting the curvature is not straightforward. For example, trying to extract the curvature mass for the heavy hole band at 25 meV in Figure 2.4(d) yields a nonsensical result due to the inflection point present near 25 meV. Equation 2.4 is still useful in that it tells us that as the valence band sharpens in k-space the effective mass should decrease.

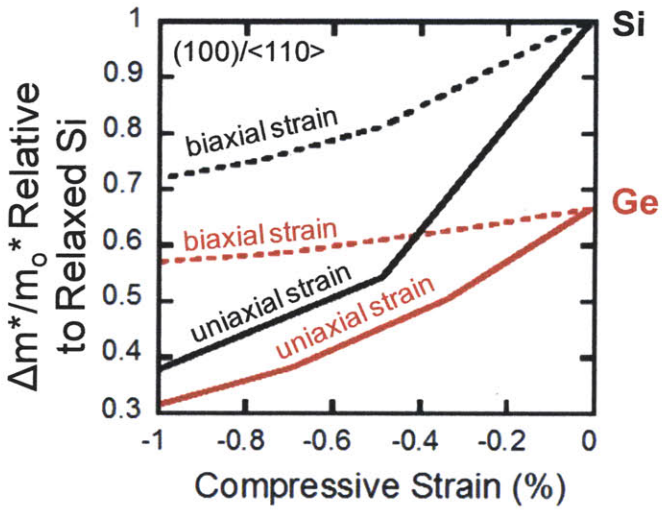


Figure 2.5 The relative change in effective mass for uniaxial and biaxial compressive strained Si and Ge. Results are from M. Uchida et al. in [48].

Comparing the strained valence bands in Figure 2.4 to the relaxed case we see a definitive sharpening of the bands. This would suggest that the hole effective mass in either biaxial or uniaxial compressive strained SiGe or Ge is smaller than its relaxed counterpart. Figure 2.5 presents results from M. Uchida's calculation of the conductivity effective mass in Si and Ge under uniaxial and biaxial compressive strain (i.e. effective mass in the direction of conduction) [48]. Plotted is change in conductivity effective mass relative to relaxed Si for biaxial and uniaxial strained Si and Ge. Indeed we see that as uniaxial and biaxial strain is applied to Si and Ge the hole conductivity effective mass decreases. Also worth nothing is that uniaxial strain has a stronger impact in reducing the effective mass in both Si and Ge than biaxial strain. This suggests that the hole mobility in uniaxial and biaxial strained Si, SiGe, and Ge should be larger than in relaxed Si, SiGe, and Ge, due in part to a reduction in the hole effective mass.

2.4.1 Carrier scattering mechanisms in Si, SiGe, and Ge

As carriers traverses through a semiconductor they undergoes scattering events [47]. These scattering events, along with the effective mass, limit the effective mobility of carriers. Ionized impurity, surface roughness, phonon, and alloy scattering are relevant scattering mechanisms that limit carrier mobility in strained-SiGe MOSFETs. From equation 2.3 we see that the hole mobility is dependent on the momentum relaxation time, τ, or scattering rate, $1/\tau$. The scattering mechanisms mentioned above occur in parallel and therefore add as such. The cumulative scattering rate as given by Matheissen's rule is

$$\frac{1}{\tau} = \frac{1}{\tau_{IM}} + \frac{1}{\tau_{SR}} + \frac{1}{\tau_{PH}} + \frac{1}{\tau_{AL}} + \frac{1}{\tau_{TF}} \qquad \text{Equation 2.5}$$

where τ_{IM} is the relaxation time due to ionized impurity scattering, τ_{SR} is the relaxation time due to surface roughness scattering, τ_{PH} is the relaxation time due to phonon scattering, τ_{AL} is the relaxation time due to alloy scattering, and τ_{TF} is the relaxation time due to thickness fluctuation scattering. A reduction in phonon scattering is in part the reason that strained Si, SiGe, and Ge exhibit a mobility enhancement relative to their unstrained counterparts. Some of the scattering mechanisms mentioned above do not play as dominant a role as others in limiting the mobility in strained Si, SiGe, and Ge.

2.4.2 Ionized impurity scattering

For ionized impurity scattering, carriers scatter when they encounter the electric field of an ionized impurity in the lattice [36][47]. This scattering mechanism usually dominates when the mobile charge density is small and/or the concentration of impurity atoms is in the moderate to high range. When the carrier density is low, the electric field emanating from the ionized impurity

isn't adequately screened. In this case the mobile charge interacts with the coulombic potential of the ionized impurity and is typically deflected through small angles. When the mobile charge concentration increases and/or the ionized impurity concentration is reduced, the field emanating from the ionized impurities is screened and scattering via this mechanism is suppressed. In this work the devices fabricated have a near intrinsic charge concentration (i.e. negligible impurity levels) and the transport metrics are extracted at moderate inversion charge densities, therefore ionized impurity scattering due to channel impurities isn't believed to play a large role in limiting the carrier mobility.

2.4.3 Surface roughness scattering

Surface roughness scattering stems from minute variations in the position of the oxide/semiconductor interface in a MOSFET [49-50]. Ideally the semiconductor/oxide interface would be an abrupt boundary, but in actuality the position of the interface varies randomly due to roughness present at the boundary. This roughness results in variations in the surface potential, which is given by

$$V[z+\Delta r]-V(z)=\frac{V[z+\Delta_m]-V(z)}{\Delta_m}\Delta(r) \qquad \text{Equation 2.6}$$

where V(z) is the surface potential in the confinement direction z, Δ_m is the root mean square (RMS) roughness of the interface fluctuation $\Delta(r)$. The perturbation Hamiltonian or scattering potential is

$$H_{SR}(z,r)=-\frac{q\Delta(r)\Delta V_m(z)}{\Delta_m} \qquad \text{Equation 2.7}$$

where $\Delta V_m(z)$ is the surface potential variation due to the RMS roughness, given by

$$\Delta V_m(z) = V[z + \Delta_m] - V(z) \qquad \text{Equation 2.8}$$

The scattering potential is then related to surface roughness scattering through the matrix element M_{fi} by

$$\frac{1}{\tau_{SR}} \propto \left|M_{fi}\right|^2 = \left|\psi_i(z) H_{SR} \psi_f(z)\right|^2 \qquad \text{Equation 2.9}$$

where Ψ_i and Ψ_f are the initial and final envelope function respectively. As the surface potential and the surface roughness increase so does the perturbation Hamiltonian in equation 2.7. Examining equation 2.9 we can see that an increase in the perturbation Hamiltonian translates into a higher surface roughness scattering rate. The higher surface potential in a MOSFET is induced by a large vertical field. The high field at the surface bends the valence band strongly and attracts carriers to the interface resulting in a large surface carrier concentration. The band bending also confines carriers close to the interface where they more readily scatter due to variations in the surface potential. At low vertical fields or mobile charge densities the carriers aren't strongly confined to the interface and therefore are not heavily influenced by variations in the surface potential. From this we see that surface roughness scattering is strongly dependent on the vertical field strength (i.e. carrier concentration). In this work of the analysis is conducted in the moderate carrier concentration regime where surface roughness scattering plays a small role in limiting the carrier mobility. As we will also see in the following section, the strained Si and Ge devices fabricated or examined in this work are buried channel devices confined by potential of a Si layer that exists between the oxide and strained SiGe or Ge channel. Therefore carriers in these devices aren't influenced by the roughness at the oxide/silicon interface, but instead at the Si/SiGe hetero-interface.

2.4.4 Thickness fluctuation scattering

Thickness fluctuation scattering becomes a significant scattering mechanism when the device layer is scaled to very small dimensions (i.e. < 5 nm). When this occurs, slight variations in the device layer thickness (i.e. variations on the order of a few atomic planes) constitute a significant portion of the total film thickness. These fluctuations result in significant variations in the subband energy levels which carriers occupy in the valence band. Following the analysis from Sakaki [55], the square potential well n^{th} subband energy is given by

$$E_n = \frac{\hbar^2 \pi^2}{2 m_z T^2} n^2 \qquad \text{Equation 2.10}$$

where m_z and T are respectively, the effective mass perpendicular to the transport plane and the thickness of the potential well. In equation 2.10 for small dimensions even a small variation in the well thickness can result in a significant change in the subband energy. When the fluctuation in valence band energy exceeds the thermal energy of the inversion charge carriers, thickness fluctuation induced scattering begins to become a significant scattering mechanism that drastically limits the mobility. The mobility dependence on thickness is rooted in the potential variations induced by the thickness fluctuation and is given by

$$\Delta V = \frac{\partial E}{\partial T_{Si}} \Delta \qquad \text{Equation 2.11}$$

where Δ is the height of the fluctuation in the Si. This potential variation translates into a carrier scattering mechanism with a mobility dependence of

$$\mu \propto \left(\frac{1}{\Delta V} \right)^2 \propto T^6 \qquad \text{Equation 2.12}$$

At low temperatures phonon scattering is suppressed and the mobility in ultrathin-body (UTB) MOSFETs is predominantly limited by the thickness fluctuations induced scattering. Previous experimental work on UTB SOI and GaAs/AlAs quantum wells shows that the mobility at low temperatures follows the T^6 dependence that was theoretically predicted, where T is the film thickness [51-55]. In the context of the thin-body strained SiGe and Ge devices the carriers are confined to a thin epitaxial layer. Fluctuations in the strained SiGe and Ge film thickness can also lead to changes in the subband energies if the film is thin enough. Films less than 5nm have been shown to be susceptible to this form of scattering [51][53-54]. In this work, the devices examined have channel thicknesses greater than 5 nm, typically about 7nm, therefore thickness fluctuation is believed to have a small impact on the carrier mobility.

2.4.5 Phonon scattering

Perhaps the most dominant scattering mechanism in strained Si, SiGe, and Ge MOSFETs is scattering due to acoustic and optical phonons. Let us examine this scattering mechanism using the description provided by Lundstrom [47]. When carriers enter the MOSFET channel they can be described as having a momentum p_0. As these carriers are swept across the channel they undergo scattering events. The effective scattering rate, $\frac{1}{\tau(p_0)}$, is a culmination of scattering rates between p_0 and other states p'. The scattering rates for parallel processes can be calculated as follows

$$\frac{1}{\tau(p_0)} = \sum_{p'} S(p_0, p') \qquad \text{Equation 2.13}$$

where the transition rates, $S(p_0,p')$, are determined by evaluating Fermi's Golden Rule. The initial step in evaluating the transition rate is to determine the matrix element of the scattering potential

$$H_{p'p} = \int_{-\infty}^{\infty} \varphi_{p'}^{*} U_S \varphi_p d^3 r \qquad \text{Equation 2.14}$$

where U_s is the scattering potential. The transition rate can now be determined by

$$S(p,p') = \frac{2\pi}{\hbar} \left| H_{p,p'} \right|^2 \delta(E(p') - E(p) - \Delta E) \qquad \text{Equation 2.15}$$

where ΔE is the change in energy that results from the scattering event.

Optical phonon scattering is strongly suppressed in strained SiGe and strained Ge. The strain induced valence band splitting present in strain SiGe separates the bands beyond the optical phonon energy resulting in no final state for carriers to scatter into [56-60]. The optical phonon energy in Si is 61 meV and in Ge is 37 meV [75]. Strain induced subband splitting strongly suppresses the inter-subband transitions supported by optical phonon scattering.

For carriers in strained SiGe or strained Ge MOSFETs, the dominant phonon scattering mechanism is acoustic phonon scattering which is given by

$$\frac{1}{\tau_{fi}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_1} \frac{1}{W_{fi}} g_{2Df}(E) \qquad \text{Equation 2.16}$$

where D_A, $1/W_{fi}$, and $g_{2Df}(E)$ are the acoustic deformation potential, the effective width of the envelope function, and the two dimensional density of states, respectively. Acoustic phonon energies are small, which tends to support intra-subband scattering transitions. If we recall the bulk dispersion relations we examined in Figure 2.4, we see a substantial separation in the HH and LH bands as either biaxial or uniaxial strain are applied to $Si_{0.6}Ge_{0.4}$ and Ge. The suppression of optical phonon scattering in strained SiGe and strained Ge is a result of this band separation and is one of the reasons why these materials exhibit a mobility enhancement relative to their relaxed

counterparts. While the results shown in Figure 2.4 are for bulk materials, it has been show that in the context of the hole inversion layer, strain also results in a significant level of HH, LH, and SO subband separation [56-58][61-62].

2.4.6 Alloy scattering

In some semiconductor alloys (e.g. $Si_{1-x}Ge_x$) the localized distribution of constituent atoms varies randomly. While the macroscopic composition of the alloy may not vary noticeably from one region of the crystal to the next the composition on the local or atomic scales can be quite large. These fluctuations result in spatial variations in the crystal potential, which gives rise to carrier scattering. Alloy scattering has been studied extensively in $Si_{1-x}Ge_x$ and in III-V alloys where the atomic distribution of constituent atoms varies randomly [108-112]. Theoretical calculations indicate that alloy scattering is a prominent scattering mechanism at low temperatures where phonon scattering is reduced [108-112]. In strained SiGe, alloy scattering should be a prominent scattering mechanism since phonon scattering is strongly suppressed due to strain induced band splitting. According to G. Bastard [113], the alloy scattering rate can be modeled as

$$\frac{1}{\tau_{AL}} = \frac{m_{xy}\Omega_o V_{alloy}^2 x(1-x)}{\hbar^3}\left(\frac{3b}{16}\right) \qquad \text{Equation 2.17a}$$

where the variational parameter b is given by

$$b = \left(\frac{33 m_z e^2 n}{8\varepsilon\hbar^2}\right)^{1/3} \qquad \text{Equation 2.17b}$$

and where m_{xy} is the in-plane carrier effective mass, Ω_o is the atomic volume, V_{alloy} is the alloy disorder potential, x is the alloy composition in a binary semiconductor, m_z is the quantization mass, and n is the two dimensional carrier concentration. The theoretical alloy scattering rate has a

dependence on the carrier concentration, where the alloy limited mobility decreases like $n^{1/3}$ when n increases. At high carrier concentrations the carrier wave function becomes more concentrated and thus more sensitive to the alloy fluctuations. The theoretical alloy scattering rate introduced above is also strongly dependent on the scattering potential used. This parameter is typically treated as an empirical or adjustable parameter used to obtain good quantitative agreement between calculated scattering rates and experimental carrier mobility. The theoretical alloy scattering rate is also strongly dependent on the in-plane carrier effective mass. Strain induced warping of the valence band which changes the carrier effective mass is also expected to influence the alloy scattering rate. Due to the strain induced suppression of phonon scattering in strained SiGe and the sensitivity of alloy scattering to changes in the in-plane effective mass, alloy scattering is considered a relevant scattering mechanism in strained SiGe.

2.5 Biaxial Strained Si, SiGe, and Ge MOSFETs

Carrier transport in biaxial strained Si, SiGe, and Ge MOSFETs has been studied extensively over the past few decades [7, 9, 10, 17, 18, 20-22, 24, 26, 63]. In Figure 2.6 two common device structures utilized in studying the electron and hole mobility characteristics of strained Si, SiGe, and Ge MOSFETs are depicted. Below each device diagram the band structure though the channel is provided. In the strained Si n-MOSFET the strained Si surface layer has the lowest conduction band potential; therefore carriers are readily confined in this layer. In the strained SiGe and Ge p-MOSFETs a potential well exists in the valence band which confines carriers in the high mobility strained SiGe and Ge layers. It is only at high vertical fields (i.e. high inversion charge densities) that carriers overcome the valence band offset to occupy the Si cap. The reason that a Si cap is incorporated into the p-MOSFETs is that the formation of a quality dielectric on strained SiGe and Ge is very difficult. There exists a large community of researchers

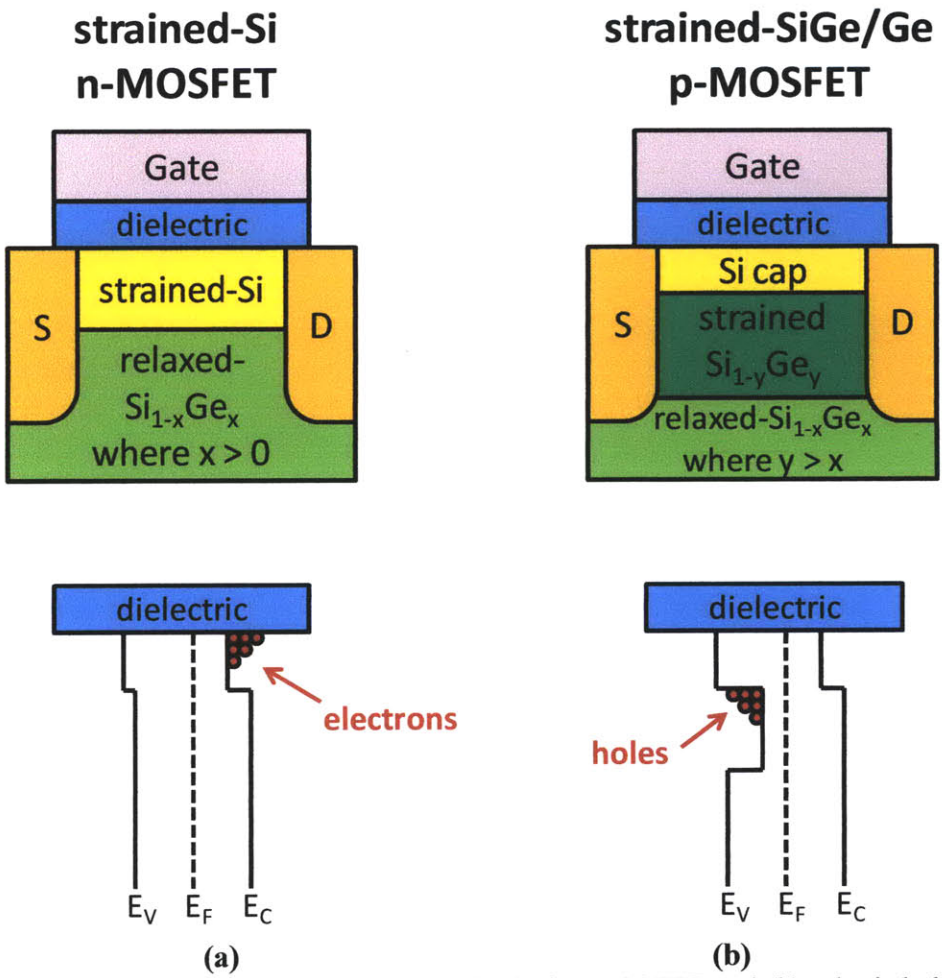


Figure 2.6 (a) A surface channel biaxial tensile strained Si n-MOSFET and (b) a buried channel biaxial compressive strained-SiGe channel p-MOSFET. The band structures are also depicted to show that band alignments in strained-Si/strained-SiGe heterostructures. The conduction band offset in (a) confines electrons in the strained-Si layer while the valence band offset in (b) confines hole in the strained-SiGe buried channel.

investigating the formation of high quality gate dielectrics on SiGe and Ge [64-68]. On the other hand, Si readily forms a high quality dielectric interface with SiO_2. The ease with which this dielectric is formed and its quality are the motivation for using a Si cap or Si passivation layer in these device structures. The presence of a Si cap though increases the effective oxide thickness (EOT) of the gate dielectric, since it further segregates carriers away from the dielectric interface. This is viewed as a parasitic effect in short channel devices where a thin gate dielectric is critical in

the ability of the gate to maintain good electrostatic control over the channel charge [69][70]. In long channel MOSFETs the Si cap has a negligible impact on electrostatic performance.

2.5.1 MOSFET mobility extraction

The carrier effective mobility has a strong bearing on the electrical performance of long channel MOSFETs. The low field effective mobility of a long channel MOSFET can be extracted in a very straightforward fashion from the linear transfer characteristics. The drain current of a long channel MOSFET in the linear regime is given by

$$I_{DS} = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_t - \frac{V_{DS}}{2}\right)V_{DS} \qquad \text{Equation 2.17a}$$

and in the saturation regime is given by

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{GS} - V_t)^2 \qquad \text{Equation 2.17b}$$

where W is the device width, L is the device length, μ is the effective carrier mobility, C_{ox} is the gate oxide capacitance, V_{GS} is the gate-to-source voltage, V_t is the threshold voltage, and V_{DS} is the drain-to-source voltage. The effective carrier mobility is extracted from the MOSFET current characteristics in the linear regime as

$$\mu = \frac{L}{W}\frac{I_{DS}}{V_{DS}Q_{inv}} \qquad \text{Equation 2.18}$$

where the inversion charge density Q_{inv} is given by

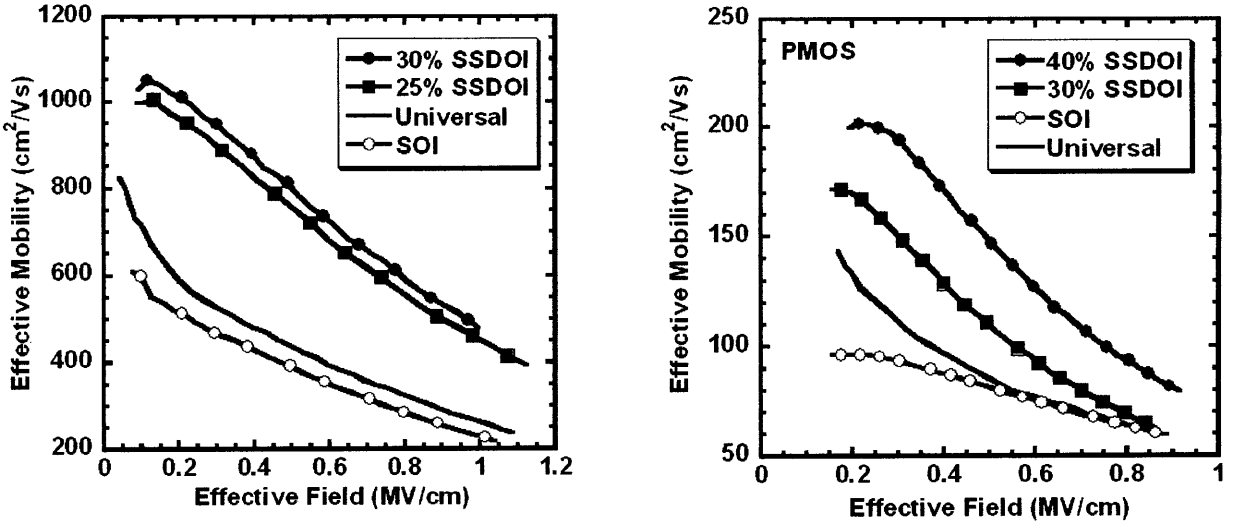
$$Q_{inv} = C_{ox}\left(V_{GS} - V_t - \frac{V_{DS}}{2}\right) = \int C_{GC}\,dV_{GS} \qquad \text{Equation 2.19}$$

where C_{GC} is the gate-to-channel capacitance. The carrier mobility is extracted from the MOSFET transfer characteristics (I_{DS} vs. V_{GS}) and gate capacitance characteristics (C_{GC} vs. V_{GS}). The

transfer characteristics are typically measured in the linear regime, when $|V_{DS}| < 50$ mV. Mobility extraction can become problematic when the extrinsic resistance is high, as a significant portion of the applied V_{DS} drops across the external resistance. The lower intrinsic V_{DS} results in an over estimation of the carrier mobility. A few solutions have been devised. One solution involves fabricating devices which enable electrical measurements independent of the extrinsic resistance [71]. Another involves using more sophisticated measurement techniques to cancel out the effects of the extrinsic resistance [72-74]. These methods will be discussed in more detail in subsequent chapters where they will be utilized to extract carrier mobility.

2.5.2 Electron mobility in strained Si n-MOSFETs

Electron and hole mobility in strained Si, SiGe, and Ge MOSFETs has been studied quite extensively. Tensile strain in Si is quite beneficial for improving electron mobility [7,53,69]. With applied strain the symmetry between the Δ_2-valleys and the Δ_4-valleys in the Si conduction band is broken and the subbands corresponding to each valley are separated in energy. For Si that is pseudomorphic to relaxed-$Si_{1-x}Ge_x$ the strain induced subband splitting increases by 67 meV for every 10% of Ge in the relaxed $Si_{1-x}Ge_x$ substrate [75,76]. As the subbands are separated in energy, inter-valley phonon scattering is suppressed. When the valley degeneracy is lifted carriers preferentially occupy the lower energy Δ_2-valley subbands, which have a lower in-plane effective mass compared to the Δ_4-valley subbands. The lower effective mass and reduction in inter-valley scattering result in an increase in electron mobility. This mobility enhancement saturates about 2x relative to relaxed Si with increasing strain. The enhancement saturation occurs when the majority of electrons occupy the low mass Δ_2 valley ellipsoids and strain induced subband splitting all but eliminates scattering between the Δ_2 and Δ_4 valley subbands [77]. In Figure 2.6 (a) the electron mobility for relaxed Si and biaxial tensile strained Si are plotted. The 25% and 30% SSDOI



(a) (b)

Figure 2.7 (a) Electron effective mobility in 25% (00/25) and 30% (00/30) SSDOI, SOI, and the universal electron mobility in Si. A ~2x mobility enhancement is observed in biaxial tensile strained-Si compared to unstrained Si. (b) Hole effective mobility in 40% (00/40) and 30% (00/30) SSDOI, SOI, and the universal hole mobility in Si. A mobility enhancement can be seen for low effective fields, but as the field strength is increased the enhancement is reduced. Results from I. Åberg [69].

substrates are biaxial tensile strained 0/25 and 0/30 Si substrates respectively. Strained Si directly on insulator (SSDOI) is an SOI-like substrate in which the strained Si film is transferred onto an oxidized handle wafer and the underlying $Si_{1-y}Ge_y$ layer is removed [78-80]. The structure and fabrication of SSDOI will be discussed in greater detail in the next chapter. The electron and hole mobilities on SSDOI substrates have been utilized extensively by I. Åberg [53, 69].

2.5.3 Hole mobility in strained Si p-MOSFETs

The hole mobility characteristics of biaxial tensile strained Si have also been studied. Recall that in strained-Si/strained-$Si_{1-y}Ge_y$ heterostructures a band offset exists between the Si and $Si_{1-y}Ge_y$ layers, which results in holes preferentially occupying the strained $Si_{1-y}Ge_y$ buried layer at low vertical effective fields [17, 26, 40, 69, 70]. In SSDOI, holes can only reside in the tensile strained Si film [53, 69]. This makes SSDOI a very useful platform for studying the hole mobility

characteristics of biaxial tensile strained Si. The hole mobility characteristics measured by I. Åberg for biaxial tensile strained 30% and 40% SSDOI (i.e. 0/30 and 0/40 strained Si respectively, as discussed in section 2.2) are presented in Figure 2.7. The hole mobility in tensile strained Si is indeed enhanced relative to relaxed SOI and the Si hole universal mobility, although this enhancement degrades at higher vertical fields. In biaxial tensile strained Si the LH and HH band degeneracy is lifted and the bands are warped. For Si strained to relaxed $Si_{0.7}Ge_{0.3}$ (i.e. 0/30) the LH band is the lowest energy band and is separated from the HH band by 128 meV [69]. Lifting the band degeneracy reduces phonon scattering, and warping of the valence bands causes a reduction in effective mass. These two modulations in the valence band result in a larger hole mobility. However, the hole mobility enhancement is reduced at high vertical fields where the separation between the LH and HH bands is reversed due to increased quantization of carriers in the inversion layer [59, 60, 69]. This causes the phonon scattering to increase and thus reduces the hole mobility. Despite the improved hole mobility in biaxial tensile strained Si, the hole mobility still lags far behind the electron mobility.

2.5.4 Hole mobility in strained SiGe and Ge p-MOSFETs

Fundamentally the hole mobility has lagged behind the electron mobility, but compressive strain in SiGe and Ge has been shown to dramatically improve the hole mobility, bringing it to values comparable to the electron mobility in relaxed Si [17, 18, 26, 63, 70]. As mentioned in the previous section the hole mobility enhancement derived from biaxial compressive strain in SiGe and Ge stems from a reduction in inter-band optical phonon scattering and a reduction in the hole effective mass. In Figure 2.8 the hole mobility for biaxial compressive strained SiGe and Ge are plotted. As the Ge fraction of the channel (Y) increases, the hole mobility steadily rises. For a 100/50 strained Ge p-MOSFET the hole mobility even exceeds the strained Si electron mobility in

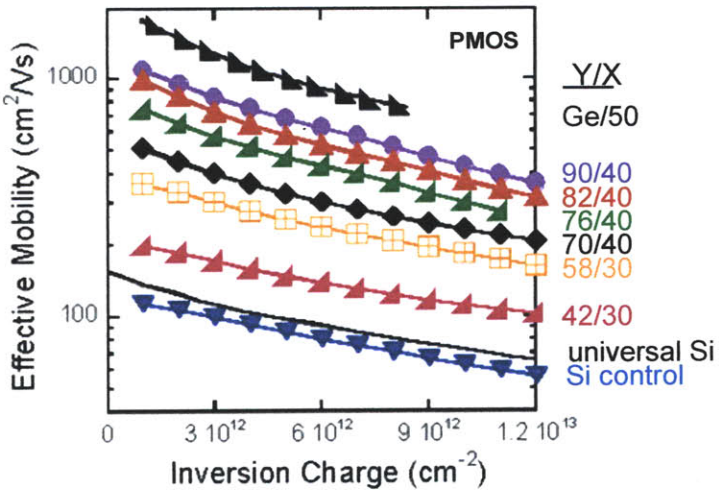


Figure 2.8 Effective hole mobility for biaxial compressive strained-$Si_{1-y}Ge_y$ pseudomorphic to relaxed $Si_{1-x}Ge_x$. Where Y and X are the channel and substrate Ge percentages respectively. As the Ge percentage in the channel increases and biaxial compressive strain is introduced the hole effective mobility increases by over a factor of 10x. Results from C. Ni Chléirigh [26].

Figure 2.7 (a). As mentioned in the introduction, future CMOS technology generations may require the use of high mobility channel materials to realize current drive improvements in deeply scaled devices. The long channel mobility results just presented are impressive enough to warrant examining the transport gains these materials can provide in scaled MOSFETs.

2.6 Carrier transport in nano-scale MOSFETs

As aggressive scaling of CMOS continues the gate length will reach a point where it is comparable to the mean free path of carriers in the channel. These devices are said to be operating in the quasi-ballistic transport regime. Fully ballistic transport occurs when carriers traverse from source to drain without scattering in the channel. According to Lundstrom's scattering theory [81][82], the current of a MOSFET operating in the ballistic transport regime is given by

$$I_D = WQ_o\upsilon_\theta \qquad \text{Equation 2.20}$$

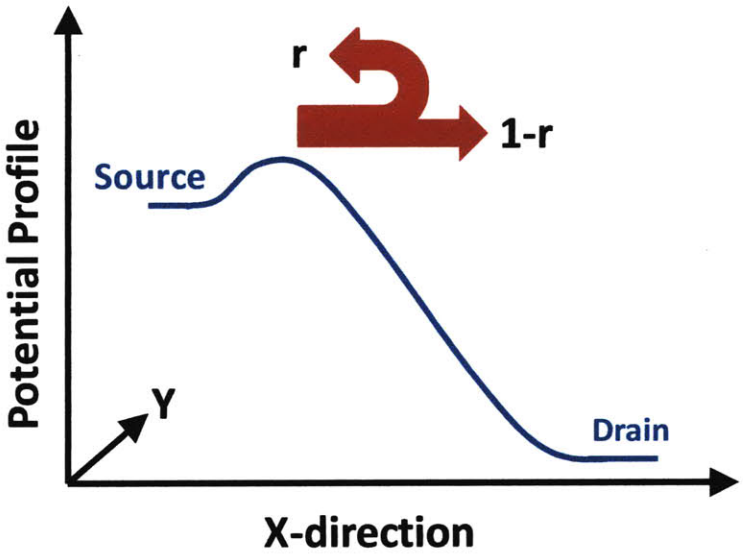


Figure 2.9 A depiction of the potential profile across the channel from source to drain in a MOSFET. In the quasi-ballistic regime of transport, a fraction of the carriers in the channel are reflected back into the source.

where I_D is the transistor drain current, W is the device width, Q_o is the inversion charge density at the top of the source barrier, and υ_θ is the ballistic velocity of carriers in the channel. The charge in the saturation regime is given by $Q_o = C_{inv}(V_{GS}-V_t)$, where C_{inv} is the inversion capacitance and V_t is the saturation threshold voltage. In the non-degenerate limit (i.e. $(E_f-\varepsilon)/k_BT < 0$) the electron and hole ballistic velocity reduces to the thermal velocity

$$\upsilon_\theta = \sqrt{\frac{2k_BT}{\pi m_x}} \qquad \text{Equation 2.21}$$

and in the degenerate limit (i.e. $(E_f-\varepsilon)/k_BT >> 1$) the electron and hole ballistic velocity is given by

$$\upsilon_\theta = \frac{4\hbar}{3} m_x^{-3/4} m_y^{-1/4} \sqrt{N_{inv}} \qquad \text{Equation 2.22}$$

where E_f is the Fermi energy, ε is the minimum band energy, k_B is the Boltzmann constant, T is the temperature, m_x is the longitudinal in-plane carrier effective mass, m_y is the transverse in-plane carrier effective mass, and N_{inv} is the inversion charge density [83]. In realistic devices a portion of the carriers entering the channel are reflected back into the source, as shown in Figure 2.9. The effective velocity of carriers at the source barrier, called the virtual source velocity, is given by

$$\upsilon_{x0} = B\upsilon_\theta = \frac{1-r}{1+r}\upsilon_\theta \qquad \text{Equation 2.23}$$

where B is the ballistic efficiency (i.e. fraction of carriers not backscattered into the source) and r is the reflection coefficient [81, 82]. The reflection coefficient depends on the ratio between the backscattering mean free path of carriers, λ, which is the average distance a carrier travels before it is back scattered into the source and the critical length for scattering, l, which is the distance over which the potential drops by kT/q.

$$r = \frac{l}{l+\lambda} \qquad \text{Equation 2.24}$$

The ballistic efficiency is given by

$$B = \frac{\lambda}{\lambda+2l} \qquad \text{Equation 2.25}$$

The current in the quasi-ballistic regime is thus given by

$$I_D = WQ_oB\upsilon_\theta = WQ_o\upsilon_{x0} \qquad \text{Equation 2.26}$$

To increase the drain current in a MOSFET operating in the quasi-ballistic transport regime either the ballistic velocity must increase or the ballistic efficiency must go up. From equation 2.21 and 2.22 we see that the ballistic velocity is strongly dependent on the carrier effective mass. Reductions in the transverse and longitudinal effective mass will increase the ballistic velocity. To

increase the ballistic efficiency one needs to increase the backscattering mean free path. According to Rahman, et al. [84] the backscattering mean free path can be expressed as

$$\lambda = \left(\frac{2\mu}{\upsilon_\theta} \frac{k_B T}{q} \right) \frac{\Im_o(\eta_F)}{\Im_{-1}(\eta_F)} \qquad \text{Equation 2.27}$$

To increase the backscattering mean free path it then becomes necessary to increase the low-field mobility, μ. While the concept of mobility can be brought into question in the quasi-ballistic regime, it can still be extracted at low V_{DS}. The ballistic efficiency is also a function of the critical length of backscattering, l. The critical length of back scattering is dependent on the channel potential profile. Since the channel profile sharpens as the gate length is scaled, the critical length of backscattering decreases as the gate length is reduced. The channel potential profile is also a function of scattering in the channel and results in l being dependent on the carrier mobility [86][87].

To increase the drain current in a MOSFETs operating in the quasi-ballistic transport regime the carrier effective mass must be reduced, the amount of scattering taking place in the channel must decrease, and/or the low-field mobility must be improved. From the previous section we saw that biaxial compressive strained SiGe and Ge offer improvements in each of these areas over relaxed Si. While the results presented in Figure 2.5 suggest that biaxial compressive strain in Si and Ge offers only a mild reduction in the carrier effective mass, the substantial reduction in scattering and resulting rise in low-field mobility warrant examining the velocity characteristics of biaxial compressive strained-SiGe. In Chapter 4 we will examine the velocity characteristics of biaxial compressive strained-SiGe to determine if the impressive mobility gains observed in biaxial strained-SiGe translate to equally large gains in velocity.

2.7 Summary and conclusions

In this chapter we reviewed the transport gains derived from introducing biaxial strain into Si, SiGe, and Ge. In biaxial tensile strained Si both electron and hole mobility enhancements have been observed relative to relaxed Si. Biaxial compressive strain in SiGe and Ge produce substantial hole mobility gains, which in some cases exceed the electron mobility in biaxial tensile strained Si. These improvements in mobility are derived from both reductions in the carrier effective mass and in phonon scattering. While mobility may be an appropriate measure of transport in long channel MOSFETs, in the nano-scale regime of quasi-ballistic transport carrier velocity becomes more relevant. With aggressive scaling of CMOS geometries bringing the gate length closer to the mean free path of a carrier in the channel, we must therefore shift our attention towards velocity. Carrier velocity and mobility are correlated through their dependence on effective mass and scattering. Mobility is therefore not entirely irrelevant in the nano-scale regime, although special attention must be paid to the mechanisms by which the mobility is improved in order to understand the potential velocity gains.

Chapter 3

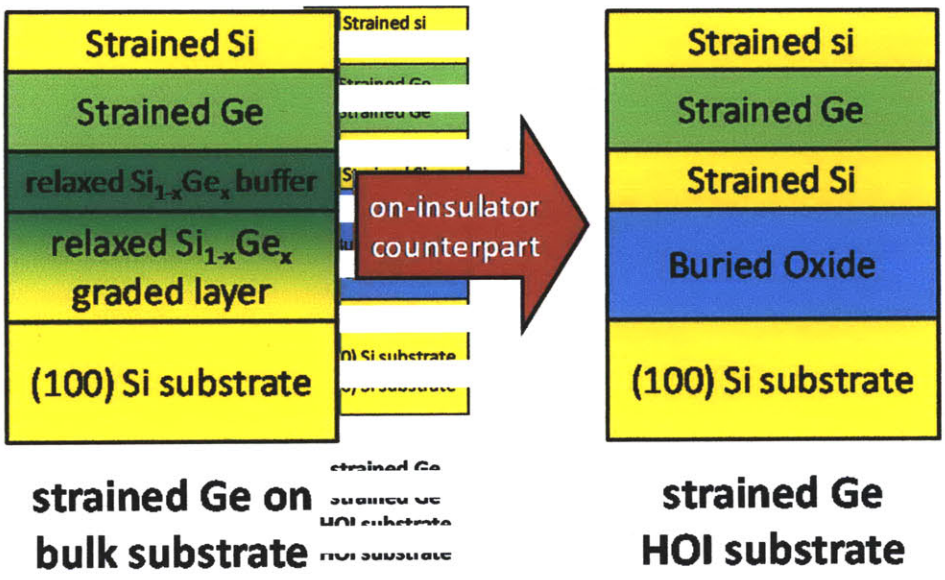
STRAINED-GE HOI

3.1 Introduction

The need to continue transistor performance improvements that are commensurate with geometric scaling motivates the study of high mobility channel materials and the use of ultrathin body metal oxide semiconductor field-effect transistor (MOSFET) architectures. Strained-Si/strained-Ge heterostructure MOSFETs on bulk have been examined previously and show a 10x enhancement in effective hole mobility when the Ge is pseudomorphic to relaxed $Si_{0.5}Ge_{0.5}$ [9, 19, 26]. While strained-SiGe/strained-Si heterostructure-on-insulator substrates have been developed, they've been limited to moderate Ge fractions (i.e. less than 55%) [69, 70, 79]. The significant mobility enhancement observed in the strained-Si/strained-Ge heterostructure provides incentive to explore the fabrication of these materials in ultra-thin body structures. In this chapter, the development of a novel strained-Si/strained-Ge heterostructure on insulator substrate (Ge HOI) will be discussed. A new Ge on strained Si growth method and low temperature bond and etch-back process have been developed to enable the fabrication of these substrates. P-MOSFETs have also been fabricated and the hole mobility characteristics examined.

3.2 Strained-Ge and the thin-body architecture

Bulk MOSFETs require the use of halo, body, and extension implants to help maintain electrostatic integrity in deeply scaled devices. These implants, though, may prove to be detrimental in deeply scaled biaxial compressive stained Ge MOSFETs where they can severely



(a) (b)

Figure 3.1 (a) A bulk biaxial compressive strained Ge (i.e. 100/X) substrate and (b) its on-insulator counterpart the biaxial compressive strained Ge (i.e. 100/X) heterostructure on insulator (HOI) substrate. Ge HOI offers better electrostatic performance in deeply scaled MOSFETs while maintaining the impressive transport characteristics offered by bulk strained Ge. A typical Ge HOI structure consists of 3 nm strained Si cladding layers with a 7nm strained Ge channel.

disrupt the channel strain. As mentioned in the previous chapter, strain induced band splitting and effective mass reductions are the source of the impressive mobility gains provided by biaxial compressive strained-SiGe and strained-Ge. Retaining the channel strain is therefore critical if transport gains are to be seen in deeply scaled devices. The thin-body architecture provides a method for maintaining electrostatic integrity at shorter gate lengths without the need of halo, body, and extension implants [88, 89]. Developing a biaxial compressive strained-Ge on insulator substrate may provide an opportunity to observe the impressive mobility gains of biaxial compressive strained-Ge and maintain good electrostatics in deeply scaled devices.

Figure 3.1 depicts Ge HOI and its bulk counter-part. In strained-Ge HOI, the biaxial compressive strained Ge layer is flanked by two Si passivation layers. As mentioned in the previous chapter, forming a high quality dielectric interface on Ge is not trivial. The native Ge

dielectric interface has a high interface trap density. In this work the strained-Ge layer is flanked by the two Si passivation layers so that high quality SiO_2/Si boundaries can be formed at the critical semiconductor/buried-oxide and semiconductor/gate-oxide interfaces.

3.3 Ge HOI substrate fabrication

Strained Ge HOI substrates are fabricated using the bond and etch back method utilized to make strained SiGe HOI and SSDOI [79, 80, 90]. In this fabrication scheme, the device layers are grown on a series of etch back layers. In Figure 3.1, the strained Ge HOI device layers consist of a strained-Si/strained-Ge/strained-Si tri-layer heterostructure. Ge HOI fabrication therefore requires the epitaxial growth of strained Ge directly on strained Si. Epitaxial growth is essential to ensure that the strained Ge layer is lattice match to the strained Si layer. This helps ensure that the strain in the Si layer is transferred into the Ge layer. Initial attempts to grow Ge on strained Si resulted in very rough Ge films. An epitaxial strained-Ge on strained-Si growth method had to be developed to enable the fabrication of strained-Ge/strained-Si heterostructures on insulator.

3.3.1 Epitaxial growth of strained-Ge on strained-Si

A novel epitaxial growth method was developed to enable the growth of thin smooth strained Ge layers (e.g. 10 nm) directly on strained Si. The growth method involves exposing the strained Si surface to Silane and Germane precursors at 525°C for a short duration (e.g. on the order of 10 sec) prior to strained Ge growth. Experiments show that the $Si_{0.5}Ge_{0.5}$ surface treatment reduces the growth delay period (i.e. incubation period) prior to Ge growth and also minimizes surface roughness.

The reduction in the incubation time was initially observed using the data provided in Figure 3.2 where Secondary Ion Mass Spectrometry (SIMS) provides a profile of the Ge content in

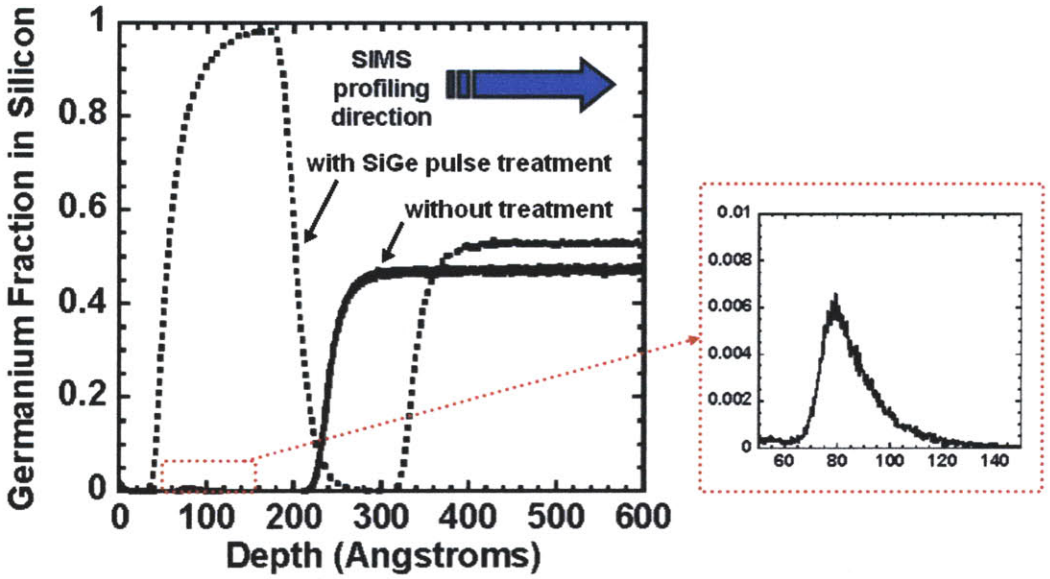


Figure 3.2 SIMS profiles of two samples where Ge growth was conducted by chemical vapor deposition at a temperature of 365°C on a strained Si surface with and without a SiGe interface surface treatment of 10 seconds. The duration of growth for the sample with the pulse was 170 seconds and the duration of Ge growth for the sample without the pulse is 140 seconds. A 15 nm film is realized after 170 seconds of Ge growth with the use of a 10 second SiGe surface treatment. A small peak in the Ge content is observed between the strained Si films in the sample where no SiGe pulse was utilized. This peak may represent the initial stages of Ge growth on the strained Si film after the growth delay period has passed.

two samples. In the first sample (i.e. solid line), Ge growth was attempted on strained Si with a growth time of 140 seconds and without the use of a $Si_{0.5}Ge_{0.5}$ surface treatment. As is evident in the SIMS Ge profile no Ge layer is present in the sample. A small peak in the Ge content is observed between the strained Si films and is magnified in the figure. This peak may represent the initial stages of Ge growth on the strained Si film after the growth delay period has passed. When the strained Si surface is treated with a 10 second SiH_4 and GeH_4 ambient suitable for $Si_{0.5}Ge_{0.5}$ growth at 525°C the growth delay is reduced and a Ge growth time of 170 seconds growth results in a 15 nm thick strained Ge film. Although there are depth resolution constraints associated with

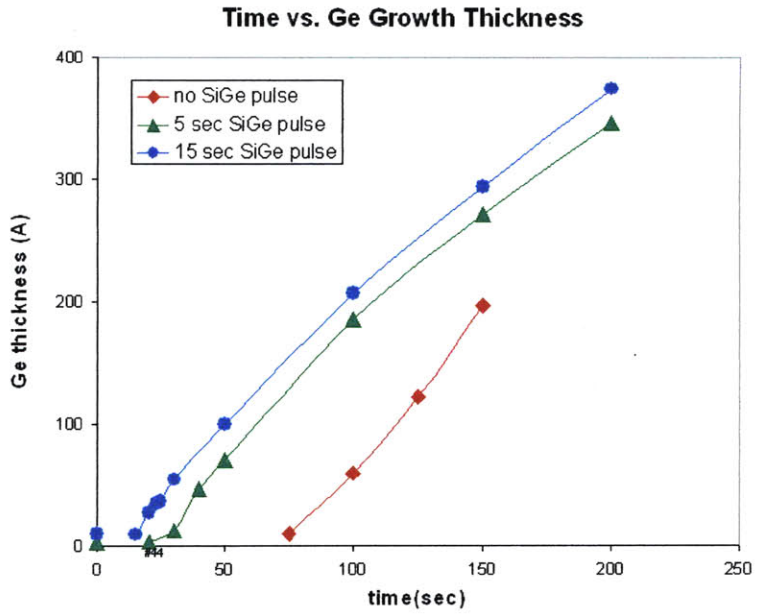


Figure 3.3 Measured Ge thickness versus time for Ge on Si growth utilizing a no SiGe surface treatment, a 10 second treatment, and a 15 second treatment. The Ge growth on the sample with the SiGe pulse treatment occurs almost immediately while growth on the sample without the pulse occurs after an incubation period (approximately 75 seconds in this example). Plot courtesy of M. Kim.

SIMS analysis it is interesting to note that the 10 second $Si_{0.5}Ge_{0.5}$ interface treatment does not produce a noticeable $Si_{0.5}Ge_{0.5}$ interfacial layer between the strained Ge and strained Si films.

Further experiments were also conducted to document the growth dynamics of Ge on relaxed strained Si with and without the use of a $Si_{0.5}Ge_{0.5}$ interfacial treatment. Figure 3.3 is a plot of the Ge film thickness measured by spectroscopic ellipsometry versus Ge film growth time. It reveals a growth delay period (during which little or no Ge film is grown) of about 75 seconds for Ge growth on relaxed Si without the use of a $Si_{0.5}Ge_{0.5}$ pulse surface treatment prior to Ge deposition. With the addition of a 15 second $Si_{0.5}Ge_{0.5}$ pulse the growth delay period is reduced considerably from about 75 to 20 seconds. The reduction in growth delay improves throughput and

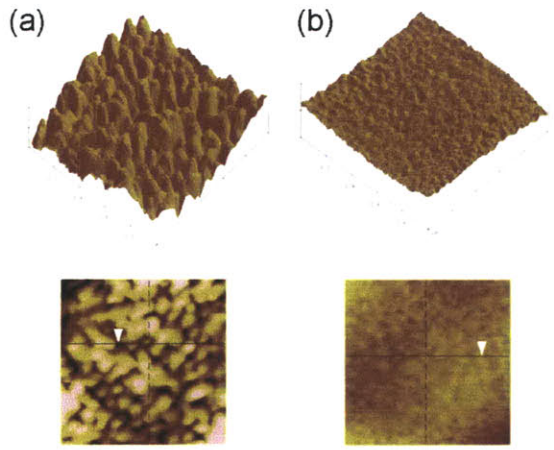


Figure 3.4 1um x 1um AFM scans of Ge films grown on strained Si substrates (a) without a SiGe pulse surface treatment, and (b) with a 10 second SiGe pulse. For (a), RMS is 2.831 nm, with average peak heights of 8nm. With the surface treatment, the Ge film is much smoother, with RMS value of 0.682 nm and peak heights of 1nm, as shown in (b). The thickness of the film in (a) is 12.5 nm and the thickness of the film in (b) is 8.2 nm. Measurements by M. Kim.

improves the reproducibility of the Ge film thickness, which may result from variations in the growth delay period.

Another advantage of this growth method includes an improvement in the surface roughness of the as-grown Ge film. In a planar MOSFET architecture surface roughness of the channel material must be kept to a minimum to prevent surface roughness scattering from becoming a significant mobility limiting mechanism. Roughness was measured by conducting Atomic Force Microscopy (AFM). Figure 3.4 quantifies the improvement in surface roughness with the use of a $Si_{0.5}Ge_{0.5}$ surface treatment when conducting Ge growth on strained Si. With the use of a 10 second $Si_{0.5}Ge_{0.5}$ surface treatment prior to Ge deposition the RMS surface roughness is improved from 2.831 nm to 0.682 nm. The average peak height is also reduced from 8 nm to 1 nm. Additional experiments were conducted to examine the impact of the surface treatment duration on

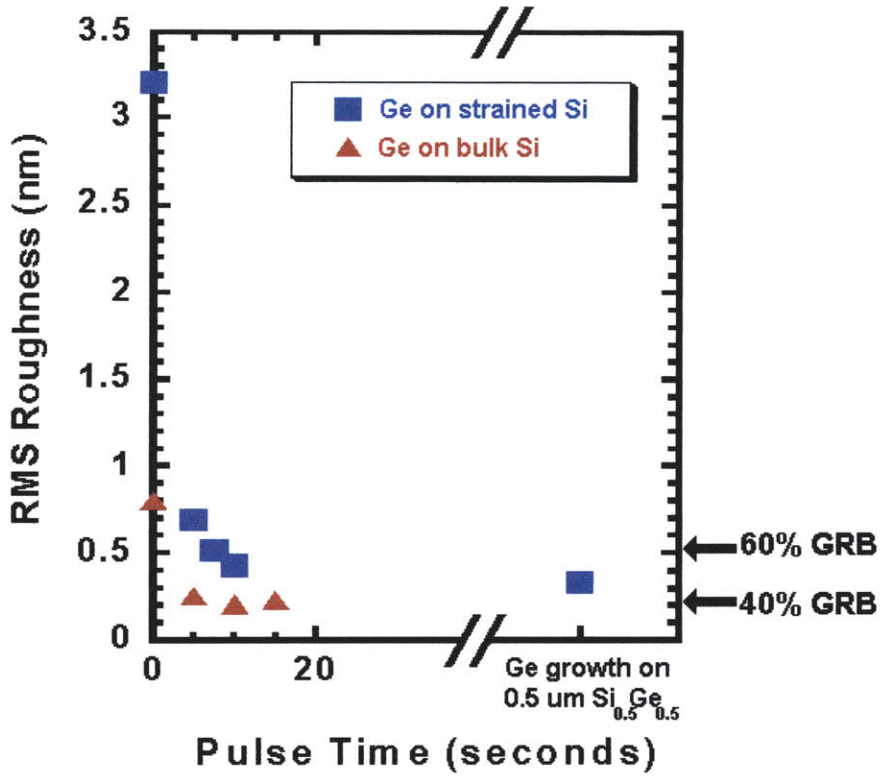


Figure 3.5 RMS surface roughness of the Ge film is plotted for various pulse times. The roughness of a 125 Angstrom-thick Ge film grown on Si strained to $Si_{0.5}Ge_{0.5}$ is plotted with the solid blue squares. The RMS surface roughness of 90 Angstrom-thick Ge films grown on bulk Si is plotted in the solid red triangles. The RMS roughness is observed to decrease as the pulse time is increased. The RMS roughness for $Si_{0.4}Ge_{0.6}$ and $Si_{0.6}Ge_{0.4}$ relaxed graded buffers (GRB) are provided as reference. AFM analysis by M. Kim.

the RMS roughness of the Ge film. This experiment was conducted on relaxed and 0/50 strained Si. In these experiments it was observed that a 12.5 nm thick Ge film grown directly on strained Si without an intermittent $Si_{0.5}Ge_{0.5}$ surface treatment exhibits an RMS roughness of 3.2 nm. Introducing an interfacial 7 second $Si_{0.5}Ge_{0.5}$ treatment prior to this deposition reduces the roughness to 0.5 nm. Similarly, an 8.5 nm Ge film grown on bulk Si without a surface treatment exhibits an RMS roughness of 0.8 nm. When a 5 second $Si_{0.5}Ge_{0.5}$ exposure is utilized prior to this Ge growth the RMS roughness is reduced to 0.25 nm. Figure 3.5 provides similar results for varied treatment durations. The observed trend is that the surface roughness decreases as the surface

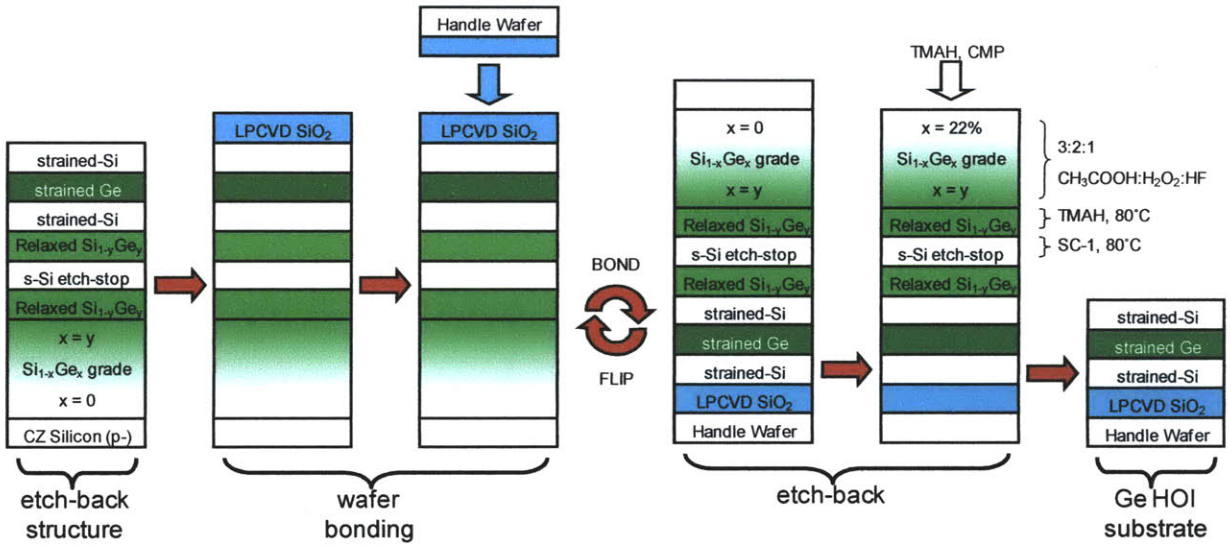


Figure 3.6 Schematic illustrating the strained Ge HOI fabrication process. The bond and etch-back process includes the growing the etch-back structure, wafer bonding, wafer grinding, wafer polishing, substrate etch-back, and the final strained Ge HOI substrate.

treatment duration is increased. It is interesting to note that a 10 second SiGe surface treatment on strained Si results in a level of surface roughness that is comparable to Ge films grown on a 0.5 micron relaxed $Si_{0.5}Ge_{0.5}$ buffer layer. This indicates a saturation in the surface roughness improvement that occurs with increasing treatment duration. In this work a 10 second $Si_{0.5}Ge_{0.5}$ surface treatment at 525°C was adopted to enable the growth of smooth strained-Ge layers on strained Si.

3.3.2 Substrate wafer bonding and etch-back

The Ge HOI fabrication flow is similar to the bond and etch back sequence used to fabricate strained-SiGe HOI and SSDOI [79, 80, 90]. A diagram of the Ge HOI substrate fabrication flow is provided in Figure 3.6. The process begins with the epitaxial growth of an "etch-back structure" on 6" diameter Si substrates in an Applied Materials Epi Centura LPCVD reactor. Before growth wafers are clean with a pre-epi cleaning sequence consisting of: 10 minutes

in 5:1:1 DI:NH_4OH:H_2O_2 (80°C), 15 seconds in 50:1 HF:DI, 15 minutes in 6:1:1 DI:HCl:H_2O_2 (80°C), 15 seconds in 50:1 HF:DI, and a spin-rinse dry (SRD) cycle. The epitaxial structure consists of a SiGe graded layer grown at 900°C, where the relaxed layer content, x, is 0.5. The SiGe grade has a compositional ramp rate of about 10% Ge for every 1 micron. Therefore a $Si_{0.5}Ge_{0.5}$ graded layer will be 5 μm thick. The high growth temperature and graded layer is utilized to reduce the density of threading dislocations in the substrate [91, 92, 93]. The grade is then capped with a $Si_{0.5}Ge_{0.5}$ layer, referred to as a relaxed buffer, of uniform composition matching the maximum composition in the grade. The relaxed buffer sets the level of strain that is present in the strained-Si/strained-Ge device layers and reduces the number of dislocations that reach the surface [94].

An 11 nm strained Si etch-stop layer is subsequently grown on the relaxed buffer. This layer is utilized to controllably approach the strained Si device layer during the etch-back process. Another etch-stop layer is subsequently grown, which consists of a 100 nm relaxed $Si_{1-x}Ge_x$ layer that matches the composition of the relaxed buffer. The ability to selectively etch Si over $Si_{1-x}Ge_x$ and vice-a-versa is the reason that alternating Si and $Si_{1-x}Ge_x$ etch-stop layers are used. This structure is ultimately capped with the strained-Si/strained-Ge tri-layer heterostructure depicted in Figure 3.6. The first strained Si layer is grown to a target thickness of 10 nm, the Ge layer was targeted to be a maximum of 8 nm, and the strained Si layer on the surface of the etch-back structure was targeted to be 6nm thick. All layers in this structure were grown un-doped. The upper limit of the strained layer thickness is set by critical thickness constraints. The Mathews-Blakeslee criterion sets the equilibrium critical thickness limit for strained films [95], though thicker films

are often used without significant dislocation density due to the large metastable thickness range of films grown at low temperatures.

Once the etch-back structures are grown the wafers are prepared for bonding. The etch-back structure is first cleaned using a modified RCA cleaning process, which consists of 10 minutes in 3:1 H_2SO_4:H_2O_2 (110°C), 15 minutes in 6:1:1 DI:HCl:H_2O_2 (80°C), and a SRD cycle. 500 nm of low temperature oxide (LTO) is then deposited on the etch-back structure and densified for 2 hours at 600°C. Chemical mechanical polishing (CMP) of the LTO was then conducted to remove 200 nm of LTO. This reduces the crosshatch-induced roughness on the surface of the oxide. A handle wafer is also prepared by growing a 100 nm thermal oxide on a p- CZ wafer. An oxide to oxide bond is utilized to fuse the two wafers together [96]. The bond process begins by cleaning the wafer pairs using a modified RCA clean, which consists of 10 minutes in 5:1:1 DI:NH_4OH:H_2O_2 (80°C), 15 minutes in 6:1:1 DI:HCl:H_2O_2 (80°C), and a spin-rinse dry (SRD) cycle. It is critical that the oxide surfaces on the etch-back structure and bond handle are not exposed to HF prior to bonding. HF exposure will roughen the oxide surface causing voids to form at the bond interface. After cleaning the wafers the etch-back wafer and bond handle are exposed to an oxygen plasma for 20 seconds. The wafers are then cleaned again in 3:1 H_2SO_4:H_2O_2 (110°C) for 10 minutes to remove any particles that may have settled on the surface. The wafers are then brought into forced contact for 2 minutes and annealed to strengthen the bond. The post bond anneal consists of a 3 hour anneal at 300°C.

Wafer grinding is then conducted to remove most of the Si substrate on the etch-back structure. Wafer grinding is outsourced and the vendor is asked to stop the wafer grinding once the bonded wafer pair reaches a thickness of 775 microns. The starting wafer thickness is typically 675 microns for each wafer. After wafer grinding the vendor then performs CMP to remove 10 microns

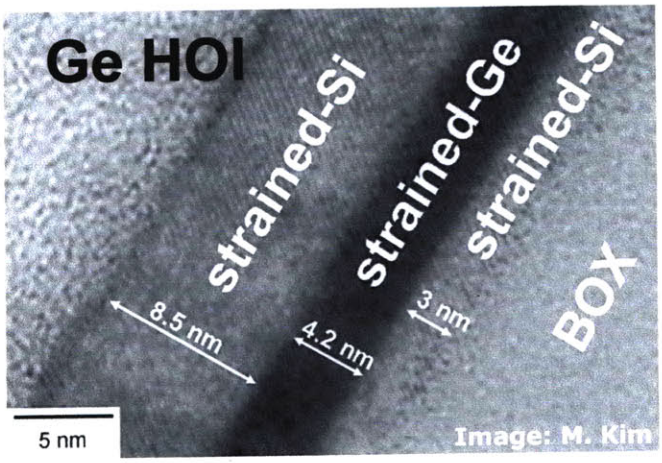


Figure 3.7 A cross-section transmission electron microscopy (XTEM) image of a strained-Si/strained-Ge herterostructure on insulator substrate. The strained Si and strained Ge layers are lattice matched to relaxed $Si_{0.5}Ge_{0.5}$ (i.e. 100/50 strained Ge and 00/50 strained Si). A novel SiGe surface treatment method developed to enable Ge HOI fabrication was utilized to grow the 4.2 nm strained Ge layer directly on strained Si.

of Si from the surface, which removes the scratches introduced during wafer grinding. This bond sequence is illustrated in Figure 3.6. The etch-back process begins once the wafers return from the wafer grind and polishing vendor. Before any further processing is conducted wafers are cleaned using a double piranha clean to remove any surface contamination that may have been introduced during wafer grinding and polishing. The post-grind-back cleaning sequence consists of the following: 10 minutes in 3:1 H_2SO_4:H_2O_2 (110°C) bath 1, 10 minutes in 3:1 H_2SO_4:H_2O_2 (110°C) bath 2, and a SRD cycle. To prevent the bond handle from thinning during the etch-back process a 2 micron thick oxide layer is deposited by PECVD on the bond handle (i.e. wafer backside). The next step in the etch-back process is to chemically etch away the Si substrate until the relaxed SiGe grade is exposed. A bath of Tetra-methyl ammonium hydroxide (TMAH) heated to 80°C is used to etch the Si substrate and stop on $Si_{0.8}Ge_{0.2}$ with a high level of selectivity (i.e. 20:1 selectivity) [97]. Immediately prior to etching Si in TMAH, it is essential to remove the native oxide from the Si

surface. This is done by dipping the bonded wafer pairs into a 50:1 H_2O:Hf bath for 20 seconds. The subsequent TMAH etch typically takes 5 to 6 hours, and as mentioned, stops abruptly on $Si_{0.8}Ge_{0.2}$. The remainder of the SiGe graded layer and SiGe relaxed buffer are removed using a (3:2:1) solution of acetic acid: hydrogen peroxide: hydrofluoric acid [98]. The etch bath must be mixed and allowed to sit for 3 hours so that the etch rate can stabilize. Typically the total volume of the bath is kept small (i.e. 1800 ml). It has been observed that this results in a more consistent etch rate. This etch has a selectivity of 23:1 for $Si_{0.7}Ge_{0.3}$:Si, and etches $Si_{0.7}Ge_{0.3}$ at a rate of ~40 nm/min [69, 79]. The subsequent 11 nm Si etch-stop layer is removed in TMAH heated to 80C after a 1 minute etch. The native oxide on the Si surface is removed prior to TMAH etching by dipping the wafers for 20 seconds in a 50:1 H_2O:HF bath. The remaining SiGe etch stop layer is removed in a 5:1:1 solution of de-ionized water: ammonium hydroxide: hydrogen peroxide heated to 80°C. The selectivity of this etch is 18:1 over Si and etches $Si_{0.7}Ge_{0.3}$ at a rate of ~3 nm/min. Once the final SiGe etch-stop layer is removed the remaining structure is the strained-Si/strained-Ge/strained-Si tri-layer heterostructure on an oxide layer, strained Ge HOI. Figure 3.6 depicts the etch-back sequence described above and final Ge HOI substrate. A high magnification cross sectional transmission electron micrograph (XTEM) of a strained-Ge HOI substrate is shown in Figure 3.7.

3.4 Ge composition and strain measurement

A low temperature bond and etch-back process described above is utilized to fabricate Ge HOI. Low temperature processing is required to avoid both strain relaxation and Ge diffusion in the device layers. The diffusivity of Ge has been observed to be enhanced in strained-Si/strained-SiGe heterostructures when the SiGe layer is under compressive strain [99]. Raman analysis and X-ray Diffraction (XRD) have been performed on blanket un-patterned substrates before and

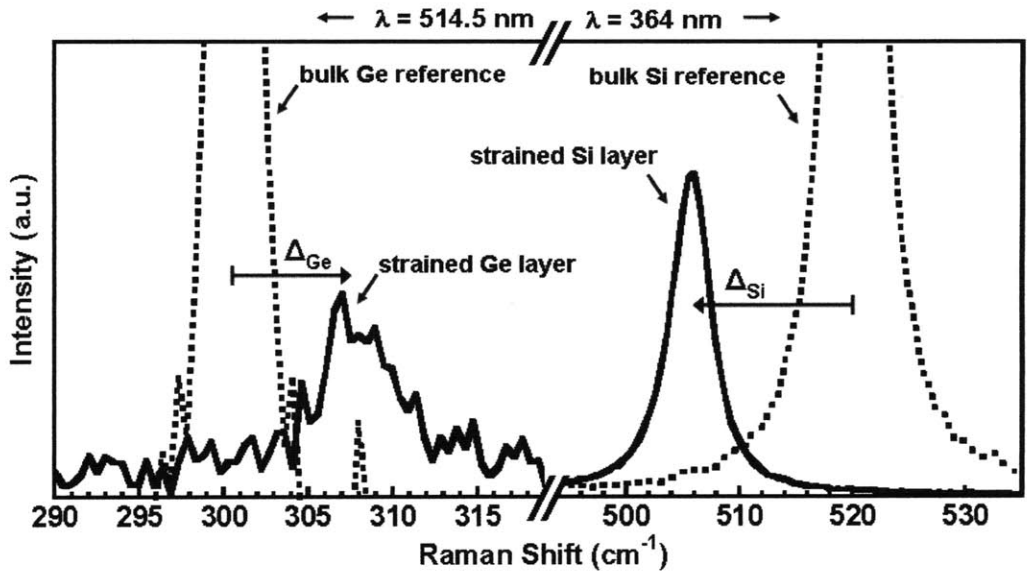


Figure 3.8 Raman spectra from the as-grown etch-back structure using 364 nm and 514 nm excitation for the Ge-Ge and Si-Si LO phonons from bulk crystals (dotted black curves) and the as-grown etch-back structure (black solid curve). The spectrum is comprised of a Ge-Ge band near 300 cm^{-1} from the Ge layer, and a Si-Si band near 520 cm^{-1} from the strained Si cap. The measured Ge and Si bands are shifted due to compressive and tensile strained respectively. Raman measurements and analysis courtesy M. Canonico (Freescale).

after bonding to measure changes in strain and Ge content in the strained-Si/strained-Ge heterostructure. XRD analysis was primarily utilized to determine the Ge content of the buried Ge layer and Raman analysis was performed to estimate the level of strain in the strained-Si and strained-Ge layers. The etch-back and Ge HOI substrates analyzed have strained-Si/strained-Ge heterostructures which are pseudomorphic (i.e. lattice matched) to relaxed $Si_{0.5}Ge_{0.5}$.

The strained Ge HOI etch-back structure is depicted in Figure 3.6 where the Si and Ge device layers are targeted to be pseudomorphic to a $Si_{0.5}Ge_{0.5}$ relaxed buffer. Raman spectra were collected from this structure using 364 nm and 514.5 nm excitation. Figure 3.8 shows UV and visible Raman spectra for the Ge-Ge and Si-Si LO phonons from bulk crystals (dotted curves) and

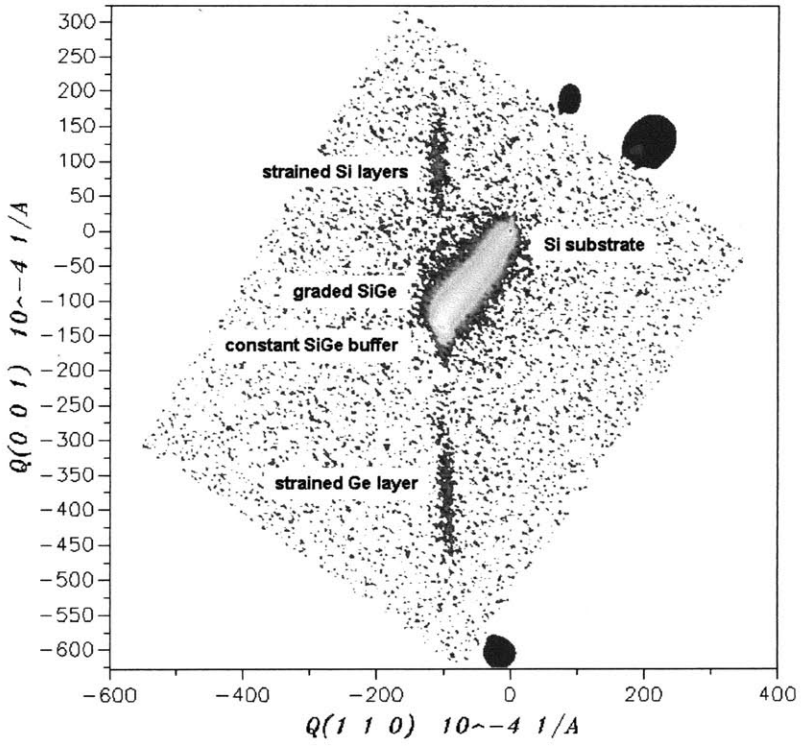


Figure 3.9 XRD measurement of the as-grown etch-back structure. The Si and Ge layers are significantly tilted relative to the relaxed Si substrate due to tetragonal distortion of the lattice by strain. The strain and Ge content were determined based on line shape fits to the diffraction peaks in the reciprocal space map. The strain in the Si and Ge layers are +1.97% and -1.85% respectively. The Ge content in the buried appears to be ~97% at.%. XRD measurements and analysis courtesy M. Canonico (Freescale).

the as-grown etch-back structure (solid curve). The spectra are fit with Lorentzian line-shapes with strain calculations based on adjustable fit parameters. Plasma lines, not shown in this spectrum, were fit using Gaussian profiles in order to account for thermal drift of the spectrometer. Each spectrum is comprised of a Ge-Ge band near 300 cm^{-1} from the Ge layer and a Si-Si band near 520 cm^{-1} from the strained Si cap. Based on a Ge-Ge frequency shift of +7.69 cm^{-1} from bulk Ge and a strain shift coefficient of -415 cm^{-1} [100], the in-plane biaxial strain in the strained Ge layer is –

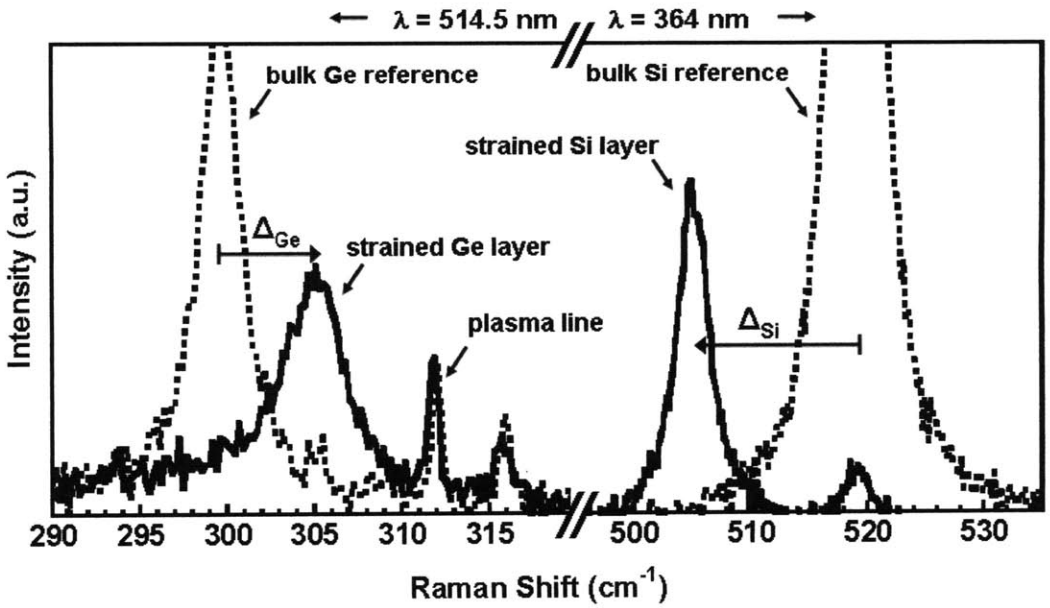


Figure 3.10 Raman spectra from the Ge HOI substrate using 364 nm and 514.5 nm excitation to obtain signal from the Si cap and Ge buried layer respectively. UV and visible Raman spectra are provided for the Ge-Ge and Si-Si LO phonons from bulk crystals (dotted black curves) and the Ge HOI substrate (black solid curve). Raman measurements and analysis courtesy M. Canonico (Freescale).

1.85%. When modeling the buried layer as pure Ge pseudomorphic to relaxed $Si_{0.5}Ge_{0.5}$ the relaxation is near 16%.

High resolution X-ray diffraction and modeling analysis were also performed by M. Canonico on the etch back structures depicted in Figure 3.6. Figure 3.9 presents the (224) Reciprocal Space Map (RSM) plotted in reciprocal lattice units taken around the Si (224) grazing exit (GE) asymmetric reflection. The Si and Ge layers are significantly tilted relative to the relaxed Si substrate due to tetragonal distortion of the lattice by strain. Based on Gaussian line shape fits to the diffraction peaks, the angular coordinates for each layer uniquely define the layer's lattice parameters. For the most general case, the Ge layer was modeled as a SiGe alloy to account for potential Si and Ge inter-diffusion. Using the calculated Ge layer lattice parameters, the relaxed

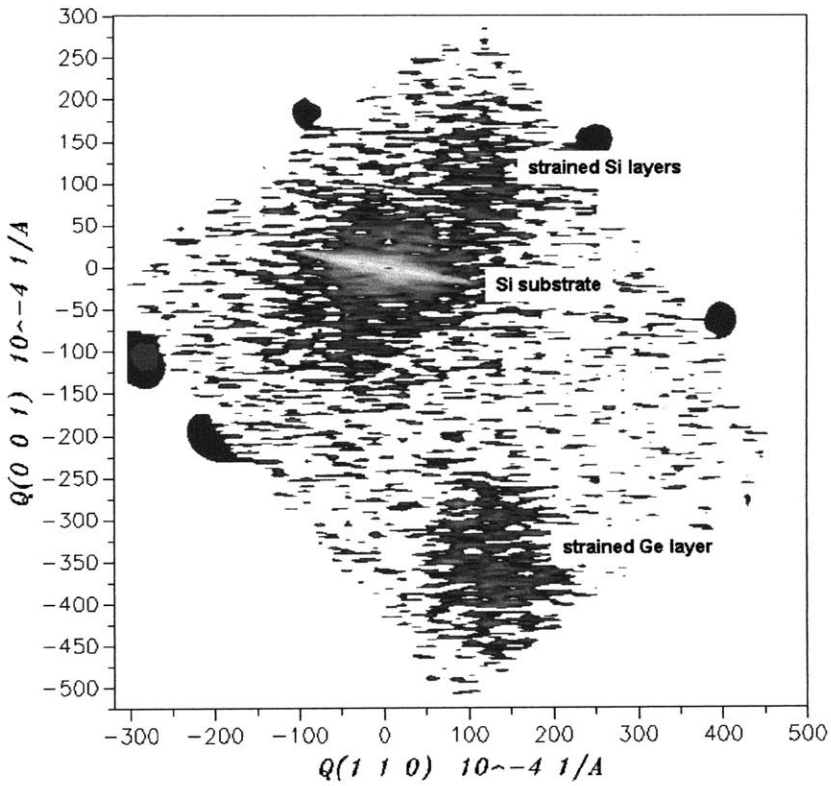


Figure 3.11 XRD measurement of the Ge HOI substrate. The Si and Ge layers are tilted relative to the relaxed Si substrate due to tetragonal distortion of the lattice by strain. The strain and Ge content were determined based on line shape fits to the diffraction peaks in the reciprocal space map. The Ge content in the buried layer appears to be ~93% at.%. XRD measurements and analysis courtesy M. Canonico (Freescale).

lattice constant and corresponding composition was determined. A successive iteration between the composition, the compositionally dependent Poisson ratio, and the relaxed lattice constant converges for a given composition and relaxation. The data suggests as much as 3-4% inter-diffusion between Si and Ge layers. If the Ge layer is modeled as having a composition of $Si_{0.03}Ge_{0.97}$ the relaxation calculated from the measured Raman shift decreases to 8%. Although the buried Ge layer was grown as a pure Ge layer the subsequent growth of the Si cap layer at 600°C

may have resulted in some Ge diffusion. The strained-Si layer has no measured relaxation with a strain shift of -14.67 cm^{-1}, corresponding to tensile strain of +1.97%.

After Ge HOI substrate fabrication Raman analysis was conducted on a blanket un-patterned substrate, similar to the substrate depicted in Figure 3.6 and imaged in Figure 3.7. These strain measurements were conducted on a Ge HOI substrate where the Si and Ge layers were targeted to be pseudomorphic to a relaxed $Si_{0.5}Ge_{0.5}$ layer. Raman spectra were collected from the substrate using the 364 nm and 514.5 nm Ar-Ion excitation wavelengths. Figure 3.10 shows UV and visible Raman spectra for the Ge HOI substrate. Since the HOI structure is grown on a fully relaxed $Si_{0.5}Ge_{0.5}$ buffer, the Ge layer is modeled as being pseudomorphic to $Si_{0.5}Ge_{0.5}$. The buried Ge layer was initially modeled as a pure Ge layer assuming no inter-diffusion. Based on a Ge-Ge frequency shift of +5.28 cm^{-1} from bulk Ge reference and a strain shift coefficient of -415 cm^{-1}, the in-plane biaxial strain is -1.27%, which represents a relaxation of 40% in the buried Ge layer.

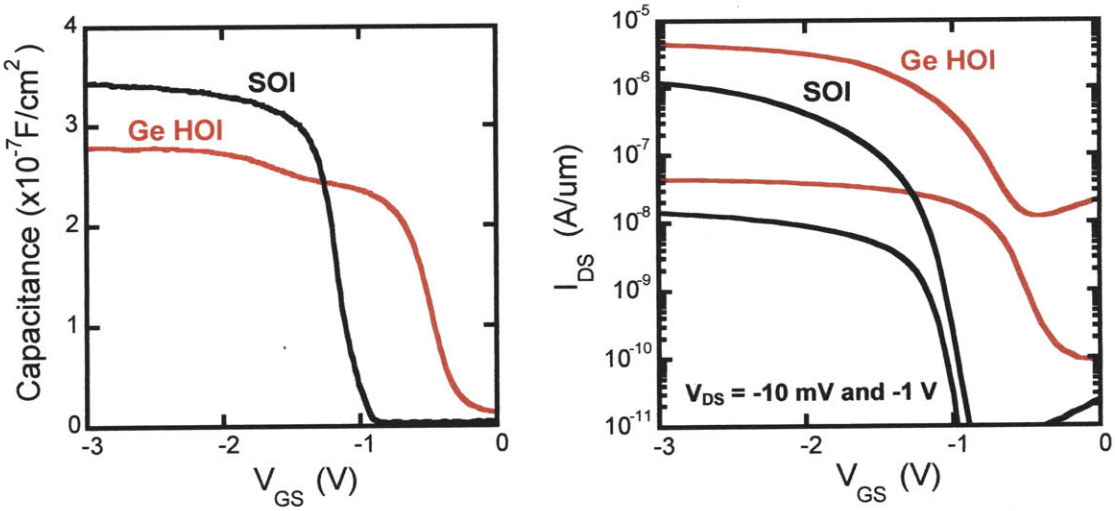
Figure 3.11 provides the XRD (224) Reciprocal Space Map (RSM) taken around the Si (224) grazing incidence (GI) asymmetric reflection. The GI geometry is used to enhance the sensitivity of the x-rays to the thin strained-Si and strained-Ge layers. The Si and Ge layers are significantly tilted relative to the substrate due to tetragonal distortion of the lattice by strain. To determine if Si and Ge interdiffusion occurred the Ge layer was modeled as a SiGe alloy which releases the constraint on the concentration. Using the peak position in the (224) RSM the Ge content in the strained-Ge layer is estimated to be 93 at.%. The drop in Ge content of the buried Ge layer during HOI fabrication is conceivable, since the substrates undergo a significant thermal treatment during the LTO densifying anneal (i.e. 2 hours at 600°C), which may cause interdiffusion between the strained-Si and strained-Ge layers. If this is taken into account and the Ge layer is modeled as a $Si_{0.07}Ge_{0.93}$ layer then the relaxation calculated from the Raman shift is 12%. The

phonon width also yields information about the periodicity of the layer. In this case, the Ge mode is 60% broader than the bulk peak, suggesting either defects due to relaxation and/or some Si-Ge inter-diffusion. Based on a Si-Si frequency shift of +14.09 cm^{-1} from bulk Si the in-plane biaxial strain in the Si cap layer is +1.89%, which represents a relaxation of 3.4%. The Si cap phonon width shows only slight broadening at 11.1% over the bulk value, indicating excellent crystallinity.

This work exhibits fabrication of the first strained-Si/strained-Ge heterostructure on insulator. XRD reveals a drop in the peak Ge content to about 97 at.% in the as-grown etch-back structure. Raman analysis on this structure reveals the Ge layer is 8% relaxed. Additional Si/Ge interdiffusion as well as relaxation in the Ge layer appears to occur during the bonding sequence. After layer transfer the Ge content of the buried layer appears to drop to 93% at.% and the layer is about 12% relaxed. The Si layers in the etch-back structure and final Ge HOI substrate are less than 5% relaxed, indicating little change in the strained Si films upon layer transfer.

3.5 Hole mobility in strained Ge HOI

P-MOSFETs have been fabricated to examine the hole mobility characteristics of strained Ge HOI. Devices were fabricated from a Ge HOI substrate consisting of a ~6 nm strained Ge layer flanked by two 3 nm strained Si cladding layers. These layers are lattice matched to relaxed $Si_{0.6}Ge_{0.4}$ (i.e. 100/40 strained Ge channel). P-MOSFET fabrication began by isolating the device regions via mesa dry etching. The mesa dimensions are greater than 10 μm, and therefore strain relaxation induced by patterning is assumed to be negligible [101,102]. Prior to gate stack formation the Ge HOI substrate is cleaned using a modified RCA cleaning process, which consists of 10 minutes in 3:1 H_2SO_4:H_2O_2 (110°C), 15 seconds in 50:1 DI:HF, 15 minutes in 6:1:1 DI:HCl:H_2O_2 (80°C), 15 seconds in 50:1 DI:HF and an SRD cycle. A 10 nm low temperature oxide (LTO) is then deposited and serves as the gate dielectric. A 100 nm thick in-situ phosphorus



(a) (b)

Figure 3.12 (a) Capacitance-voltage (CV) characteristics and (b) transfer characteristics for a strained Ge HOI (i.e. 100/40 strained Ge) and relaxed SOI control p-MOSFETs. The CV measurement frequency was 100 khz. The MOSFET gate length is 100 μm and width is 15 μm. The transfer characteristics were measured with V_{DS} = -10 mV and -1V.

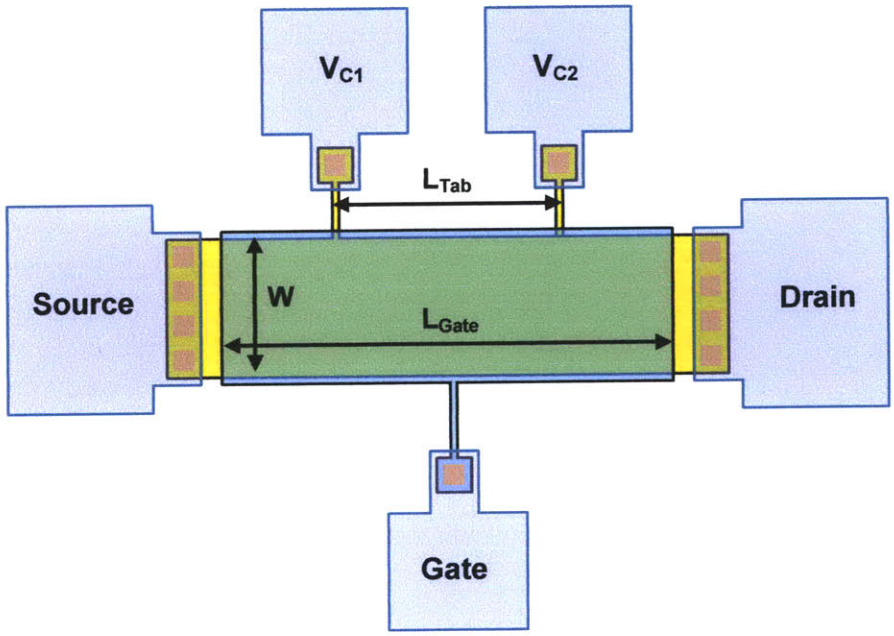


Figure 3.13 A diagram depicting the device architecture utilized in this work. The gate, source, drain, and channel voltage contacts are indicated in the diagram. The channel voltage measurements tabs are utilized to measure the intrinsic channel potential independent of the source/drain series resistance. The MOSFET gate length (L_{Gate}) and width (W) are 100 μm and 15 μm respectively. The distance between the channel voltage tabs (V_{C1} and V_{C2}) is 36 μm. The channel voltage tabs are spaced 32 μm from the left and right edges of the gate.

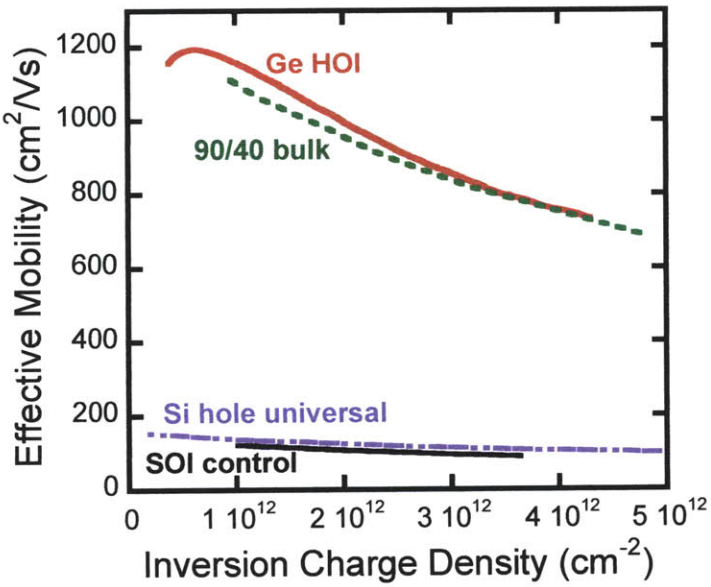


Figure 3.14 Measured effective hole mobility versus inversion charge density for a strained Ge 100/40 HOI p-MOSFET, a bulk 90/40 strained SiGe heterostructure p-MOSFET, a relaxed SOI control p-MOSFET, and the universal Si hole mobility. A 9x mobility enhancement is observed for both the Ge HOI and bulk heterostructure substrates over the Si universal hole mobility.

doped polycrystalline Si was subsequently deposited to form the gate. Prior to gate etching the front side of the wafer is coated with resist to protect the wafer during back-side poly-Si etching. The back-side poly-Si is etched in a Cl_2 plasma and the front-side protection was subsequently removed. The gate level is then patterned and etched in a Cl_2 plasma.

The self-aligned formation of the source/drain regions was done by implanting BF_2 at an energy of 17 keV with an implant dose of $4x10^{15}$ cm^{-2}. The gate resist is then removed from the gate. The wafers are cleaned prior to inter-layer dielectric deposition using a modified RCA cleaning process, which consists of 10 minutes in 5:1:1 DI:NH_4OH:H_2O_2 (80°C), 15 minutes in 6:1:1 DI:HCl:H_2O_2 (80°C), 10 seconds in 50:1 DI:HF and a spin-rinse dry (SRD) cycle. A 150nm LTO dielectric inter-layer was deposited. The modified RCA clean was then repeated prior to the

dopant activation anneal. The dopant activation anneal sequence consists of 2 minutes at 625°C followed by 15 seconds at 750°C. Contact vias were subsequently patterned and opened using a dilute 5:1 DI:BOE timed wet etch. A 30 minute 500°C forming gas anneal was then done prior to metallization. Immediately before metal deposition, wafers were exposed to 50:1 DI:HF for 15 seconds to remove the native oxide on the Si surface. Metallization consisted of a 150 nm of Ti followed by 500 nm of $Al_{0.98}Si_{0.02}$. A final forming gas anneal was conducted for 30 minutes at 500°C.

After device fabrication, valid operation was verified by conducting electrical measurements. MOSFET transfer (i.e. I_{DS} vs. V_{GS}) and gate-capacitance (i.e. C_{GC} vs. V_{GS}) characteristics were measured and are presented in Figure 3.12. The difference in C_{max} is attributed to a difference in the deposited LTO gate dielectric thickness. The current is higher for p-MOSFETs fabricated on strained-Ge HOI compared to those on unstrained SOI. The leakage current is also larger for strained-Ge HOI device. This may be due to band-to-band tunneling in the off-state, or implant damage that may have created defects in the crystal which short the source/drain p-n junctions [7, 27, 103-107]]. The larger current observed in strained Ge HOI is mainly attributed to the higher hole mobility in biaxial compressive strained Ge relative to relaxed Si. This was confirmed by extracting the effective hole mobility in both sets of devices. A mobility extraction MOSFET structure was utilized to extract the effective hole mobility independent of the extrinsic parasitic resistance [71]. This device architecture incorporates voltage tabs in the channel that are used to measure the intrinsic drain-to-source voltage. Figure 3.13 provides a diagram of the mobility extraction MOSFET design. The mobility extraction was done in accordance with the description provided in 2.5.1. The effective hole mobility for 100/40 strained-Ge HOI, a 90/40 bulk substrate, and relaxed SOI are plotted in Figure 3.14.

3.6 Summary and conclusions

This work exhibits fabrication of the first strained-Si/strained-Ge heterostructure on insulator. The targeted structure was a pure stained Ge layer passivated by two cladding strained Si layers resting on a buried oxide. XRD analysis reveals a drop in peak Ge content to about 97% in the strained Ge layer of the epitaxially grown etch-back structure. Raman analysis on this structure reveals that this layer is about 8% relaxed. The observed drop in Ge content and strain may have occurred during the growth of the final Si layer which was conducted at 600°C. Additional Si/Ge interdiffusion as well as relaxation in the Ge layer appears to occur during the wafer bonding process. After layer transfer the Ge content of the strained Ge layer drops to 93% and the layer is about 12% relaxed. Further optimization of the bond process is needed to limit the Si and Ge interdiffusion as well as the relaxation that occurs during substrate fabrication. The strained Si layers in the etch-back structure and final Ge HOI substrate are less than 5% relaxed, indicating little change in the strained Si films upon layer transfer. The extracted mobility characteristics reveal a 9x hole mobility enhancement relative to relaxed SOI. The strained Ge HOI hole mobility is quite comparable to the mobility in a 90/40 bulk p-MOSFET (i.e. bulk p-MOSFET with a strained $Si_{0.1}Ge_{0.9}$ channel pseudomorphic to relaxed $Si_{0.6}Ge_{0.4}$). The XRD analysis performed on the completed Ge HOI substrate suggested a 7% drop in the Ge content of the strained Ge layer. This is in good agreement with the mobility result which shows that the Ge HOI hole mobility is comparable to the that of a 90/40 bulk p-MOSFET, again where the peak channel Ge composition is 90%. The mobility result also suggests that there may have been a slight drop in peak channel Ge percentage. Regardless, the hole mobility observed in strained Ge HOI is still quite impressive. The mobility gains provided by biaxial compressive strained SiGe and Ge are substantial, but for

these materials to be viable options for deeply scaled CMOS the transport benefits must translate well into a scaled device platform. In the next chapter we will examine the transport performance of short channel biaxial compressive strained SiGe p-MOSFETs.

Chapter 4

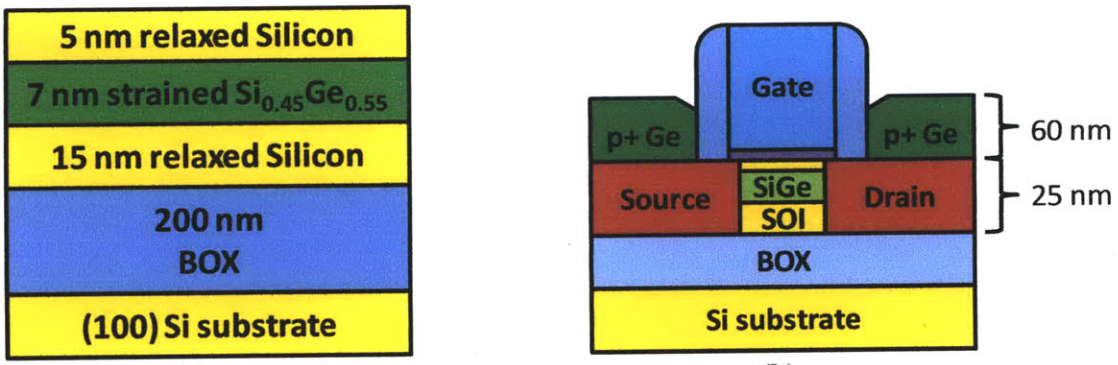
HOLE TRANSPORT IN SHORT CHANNEL STRAINED-SIGE P-MOSFETS

4.1 Introduction

In this chapter the carrier transport properties of short channel biaxial compressive strained-SiGe p-MOSFETs are explored. The hole mobility and velocity are measured in sub-100 nm strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs on insulator. The goal is to assess the scalability of these transport metrics. An ultrathin-body architecture is utilized to improve electrostatics at shorter gate lengths without the need for halo or body implants, which may impact the channel strain or degrade carrier mobility by introducing coulombic scattering centers [20, 24, 114-116]. Process steps which might disrupt the channel strain were modified or eliminated in an attempt to examine the intrinsic transport performance gains independent of process conditions. Band structure and ballistic velocity simulations are also presented to explore the benefits of introducing uniaxial compressive stress to an already biaxial compressive strained-SiGe channel.

4.2 Short channel strained SiGe p-MOSFET fabrication

Strained $Si_{0.45}Ge_{0.55}$ channel p-MOSFETs were fabricated on relaxed-Si/strained-$Si_{0.45}Ge_{0.55}$ heterostructure on-insulator substrates. These substrates were generated by growing a 7 nm $Si_{0.45}Ge_{0.55}$ layer on a 15 nm relaxed (100) oriented SOI substrate. The strained $Si_{0.45}Ge_{0.55}$ layer is grown pseudomorphic to the underlying relaxed SOI layer (i.e. 55/0), and is therefore under -2.3% biaxial compressive strain. After growth of the strained $Si_{0.45}Ge_{0.55}$ layer a 5 nm relaxed Si passivation layer was grown to enable the formation of a high quality dielectric



(a) (b)

Figure 4.1 (a) A schematic view of the device structure. The channel consists of a 7 nm thick biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ layer pseudomorphic to a 15 nm thick relaxed SOI. The structure is capped with 5 nm of Si. (b) A cross-section diagram the strained-$Si_{0.45}Ge_{0.55}$ p-MOSFET structure. About 2 nm of the Si cap was lost during the gate oxidation resulting in a total body thickness of 25 nm. 60 nm of heavily boron doped Ge was selectively grown in the source/drain region to mitigate the extrinsic series resistance.

interface. The relaxed-Si/strained-$Si_{0.45}Ge_{0.55}$ heterostructure on insulator substrate used in this work is depicted in Figure 4.1a. All layers are nominally undoped.

Short channel p-MOSFETs were fabricated on the substrates described above. A mesa isolation scheme oriented in the <110> direction was used to electrically isolate devices from one another. The gate stack was formed by thermally oxidizing the Si passivation layer at 600°C forming a 3.6 nm gate oxide and subsequently depositing a 100 nm of heavily n-doped polycrystalline silicon. A 75 nm silicon nitride layer was then deposited for use as a patterning hard mask during the gate etch. Hybrid e^--beam and photo lithography were used to pattern a nitride hard mask on the gate. Gate lengths down to 65 nm were patterned using XR-1541 (Dow Corning™) e^--beam resist. The extension region was then formed by implanting Boron into the substrate (Boron, 6 keV, $2x10^{14}$ cm^{-2}). A medium-dose extension implant was utilized to minimize strain relaxation in the $Si_{0.45}Ge_{0.55}$ channel. Retaining the channel strain along the <110> transport direction is critical to observe enhanced hole transport characteristics. 120 nm of LTO was then deposited and spacers were formed. The deep source/drain implant was omitted from this process

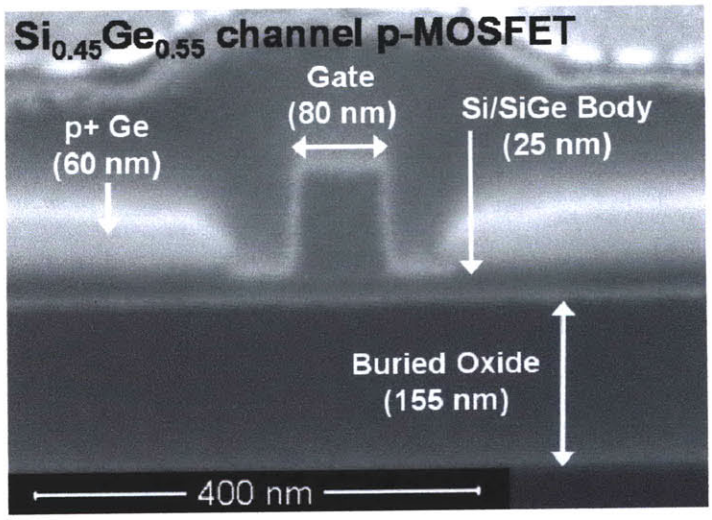
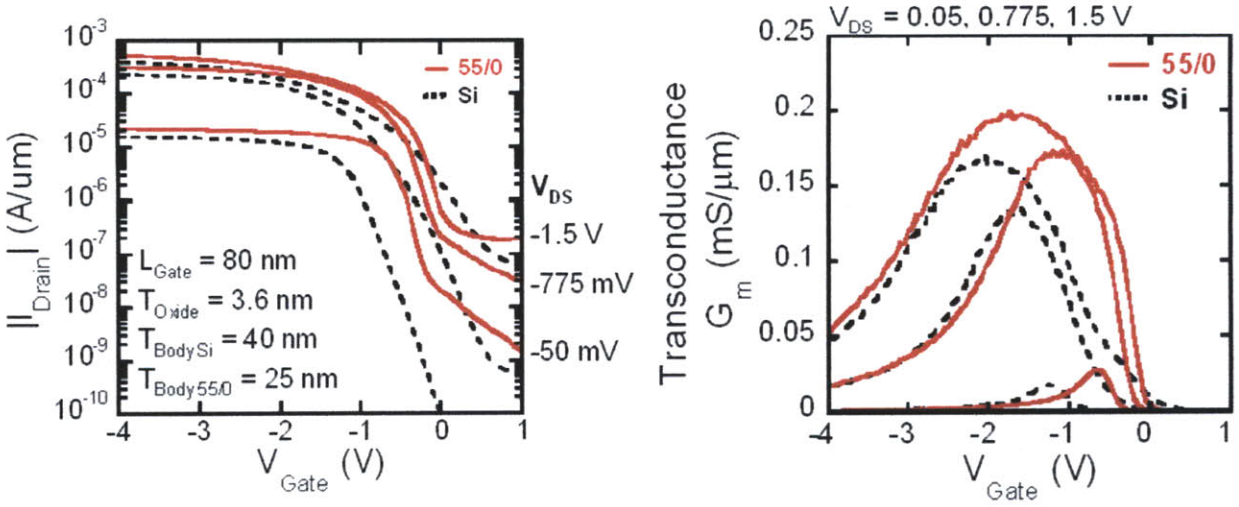


Figure 4.2 A cross-section SEM micrograph of an 80 nm long strained-$Si_{0.45}Ge_{0.55}$ p-MOSFET. The total channel thickness is 25 nm. 60 nm of heavily boron doped Ge was selectively grown in the source/drain region.

to avoid relaxation of the channel strained. Instead, boron-doped germanium was selectively grown in the source/drain region to reduce the extrinsic parasitic series resistance. Dopants were activated with a rapid thermal anneal consisting of 30 sec at 650°C followed by 5 sec at 700°C. A conservative thermal budget was maintained to minimize Ge out diffusion from the strained-$Si_{0.45}Ge_{0.55}$ layer. Silicon control devices were also fabricated on relaxed SOI for comparison. In Figure 4.2 a cross-section scanning electron micrograph of a completed 80 nm strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFET is provided.

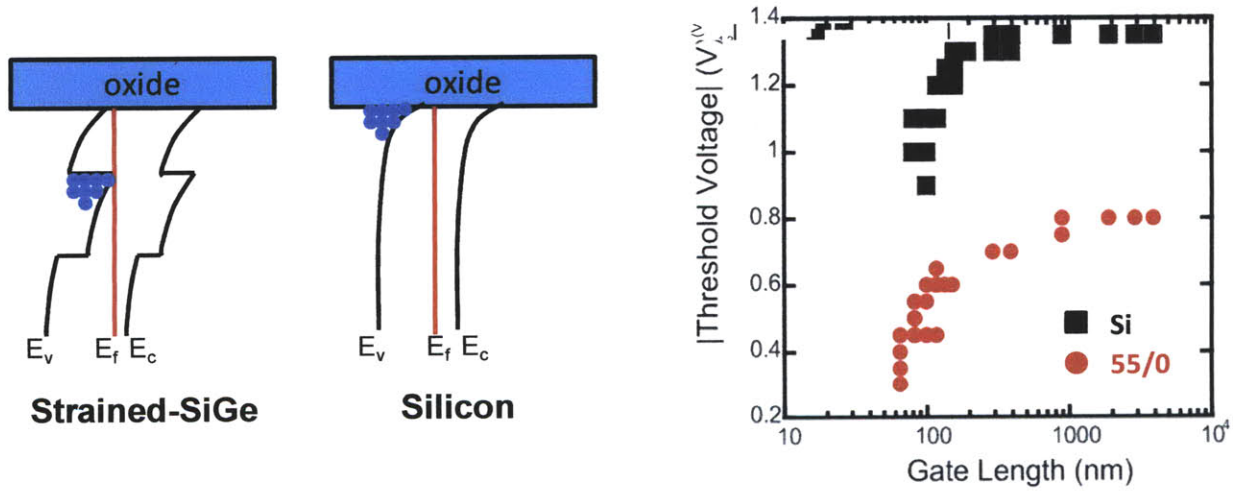
4.3 Short channel strained SiGe p-MOSFET electrical results

After device fabrication electrical measurements were performed to confirm valid devices operation. Standard transfer (i.e. I_{DS}-V_{GS}) and transconductance (i.e. G_m-V_{GS}) curves are presented in Figure 4.3 for 80 nm gate length strained $Si_{0.45}Ge_{0.55}$ and relaxed Si control p-MOSFETs. The strained $Si_{0.45}Ge_{0.55}$ channel devices exhibit a larger current and transconductance compared to



(a) (b)

Figure 4.3 (a) The transfer (I_{DS} vs. V_{GS}) and (b) transconductance (G_m vs. V_{GS}) characteristics for 80 nm relaxed-Si and strained-$Si_{0.45}Ge_{0.55}$ (wafer number 5142) p-MOSFETs.



(a) (b)

Figure 4.4 (a) A depiction of the band alignment for strained SiGe and relaxed Si channel p-FETs. In strained-SiGe p-MOSFETs, carriers are segregated away from the dielectric interface by a valence band offset which confines then in the strained-SiGe layer. (b) The extracted threshold voltages for $Si_{0.45}Ge_{0.55}$ and Si channel devices are plotted. A threshold voltage difference of about 0.5 V exists between Si and strained SiGe devices due to the valence band offset.

the relaxed Si control devices. The observed current and transconductance enhancement can result from differences in carrier mobility, extrinsic resistance, threshold voltage, and gate capacitance.

In Figure 4.3 (a) and (b) we see evidence of a threshold voltage difference between strained $Si_{0.45}Ge_{0.55}$ and Si control devices. The threshold voltage difference is due to the band offset at the Si/strained-SiGe interface. The finite potential well which confines carriers in the strained $Si_{0.45}Ge_{0.55}$ layer also puts the valence band edge closer to the Fermi level resulting in a lower threshold voltage (compared to the relaxed Si device). In Figure 4.4 (a) a schematic of the band alignment for strained SiGe and relaxed Si channel p-FETs is provided. In Figure 4.4 (b) the extracted threshold voltages for the strained-$Si_{0.45}Ge_{0.55}$ and Si channel devices are plotted. The threshold voltage was extracted using the transconductance change (i.e. dG_m/dV_{GS}) threshold voltage extraction method [119]. This method was utilized because it eliminates the influence of mobility degradation and parasitic resistance. A ~0.6 V difference in the threshold voltage was observed between strained-$Si_{0.45}Ge_{0.55}$ and Si channel devices.

When comparing MOSFET performance, differences in the extrinsic resistance must be taken into account to ensure that the intrinsic bias voltages are comparable. Series resistance extraction was performed using the l-array and G_o methods [117, 118]. The l-array method consists of plotting the total device resistance ($R_{total} = V_{DS}/I_{DS}$) as a function of the gate length for a variety of over drive conditions. A linear fit for each over drive curve is extrapolated out to the vertical axis and the intercept provides an estimate of the extrinsic source/drain resistance for the group of devices plotted. The physical gate lengths were determined by cross-section SEM imaging devices with physical gate lengths of 155 nm and 80 nm. Figure 4.5 is a plot of the target versus physical gate length. The offset between the target and physical gate length was determined to be

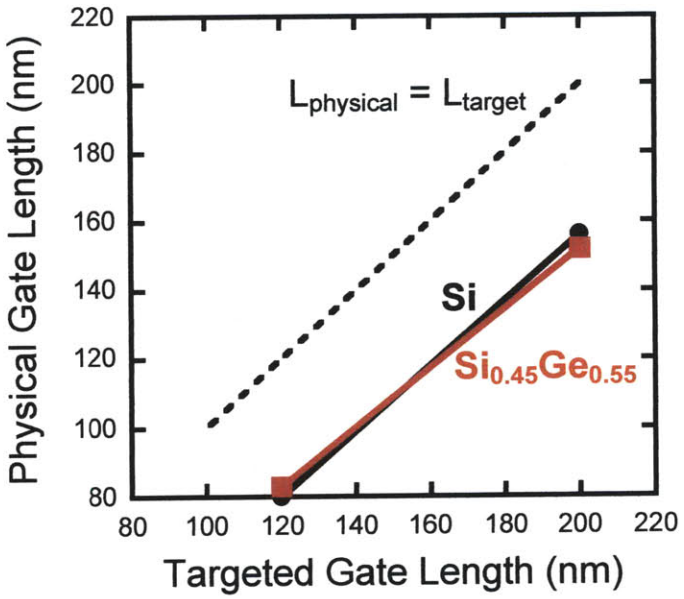
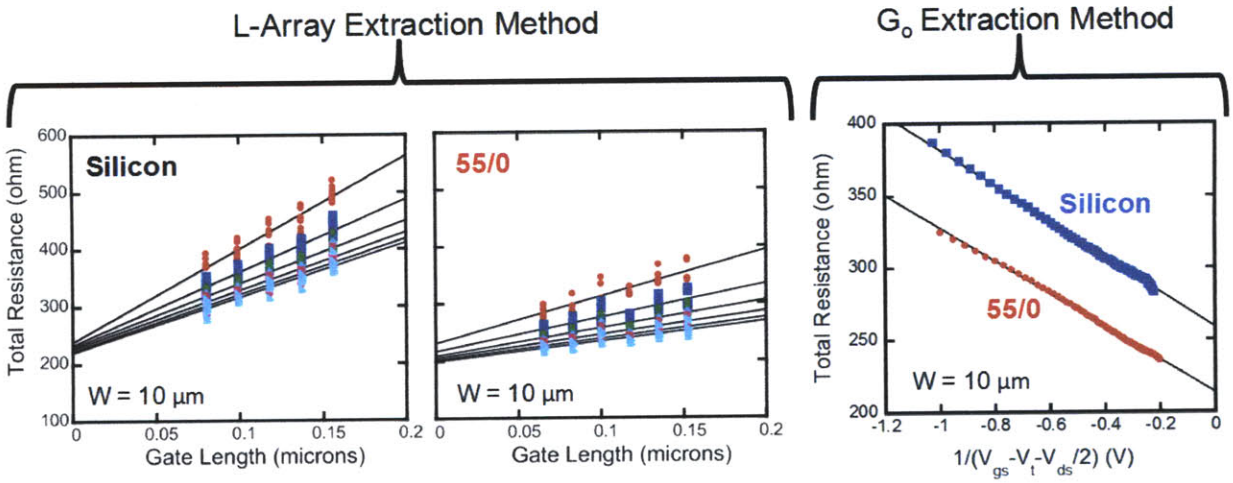


Figure 4.5 The physical gate length measured via XSEM imaging is plotted versus the e-beam targeted gate length. The two imaged Si devices (black closed symbols) and two imaged $Si_{0.45}Ge_{0.55}$ devices (red closed symbols) are plotted. The offset between the target and physical gate length was determined to be approximately 35 nm for both Si and $Si_{0.45}Ge_{0.55}$ channel devices. This offset was applied to all target gate length values to determine the physical gate length.

approximately 35 nm for both Si and $Si_{0.45}Ge_{0.55}$ channel devices. This offset was applied to all target gate length values to determine the physical gate length. In short channel devices where the physical gate length and effective gate length differ it is appropriate to use the effective gate length in combination with the l-array method to estimate the extrinsic resistance. Extracting the effective gate length via capacitance method was not possible due to the rather high extrinsic resistance and therefore the physical gate length was used. The l-array estimate of the extrinsic resistance for strained $Si_{0.45}Ge_{0.55}$ devices is 2100 ohm-μm and for Si control devices is 2400 ohm-μm, Figure 4.6.

The extrinsic resistance was also extracted on a device-by-device basis using the G_o extraction method [118]. This method relies on plotting R_{total} as a function of the inverse over-drive in the linear regime (i.e. $1/(V_{GS}-V_T-V_{DS}/2)$. The data is extrapolated out to the vertical axis and the



	R_{ext} (L-Array method)	R_{ext} (G_o method)
Silicon	2400 ohm-µm	2620 ohm-µm
55/0	2100 ohm-µm	2010 ohm-µm

Figure 4.6 The L-Array [117] and G_o [118] extraction plots for a Si and strainded-$Si_{0.45}Ge_{0.55}$ are plotted. The L-Array plot has over-drive curves corresponding to 0.5V, 1V, 1.5V, 2V, 2.5V, and 3V. The average R_{ext} for the l-array and Go methods are reported in the table. The R_{ext} values are in good agreement providing confidence in the extracted results. The reported R_{ext} values are rather high. This is due in part to the large distance between the gate edge and source/drain contact plugs (2 µm) and the absence of a silicide or germanide process. In addition, some contribution to R_{ext} may be expected from the S/D extension process (moderate dose and low temperature activation) which largely preserved the channel strain.

intercept provides a measure of R_{ext} for that device. In Figure 4.6 the G_o extraction plot for a Si and strained-$Si_{0.45}Ge_{0.55}$ p-MOSFET are plotted. The average R_{ext} for the l-array and Go methods reported in Figure 4.6 are in good agreement. The reported R_{ext} values are rather high. This is due in part to the large distance between the gate edge and source/drain contact plugs (2 µm) and the absence of a silicide or germanide process. In addition, some contribution to R_{ext} may be expected from the S/D extension process (moderate dose and low temperature activation) which largely preserved the channel strain, as shown in the next section. The lower R_{ext} in strained $Si_{0.45}Ge_{0.55}$ p-MOSFETs contributes to the higher current observed relative to relaxed Si. This difference in R_{ext}

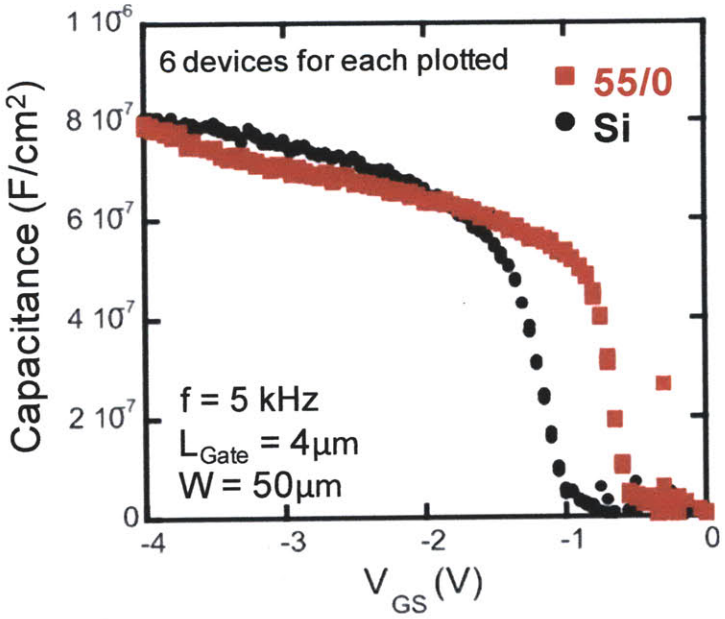


Figure 4.7 Measured gate capacitance-voltage (CV) curves for long channel (4 μm long x 50 μm wide) Si control and strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs. The measurement frequency was 5 kHz.

must be compensated for when comparing devices. Later in this chapter the effective hole mobility will be extracted using a method which compensates for the extrinsic R_{ext}. This will help us gauge the intrinsic device performance independent of parasitic effects like R_{ext}.

The measured gate capacitance-voltage (C_{GC}-V_{GS}) curves for long channel Si and strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs are presented in Figure 4.7. The measurement frequency was 5 kHz. The large series resistance of these devices prevented measurement at higher frequencies and the measurement of short gate length devices. There is a noticeable threshold voltage difference between Si and strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs due to the valence band offset discussed earlier. This valence band offset also segregates carriers away from the gate-oxide/silicon interface effectively increasing the dielectric thickness. Proof of this effect exists in the CV curves, where the maximum capacitance of the strained-$Si_{0.45}Ge_{0.55}$ devices is lower than that of the Si devices.

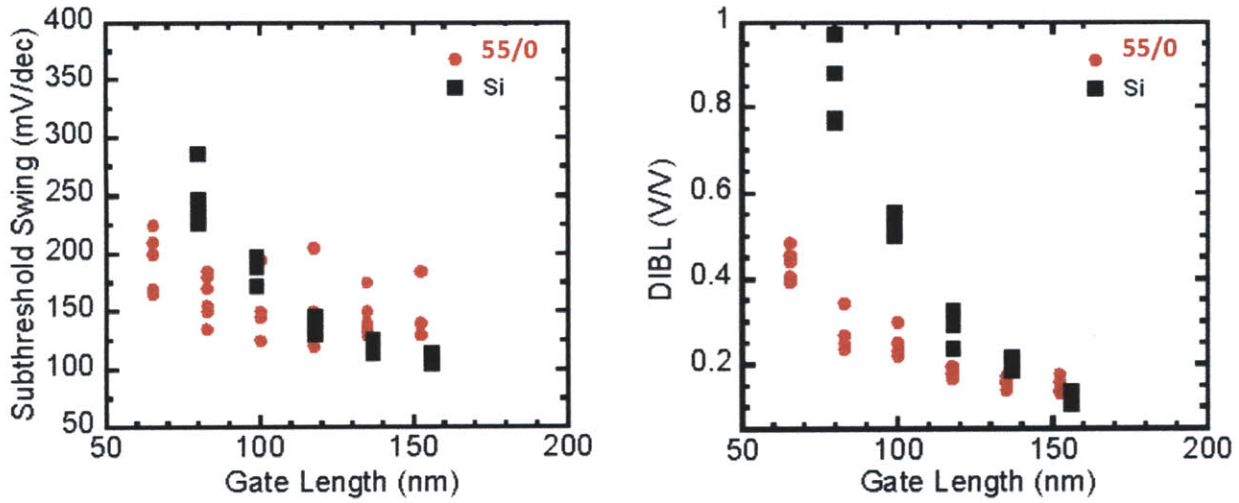
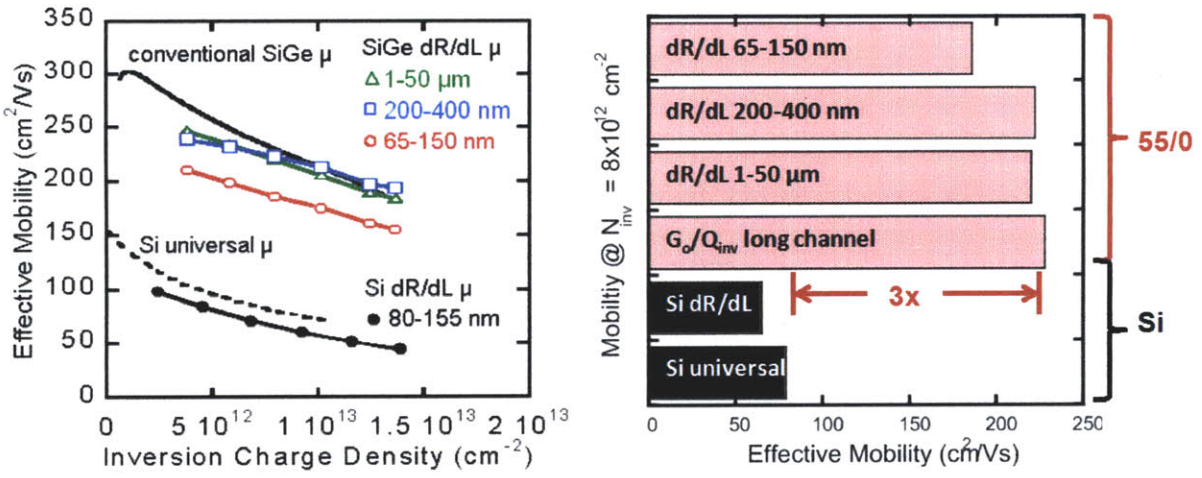


Figure 4.8 (a) Subthreshold swing vs. L_{Gate} comparison between strained-$Si_{0.45}Ge_{0.55}$ and Si control devices. (b) DIBL vs. L_{Gate} comparison between strained-$Si_{0.45}Ge_{0.55}$ and Si control p-MOSFETs. The strained-$Si_{0.45}Ge_{0.55}$ channel devices exhibit improved electrostatic behavior at shorter gate lengths due to a thinner body. DIBL was measured using the constant current method in the subthreshold regime. The subthreshold swing was measured at V_{DS} = -50 mV.

In Figure 4.8 the electrostatic metrics, DIBL and subthreshold swing, are plotted versus gate length. Reasonable electrostatic behavior is observed down to a gate length of 100 nm for strained $Si_{0.45}Ge_{0.55}$ devices and 120 nm for the Si control. The difference in electrostatic behavior is mainly attributed to the difference in body thickness between devices. The strained $Si_{0.45}Ge_{0.55}$ devices have a total body thickness of 25 nm, which includes a 3 nm Si cap (reduced from 5 nm after cleaning and oxidation), 7 nm buried $Si_{0.45}Ge_{0.55}$ channel, and 15 nm underlying SOI film. The Si control devices have a body thickness of 40 nm. The electrostatic benefit of the thin body architecture results from the fact that the field lines emanating from the drain terminating in the underlying substrate as opposed to the channel. This gives the gate greater control over the channel charge. As the body thickness is reduced to less than a third of the gate length a dramatic improvement in electrostatic performance is observed [7, 88, 89]. In fact, a general rule of thumb is that the body thickness in thin-body MOSFETs should be less than a



(a) (b)

Figure 4.9 (a) Comparison between the long channel (g_D/Q_{inv}) and short channel dR/dL extracted mobility [72] for Si and strained-SiGe p-MOSFETs. (b) The hole mobility values for the mobility curves in (a) are plotted for an inversion charge density of $8x10^{12}$ cm^{-2}. A 3x enhancement over the Si hole universal mobility is observed for strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs with L_{Gate} ranging from 0.2-50 μm. Devices with gate lengths ranging from 65-150 nm show a 2.4x enhancement. The dR/dL mobility curve for Si p-MOSFETs with gate lengths ranging from 80-155 nm is also plotted for comparison.

third of the gate length in order to maintain electrostatic integrity. Despite the degraded electrostatics at shorter gate lengths we can still extract meaningful transport metrics like mobility. In the next section we will extract the short channel mobility to gauge the intrinsic transport performance of strained $Si_{0.45}Ge_{0.55}$ and Si p-MOSFETs.

4.4 Hole mobility in short channel strained SiGe p-MOSFETs

The hole mobility characteristics of short channel strained $Si_{0.45}Ge_{0.55}$ and Si p-MOSFETs are examined to compare the intrinsic transport characteristics independent of differences in R_{ext}, C_{GC}, threshold voltage, subthreshold swing, and DIBL. Hole effective mobility was extracted from short channel strained $Si_{0.45}Ge_{0.55}$ and Si control devices using the dR/dL method [72]. This extraction method provides a measure of the mobility that is independent of the extrinsic resistance. The dR/dL mobility is calculated from the slope of the

total device resistance versus gate length curves shown in Figure 4.6. This extraction method is a measure of the average mobility for a range of gate lengths and assumes that the mobility as well as the series resistance are constant for devices in a given range. The linearity of the L-array data in Figure 4.6 suggests that neither the effective hole mobility nor the extrinsic resistance vary significantly as a function of gate length. The dR/dL hole effective mobility is given by

$$\mu_{eff} = \frac{1}{WQ_{inv}\dfrac{dR_{Total}}{dL}} \qquad \text{Equation 4.1}$$

where W is the device width, Q_{inv} is the inversion charge density, and dR_{Total}/dL is the slope of the L-array data in Figure 4.6. With this method the slope of each over drive curve in the L-array plot provides the basis for calculating the mobility. As mentioned earlier measuring the short channel C_{GC}-V_{GS} characteristics was not possible due to the high extrinsic resistance of these devices. The inversion charge density (i.e. Q_{inv}) was therefore estimated by integrating the C_{GC}-V_{GS} characteristics measured on large area MOSFETs with a gate length of 4 microns and a device width of 50 μm, Figure. 4.7. Both DIBL and V_{th} roll off were taken into account when integrating the normalized large area C_{GC}-V_{GS} characteristics to estimate the inversion charge density at shorter gate lengths. The Q_{inv} estimate is given by

$$Q_{inv} = \int_0^{V_{GS}-V_{t,short}-V_{t,long}} C_{GC}\, dV_{GS} \qquad \text{Equation 4.2}$$

The long channel hole effective mobility was extracted using both the dR_{Total}/dL and the more conventional (g_D/Q_{inv}) approach

$$\mu_{eff} = \frac{g_D L}{Q_{inv} W} \qquad \text{Equation 4.3}$$

where g_D is the output conductance measured at low V_{DS}, L is the gate length, W is the device

width, and Q_{inv} is the inversion charge density [117].

The dR/dL mobility was calculated for strained $Si_{0.45}Ge_{0.55}$ devices with gate lengths ranging from 65-150 nm, 200-400 nm, and 1-50 μm. The conventional g_D/Q_{inv} effective mobility was extracted from a 100 μm long strained $Si_{0.45}Ge_{0.55}$ channel mobility extraction MOSFET for comparative purposes [71]. The extracted effective hole mobility curves are presented in Figure 4.9(a). The long channel dR/dL (i.e. 200-400 nm and 1-50 μm gate lengths) and g_D/Q_{inv} strained $Si_{0.45}Ge_{0.55}$ mobility are in good agreement. This agreement helps validate the dR/dL mobility extraction method. The Si hole universal mobility and dR/dL mobility for Si p-MOSFETs with gate lengths ranging from 80-155 nm are also plotted in Figure 4.9(a). The short channel Si dR/dL mobility and Si hole universal mobility are in good agreement, which also helps validate the dR/dL mobility extraction method. The reported mobilities for both long and short channel strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs are higher than the Si control and hole universal mobility curves. In Figure 4.9 (b) the hole mobility values for the mobility curves in Figure 4.9 (a) are plotted for an inversion charge density of $8x10^{12}$ cm^{-2}. This plot clearly illustrates the 3x hole mobility enhancement provided by long channel strained $Si_{0.45}Ge_{0.55}$ p-MOSFETs over relaxed Si. The short channel strained $Si_{0.45}Ge_{0.55}$ mobility is slightly lower than the long channel mobility, but maintains a substantial enhancement at 2.4x.

The drop in mobility at shorter gate lengths may result from a slight relaxation in the channel strain, Coulombic scattering from the extension implants, or scattering off of non-Coulombian (neutral) defects at the extension edge. In patterned structures significant strain relaxation occurs in the vicinity of the free surface. Ion implantation can create an effective free surface by severely disrupting the lattice at the implant edge [120, 121]. Strain relaxation has been observed in patterned strained-Si/strained-Ge heterostructures, where the mesa etched

heterostructure dimensions are less than 100 nm [120]. While the implant conditions in this work were relatively mild, they may have disrupted the lattice enough to induce some strain relaxation which becomes evident at shorter gate lengths. Remote Coulombic scattering from the extension implant may also be degrading the mobility at shorter gate lengths. As gate lengths are scaled and a greater portion of carriers in the channel come into close proximity with the heavily doped source/drains, long range Coulombic interactions are expected to become a significant mobility limiting mechanism. This effect is only expected to become significant when the MOSFET gate lengths is scaled below 50 nm [115, 116], and may not be a significant mobility limiting mechanism for the devices fabricated in this work. Scattering from non-Coulombian (neutral) defects may be contributing to the observed mobility degradation. Neutral defect scattering has been observed in devices with gate lengths smaller than 200 nm [122]. This scattering mechanism arises from neutral defects at the source/drain extension edge or at the dielectric interface near the source/drain. These neutral crystalline defects are typically introduced during ion implantation of the extension region or deep source/drain. Moreover the strain in strained $Si_{0.45}Ge_{0.55}$ channel devices relaxes during ion implantation by generating crystalline defects in addition to those created by the physical bombardment of ions during implantation. A substantial activation anneal is essential to adequately repair these neutral crystalline defects [122]. In this work the conservative thermal budget used to minimize strain relaxation and Ge out-diffusion may have not been adequate in repairing these crystalline defects. Consequently neutral defect scattering may be contributing to the slight mobility degradation observed in short channel strained $Si_{0.45}Ge_{0.55}$ p-MOSFETs.

4.5 Hole velocity in short channel strained SiGe p-MOSFETs

As aggressive geometric scaling of CMOS continues the gate length will reach a point

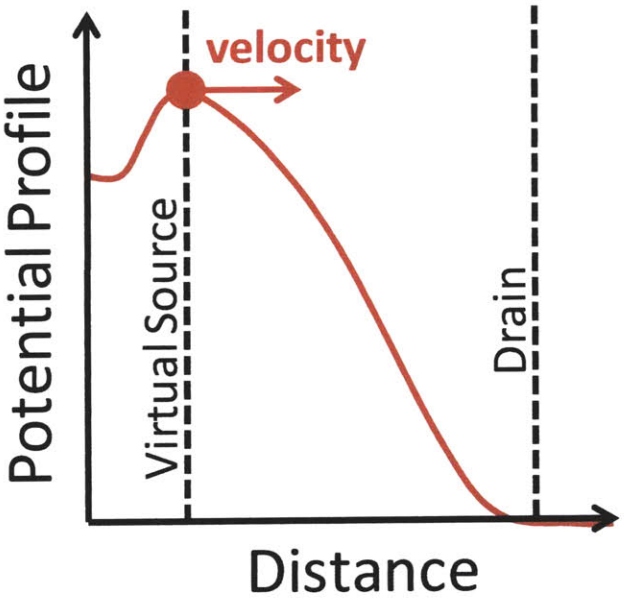


Figure 4.10 A depiction of the source to drain potential distribution is provided. The virtual source velocity is a measure of the velocity for carriers coming into the channel from the top of the source barrier.

where it is comparable to the mean free path of carriers in the channel. In this regime carrier mobility becomes an ambiguous transport measure. A more appropriate transport metric is velocity. Since the 90 nm CMOS technology node uniaxial strain has been utilized to increase the carrier velocity and consequently boost the on-current [1][2]. The virtual source velocity enhancement provided by uniaxial strained Si in state of the art p-MOSFETs is about 2x relative to relaxed Si [87]. This enhancement is expected to saturate in uniaxial strained Si with increasing levels of strain [48][123]. Alternative channel materials are sought which provide an even greater enhancement than uniaxial strained Si. Some obvious candidates include biaxial compressive strained SiGe and strained Ge, which can provide very impressive mobility gains over relaxed Si. In this section we will examine whether these impressive mobility gains translate to a significant velocity gain.

Three velocity extraction methods have been employed. The virtual source velocity (υ_{xo}), the effective velocity extracted from I_{on} (υ_{id}), and the effective velocity extracted from the transconductance (υ_{gmi}) were extracted for both Si and strained-$Si_{0.45}Ge_{0.55}$ channel devices. These velocity extraction methods were derived by A. Lochtefeld et al. and A. Khakifirooz [87][124][125]. In Figure 4.10 a depiction of the source to drain potential distribution is provided. The extracted velocities provide a measure of the velocity for carriers coming into the channel from the top of the source barrier. The extracted velocities are defined as follows,

$$\upsilon_{gmi} = \frac{g_{mi}}{WC_{inv}} \qquad \text{Equation 4.4}$$

and

$$\upsilon_{xo} = \frac{\upsilon}{1 - WC_{inv} R_S (1 + 2\delta)\upsilon} \qquad \text{Equation 4.5}$$

where

$$\upsilon_{id} = \frac{I_D}{\frac{V_{GS} - \Delta V_t}{W \int_0 C_{GSD}\, dV_{GS}}} \qquad \text{Equation 4.6}$$

and where I_D is the drain current, V_{GS} is the gate-to-source voltage, W is the device width, ΔV_t is the threshold voltage difference due to roll-off and DIBL at a given gate length, C_{gsd} is the gate-to-source/drain capacitance, g_{mi} is the intrinsic transconductance correcting for the source resistance [126], υ is the effective velocity of carriers ($\upsilon = I_D/WQ_{inv}$), C_{inv} is the gate capacitance at inversion, R_S is the source resistance which is assumed to be half of R_{SD}, and δ is the DIBL coefficient [87][125]. It should be noted that the average velocity (υ) is the same by definition as the effective velocity (υ_{id}).

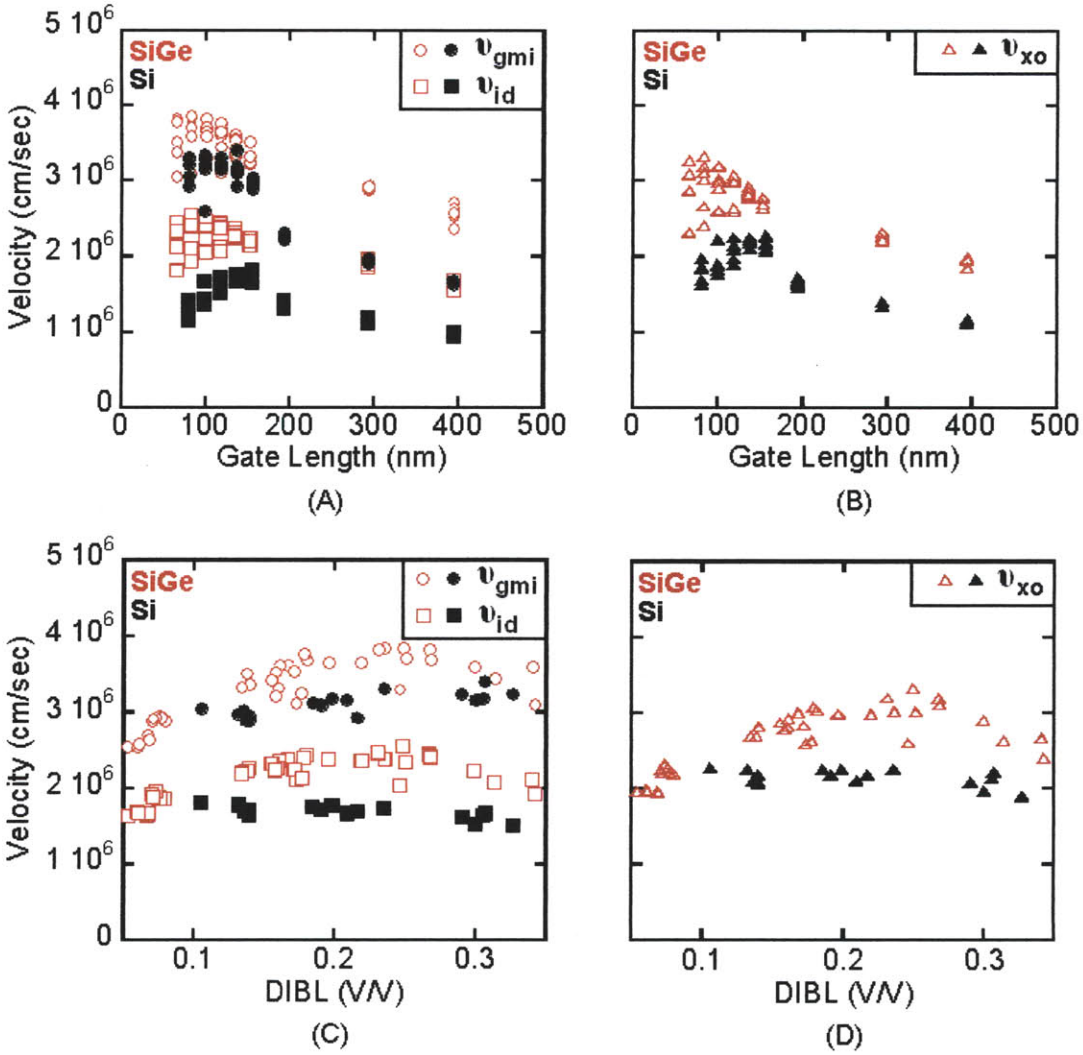


Figure 4.11 A comparison of (A) υ_{gmi} and υ_{id} vs. L_{Gate}, (B) υ_{xo} vs. L_{Gate}, (C) υ_{gmi} and υ_{id} vs. DIBL, and (D) υ_{xo} vs. DIBL between strained-$Si_{0.45}Ge_{0.55}$ (open symbols) and Si (closed symbols) control devices where V_{DS} = -1.5 V. The open symbols represent strained-SiGe channel devices while the closed symbols represent the Si control devices.

The velocities described in equations 4.4-4.6 were extracted from short channel biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ and relaxed-Si p-MOSFETs. The bias conditions at which υ_{id}, υ_{gmi}, and υ_{xo} were calculated correspond to the peak transconductance (g_m), where V_{DS} = -1.5V. The inversion charge density was estimated by integrating the C-V characteristics of large area MOSFETs. The inversion capacitance was also estimated from large area C-V characteristics.

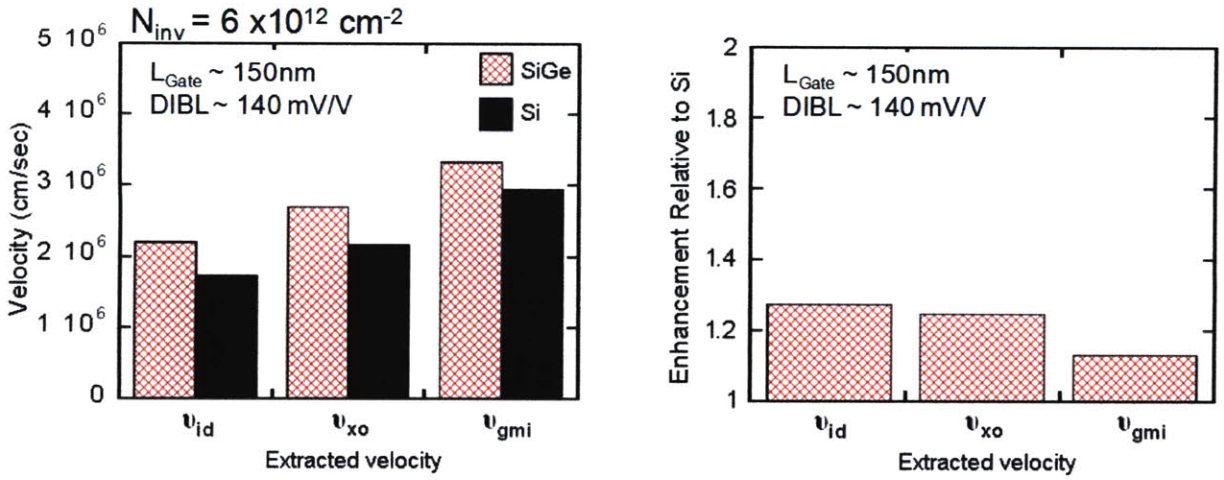


Figure 4.12 (a) A comparison of the average υ_{id}, υ_{gmi}, and υ_{xo} extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ and Si control devices examined here have an average L_{Gate} = 150 nm and DIBL = 140 mV/V. (b) The enhancement relative to the Si control for the average υ_{id}, υ_{gmi}, and υ_{xo} extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs exhibit an enhancement over Si control devices ranging from 1.13-1.27x. All devices have an average L_{Gate} = 150 nm and DIBL = 140 mV/V.

Corrections were made for V_t roll off and DIBL in estimating the inversion charge density and capacitance. The average gate overdrive at which υ_{id}, υ_{gmi}, and υ_{xo} were calculated is -1.4 V. This corresponds to an inversion charge density of about $6x10^{12}$ cm^{-2}. The calculated hole velocities are plotted in Figure 4.11(a) and 4.11(b) vs. gate length and in Fig. 4.11(c) and 4.11(d) vs. DIBL.

The reported velocities in Figure 4.11 are higher in biaxial compressive strained $Si_{0.45}Ge_{0.55}$ (55/0) channel p-MOSFETs than in the Si control devices. An error and sensitivity analysis of the extracted velocities is provided in appendix E. In Figure 4.11(a) and 4.11(b) the velocity increases as the gate length is scaled. The reported velocities are also consistently higher in strained $Si_{0.45}Ge_{0.55}$ than in Si across all gate lengths. The velocity's dependence on DIBL presented in Figure 4.11(c) and 4.11(d) is less dramatic when DIBL is greater than 0.1 V/V. A slight increase in velocity is observed as DIBL increases. Measurements and simulations performed by H. Hu et al. indicate that the carrier velocity is sensitive to the device parameters, some of which include gate

oxide thickness, source/drain junction depth, source/drain doping profile, DIBL, gate length, and the depletion region widths of the source/drain regions [127].

In Figure 4.12(a) a comparison of the extracted velocities is made between strained-$Si_{0.45}Ge_{0.55}$ and Si p-MOSFETs with similar DIBL, gate length, and inversion charge density values, 140 mV/V, 150 nm, and $6x10^{12}$ cm^{-2} respectively. Since the velocity is dependent on each of these parameters it is essential to make the velocity comparison when these parameters are of similar value. The velocities reported in Figure 4.12(a) are consistently higher in strained $Si_{0.45}Ge_{0.55}$ than in Si. The extracted virtual source velocity for the 150 nm long relaxed Si devices from this work are lower than the relaxed Si velocities reported in Figure 1.1 for state of the art Si p-MOSFETs also at 150 nm. The lower virtual source velocity may result from an increase in the source back scattering of holes from neutral defects at the source edge [122]. These defects would have been introduced during the extension implant. The mild activation anneal used during device fabrication (i.e. 5 seconds at 700°C) may not have been adequate enough to repair these defects. The relative hole velocity enhancement for short channel strained $Si_{0.45}Ge_{0.55}$ p-MOSFETs are plotted in Figure 4.12(b) for all velocity extraction methods. The enhancements relative to Si range from 1.1x to 1.25x. In Appendix E a sensitivity analysis is performed to gauge the sensitivity of the extracted velocity and enhancement ratio on the various extraction parameters (e.g. R_{SD} and DIBL). While the extracted velocities do express some sensitivity to these extraction parameters, the velocity enhancement provided with biaxial strained-$Si_{0.45}Ge_{0.55}$ remains modest in comparison to the 2.4x hole mobility enhancement observed in short channel strained $Si_{0.45}Ge_{0.55}$ devices.

In Chapter 2 the dependence of the ballistic velocity (υ_θ) on the carrier effective mass was discussed. Since the virtual source velocity (υ_θ) is related to the ballistic velocity (υ_{x0}) through the

ballistic efficiency (B), it also shares this dependence on the effective mass. In Figure 2.5 we saw that biaxial strain in Si and Ge is not very effective in reducing the carrier effective mass. This mild reduction in the effective mass should thus be expected to translate into a mild velocity improvement with biaxial strain, and indeed this is the result we see in Figure 4.12(b). The velocity characteristics in Si, SiGe, and Ge MOSFETs are strongly tied to changes in the effective mass, and therefore more ideal strain configurations which result in greater reductions in the effective mass are needed to observe a significant velocity increase. The results in Figure 4.12(b) suggest that biaxial strain is not an ideal strain configuration for improving the carrier velocity relative to relaxed Si. In the next section we will examine why. In fact, the velocity improvements seen in state-of-the-art uniaxial strained Si (2x [87]) relative to relaxed Si greatly exceed the enhancements observed here with biaxial strained $Si_{0.45}Ge_{0.55}$. (1.25x). In the next section we will discuss alternate strain configurations for increasing the carrier velocity in strained Si, SiGe, and Ge.

4.6 Hole velocity in asymmetrically strained SiGe p-MOSFETs

As mentioned previously, hole velocity is correlated to the carrier effective mass. Figure 2.4 provides the k•p simulated valence bands in the <110> direction for a variety of strain configurations. In Figures 2.4(f)-(h) applied uniaxial stress strongly warps the valence bands. This type of band deformation is favorable for reducing the carrier effective mass and increasing carrier velocity [48][123]. Velocity calculations performed by Uchida *et al.* and Antoniadis *et al.* indicate that uniaxial compressive stress when applied to (100) Si or Ge along the <110> direction is much more effective than biaxial compressive strain in increasing the carrier velocity [48][123]. However, these simulations only examine biaxial and uniaxial strain as individual and distinct strain configurations. In this section we will examine the velocity characteristics of

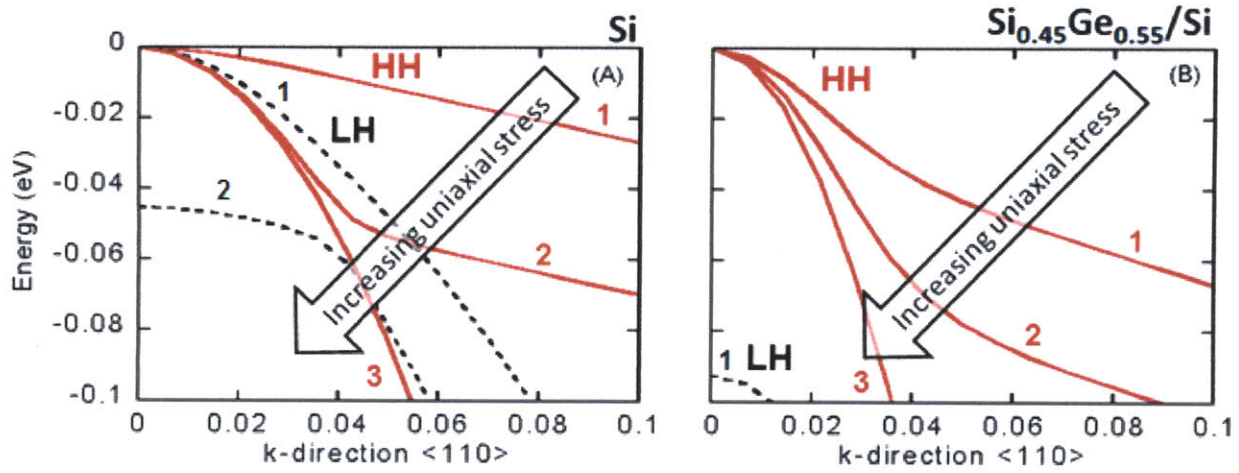


Figure 4.13 <110> E-k dispersion relation for (A) Si and (B) strained-$Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed-Si (55/0) with (1) 0, (2) -1, and (3) -3 GPa of uniaxial stress applied in the <110> direction. The solid lines represent the HH band and the dashed lines represent the LH band. The arrows indicate the direction of increasing uniaxial stress going from 0 to -3 GPa. The addition of uniaxial stress increases the curvature of HH band. Simulations were performed using *nextnano*[3] [30].

biaxial strained SiGe and Ge with an added uniaxial strain component in the <110> transport direction.

Figure 4.13 shows the E-k dispersion relations for relaxed-Si and biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ (55/0) with (1) 0 GPa, (2) -1 GPa, and (3) -3 GPa of additive uniaxial compressive stress in the <110> direction. As the additive uniaxial compressive stress in Si and biaxial strained-$Si_{0.45}Ge_{0.55}$ increases, the valence bands exhibit a higher degree of curvature near the valence band edge. This increase in curvature should translate into a reduction in the carrier effective mass. Since the degree of curvature is greater in strained-SiGe than in Si, a lower effective mass is expected for strained-SiGe and therefore a higher carrier velocity.

The ballistic velocity characteristics of these materials and a few others have been simulated to gauge the impact of additive uniaxial stress on the velocity performance of biaxial compressive strained-SiGe. Simulations were performed by calculating the 2D E-k dispersion

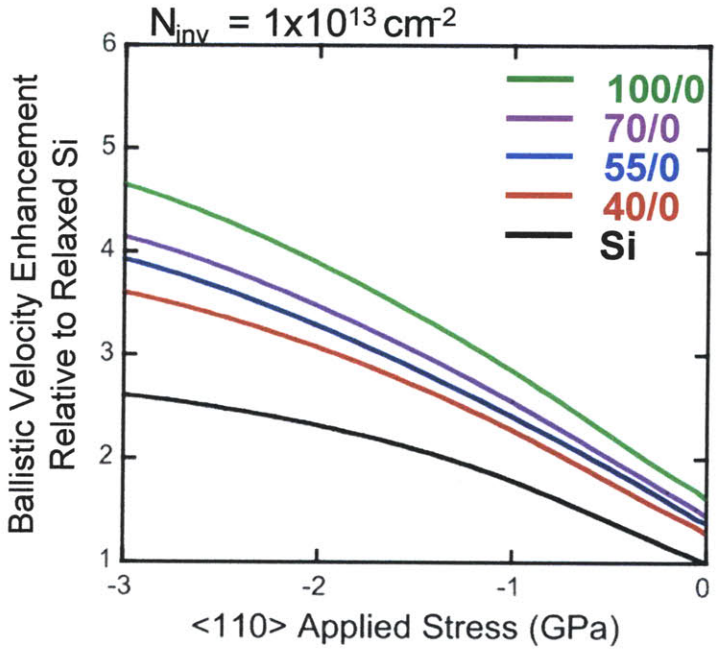


Figure 4.14 The simulated ballistic velocity enhancement relative to relaxed Si with applied compressive uniaxial stress for Si, biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ pseudomorphic to relaxed-Si (40/0), biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed-Si (55/0), biaxial compressive strained-$Si_{0.3}Ge_{0.7}$ pseudomorphic to relaxed-Si (70/0), and biaxial compressive strained-Ge pseudomorphic to relaxed-Si (100/0). Simulations were performed using *nextnano*[3] and FETtoy [30][128].

relation using *nextnano*[3] [30]. The simulated band structure was used as an input to FETtoy which calculates the ballistic current [128]. The calculated ballistic current and Q_{inv} were used to determine the ballistic velocity (υ_θ) according to $\upsilon_\theta = I_{ballistic}/WQ_{inv}$. In Figure 4.14 the simulated ballistic velocity enhancement relative to relaxed Si is provided for Si, biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ pseudomorphic to relaxed-Si (40/0), biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed-Si (55/0), biaxial compressive strained-$Si_{0.3}Ge_{0.7}$ pseudomorphic to relaxed-Si (70/0) and biaxial compressive strained-Ge pseudomorphic to relaxed-Si (100/0) all with an additive <110> uniaxial stress component ranging from 0 GPa to -3 GPa.

First let us examine the curves where the uniaxial compressive strain component in the <110> direction is zero. The ballistic velocity enhancements are quite modest for the 40/0, 55/0,

70/0, and 100/0 channel devices with no added <110> stress. Since the virtual source velocity (υ_{xo}) is related to the ballistic velocity (υ_{θ}) through the ballistic efficiency, a comparison of the relative change in υ_{xo} and υ_{θ} velocities is valid assuming the ballistic efficiency doesn't change as well. The calculated ballistic velocity enhancement for 55/0 with no applied uniaxial strain is approximately 1.4x, which is comparable to the measured virtual source velocity enhancement for this material which is approximately 1.25x. The agreement between the simulated and measured relative velocity enhancement lends some confidence to this simulation approach.

In Figure 4.14 we see that by adding a uniaxial compressive stress component in the <110> direction we can significantly increase the ballistic velocity enhancement relative to relaxed Si. In state-of-the-art Si p-MOSFETs which have about -1 GPa of uniaxial compressive channel stress in the channel, the virtual source velocity enhancement has been measured to be about 2x [87]. This is also comparable to the calculated value in Figure 4.14, which is approximately 1.8x. From the simulated result we see that the velocity enhancement in Si will saturate with increasing uniaxial stress. This predicts a fundamental limit in the performance gains that can be obtained from a Si channel. Fortunately though, more substantial velocity gains are predicted with the incorporation of Ge into the channel and the application of compressive uniaxial stress in the <110> direction. A 55/0 p-MOSFET with -1 GPa of uniaxial compressive stress is predicted to provide a 2.5x velocity enhancement over Si. This enhancement factor increases to 3x when the channel Ge content increases to 100% and the uniaxial stress is held constant at -1 GPa. These simulations suggest that the enhancement factors can be pushed even higher with the incorporation of more stress into the channel.

4.7 Summary and conclusions

Biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs with gate lengths down to 65 nm were fabricated to explore the merits of a strained-$Si_{0.45}Ge_{0.55}$ channel. Care was taken to avoid process steps that might alter or eliminate the strain in the channel. Hole mobility and velocity were extracted and benchmarked against comparable Si control devices. Devices with gate lengths in the range of 65-150nm are observed to exhibit a 2.4x hole effective mobility enhancement over the Si control mobility. While a slight drop in mobility is observed as the gate length is reduced the observed mobility enhancement is still substantial. Three velocity extraction methods were employed and the velocity characteristics of scaled strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs have been documented. A modest 1.25x velocity enhancement is observed in biaxial compressive stained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs over control devices with a similar gate length and DIBL. While biaxial compressive strain in SiGe is beneficial in providing a substantial mobility enhancement, it does not prove to be as beneficial to the carrier velocity. Band structure and ballistic velocity calculations indicate that a substantial enhancement in velocity can be expected with the incorporation of Ge into the channel and the addition of uniaxial stress. While the velocity enhancement provided by uniaxial compressive stress in Si is expected to saturate at about 2.7x relative to relaxed Si, simulations predict that a strained-$Si_{0.45}Ge_{0.55}$ channel will outperform relaxed Si by 4.3x with -3 GPa of uniaxial compressive channel stress. Moving to a pure Ge channel is predicted to provide a slightly higher performance gain at 5.2x, again with -3 GPa of uniaxial compressive channel stress. This suggests that even moderate amounts of Ge incorporated into the channel and combined with uniaxial compressive stress can provide a significant velocity enhancement over relaxed Si channel p-MOSFETs. This result is quite promising and indicates that combing uniaxial strain

with even moderate amounts of Ge in the channel, which eases integration issues relative to pure Ge, may provide substantial velocity improvement relative to a relaxed Si channel p-MOSFET.

Chapter 5

HOLE MOBILITY IN ASYMMETRICALLY STRAINED SIGE-CHANNEL P-MOSFETS

5.1 Introduction

Exceptionally high hole mobility gains have been observed in biaxial compressive strained-SiGe relative to relaxed-Si. Over a 10x hole mobility enhancement relative to relaxed-Si has been measured for biaxial compressive strained-Ge channel p-MOSFETs pseudomorphic to relaxed-$Si_{0.5}Ge_{0.5}$ [63]. The hole mobility improvement observed in biaxial compressive strained-SiGe stems from a mild reduction in the hole effective mass and strong suppression of phonon scattering [48][75][129]. While the hole mobility characteristics of biaxial compressive strained SiGe are impressive the velocity characteristics are more modest. The simulation results presented in the previous chapter predict that the velocity characteristics of biaxial strained SiGe will improve with the addition of <110> strain. Added <110> produces a more significant reduction in the hole effective mass than biaxial strain. Both the hole effective mobility and velocity should benefit from this mass reduction. To date, there are no experimental reports examining the transport impact of combining biaxial and additive uniaxial compressive strain in high-Ge content strained-SiGe channel devices. Existing work is limited to low Ge content devices with small amounts of in-plane biaxial compressive strain [130].

In this chapter, the hole mobility characteristics of high-Ge content biaxial compressive strained-SiGe p-MOSFETs with additive uniaxial strain are examined. Since hole mobility and

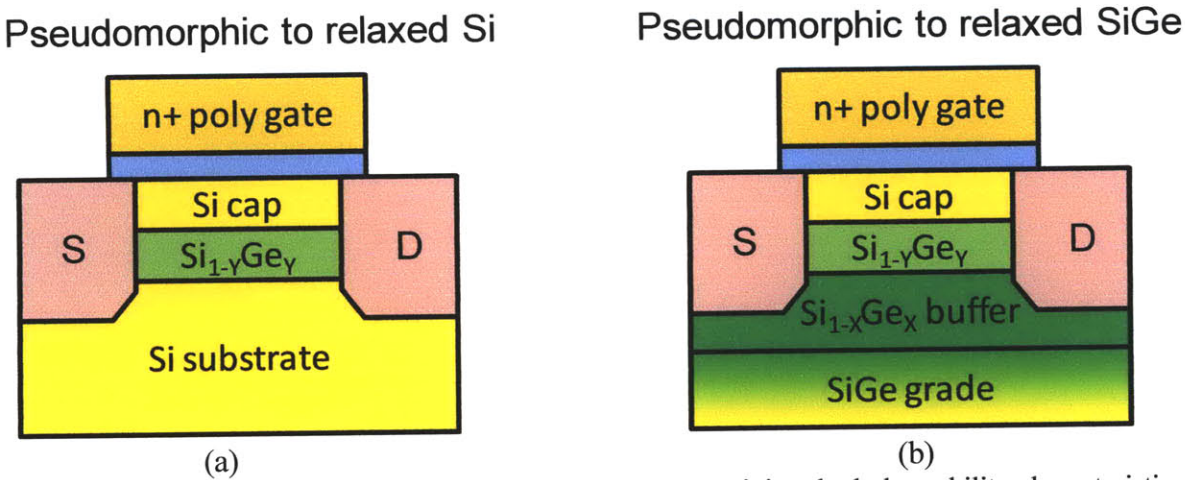


Figure 5.1 The strained-SiGe p-MOSFET structures used in examining the hole mobility characteristics of biaxial compressive strained-SiGe with added <110> uniaxial compressive strain. (a) Strained-$Si_{1-y}Ge_y$ pseudomorphic to relaxed-Si and (b) strained-$Si_{1-y}Ge_y$ pseudomorphic to relaxed-$Si_{1-x}Ge_x$ are the two channel structures used to introduce biaxial compressive strain into the buried $Si_{1-y}Ge_y$ channel.

velocity are correlated through their dependence on effective mass, a mass driven change in mobility is expected to result in a corresponding change in velocity. Due the mass dependence of both carrier velocity and mobility the correlation between the two follows a power law dependence: $\upsilon_\theta = \mu^\alpha$ where, $\alpha \approx 0.5$ when the mobility increase is purely due to an increase in effective mass [87][124]. When the mobility increase involves scattering, mobility and velocity are more weakly correlated, where $\alpha < 0.5$. In this chapter we will explore the hole mobility characteristics of biaxial compressive strained-SiGe with added <110> strain and attempt to determine if the change in mobility is solely a mass driven phenomenon or due in part to changes in scattering. This will be helpful in evaluating the merits of combining biaxial compressive strain with added <110> longitudinal compressive strain for the purpose of increasing carrier velocity in short channel devices.

Device Structure	Epi number	Channel Ge %	Substrate Ge %	Biaxial Compressive Strain
100/40	4583	100 %	40 %	-2.4 %
63/0	4530	63 %	0 %	-2.6 %
58/30	2778	58 %	30 %	-1.1 %
43/0	4515	43 %	0 %	-1.8 %
42/30	2775	42 %	30 %	-0.5 %
Si control	4540	0 %	0 %	0 %

Table 5.1 The device structures used in examining the hole mobility characteristics of asymmetrically strained-$Si_{1-y}Ge_y$. The Y/X notation is used to indicate the channel Ge fraction and provide information on the amount of biaxial compressive strain present in the channel. Device structure with nominally $Si_{0.6}Ge_{0.4}$, $Si_{0.4}Ge_{0.6}$, and pure Ge channels were used.

5.2 Biaxial strained SiGe p-MOSFETs with added uniaxial strain

Uniaxial longitudinal compressive strain was applied mechanically to <110>/(100) oriented biaxial compressive strained SiGe p-MOSFETs. The devices examined in this chapter and illustrate in Figure 5.1 were fabricated by Cait Ni Chléirigh [26]. The channel structure consists of a Si cap (2 to 3 nm) and a buried strained-SiGe channel (5 to 15nm). The channel was phosphorus doped with a nominal concentration of $1x10^{17}$ cm^{-3}. The channel doping was consistent across all devices making the vertical field profiles similar. The gate oxide thickness is 3.5nm in all a cases except for the Ge-channel device where it is 11nm. The maximum thermal budget was the source drain activation anneal which was 10 seconds at 800°C for strained Ge channel compositions up to 70%, and 10 seconds at 650°C for strained Ge channels. A complete description of the device

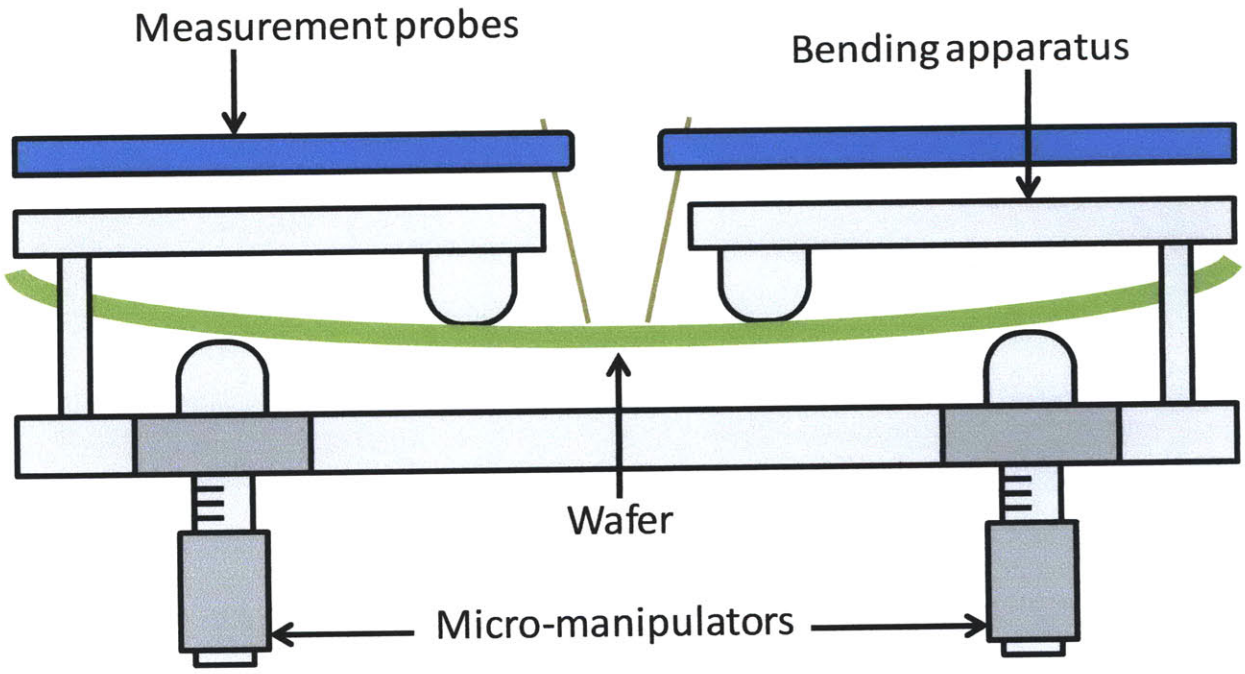
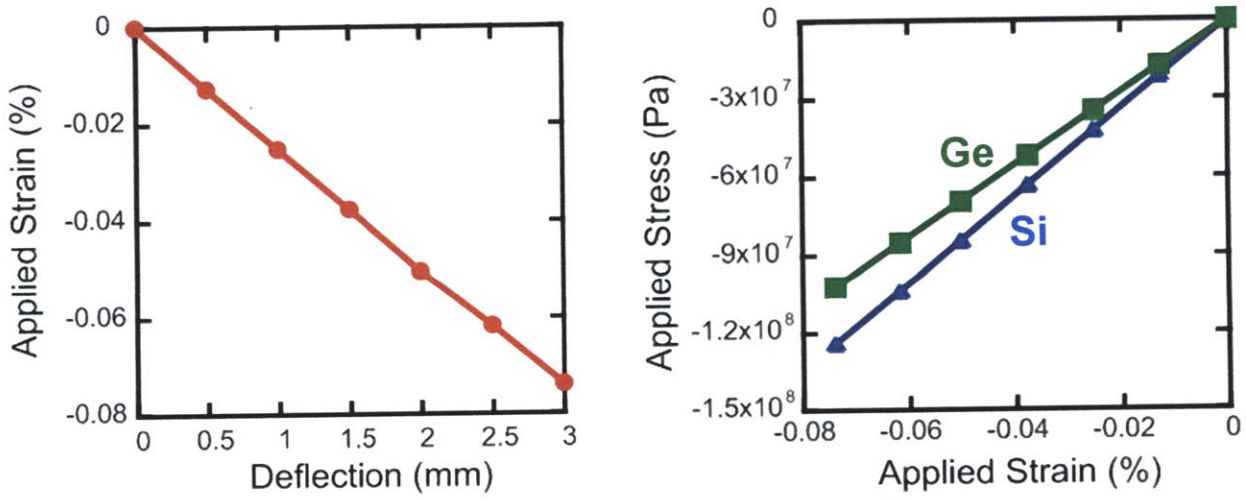


Figure 5.2 The bending apparatus used in this work to introduce <110> uniaxial compressive strain into biaxial compressive strained-SiGe channel p-MOSFETs. The micro-manipulators are used to adjust the sample deflection and strain the sample.



(a) (b)

Figure 5.3 (a) The measured strain in the sample as a function of the micromanipulator deflection. The sample strain was measured using a strain gauge adhered to the wafer backside. (b) The applied stress in the wafer for Si and Ge. Approximately 100 MPa of <110> uniaxial compressive stress can be applied with the bending apparatus depicted above.

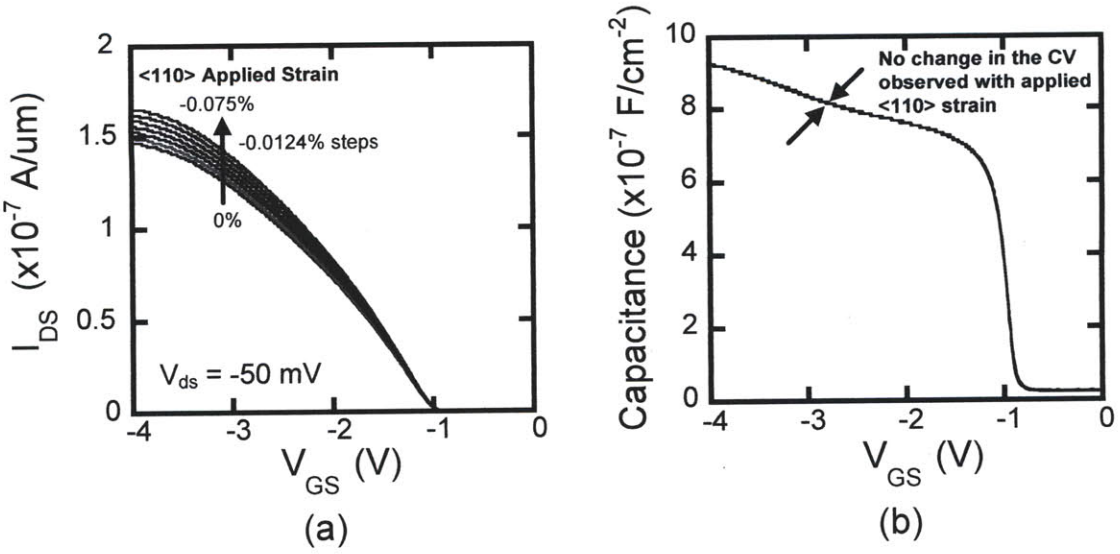


Figure 5.4 (a) Transfer characteristics for a 43/0 p-MOSFET with applied <110> longitudinal uniaxial compressive strain. The arrows indicate the direction of increasing uniaxial strain starting from 0% strain at the lowest curve and increasing in 0.0124% increments. (b) The C-V characteristics with applied strain for the same 43/0 p-MOSFET in (a). The seven C-V curves overlay, which indicates no change in inversion charge density or distribution with applied <110> uniaxial compressive strain.

fabrication process is described in [131] for devices on Si substrates and in [132] for those on SiGe virtual substrates. The biaxial compressive strain present in the strained-$Si_{1-y}Ge_y$ channel varies depending upon the Ge composition of the relaxed-$Si_{1-x}Ge_x$ substrate, where $0 < y < 1$ and $0 < x < 0.4$ in this study. Table 1 summarizes the device structures examined in this work and indicates the calculated levels of biaxial compressive strain present in the channel. The Y/X notation is utilized to indicate the channel (Y) and virtual substrate (X) Ge compositions respectively. The channel Ge composition was determined by either Secondary Ion Mass Spectroscopy (SIMS) or Rutherford Back Scattering (RBS) after device processing. The measured channel Ge compositions are comparable to the targeted values, 40%, 60%, and 100% suggesting minimal strain relaxation via inter-diffusion. The channel strain reported in Table 1 was calculated from the relation $\varepsilon = 1 - a_y/a_x$, where a_y and a_x are the $Si_{1-y}Ge_y$ and $Si_{1-x}Ge_x$ lattice constants in the channel and virtual substrate

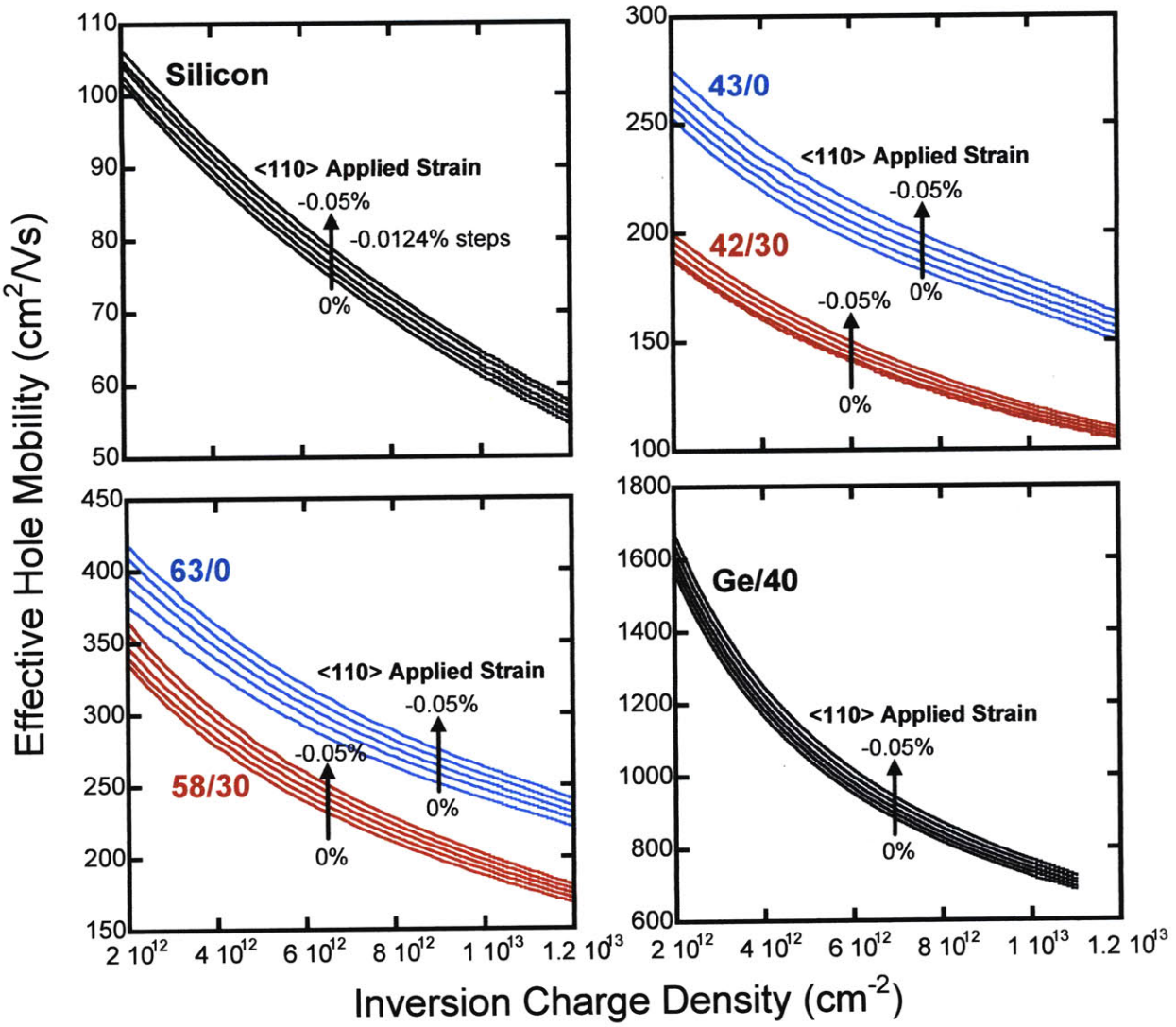


Figure 5.5 Effective hole mobility curves for Si, 43/0, 42/30, 63/0, 58/30, and 100/40 MOSFETs for various values of applied <110> longitudinal uniaxial compressive strain. The arrows indicate the direction of increasing uniaxial compressive strain starting from 0% strain at the lowest curve and increasing in 0.0124% increments.

respectively. Additive <110> uniaxial strain was applied using a mechanical bending apparatus. The bending apparatus used is illustrated in Figure 5.2. The level of applied mechanical strain was measured using a commercial strain gauge adhered to the wafer backside. Gauge measurements indicate that up to about -0.07% strain can be applied to the device using this bending apparatus. The measured strain versus sample deflection and stress versus strain curves for Si and Ge are

provided in Figure 5.3a and 5.3b respectively. The Young's modulus used for Si is 168 GPa and for Ge is 138 GPa. These values were taken from [130].

The mobility extraction MOSFET structure illustrated in Figure 3.12 was utilized to extract the effective mobility independent of the extrinsic parasitic resistance [71]. The device gate length is 100 μm and width is 15 μm. The effective hole mobility was extracted using the transfer (I_{DS}-V_{GS}) and capacitance-voltage (C-V) characteristics measured on each device as uniaxial strain was applied, Figure 5.4. An increase in on-current is observed with increasing longitudinal uniaxial compressive strain. No change in the threshold voltage or C_{max} was observed with applied strain. This indicates that the observed change in current stems from a change in the effective hole mobility and that carrier confinement in the strained $Si_{1-x}Ge_x$ channel doesn't change with the small amounts of applied strain. The hole mobility curves for some of the devices in Table 1 are plotted in Figure 5.5. The arrows indicate the direction of increasing applied mechanical strain. In Figure 5.6 the relative mobility enhancements at an inversion charge density of $N_{inv} = 4x10^{12}$ cm^{-2}. The carrier density at which the mobility enhancement comparison is made corresponds to an approximate gate to source voltage of -1.9 V in Figure 5.5. This bias point is in the plateau region of the C-V characteristics indicating that carriers predominantly occupy the buried SiGe channel [10][40][131].

5.3 Hole mobility in strained SiGe p-MOSFET under mechanical strain

It is interesting to see that the substantial hole mobility enhancement provided by biaxial compressive strained-SiGe relative to relaxed Si continues to increase with the application of <110> uniaxial compressive strain. Also worth noting is that the relative change in mobility for biaxial compressive strained-SiGe devices is larger than that of Si. Figure 5.6 shows that the hole mobility in biaxial compressive strained-SiGe (e.g. 43/0, 42/30, 63/0, 58/30 and 100/40)

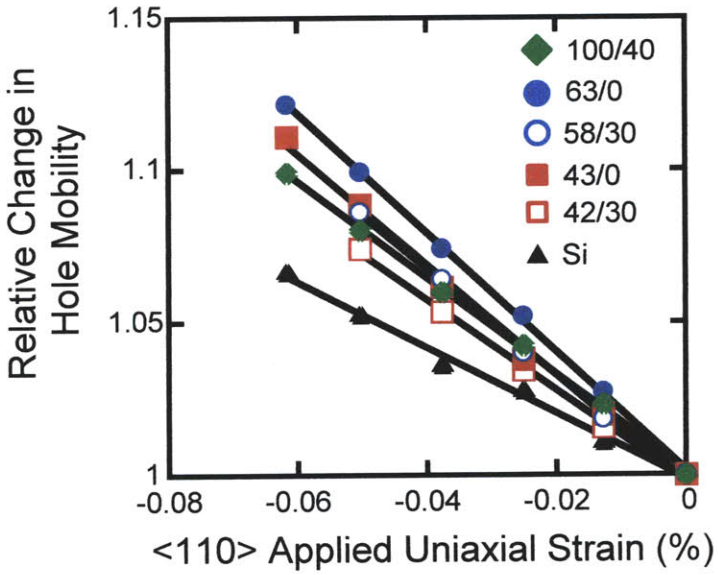


Figure 5.6 The relative mobility enhancement for the devices in Table 1 with applied <110> uniaxial compressive strain. Si, 43/0, 63/0, and 100/40 MOSFETs are represented by the closed symbols while the open symbols represent the results for 58/30 and 42/30 MOSFETs.

expresses a greater sensitivity to applied uniaxial strain than Si. The sensitivity to applied uniaxial mechanical strain increases as the amount of biaxial compressive strain in the channel increases. The longitudinal piezoresistance coefficients were extracted in accordance with $\mu/\mu_o = -(\pi_L\sigma_L + \pi_T\sigma_T)$ from [130], where μ/μ_o is the relative change in mobility with applied stress (σ). The longitudinal piezoresistance coefficients (π_L) are plotted as a function of biaxial strain in Figure 5.7 to better examine the biaxial strain dependence. The piezoresistance coefficients for relaxed Si, Ge, and SOI reported by O. Weber in [130] are also plotted for comparison. The longitudinal piezoresistance coefficients for Si and Ge have also been extracted by C.S. Smith and are reported in [138]. The longitudinal piezoresistance coefficients in Figure 5.7 are grouped according to the nominal channel Ge composition (i.e. Si, $Si_{0.6}Ge_{0.4}$, $Si_{0.4}Ge_{0.6}$, and Ge). The piezoresistance coefficients appear to be correlated to the initial biaxial compressive strain in the channel. As the channel biaxial strain increases a substantial rise in π_L is observed. This effect

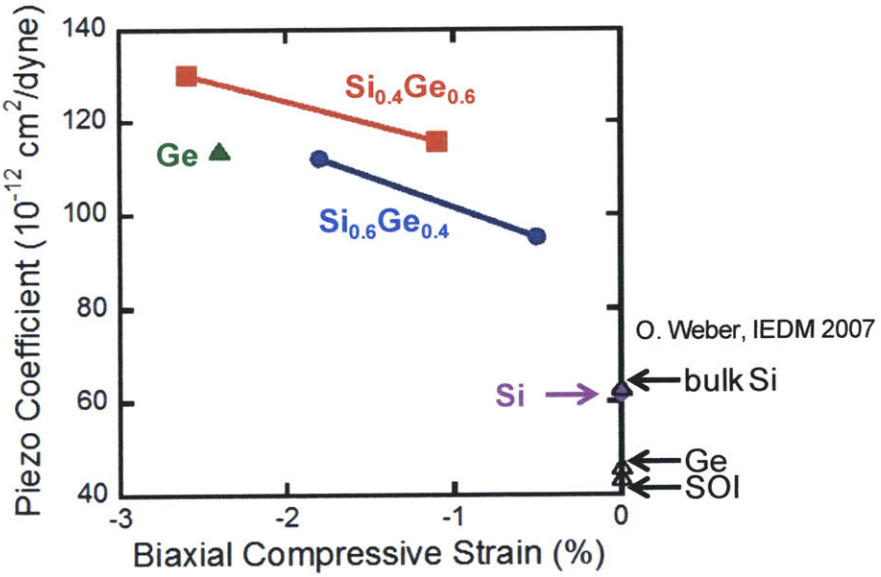


Figure 5.7 Longitudinal piezoresistance coefficients plotted as a function of biaxial compressive strain. The nominal channel material for the MOSFETs examined in this work are indicated on the plot (solid symbols). Piezoresistance coefficients for relaxed bulk Si, Ge, and SOI reported by O. Weber in [60] are also plotted (open symbols).

though does not appear to be directly correlated to the channel Ge fraction. The piezoresistance coefficients increase as the nominal channel Ge composition increases from 40% to 60%, but then decreases when the channel Ge composition reaches 100%. Measurements of the transverse piezoresistance coefficients (π_T) are discussed in Appendix D, and show a dependence on biaxial strain which reflects the behavior observed in the longitudinal piezoresistance coefficients. The longitudinal piezoresistance coefficients for strained $Si_{0.7}Ge_{0.3}$ and Si have been reported in [137]. The longitudinal piezoresistance coefficient reported for Si in [137] is larger than what is reported in Figure 5.7, and the strained $Si_{0.7}Ge_{0.3}$ coefficient is comparable to the value reported for the higher Ge content strained SiGe result in this work. The reported piezoresistance coefficients vary greatly from source to source and the reason for this is not yet understood. Differences in the substrate and device structure between these experiments may lead to

differences in the amount of substrate stain that gets transferred into the channel of the device, but this has yet to be confirmed.

In relaxed Si and Ge, small amounts of applied uniaxial strain (i.e. less than 500 MPa) provide an increase in mobility that is driven by a reduction in the carrier effective mass more so than a modulation in the scattering characteristics [48][60]. The hole mobility in biaxial compressive strained SiGe and Ge exhibits a greater sensitivity to applied mechanical strain than relaxed Si or Ge. This suggests that either a larger reduction in the hole effective mass is occurring in the initially biaxial strained material or that the hole mobility is also benefiting from a reduction in scattering (e.g. phonon or alloy scattering). Further analysis is provided in the following section.

5.4 Hole transport analysis in asymmetrically strained SiGe p-MOSFETs

While the impact of purely uniaxial or biaxial strain on the valence band structure of Si, SiGe, and Ge has been studied extensively [48][59-61][75][133], the effects of combining biaxial compressive strain with added uniaxial strain have received less attention. To date, there are no theoretical reports examining the transport impact of combining biaxial and additive uniaxial compressive strain in high-Ge content strained-SiGe channel devices. Existing experimental work is limited to examining the piezoresistance coefficients of low Ge content devices with small amounts of in-plane biaxial compressive strain [60]. In this section we will attempt to develop an understand of how the hole mobility in biaxial compressive strained SiGe is impacted by the addition of a <110> uniaxial strain component. To do so we must first examine how the valence band structure of bulk biaxial compressive strained SiGe and Ge changes with applied uniaxial strain. This is essential since strain induced modulations in the valence band structure of Si, SiGe, and Ge can lead to changes in carrier effective mass and scattering characteristics.

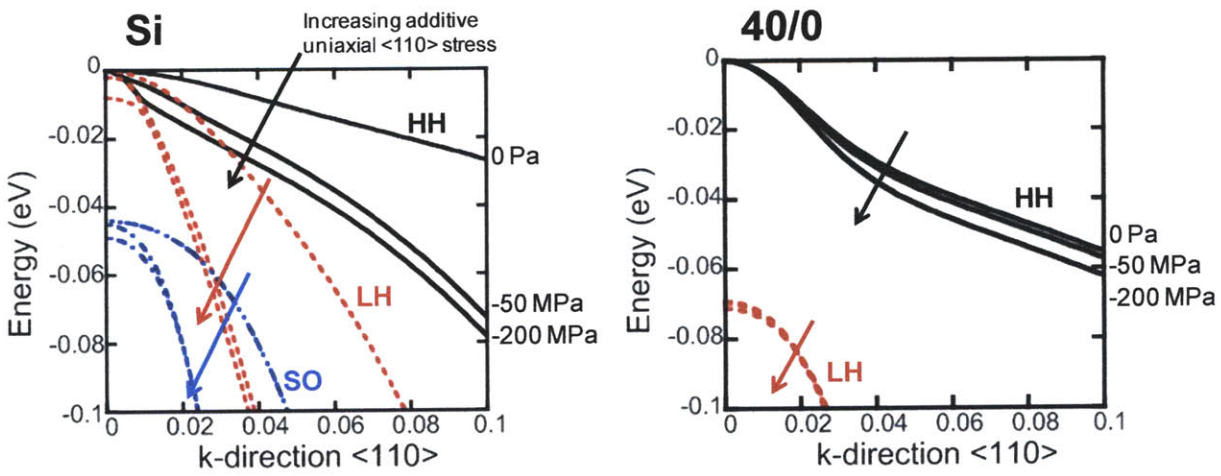


Figure 5.8 The E-k dispersion relations for Si and 40/0 strained-$Si_{0.6}Ge_{0.4}$ with added compressive stress in the <110> direction (i.e. 0 Pa, -50 MPa, and -200 MPa of <110> added stress). The arrows indicate the direction of increasing <110> compressive stress. The heavy hole (HH) band is plotted in black, light hole band in red, and the split off band in blue. The valence band structure was calculated using the 6x6 k·p method in nextnano3 [30] with the Luttinger parameters provided in [75].

According to the Drude model for carrier mobility (equation 2.3), the hole mobility is governed by the carrier effective mass and scattering characteristics. Therefore the change in hole mobility observed with applied uniaxial strain in Figure 5.6 is derived from a change in the carrier effective mass and/or a change in the hole scattering characteristics. First we will try to quantify the extent to which the hole effective mass changes with applied uniaxial strain and see if the change in hole mobility with applied uniaxial strain is solely a mass driven phenomenon.

In Figure 5.8 the bulk heavy hole (HH), light hole (LH), and split off (SO) valence bands are plotted for Si and biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ pseudomorphic to relaxed-Si (40/0), both with small amount of added <110> uniaxial compressive stress (i.e. 0 MPa, 50 MPa, and 200 MPa of added uniaxial compressive stress). The simulated stress values are comparable to the levels of stress added during the mechanical bending experiments described in the previous section. The valence band dispersion relations were calculated using the 6x6 k·p method in

nextnano^3 [30]. In Figure 5.8 we see that both sets of bands exhibit some deformation in the presence of added uniaxial compressive stress, yet it is Si that exhibits a greater degree of change. Let us recall from equation 2.4 that the carrier effective mass is a function of the amount of curvature present in the band. The increased curvature/sharpening of the valence bands in Si and 40/0 strained-SiGe suggests that a reduction in the carrier effective mass should occur with the application of small amounts of <110> uniaxial compressive stress. To quantify the extent to which the effective mass changes both the HH and LH effective mass have been extracted. The SO mass will be ignored in this analysis since a relatively small portion of carriers in the MOS hole inversion layer reside in this band. While the curvature mass is typically used in defining the transport mass, it is difficult to do so in the context of the valence band structure of strained Si, SiGe, and Ge due to the highly non-parabolic nature of the bands. Attempting to extract the curvature mass at kT/q from the band edge of the HH band in 40/0 strained-SiGe results in an unrealistically large effective mass value. This is due to the inflection point present near kT/q. The Density of States (DOS) effective mass has been extracted instead to bypass this issue. The difficulty of defining a "curvature" mass for holes in the context of the highly non-parabolic valence bands of Si, SiGe, and Ge has been acknowledged by Fischetti et al. [75]. Instead Fischetti adopts the DOS mass in an attempt to gauge the impact of strain and Ge content on the hole effective mass. In this work a more simplified DOS mass calculation is used. The DOS mass relation is given by

$$\left(\frac{m^*}{m_o^*}\right)^{3/2} = \pi^{-3/2}\int \exp\left(\frac{E(x)}{K_B T}\right)dx \qquad \text{Equation 5.1}$$

where E(x) is the valence band energy in k-space given in terms of x [134], which is given by

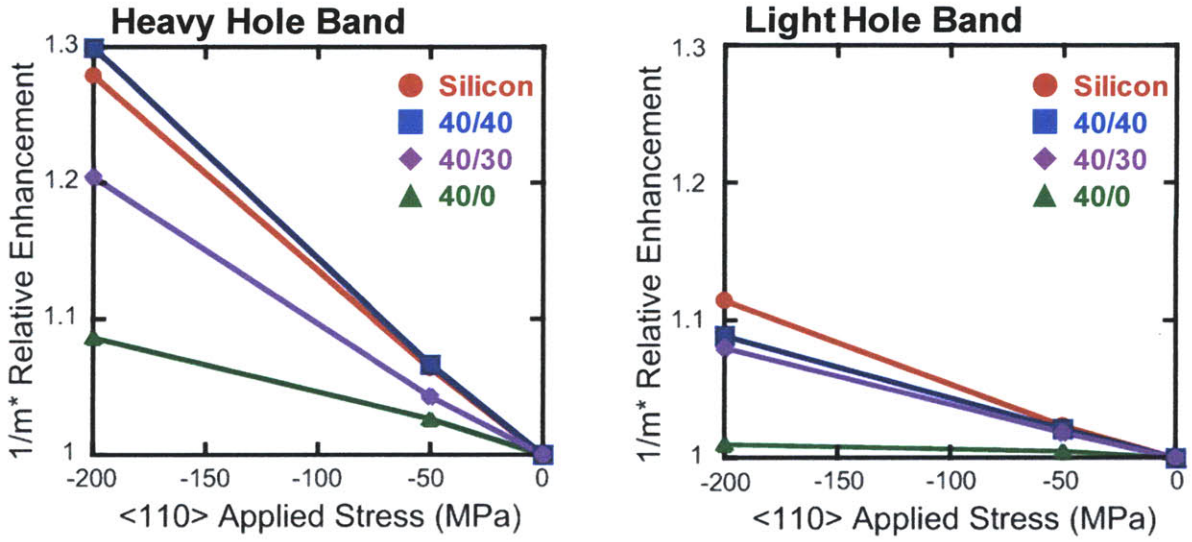


Figure 5.9 The relative change in heavy hole (HH) and light hole (LH) inverse effective mass in Si, 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, 40/30 strained-$Si_{0.6}Ge_{0.4}$, and 40/0 strained-$Si_{0.6}Ge_{0.4}$ with added <110> compressive stress.

$$x = \frac{\hbar k}{(2 m_o K_B T)^{1/2}} \qquad \text{Equation 5.2}$$

In calculating the DOS effective mass the HH and LH bands are first simulated using the 6x6 k·p method in nextnano3. The bands are then integrated along the <110> direction up to an energy of kT/q from the band edge.

In Figure 5.9 the relative change in the HH and LH inverse effective mass with applied <110> uniaxial compressive stress is plotted for Si, 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, 40/30 strained-$Si_{0.6}Ge_{0.4}$, and 40/0 strained-$Si_{0.6}Ge_{0.4}$. A reduction in the HH and LH effective mass is seen with the addition of <110> uniaxial compressive stress for all the simulated cases. The simulated mass response to applied <110> stress exhibits a dependence on the amount of in-plane biaxial compressive strain present in the material. The simulated cases without in-plane biaxial compressive strain (i.e. Si and 40/40 relaxed-$Si_{0.6}Ge_{0.4}$), experience the largest mass

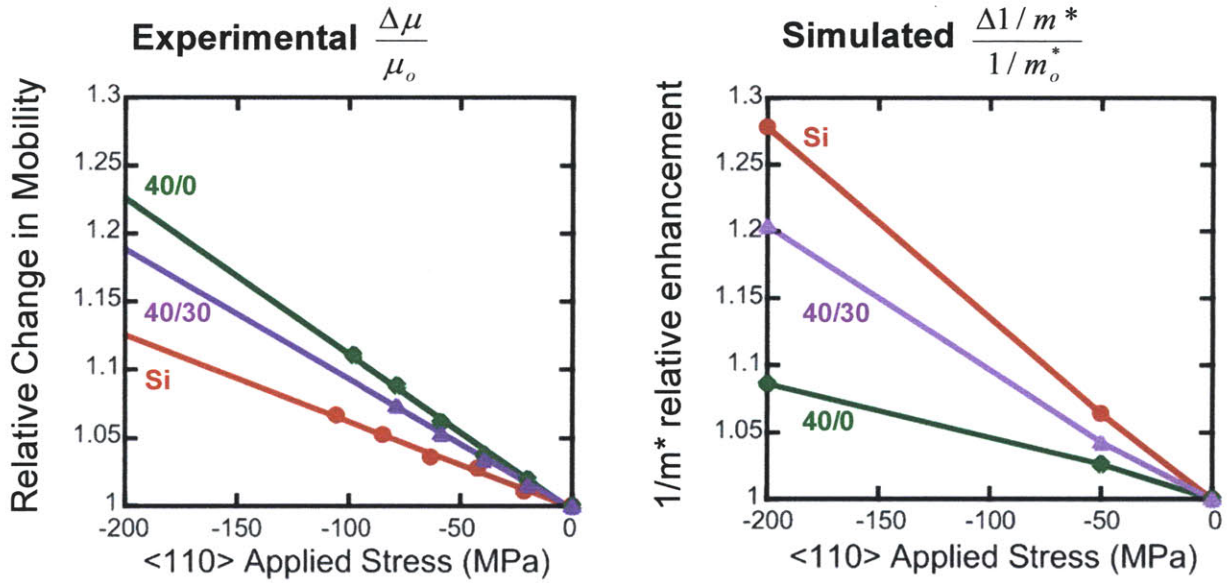


Figure 5.10 A comparison between the measured relative change in mobility and calculated relative change in the inverse effective mass for Si, 40/30 strained-$Si_{0.6}Ge_{0.4}$, and 40/0 strained-$Si_{0.6}Ge_{0.4}$ with added <110> uniaxial compressive stress.

change with added <110> stress. For the materials with initial in-plane biaxial compressive strain (i.e. 40/30 and 40/0 strained-$Si_{0.6}Ge_{0.4}$), the effective mass change with added <110> stress is smaller. This may be due to that fact that in-plane biaxial compressive strain already introduces a great deal of band warping in the HH and LH valence bands, and the addition of a small <110> stress component does little to further warp the bands.

In Figure 5.10 the simulated effective mass is compared to the measured hole mobility change with added <110> stress. Recall that the measured hole mobility in biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ (i.e. 40/0 and 40/30) expresses a greater sensitivity to added <110> strain than Si. The simulated effective mass response to added uniaxial stress exhibits the opposite trend where biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ (i.e. 40/0 and 40/30) shows a weaker sensitivity to added <110> strain than Si. The simulated result suggests that the hole mobility increase in biaxial compressive strained SiGe may also be driven by changes in the hole scattering

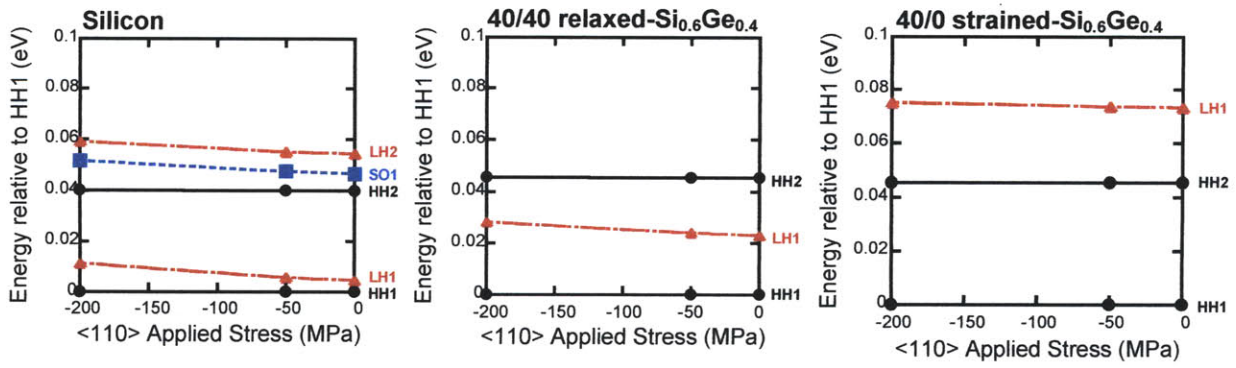


Figure 5.11 The subband structure for Si, 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, and 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ with added <110> stress, calculated using nextnano^3 [30]. The 6x6 k·p method is used to calculate the multi-band Schrodinger-Poisson solution in a 1 mV/cm triangular potential well. All subbands up to 0.1 eV from the first HH subband are plotted for each material system.

characteristics in addition to a change in the hole effective mass.

The increase in hole mobility of Si with small amounts of applied <110> stress (i.e. up to 500 MPa) is attributed to a change in the hole effective mass [59-61]. Calculations of the hole scattering characteristics performed by Thompson et al. for Si p-MOSFETs with applied <110> stress suggest that acoustic phonon, optical phonon, and surface roughness scattering have a negligible dependence on applied <110> stress (for stress values up to 500 MPa) [59-61]. The scattering characteristics of biaxial compressive strain SiGe with added <110> stress have received little attention.

The subband structure of Si, 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, and 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ have been simulated to develop some insight into how the scattering characteristics of biaxial compressive strained SiGe may be modulated by the presence of an added <110> stress component. The subband structure for Si, 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, and 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ with added <110> stress were calculated using nextnano^3. The 6x6 kp method is used to calculate the multi-band Schrodinger-Poisson solution in a 1

mV/cm triangular potential well. This approach calculates the eigenstates (i.e. subbands) corresponding to the HH, LH, and SO bands in the triangular well. The triangular well profile is meant to emulate the potential profile in the inversion layer of an MOS structure. In Figure 5.11 all subbands up to 0.1 eV from the first HH subband are plotted for Si, 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, and 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ as a function of added <110> stress. These simulations show little modulation in the subband position with added <110> stress. The change in subband position is about 5 meV with -200 MPa of added <110> compressive stress for all simulated cases. Recall that in Si, no change in the phonon or surface roughness scattering characteristics is expected in this low stress regime. This is in part due to the fact that the subband positions are not significantly modulated with the addition of small amounts of <110> compressive stress. In 40/40 relaxed-$Si_{0.6}Ge_{0.4}$, and 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ the relative position of the subbands does not change dramatically with added <110> stress either. This may be an indicator that the phonon scattering characteristics in these materials doesn't change much in the low stress regime. Comparing the subband structures of 40/40 relaxed-$Si_{0.6}Ge_{0.4}$ and 40/0 biaxial compressive strained-$Si_{0.6}Ge_{0.4}$ we see that the biaxial strain induced subband splitting in 40/0 strained-$Si_{0.6}Ge_{0.4}$ separates out the first LH band from the first two HH bands. Strain induced subband splitting dramatic reduces inter-subband phonon scattering. The large hole mobilities reported in biaxial compressive strained SiGe are mostly driven by this phenomenon [26][39-45][56-62]. This lends to the thought that a modulation in phonon scattering is not supplementing the change in effective mass with added <110> stress to produce a larger relative change in mobility for biaxial strained-SiGe over Si.

To explain the larger relative change in mobility observed in biaxial compressive strained-SiGe it may be necessary to look to other scattering mechanisms that may be changing

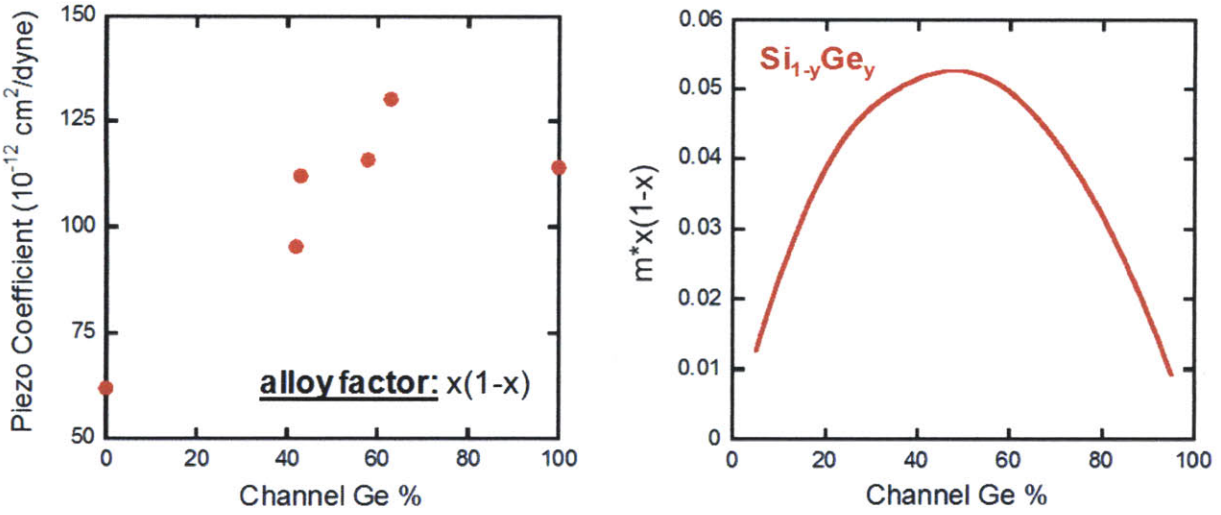


Figure 5.12 (a) The <110> longitudinal piezoresistance coefficients as a function of channel Ge% in $Si_{1-y}Ge_y$. (b) The calculated m*x(1-x) in $Si_{1-y}Ge_y$ as a function of the channel Ge percentage.

with added <110> stress. Alloy scattering has been studied extensively in $Si_{1-x}Ge_x$ and in III-V alloys where the atomic distribution of constituent atoms varies randomly [108-112]. Theoretical calculations indicate that alloy scattering is a significant scattering mechanism at low temperatures where phonon scattering is reduced [108-112]. This may also be the case in biaxial compressive strained-SiGe where strain induced subband splitting strongly suppresses phonon scattering at room temperature. In Figure 5.12(a) the <110> longitudinal piezoresistance coefficients are plotted as a function of the channel Ge percentage. It appears that the piezoresistance coefficients may be correlated to the alloy factor, x(1-x). According to G. Bastard, the alloy scattering rate in SiGe is proportional to m*x(1-x) [113]. The piezoresistance results in Figure 5.12(a) mirror the calculated m*x(1-x) result in Figure 5.12(b) for $Si_{1-y}Ge_y$. This may provide some additional that changes in alloy scattering may also be driving the observed change in hole mobility with added <110> stress. A detailed analysis of the impact that added <110> strain has on the relevant scattering in biaxial compressive strained-SiGe is required to

validate this hypothesis.

5.5 Summary and conclusions

In this chapter the hole mobility characteristics of biaxial compressive strained-SiGe p-MOSFETs with added <110> uniaxial compressive strain were examined for the first time. The substantial hole mobility enhancement provided by biaxial compressive strained-SiGe relative to relaxed Si continues to increase with the application of <110> uniaxial compressive strain. It was also found that the hole mobility in biaxial compressive strained-SiGe (e.g. 43/0, 42/30, 63/0, 58/30 and 100/40) expresses a greater sensitivity to applied uniaxial strain than Si. This sensitivity to applied <110> strain increases as the amount of in-plain biaxial compressive strain in the channel increases. Upon examining the longitudinal piezoresistance coefficients we see that the hole mobility response to applied <110> stress in SiGe is correlated to the amount of in-plane biaxial compressive strain present in the channel.

The impact of applied <110> stress on the effective mass was examined to determine if the relative mobility increase in biaxial compressive strained-SiGe with added <110> strain is a mass driven phenomenon. While added stress does provide a change in the hole effective mass, the relative expected change in mass is smaller in biaxial compressive strained-SiGe than in Si with added <110> strain. The mobility increase in Si with added uniaxial strain has been attributed primarily to a change in effective mass, when the applied <110> compressive stress is less than 500 MPa. To compensate for the smaller relative change in mass calculated for biaxial compressive strained-SiGe a simultaneous change in the scattering characteristics must also be occurring. Biaxial compressive strained-SiGe and Si share most of the same scattering mechanisms, with the exception of alloy scattering. The hole mobility in biaxial compressive strained SiGe may be also benefiting from changes in alloy scattering. A more detailed analysis

is needed to confirm this.

Since the relative change in mobility observed in biaxial compressive strained SiGe is in part driven by a change in the hole effective mass, the combination of biaxial compressive strain with added <110> uniaxial compressive strain should be somewhat beneficial for increasing the hole velocity. It does appear that a change in scattering may be influencing the change in mobility observed with applies stress, and therefore the correlation factor, α, discussed in the introduction is expected to be less than 0.5.

Chapter 6

THESIS SUMMARY AND CONCLUSIONS

6.1 Thesis summary

In this chapter the main themes and topics of this thesis will be reviewed. The major contributions and suggestions for future work will also be discussed.

6.1.1 Strained Ge HOI

This work exhibits fabrication of the first strained-Si/strained-Ge heterostructure on insulator. XRD analysis revealed a drop in peak Ge content to about 97 at.% in the strained Ge layer of the epitaxially grown etch-back structure. Raman analysis on this structure revealed that this layer is about 8% relaxed. The observed drop in Ge content and strain may have occurred during the growth of the final Si layer which was conducted at 600°C. Additional Si/Ge interdiffusion as well as relaxation in the Ge layer appears to occur during the bonding sequence. After layer transfer the Ge content of the strained Ge layer appears to drop to 93% at.% and the layer is about 12% relaxed. Further optimization of the bond process is needed to limit the Si and Ge interdiffusion as well as the relaxation that occurs during substrate fabrication. The strained Si layers in the etch-back structure and final Ge HOI substrate are less than 5% relaxed, indicating little change in the strained Si films upon layer transfer. The extracted mobility characteristics reveal a 9x hole mobility enhancement relative to relaxed SOI. The strained Ge HOI hole mobility is quite comparable to the mobility in a 90/40 bulk p-MOSFET (i.e. bulk p-MOSFET with a strained $Si_{0.1}Ge_{0.9}$ channel pseudomorphic to relaxed $Si_{0.6}Ge_{0.4}$). Recall that XRD analysis performed on the completed Ge HOI substrate suggested a 7 at.% drop in the Ge content of the

strained Ge layer. This is in good agreement with the mobility result which shows that the Ge HOI hole mobility is comparable to the that of a 90/40 bulk p-MOSFET, again where the peak channel Ge composition is 90 at.%. This also suggests that there may have been a slight drop in peak channel Ge percentage. Regardless, the hole mobility observed in strained Ge HOI is still quite impressive.

6.1.2 Hole transport in short channel strained-SiGe p-MOSFETs

Biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs with gate lengths down to 65 nm have been fabricated to explore the merits of a strained-$Si_{0.45}Ge_{0.55}$ channel. Hole mobility and velocity were extracted and benchmarked against comparable Si control devices. Devices with gate lengths in the range of 65-150nm are observed to exhibit a 2.4x hole effective mobility enhancement over the Si control mobility. While a slight drop in mobility is observed as the gate length is reduced the observed mobility enhancement is still substantial. Three velocity extraction methods were employed and the velocity characteristics of scaled strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs have been documented. A modest 1.25x velocity enhancement is observed in biaxial compressive stained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs over control devices with a similar gate length and DIBL. While biaxial compressive strain in SiGe is very beneficial in providing a substantial mobility enhancement, it does not prove to be as beneficial to the carrier velocity. Band structure and ballistic velocity calculations indicate that a substantial enhancement in velocity can be expected with the incorporation of Ge into the channel and the addition of uniaxial stress. While the velocity enhancement provided by uniaxial compressive stress in Si is expected to saturate at about 2.7x relative to relaxed Si, simulations predict that a strained-$Si_{0.45}Ge_{0.55}$ channel will outperform relaxed Si by 4.3x with -3 GPa of uniaxial compressive channel stress. Moving to a pure Ge channel is predicted to provide a slightly higher performance gain at 5.2x, again with -3 GPa of

uniaxial compressive channel stress. This suggests that even moderate amounts of Ge incorporated into the channel and combined with uniaxial compressive stress can provide a significant velocity enhancement over relaxed Si channel p-MOSFETs. This result is quite promising and indicates that with appropriate strain, even a moderate concentration of Ge in the channel (50 at. %), which could ease integration issues relative to pure Ge, may provide substantial velocity improvement relative to a Si channel p-MOSFET.

6.1.3 Hole mobility in asymmetrically strained SiGe p-MOSFETs

The hole mobility characteristics of biaxial compressive strained-SiGe p-MOSFETs with added <110> uniaxial compressive strain have been examined for the first time. The substantial hole mobility enhancement provided by biaxial compressive strained-SiGe relative to relaxed Si continues to increase with the application of <110> uniaxial compressive strain. It was also found that the hole mobility in biaxial compressive strained-SiGe (e.g. 43/0, 42/30, 63/0, 58/30 and 100/40) expresses a greater sensitivity to applied uniaxial strain than Si. This sensitivity to applied <110> strain increases as the amount of in-plane biaxial compressive strain in the channel increases. Upon examining the longitudinal piezoresistance coefficients we see that the hole mobility response to applied <110> stress in SiGe is correlated to the amount of in-plane biaxial strain present in the channel.

The impact of applied <110> stress on the effective mass was estimated to determine if the relative mobility increase in biaxial compressive strained-SiGe with added <110> strain is a mass driven phenomenon. While added stress does provide a change in the hole effective mass, the expected relative change in mass is smaller in biaxial compressive strained-SiGe than in Si with added <110> strain. The mobility increase in Si with added uniaxial strain has been attributed solely to a change in effective mass, when the applied <110> compressive stress is less

than 500 MPa. To compensate for the smaller relative change in mass calculated for biaxial compressive strained-SiGe a simultaneous change in the scattering characteristics must also be occurring. Biaxial compressive strained-SiGe and Si share most of the same scattering mechanisms, with the exception of alloy scattering. The hole mobility in biaxial compressive strained SiGe may be also benefiting from changes in alloy scattering. A more detailed analysis is needed to confirm this.

Since the relative change in mobility observed in biaxial compressive strained SiGe is in part driven by a change in the hole effective mass, the combination of biaxial compressive strain with added <110> uniaxial compressive strain should be beneficial for increasing the hole velocity. It does appear that a change in scattering may be influencing the change in mobility observed with applies stress, and therefore the correlation factor, α, is expected to be less than 0.5.

6.2 Conclusions

The need to continue transistor performance improvements that are commensurate with geometric scaling motivates the study of high mobility channel materials and the use of ultrathin body metal oxide semiconductor field-effect transistor (MOSFET) architectures. The significant mobility enhancement and electrostatic benefits observed in the biaxial compressive strained-SiGe and strained-Ge HOI provides incentive to explore the fabrication of thin-body p-MOSFETs for this purpose. In chapters 3 and 4 the long channel hole mobility characteristics of thin-body biaxial compressive strained-Ge and strained-SiGe p-MOSFETs were explored. While the hole mobility gains in long channel strained-SiGe and strained-Ge p-MOSFETs are substantial the short channel transport gains need to be equally impressive for these materials to be viable options for deeply scaled CMOS. The short channel hole mobility extracted from scaled biaxial compressive strained-

SiGe p-MOSFETs show that a high hole mobility can be maintained as the gate length is scaled. This does come at a cost though. Process steps that could have relaxed the channel strain were modified or eliminated. Steps like halo implants which would have improved the electrostatic performance, but severely disrupted the channel strain were eliminated. The maximum temperature and duration of the activation anneal was also minimized to avoid strain relaxation. A more fundamental limit to the potential transport gains of biaxial compressive strained-SiGe exists. While the hole mobility enhancement observed at shorter gate lengths was quite impressive, the hole velocity enhancement provided over relaxed Si was quite modest. The modest velocity gains observed in strained-SiGe appear to be rooted in the fact that biaxial compressive strain in SiGe in not very effective in reducing the hole effective mass, which is needed to increase hole velocity. A solution has been found though. Through simulations it was determined that the introduction of a <110> uniaxial compressive strain component in biaxial strained-SiGe produces a more impressive hole velocity boost. This is due to the fact that as in Si, uniaxial strain in SiGe is more effective than biaxial strain in reducing the hole effective mass.

The hole mobility characteristics of asymmetric strained-SiGe and strained-Ge p-MOSFETs have also been explored. The substantial hole mobility enhancement provided by biaxial compressive strained-SiGe relative to relaxed Si continues to increase with the application of <110> uniaxial compressive strain. The impact of applied <110> stress on the effective mass was examined to determine if the relative mobility increase in biaxial compressive strained-SiGe with added <110> strain is a mass driven phenomenon. While added stress does provide a change in the hole effective mass, the relative change in mass is smaller in biaxial compressive strained-SiGe than in Si with added <110> strain. The hole mobility in biaxial compressive strained SiGe may also be benefiting from changes in the scattering characteristics.

Since the relative change in mobility observed in biaxial compressive strained SiGe is in part driven by a change in the hole effective mass, the combination of biaxial compressive strain with added <110> uniaxial compressive strain should lead to an for increase in the hole velocity. This observation supports the ballistic velocity simulations in chapter 4 which concluded that asymmetric strain is needed to reduced the hole effective mass and consequently increase hole velocity. This thesis concludes that asymmetric strained-SiGe has the potential be a viable technological option for future CMOS logic nodes. A few hurdles need to be overcome to realize the practical implementation of asymmetric strained-SiGe in CMOS. An efficient and practical means for introducing asymmetric strain into SiGe needs to be devised. This issue may be resolved through the use of embedded strained-SiGe source drains or through patterning induced strain relaxation in the transverse direction. Incorporating asymmetric strained SiGe onto a state of the art CMOS process line is viewed as a significant challenge since a good number of the process steps used in manufacturing CMOS logic transistors have the potential to severely disrupt the channel strain profile. Another issue to contend with is eliminating the Si passivation layers utilized in this work. This is viewed as a significant hurdle since the gate dielectric significantly influences the electrostatics and the transport characteristics of the device.

6.3 Contributions

- Development of a strained-Ge on strained-Si growth method utilizing an interfacial SiGe surface treatment (patent pending)
- Development of a low temperature wafer bond and etch-back process for the development of strained-Ge/strained-Si heterostructures on insulator
- Development of high hole mobility strained-Ge heterostructure on insulator

- Fabrication of high hole mobility short channel strained-SiGe p-MOSFET
- Extraction of the hole velocity characteristics in short channel strained-SiGe p-MOSFETs
- First measurement of the hole mobility characteristics of biaxial compressive strained SiGe and Ge p-MOSFETs with additive longitudinal and transverse strain
- First measurement of the longitudinal and transverse piezoresistance coefficients in biaxial compressive strained SiGe and Ge

6.4 Suggestions for future work

- Refine strained Ge on strained Si growth to produce smoother films
- Develop a strained-Ge on insulator substrate that uses high-k dielectric passivation as opposed to strained-Si cladding layers
- Study the hole velocity characteristics of asymmetrically strained short channel strained SiGe p-MOSFETs
- Fabricate short channel strained SiGe p-MOSFETs with embedded SiGe source/drains to induce an asymmetric channel strain profile which may improve the hole velocity characteristics of biaxial compressive strained SiGe
- Perform a comprehensive study of the hole velocity characteristics in biaxial compressive strained SiGe p-MOSFETs with additive longitudinal and transverse applied strain
- Attempt to incorporate more than 200 MPa of additive uniaxial compressive strain onto biaxial compressive strained SiGe p-MOSFETs to examine the hole mobility characteristics of highly asymmetrically strained SiGe p-MOSFETs

- Try to conduct low temperature measurements of the hole velocity and mobility characteristics of biaxial compressive strained SiGe p-MOSFETs with added uniaxial compressive strain
- Perform a more rigorous theoretical investigation to examine why the longitudinal piezoresistance coefficients of biaxial strained SiGe p-MOSFETs increase as the channel biaxial strain increases
- Perform a more rigorous theoretical investigation to determine whether modulations in the carrier effective mass or scattering lead to the higher longitudinal piezoresistance coefficients observed for biaxial strained SiGe p-MOSFETs over relaxed Si p-MOSFETs
- Fabricate and examine the longitudinal piezoresistance coefficients of fully relaxed SiGe and Ge p-MOSFETs to see if it is indeed the biaxial strain that is increasing the longitudinal piezoresistance coefficients of biaxial compressive strained SiGe and Ge

Appendix A

SSDOI AND GE HOI FABRICATION

SSDOI Fabrication Flow

The procedures outlined below are for the fabrication of strained Silicon directly on Insulator (SSDOI) and strained-Si/strained-Ge Heterostructures on Insulator (Ge HOI). The machines utilized in SSDOI and Ge HOI fabrication are located in the Microsystems Technology Laboratories at MIT.

Step Name	Step Description	MTL Tool/Machine Name
1. Grow the SSDOI or Ge HOI etch-back structure	Grow the etch-back structure in the Hoyt group Applied Materials Epi Centura	Applied Materials Epi Centura Hoyt Epi Lab
2. Clean etch back wafer prior to LTO deposition	Modified RCA Clean (1) 5 minute piranha (2) 15 sec 50:1 HF dip (3) 10 minute SC-2 (4) Spin Rinse Dry	ICL RCA Station
3. Deposit LTO	Deposit at will become part of the buried oxide. Deposit 500 nm.	ICL LTO Tube 6C
4.LTO Densification	LTO densifying anneal and out gas prior to bonding (1) 2 hours at 550C	ICL Tube 5B
5. Prepare bond handle wafer	Oxidize a new p- Si wafer. Use a 1000C wet oxidation to form a 100 nm oxide.	ICL Tube 5C
6. CMP the cross hatch induced surface roughness	Remove 200 nm via dielectric CMP	ICL CMP
7. Post CMP clean	Double piranha clean (1) 10 minute blue piranha (2) 10 minute green piranha Note: Do not use HF prior to bonding. HF will roughen the oxide surface and introduce voids at the bond interface	ICL Premetal Station
8. Pre-Bond RCA clean	Clean both the etch back and	ICL RCA Station

	bond handle wafers (1) 10 minute SC1 (2) 15 minute SC2	
9. Oxygen plasma surface bond surface prep	Expose the bond interfaces to an oxygen plasma for 20 sec prior to bonding.	ICL AME 5000
10. Pre-bond piranha clean	One last clean prior to bonding to remove particles from the handle and etch-back wafer surface (1) 10 minute Piranha	TRL RCA Station
11. Wafer bonding	Bring wafers into forced contact for 120 seconds using the EV620 in TRL	TRL EV620
12.Wafer bond Anneal	Strengthen the wafer bond with an anneal at 300C for 5 hours	TRL Tube A1
13. Wafer grinding	Send wafers out for grinding on the etch-back wafer side of the bonded pair. Typically the bonded wafer pair is ground down to a thickness of 775 microns and 10 microns is polished off via CMP to remove the scratches introduced to the wafer surface during wafer grinding	Outsourced to GDSI or SQI
14. Sponge clean the wafer bonded pair	Sponge clean the bonded wafer pairs in the CMP room under a stream of DI wafer	ICL CMP room
15. Post grind back clean	Double piranha clean (1) 10 minute blue piranha (2) 15 sec HF dip (3) 10 minute green piranha	ICL Premetal Station
16. Back side wafer protection	Deposit 2 microns of DCVD oxide in 0.5 micron increments. Only deposit 0.5 microns at a time. Depositing more will cause the bonded wafer pair to delaminate during oxide deposition due to prolonged high temp exposure	ICL DCVD
17. TMAH Si substrate etch	Etch bonded wafer pairs to expose the SiGe grade in the etch back structure. Dip the	ICL KOH-TMAH-hood

	bonded wafer pair in a 50:1 DI:HF bath for 15 sec to remove the native oxide prior to TMAH etching. Then etch the Si substrate in TMAH at 80C for about 6 hours when the cross hatch becomes visible on the wafer surface. Note the cross hatch is difficult to see, so be patient during the etch so that you can notice when the cross hatch becomes visible. Take the wafers out a few times during the etch to see the cross hatch come in	
18. SiGe grade Etch	Etch the remaining SiGe and relaxed buffer in a 3:2:1 solution of Acetic Acid:H2O2:HF. It is best to mix a solution of 900ml:600ml:300ml. This provides the most stable etch rate. The etch time runs about 15-30 minutes. The etch is complete when the surface changes from a silvery color towards another color and stabilizes.	TRL Acidhood2
19. TMAH Si etch stop etch	Etch the Si etch stop in TMAH at 80C for 60 sec. Dip the wafer in 50:1 HF prior to the TMAH etch to remove the native oxide.	ICL KOH-TMAH-hood
20. Final SiGe etch stop etch	Etch the final SiGe etch stop in an SC-1bath at 80C. Etch for 2 minutes at a time and measure the remaining structure in the UV1280 to monitor how much of the SiGe etch stop is remaining. Continue etching the SiGe layer until the device structure is reached	TRL Acid-hood2

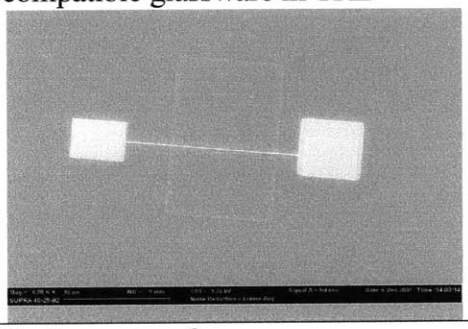
Appendix B

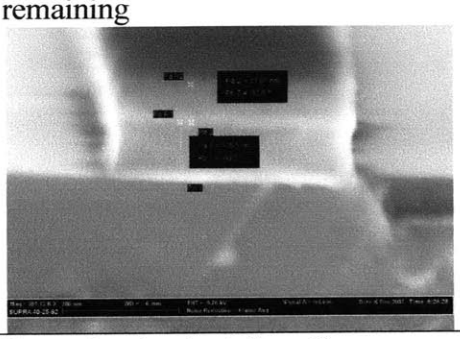
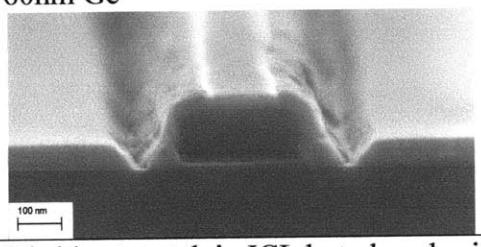
SHORT CHANNEL MOSFET FABRICATION

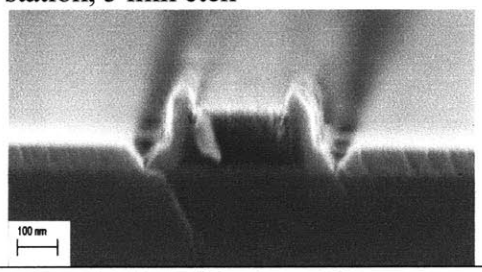
Short Channel MOSFET Fabrication Flow

The procedures outlined below are for the fabrication of short channel Si and strained SiGe MOSFETs on insulator. The machines utilized in short channel MOSFET fabrication are located in the Microsystems Technology Laboratories at MIT. Most steps will need to be optimized prior to running them on product wafers. It is critical that dummy wafers be processed in parallel with both blanket and patterned features to provide samples for optimizing etch rates and deposition time.

Step Name	**Step Description**	**MTL Tool/Machine Name**
1. Coat wafers	Resist coat wafers	ICL coater track
2.Expose E-beam alignment marks (EAM)	Expose ebeam alignment marks in ICL i-line stepper	ICL i-stepper
3. Develop resist	Develop resist	ICL developer track
4. Etch EAM into device layer	Etch the EAM marks into the device layer	ICL AME 5000
5. Etch EAM into BOX	Etch the EAM marks into the BOX	ICL AME 5000
6. Etch EAM into the Si substrate	Etch the EAM marks into the Si substrate	ICL AME 5000
7. Ash resist	Ash EAM level resist	ICL Asher
8. Coat wafers	Resist coat wafers	ICL coater track
9. Expose STI layer	Expose STI layer in ICL i-stepper	ICL i-stepper
10. Develop resist	Develop resist	ICL developer track
11. Etch STI into device layer	Etch the STI layer into the device layer	ICL AME 5000
12. Ash resist	Ash STI level resist	ICL Asher
13.Resist piranha clean	10 minute blue piranha clean, no HF	ICL Premetal Station
14. Standard RCA clean	Wafer clean prior to gate stack formation (1) 10 minute SC1 (2) 15 sec HF dip (3) 15 minute SC2 (4) SRD	ICL RCA Station
15. Gate oxide formation	Gate oxidation of the Si cap. 600C	ICL Tube 5D

	oxidation in tube 5D. 3 hours produces a 3.5 nm oxide	
16. n-doped Poly-Si gate deposition	100 nm poly-Si deposition in tube 6A-nPoly.	ICL Tube 6A
17. Nitride hard mask deposition	Deposit 75 nm of DCVD nitride	ICL DCVD
18. Front side resist protect	Front side resist protect in the ICL coater	ICL Coater Track
19. Back-side poly-Si etch	Backside poly Si etch in the LAM	ICL LAM
20. Ash resist	Ash front-side protection	ICL Asher
21. Coat front side with e-beam resist	Coat the wafer with HSQ e-beam resist.	TRL PMMA Spinner
22. Prebake HSQ	Bake HSQ for 4 minutes at 90C on the hot plate in the Heidelberg room	TRL Heidelburg Hot Plate
23. Drop latex nano-particles for e-beam focusing	Drop 90 nm Latex nano-particles wafer and die to be patterned	SEBL E-beam patterning facility
24. E-beam write the short channel gate pattern	e-beam writing on ICL compatible stage in SEBL RLE, 30kV, dose 1200uC/cm2, 10kV, dose 400uC/cm17	SEBL E-beam patterning facility
25. Develop HSQ e-beam resist	Develop HSQ e-beam resist using 25% TMAH for 1min using ICL compatible glassware in TRL 	TRL Acidhood2
26. Coat wafers	Resist coat wafers	ICL coater track
27. Expose photo gate level	Expose photo gate level using i-line stepper	ICL i-stepper
28. Develop resist	Develop resist	ICL developer track
29. Etch nitride hard mask	Etch nitride hardmask, AME 5000 ICL, recipe NITRIDE CF4, @ 33 A/sec, used 25sec etch time	ICL AME 5000
30. Ash resist	Ash front-side protection	ICL Asher
31. Strip HSQ e-beam resist	Strip HSQ in a 50:1 HF:DI bath for 50 seconds	ICL Acidhood2
32. Etch poly-Si gate	Etch poly-Si to form the gate, AME 5000 ICL, used recipe JK SOFT GP	ICL AME 5000

	ETCH ran it as 30,5,5 (main, soft, over etch) measured 40A of oxide remaining 	
33. Extension Implant	Extension implantation, Boron 2e14cm-2, 0 tilt, 6keV	Implant done at Innovion
34. Post Implant Clean	Post implantation cleaning. (1) 10 minute blue piranha (2) 10 minute green piranha	ICL Premetal Station
35. Modified RCA Clean	Substrate cleaning prior to LTO spacer deposition (1) 5min piranha (2) 15sec HF (3) 5 min SC-2	ICL RCA Station
36. Spacer LTO Deposition	Deposit 140 nm of LTO to form the spacers	ICL LTO 6C
37. Spacer Dry Etch	Spacer dry etch in the AME 5000, etch until 15 nm of oxide remains	ICL AME 5000
38. Spacer Wet Etch	Spacer wet etch in acid hood2 wet etch, 50:1, 1min	TRL Acidhood2
39. Ge RCA Clean	Ge RCA clean prior to Ge selective epitaxy (1) NH4OH:H2O 1:4 5 min (2) H2O2:H20 1:6 15sec (3) HCl:H2O 1:4 30sec (4) 15 sec HF dip (5) SRD dry	ICL-RCA Station
40. Ge SEG for elevated source/drain	Ge SEG, boron doped, recipe GE SEG: DOPED-1 recipe, 154 sec, 55-60nm Ge 	Epi Centura Hoyt Epi Lab
41. Nitride Hardmask	Nitride wet etch in ICL hot phosphoric	ICL Hot Phosphoric Station

removal	station, 5 min etch 	
41. ILD Deposition	200 nm ILD oxide deposition	ICL DCVD
42. Standard RCA clean	Wafer clean prior to gate stack formation (1) 10 minute SC1 (2) 15 sec HF dip (3) 15 minute SC2 (4) SRD	ICL RCA Station
43. RTP Dopant Activation	RTA dopant activation in ICL RTP	ICL RTP
44. Coat wafers	Resist coat wafers	ICL coater track
45. Expose via level	Expose via level using i-line stepper	ICL i-stepper
46. Develop resist	Develop resist	ICL developer track
47. ICL Partial Dry Etch	Partial dry etch via until 15 nm of oxide remains	ICL AME 5000
48. Wet Etch Remaining Oxide	Wet etch remaining oxide in via, HF bath 50:1 1min	TRL Acidhood2
49. Ash resist	Ash via level resist	ICL Asher
50. Sinter Anneal	Sinter anneal, 450C 30min	TRL Tube A3
51. Premetal HF Dip	Pre-metal HF dip, 50:1 for 15 sec	ICL Premetal Station
52. Contact Metal Deposition	Metal deposition, 150 nm Ti followed by 1um of Al	ICL Endura
53. Coat wafers	Resist coat wafers	ICL coater track
54. Expose metal contact level	Expose metal contact level using i-line stepper	ICL i-stepper
55. Develop resist	Develop resist	ICL developer track
56. Etch metal contacts	Etch contacts, ICL rainbow, 105 sec is good with manual endpoint	ICL Rainbow Etcher
57. Ash resist	Ash via level resist	ICL Asher
58. Sinter Anneal	Sinter anneal, 450C 30min	TRL Tube A3

Appendix C

DEVICE BENDING MEASUREMENT AND ANALYSIS

Device bending measurements

The procedures outlined here are to introduce either uniaxial compressive or tensile strain during electrical measurements. This method uses the bending apparatus in the Dimitri Antoniadis measurement laboratory.

Step Name	Step Description	MTL Tool/Machine Name
1.Cut sample strip prior to bending	Cut a 6 inch long sample (from a 6 inch or larger wafer) that is at least 2 cm wide. A 2 cm wide sample is less likely to break and will still provide you with enough room to maneuver the sample in the bending chuck. This can be done by either cleaving or die saw. I find cleaving to be risky, especially when you only have one wafer to work with, so I tend to cut all of my samples on the die saw.	ICL Die Saw or TRL Cleaving Bench
2. Configure Bending Apparatus for Tensile or Compressive Strain	Configure the bending apparatus for either tensile or compressive strain by removing the top screws and plate and then inserting the correct plate configuration to obtain the desired strain. It is important to note that one full rotation of the micromanipulators on the bending apparatus constitutes a 0.5 mm of sample deflection. When adjusting the sample strain one should alternate between adjusting the	Measurement Lab

	micromanipulator on either side of the sample SLOWLY. The maximum deflection obtained using this apparatus is approximately 3 mm. I typically adjust the deflection in 0.5 mm increments between measurements.	
3. (Optional) Calibrate the applied strain level	Adhere a strain gauge to the device wafer or a dummy sample and bending it to correlate the sample deflection from the micromanipulators with the amount of applied strain in the wafer/sample	Measurement Lab
4. Set up for a measurement	Attach and place all of the measurement probes that will be needed during the device measurement. Lower the micromanipulators and insert the sample. Raise the sample until it is held in place against the top place. Align the measurement probes with the device.	Measurement Lab
5. Initial measurement	First exercise the sample by bending it a little and then bring the deflection back to 0. This breaks the static friction in the sample and produces a more uniform application of strain in the sample. For the first measurement lower the probes onto the device and make an initial measurement at strain=0/deflection=0.	Measurement Lab
6. Raise the probes and adjust strain	Raise the measurement probes. Adjust the micromanipulators to increase the strain level. I typically increase the manipulator deflection by 0.5mm at a time. The largest deflection I usually get without any breakage is 3mm.	Measurement Lab

7. Strained Measurement	Lower the probes onto the sample after the strain adjustment is complete. Repeat the electrical measurement. Continue steps 6-7 until you've reached 3mm deflection	Measurement Lab
8. Lift measurement probes	When your measurements are done raise the probes up and away from the devices. If the probes are not placed significantly far enough away from the device then when the sample is extracted it can get damaged.	Measurement Lab
9. Un-strain the sample	Slowly reverse the deflection. Alternate between manipulators and release the strain in small increments.	Measurement Lab
10. Remove and store sample	Remove and store your sample	Measurement Lab
11. Put the probes back	Put the probes back in place where you found them	Measurement Lab
12. Put all other supplies away	Put up all other lab supplies used and make sure the lab is clean	Measurement Lab

Appendix D

HOLE MOBILTIY IN STRAINED SIGE P-MOSFETS WITH ADDED TRANSVESE STRAIN

D.1 Strained-SiGe p-MOSFETs with added <110> transverse strain

In chapter 5 the mobility characteristics of biaxial compressive strained-SiGe p-MOSFETs with added <110> longitudinal strain were examined. In this appendix the impact of added transverse strain will be investigated using the same set of devices. The device structures and processing conditions are described in detail in section 5.2. Transverse strain was added utilizing the bending apparatus described in section 5.2. The transfer and capacitance-voltage characteristics are a 43/0 strained-SiGe p-MOSFET with added <110> uniaxial transverse strain are plotted in Figure D1. A reduction in the on-current occurs with added transverse strain, while no change in the CV characteristics is observed. This is indicates that the current change that occurs with added transverse strain arises from a change in the hole mobility. The lack of change in the CV characteristics suggests that carrier confinement doesn't change as transverse strain is added. The extracted mobility characteristics in Figure D2 show the mobility decreasing as <110> transverse strain is applied. A reduction in mobility is seen for all devices including the relaxed Si control. In Figure D3 the relative change in mobility is plotted for biaxial compressive strained SiGe devices with applied longitudinal and transverse strain. The transverse mobility trends mirrors the result for added longitudinal strain. The biaxial compressive strained SiGe and Ge devices express a greater sensitivity to the applied longitudinal and transverse strain compared to the relaxed Si control. In the case of applied transverse strain the biaxial compressive strained SiGe and Ge p-MOSFETs

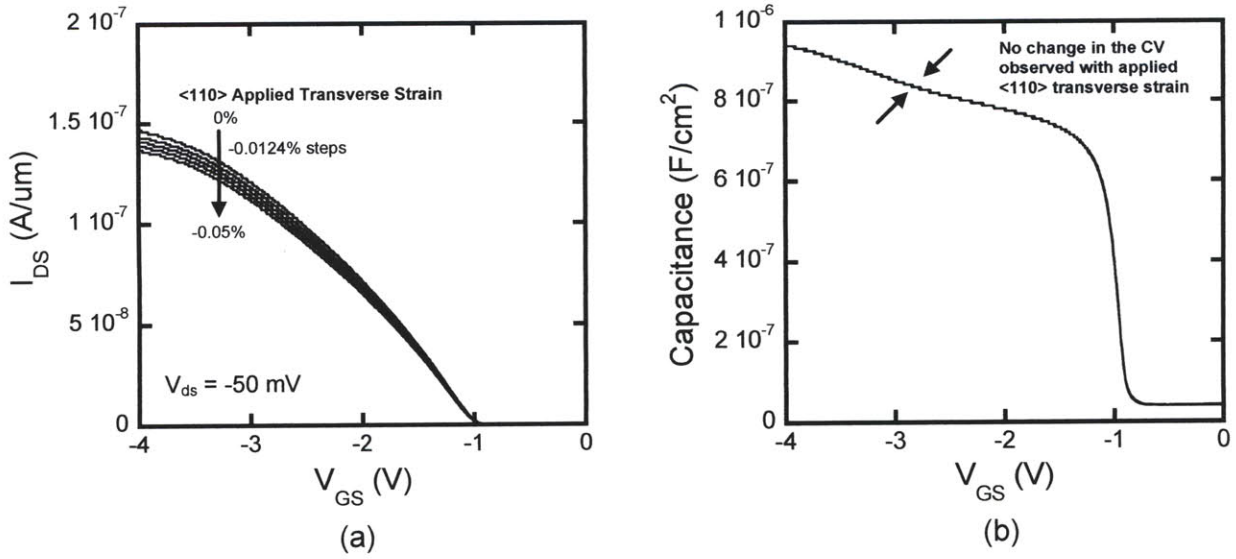


Figure D1 (a) Transfer characteristics for a 43/0 p-MOSFET with applied <110> transverse uniaxial compressive strain. The arrows indicate the direction of increasing strain starting from 0% strain at the lowest curve and increasing in 0.0124% increments. (b) The C-V characteristics with applied strain for the same 43/0 p-MOSFET in (a). The five C-V curves overlay, which indicates no change in inversion charge density or distribution with applied <110> uniaxial compressive strain.

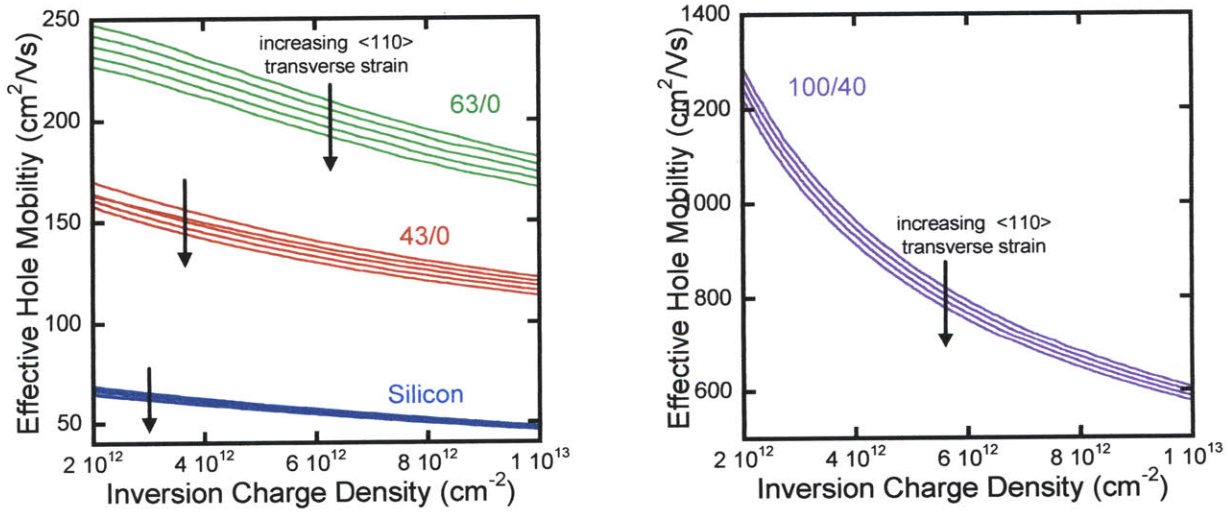


Figure D2 Effective hole mobility curves for Si, 43/0, 63/0, and 100/40 p-MOSFETs with applied <110> transverse uniaxial compressive strain. The arrows indicate the direction of increasing uniaxial compressive strain starting from 0% strain at the lowest curve and increasing in 0.0124% increments. The mobility decreases with added <110> transverse strain.

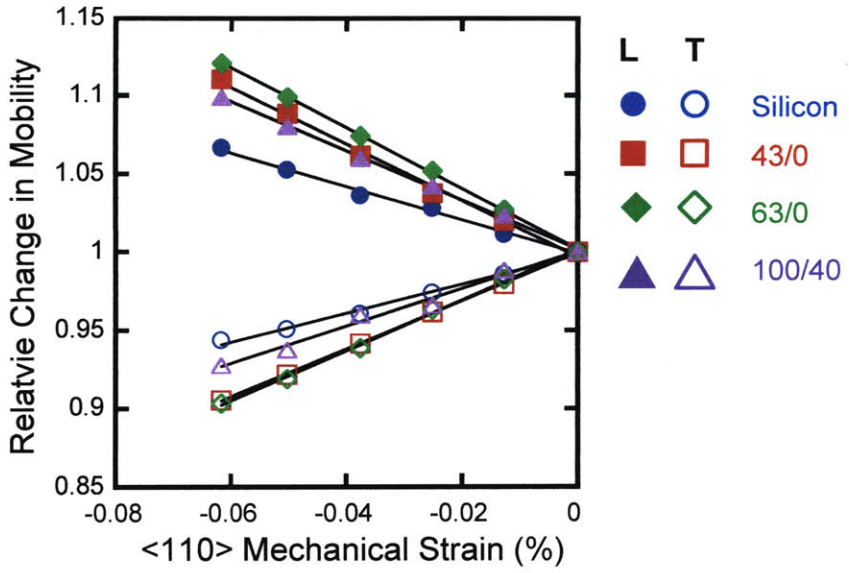


Figure D3 The relative mobility enhancement for the devices in Table 5.1 with applied longitudinal (open symbols) and transverse (closed symbols) compressive strain.

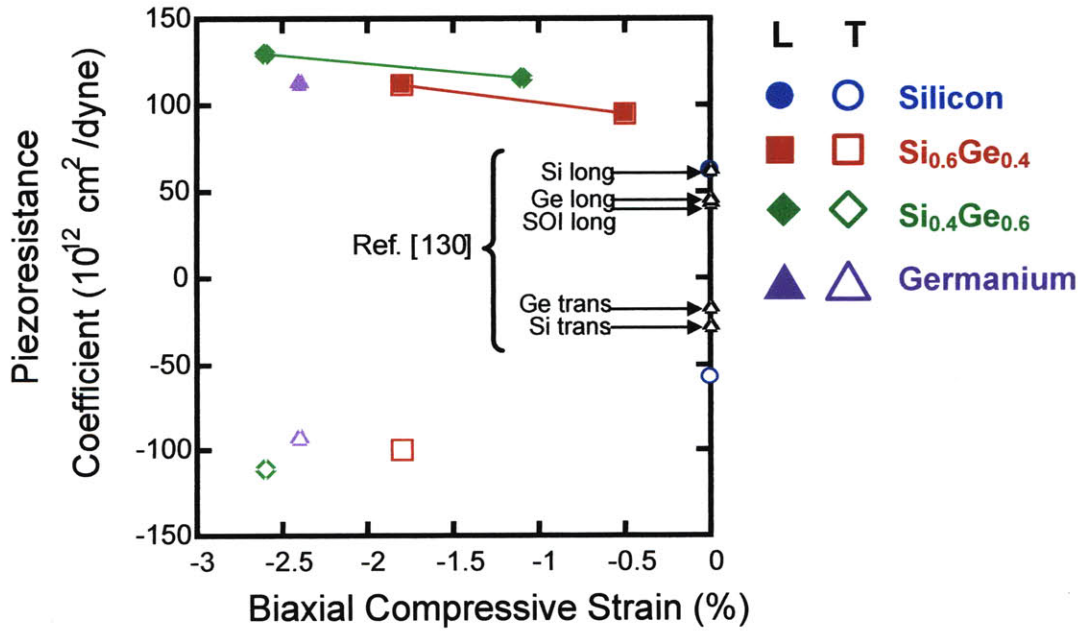


Figure D4 Longitudinal (open symbols) and transverse (closed symbols) piezoresistance coefficients for Si, biaxial compressive strained-$Si_{0.6}Ge_{0.4}$, biaxial compressive strained-$Si_{0.4}Ge_{0.6}$, and biaxial compressive strained Ge are plotted as a function of biaxial compressive strain. The longitudinal and transverse piezoresistance coefficients for relaxed bulk Si, Ge, and SOI reported by O. Weber in [130] are also plotted.

exhibit a greater reduction in mobility with the application of transverse strain. The transverse piezoresistance coefficients (π_T) are plotted as a function of biaxial strain in Figure D4. The drop in mobility with added strain produces negative transverse piezoresistance coefficients. The transverse piezoresistance coefficients for relaxed Si and Ge reported by O. Weber in [130] are also plotted for comparison. Both the longitudinal and transverse piezoresistance coefficients appear to be correlated to the amount of biaxial compressive strain in the strained SiGe channel. As the channel biaxial strain increases a substantial reduction in π_L and π_T is observed. This effect though does not appear to be directly correlated to the channel Ge fraction. The piezoresistance coefficients increase as the nominal channel Ge composition goes from 40% to 60%, but then decrease when the channel Ge composition reaches 100%.

In Figure D3 and D4 we saw that the hole mobility in biaxial compressive strained SiGe and Ge exhibits a greater sensitivity to applied longitudinal and transverse mechanical strain than their relaxed counterparts. This result may prove beneficial in deeply scaled p-MOSFETs where novel channel materials are needed that can provide transports gains greater than that of uniaxial strained Si.

Appendix E

VELOCITY SENSITIVITY ANALYSIS

E.1 Velocity sensitivity analysis

In this appendix we will examine the sensitivity of the extracted hole velocities, υ_{gmi} and υ_{xo}, to variations in the extraction parameters (e.g. R_{SD} and DIBL). The velocities defined in Equation 4.4 and 4.5 possess corrections for parasitic effects like R_{SD} and DIBL. When the values of R_{SD} and DIBL are large the correction factor for υ_{gmi} and υ_{xo} can become substantial and express a greater sensitivity to variations in these parameters. Since there is statistical variation in the extraction parameters it is important to develop an understanding of the error that can be derived from variations in these parameters.

We begin by examining the statistical variation of the extracted hole velocities. In Figure E1 the mean υ_{gmi} and υ_{xo} values are plotted versus gate length with error bars to indicate the one sigma standard deviation range. A more appropriate comparison of the velocities in Si and $Si_{0.45}Ge_{0.55}$ channel p-MOSFETs is made when both the gate length and DIBL values are similar. This comparison is made in Figure E2 where the mean υ_{gmi} and υ_{xo} velocities are provided for devices with a 150 nm gate length and 140 mV/V DIBL. Error bars have also been plotted to indicate the one sigma standard deviation range. This variation in the extracted velocities is translated to the calculated enhancement factors in Figure E2(b). While there appears to be some scatter in the velocity enhancement factor, the range within which the distribution lies still produces a relatively mild velocity gain relative to the hole mobility enhancement measured in these same devices.

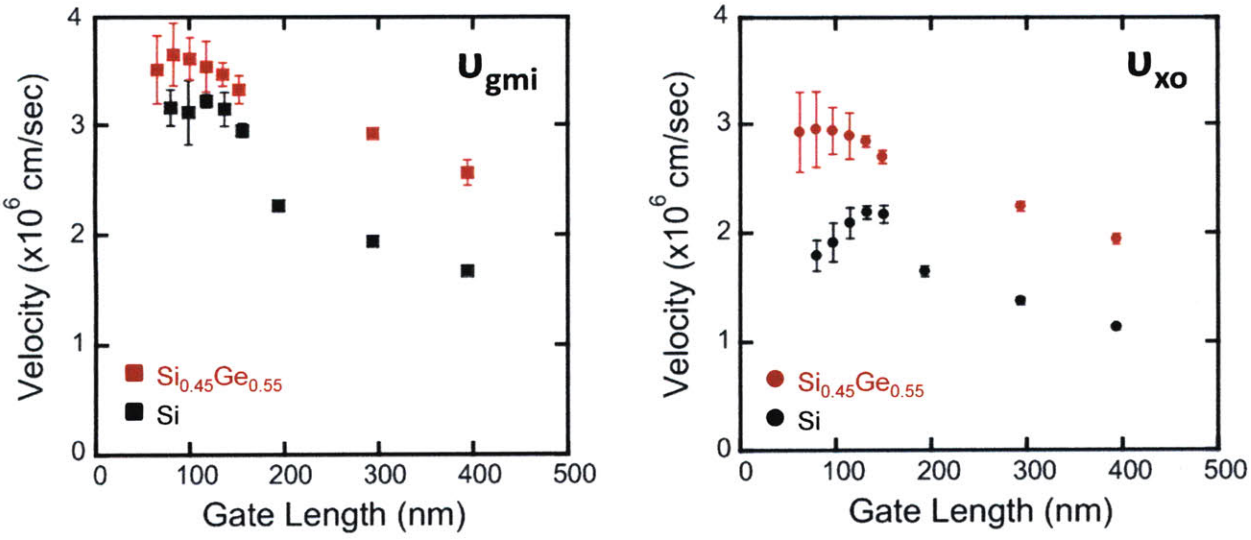
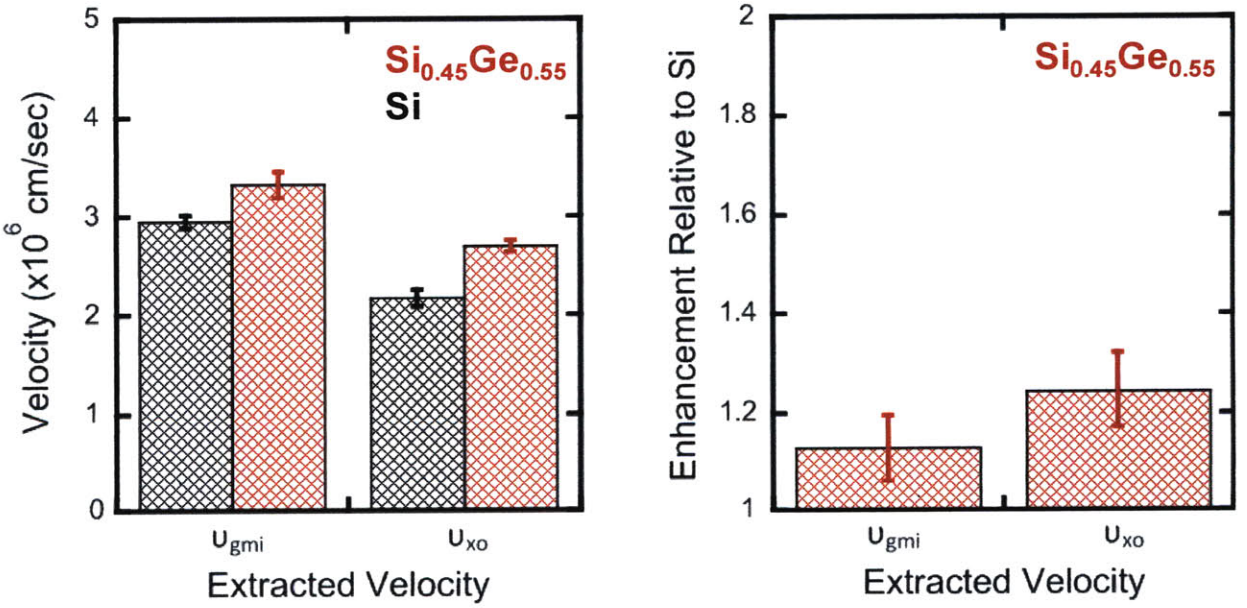


Figure E1 A comparison of the average υ_{gmi} and υ_{xo} extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ and Si control devices examined here have an average L_{Gate} = 150 nm and DIBL = 140 mV/V. Error bars have been added to indicated the one sigma variation of the extracted velocities.



(a) (b)

Figure E2 (a) A comparison of the average υ_{gmi} and υ_{xo} extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ (red) and Si (black) control devices examined here have an average L_{Gate} = 150 nm and DIBL = 140 mV/V. (b) The enhancement relative to the Si control for the average υ_{gmi} and υ_{xo} extracted hole velocities. Error bars have been added which indicate the one sigma variation range of the extracted velocities and calculated enhancement relative to relaxed Si.

	mean R_{sd} (Ω-μm)	3σ R_{sd} (Ω-μm)	mean DIBL (V/V)	3σ DIBL (V/V)
SiGe	2004	223	0.152	0.060
Si	2706	222	0.132	0.039

Table E1 The mean R_{SD} and DIBL values for 150 nm long strained-$Si_{0.45}Ge_{0.55}$ (red) and Si (black) devices. Also provided are the 3-sigma standard deviation values for each parameter.

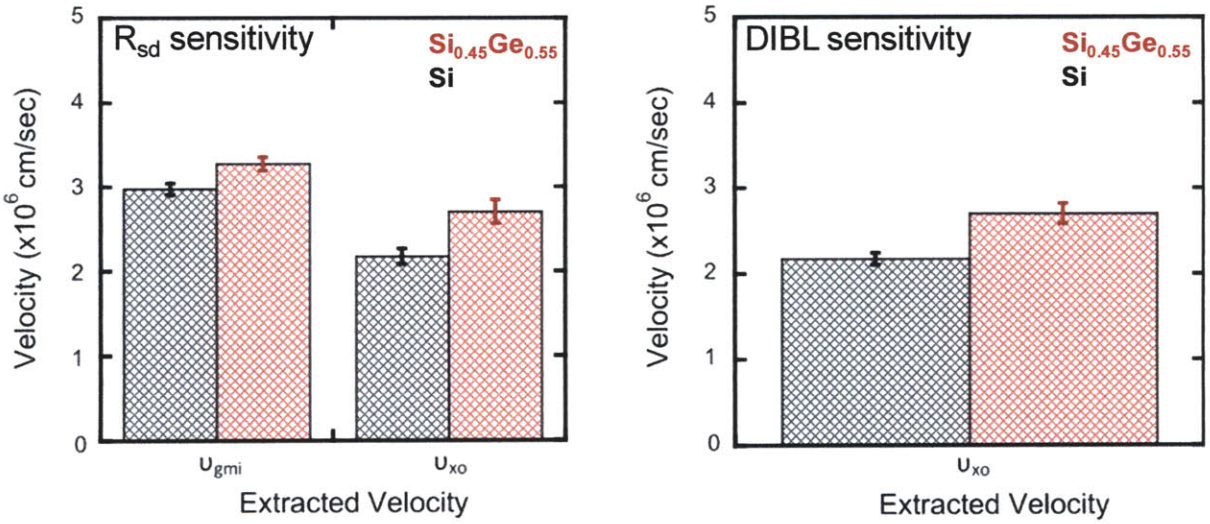


Figure E3 The extracted velocities are plotted for strained $Si_{0.45}Ge_{0.55}$ (red) and Si (black) where both the sensitivity to RSD and DIBL are explored. The error bars in show the range in velocity associated with the 3-sigma variation of either R_{SD} or DIBL. This range constitutes less than a +/- 5% change in velocity.

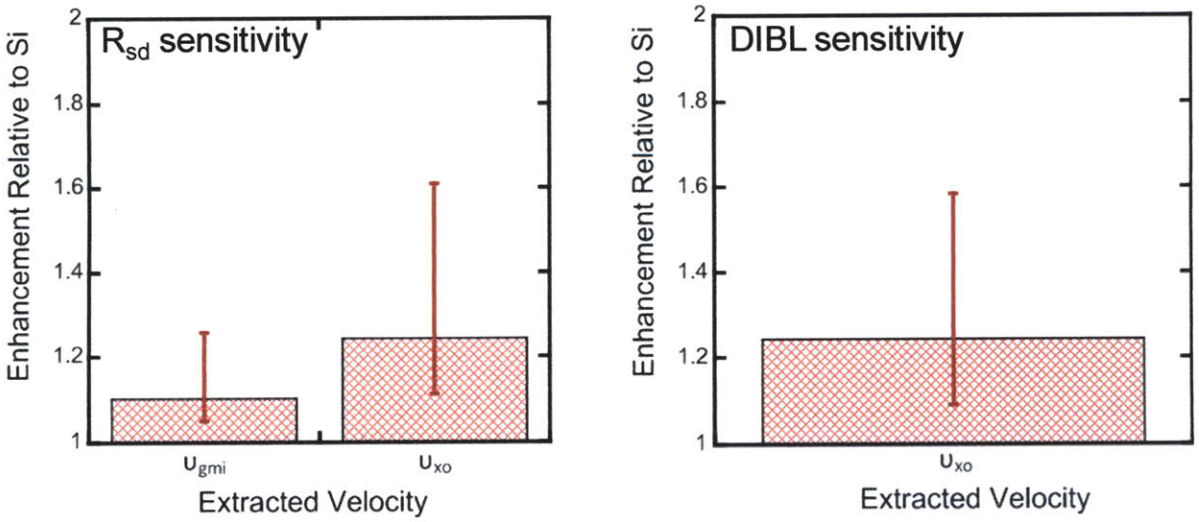


Figure E4 The velocity enhancement relative to relaxed Si is plotted for strained $Si_{0.45}Ge_{0.55}$ devices where both the sensitivity to R_{SD} and DIBL are explored. The error bars in show the range in enhancement associated with the 3-sigma variation of either R_{SD} or DIBL.

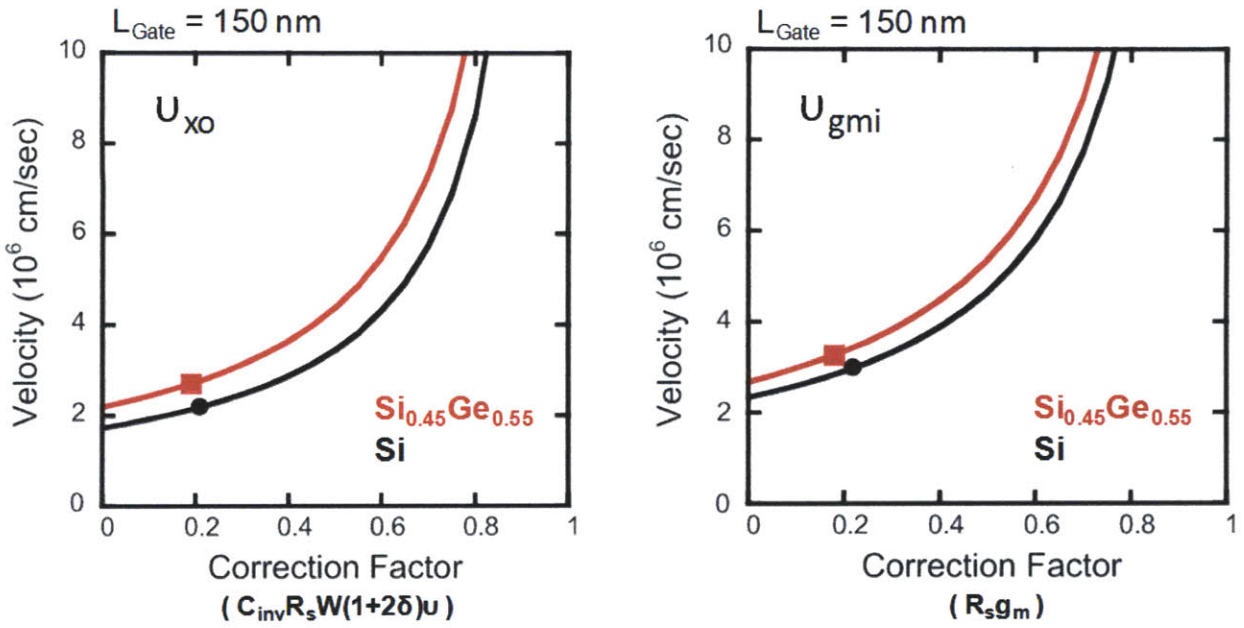


Figure E5 The sensitivity of the extracted virtual source to the correction factor $C_{inv}R_sW(1+2\delta)\upsilon$, and the transconductance effective velocity to the correction factor R_sg_m.

The devices fabricated in this work exhibit statistical variation in the extracted R_{SD} and DIBL values. In Table E1 the mean R_{SD} and DIBL values along with the 3-sigma standard deviation values are reported. To examine the sensitivity of the extracted velocities both υ_{gmi} and υ_{xo} have been extracted using the mean values for R_{SD} and DIBL for 150 nm long devices as well as the mean +/- 3-sigma variation of these parameters. The 3-sigma range is provided since statistically it represents the range within which 99% of the data is contained. This analysis helpful in understanding the limits of the extracted velocities given the variation in R_{SD} and DIBL and also provides a sense of the sensitivity that υ_{gmi} and υ_{xo} express to these parameters. In Figure E3 the extracted velocities are plotted for strained $Si_{0.45}Ge_{0.55}$ and Si where both the sensitivity to 3-sigma variations in R_{SD} and DIBL are explored. When examining the R_{SD} sensitivity the mean DIBL value was used throughout the analysis and when examining the DIBL sensitivity the mean RSD

value was used. The DIBL sensitivity of υ_{gmi} was not explored since there is no correction for DIBL in the extraction of υ_{gmi}. The error bars in Figure E3 show the range in velocity associated with the 3-sigma variation of either R_{SD} or DIBL. This range constitutes less than a +/- 5% change in velocity. This mild variation is amplified in calculating the strained-$Si_{0.45}Ge_{0.55}$ velocity enhancement relative to relaxed Si. The strained-$Si_{0.45}Ge_{0.55}$ velocity enhancement plotted for υ_{gmi} and υ_{xo} in Figure E4 shows a much greater sensitivity to the 3-sigma variation in R_{SD} and DIBL. While the range of the strained-$Si_{0.45}Ge_{0.55}$ velocity enhancement factor in Figure E4 is rather larger, the limits of the distribution are still representative of a fairly mild velocity gain compared to the 2.4x mobility enhancement observed in these devices. In Figure E5 the sensitivity to the parasitic correction factor in the virtual source and transconductance effective velocities are explored for 150 nm long strained-$Si_{0.45}Ge_{0.55}$ and Si devices. The correction factor for both the virtual source velocity and the transconductance velocity is approximately 0.2. Examining Figure E5 we see that the correction factors for both υ_{gmi} and υ_{xo} are low enough such that variations in the extraction factors R_s, C_{inv}, and DIBL lead to relatively small variations in the extracted velocities.

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