Peak Power Tracking for a Solar Buck Charger

by

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Abstract

This thesis discusses the design, implementation, and testing of a buck converter with peak power tracking. The peak power tracker uses a perturb and observe algorithm to actively track the solar panel's peak power point and a global sweep algorithm accounts for startup and multiple local maxima. The tracker takes the place of the current mode loop in the converter's control scheme by providing a battery with peak charging current. A voltage mode loop is also designed to take over control from the tracker to complete the multi-loop structure. A solar panel simulator is designed to mimic the characteristics of an actual solar panel to allow careful testing of the tracking algorithms. A test circuit board is built and its operation is verified. Finally, the power extracting potential of the active tracking method from this thesis is compared to two simpler solar regulators.

VI-A Company Thesis Supervisor: Jay Celani
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I thank my M.I.T. thesis advisor, Professor David J. Perreault, for his guidance and help in the writing of this thesis. His continual patience and encouragement helped to make my thesis process an enjoyable experience.

Finally, I would like to thank my parents for the love and support they have given me my entire life. Particularly, over the past five years at M.I.T., great life advice was always available when I needed it, and even when I did not think I needed it. From preparing me for my first spelling test in grade school to helping me move into my dorm freshman year, they have been an integral part of my life. I would not be where I am today without them.

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Chapter 1

Introduction

With the technology available, there is a limit to the amount of solar energy that can be captured by photovoltaic (PV) cells for a given amount of solar irradiation. It is, of course, desirable to operate PV cells at this upper limit in order to extract the maximum amount of energy from this renewable source.

1.1 Solar Panel Characteristics

In order to figure out how to extract maximum power, it is useful to understand the electrical characteristics of a solar panel. Under illumination, the typical panel has a characteristic open-circuit voltage and short-circuit current. These two operating points represent zero-power points since the panel generates no current at the open-circuit point and no voltage across the terminals at the short-circuit point, and the power delivered by the panel is defined as the voltage across its terminals multiplied by the current it sources. If the goal is to extract power, then the zero-power points are not desirable operating points. Figure 1-1 shows the current vs. voltage (I-V) measurements of an actual solar panel that I characterized outside on a fairly sunny day. The panel is a 15 Watt, 30 cell, amorphous panel from Topray Solar Company.

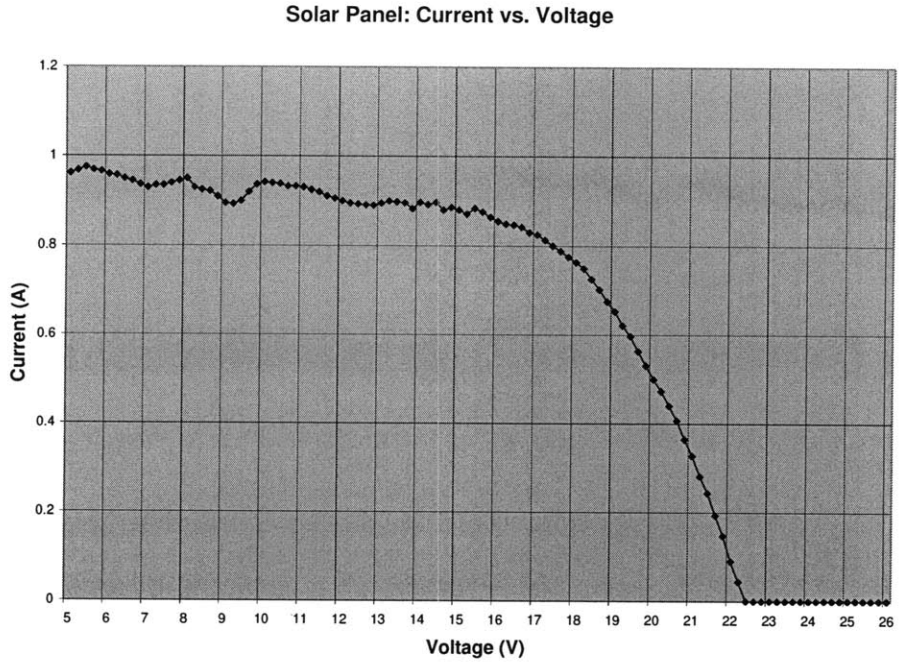

Figure 1-1: Current vs. voltage characteristics for Topray solar panel

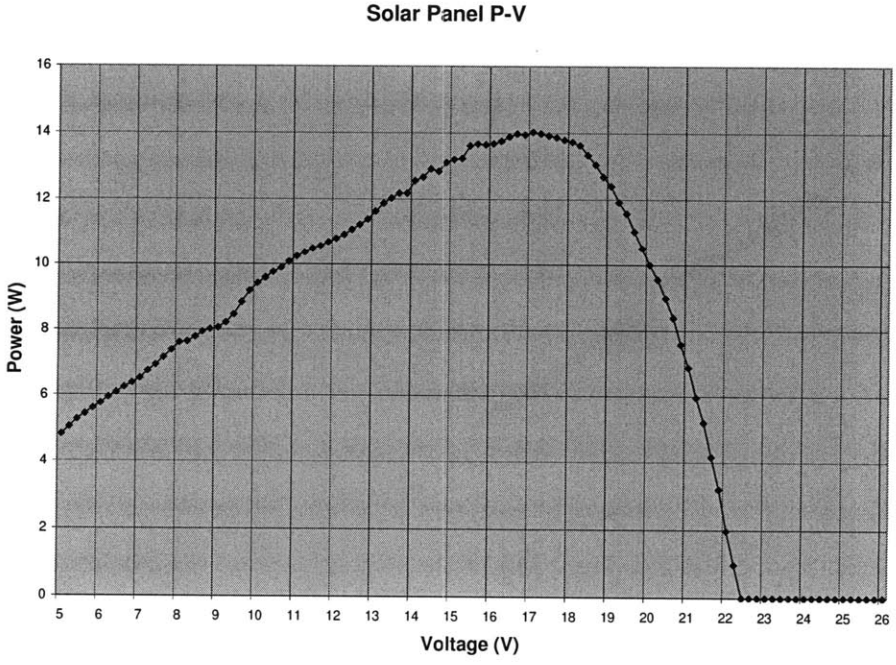

Figure 1-2: Power vs. voltage characteristics for Topray solar panel

The data is not perfectly smooth due to changing irradiance levels as clouds passed by. Figure 1-2 shows the associated power vs. voltage curve where there is a certain operating voltage (and current) that delivers peak power to its load. We can see from Figure 1-2 that the peak power point in this case is at approximately 17V. In this paper, I tend to refer to the panel's operating point as a voltage. From Figure 1-1 we can see that for a given insolation every voltage has a corresponding current so it would be just as appropriate to refer to the operating current.

It is now evident why we don't want to simply connect a solar panel directly to a battery. Let's say, for example, that we have an 8V battery that we want to charge. Direct connection to the solar panel would cause the panel to be operating at 8V. If we check the 8V operating voltage in Figure 1-2, we see that 8V is not even close to the peak power point. This is why we need a power converter, which takes one input voltage and supplies another voltage with little power loss. In the previous example, we would want a buck converter that supplies the 8V battery while drawing an amount of current that causes the solar panel to sit at its peak power point (17V). Now we are extracting maximum power from the solar panel.

There is another problem, which is the tendency of the peak power point to change as the panel heats up. While the panel transforms solar energy into electrical energy, it also dissipates a significant amount of energy in the form of heat. Figure 1-3 shows real data taken from a SunSei amorphous solar panel. The power vs. voltage characteristics are shown for different panel temperatures. We can see how the curve shifts inward and the peak power point shifts left as the temperature of the panel increases. As the panel temperature changes from 35 degrees C to 85 degrees C, the peak power point changes from about 13.7V to about 11.8V. Therefore, if we use a converter and fix the solar input at 13.7V, we will be extracting peak power until the panel starts heating up. When the panel gets hot, it will be operating at a voltage higher than the peak power point, since the peak power point has shifted to the left as shown in Figure 1-3. Figure 1-4 shows the same trend for a MySoldius monocrystalline solar panel. Notice how there is a larger price to pay for not accounting for the temperature shift.

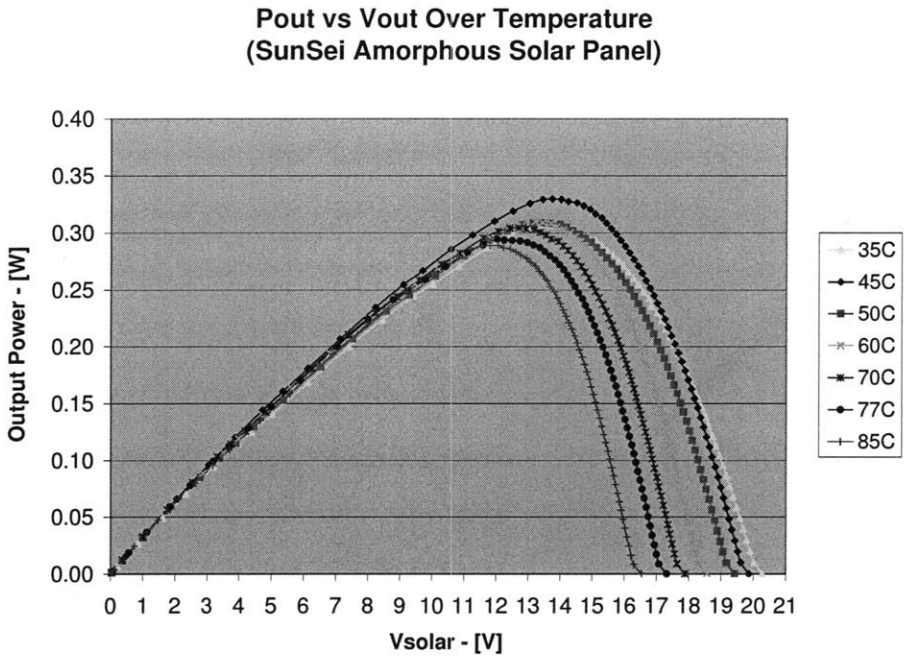

Figure 1-3: Current vs. voltage characteristics over various temperatures for a SunSei amorphous panel

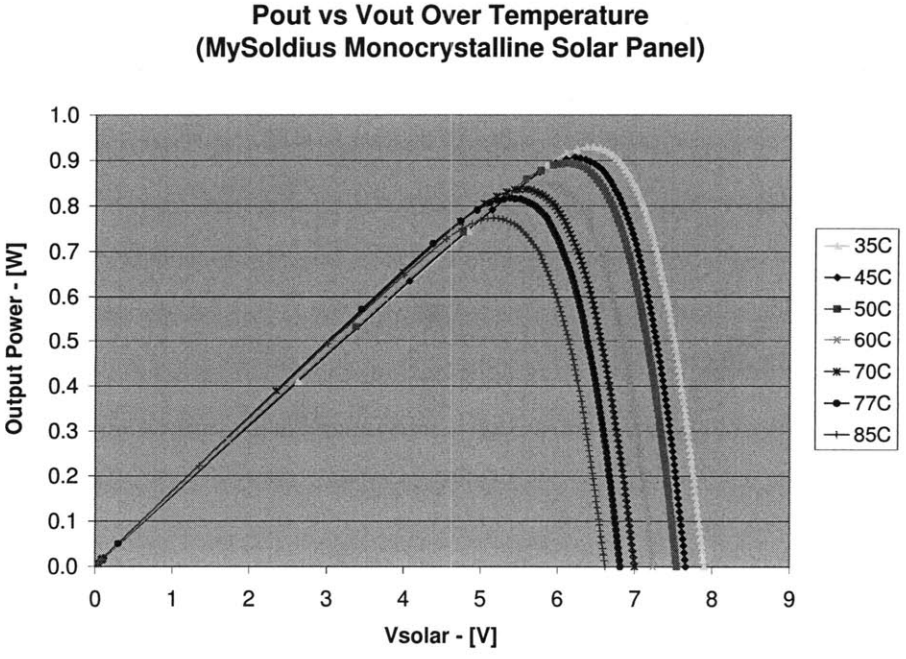

Figure 1-4: Current vs. voltage characteristics over various temperatures for a MySoldius monocrystalline panel

1.2 Previous Work

There has been extensive work done in the field of peak power tracking for PV arrays. This section provides a general review of previous work done with a few specific examples of peak power tracking methods that are especially relevant to this thesis.

One paper performed a comparison of the energy extraction capabilities between an active peak power tracker and a constant voltage system [1]. The tracker that was used was a perturb and observe system, which perturbs its operating point, measures the power change, and then perturbs its operating point again in the direction of increasing power. This allows the system to climb the power hill and dither back and forth at the peak. The constant voltage system requires the user to program the converter to operate the solar panel at a fixed voltage. Solar panel characteristics are widely available and so the peak power point can easily be programmed in. The experiment used in the paper to determine system effectiveness of extracting energy from a solar panel was to define system efficiency as: $\eta_{MPPT} = \frac{\int_0^t P_{actual}(t)dt}{\int_0^t P_{max}(t)dt}$

This formula means that system efficiency (or its effectiveness of extracting power) is defined as the ratio of actual power produced to maximum potential power available. P_{actual} was the actual power produced by the solar panel. At the same time, P_{max} was determined by measuring solar irradiance and the PV array temperature with a pyranometer and a thermistor. Since both P_{actual} and P_{max} change with light intensity and panel temperature, both variables are functions of time. The averaged results from this study are shown in Table 1.1. We can see from these results that the perturb and observe method operated the panel at a higher average power point than the constant voltage method.

	Perturb-Observe	Incremental Cond.	Constant Voltage
Array	96.5%	98.2%	88.1%
Simulator	97.2%	98.5%	92.7%

Table 1.1: Overall efficiencies of tracking algorithms [1]

A simple tracking method that will be used for comparison in this thesis is the bang-bang method (a particular design was done by Maxim [2]). This design utilizes

the hysteresis of a comparator to control the shutdown pin of a buck converter. A "reservoir capacitor" [2, p. 2] on the converter input is charged by the solar panel when the converter is in shutdown. The converter is turned on when the capacitor reaches a certain level and power is transferred. When the capacitor again drops below a certain level the shutdown pin is engaged again and the cycle repeats. This method is essentially a programmable dither and can be set to dither about the peak power point. This method would, however, require temperature compensation to account for the shifting peak power point.

Another tracking method is the input regulation scheme, which Linear Technology's LT3652 uses [3]. The LT3652 is a monolithic step-down battery charger with a programmable current of up to 2A. The unique feature of this design is the input regulation scheme on its input. When its V_{inREG} pin drops below a certain reference voltage, the output charge current is reduced, thus regulating the input voltage. When used with a solar panel input, the input regulation loop can be used to program peak power. The charge current will then servo to the maximum charge current [3, p. 7]. This method still needs temperature compensation. However, compared to the bang-bang method, the input regulation scheme allows the user to program a specific operating voltage and the battery is constantly being charged by the reduced current, while the bang-bang method cyclically charges and then shuts down.

A specific design that was very influential to my design was Joseph Duncan's, "A Global Maximum Power Point Tracking DC-DC Converter" [4]. Duncan uses the perturb and observe algorithm that was used in the comparison paper [1], to keep the system operating around a local maximum. Again, this involves changing the operating point of the solar input and then changing the operating point in the same direction or opposite direction when we observe power increasing or decreasing, respectively. The process repeats as the system climbs toward the peak power point. Duncan also uses a global sweep method, which sweeps the entire operating range to assure that the system is dithering around the global maximum, and not a lower local maximum. There is also a supervisor system to control when each algorithm is engaged. The application for Duncan's design is for a boost, or step-up converter,

whereas the application to this thesis is for a buck, or step-down converter.

There is one paper, in particular, which describes optimizing the perturb and observe method [5]. If the perturbations of the operating point are relatively large, the system can adjust more easily for rapidly changing irradiance conditions but the dithering of the operating point at steady state would incur some losses. For smaller perturbations, there would be less loss at steady state but the system could become unstable for rapidly changing irradiance conditions since the system would not be able to keep up. Results showed that it would, in fact, be beneficial to design this perturbation step size specific to the panel and converter being used. The step size trade off from this paper is discussed later in this thesis, after the design is presented.

1.3 General Approach

We have now seen from Figure 1-3 and Figure 1-4 that the peak power point changes with operation, and so it would be desirable to have the converter track that peak power point. In this paper, I will design a peak power tracking circuit and a buck converter. The tracker will take the place of the converter's current mode loop and provide peak charging current to the load. A voltage mode loop will also be designed to take control from the tracker near regulation of the load. After designing and testing the peak power tracking converter, I will compare its energy extraction potential with the simpler methods presented in the previous section. An active tracking system that is more effective and more convenient at extracting peak power from a solar panel would warrant the development of a peak power tracking charger integrated circuit.

1.4 Block Diagram

The purpose of the system is to deliver current to the battery using the power generated by the solar panel under illumination. The system block diagram in Figure 1-5 shows the solar input with its characteristic combination of V_{solar} and I_{solar} creating

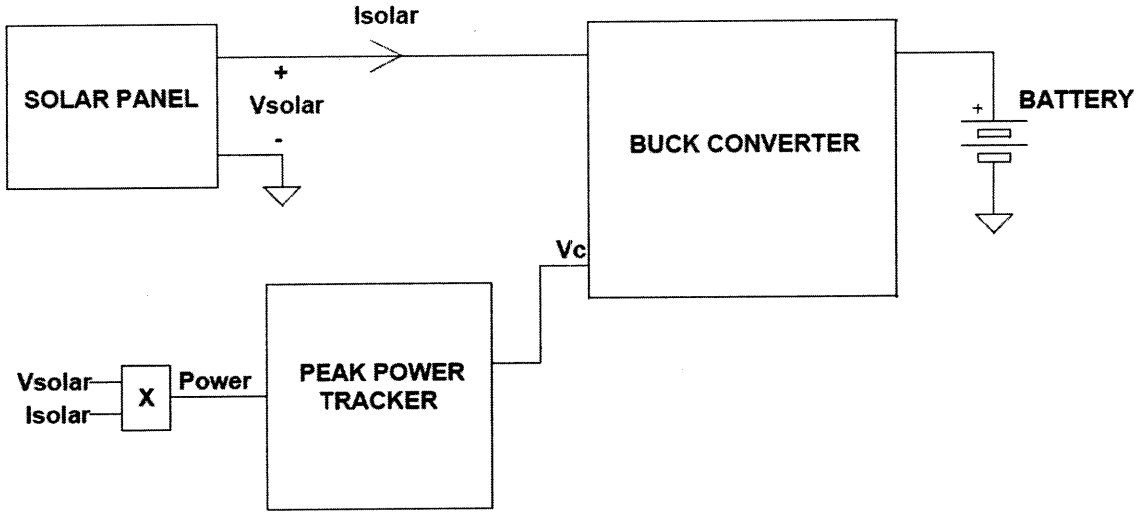

Figure 1-5: System-level block diagram of the solar powered battery charger with peak power tracking

an input power, P_{solar}, to be transferred to the battery. As discussed in Section 1.1, a buck or boost converter is required to step the voltage up or down, respectively, from the solar input to the battery output. This paper discusses the design of the system with a buck, or step-down, converter since the V_{solar} that is used ranges from 0-25V and the "fully-charged" battery simulator is set to 5V. The system transfers power while stepping the voltage down and the current up. The panel simulator used has a peak power point of about 17.5V and we saw from Figure 1-3 that the peak power point only changes by a few volts as the panel heats up. Therefore, for this application, it is safe to say that there is no use for the panel to be operated at less than or even near 5V, and so a buck converter is sufficient.

The main feature of the system is the peak power tracker, which takes a reading of the solar power as input and outputs V_c, or the control voltage. V_c controls the input operating voltage of the buck converter, which in this case, is the operating voltage of the solar panel. The tracker regulates the operating point of the solar panel to allow the buck converter to extract peak power and deliver that power to the battery.

1.5 Overview

This paper is organized as follows: In Chapter 2, the design and implementation of the peak power tracker is described and simulation results verify its operation. In Chapter 3, the design and implementation of the converter is described and particular attention is paid to its control loop scheme. Simulation results are used to verify the operation of the converter. Chapter 4 describes the rest of the parts of the block diagram and the system-level operation is described. A test board is built to verify system operation along with simulation results. Chapter 5 analytically examines the power extracting capabilities of the system presented in Chapters 2, 3, and 4 compared to the bang-bang and input regulation methods presented earlier in this chapter. Finally, Chapter 6 provides a conclusion that discusses the relevance of the comparisons from Chapter 5 and proposes future work from this thesis.

Chapter 2

Peak Power Tracker

This chapter describes the design of the peak power tracker block from Figure 1-5. The first section explains the algorithms used by the tracker. Then the implementation of those algorithms is described. At the end of the chapter, LTSpice results are discussed.

2.1 Algorithms

2.1.1 Perturb and Observe Algorithm

The perturb and observe algorithm runs for most of the operation time. It is responsible for maintaining the peak operating point and tracking that point as it moves with increasing panel temperature. The algorithm works cyclically with two main parts. A perturbation of the operating point results in a change in power delivered by the panel, which can be verified by looking at the power vs. operating voltage characteristics from Figure 1-2. Any finite change in the operating voltage will result in a change in power, as long as the change keeps the operating voltage exclusively to one side of the peak power point.[1] The first part of the cycle is determining whether power rose or fell as the perturbation was made. The second part of the cycle is to

[1]We can imagine a perturbation that originates from the left side of the peak power point, for example, and results in an operating voltage to the right of the peak power point at exactly the same power level as the perturbation originated from. This zero-change phenomenon is actually not a problem since a perturbation in the wrong direction will self-correct.

then perturb the system again in the same direction (on the x-axis in Figure 1-2) if power rose and the opposite direction if power fell. If we continuously repeat this cycle, the system will climb the power hill until it gets to the top, at which time it will dither back and forth. Any shift in the peak power point will be tracked by the circuit.

2.1.2 Global Sweep Algorithm

For less than one percent of the total operation time, a global sweep algorithm runs. The concept is identical to Duncan's, but again, the implementation is different. The program interrupts the perturb and observe program and sweeps the entire operating range, measuring power delivered by the solar panel at every interval. The peak power point is recorded and the operating point is set to that peak power point. Then the perturb and observe takes over again. There are two main functions of the global sweep. Its first function is to account for the system's startup. It is possible, upon startup, that the operating point is pinned high or low. After a global sweep runs (about every 5 seconds in my design) the operating point will be set at (or very near) the peak power point. The second function of the the global sweep is to decipher the absolute peak power point when there are multiple peaks. It is possible for the perturb and observe to get stuck dithering about an operating point that is a local maximum and not the absolute maximum.

2.2 Tracker Block Diagram

The algorithms from the previous section are implemented using three main blocks, as seen in the block diagram in Figure 2-1. The same circuitry is actually used for both algorithms. The front-end of the tracker is the sample and hold and the power sensor. This block samples the power of step n and compares it to the sample from step n-1. It then makes the decision of whether to step the control voltage up or down. The back-end of the tracker is the control voltage stepper. During the perturb and observe, this block ramps the control voltage up or down, depending on the command

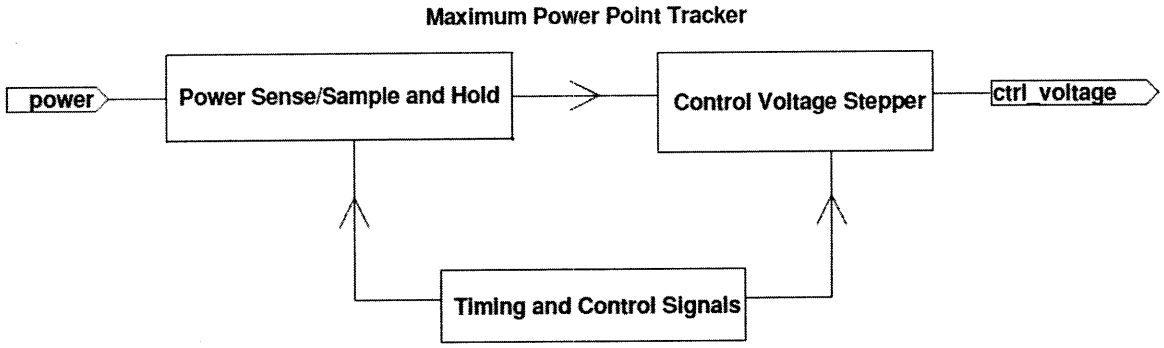

Figure 2-1: Block diagram of peak power tracker

from the front-end block. During the global sweep, the control voltage corresponding to the peak power point is saved and loaded. The timing and control signals regulate the operation of the two blocks and also engage the global sweep to interrupt the perturb and observe.

2.3 Tracker Implementation

This section describes the implementation of each tracker algorithm described in the first section of this chapter. Since the timing circuitry block from Figure 2-1 controls the operation of the algorithms, the implementation of that block is described first.

2.3.1 Timing Circuitry

Looking at the timing circuitry in Figure 2-2, the LTC1799 is a precision oscillator with a programmable frequency [6]. Its clock signal drives a cascade of four 4-bit binary counters (74HC163) [7]. Cascading the counters as shown in Figure 2-2 creates an effective 16-bit counter, allowing the use of a large range of clock frequencies. For example, the Q1 pin of the first counter has half the frequency of the Q0 pin on that same counter and the Q0 pin of the second counter has half the frequency of the Q3 pin of the first counter. Also, while Q0 to Q3 are all square waves with 50 percent duty ratio, the TC pins are short pulses with the same frequency as their corresponding Q3 pins.

The first counter creates the signal 800u from its Q3, which has a pulse width of

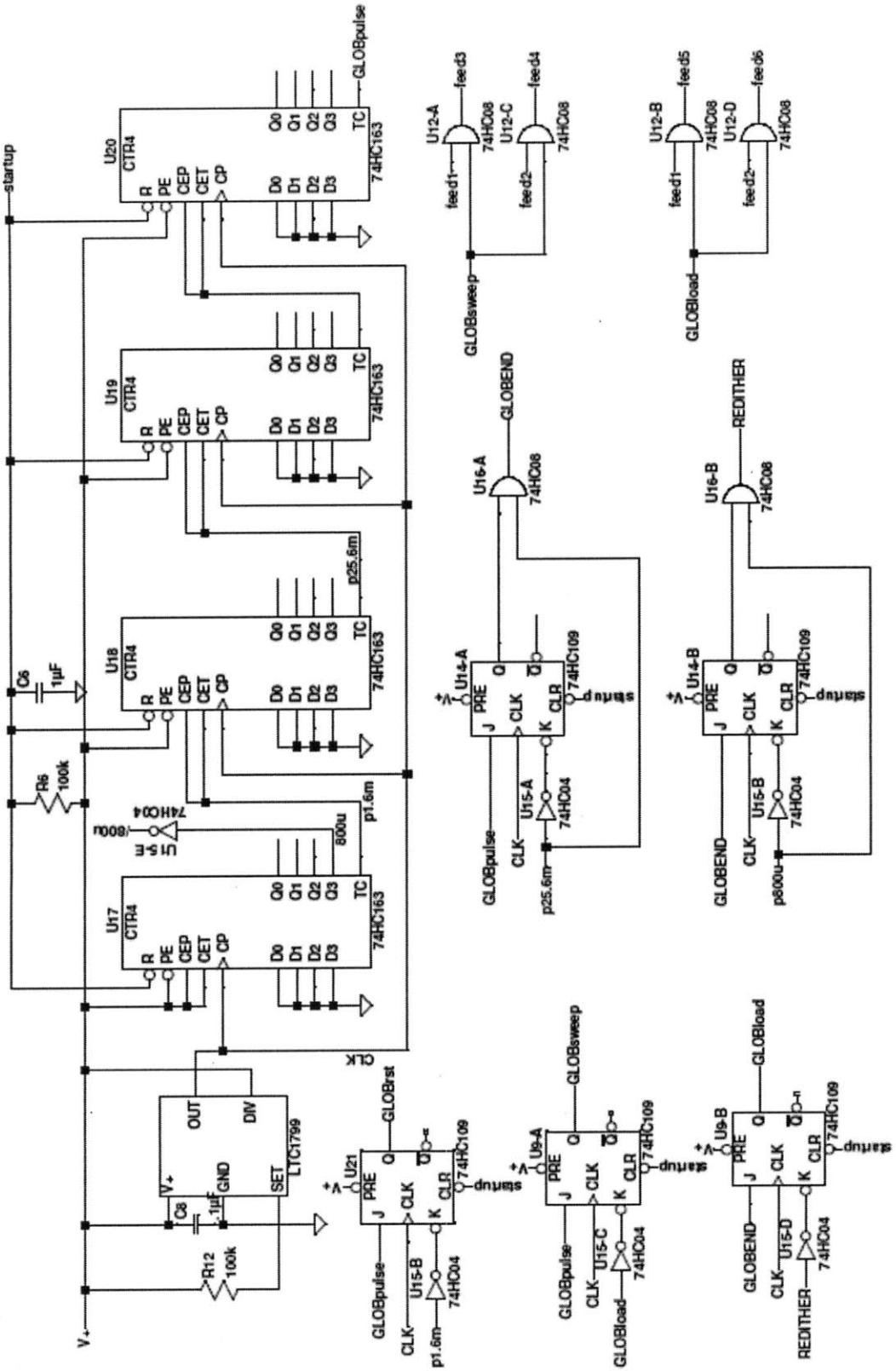

Figure 2-2: Schematic of timing and control circuitry

800μs and its compliment, /800u via an inverter. These two complimentary signals are used to control the sample and hold section of the front-end block. The fourth counter contains the lowest frequency signals, including GLOBpulse, which is used to interrupt the perturb and observe and engage the global sweep. The GLOBsweep signal changes the functionality of the front-end block so that the circuitry can be used for the global sweep. The GLOBload signal conditions the back-end block to load the control voltage corresponding to the peak power point. The feed3/feed5 and feed4/feed6 are meant to mimic feed1 and feed2, respectively, during the different phases of the global sweep.

2.3.2 Perturb and Observe Implementation

The "observing" is done by the front-end circuitry of the tracker. From Figure 2-3, $V_{powerin}$ is alternately sampled across capacitors C1 and C2. C7 and C12 assist to filter out high frequency noise. Since GLOBsweep will be low during this time, the complimentary clock signals, 800u and /800u, pass through to control the two switches, U4-A and U4-B. Every sample is compared to the previous sample, which is being held on the other capacitor. U8-B, a JK flip-flop, is configured in such a way that if its J input receives a zero value, its outputs will keep their previous state and if the J input receives a high value, its outputs will change state. Therefore, at a particular moment, if the U4-A switch is closed and C1 is taking a sample, the U7-A comparator compares that sample to the previous sample on C2. If C1 sees a higher voltage, U7-A will go high, causing the output of the AND gate, U1-C, to be high, and the output of the NOR gate U10-A to be low. Thus, the JK flip-flop keeps the same state and the control voltage is stepped in the same direction as its previous step. This is what we want to happen since power increased. In a similar analysis, if C1 does not see a larger power reading during its sample, the JK flip-flop changes state, and the control voltage is stepped in the opposite direction from its previous step.

The "perturbing" is done by the back-end circuitry. The RampDirection input in Figure 2-4 comes from the inverting output of the decision-making JK flip-flop from

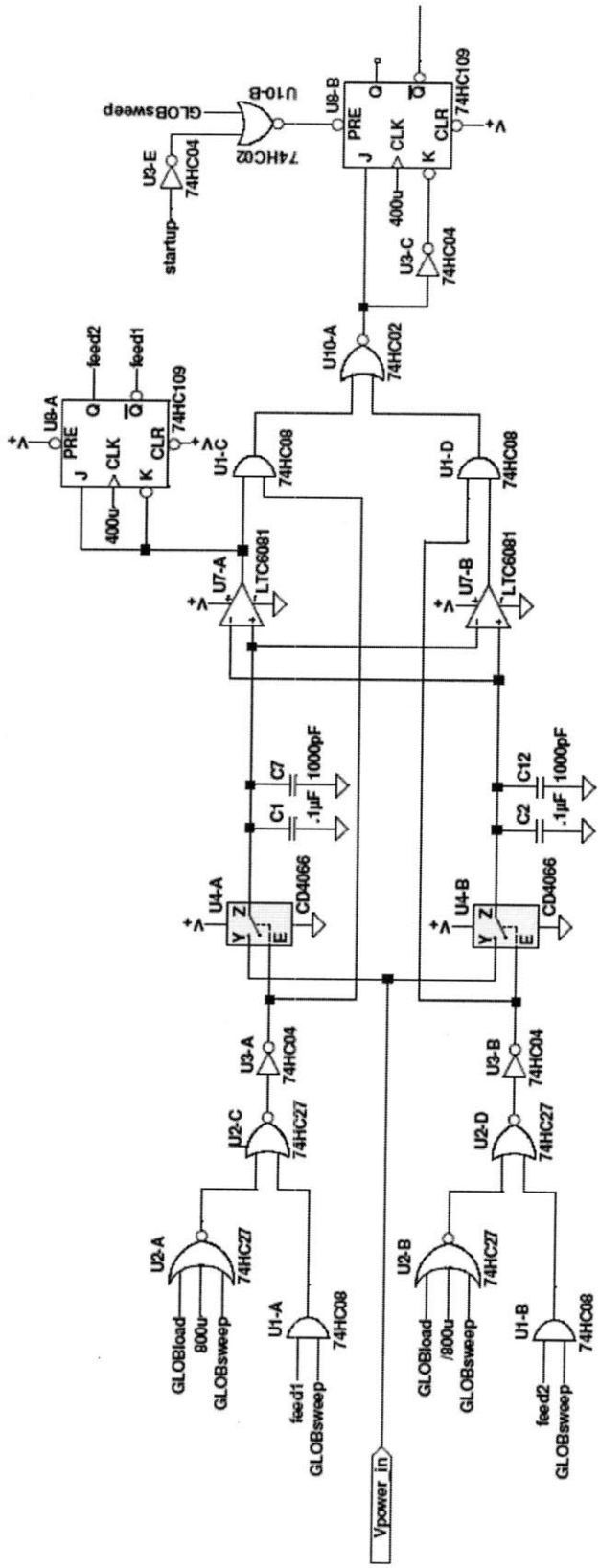

Figure 2-3: Schematic of front-end circuitry

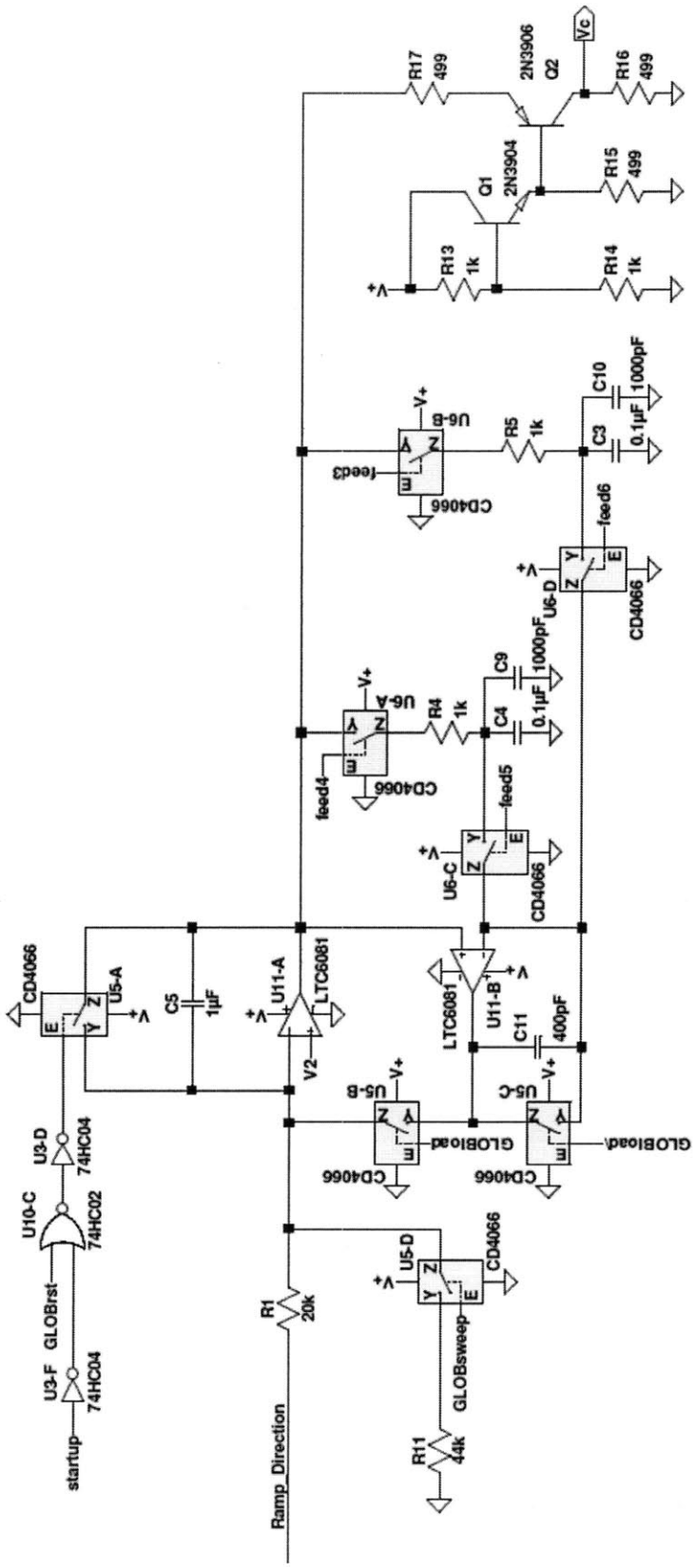

Figure 2-4: Schematic of back-end circuitry

the front-end. During the perturb and observe, all switches in the back-end circuitry are off. The U11-A op-amp is left in an integrating configuration with input resistor R1 and feedback capacitor C5. Therefore, if RampDirection is low, the output of the integrator will ramp up and if RampDirection is high, the output will ramp down. A smaller feedback capacitor allows for a quicker charge rate for a given current and a smaller input resistor allows for a larger charging current. Therefore, on the test board, R1 was implemented as a variable resistor, so the ramp rate could be changed quickly. Since the output of the integrator is referenced to half the supply voltage, the output network level-shifts the control voltage (Vc) so that it is referenced to ground. U11-A, the LTC6081, is a precision rail-to-rail op amp [8]. It is important that the op amp be able to rail high in order to maximize the control voltage range. Also, this precision op-amp has a maximum offset voltage of $70\mu V$, which is important to assure that the integrator ramps up and down at the same rate.

2.3.3 Global Sweep Implementation

During the global sweep, we want to measure the entire operating range and load the control voltage corresponding to the peak power point. The global sweep, which is engaged by the GLOBpulse signal, is performed in three phases, the reset, the sweep, and the load. The control signals that perform the three phases can be seen in Figure 2-5 and originates from the timing circuitry in Figure 2-2.

The purpose of the reset phase is to pin the control voltage to zero so that the tracker can begin its sweep of the entire operating range. The 1.6ms GLOBrst pulse shorts out the integrator's feedback capacitor as shown in Figure 2-4, resetting the integrator output to the reference and the Vc output to zero.

The front-end and back-end work together during the sweep phase to find the control voltage corresponding to the peak power point. While the integrator sweeps the control voltage range, the front-end monitors and records the peak power level. The GLOBsweep signal assures that the sampling switches on the back-end (U6-A and U6-B) are synchronized with the sampling switches from the front end. This allows the capacitors C3 and C4 to sample the control voltages corresponding to the

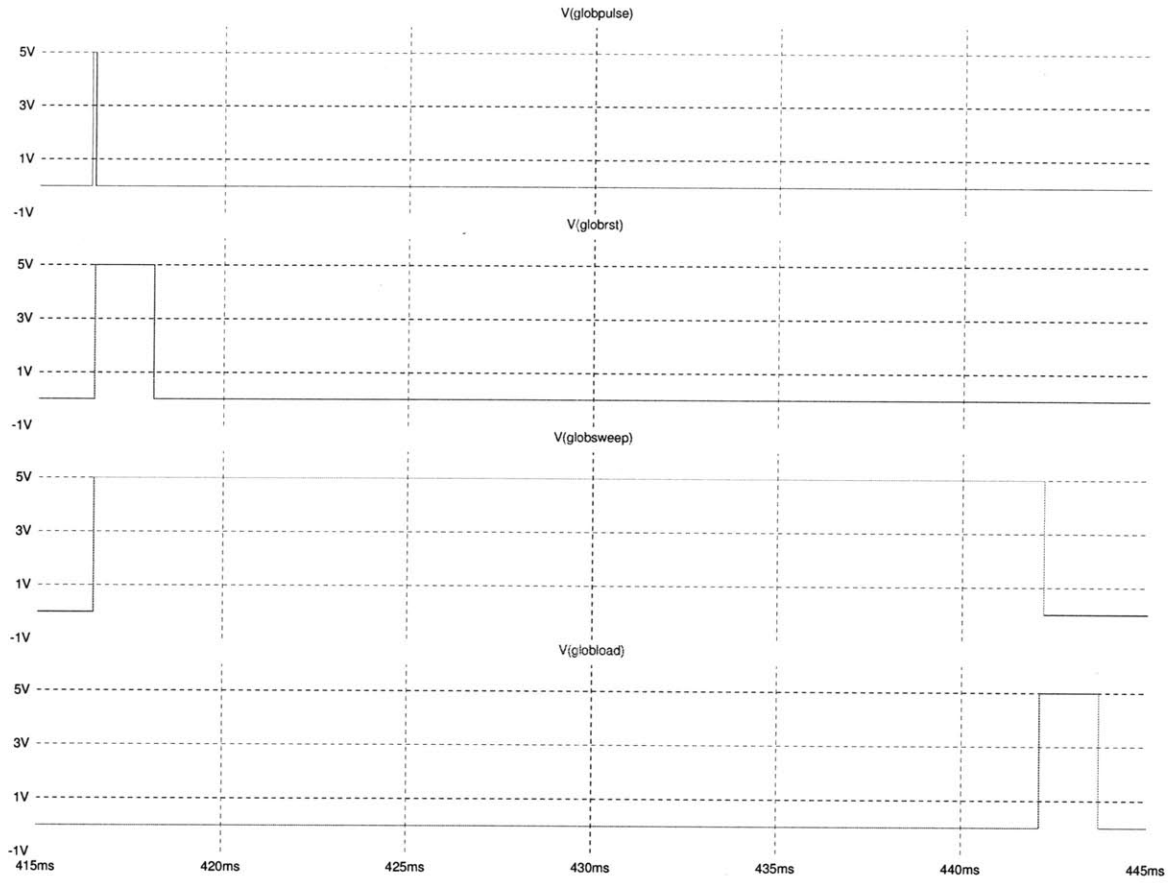

Figure 2-5: Global sweep timing signals

sampled power levels on the front end. The next paragraph describes this process in more detail.

The U8-B JK flip-flop is preset by the GLOBsweep signal so that the /Q pin is fixed low. This causes the integrator to ramp the control voltage up, but the ramp rate is faster than the perturb and observe ramp rate. The reason for this is GLOBsweep switches resistor R11 in parallel with the integrator's input resistor R1. With a faster ramp rate, the operating range is more coarsely sampled. However, a faster sweeping speed is well worth the trade off of slight inaccuracies since the perturb and observe can fine tune the tracking when it takes over. As the operating range is swept toward the peak power point, the front-end sees a steadily increasing power level. Since GLOBsweep is high, feed1 and feed2 control the sampling switches (U4-A and U4-B). If feed1 is high and C1 is sampling the steadily increasing power

level, the comparator U7-A will be high. On the next clock edge of the U8-A JK flip-flop, feed2 will go high and cause C2 to start sampling the input power level while C1 saves its power level for comparison. The two capacitors continue switching functions until the power level starts decreasing, in which case the "off" capacitor holds the peak power level. Since the largest value is always saved, multiple power peaks are accounted for. During the sweep phase, feed3 and feed4 are equivalent to feed1 and feed2, respectively. Therefore, C3 and C4 on the back-end sample the control voltage corresponding to the power level sampled by C1 and C2, respectively. If, for example, C1 were to end up with the peak power level, then the peak power control voltage would be saved on C3.

The load phase of the global sweep loads the saved peak power point onto the output of the integrator. While GLOBload is high, feed5 and feed6 are equivalent to feed1 and feed2, respectively. If, for example, C3 holds the peak power point, then feed6 will turn the U6-D switch on and load the peak power point onto the inverting input of the U11-B op-amp. The non-inverting input (which is the output of the integrator) will quickly settle to the same value through the feedback of the integrating op-amp. Capacitor C11 functions as a loop compensator. Now, the control voltage corresponding to the peak power point is loaded and the tracker can resume the perturb and observe.

2.4 LTSpice Simulation of Tracker

Figure 2-6 shows the results of an open-loop simulation of the tracker described in this section. The input is a simple sine wave so that we can see how the perturb and observe reacts to increasing and decreasing power levels. We can also test the global sweep by checking if it loads the correct control voltage after sweeping the entire operating range. For the purposes of the simulation, the global sweep is engaged once every 60ms so that it can be seen twice in Figure 2-6 with acceptable resolution.

At about the 5ms mark in Figure 2-6, we see the control voltage (Vc) reset to zero and then ramp up as it looks for the global peak power point. At about 33ms, Vc

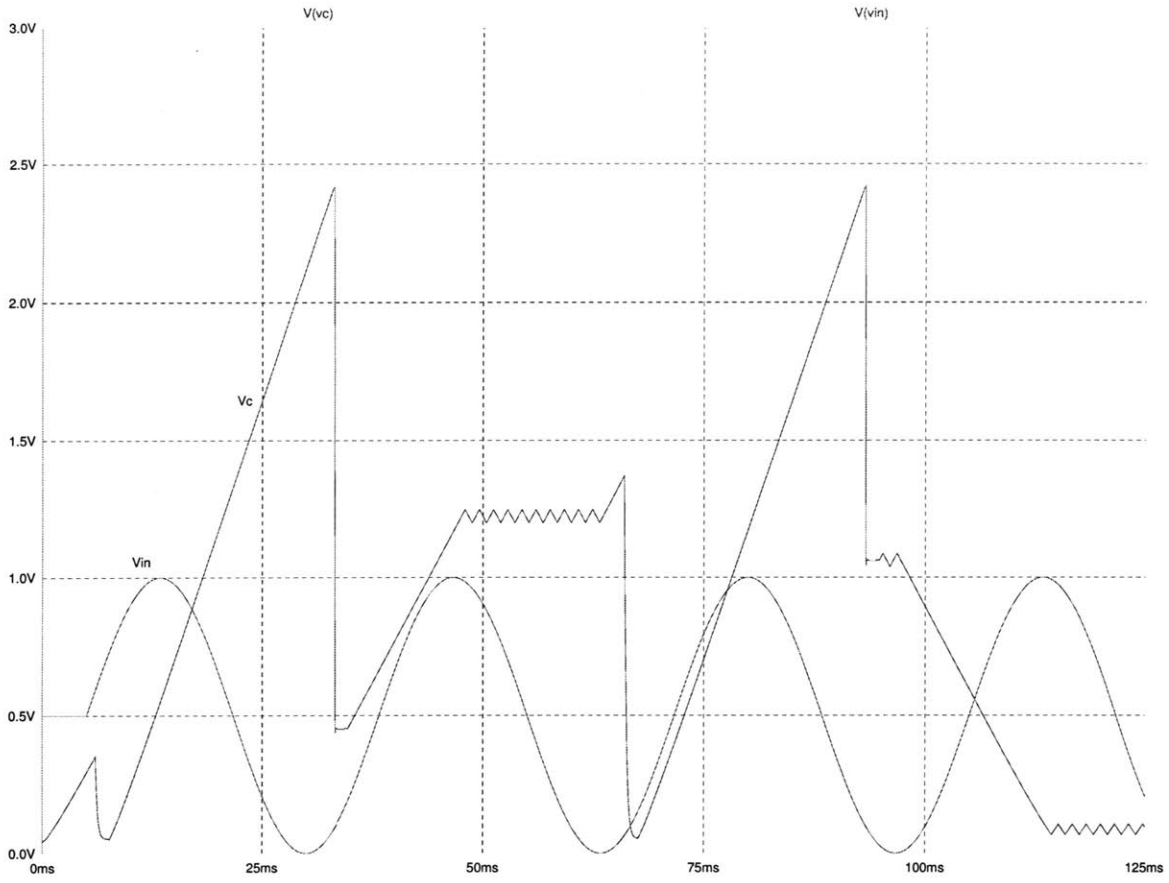

Figure 2-6: Open-loop simulation of tracker with sine wave input

quickly settles to the value that corresponds to the peak point in the sine wave. At about 35ms, the perturb and observe takes over and we see Vc ramping in a single direction. This is what we expect since the sine wave is increasing and the tracker thinks it is climbing the power curve. When the sine wave starts to decrease at about 47ms, Vc starts dithering back and forth. This is also what we expect since the tracker thinks it is going in the wrong direction and so it changes its direction every step.

Chapter 3

Converter

This chapter goes through the design, implementation, and testing of the converter block of the system. This chapter starts with the choice of a buck converter with voltage mode control. Then the design and implementation of the converter is described. Finally, the results of an LTSpice simulation are shown.

3.1 Buck Converter

The basic topology of a DC-DC buck, or step-down, converter is shown in Figure 3-1. In an ideal converter, the voltage across the load in steady state will be V_{out}=D*V_{in} [9], where D is the duty ratio of the switch. Since P_{out}=P_{in} in an ideal converter, I_{out}=I_{in}/D, so while the buck steps down the voltage, it steps up the current to transfer power with minimal loss.

As explained in Section 1.1, the choice of a buck as opposed to a boost is due to the desire to step down the voltage while conserving power. The next section discusses the control scheme of the converter.

3.2 Voltage Mode Control

Many modern converters use multi-loop feedback to control the charging process of a battery. A voltage mode loop compares the output voltage to a reference and adjusts

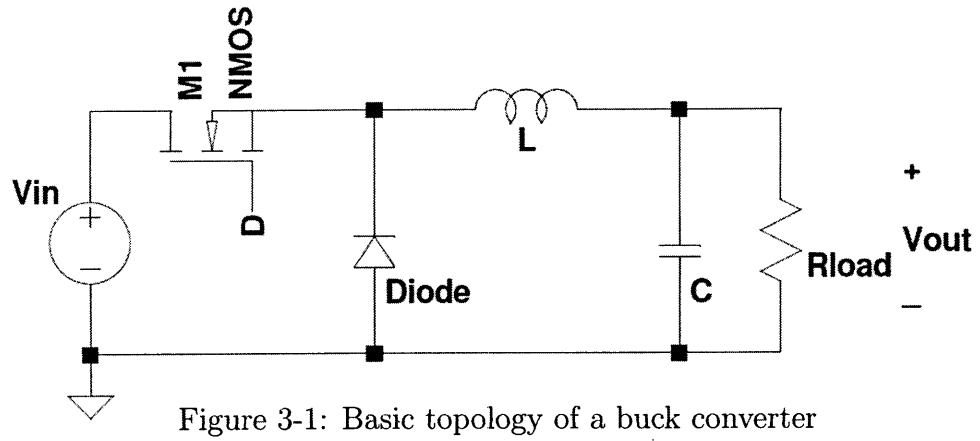

Figure 3-1: Basic topology of a buck converter

the duty ratio to achieve a final regulated output voltage. A current mode loop regulates the inductor current making it possible to directly regulate the maximum charge current since batteries have current limits. Moreover, a converter with multi-loop feedback is amenable to implementing a multi-stage charging process, in which a constant current is used to charge the battery with the battery's current limit until the battery becomes close to fully charged (a constant current charge). The voltage loop then takes over to complete the charge to the final voltage (a constant voltage charge).

Due to the application of the converter in this thesis, only a single duty ratio control loop is used, which, for most of the charging duration, focuses on controlling duty ratio to regulate input power to be at a maximum. Instead of using current mode feedback control, the converter is controlled by the peak power tracker described in the previous chapter. When the voltage mode loop senses that the battery is near full charge, it takes over control from the peak power tracker to finish the charge. Although we lose direct control over maximum charge current, it is not of much concern due to the application of the converter. The solar panel acts as a charge current limiter since it has a peak power point.

Figure 3-2 shows the topology of voltage mode control [10]. The output voltage is divided and compared to a reference in the compensator. The compensator output, COMP in Figure 3-2, is then compared to a sawtooth wave to form an adjustable duty ratio, based on the value of the COMP node. If, for example, V_{out} was too low,

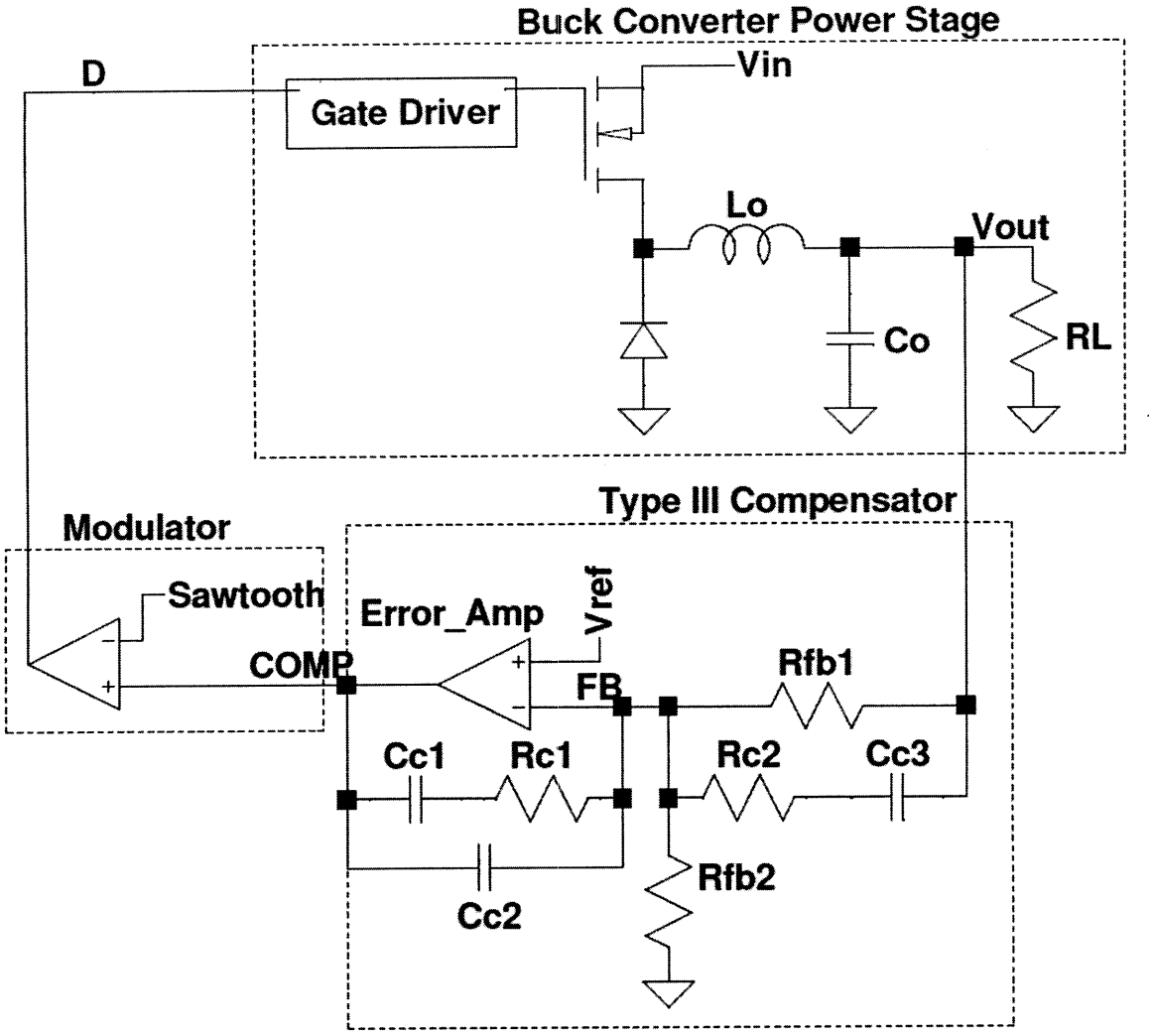

Figure 3-2: Basic topology of a buck converter with a voltage mode control loop [10]

then FB inside the compensator would be below $Vref$ and the error amplifier would create a larger duty ratio and a larger output voltage.

3.3 Converter Design

The converter design will be described in terms of the three blocks illustrated in Figure 3-2: the modulator, the power converter, and the compensator. The full schematic of the converter presented in this section is shown in Figure 3-3.

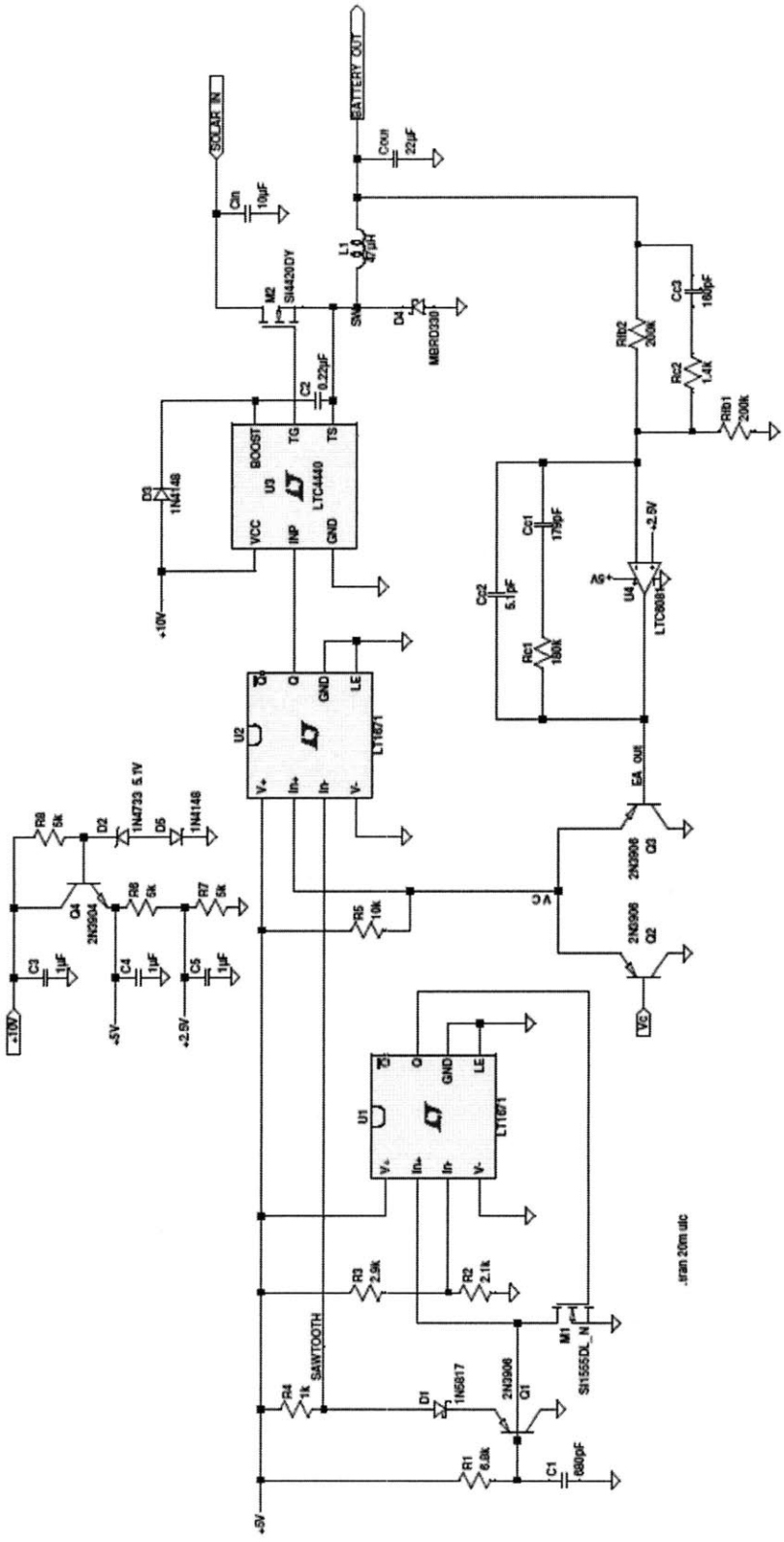

Figure 3-3: Schematic of power converter

3.3.1 Modulator

The modulator starts with the generation of the sawtooth waveform. From Figure 3-3, the reference 5V supply charges C1 through R1. The voltage on C1 is the non-inverting input to the comparator U1 and keeps increasing until it surpasses the reference on the inverting input. When the comparator trips, M1 turns on and the capacitor is quickly discharged. This process creates a sawtooth waveform across C1, which is level-shifted up to the node labeled SAWTOOTH. The SAWTOOTH signal is compared by comparator U2 to the output of the error amplifier (EAout) from the compensator, producing the duty ratio to control the power converter's switch. A larger value of EAout produces a larger duty ratio. R5 functions as a simple current source to drive Q3. This allows the emitter of Q3 to track the value of EAout. The purpose of the Q2-Q3 pair will be explained in the next chapter.

The values of R1 and C1 are chosen to produce a switching frequency of 346kHz. The comparators are both the LT1671, which is a fast, low power, ground-sensing comparator.

3.3.2 Power Converter

For the design of the power converter, we need to choose a switch, diode, and inductor that are rated at an appropriate current and voltage. A gate driver is also needed for the switch. Sizing the inductor involves weighing trade offs. In general, it is desirable to have a smaller inductor to save space and cost, however a smaller inductor will have larger ripple current. Since cost and space are not main considerations in this thesis, the inductor is sized to produce a peak-to-peak inductor current ripple of about 15%-20% of its DC value. If we assume that the solar input provides 6.8W of power[1], that the power converter is 91% efficient at transferring power[2], and that the output battery is 5V, the DC current through the inductor will be about 1.25A. A 47μH inductor results in a ripple current of 230mA peak-peak, or 18.4% of the

[1]The panel simulator that is used in the system testing has a peak power output of about 6.8W. The panel simulator is described in the next chapter

[2]the power converter's efficiency was determined experimentally

DC value. The 47μH inductor used has an average current rating of 2.5A and a DCR of 0.1Ω. The diode is the 3A 30V MBRD330 Schottky rectifier [12]. Besides appropriate power ratings, the MBRD330 has a low forward voltage drop and is very suitable for high frequency operation. The switch used is the Si4420DY N-Channel power MOSFET [13]. This device is rated at 12.5A and 30V, more than sufficient for the power levels being used. It also has very low $R_{DS(ON)}$ to help maximize the efficiency of the power converter. A gate driver is required to turn the switch on and off since power MOSFETs have a large gate capacitance and the U2 comparator cannot source enough current to drive the gate. The LTC4440 is a high speed, high voltage high side gate driver for an N-channel MOSFET [14]. Its 10V supply allows it to place almost 10V across the gate-source junction of the switch. The larger gate-to-source voltage results in a smaller $R_{DS(ON)}$ for the switch.

3.3.3 Compensator

The compensation of the voltage mode loop follows the technique presented in [10]. A type III compensator is used to provide the control loop with adequate phase margin. Figure 3-4 shows the bode plot of the converter transfer function from duty ratio to output, without compensation. The formula for the transfer function includes the effects of the equivalent series resistance (ESR) of the output capacitor and the DC resistance (DCR) of the inductor (about 0.1Ω). The converter transfer function, G_{vd}, is shown below. The values used to generate the bode plot are from the converter schematic in Figure 3-3. The load resistance is set to 4Ω to cause an output current of 1.25A.

$$G_{vd}(s) = V_{in}\frac{R_L(1+sR_{ESR}C_O)}{(R_L+R_{DAMP})+s[L_O+C_O(R_{ESR}(R_L+R_{DAMP})+R_LR_{DAMP})]+s^2C_OL_O(R_L+R_{ESR})}$$

Since the bode plot only shows a small phase margin of 8 degrees, it is apparent that the compensator needs to induce positive phase shift. The type III compensator, as shown in Figure 3-2, introduces 3 poles and 2 zeros to the system. Both zeros are placed at the frequency of the LC double pole to mitigate its effect and provide positive phase shift to allow for a larger phase margin at crossover. One pole is placed at the zero created by the output capacitance and its ESR to mitigate its effect. Another pole

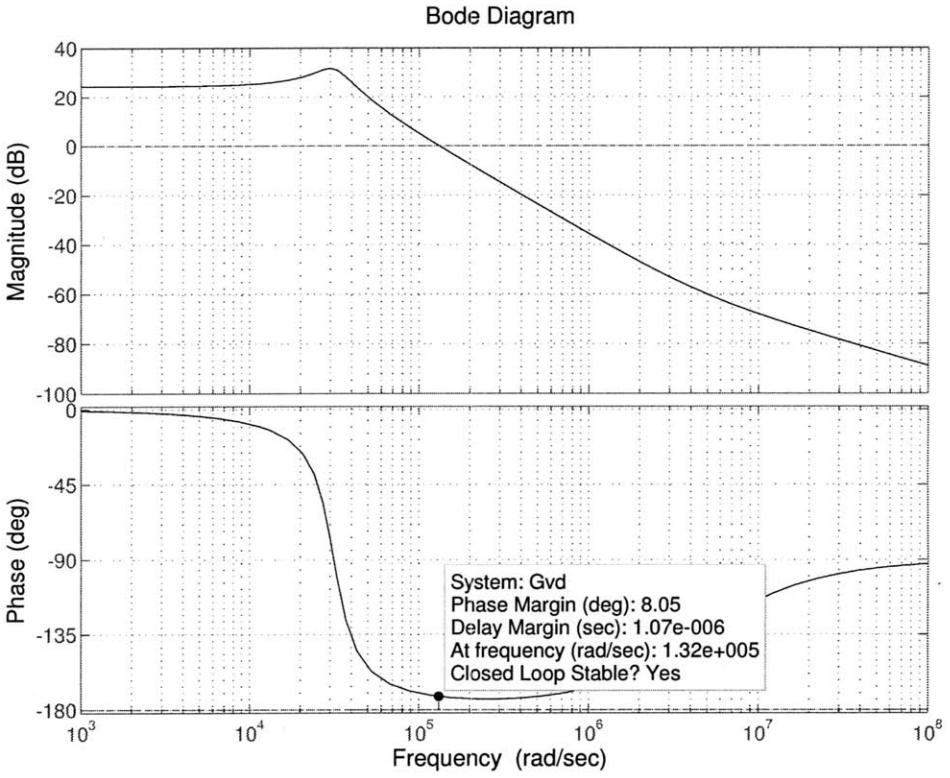

Figure 3-4: Bode Plot of Buck Converter Transfer Function from Duty Cycle to Output

is placed at approximately half the switching frequency to filter out high frequency noise from the switching. The last pole is at the origin for high loop DC gain[10]. Figure 3-5 shows the bode plot of the loop transfer function with compensation. The phase margin is now a very stable 66.5 degrees and the crossover frequency is located at the peak of the phase bump, which allows for stability even if the DC gain of the loop is changed.[3] We also notice that the crossover frequency is placed at approximately one-tenth the switching frequency to attenuate switching noise. The transfer function of the type III compensator is shown below. The MATLAB source code is found in Appendix A. In the code, Fm is the modulator gain, which is inversely proportional to the ramp voltage of the sawtooth wave.

$$G_c(s) = \frac{(1+sR_{C1}C_{C1})[1+s(R_{FB1}+R_{C2})C_{C3}]}{sR_{FB1}C_{C1}(1+sR_{C2}C_{C3})[1+sR_{C1}\frac{C_{C1}C_{C2}}{C_{C1}+C_{C2}}]}$$

3.4 Charger LTSpice Simulation

To test the voltage mode converter in LTSpice, a 17V supply is connected to the input to simulate the voltage of the peak power point. A 4Ω load is connected at the output to simulate the 1.25A charge current that would result with a 5V output and input at peak power. Additionally, a current source steps the load from 1.25A to 2.5A, and then back to 1.25A. The output voltage and inductor current are shown in Figure 3-6. The first plot shows the output voltage settling to 5V in about 200μs. The initial overshoot of 5V is expected since the output starts at zero, causing the error amplifier to force a duty ratio of 1. The second plot zooms in on V_{out} to show the transient response to the load steps. The first step is the transition from 1.25A to 2.5A as shown by the inductor current in the third plot. The maximum excursion is 300mV and the settling time is about 50μs. The third plot also shows the small ripple current on the inductor due to its large size.

[3]Changes in the input voltage level and effective load resistance will change the DC gain of the loop

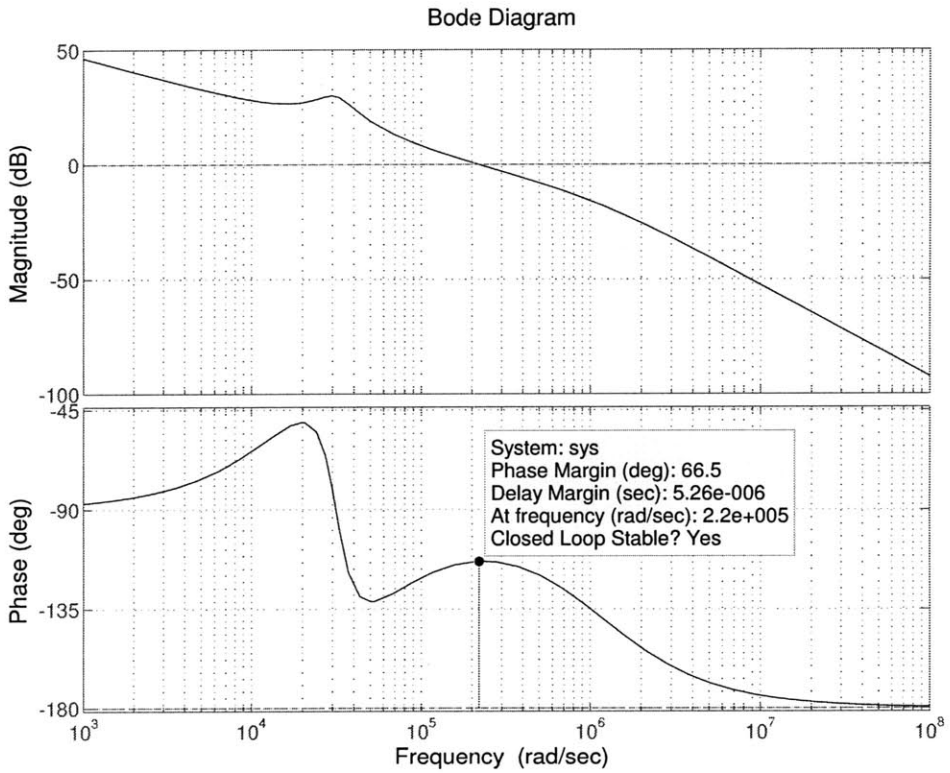

Figure 3-5: Bode Plot of Buck Converter with Type III Compensation

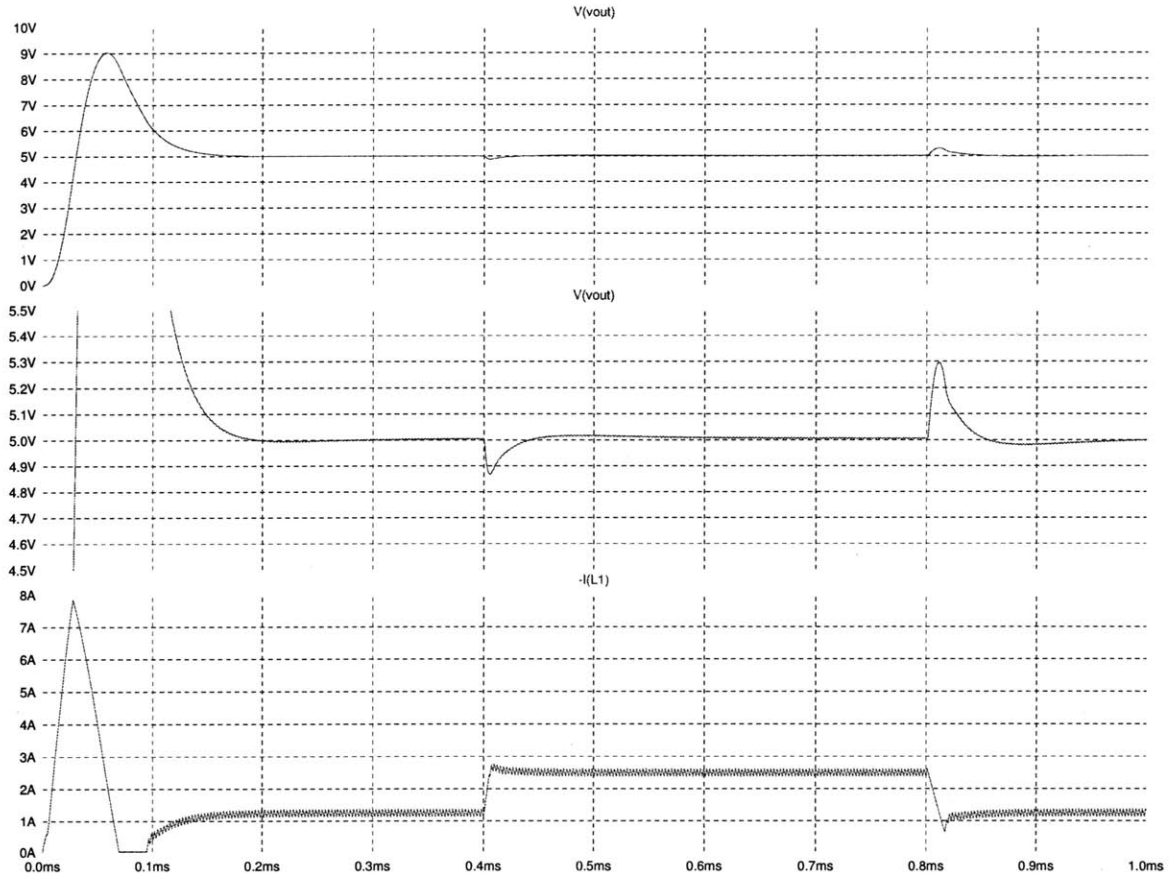

Figure 3-6: Closed loop simulation of buck converter with load step

Chapter 4

System Operation

We now return to the system block diagram from Figure 1-5. The design and operation of the two major blocks of the system, the peak power tracker and the buck converter, have now been described. This chapter begins by explaining the remaining components of the system and how the blocks work together to track the peak power point. LTSpice simulations and results from the actual test circuit are then shown. This chapter ends by discussing some of the main design concepts that affect the operation of the system.

4.1 Solar Panel Simulator

The solar panel simulator shown in Figure 4-1 is used in the LTSpice simulations and the test circuit board. The simulator receives a 25V input and is essentially a soft current limit circuit. The characteristics of the LTSpice version of the panel simulator are shown in Figure 4-2. To characterize the real panel simulator, an adjustable current load was used to sweep the operating current range and record the resulting voltage. A heating gun set to 80 degrees C forced air onto the panel simulator in order to keep it at a steady temperature and prevent variation in the transistors and resistors.[1]

The characteristics of the actual panel simulator are shown in Appendix B. Only a

[1]The gun was kept on the simulator at the same temperature during system testing for consistency

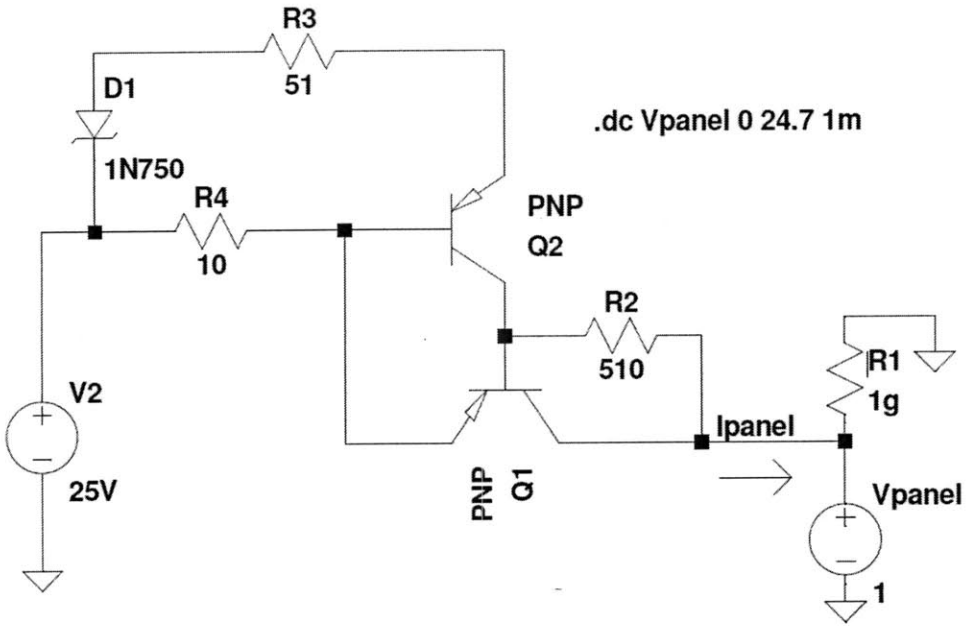

Figure 4-1: Solar panel simulator schematic

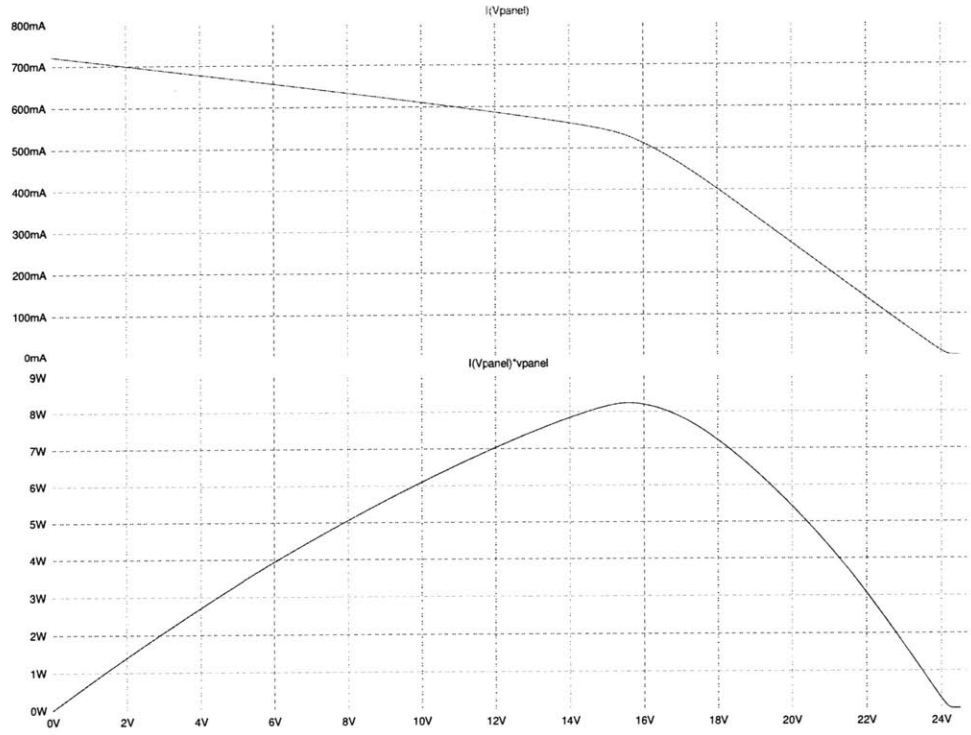

Figure 4-2: Characteristics for LTSpice solar panel simulator

limited range of operating points was measured since the methods that are analyzed in this thesis operate well within that range. The characteristics of the real and LTSpice versions differ slightly since different component values were used. The graphs in Appendix B are titled "cool" because this data was collected with the input of the panel simulator at 25V, which represents an operating solar panel before it heats up. Appendix C shows the same type of data and figures as Appendix B, but with the input of the panel simulator at 21V, which represents a hot operating solar panel with a shifted peak power point. Therefore, the figures in Appendix C are titled "hot". Both sets of data will be used in the next chapter to evaluate the extraction capabilities of the tracking algorithms.

4.2 Multiplier

The input of the peak power tracker is solar power, P_{solar}, as shown in the block diagram from Figure 1-5. The system uses the analog multiplier AD633 [15] to multiply the panel's voltage by the panel's current, which creates a voltage representing P_{solar}. The schematic for this function is shown in Figure 4-3. To obtain a reading of the panel's current, the LT6105 [16] precision current sense amplifier measures the voltage drop across the sense resistor R1. The LT6105 was chosen because of its wide input common mode range of -0.3V to 44V with respect to its negative supply voltage. This allows the power to be calculated for the panel's entire operating range. The AD633 then multiplies the solar current reading by the divided down solar voltage to produce a power reading. The AD633 was chosen due to its low cost and simplicity of not requiring external components. The output of the multiplier is subjected to the R7-C2 low-pass filter which has a -3dB frequency of 1.9kHz. The filter allows the passage of the low frequency dither signal (1.25 kHz), but provides good attenuation of the higher frequency input-referred ripple (346 kHz).

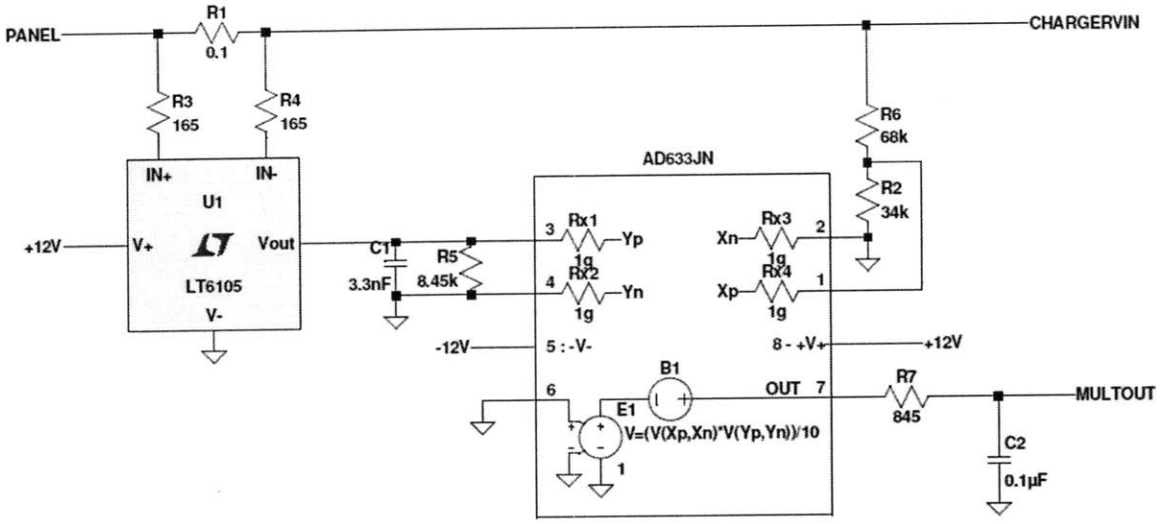

Figure 4-3: AD633 multiplier - multiplies the panel voltage by the panel current via the LT6105 current sense amplifier

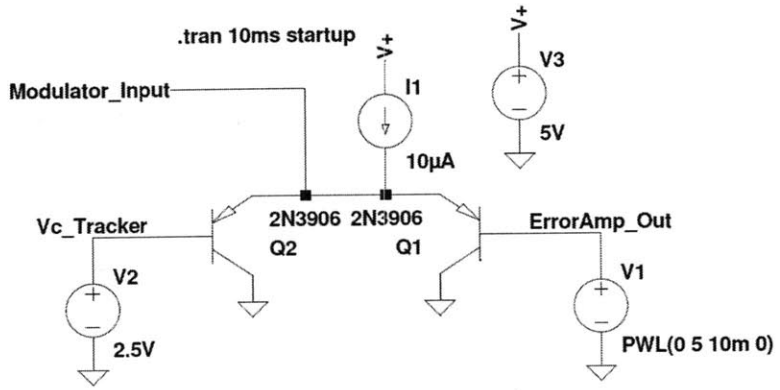

Figure 4-4: Circuitry that allows the voltage mode loop to take control from the tracker

4.3 "Handoff" Charging Technique

The "handoff" is the transfer of converter control from the peak power tracker to the error amplifier. The simple circuit in Figure 4-4 mediates the transition. Whichever base has the lower voltage, pulls the emitter down and has complete control over the value at the modulator input. To show this, Vc is kept at 2.5 V while the error amp output is slowly ramped from 5V down to 0V. The results are shown in Figure 4-5 where the modulator input tracks Vc until the error amp output falls below 2.5V, in which case control is transferred.

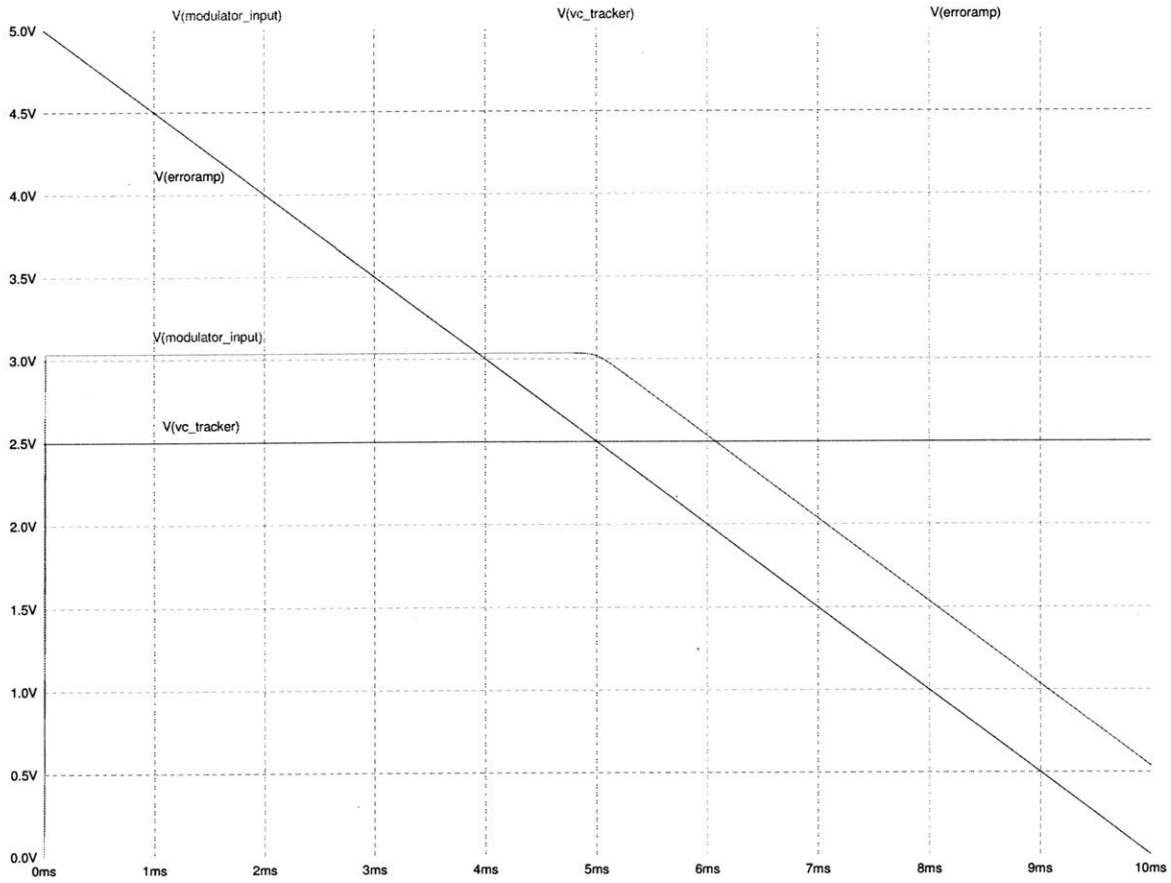

Figure 4-5: The smaller voltage between the error amp output and the tracker output controls the modulator input

The charger system works in a similar way to the test in Figure 4-4. Looking now at Figure 3-3, if the battery output is below its regulation value, the output of the error amplifier will be railed high at 5V. Meanwhile, the peak power tracker will be running its tracking algorithms with an output voltage range at Vc of 0-2.5V. The tracker will therefore have control of the circuit and will cause the converter to deliver maximum charge current to the battery. The function of the error amplifier is to sense when the battery regulation voltage is reached. As the battery voltage approaches regulation, the output of the error amplifier ramps down and takes over control from the peak power tracker. As the error amplifier output ramps down to zero, the duty ratio of the switching decreases toward zero, bringing the panel voltage up near its open-circuit point.[2] The system testing in the next section will demonstrate the transfer of control near regulation.

4.4 System LTSpice Simulation

The LTSpice simulation of the system looks at three main tests: (1) Find and hold a static peak power point using both algorithms (2) Track a dynamic power point using the perturb and observe algorithm and (3) Transfer control of the converter from the tracker to the voltage mode loop. To make the simulation run at a reasonable speed, simplifications are made to the schematics shown in Chapter 2 and Chapter 3. In the peak power tracker, simpler behavioral models are used for all the switches and logic gates.[3] Also, all the timing and control signals are generated by ideal voltage sources. For the converter, an ideal switch is used to eliminate the need for the gate driver.

The three tests are shown in Appendix D. In Figure D-1, the panel voltage does a global sweep, which results in it finding the peak power point (15.6V), and then the perturb and observe holds that peak operating point. In Figure D-2, the input voltage to the panel simulator is ramped down from 25V at 30ms to 20V at 80ms. This changes the peak power point from 15.6V to 11.1V, which simulates the panel

[2]Since Vout=D*Vin, and Vout is constant, a smaller duty ratio results in a larger Vin.

[3]The ON resistance (400Ω) and OFF resistance (500Mω) of the CD4066 switches are entered into the behavioral models

heating up. The perturb and observe algorithm tracks the decreasing peak power point. Figure D-3 demonstrates the "handoff" function. Looking at the panel voltage and Vc, the system first goes through the global sweep and loads the peak operating point. Just after the global sweep, the high charge current associated with the peak power point immediately completes the constant current phase. The battery voltage actually goes just above its 5V regulation point due to the voltage drop across the battery's internal resistance. The error amplifier output senses the high voltage on the output and begins to fall. When the error amp output falls below Vc, it takes over control and begins the constant voltage phase. This change in control can be seen at the 35ms mark by the rise in panel voltage and the drop in charge current.

4.5 Real Circuit Testing

After verifying correct system operation in LTSpice, a test board was built based on the schematics from Chapter 2 and Chapter 3. Integrated circuits (ICs) were used for all digital circuitry. The main objective for the spaced-out layout of the boards, as seen in the photograph in Figure 4-6, was to facilitate debugging and making quick changes to the board. Figure E-1, Figure E-2, and Figure E-3 are oscilloscope readings from the test board and show the same three tests explained in the previous section. For the third test showing the control transition, the output was manually brought to regulation by turning up the supply on the output. Therefore, the voltage loop doesn't take over control, it just shuts the converter off.

4.6 Frequency Design

Choosing the frequency of the perturb and observe algorithm has much to do with the application of the peak power tracker. The frequency used in this thesis is probably near the upper limit that is necessary for a solar peak power tracker. The tracker samples the power and perturbs 1250 times per second. Atmospheric conditions change very slowly, so in reality, a few samples per second would be sufficient in

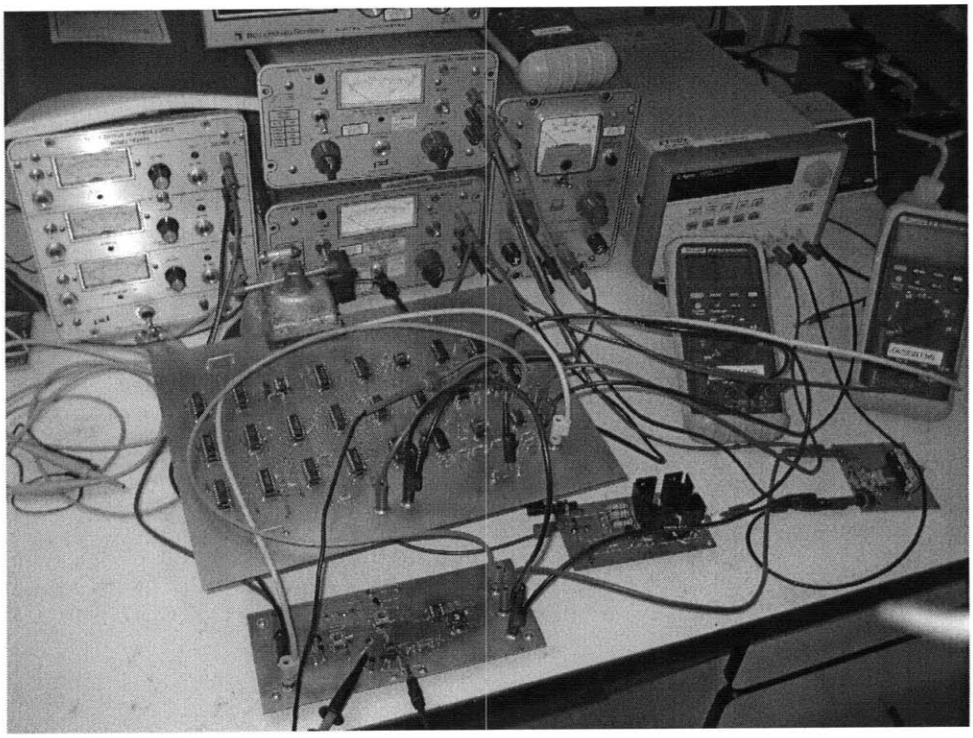

Figure 4-6: Photograph of system test setup

terms of dynamically tracking the peak power point.

The main advantage for a slower frequency is noise filtering. As the operating point moves closer to peak power, the power curve get flatter. As the power curve gets flatter, a perturbation results in a smaller difference in power. This makes the decision of whether power went up or down more susceptible to noise. With a slower sampling frequency, more attenuation of noise is possible with a low-pass filter.[4] The trade off for better noise filtering is the longer "hold" time of the sampling capacitors from Figure 2-3. As the sampling frequency gets slower, to prevent charge leakage through the OFF resistance of the switches and the inputs of the comparators, either larger sampling capacitors or more complex sampling methods are needed.

[4]The low-pass filter that is being referred to is the R7-C2 filter from Figure 4-3

4.7 Ramp Rate Design

The design of the ramp rate, or the magnitude of the perturbations, will depend on the flatness of the power curve's peak. For smaller perturbations, there will be smaller differences in power, which makes the decision more susceptible to noise, as mentioned in the previous section. Figure E-4 from Appendix E shows the panel voltage of the test board getting lost because the perturbation size is too small. Larger perturbations keep the system more stable since every sample will measure a large difference in power from the previous sample. Even if the system makes one wrong move, the subsequent step will self-correct as it will sense it is moving the wrong way on the power curve. The drawback to the large perturbation, however, can be seen in Figure E-5, which shows the panel voltage of the test board with very large perturbations. While the system seems stable, the panel voltage is dithering between very far above and very far below the peak power point, and we want to stay as close as possible to the peak point. It is therefore desirable to make the perturbation size as small as possible where the system is still stable. Figure E-1 shows a good example of this optimization performed experimentally.

Chapter 5

Performance Analysis

This chapter looks to explore the power extracting potential of the active peak power tracking technique, such as the one presented in this thesis, with the input regulation loop and "bang-bang" methods that were presented in Chapter 1. The analysis in this chapter does not include the use of a temperature controller for adjusting to a dynamic peak power point, but its role will be considered in the conclusion. First the performance metric of averaged percent of peak power is explained. Then the power extracting capabilities of each method are examined and discussed.

5.1 Averaged Percent of Peak Power

The performance of each method will be calculated based on the percent of peak power it can extract from the solar panel simulator. Percent of peak power, for a given operating voltage, is the power generated by that operating voltage divided by the power generated by the peak power point. In order to account for the changing peak power point under temperature change, each method's performance will be an average of its performance using the "cool" characteristics from Appendix B and its performance using the "hot" characteristics from Appendix C.[1] The "cool" and "hot" conditions are weighted evenly in this analysis, but if the panel were meant

[1]Note that for the perturb and observe and for the bang-bang, the operating voltage is a range of voltages, which will be averaged. Then its averaged performance under each temperature condition will again be averaged together.

to be operating for a very long time, then the "hot" condition should be weighted higher.

5.2 Performance

For the peak power tracking method from this thesis, experimental results will be used to measure extraction capabilities from the panel simulator. Due to the relative simplicity of the tracking algorithms of the input regulation loop and the "bang-bang" methods, theoretical results will be used.

5.2.1 Active Peak Power Tracking Results

For the active peak power tracking technique presented in this thesis, we will consider the oscilloscope screen shots from Appendix E. From Figure E-1, we see that the perturb and observe keeps the operating voltage approximately between 16.5V and 18.0V for a "cool" panel. If we average the % of peak power for that operating range from Table B.1, we get 99.78%. For the "hot" panel, Figure E-6 shows that the perturb and observe keeps the operating voltage approximately between 13.6V and 14.8V. From Table C.1, this corresponds to an average % of peak power of 99.79%. Therefore, weighting the two temperature conditions evenly, the active peak power tracking method from this thesis achieves 99.79% efficiency of power extraction from the solar panel simulator.

5.2.2 Bang-Bang Method Results

We will assume that the bang-bang method can be set to dither by 1V at a specified voltage range. Its dither must be averaged like with the perturb and observe, but it must be preset to a certain range and then left there as the panel heats up. Table 5.1 shows the results of three different tests. The first test places the bang-bang's dither at the "cool" peak power point, the second test places the dither between the two peak power points, and the third test places the dither at the "hot" peak power point.

Voltage range	% peak power "cool"	% peak power "hot"	Overall % peak power
16.9V - 17.9V	99.86%	77.29%	88.58%
15.3V - 16.3V	98.18%	96.30%	97.24%
13.7V - 14.7V	94.38%	99.84%	97.11%

Table 5.1: Results of the bang-bang method's power extraction capabilities for three different operating ranges

5.2.3 Input Regulation Method Results

The same tests are applied to the input regulation method and we will assume that the operating voltage can be placed anywhere, but must stay at that voltage for both the "cool" and the "hot" tests. Table 5.2 shows the results of placing the operating voltage at the "cool" peak power point, between the peak power points, and at the "hot" peak power point.

Voltage	% peak power "cool"	% peak power "hot"	Overall % peak power
17.4V	100%	77.79%	88.90%
15.8V	98.26%	96.41%	97.34%
14.2V	94.37%	100%	97.19%

Table 5.2: Results of the input regulation method's power extraction capabilities for three different operating voltages

5.2.4 Discussion of Results

The active peak power tracker has the advantage of being able to adjust for the changing peak power point, so it makes sense that it has a higher efficiency than the other two methods. However, the bang-bang and input regulation methods perform very well if placed correctly. We can see from Table 5.1 and Table 5.2 that the power extraction capabilities take a big hit if the operating voltage misses high of the peak power point. From all the power vs. voltage curves in this thesis, it shows that the power drops off much faster on the high side of the peak power point. Therefore, it is desirable to preset the Bang-Bang method and the input regulation method to be closer to the "hot" peak power point. When the panel is cool, the operating voltage will be too low, but from the above tables, the system is still extracting over 94% of

peak power and that number will rise as the panel heats up.

Chapter 6

Conclusions

This thesis has illustrated the design of a peak power tracking buck converter with application to a battery charger. The peak power tracker, as verified by the tests from Appendix D and Appendix E, successfully locates, tracks, and maintains the peak power point. Operation at the peak power point allows maximum charge current to flow into the battery output. The tracker takes the place of the current control loop in the multi-loop structure of the converter. When the battery output is close to its regulation voltage, the voltage control loop takes over via the handoff circuit and applies constant voltage charging.

The active peak power tracker designed in this thesis was then examined for its power extraction capabilities. The bang-bang method and the input regulation method were also examined for comparison. Without temperature compensation, the active peak power tracker would be able to extract the most power from the panel. Although we saw that the other two methods could perform well if their operating points were properly placed. In theory, using temperature compensation should allow the two simpler methods to extract power at about the same efficiency as the active peak power tracker. However, the real advantage of the active peak power tracker designed in this thesis is the convenience of it. It finds and maintains the peak power point by itself, whereas the other methods need setup time required. Another advantage of the active peak power tracker is that it is not panel specific. The tracker must be adjusted to work with the converter, but it should be able to handle any solar

panel that the charger can handle.[1] The tracker is a self sufficient system. If it makes a wrong turn, the tracker immediately senses it is headed in the wrong direction and corrects itself. If the system gets lost or reset, the global sweep is there to get it back on track.

6.1 Future Work

As mentioned in Chapter 4, the frequency at which the peak power tracker is ran is really the upper limit that is necessary for a PV application. Under normal conditions, the dynamics of a solar panel are quite slow. Therefore, it almost seems unnecessary to have the dynamic perturb and observe algorithm running. Why not just use the global sweep algorithm? It can be engaged once every few seconds and then the peak operating point that it finds is just held until the next global sweep. In fact, we can even replace the perturb and observe with the input regulation scheme. A global sweep can run, find the peak power point and preset the input regulation loop automatically. This would eliminate the need for temperature compensation and not require the user to preset the system based on the panel being used.

[1]However, the input range of the current sensor and multiplier could limit the tracker in certain cases.

Appendix A

MATLAB Code for Bode Plots

```
%% Bode Plot of Buck Converter Transfer Function from Duty Cycle to Output
    Rl=4; % converter component values
    Cout=22e-6;
    L=47e-6;
    Vin=17;
    Resr=.01; % converter parasitic values
    Rdcr=.1;
    Rdamp=Rdcr+.01;
    s=tf('s');
    Gvd=Vin*Rl*(1+s*Resr*Cout)/((Rl+Rdamp)+s*(L+Cout*(Resr*
    (Rl+Rdamp)+Rl*Rdamp))+s^2 * L * Cout * (Rl + Resr));
    % buck converter transfer function
    bode(Gvd)
    %% Bode Plot of Buck Converter with Type III Compensation
    Rc1=180e3; % type III compensator component values
    Cc1=179e-12;
    Rc2=1.4e3;
    Cc2=5.1e-12;
    Cc3=160e-12;
    Rfb1=200e3;
```

```
Rfb2=200e3;
s=tf('s');
Gc=(1+s*Rc1*Cc1)*(1+s*(Rfb1+Rc2)*Cc3)/(s*Rfb1*Cc1*
(1+s*Rc2*Cc3)*(1+s*Rc1*Cc1*Cc2/(Cc1+Cc2)));
% type III compensator transfer function
Fm=1/2.2; % Modulator gain = 1/Vramp
sys=Gc*Gvd*Fm; % Overall system loop transfer function
bode(sys)
```

Appendix B

Solar Panel Simulator Data and Graphs

Table B.1: Current, voltage, power, and % of peak power data for solar panel simulator

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
10.0	518.0	5.180	76.33
10.1	516.0	5.212	76.80
10.2	514.5	5.248	77.33
10.3	513.0	5.284	77.86
10.4	511.5	5.320	78.39
10.5	510.0	5.355	78.91
10.6	509.0	5.395	79.51
10.7	507.5	5.430	80.02
10.8	506.0	5.465	80.53
10.9	504.5	5.499	81.04
11.0	503.0	5.533	81.54
11.1	501.5	5.567	82.03

Continued on next page

Table B.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
11.2	500.0	5.600	82.52
11.3	498.5	5.633	83.01
11.4	497.0	5.666	83.49
11.5	495.0	5.693	83.89
11.6	493.0	5.719	84.27
11.7	491.5	5.751	84.74
11.8	490.0	5.782	85.20
11.9	488.5	5.813	85.66
12.0	487.0	5.844	86.12
12.1	485.5	5.875	86.57
12.2	484.0	5.905	87.01
12.3	482.5	5.935	87.46
12.4	481.0	5.964	87.89
12.5	479.5	5.994	88.33
12.6	478.0	6.023	88.75
12.7	476.5	6.052	89.18
12.8	475.0	6.080	89.60
12.9	473.0	6.102	89.92
13.0	471.0	6.123	90.23
13.1	469.5	6.150	90.63
13.2	468.0	6.178	91.03
13.3	466.5	6.204	91.43
13.4	465.0	6.231	91.82
13.5	463.0	6.251	92.11
13.6	461.0	6.270	92.39
13.7	459.5	6.295	92.77

Continued on next page

Table B.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
13.8	458.0	6.320	93.14
13.9	456.5	6.345	93.51
14.0	455.0	6.370	93.87
14.1	453.0	6.387	94.12
14.2	451.0	6.404	94.37
14.3	449.5	6.428	94.72
14.4	448.0	6.451	95.07
14.5	446.0	6.467	95.30
14.6	444.0	6.482	95.53
14.7	442.0	6.497	95.75
14.8	440.0	6.512	95.96
14.9	438.0	6.526	96.17
15.0	436.0	6.540	96.37
15.1	435.0	6.569	96.79
15.2	433.0	6.582	96.99
15.3	431.0	6.594	97.18
15.4	429.0	6.607	97.36
15.5	428.0	6.634	97.76
15.6	426.0	6.646	97.93
15.7	424.0	6.657	98.10
15.8	422.0	6.668	98.26
15.9	420.0	6.678	98.41
16.0	418.0	6.688	98.56
16.1	416.0	6.698	98.70
16.2	414.0	6.707	98.83
16.3	412.0	6.716	98.96

Continued on next page

Table B.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
16.4	410.0	6.724	99.09
16.5	408.5	6.740	99.33
16.6	407.0	6.756	99.56
16.7	405.0	6.764	99.67
16.8	402.5	6.762	99.65
16.9	400.0	6.760	99.62
17.0	398.0	6.766	99.71
17.1	396.0	6.772	99.79
17.2	394.0	6.777	99.86
17.3	392.0	6.782	99.94
17.4	390.0	6.786	100.00
17.5	387.5	6.781	99.93
17.6	385.0	6.776	99.85
17.7	383.0	6.779	99.90
17.8	381.0	6.782	99.94
17.9	379.0	6.784	99.97
18.0	376.0	6.768	99.73
18.1	374.0	6.769	99.76
18.2	372.0	6.770	99.77
18.3	369.0	6.753	99.51
18.4	366.0	6.734	99.24
18.5	364.0	6.734	99.23
18.6	361.0	6.715	98.95
18.7	359.0	6.713	98.93
18.8	356.0	6.693	98.63
18.9	353.0	6.672	98.32

Continued on next page

Table B.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
19.0	350.0	6.650	98.00
19.1	347.0	6.628	97.67
19.2	345.0	6.624	97.61
19.3	342.0	6.601	97.27
19.4	339.0	6.577	96.91
19.5	335.0	6.533	96.26
19.6	332.0	6.507	95.89
19.7	329.0	6.481	95.51
19.8	325.0	6.435	94.83
19.9	322.0	6.408	94.43
20.0	318.0	6.360	93.72
20.1	314.0	6.311	93.01
20.2	310.0	6.262	92.28
20.3	306.0	6.212	91.54
20.4	302.0	6.161	90.79
20.5	297.0	6.089	89.72
20.6	293.0	6.036	88.94
20.7	288.0	5.962	87.85
20.8	283.0	5.886	86.74
20.9	278.0	5.810	85.62
21.0	272.0	5.712	84.17
21.1	266.0	5.613	82.71
21.2	260.0	5.512	81.23
21.3	254.0	5.410	79.73
21.4	247.0	5.286	77.89
21.5	240.0	5.160	76.04

Continued on next page

Table B.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
21.6	233.0	5.033	74.16
21.7	226.0	4.904	72.27
21.8	218.0	4.752	70.03
21.9	210.0	4.599	67.77
22.0	202.0	4.444	65.49
22.1	194.0	4.287	63.18
22.2	186.0	4.129	60.85
22.3	178.0	3.969	58.49
22.4	170.0	3.808	56.12
22.5	161.0	3.623	53.38
22.6	152.0	3.435	50.62
22.7	144.0	3.269	48.17
22.8	136.0	3.101	45.69
22.9	128.0	2.931	43.19
23.0	120.0	2.760	40.67
23.1	112.0	2.587	38.13
23.2	103.0	2.390	35.21

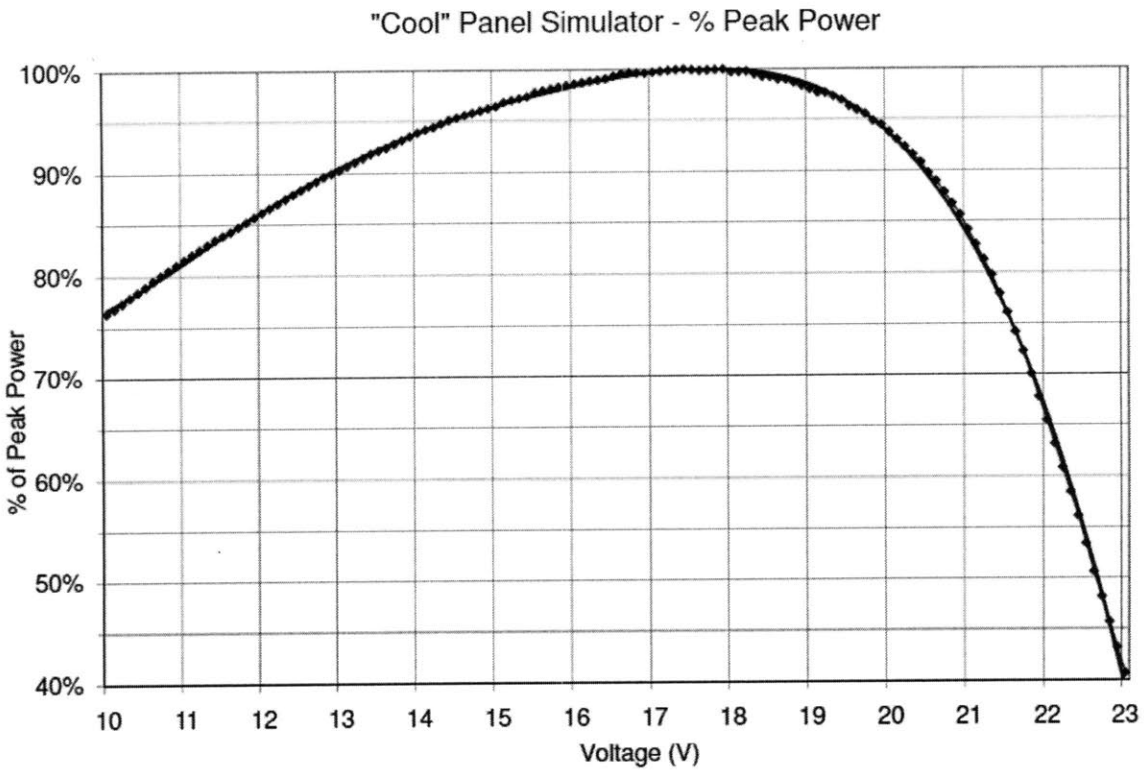

Figure B-1: Percent of peak power vs. operating voltage for solar panel simulator

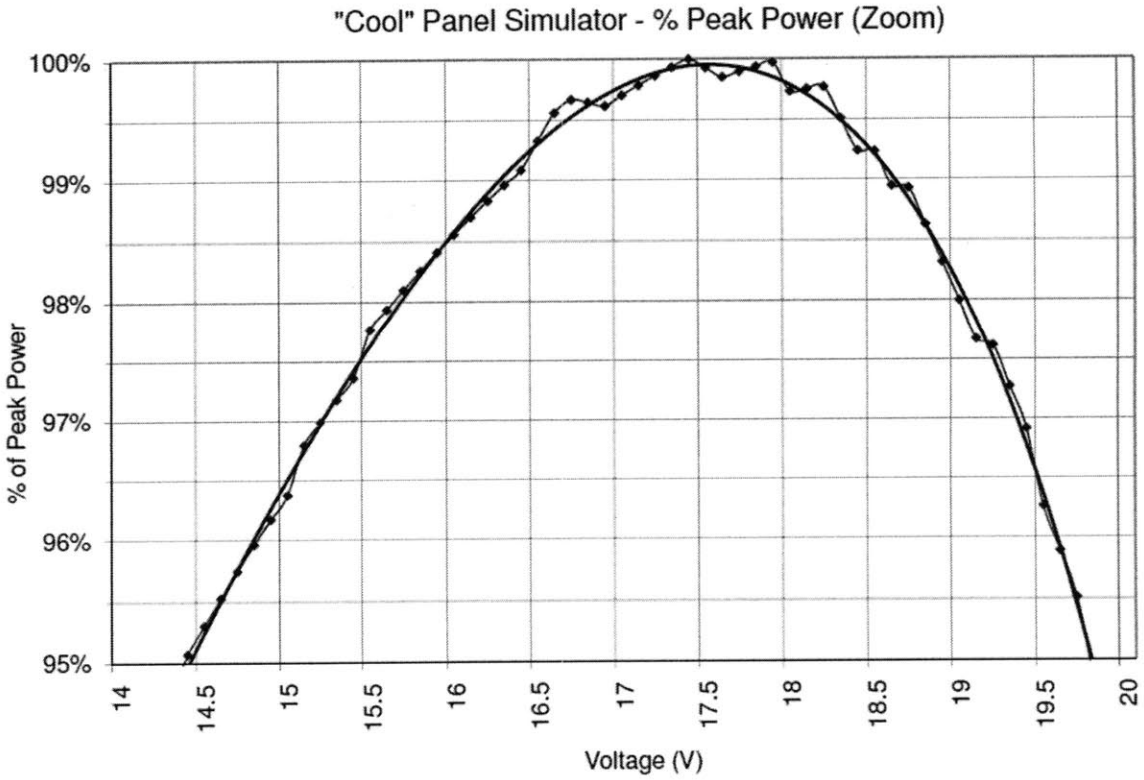

Figure B-2: Zoomed in on the peak power point of Figure B-1

Appendix C

"Hot" Solar Panel Simulator Data and Graphs

Table C.1: Current, voltage, power, and % of peak power data for "hot" solar panel simulator

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
7.5	492.0	3.690	70.81
7.6	491.0	3.732	71.60
7.7	489.5	3.769	72.33
7.8	488.0	3.806	73.04
7.9	486.5	3.843	73.75
8.0	485.0	3.880	74.45
8.1	483.5	3.916	75.15
8.2	482.0	3.952	75.84
8.3	480.0	3.984	76.45
8.4	478.0	4.015	77.05
8.5	476.5	4.050	77.72
8.6	475.0	4.085	78.39
Continued on next page			

Table C.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
8.7	473.5	4.119	79.05
8.8	472.0	4.154	79.70
8.9	470.0	4.183	80.27
9.0	468.0	4.212	80.82
9.1	466.5	4.245	81.46
9.2	465.0	4.278	82.09
9.3	463.5	4.311	82.71
9.4	462.0	4.343	83.33
9.5	460.0	4.370	83.85
9.6	458.0	4.397	84.37
9.7	456.5	4.428	84.97
9.8	455.0	4.459	85.56
9.9	453.5	4.490	86.15
10.0	452.0	4.520	86.73
10.1	450.0	4.545	87.21
10.2	448.0	4.570	87.68
10.3	446.5	4.599	88.25
10.4	445.0	4.628	88.81
10.5	443.0	4.651	89.26
10.6	441.0	4.675	89.70
10.7	439.0	4.697	90.14
10.8	438.0	4.730	90.77
10.9	436.0	4.752	91.19
11.0	434.0	4.774	91.61
11.1	432.0	4.795	92.01
11.2	430.0	4.816	92.41

Continued on next page

Table C.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
11.3	428.0	4.836	92.80
11.4	426.0	4.856	93.19
11.5	424.0	4.876	93.56
11.6	422.0	4.895	93.93
11.7	421.0	4.926	94.52
11.8	419.0	4.944	94.87
11.9	417.0	4.962	95.22
12.0	415.0	4.980	95.56
12.1	413.0	4.997	95.89
12.2	411.0	5.014	96.22
12.3	409.0	5.031	96.53
12.4	407.0	5.047	96.84
12.5	405.0	5.062	97.14
12.6	403.0	5.078	97.44
12.7	401.0	5.093	97.72
12.8	399.0	5.107	98.00
12.9	397.0	5.121	98.27
13.0	395.0	5.135	98.53
13.1	392.0	5.135	98.54
13.2	390.0	5.148	98.78
13.3	388.0	5.160	99.02
13.4	386.0	5.172	99.25
13.5	384.0	5.184	99.47
13.6	381.5	5.188	99.56
13.7	379.0	5.192	99.63
13.8	377.0	5.203	99.83

Continued on next page

Table C.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
13.9	374.5	5.206	99.89
14.0	372.0	5.208	99.93
14.1	369.5	5.210	99.97
14.2	367.0	5.211	100.00
14.3	364.0	5.205	99.88
14.4	361.5	5.206	99.89
14.5	359.0	5.205	99.89
14.6	356.0	5.198	99.74
14.7	353.0	5.189	99.57
14.8	350.5	5.187	99.54
14.9	348.0	5.185	99.50
15.0	345.0	5.175	99.30
15.1	342.0	5.164	99.09
15.2	339.0	5.153	98.88
15.3	336.0	5.141	98.65
15.4	332.5	5.120	98.26
15.5	329.0	5.099	97.85
15.6	326.0	5.086	97.59
15.7	322.0	5.055	97.01
15.8	318.0	5.024	96.41
15.9	315.0	5.008	96.11
16.0	311.0	4.976	95.48
16.1	307.0	4.943	94.84
16.2	302.0	4.892	93.88
16.3	298.0	4.857	93.21
16.4	293.0	4.805	92.21

Continued on next page

Table C.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
16.5	288.0	4.752	91.18
16.6	283.0	4.698	90.14
16.7	278.0	4.643	89.09
16.8	272.0	4.570	87.68
16.9	266.0	4.495	86.26
17.0	260.0	4.420	84.81
17.1	254.0	4.343	83.34
17.2	247.0	4.248	81.52
17.3	240.0	4.152	79.67
17.4	233.0	4.054	77.79
17.5	226.0	3.955	75.89
17.6	218.0	3.837	73.62
17.7	210.0	3.717	71.32
17.8	203.0	3.613	69.34
17.9	194.0	3.473	66.63
18.0	187.0	3.366	64.59
18.1	178.0	3.222	61.82
18.2	170.0	3.094	59.37
18.3	162.0	2.965	56.89
18.4	154.0	2.834	54.37
18.5	145.0	2.683	51.47
18.6	137.0	2.548	48.90
18.7	128.0	2.394	45.93
18.8	120.0	2.256	43.29
18.9	112.0	2.117	40.62
19.0	103.0	1.957	37.55

Continued on next page

Table C.1 – continued from previous page

Voltage (V)	Current (mA)	Power (W)	% of Peak Power
19.1	95.0	1.815	34.82
19.2	87.0	1.670	32.05
19.3	79.0	1.525	29.26
19.4	70.5	1.368	26.24
19.5	62.0	1.209	23.20
19.6	53.0	1.039	19.93
19.7	45.0	0.887	17.01
19.8	37.0	0.733	14.06
19.9	29.0	0.577	11.07
20.0	22.0	0.440	8.44
20.1	14.0	0.281	5.40
20.2	7.4	0.149	2.87
20.3	1.7	0.035	0.66
20.4	0.1	0.002	0.04
20.5	0.0	0.000	0.00

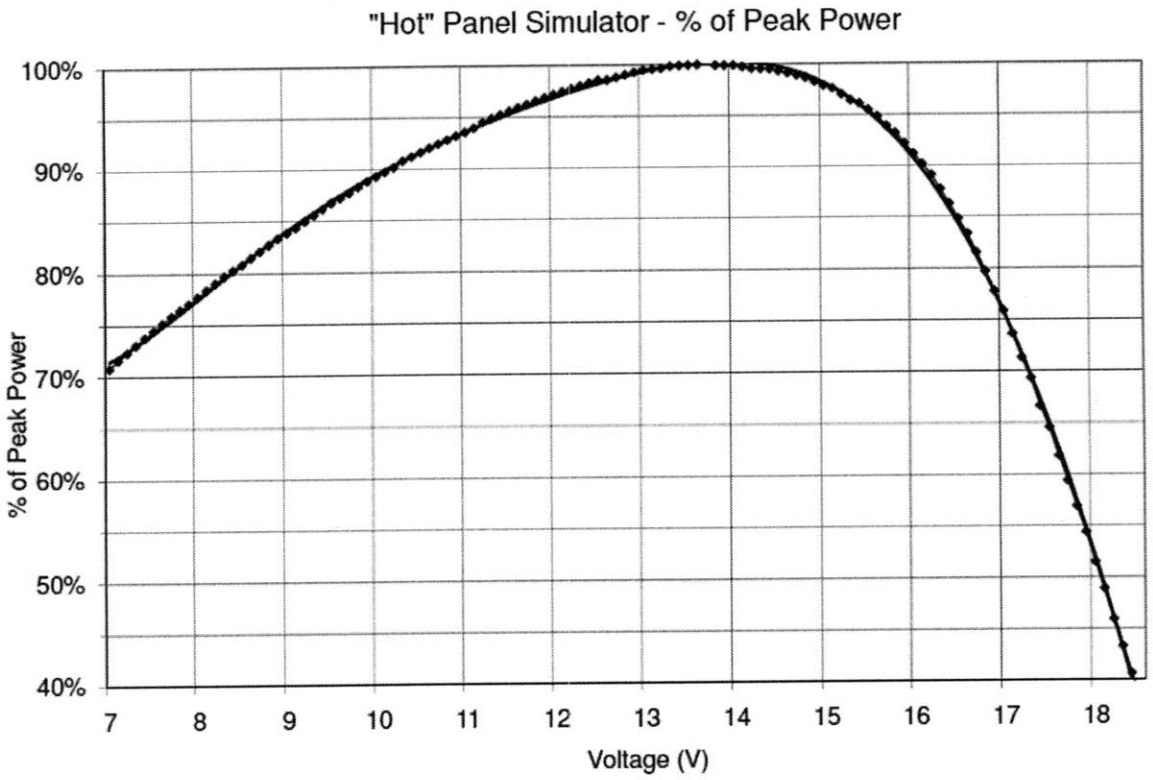

Figure C-1: The open-circuit voltage of the solar panel simulator is reduced to simulate a changing peak power point as panel temperature increases

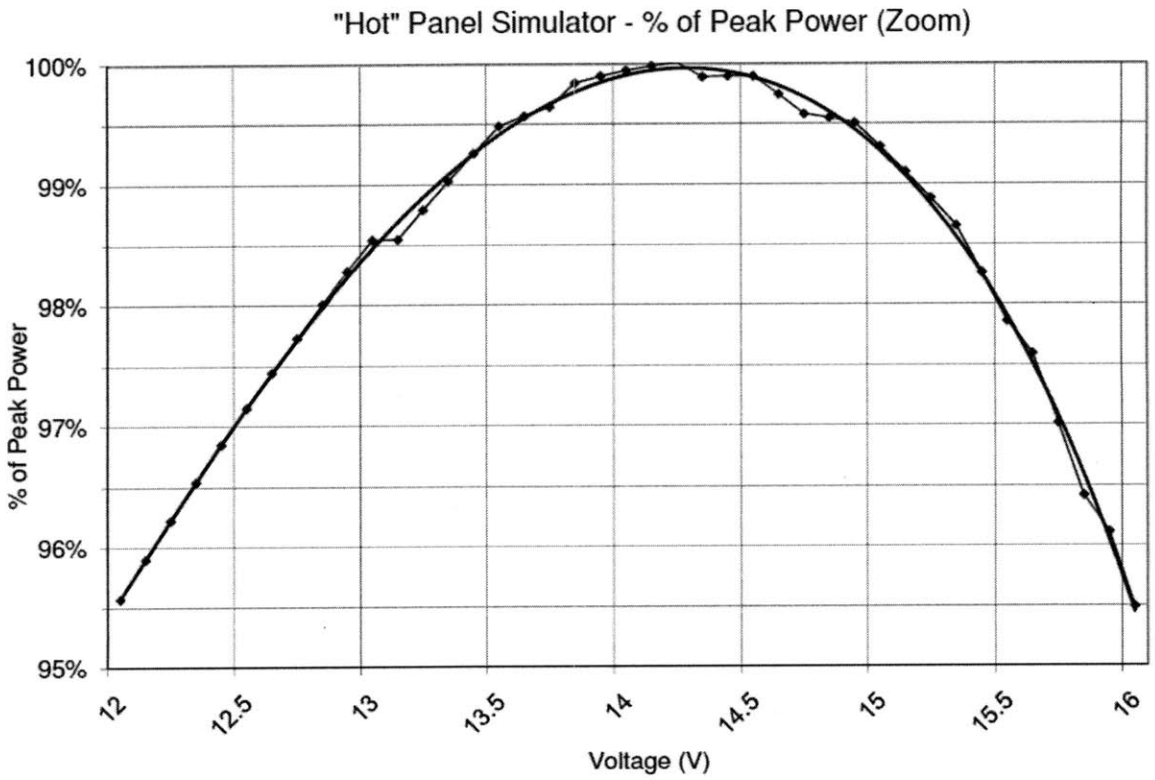

Figure C-2: Zoomed in on the peak power point of Figure C-1

Appendix D

LTSpice System Simulation Figures

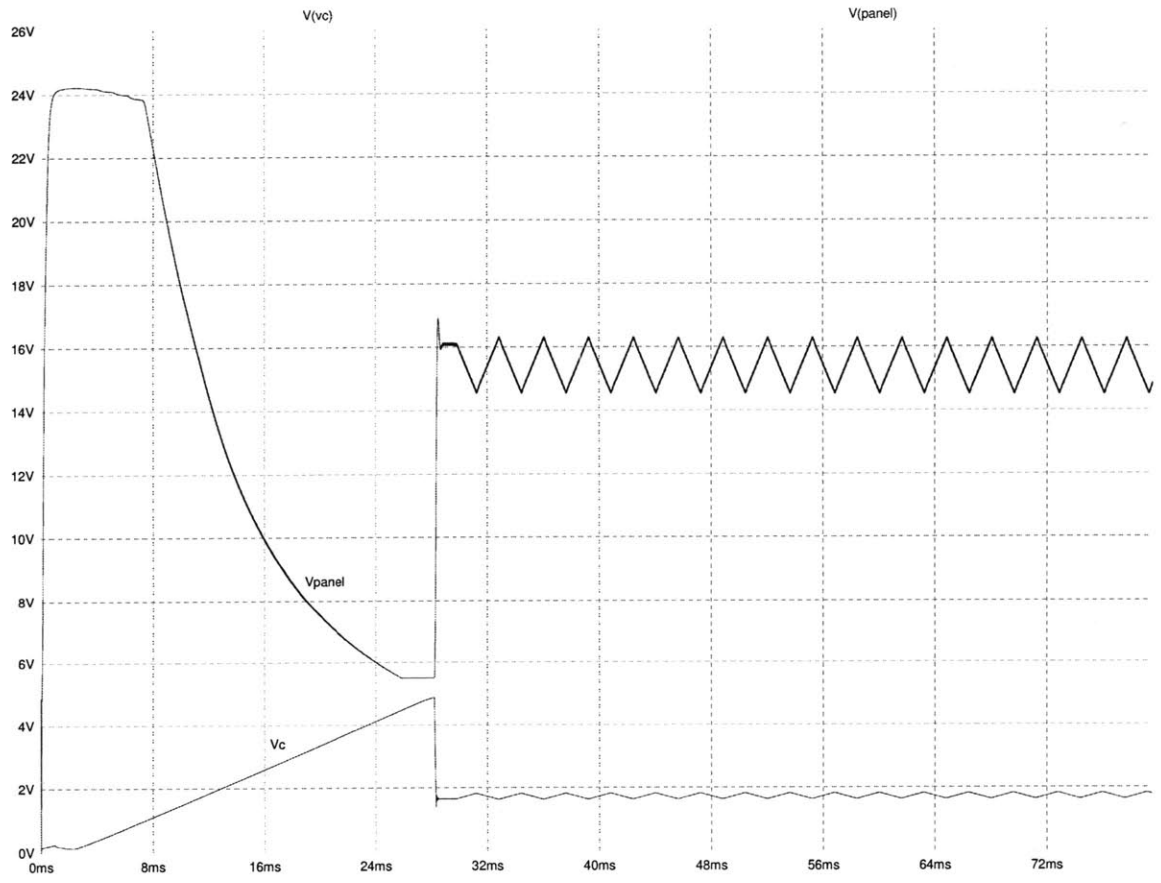

Figure D-1: The global sweep finds the peak power point and the perturb and observe maintains that operating point

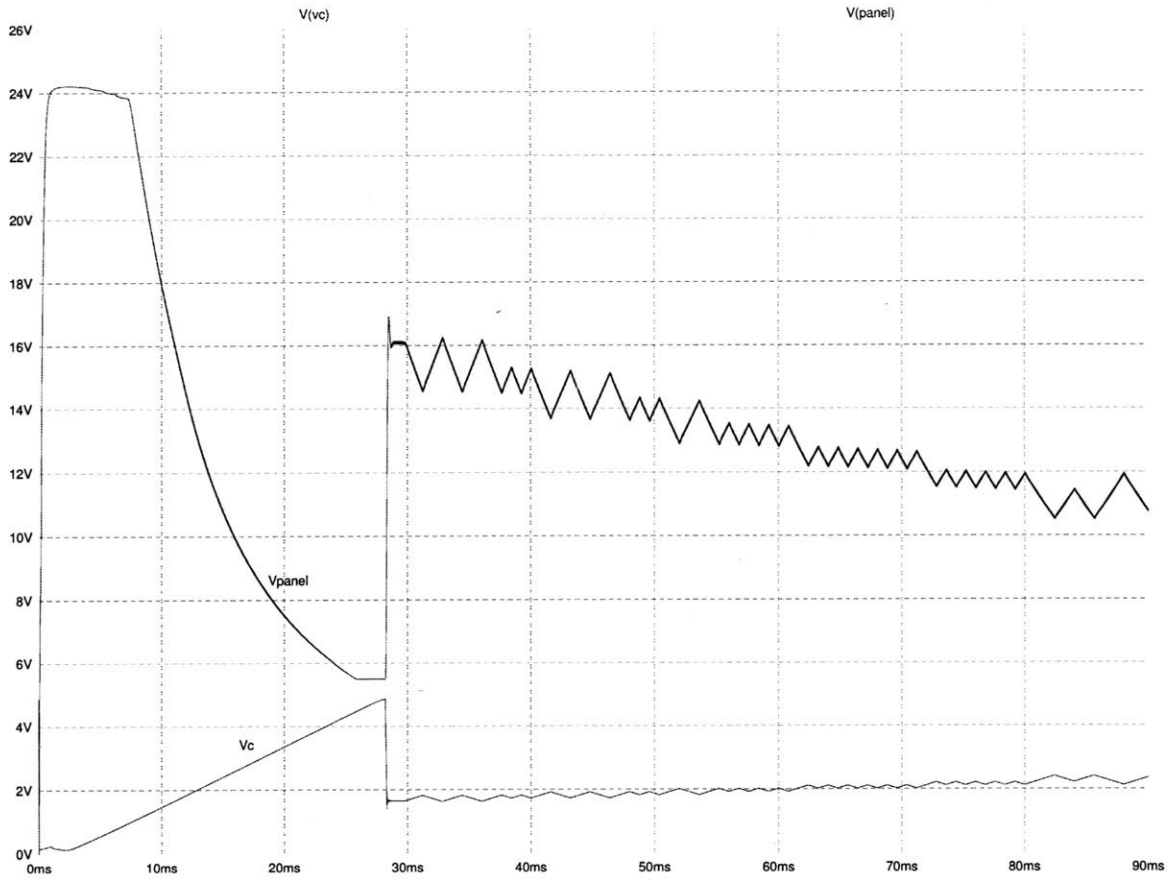

Figure D-2: The perturb and observe algorithm tracks the peak power point that is decreasing with time

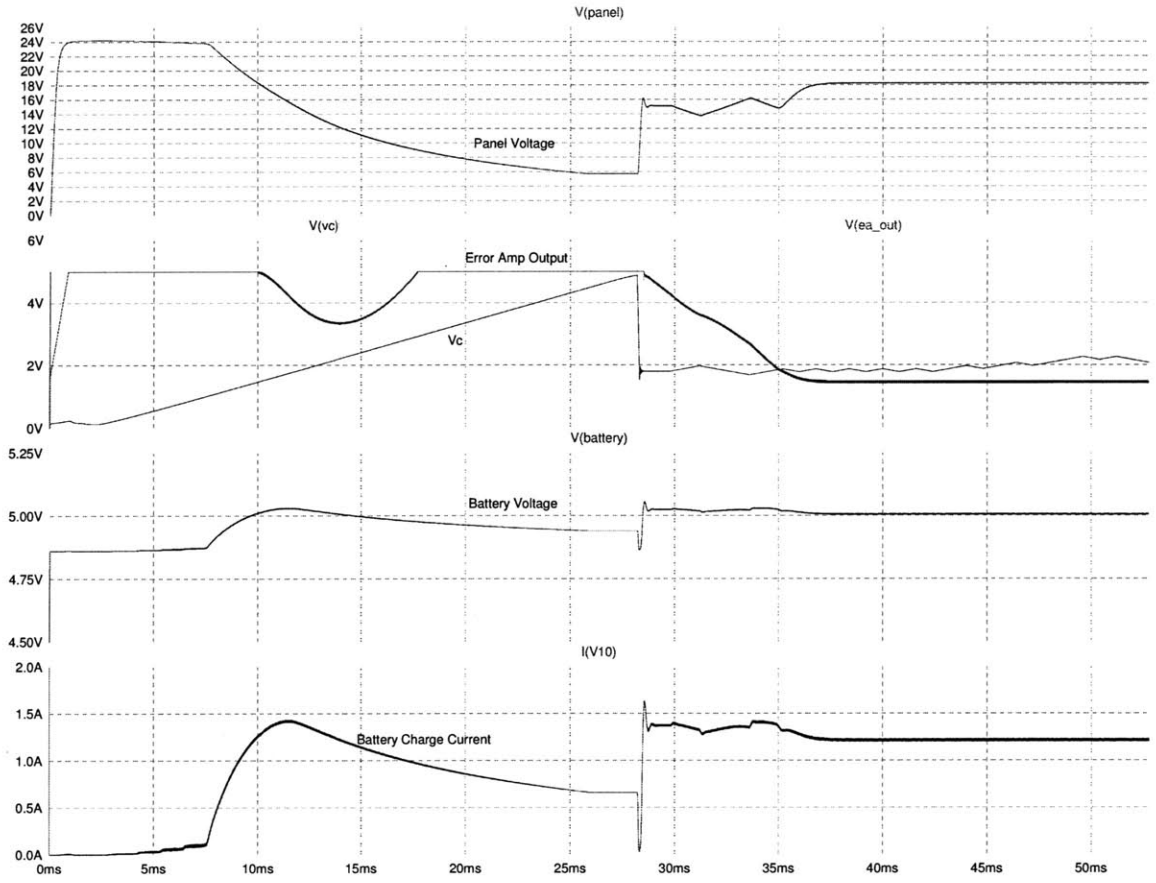

Figure D-3: At 35ms, the error amplifier takes over control of the converter and begins the constant voltage phase of the charge process

Appendix E

Oscilloscope Readings for Test Board

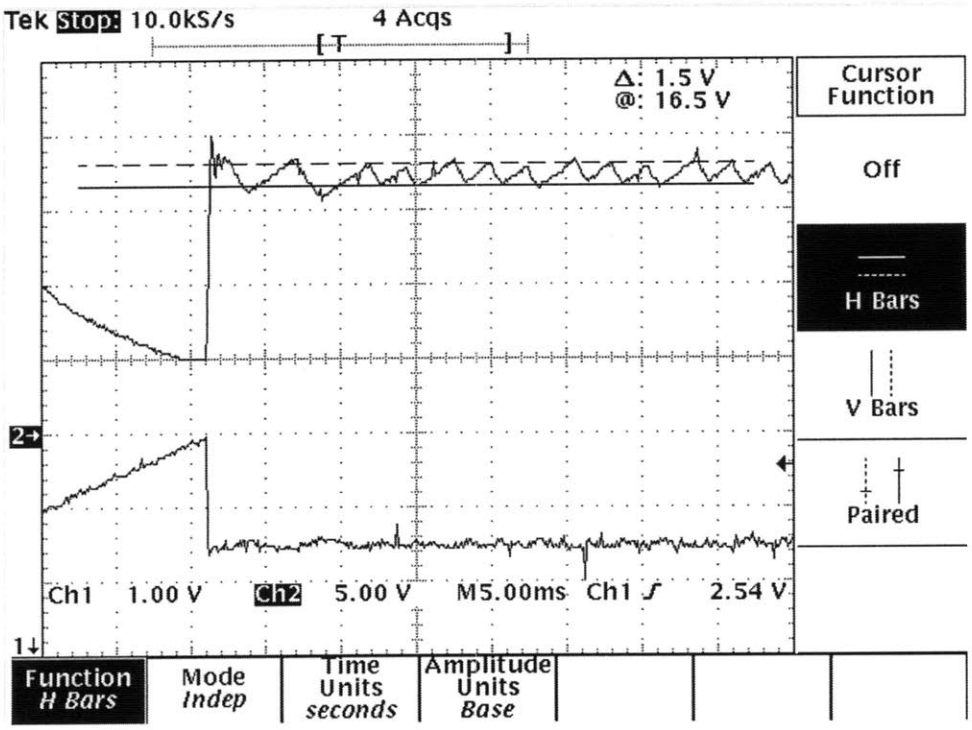

Figure E-1: Oscilloscope reading of panel voltage(top) and control voltage verifying operation of global sweep and perturb and observe algorithms

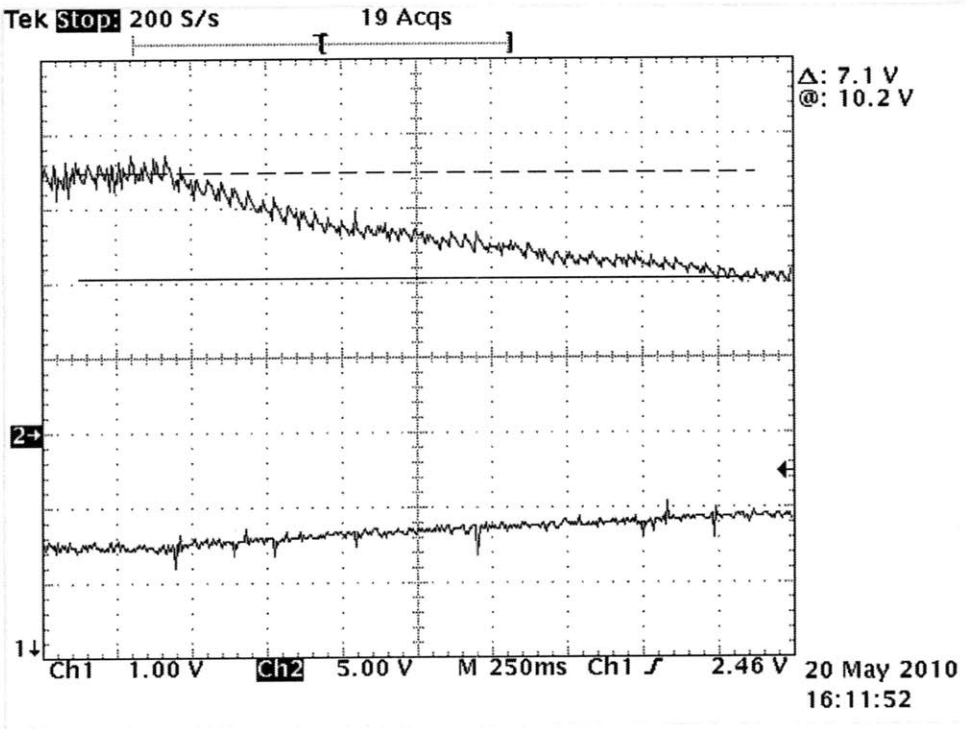

Figure E-2: Oscilloscope reading of panel voltage and control voltage during a downward shift of the peak power point - The panel voltage tracks the changing power point

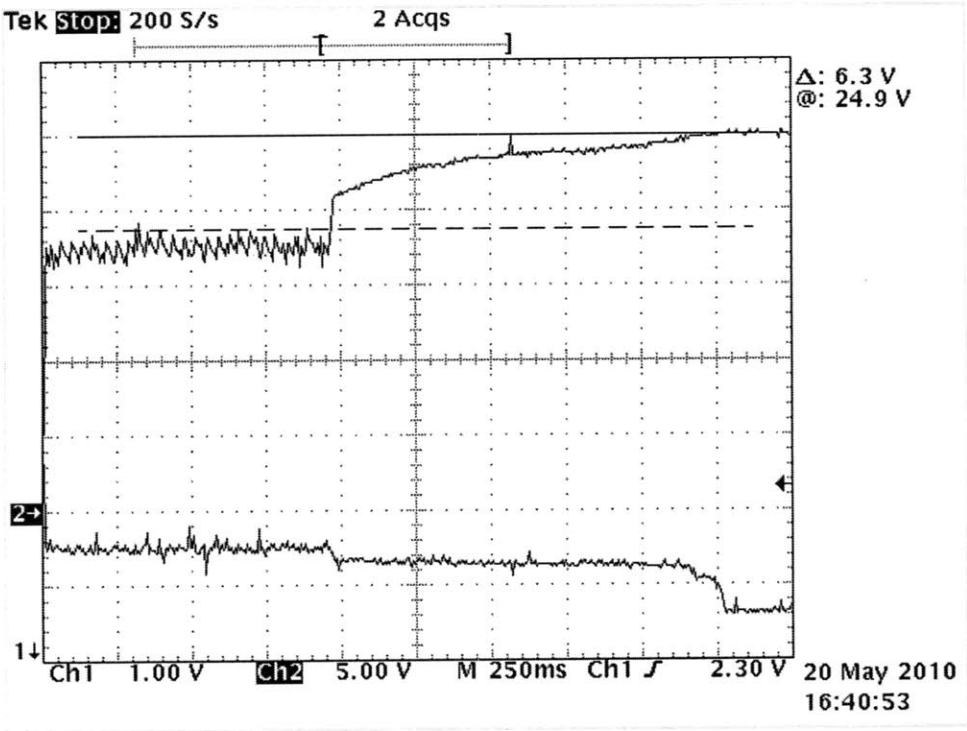

Figure E-3: The converter achieving regulation - The power supply on the ouput is slowly turned up to the 5V regulation point. From the plot, we can see the panel voltage(top) rise slowly and then it hits its open-circuit point

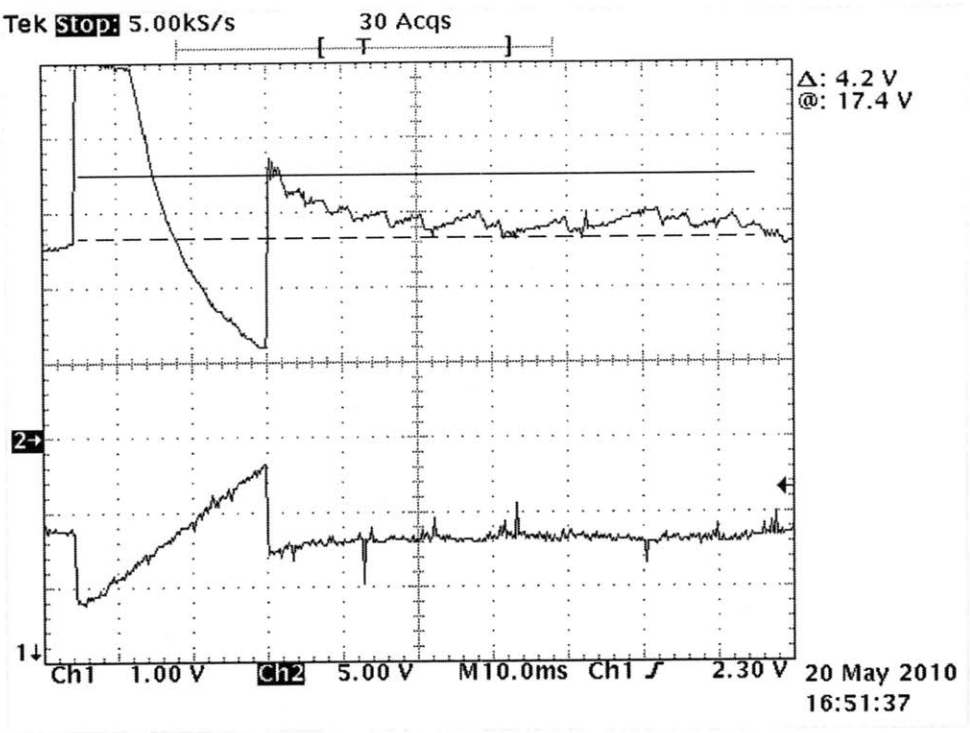

Figure E-4: Oscilloscope reading of panel voltage(top) and control voltage showing perturbations that are too small and cause the system to get lost

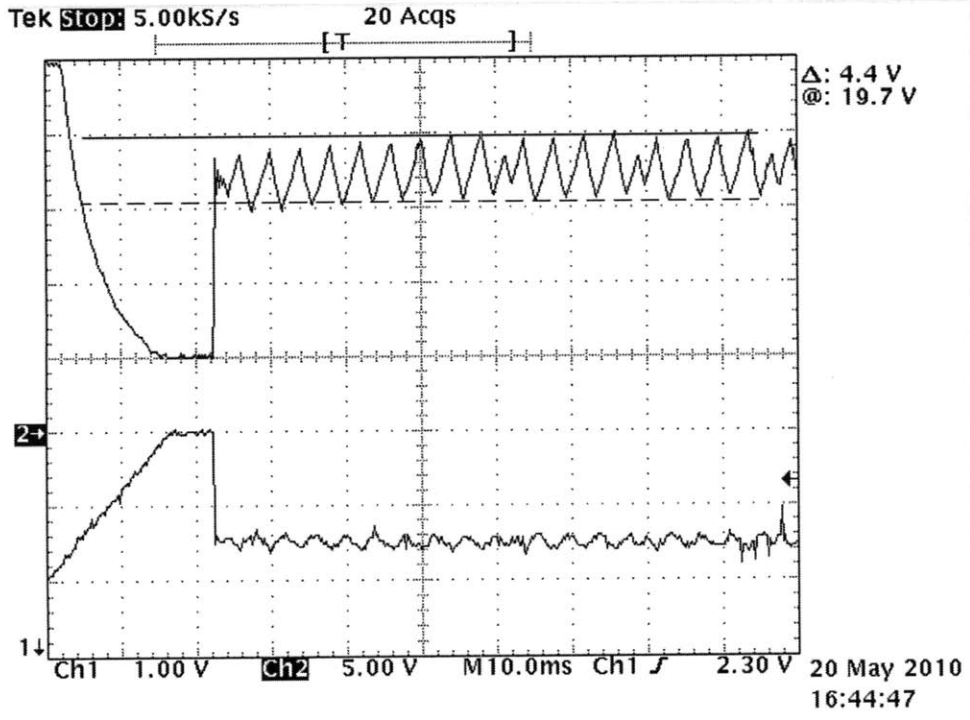

Figure E-5: Oscilloscope reading of panel voltage(top) and control voltage showing large perturbations that stray too far from the peak power point

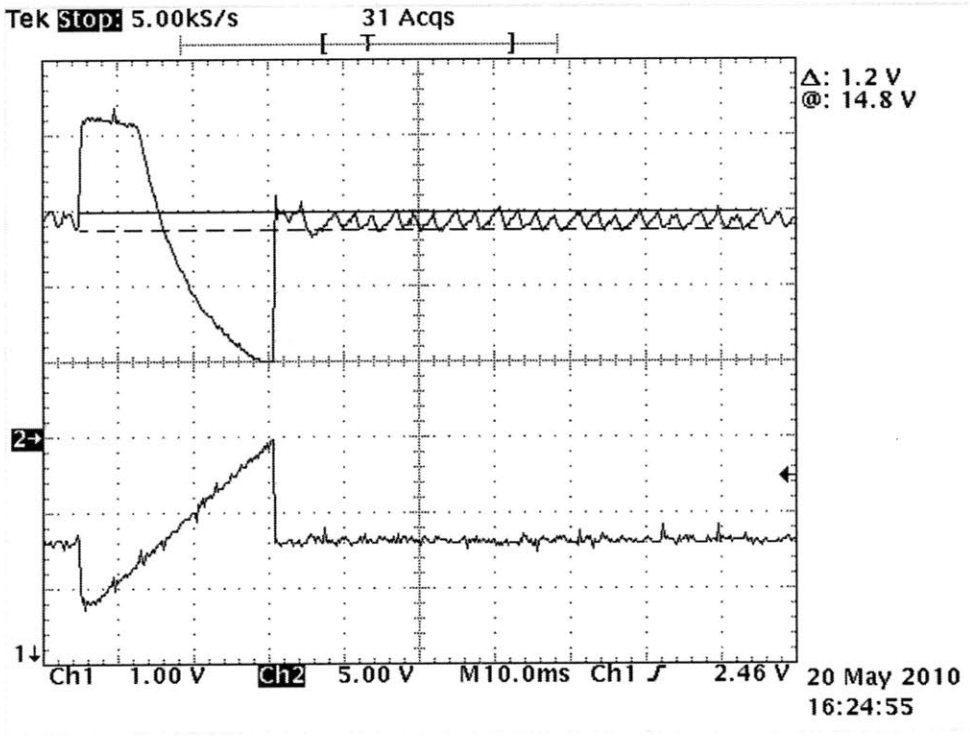

Figure E-6: Oscilloscope reading of panel voltage(top) and control voltage showing the system achieve the peak power point for a "hot" solar panel

Bibliography

[1] D. P. Hohm, M. E. Ropp, "Comparative Study of Maximum Power Point Tracking Algorithms Using Experimental, Programmable, Maximum Power Point Tracking Test Bed." *IEEE Photovoltaic Conference*, 2000.

[2] Application Note 484, "Harnessing Solar Power with Smart Power-Conversion Techniques," Maxim Integrated Products

[3] "Linear Technology LT3652 Datasheet," Linear Technology Corporation 2010.

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