

# Design and Implementation of A Truecolor Wide Dimming Single-Pin LED Driver

by  
Zhen Li

Submitted to the Department of Electrical Engineering and Computer Science

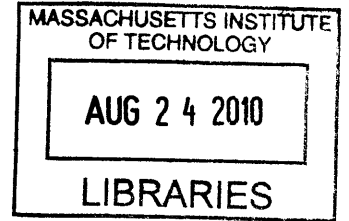
in Partial Fulfillment of the Requirements for the Degree of  
Master of Engineering in Electrical Engineering and Computer Science  
at the MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2010

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## Abstract

This thesis develops a single-pin LED driver used in wide screen displays. With the increasing size of the displays, a more compact multi-channel driver solution is needed for the increasing number of back light LEDs. This thesis focuses on the pin count and the accuracy. Simulation results and experimental data show that the low-side current sampling scheme is able to work with the least number of pins with acceptable accuracy.

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## Acknowledgments

This thesis would not have been possible without assistance of the people below. I would like to thank Michael Negrete and Bryan Legates for proposing the idea behind this thesis. Michael Negrete served as a great mentor and supervisor. He was always ready to answer my numerous questions and provide his technical expertise. I learned a great deal from his expertise in the area of circuit design and power electronics, and moreover, from his perspective as a designer, which will surely continue to benefit me in my future life.

I would like to thank Professor James Roberge for volunteering to be my thesis advisor with his already tremendous work load. I will not forget how many times I jumped into his office and started drawing circuit schematics on his blackboard. He gave insightful technical comments to many of the concepts presented in my thesis, and amazingly, provided rhetorical comments as well.

This thesis would not be possible without the support from Linear Technology. There are many other individuals that served as valuable sources of information at Linear Technology that I would like to thank too. Throughout my VI-A internship, Jim Williams always made sure my time at Linear was exciting by teaching me both old-school and contemporary circuit techniques, especially the design ideas from antique HP instruments, and showing me his various collections of electronics with tubes, discrete transistors and ICs. And last but not least, I could not have done such a professional job on the IC mask design without the excellent work of Kevin Tu.

I would also like to thank all my family and friends that have supported throughout my life, especially when times have been tough. I extend my biggest thanks to my parents, who have served as a crucial role model and inspiration of my life. My father has encouraged a curiosity about how things work at an early age, and his collections of antique electronics certainly have a positive impact on my ability to excel at circuit design. I would like to thank my mother for helping me develop the personal skills and keeping my life full of optimism.



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# Chapter 1

## Introduction

### 1.1 Background and Motivations

A low-cost, multi-channel, true-color LED (Light-Emitting Diode) driver with 1000:1 dimming range is developed in this thesis. This product targets the backlight of HDTV screens as well as other flat screen monitors. For a screen backlight, the LED is more attractive because it can provide better color depth and longer lifetime than the current technology, the CCFL (Cold Cathode Fluorescent Lamp), does. The LED also has much faster response time than the CCFL (50ns v.s. 1s), which leads to a dramatic improvement in contrast rate by backlight dimming. Moreover, unlike the CCFL, the LED does not require a high voltage startup circuit, which can reduce component size and stress, offering a more compact solution with improved safety. (Figure 1-1)

The backlight of an HDTV requires uniform intensity (brightness) over a large area with regional dimming ability. In addition, the backlight color should not change when the brightness changes. Because a white LED has a slight blue shift as the driving current increases, a well managed pulse width modulated (PWM) current driver is desirable for dimming, with a constant on-state current (the current through the LED when it is producing light).

Light-emitting diodes, especially low power white LEDs, have recently become widely available at a competitive price compared with fluorescent lamps and incan-

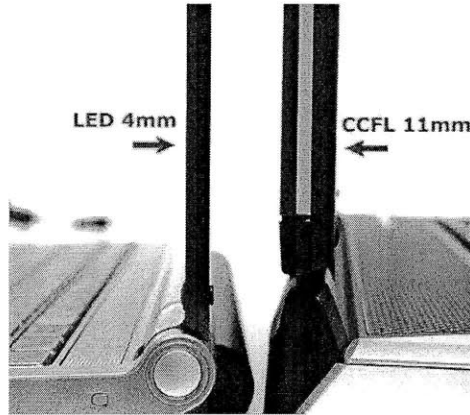


Figure 1-1: LED Backlight: A More Compact Solution

descent light bulbs. Therefore, a large array of white LEDs (16x16 or more) becomes a preferable solution for screen backlight. However, the forward drop  $V_F$  varies for the widely available white LEDs, often from 3.0V to 3.6V. In order to drive the LEDs to the same intensity (or the same power), using multiple matched current sources, each driving a string of LEDs in series, is a popular solution for large arrays.

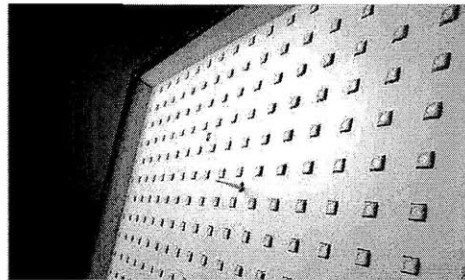


Figure 1-2: Large LED Array As Backlight

## 1.2 Major Applications

Linear Technology Corporation presently sells several multi-channel LED drivers. One example is the LT3595, a 16-channel buck mode LED driver. An application circuit of the LT3595 is shown in Figure 1-3. A typical application of this proposed part is similar to that of LT3595.

There is little reason to design a regulator without considering whether there is a need for new features and more impressive design specifications, except the latter

may be fun. A new buck mode LED driver with internal current sensing capability does have some appealing features to customers. By only having one pin per channel, the proposed part achieves comparable functionality with smaller die size, simpler board layout, and lower cost. Moreover, it becomes feasible to fit 32 or more channels on a single chip.

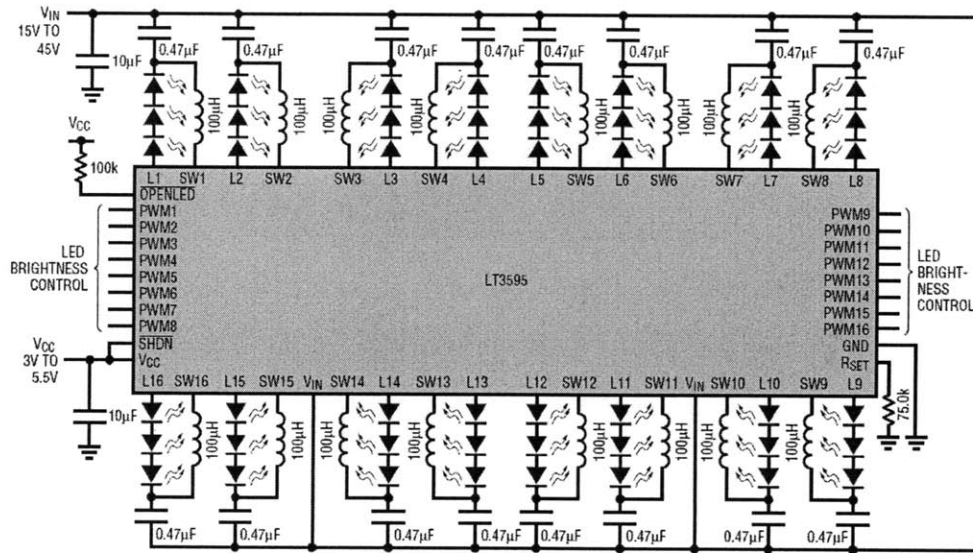


Figure 1-3: 16-Channel LED Driver (LT3595)

### 1.3 Thesis Organization

Chapter 2 covers the basics of the buck switching regulator operation and control. Then, the control scheme of single-pin operation is described. The sampling method and related control issues are further discussed in Chapter 3. Chapter 4 examines the modeling of a matched delay network, which is used as part of the switch on-current sampling scheme. Next, the design of each sub-circuit of the buck mode regulator is detailed in Chapter 5. Chapter 6 briefly reviews some layout techniques and issues related to this design. Bench test results of the silicon are reported in Chapter 7. Finally, the issues and future improvements discussed in the thesis are summarized in Chapter 8.



# Chapter 2

## System Overview

This chapter describes the basics of buck mode switching regulators (also referred as “low side switching step-down regulators”) and buck mode switching regulator integrated circuits. It then outlines the control scheme used in the proposed project, including how the synchronous sample-and-hold circuit is used to estimate the average output current, in order to achieve one pin per channel operation.

### 2.1 Buck Mode Switching Regulator

The circuit topology of a basic buck switching regulator is shown in Figure 2-1, with a bipolar switch connected to the high voltage side ( $V_{in}$ ) of the circuit.

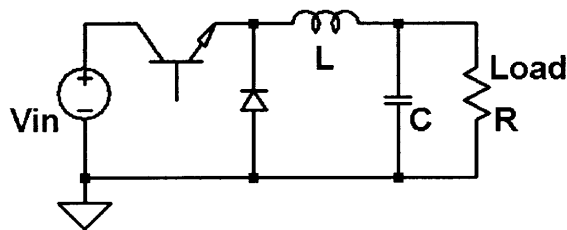


Figure 2-1: Basic Buck Switching Regulator Topology

An alternate topology for a basic buck switching regulator is shown in Figure 2-2. It has a low side switch, with the emitter connected to ground. It is often called a “buck mode” regulator.

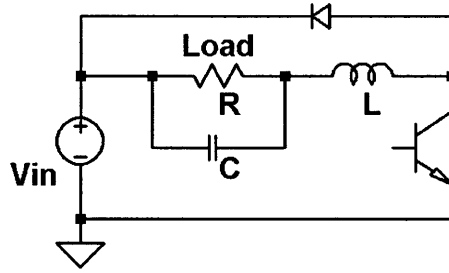


Figure 2-2: Basic Buck Mode Switching Regulator Topology

These circuits do not show any of the feedback circuitry which is used to control and drive the switch. The feedback circuitry and the choice of switch are two of the most difficult parts of designing a regulator system. The switch and the feedback circuitry are the aspects of the regulator which are integrated in the proposed IC, and the other elements (the inductor, the Schottky diode, and etc.) are discrete, external components.

## 2.2 Single-Pin Buck Mode Current Source

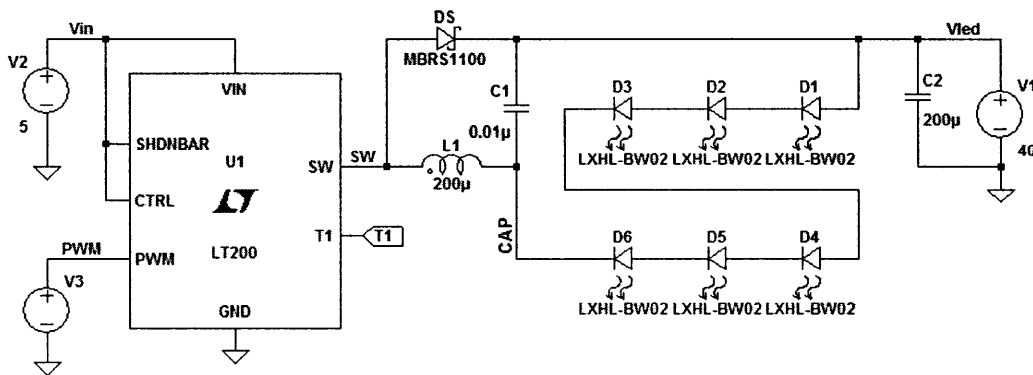


Figure 2-3: Typical Application Circuit for Proposed Part

The typical application circuit for a single channel version of the proposed part is shown in Figure 2-3. The internal switch is connected between the SW and GND pins. The diode DS, inductor L1, and capacitor C1 are the same as shown in the basic topology. The LED string, D1 to D6, is the actual load that the part drives. The shutdown pin (SHDNBAR) can be tied low to put the part in a sleep mode and

is tied high, usually to  $V_{in}$ , for normal operation. The analog control pin (CTRL) can be driven to a voltage between 0 and 1.25V (bandgap voltage) to achieve linear dimming, and when connected to a voltage higher than 1.25V, e.g.  $V_{in}$ , the part is turned fully on. A digital control signal (V3) is fed to the PWM pin to achieve 1000:1 pulse width modulation (PWM) dimming ratio by changing the duty cycle the LEDs. The details of analog and PWM dimming are discussed in the next section. Finally, the T1 pin is used for on-wafer temperature coefficient trimming, and is not bonded out for parts in production.

The part detects and regulates the output current (the current through the LED string) internally, by sensing the emitter current in the internal switch. Therefore, the switch pin (SW) is the only pin that is connected to the LED string. Moreover, in a multi-channel version, the SW pin is the only pin that needs to be populated (SW1, SW2 ...) to match the number of LED strings. This is why the part is named as a “one pin per channel” or “single-pin” LED driver.

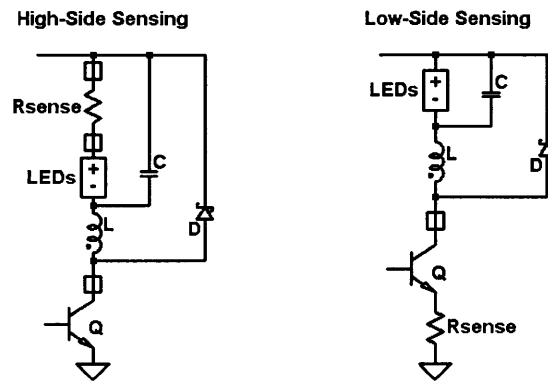


Figure 2-4: Current Sensing Schemes: High-Side v.s. Low-Side

Unlike the traditional high-side current sensing scheme for buck mode regulators (on the left in Figure 2-4), this part does not sense the LED current or the inductor current directly. Instead, it only looks at the emitter current in the power switch. This constraint increases design complexity. The inductor current, which has the same average value as the output (LED) current, is a good representation of the output current. However, the switch current only tracks the inductor current when the switch (Q) is on, as shown in Figure 2-4 and Figure 2-5. There is also a large

spike on the switch current at the moment the switch turns on, (Figure 2-5), which further complicates the current sensing task.

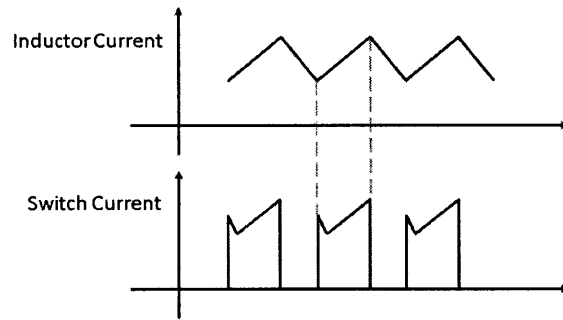


Figure 2-5: Current Sensing Schemes: Inductor Current v.s. Switch Current

## 2.3 Control Scheme

A simplified schematic of the buck mode current regulation system is shown in Figure 2-6. The control of the system is a combination of a duty cycle (or pulse width) modulation and a linear on-state current feedback. Both regulation points can be adjusted by the user via control pins: the PWM pin for duty cycle modulation, and the CTRL pin for linear control.

The duty cycle control is open loop. Since the PWM signal is relatively slow (100Hz for 1000:1 dimming, 1kHz for 100:1 dimming), the entire system is expected to track the PWM signal. The linear current control is closed loop. The average current when the switch is on (with the spike removed) is extracted from the sensed switch current (Figure 2-5) by using a sample and hold circuit, and is regulated in a feedback loop. The details of the two current control methods are addressed in the following two sections, followed by the analysis of the current feedback loops.

### 2.3.1 Duty Cycle Control

The duty cycle control is fairly straight-forward. The clock signal (top in Figure 2-7) is AND'ed with the PWM signal (middle), and the resulting signal is called the SET

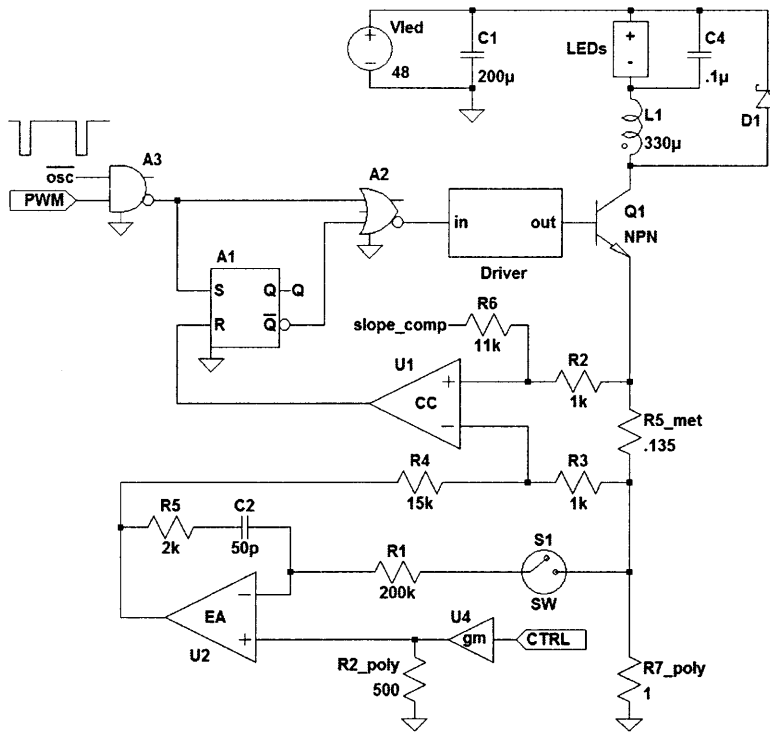


Figure 2-6: Simplified Schematic of the System

signal (bottom), used to control the power switch. When the PWM signal is low, the power switch is forced to be off, thus the output current vanishes.

Because the inductor current is not actively turned off, the LED light does not go off immediately after the PWM pin goes low. The delay between the falling edges of the PWM signal and the output current depends on the size of the inductor and the output capacitor. For a dimming ratio of 1000:1 at 100Hz, the minimum on-state time is 10µs. The delay is often chosen to be a small portion of that time, about 3µs. The delay should not be too small, since a shorter delay requires the use of a smaller inductor or a smaller output capacitor or both, which increases the output current ripple. Some choices of the inductor and capacitor values are available in Section 7.1.

In the actual implementation, the AND gate does not exist. Instead, the oscillator is turned off when the PWM signal is low. This design not only simplifies the circuitry, but also saves power, especially when the part is running under low PWM duty cycles.

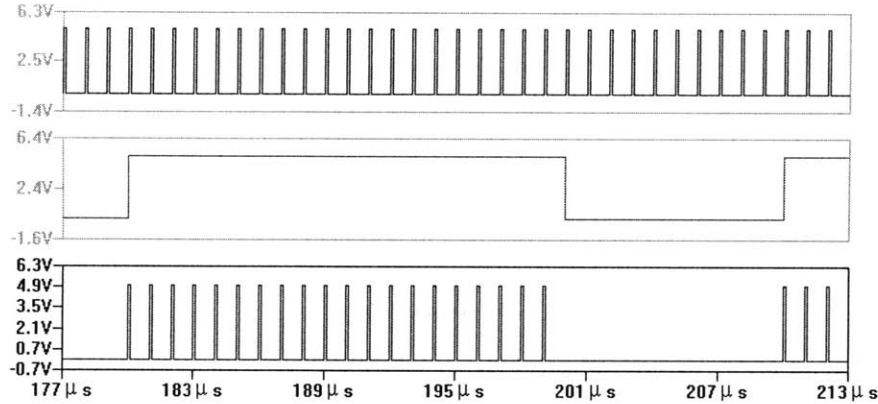


Figure 2-7: Pulse Width Modulation (PWM) Dimming

### 2.3.2 Output Current Estimation and Control

In order to introduce any feedback regulation on the output current, the output current first needs to be sensed. However, there is no direct way to sense the output current or the inductor current, since the only electrical connection between the output and the part is the switch pin. Nonetheless, the emitter current in the power switch is approximately the same as the inductor current while the switch is on, ignoring the base current. See Figure 2-4 and Figure 2-5. Since the inductor current and the output current have the same average value, as a first order approximation, the output current sensing is done by sampling and averaging the emitter current when the switch is on.

Once the output current is estimated, the feedback loop then forces the output current to track a preset target value, by changing the inductor peak current. The target output current is set by the CTRL voltage or the bandgap voltage, whichever is lower. With the absence of CTRL signal (floating CTRL pin), the CTRL voltage defaults to the bandgap reference voltage, and the corresponding output current is 100mA.

### 2.3.3 Loop Analysis

Ignoring the switching ripples, the system operates under linear feedback regulation in the on-state (when the PWM is high). A block diagram (Figure 2-8) is derived

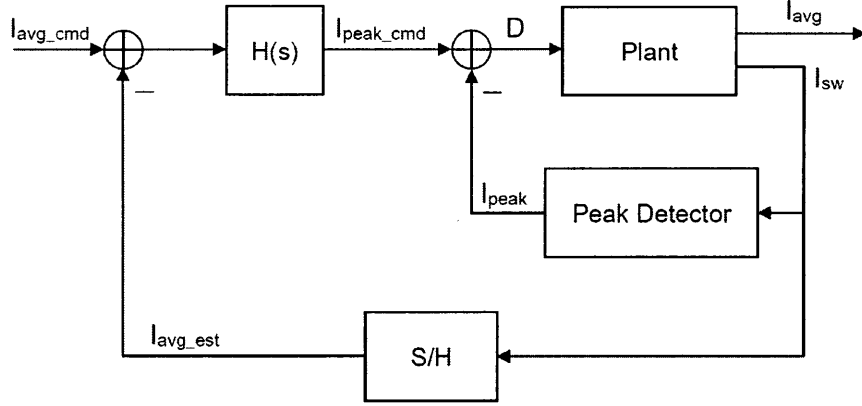


Figure 2-8: Block Diagram

from the system schematic (Figure 2-6). The feedback loop crossover frequency is set by the resistor-capacitor pair (R1 and C2) in the integrator, together with the attenuation ratio of the sensing resistors (R5\_met and R7\_poly), as shown in Figure 2-6. The loop transfer function is derived below.

The transfer function of the integrator (EA, R1 and C2, ignoring the effect of R5 for now) is:

$$H_{int}(s) = \frac{1}{R_1 C_2 s} \quad (2.1)$$

The effective input to the integrator is the difference between the intended LED output current,  $I_{avg\_cmd}$  (set by the CTRL pin voltage), and the estimation of the average inductor current,  $I_{avg\_est}$ , by the sample-and-hold circuit.

The sample-and-hold circuit measures the switch current, whose average is the same as that of the LED current when the switch is on, as discussed in the previous section. If the sample-and-hold circuit works ideally, the estimation  $I_{avg\_est}$  should track the actual output current  $I_{avg}$ :

$$I_{avg\_est} = I_{avg} \quad (2.2)$$

The output of the integrator goes to the current comparator (CC in Figure 2-6).

Right before the current comparator triggers, the voltages at its inputs are equal:

$$v_{C+} = v_{C-} \quad (2.3)$$

Thus at this time,

$$I_{peak\_cmd} = I_{peak} \quad (2.4)$$

At the moment the comparator triggers and turns off the power switch, the inductor current is at its peak value,  $I_{peak}$ . Therefore,

$$\begin{aligned} v_{C+} &= I_{peak}(R_{5\_met} + R_{7\_poly}) \quad (2.5) \\ v_{C-} &= \frac{R_3}{R_3 + R_4}(I_{avg\_cmd} - I_{avg\_est})R_{7\_poly}H_{int}(s) + \frac{R_4}{R_3 + R_4}I_{peak}R_{7\_poly} \quad (2.6) \end{aligned}$$

A slope compensation is introduced at the positive input of the comparator for the ripple stability. It has little impact on the loop dynamics, and therefore is ignored for simplicity.

Putting the equations together, with  $R_3/R_4 = 15$  and  $R_{7\_poly}/R_{5\_met} = 8$  approximately, we get the transfer function of the control block, that is, the integrator, the current comparator and the resistor divider:

$$H(s) = \frac{I_{peak\_cmd}}{I_{avg\_cmd} - I_{avg\_est}} = \frac{1}{3R_1C_2s} \quad (2.7)$$

The control block,  $H(s)$ , then commands the plant (the raw buck mode converter) with an intended peak inductor current  $I_{peak\_cmd}$ , and the ultimate output from the plant is the average LED current,  $I_{avg}$ . The relationship between  $I_{peak}$  ( $=I_{peak\_cmd}$ ) and  $I_{avg}$  depends on the output filter, the switching details and many other factors, which are mostly nonlinear. As a first-order approximation, we assume:

$$I_{avg} = \alpha I_{peak} \quad (2.8)$$

One of the dominant factors that affect the coefficient  $\alpha$  is the inductor current ripple. If the current ripple is small, the average and the peak are nearly the same,

and  $\alpha$  is close to 1. Even when the inductor current ripple is 30% of its average value,  $\alpha$  is still 0.77. When the inductor current ripple is constant,  $\alpha$  does not change. In this case, the “ $\alpha$  modulation” does not significantly change the loop crossover frequency. In other words, the “ $\alpha$  modulation” effect is often negligible in the real world.

Thus, the loop transfer function is,

$$L(s) = \alpha H(s) = \frac{\alpha}{3R_1C_2s} \quad (2.9)$$

Crossover frequency, assuming  $\alpha = 1$ ,

$$f_c = \frac{\alpha}{2\pi * 3R_1C_2} = 5.3kHz \quad (2.10)$$

The loop crossover is more than two orders of magnitude below the switching frequency (1MHz). Even with some moderate “ $\alpha$  modulation”, the loop can still crossover with near 90 degrees of phase margin. Therefore, this system is very stable.

## 2.4 Features and Challenges

### 2.4.1 Low-Side Output Current Sampling

The advantage of low-side current sampling is obvious: it simplifies the application circuit, and reduces part pin-count. The price we pay is the circuit complexity. This scheme does not only require a sample-and-hold circuit to properly sense the output current, but also needs a blank-out timer to block the current spike at the power switch turns on. Because of the blank-out time, some additional time alignment (delay network) is introduced to center the sampling signal with the switch current. (Figure 2-9) These details are discussed in the next two chapters.

### 2.4.2 PWM Dimming

As noted above, the loop crossover is about 5kHz, but the PWM control frequency can be as high as 1kHz. For low PWM duty ratios, the slow response of the loop

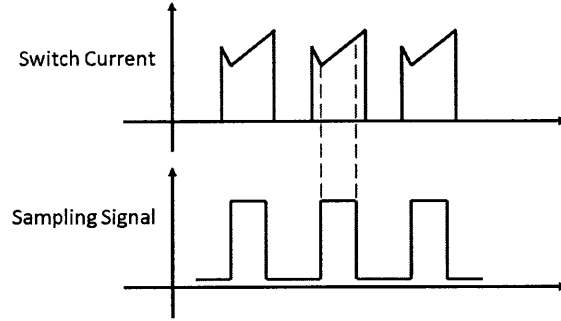


Figure 2-9: Current Sensing Schemes: Switch Current v.s. Sampling Signal

introduces an output error much larger than one part in a thousand. The solution is to save the loop information, say  $I_{peak\_cmd}$ , during the time when PWM is low, and restore it immediately after PWM goes high. Thanks to the new BiCMOS process at Linear Technology, this performance is achieved by using a very low leakage hold capacitor (C2) in the integrator, a MOS input pair for the error amplifier (EA) and a low leakage MOS switch as the sampling switch (S1) (see Figure 2-6). Thus, the total leakage current from the hold capacitor (C2) is lower than 10pA, and therefore, the capacitor (C2) voltage droop during the time that the PWM signal is low is less than 0.2mV.

### 2.4.3 Output Accuracy

There is a fundamental difficulty in this design. It is necessary to get an accurate output current based on a voltage reference, but precise resistor values are not available with the IC process used. This issue is solved in multiple steps.

For the absolute accuracy, some trimming procedure is required. In this design, a metal-fuse is included to trim the output current to exactly 100mA when the part is fully on. This is further discussed in Section 7.4.

The second step is the temperature stability. In this process, the thin-film resistor is the type with the lowest temperature coefficient. However, the thin-film resistors have large values (in  $k\Omega$ ) which are not suitable for switch current sensing. Therefore, the method with a matched poly resistor pair is used: the CTRL voltage is first converted to a temperature-stable current with thin-film resistors, then this current

is fed into one poly resistor ( $R_{2\_poly}$  in Figure 2-6) in the matched pair to generate the reference voltage for the integrator. The other poly resistor ( $R_{7\_poly}$ ) in this pair is, of course, used as a switch current sensor. This poly pair is carefully laid out so that they have well-matched temperature coefficients. The layout details are discussed in Section 6.3.



# Chapter 3

## Sampling Scheme

This chapter extends the discussion on the sample-and-hold circuit that was introduced in Chapter 2. The synchronous sample-and-hold circuit is essential for low-side current sensing buck mode regulators, because the power switch current is discontinuous, and only represents the output current when the switch is on. Various techniques, including current spike blanking and injection charge cancellation, have to be implemented in the sample-and-hold circuit in order to measure the switch current and estimate average output current accurately.

### 3.1 Global View

The general idea of the sample-and-hold circuit is quite simple. As shown in Figure 3-1, the sampling switch (S1) is synchronized with the power switch (Q1). Therefore, the integrator (error amplifier with R1 and C2) has the inductor current  $I_L$  multiplied by  $R_{7\_poly}$  as its input when the power switch is on, and sees high impedance when the switch is off.

In steady state, the two inputs to the error amplifier (EA) are forced to be equal. That is,  $V_- = V_+$ . On the other hand,  $V_-$  equals the average on-state voltage (i.e. average over the sampling time) across the current sensing resistor  $R_{7\_poly}$ , so that the net average current through  $R_1$  is zero.

$$V_- = I_L R_{7\_poly} \quad (3.1)$$

And nominally,

$$V_- = V_+ = 100mV \quad (3.2)$$

Given  $R_{7\_poly} = 1\Omega$ , the nominal output current is set at 100mA.

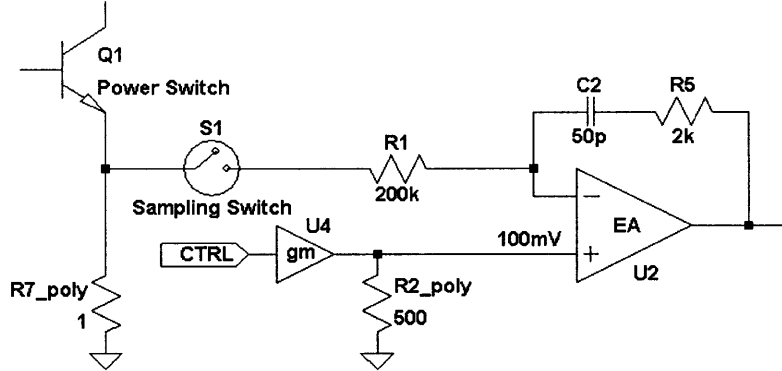


Figure 3-1: Sample-and-hold Circuit

## 3.2 Sampling Issues

### 3.2.1 Switch-on Current Spike

As shown in Figure 2-9, there is a current spike in the power switch at the time it turns on. This spike is caused by the parasitic capacitor at the collector of the power switch. When the power switch is off, its collector is at a high voltage  $V_{in}$ , and the parasitic capacitor is charged up; at the moment the switch is turned on, all the charge stored in this parasitic capacitor gets dumped to the ground through the power switch.

This issue by itself can be solved by introducing a simple current blanking signal to block the sampling switch (delay sampling) by a short amount of time. In this case, the blanking time is about 50ns. A simplified current blanking circuit is shown in Figure 3-2.

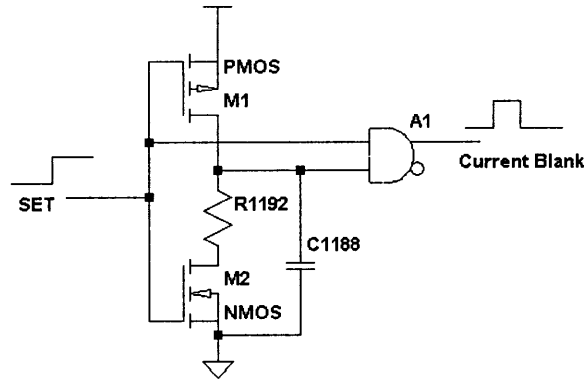


Figure 3-2: Current Blanking Circuit

With the current blanking circuitry, the remaining issue is that the sampling signal is no longer symmetric around the switch current. From Figure 3-3, one can see the average of sampled signal is higher than the average of the real switch current (without the current spike). Therefore, the output current is over estimated.

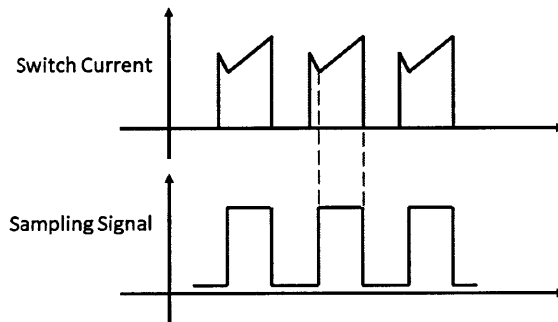


Figure 3-3: Asymmetric Sampling Signal

With a switching period of  $1\mu s$  and a blanking time of  $50ns$ , depending on the duty cycle, the estimation error can be 2.5% ( $D=1$ ) to 12.5% ( $D=0.2$ ) of the inductor current ripple. For a current ripple of 40%, this error can contribute as much as 5% to the total output current error. Moreover, since the duty cycle is a function of the input voltage, and the error depends on the duty cycle, this effect degrades the line regulation.

Obviously, this issue can be solved by introducing an equal amount of blanking time at the end of the sampling time. However, this idea cannot be easily implemented because it requires a prediction of the switch turn-off edge. A few possible solutions

are explored in Section 3.3, and the implementation is detailed in the next chapter.

### 3.2.2 Switch Charge Injection

The sampling switch (S1) shown in Figure 3-1 is an n-type MOSFET with substrate connected to ground. Under normal operation conditions, the drain-to-source voltage can never be larger than 150mV, which guarantees that the body diodes stay off. This device is symmetric, and the drain and the source may interchange in different situations.

Part of the charge stored in the parasitic capacitors of the MOS switch is dumped into the integration capacitor at the switch transitions, and the charge causes a steady state error. Despite the symmetry in the sampling switch, one end of the the switch is connected to a much lower impedance ( $R_{7\_poly} = 1\Omega$ ) than the other ( $R_1 = 200k\Omega$ ), and therefore the charge dump process is asymmetric. (Figure 3-1)

When the sampling switch turns on, almost all the charge in the switch dumps through the low impedance path, so little charge gets dumped to the integration capacitor. However, when the sampling switch turns off, the behavior is slightly more complicated: First, when the gate voltage of the sampling switch drops but remains above  $V_T$ , most of the charge still goes through the channel and  $R_{7\_poly}$  to ground; then, when the gate voltage gets close to  $V_T$ , channel resistance increases, and the charge splits in both direction; finally, the MOS switch turns completely off, and the rest of the charge on the overlap parasitic capacitor (only the integrator side) all dumps to the integration capacitor.

Roughly, the charge that dumps to the integration capacitor during the sampling switch turn-off transition is,

$$Q_{CI} = C_{OL}V_T = C_{GD}V_T \quad (3.3)$$

The size of  $C_{GD}$  is nowhere close to that of the integration capacitor ( $C_2$ ). However, this error is cumulative. In each clock cycle, the amount of charge  $Q_{CI}$  dumps to  $C_2$ . This is equivalent to a steady state leakage current through  $R_1$ . In order to

make up for the difference, the output current is brought up (erroneously) by  $\Delta I$ ,

$$\frac{\Delta I R_{\tau\text{-poly}}}{R_1} DT = Q_{CI} = C_{GD} V_T \quad (3.4)$$

Here  $D$  is the duty cycle, and  $T$  is the switching period,  $1\mu s$ .

Even with a  $C_{GD}$  in the sub- $fF$  range, the output current error can still be as large as a few mA, or a few percent of output current. The error is duty cycle (or input voltage) dependent, and it also changes with temperature ( $V_T$ ).

### 3.3 Methods of Blanking Time Control

#### 3.3.1 Capacitor Timer

From the current comparator triggering to the power switch turning off, the delay is tens of nanoseconds. If the sampling switch is turned off when the current comparator triggers, and a timer measures this delay and applies the same amount of delay to the beginning as the current blanking time, the sampling signal will be centered around the power switch current.

A simplified schematic of a capacitor timer is shown in Figure 3-4. It charges up the first capacitor ( $C_1$ ) during the delay from the current comparator to the power switch, holds the voltage on  $C_1$ , and then charges up the second capacitor ( $C_2$ ) during the current blanking time of the next switch cycle. Once the voltage on  $C_2$  reaches the same level as that on  $C_1$ , the comparator  $U_1$  turns on the sampling switch for the new cycle.

#### 3.3.2 Delay Lock Loop

A delay lock loop (DLL) employs the same timer as above, but instead of trying to match the delays in an open loop way, it takes measurements of both delays, and forces them to equal with the help of a feedback loop.

Specifically, the DLL first measures the delay from the power switch turn-on edge to the sampling switch turn-on edge, or the current blanking time, and also measures

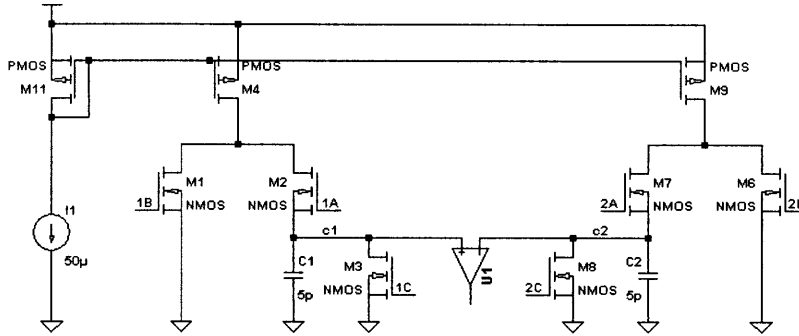


Figure 3-4: Capacitor Timer

the delay from the sampling switch turn-off edge to the power switch turn-off edge. Then, the DLL integrates the difference between the two delays, and adjusts the current blanking time to force the difference to be zero. In that way, the sampling signal is centered around the power switch current.

### 3.3.3 Matched Delay Network

The matched delay method also utilizes the current-comparator-to-power-switch delay, and uses the current comparator output to turn off the sampling switch. But instead of measuring the delays and trying to match them, the matched delay method simply uses a matched delay network as the current blanking timer.

A matched delay network is a mirror copy of the circuit from the current comparator to the power switch. Thanks to good matching properties in integrated circuits, the matched delay network has approximately the same delay as the real comparator, driver, and power switch chain. Therefore, the two delays are matched, and the sampling signal is centered. In fact, all the components in that chain do not have to be copied; a scaled-down version works almost as well as a full copy.

### 3.3.4 Comparison of Blanking Time Control Methods

The capacitor timer is a neat circuit, but the whole idea of matching the delays with a stop watch is more like a head-fake. The comparator ( $U_1$ ) in the timer circuit (Figure 3-4) has to be ultra fast: much faster than the to-be-matched delays, which

are around 30ns. If one had the fast comparator, one could have used it as the current comparator, followed by some RC timer similar to Figure 3-2 to match the delays.

The “right way” to get rid of the delay mismatch is to use a delay lock loop. Like PLLs, DLLs have good performance, but they are much more complex compared to the alternatives. One possible issue is the DLL may interfere with the main loop.

The matched delay network is relatively easy to implement, and has acceptable performance. Since the starting error from asymmetric sampling is about 5%, reducing it by a factor of 5 or 10 is sufficient. Given the design time constraint, the matched delay network is implemented in this project. Details are discussed in the next chapter.

### 3.4 Switch Charge Cancellation

From the discussion in Section 3.2.2, the output current error  $\Delta I$  due to switch charge injection can be estimated by,

$$\frac{\Delta I R_{7\_poly}}{R_1} DT = C_{GD} V_T \quad (3.5)$$

One way to reduce the error is to use a smaller integration resistor,  $R_1$ . Intuitively, a smaller  $R_1$  means a larger gain-bandwidth product (or loop crossover frequency), which leads to a better error correction capability. However, increasing the loop crossover frequency too much may cause stability problems. In this design, a metal trim is placed with the options of  $R_1 = 200k\Omega$ ,  $100k\Omega$ , or  $50k\Omega$ .

Furthermore, given the injected charge is approximately  $C_{GD} V_T$ , the same amount of charge can be pulled out from the output node of the sampling switch, so as to achieve injecting charge cancellation. A special low-charge-injection sampling switch, shown in Figure 3-5, was designed for this purpose.

This special sampling switch looks more like a hack. However, (we believe) this is a carefully designed hack, and will always work, as explained below.

The MOS switch on the left,  $M_1$ , is the main switch. The sampling signal turns  $M_1$  off when switching from the sample mode to the hold mode. The inverter  $A_1$

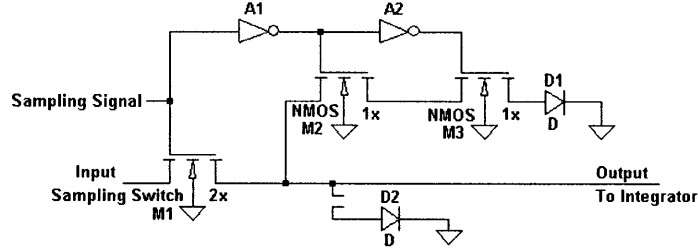


Figure 3-5: Low-charge-injection Sampling Switch

is designed to be slightly slower than the switches ( $M_1$ ,  $M_2$  and  $M_3$ ), while the inverter  $A_2$  is faster than the three switches. The power supply for  $M_2$  and  $M_3$  is approximately  $2V_T$ .

From Section 3.2.2, the excess (negative) charge injected to the output by  $M_1$  at the falling edge of the sampling signal is,

$$Q_{CI\_M1} = C_{OL\_M1} V_T \quad (3.6)$$

Because of the carefully chosen inverter delays, after  $M_1$  is off,  $M_2$  and  $M_3$  turn on and off respectively at the same moment.  $M_2$  and  $M_3$  are matched devices, so ideally  $M_3$  takes all the charge in the channel (or on  $C_{OX}$ ) of  $M_3$  and the charge in the  $C_{OL}$  that is connected to  $M_3$ . The charge on the  $C_{OL}$  of  $M_2$  on the other side, that is, connected to  $M_1$ , gets dumped to the output node of sampling switch. The charge dump by  $M_2$  is,

$$Q_{CI\_M2} = C_{OL\_M2} V_{DD} \quad (3.7)$$

$M_2$  is sized to be half of  $M_1$ , which says,  $C_{OL\_M2} = \frac{1}{2} C_{OL\_M1}$ . The voltage  $V_{DD}$  is chosen to be  $2V_T$ . Thereby,  $Q_{CI\_M2} = Q_{CI\_M1}$ , yielding perfect switch charge cancellation.

One potential issue with this cancellation method is that the amount of charge  $M_3$  takes from  $M_2$  is non-deterministic. It relies on the precise timing, and may be sensitive to process variations. Circuit simulation does not give any convincing results, even though spice claims more than 95% of cancellation in typical cases, and more than 80% of cancellation in all process/temperature corners. However,

given the starting error is only a few percent, and the absolute error (not the input or temperature dependence) can be trimmed out aggregately, reducing the charge injection by a factor of 3 to 5 is sufficient.



# Chapter 4

## Matched Delay Network

This chapter describes the circuits that generate the proper sampling signal for the sample-and-hold in Chapter 3. The sampling signal goes low when the current comparator triggers, and after the delay of the latch logic and the power switch driver, the power switch turns off. The same amount of delay is applied to the rising edge of the sampling signal, as the blanking time for the current spike.

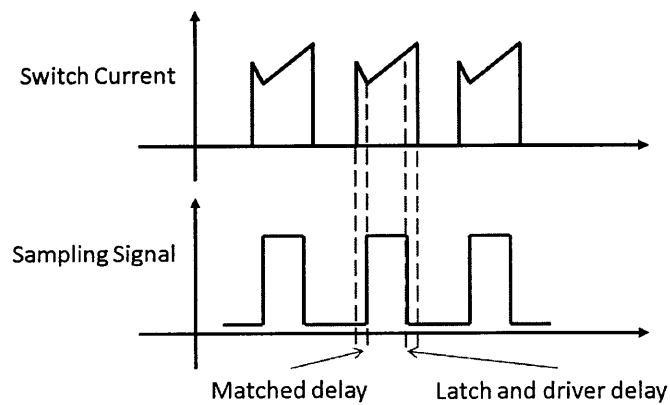


Figure 4-1: Matched Delays

## 4.1 Delay Models

### 4.1.1 Logic Delay

From the current comparator to the power switch driver, there are a few inverters, an SR latch and a NOR gate. A copy of the minimum size inverters are used in the model, and the NOR gate is replaced as a NAND gate (not shown in Figure 4-2) with customized size for design simplicity. With area constraints, the latch is modeled as a pair of trimmable asymmetric inverters.

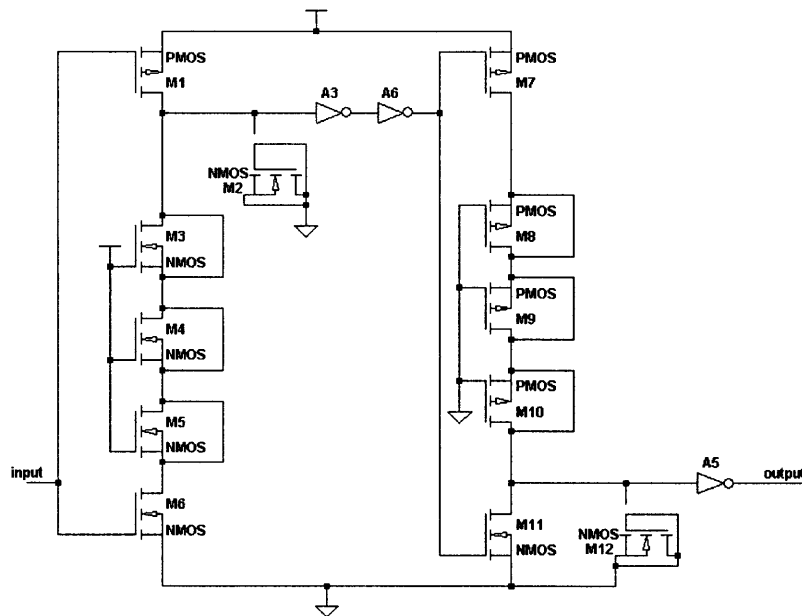


Figure 4-2: Logic Delay Model

### 4.1.2 Driver Delay

The driver of the power switch (or the giant NPN transistor) is a series of bipolar inverters. In order to drive the power switch on and off fast, the transistors in the driver have large sizes, and depending on the output current, they often operate in semi-saturation.

A scaled down version of the driver is made, and the current sources are chosen so that the transistors in the model are operating at the same “forced beta” ( $i_C/i_B$ )

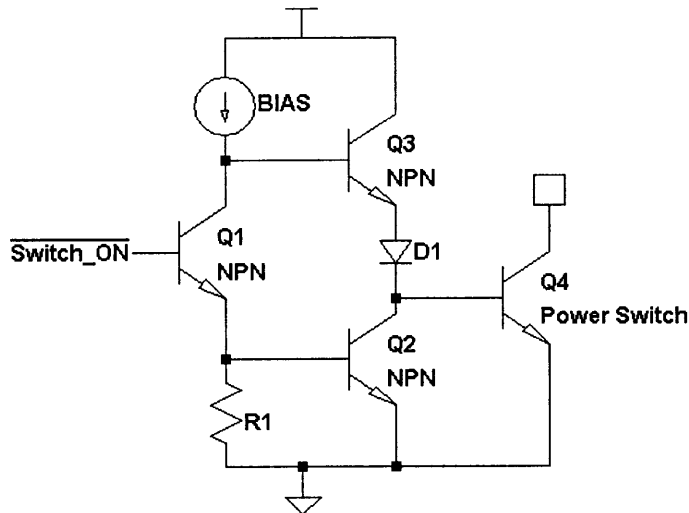


Figure 4-3: Simplified Driver Circuit

as that of the transistors in the actual driver. The current sources can also be metal-trimmed.

The current gain ( $\beta$ ) of the transistors can change dramatically at different temperatures. The driver circuit is physically close to the power switch, and thus, gets hot quickly after the part is powered on. The driver delay model has to make up for this temperature drifting effect. The best solution was, to place the model circuit equally close to the power switch, so that they are on the same isothermal line and match well with each other. More details are presented in Chapter 6.

### 4.1.3 Switch Delay

There is one delay that cannot be modeled or corrected: the switch delay. After the base of the power NPN is driven high with a lot of current (and enough base charge), the collector voltage stays high for a little while due to the capacitance at the collector node (switch node). As shown in Figure 2-3, the collector is connected to an inductor and a Schottky diode externally. Unless measuring the switch node voltage directly, the parasitic capacitance, as well as the delay, is unknown when designing the chip, and depends on the customer's choices of discrete components and board layout. However, a good board design should minimize the parasitic capacitance at

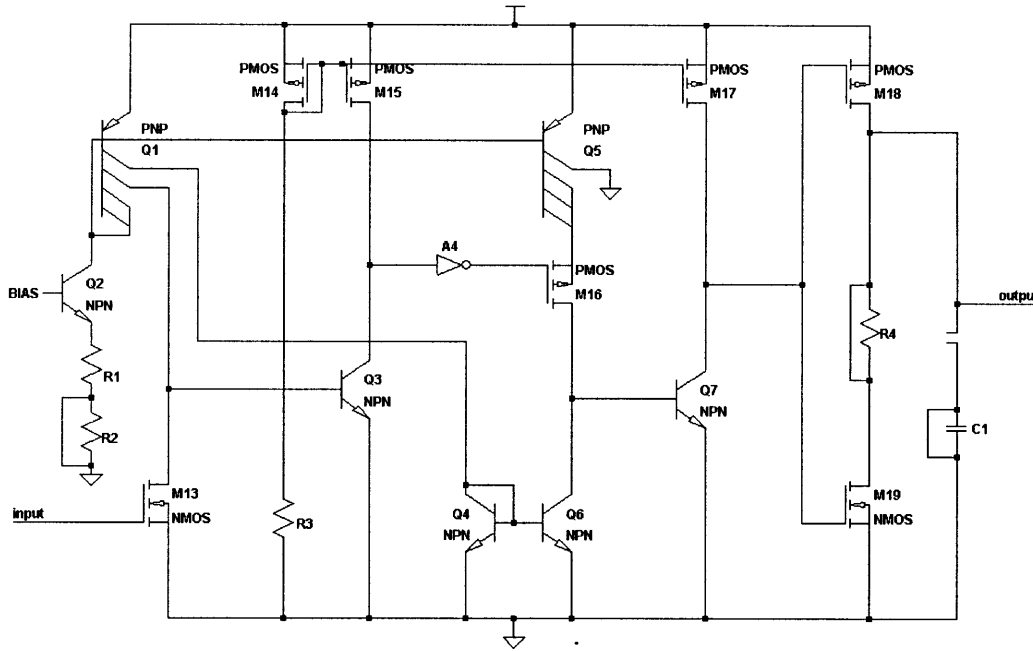


Figure 4-4: Driver Delay Model

the switch node (down to a few pF), and as a result the switch delay is typically a few nanoseconds. In this case, the error from switch delay can often be ignored.

## 4.2 Trimming Options

### 4.2.1 Metal Trimming

When designing the matched delay network, there was not enough experimental data on the time delays of semi-saturated bipolar transistors or CMOS latches, or a spice model for these operation regions. Therefore, many metal options are added to the design for post fabrication trimming. For example, in Figure 4-2, the drains and sources of  $M_3$ ,  $M_4$ , and  $M_5$  are shorted originally, and they each can be “cut in” to increase the falling edge delay if needed.

There are three major trimming spots in this delay network: a pair of CMOS inverters with independently adjustable rising/falling edge delays, adjustable current sources to change the saturation level of the bipolar inverters, and a variable RC delay. Practical details about metal options (layout and cut/smear) are discussed in

## 4.2.2 Trimming Procedure

Since direct delay measurements can hardly be made, a well-designed trimming plan is needed for the delay network. The mismatch between the actual delay and the matched network delay is only tens of nanoseconds or less, which is comparable to the delay variation caused by the probe tips.

As discussed in Section 3.2.1, the delay mismatch causes an error in the average output current estimation. When the duty cycle decreases, the estimation error increases, which shows up as an imperfection in the line regulation (input voltage dependence).

The duty cycle dependence is harmful as an error source, but it also provides hints for the delay trimming. If the matched delay was too short, the output would be underestimated, and thereby the output current would be above the command. Keeping the command and the load the same, if the input voltage was increased, the duty cycle would decrease, and the estimation error would increase. Given the estimation error resulted in a positive error in the output current, when the estimation error increased, the output current would further increase. By iteratively correcting the delay network, the delay mismatch would be eliminated.

Test Condition		Test Result	Conclusion
Input Voltage	Duty Cycle	Output Current	Matched Delay
increase	decrease	increases	too short
increase	decrease	decreases	too long

Table 4.1: Delay Mismatch Trimming



# Chapter 5

## Chip Design

In this chapter, the whole chip design is revisited in an analyst's perspective. The actual circuit design of each block is described first, followed by detailed explanation on a few features that are not previously discussed and are unique to this chip, including the implementation of the PWM function, the CTRL pin interface, and the power on reset.

### 5.1 Overview

This chip is based on the previous IC designs of Linear Technology, LT3951 and LT3594. It consists of eight function blocks as shown in Figure 5-1: the internal supply, the oscillator, the logic control, the current comparator (CC), the delay network, the error amplifier (EA), the driver together with the power switch, and the power-on reset circuit (POR).

### 5.2 Internal Supply

#### 5.2.1 Bandgap

The bandgap circuit is the reference for the entire IC and regulates the output current; thus, it has to be accurate and constant across temperature and process corners.

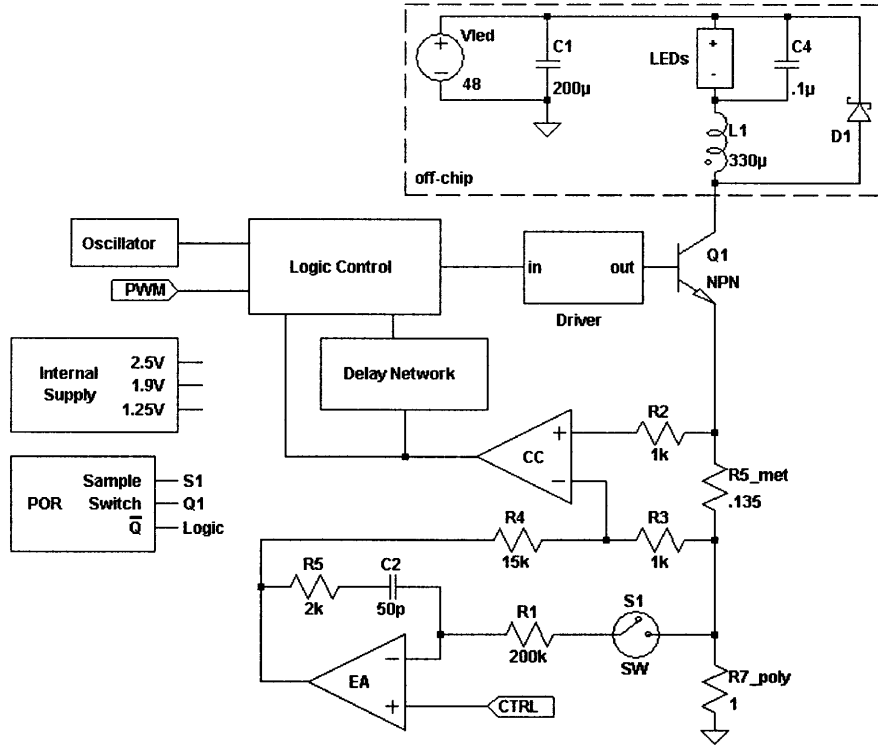


Figure 5-1: Chip Block Diagram

A bandgap reference is the combination of a negative temperature coefficient voltage (which is usually a  $V_{be}$ ) and a positive temperature coefficient voltage. A  $\Delta V_{be}$  is proportional to absolute temperature (PTAT), and is often used as the positive temperature coefficient voltage. When these two voltages are combined in the proper proportion, the temperature coefficients cancel to yield a voltage which is approximately constant across a wide range of temperature.

The  $\Delta V_{be}$  generated by  $Q_3$  and  $Q_4$  is not accurately known before fabrication because the effective area ratio of the two transistors cannot be designed to be 0.1% accurate. Therefore, some trimming procedure is required to get a zero temperature coefficient.

In reality, this chip does not have a bond pad for the bandgap voltage. In the final trimming process, instead of the bandgap voltage, the output current is trimmed to have a zero temperature coefficient. This is a better approach, because what matters is the output current temperature stability, and the bandgap is used to sweep out the

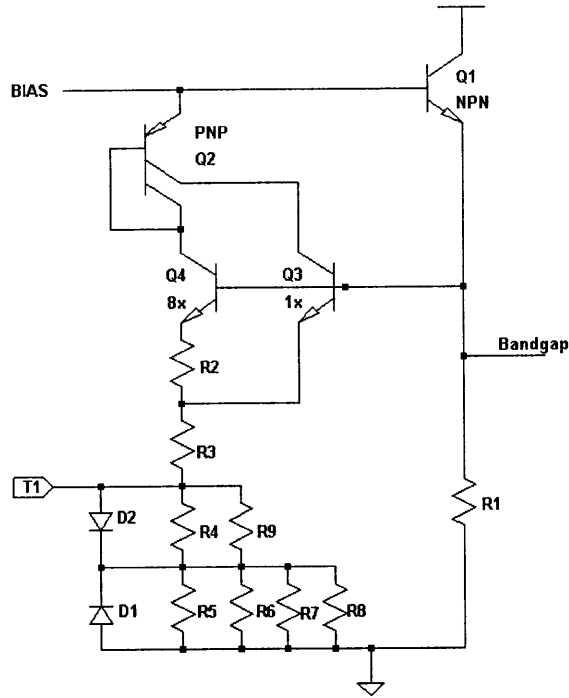


Figure 5-2: Simplified Bandgap Circuit

residue temperature coefficients in the rest of the circuit.

## 5.2.2 Internal Rail Buffers

From the bandgap voltage, a few internal rail voltages are generated to power up the chip. These voltages are generated by linear voltage regulators. The 2.5V supply is the most commonly used rail voltage over the chip, and the 1.9V ( $\text{Bandgap} + V_{be}$ ) is also used in many blocks.

The shutdown function is also implemented here. When the shutdown is enabled, the bias for the bandgap circuit is clamped down to ground. All the internal rail buffers are thereby turned off. The quiescent current in shutdown mode is less than  $1\mu A$ .

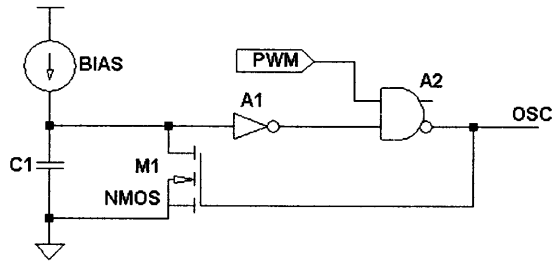


Figure 5-3: Simplified Oscillator Circuit

## 5.3 Oscillator

The oscillator circuit is self-explanatory. The frequency is determined by the bias current, the capacitor and the inverter threshold. The bias current can be programmed at two levels, corresponding to 500kHz and 1MHz switch frequency.

The PWM function is implemented in this block. When PWM goes low, the NAND gate always gives a high at its output, therefore, the capacitor is always discharged and the oscillator is disabled. At this time, the chip is not switching and the output is zero, but all the internal supplies are still on, and the integrator still remembers its previous state (Section 2.4.2). This is essential for fast wake-up at the PWM turn-on transition, enabling a dimming range up to 1000:1 at 100Hz.

Another advantage of integrating the PWM function into the oscillator is the so-called “PWM synchronization”, which simply means the oscillator rising edge is lined up with the PWM rising edge. This is done by starting a fresh clock cycle each time when PWM goes high. The PWM synchronization feature is important for applications that require very low dimming ratios (e.g. the GPS back light in a dark night). For a fixed PWM pulse that is only a few switching cycles long, if not synchronized, the relative phase of the PWM signal and the oscillator output may vary over time, and thus the output current pulse has a time-variant width. The output current may also contain sub-harmonics of the PWM frequency. In the case of a back light, the screen blinks.

## 5.4 Current Comparator

### 5.4.1 Common Base Differential Pair

The current comparator detects and regulates the peak current in the power switch. It measures the voltage across a small current sensing resistor ( $0.135\Omega$ ), and triggers when this voltage reaches a threshold set by the error amplifier. The common base comparator topology is chosen for its speed, and moderate input impedance.

As shown in Figure 5-4, the current sensing inputs are differential, and the peak current threshold is introduced as an offset.

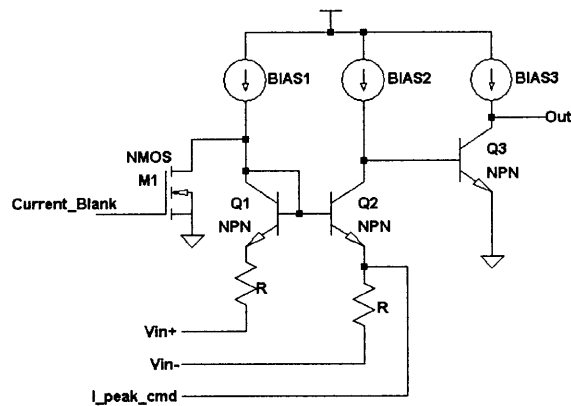


Figure 5-4: Simplified Current Comparator Circuit

### 5.4.2 Current Blanking

A current blanking circuit is also adopted in this comparator. The current spike through the power switch at its turn-on transition may be large enough to falsely trigger the current comparator (Figure 2-5). This is not the same current blanking function as used in the sampling circuit, although the two blanking circuits are similar, and they target at the same current spike.

The blanking circuit is a simple one-shot on the rising edge of the switch-on signal (SET), as shown in Figure 5-5. The current comparator output is then forced low when the blanking signal is present (Figure 5-4).

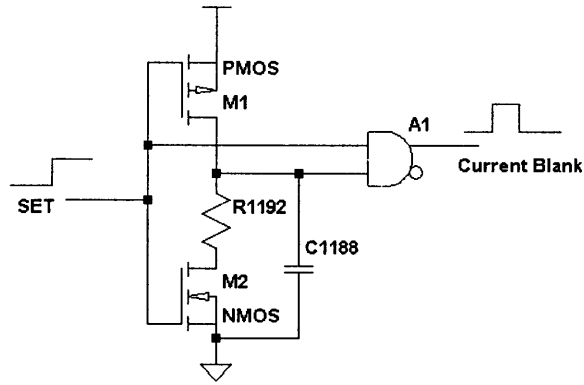


Figure 5-5: Simplified Current Blanking Circuit

### 5.4.3 Hard Current Limit

Under no circumstances does the switch current need to be larger than 200mA. A hard current limit circuit is used to ensure this rule. The hard limit is necessary especially during startup. The global feedback loop is relatively slow ( $5kHz$ ), and it takes a few milliseconds for the integration capacitor to charge up. Without the hard current limit, the inductor current may keep increasing during that time, up to a few amps. The hard limit is also helpful as a fault protection.

The hard current limit circuit is very similar to the normal current comparator (Figure 5-4). With a preset offset, the hard current limit circuit always triggers at about 200mA.

## 5.5 Delay Network

As discussed in Chapter 4, the delay network is a combination of a logic delay model, a driver delay model, and an adjustable RC delay circuit. It works as a one-shot circuit at the power switch turn-on edge. The width of the one-shot pulse (or the blanking signal) is the matched delay time. The matched delay blanking signal is then passed to the logic circuits to generate the sampling signal.

## 5.6 Logic Control

The digital logic circuit that controls the power switch and the sampling switch is very simple. An SR latch controls the power switch. The oscillator sets the latch, and the current comparator, together with the hard current limit circuit, resets it. The sampling switch is on as long as the power switch is on, except when the current comparator triggers or the matched delay blanking is on.

## 5.7 Error Amplifier

The error amplifier is a standard one-stage operational amplifier with PMOS input pairs. It has low input offset to minimize the output current error. Large PMOS devices with cross coupled layout are used to increase matching. The layout details are discussed in Section 6.2.

The analog dimming (CTRL) function is also implemented in this block. The CTRL voltage or the bandgap voltage, whichever is lower, is proportionally converted into a current, and this current is fed into a poly resistor ( $R_{2\_poly}$ ) that is matched with the current sensing resistor. (Figure 5-6) This series conversion, from voltage to current and back to voltage, also helps move from the (quiet) analog ground (AGND) to the (noisy) power ground (PGND). This step is necessary because the current sensing resistor is in series with the power switch and it carries a large current to ground, namely PGND.

## 5.8 Driver

The power switch is a specially designed large NPN bipolar transistor, or an array of them. To drive it fast and efficiently, a customized driver circuit is needed.

A simplified schematic of the driver is shown in Figure 5-7. It operates under  $V_{in}$  directly, instead of the internal rail, for large currents. Therefore, the devices are carefully chosen to withstand high voltages (up to 70V).

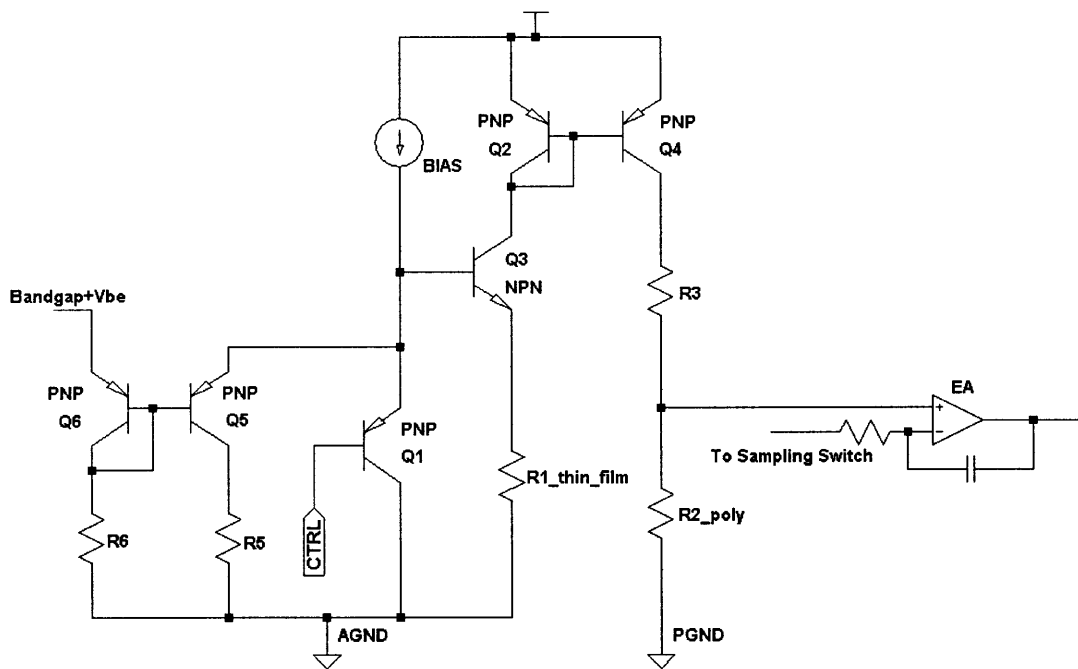


Figure 5-6: CTRL Signal Input

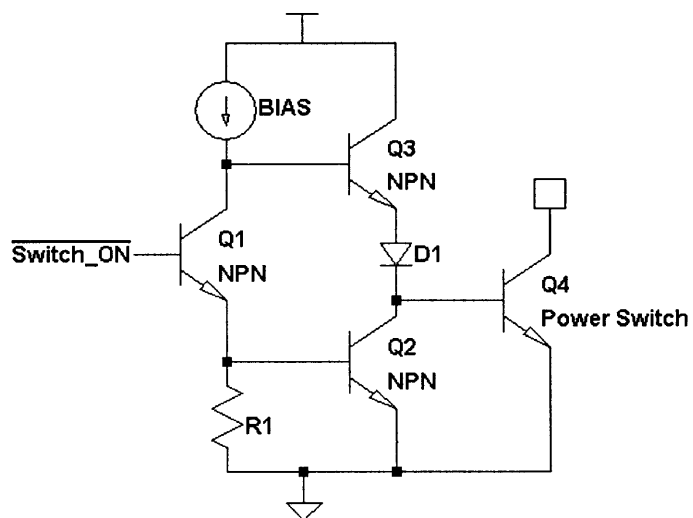


Figure 5-7: Simplified Driver Circuit

In order to turn the power switch (Q4) on rapidly, a large current (close to the normal collector current, 100mA) is dumped into the base of the power device at the turn-on transition. However, if the base current was that high during normal operation, the power device would be in hard saturation, and it would take a long time to turn off. Thus, a saturation catch circuit (sat-catch) is implemented. (Not shown in Figure 5-7) Once the Q4 collector voltage drops below 0.4V (or 2/3 of  $V_{BE}$ ), the sat-catch kicks in and steals some base current from the power device. The sat-catch works as a small feedback circuit that keeps the power device out of hard saturation. Thereby, the power device can switch on and off quickly.

## 5.9 Power-on Reset

Some of the logic circuits in this part, e.g. the SR latch, may have ambiguous initial states when the system is powered on. In order to make sure the part always starts from a known condition, a power-on reset circuit is needed.

The power-on reset circuit is shown in Figure 5-8. When the input voltage first goes high,  $M_1$  is still off, and the following MOSFETs,  $M_3$  to  $M_5$ , force the sampling switch, the power switch, and the negative output of the SR latch, to be off or low, respectively. After a short while, the  $C_{GS}$  of  $M_1$  is charged up through  $M_2$ , and  $M_1$  turns on. In the steady state,  $M_1$  is always on, and then the power-on reset circuit does nothing to the rest of the world.

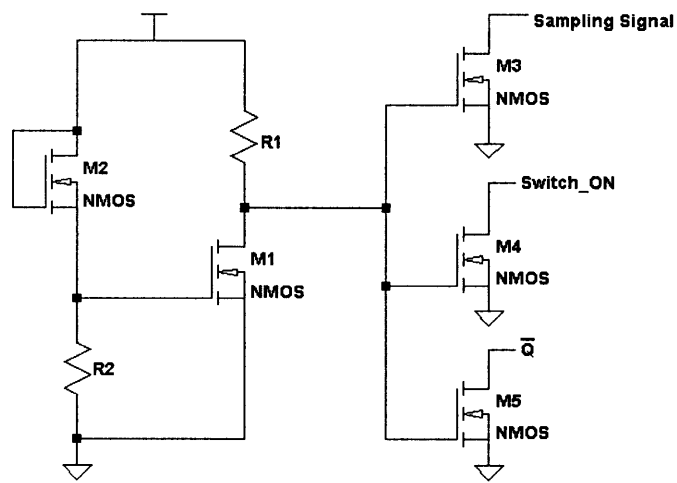


Figure 5-8: Power-on Reset Circuit

# Chapter 6

## Layout Issues

This chapter briefly discusses about some of the layout issues with this part. The analog layout is a piece of mysterious art work, and the discussion here is neither detailed nor complete. Instead, this chapter is only focused on a few techniques mentioned in the previous chapters.

(A side note: Up to this point, all the circuit design is done. One might think, “the rest are just details.” This is both true and false. It is true that the layout work is much into the details, and does not have many “big ideas.” However, it is false because the layout work actually has as many challenges as the circuit design does. Both time-wise and effort-wise, it requires as much as the design phase.)

### 6.1 Floor Plan

This chip layout starts with an advised area constraint of 80mil\*25mil. With the constraint, a floor plan is made, as shown in Figure 6-1.

The square boxes in capital letters are bonding pads, and the boxes in small letters are function blocks.  $R_{sense}$  and  $R_{metal}$  are two current sensing resistors, corresponding to  $R_{7\_poly}$  and  $R_{5\_met}$  in Figure 5-1. The pre-regulator (pre-reg) and the bandgap are part of the internal supply block, and the power-on reset is placed inside the pre-reg.

The sensitive parts, such as the bandgap and the error amplifier, are placed far

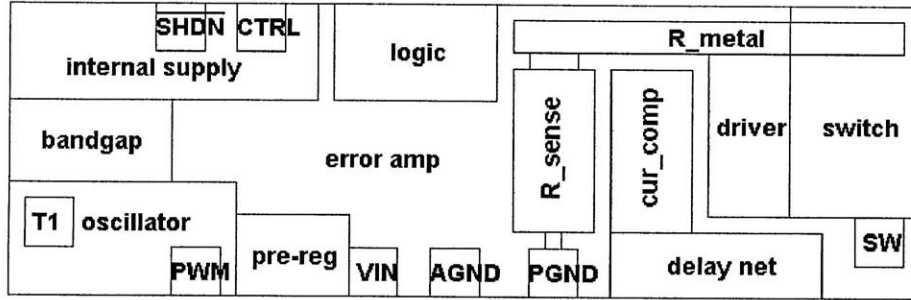


Figure 6-1: Layout Floor Plan

from the power switch, which is hot and noisy. The matched delay network (delay net) is placed next to the power switch and the driver circuit, so that they are always at about the same temperature to improve delay matching.

## 6.2 Matched MOSFET Pairs

As discussed in Section 5.7, the input PMOS pair of the error amplifier has to be well matched, in order to minimize the input offset. A cross coupled PMOS pair is designed in a separate n-well, as shown in Figure 6-2. The layout follows the common centroid (ABBA) rule, and whenever there has to be a metal crossing the matched pair, it has to go over both devices.

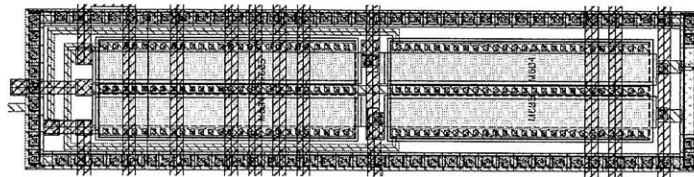


Figure 6-2: Matched MOSFET Pairs Layout

## 6.3 Matched Poly Resistors

One of the current sensing resistors,  $R_{7\_poly} = 1\Omega$  (Figure 5-1), is matched with another poly resistor in the error amplifier,  $R_{2\_poly} = 576\Omega$  (Figure 5-6). The matched resistors are both made of  $24\Omega$  unit resistors. The  $1\Omega$  resistor is made up of 24 unit

resistors in parallel, and the  $576\Omega$  resistor is 24 unit resistors in series. It also follows the common centroid rule, and there are dummy devices around the 6 by 8 resistor array.

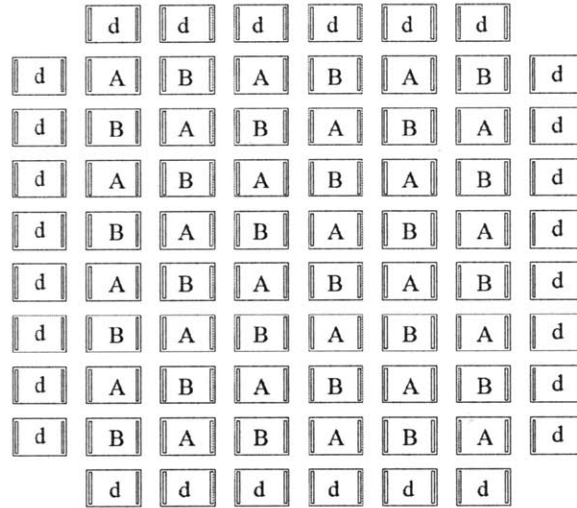


Figure 6-3: Matched Poly Resistors Layout Plan

The layout plan is shown in Figure 6-3. All the A's are part of the current sensing resistor,  $R_{7\_poly}$ , and they are in parallel; all the B's are part of  $R_{2\_poly}$ , and they are in series. The actual layout is shown in Figure 6-4. (Notice, it's rotated to the right.)

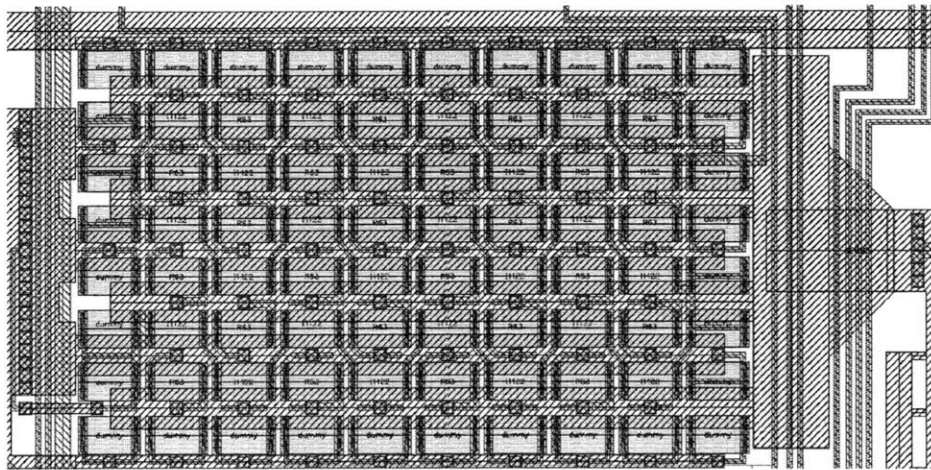


Figure 6-4: Matched Poly Resistors Layout

## 6.4 Metal Options

A metal option is a planned circuit change option that can be easily done only on the metal layer. In most cases, one option only requires a metal change at one spot. Metal options are useful in different aspects. In the engineering phase, a metal option gives the engineer some freedom to trim or modify the silicon after fabrication. In the production phase, different versions of a product are usually a few metal options different from each other. Unlike the fuse trimming, metal options are done on the wafer, and are not accessible after packaging.

There are two types of metal options used in this part: a metal cut and a metal smear (Figure 6-5). A metal cut option is a minimum width metal interconnection on the very top layer, which can be cut later with a probe needle. A metal smear, as contrast, is made of two big blocks of top layer metal with minimum separation. Because the cut or smear operation may stress the part, no sensitive devices are placed under the metal options.

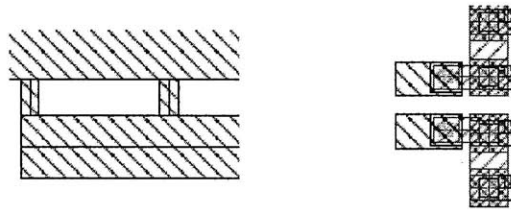


Figure 6-5: Metal Cut (Left) and Metal Smear (Right)

## 6.5 Ground and VDD Routing

Similar to the PCB design, a star connection is preferable for ground and VDD routing. However, given other constraints, a star connection is not always feasible. For layout simplicity, a wide ground ring with two layers of metal in parallel is used as the ground backbone, and every block taps off the ring, as shown in Figure 6-6. The ring breaks in the middle into two halves. The left half is for the analog ground, and the right half is for the power ground. The resistance of the ring is very low.

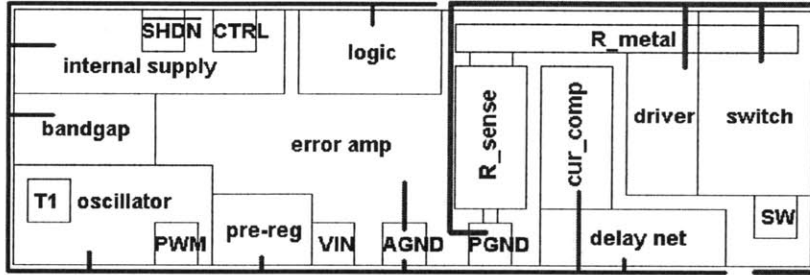


Figure 6-6: Ground Routing

Even if the logic circuit dumps a few milliamps of current on the AGND backbone, the ground voltage at the bandgap is still less than 1mV.

The VDD routing is closer to a star connection. (Figure 6-7) However, the VDD routes are made of narrower metal, which is more resistive.

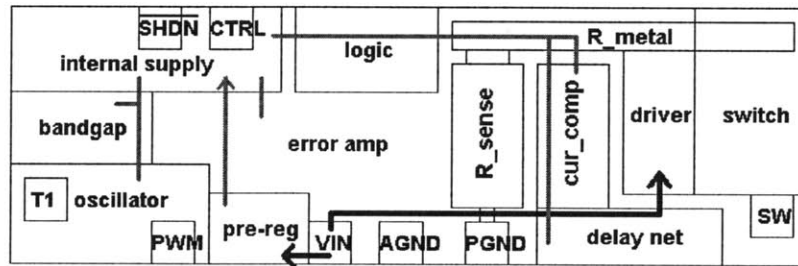


Figure 6-7: VDD Routing

## 6.6 Final Layout

A brief image of the final layout is shown in Figure 6-8. In the end, the actual die area is 80mil\*27mil.

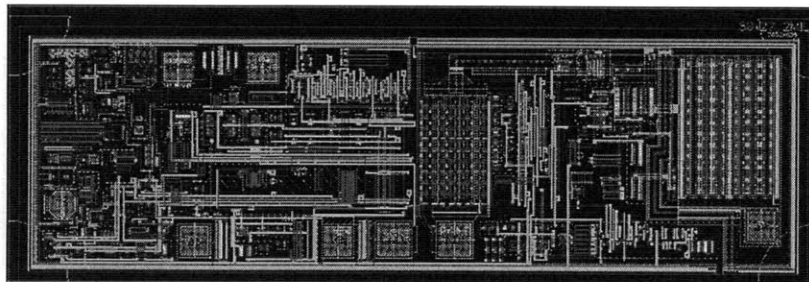


Figure 6-8: Final Layout

On September 16, 2008, a tape-out form was signed. The design work was finished. It was not relaxing period of time. The following six weeks were full of worries and anxieties, while the silicon was being fabricated.

# Chapter 7

## Board Level Testing

This chapter describes the design of the evaluation circuit, followed by the test results of the chip. The accuracy and stability of the chip are also examined under various operation conditions, including extreme inputs and temperature corners. Issues found in the experiments are also reported at the end of this chapter.

### 7.1 Evaluation Circuit Design

The evaluation circuit was designed during the fabrication period. As shown in Figure 7-1, it is similar to the typical application circuit shown in Figure 2-3. The supply voltage for the LED string, V1, is able to go up to 70V, depending on the number of LEDs in series. The input of the part, V2, can be any voltage between 4V and 36V.

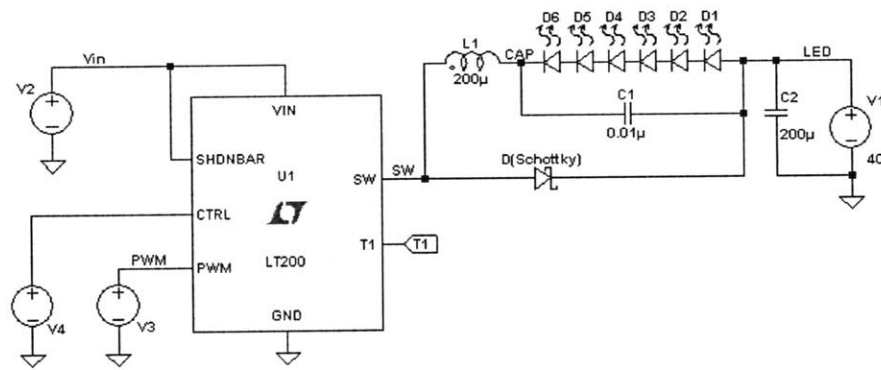


Figure 7-1: Evaluation Circuit Schematic

A square wave function generator, V3, is connected to the PWM input. It generates a 0-5V PWM signal at 100Hz, with a variable duty cycle from 1:1000 to 1. An adjustable voltage source, from 0 to 2V, is connected to the CTRL pin for the analog dimming.

## 7.2 Board Level Simulation

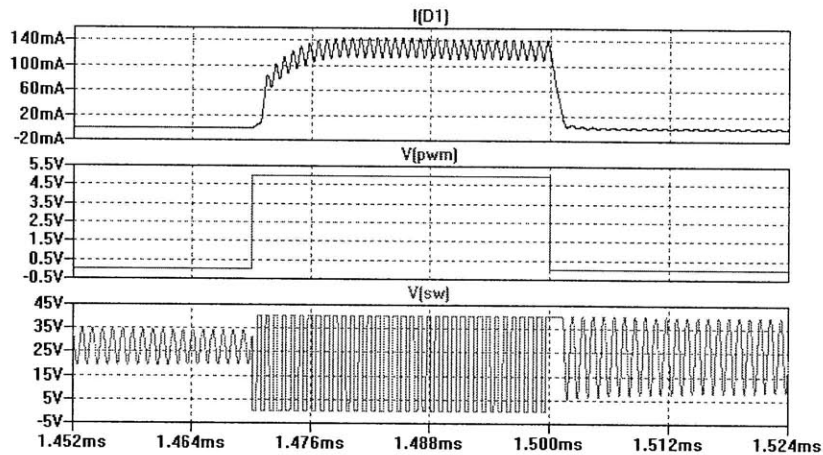


Figure 7-2: Simulation: Output Current at PWM Rising Edge

This evaluation circuit was verified by simulation at both the block behavior level and the transistor level. MATLAB and LTSpice were used for the simulation. One of the simulation results is shown in Figure 7-2. The output LED current,  $I(D1)$ , is shown on the top, followed by the PWM input signal in the middle. The switch node voltage,  $V(sw)$  is at the bottom.

Notice that the on-state output current, ( $I(D1)$  in Figure 7-2), was higher than the set value, 100mA. There were two reasons for this: First, the output current was intentionally designed to be slightly higher than needed, because it was easier to reduce the output current during the trimming procedure than to increase it. Second, at the rising edge of the PWM signal, the output current did not catch up immediately, decreasing the average output current. The global feedback loop tried to fix this error by increasing the on-state current.

## 7.3 Copper Board Design

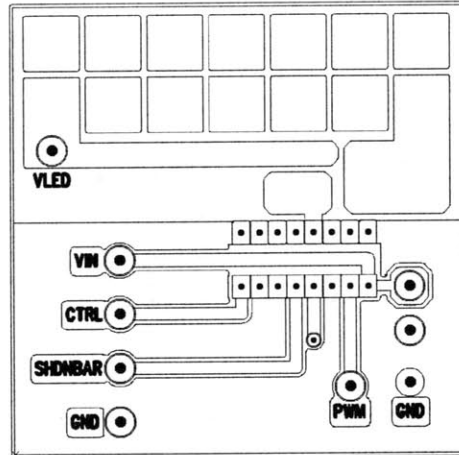


Figure 7-3: Evaluation Board Layout

A copper board was designed for the experiment. As shown in Figure 7-3, it could fit 12 LEDs in series. The switch node area (the small piece of copper connected to the fifth pin in the top row) was minimized to reduce the parasitic capacitance. A photo of the complete evaluation board is shown in Figure 7-4.

## 7.4 Experimental Results

### 7.4.1 Out of the Box

On October 30, 2008, the first silicon was received. After a busy day of setting up a test bench, the LEDs shone, with tears of excitement. The first photo of a working board was taken on October 31, shown in Figure 7-4.

The first oscilloscope screenshot is shown in Figure 7-5. The output current was on channel 1; the PWM input voltage was on channel 3; the switch node voltage was on channel 4. Comparing the first oscilloscope screenshot in Figure 7-5 to the simulation result in Figure 7-2, one can easily see the similarities.

With an increased duty cycle and the switching details, the second screenshot is shown in Figure 7-6. Notice that with a larger duty cycle, the on-state output current is lowered to near 100mA, because the error at the PWM rising edge is insignificant.

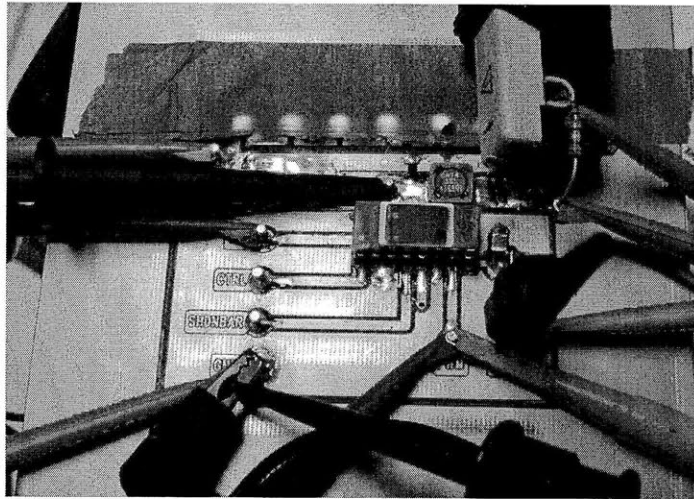


Figure 7-4: Working Evaluation Board

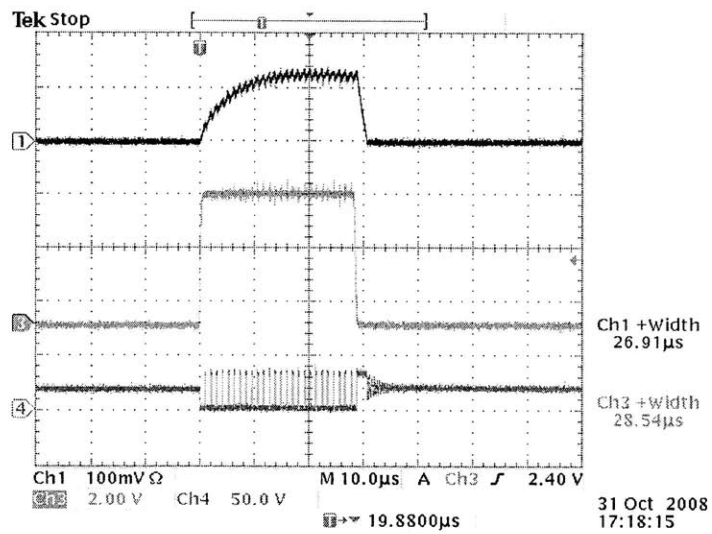


Figure 7-5: First Screenshot: Output Current at PWM Rising Edge

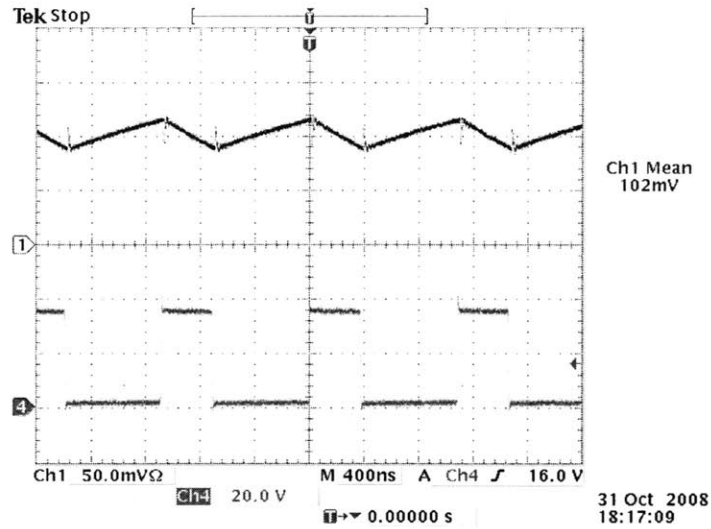


Figure 7-6: Second Screenshot: Output Current and Switch Voltage

## 7.4.2 PWM Dimming Linearity

At various PWM duty cycles, the average output current was measured. The data demonstrated perfect linearity. (Figure 7-7)

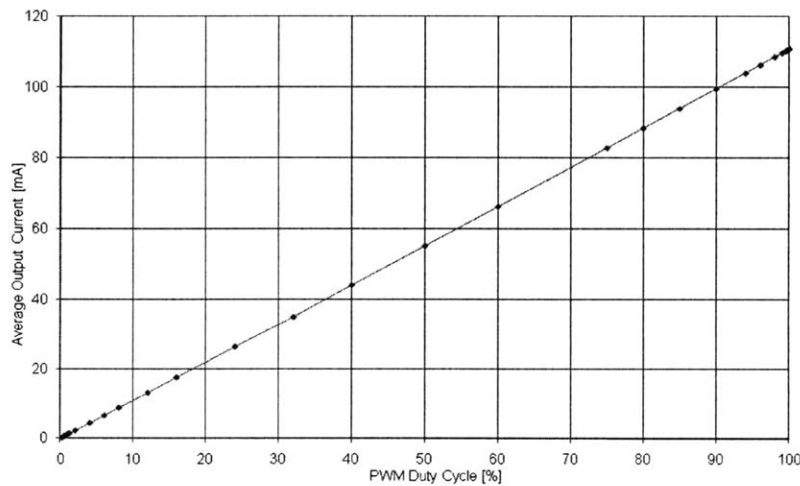


Figure 7-7: PWM Dimming Linearity

The linearity might degrade at low duty cycles, due to the finite rise time of the output current (as explained in Section 7.2). However, even at very low duty cycles (2% or less), the PWM dimming still had good linearity. As shown in Figure 7-8, the maximum error was smaller than 0.02%. Therefore, 1000:1 PWM dimming ratio was

achieved.

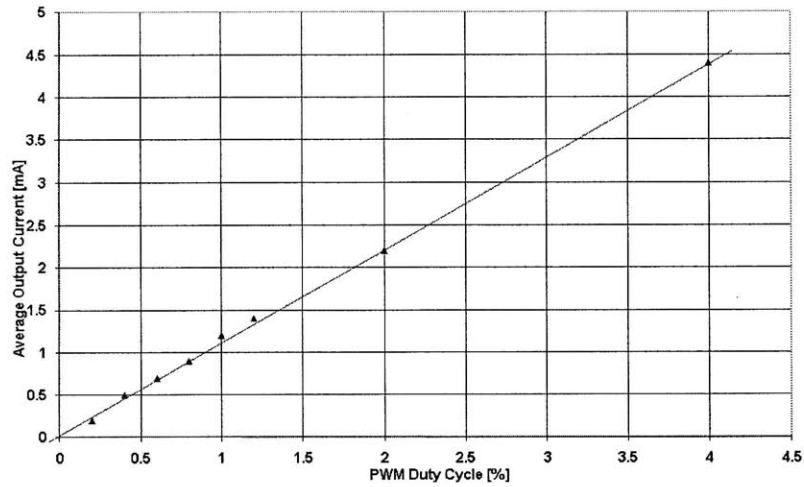


Figure 7-8: PWM Dimming Linearity (at Low Duty Cycle)

### 7.4.3 Analog Dimming Linearity

The analog dimming linearity was also examined by measuring the average output current at different CTRL pin voltages, as shown in Figure 7-9. It showed good linearity as well, when the part operated in the continuous conducting mode and when the CTRL pin voltage was not close to the bandgap voltage.

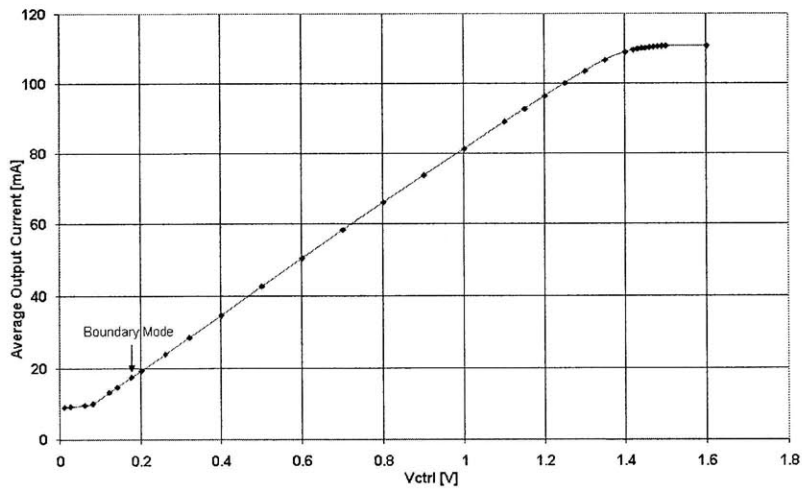


Figure 7-9: Analog Dimming Linearity

### 7.4.4 Power Supply Rejection

With six LEDs at the load, the part regulated its output current with inputs from 23V to 55V, as shown in Figure 7-10. The regulation failed when the maximum duty cycle was reached.

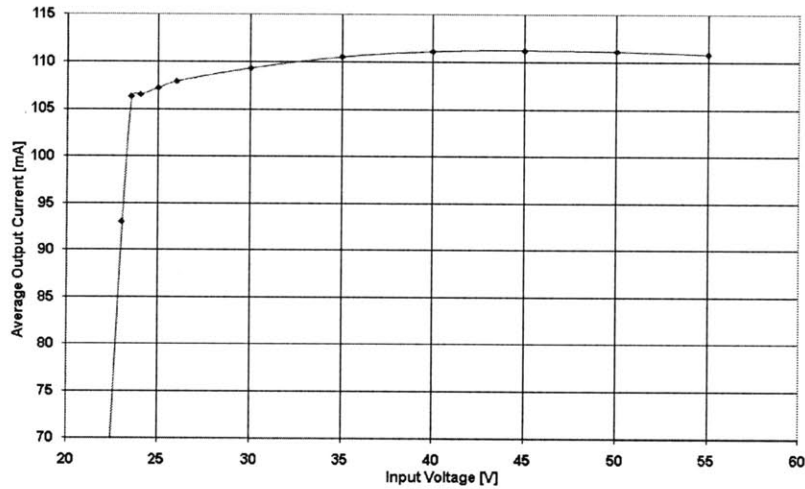


Figure 7-10: Power Supply Rejection

With two LEDs at the load, the part operated at a wider duty cycle range. (Figure 7-11) Besides the maximum duty cycle limit at the input voltage of 8V, the minimum duty cycle limit also occurred at the input voltage of 36V.

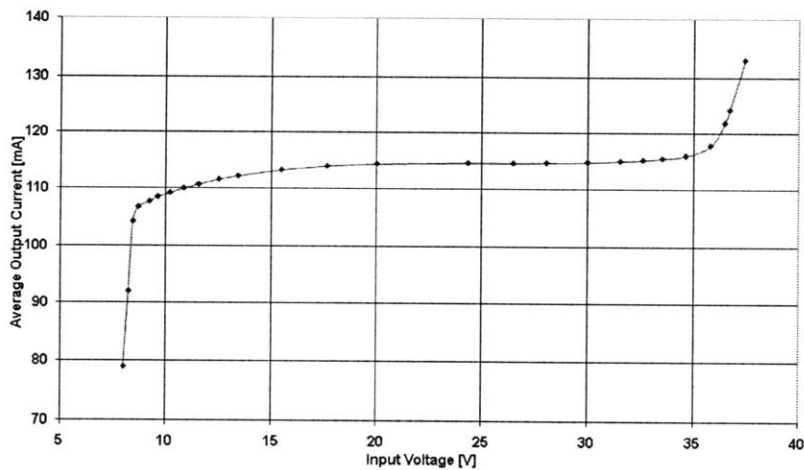


Figure 7-11: Power Supply Rejection (at Low Vout)

## 7.5 Metal Trimming

### 7.5.1 Bandgap Trimming

The bandgap trimming option was designed to reduce the temperature dependence of the output current. Before any trimming was done, the full output current was measured at different temperatures, as shown in Figure 7-12.

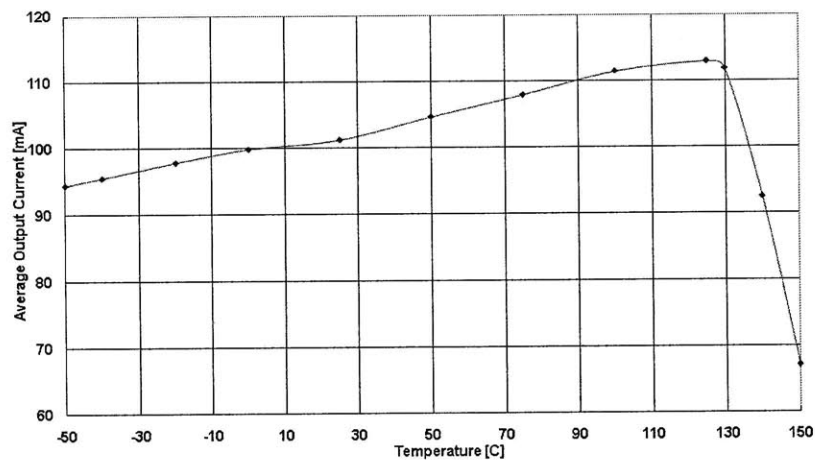


Figure 7-12: Temperature Coefficient

The measurements showed that the part had a positive temperature coefficient, at about  $0.1\%/^{\circ}\text{C}$ . A zener diode was shorted out in the bandgap circuit. The PTAT component in the bandgap was therefore reduced, and the total temperature coefficient was decreased. As shown in Figure 7-13, the output current was much flatter over temperature.

This method worked out well for a few chips. However, it is not practical for real production, because it requires a temperature cycle for every chip. In production, one suggested method is to use the “magical voltage” of the bandgap reference. Since the bandgap temperature coefficient is related to its voltage, the bandgap voltage can be trimmed to a proper value, based on the temperature coefficient data from a small group of chips.

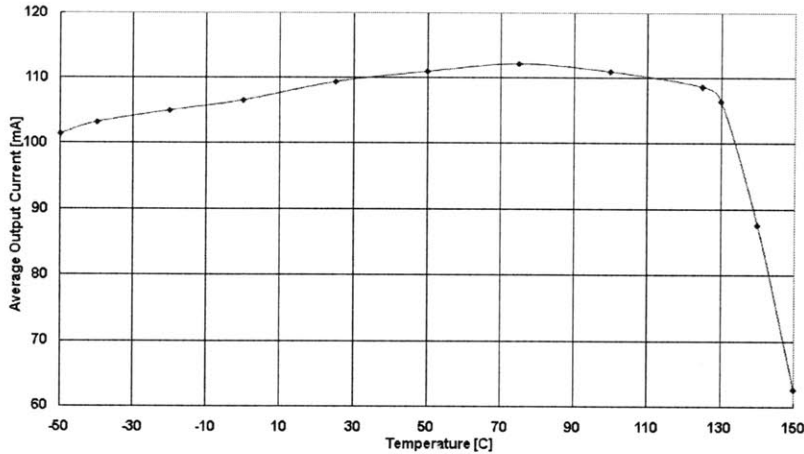


Figure 7-13: Temperature Coefficient After Trimming

### 7.5.2 Absolute Output Current Trimming

The absolute output current was trimmed at last, by cutting-in a few small poly or thin film resistors. The poly and thin film resistors had opposite temperature coefficients, and the number of poly resistors and thin film ones was matched, so that the overall temperature coefficient was unchanged. After cutting a few metal options, the output current was reduced to  $100 \pm 3mA$ .

This trim does not exist in production. Once the proper combination of metal options is found, the metal layer is edited, and the options become final before production.

### 7.5.3 Delay Trimming

As discussed in Section 4.2, the matched delay network also needs to be trimmed. The measurements, shown in Figure 7-14 and 7-15, lead to the conclusion that the sampling circuit overestimated the output current, and the matched delay was too long.

However, there were still some discrepancies in the measurements. For example, the estimation error should decrease when the duty cycle increased, and it should converge when the duty cycle was large. However, in Figure 7-15, the output current decreased even faster when the duty cycle was larger. This trend occurred before the

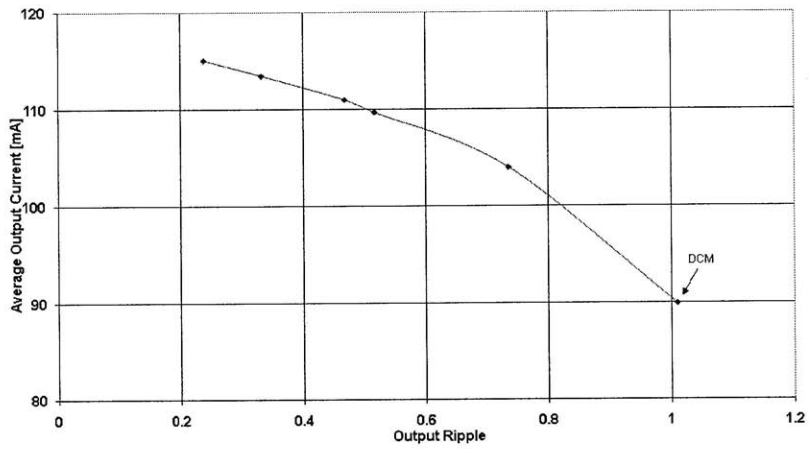


Figure 7-14: Output Accuracy v.s. Inductor Current Ripple, ( $D=30\%$ )

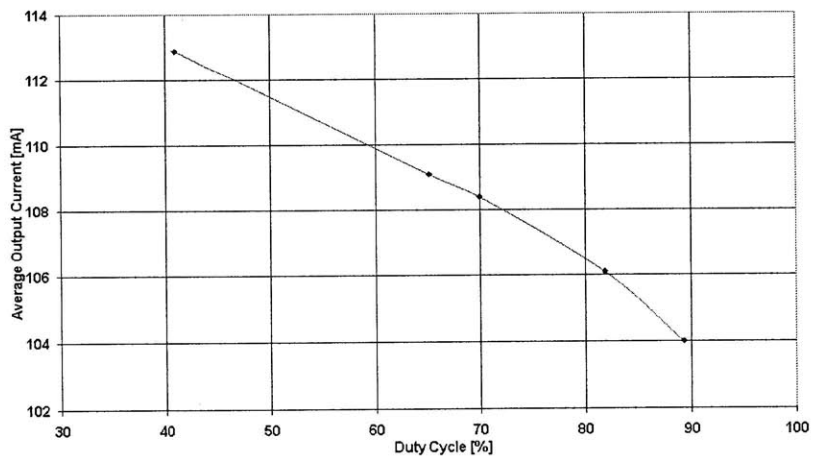


Figure 7-15: Output Accuracy v.s. Duty Cycle (Ripple=30%)

duty cycle reached its maximum limit. More investigation was needed to get a better understanding of the matched delay network.

## 7.6 Known Issues

### 7.6.1 Bipolar Logic Saturation

As shown in Figure 7-16, the duty cycle could not go below 22%. For stability reasons, there was a designed minimum on-time of about 100ns, which corresponded to a minimum duty cycle of 10%. The additional 120ns of delay was unexpected.

The additional delay was due to the saturation of a bipolar inverter in the current comparator. As shown in Figure 5-4, when the current blanking was on, Q2 was turned off completely. All the bias current in BIAS2 went to the base of Q3, pushing it into hard saturation. After the current blanking went off, it took Q3 more than 100ns to recover from saturation. Thereby, the minimum on-time was increased by more than 100ns.

This issue can be patched by decreasing the current blanking time.

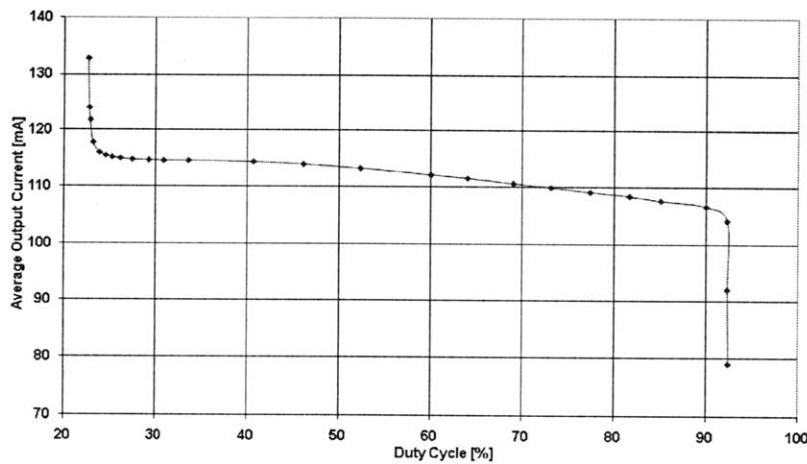


Figure 7-16: Duty Cycle Limits

## 7.6.2 Maximum Duty Cycle Limit

If the saturation issue stated above was considered as a circuit design error, this problem was a system architecture mistake. This design is based on a previous boost converter design, and the minimum off-time (or maximum duty cycle) is necessary for a boost converter. As shown Figure 7-16, the maximum duty cycle of this part is about 92%.

However, for a buck mode regulator, the maximum duty cycle limit is completely unnecessary. When the input voltage is low, the switch turns on forever without any issue.

At the rising edge of the PWM signal (Figure 7-5), if the duty cycle is allowed to go to 100%, the output current ramps up faster. Simulation results showed that the PWM linearity was further improved in that case.

## 7.7 Summary of Specifications

Parameter	Condition	Min	Typ	Max	Unit
Input Voltage	-	4		70	V
Chip Supply Voltage	-	4	5	36	V
Output Current	Fully on, untrimmed	90	105	120	mA
Output Current	Fully on, trimmed	100	105	110	mA
PWM Dimming Accuracy	-		0.1		%
Analog Dimming Linearity	-		3		%
Efficiency	$V_{IN}=40V, V_{OUT}=25V$		84		%
Bias Current	$V_{IN}=5V, PWM=0$		4		mA
Switching Frequency	-	0.8	1.0	1.2	MHz
Switch Current Limit	-		150		mA
Switch $V_{CESAT}$	-		400		mV
Switch Leakage Current	$V_{SW}=50V$		1		uA
Minimum Duty Cycle	-		22		%
Maximum Duty Cycle	-		92		%
$V_{CTRL}$ for Full LED Current	-	1.15	1.25	1.35	V
$V_{CTRL}$ to Shutdown IC	-	0.55	0.65	0.75	V
Operation Temperature	-	-40	25	125	°C

Table 7.1: Summary of Specifications

# Chapter 8

## Conclusion and Future Work

This chapter summarizes the project, and discusses possible improvements for the next version. It then presents the challenges and considerations of the ultimate goal of the project, a multi-channel LED driver that can drive more than 150 LEDs in 16 channels.

### 8.1 Conclusion

This thesis investigates the design and implementation of a single-pin LED driver used in wide screen displays. Since a large number of LEDs with uniform brightness are used as the back lights, this thesis focuses on the pin count and the accuracy. Simulation results and experimental data show that the low-side current sampling scheme is able to work with the least number of pins with acceptable accuracy. This is a good result for display makers with the increasing size of screens. With the PWM dimming function, part of the display can be dimmed, with the color unchanged, to achieve higher contrast rate.

### 8.2 What If Doing It Again

In the design, besides the issues discussed in Section 7.6, there are a few places that may be improved in some aspects.

### 8.2.1 Matched Poly Resistors

The size of the matched poly resistors can be reduced by a factor of two to three, limited by the maximum current density of the resistors and metal connections. The poly resistor matching is better than expected. The measured ratio was 574:1, while the theoretical value is 576:1.

### 8.2.2 Error Amplifier Gain

The error amplifier is a one-stage op-amp. The DC gain of the op-amp is about 200. That is to say, with 1V output, the differential input voltage is 5mV, which accounts 5% of absolute error. Fortunately, the absolute error can be trimmed out later. But the differential input voltage varies when the output changes, that is, when the peak inductor current changes. This implies that the output current may change when current ripple (or inductor) changes.

It is easy to eliminate this trouble. Since the loop is dominant pole compensated, simply adding another stage of gain should increase the DC gain to at least 3000. In that case, none of the issues will remain.

### 8.2.3 Beta Correction

Another error source is the finite beta of the power switch (NPN). While sensing the emitter current in the switch, the output LED current is equal to the average of the collector current. The DC beta of the switch is designed to be near 50 in normal conditions. Therefore, it's a 2% absolute error, which can also be trimmed out. However, since the beta varies a lot over process and temperature corners, it may cause run-to-run errors and thermal reliability issues.

One way to eliminate this error is to put a third matched poly resistor in series with the base of the switch, and subtract the base current from the emitter current to get a better estimation of the output current.

## 8.3 Going Multi-channel

The final version of this chip will have 16 (or more) output channels, with a serial communication port for the PWM dimming function. Each channel can still drive at least 12 LEDs in series, so overall this chip alone can drive more than 150 LEDs.

There will be only one central oscillator, and the 16 switches will be synchronized. This can significantly reduce the cross-coupled switching noise. The PWM signals will be generated on chip, and they will be synchronized to the oscillator as well.

The efficiency has to be very high due to thermal reasons. Assuming a forward drop of 3.3V for a white LED, 150 LEDs running at 100mA each will consume 50W. Under the high voltage operation conditions, the energy loss on the chip can be designed 2% or less. Even in that case, the heat generated on the chip is still 1W, which is close to the limit that can be dissipated without using a heat sink.



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