A Multi-scale Model for Copper Dishing in Chemical-Mechanical Polishing

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***Abstract*—The present success in the manufacture of multi-layer interconnects in ultra-large-scale integration is largely due to the acceptable planarization capabilities of the chemical-mechanical polishing (CMP) process. In the past decade, copper has emerged as the preferred interconnect material. The greatest challenge in Cu CMP at present is the control of wafer surface non-uniformity at various scales. As the size of a wafer has increased to 300 mm, the wafer-level non-uniformity has assumed critical importance. Moreover, the pattern geometry in each die has become quite complex due to a wide range of feature sizes and multi-level structures. Therefore, it is important to develop a non-uniformity model that integrates wafer-, die- and feature-level variations into a unified, multi-scale dielectric erosion and Cu dishing model. In this paper, a systematic way of characterizing and modeling dishing in the single-step Cu CMP process is presented. The possible causes of dishing at each scale are identified in terms of several geometric and process parameters. The feature-scale pressure calculation based on the step-height at each polishing stage is introduced. The dishing model is based on pad elastic deformation and the evolving pattern geometry, and is integrated with the wafer- and die-level variations. Experimental and analytical means of determining the model parameters are outlined and the model is validated by polishing experiments on patterned wafers. Finally, practical approaches for minimizing Cu dishing are suggested.**

***Index Terms*— Chemical mechanical polishing, Cu dishing, Semiconductor manufacturing.**

I. Introduction

THE relentless advances in ultra-large-scale integration technology necessitate the design and fabrication of sub-micron features of higher resolution, denser packing, and multi-layer interconnects. The present success in satisfying the stringent specifications is largely due to the acceptable local and global planarization capabilities of the chemical-mechanical polishing (CMP) process.

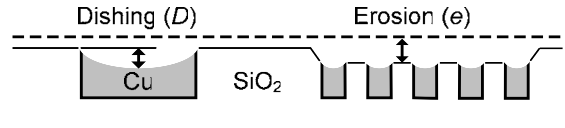

Fig. 1. Schematics of a surface profile after CMP in a single-layer Cu interconnect structure.

In the past decade, copper has emerged as the preferred interconnect material. Interconnect Cu lines are produced by a multi-level damascene scheme, comprising dielectric trench patterning and Cu deposition, followed by CMP. The greatest challenge in Cu CMP at present is the control of wafer surface non-uniformity at various scales, primarily due to dielectric erosion and Cu dishing as shown in Fig. 1. Generally, dielectric erosion is more prevalent than Cu dishing in the dense sub-micron, copper-line region, whereas dishing is far more significant than erosion at the global wiring level [1].

As the wafer size has increased to 300mm and the pattern geometry of a die has become complex, due to a wide range of feature sizes, the importance of a multi-scale non-uniformity model, too, has increased. Such a model should integrate wafer-, die- and feature-level variations in dielectric erosion and Cu dishing. Past efforts to characterize relations among non-uniformity and process parameters have been primarily confined to extensive experimental investigations [2]-[6]. Several semi-theoretical models are available, but such models essentially address the effect of one variable at a time and are confined only to the feature-level or at most the die-level [3], [7]-[12].

In this paper, accordingly, a Cu dishing model is presented based on feature-level step-height evolution. The local pressure distribution is determined in each polishing stage in terms of the evolving step-height and pattern geometry. The contact pressure at a given step height is calculated from the elastic deformation of the pad due to the applied pressure. The pad is assumed to deform as discrete, uniaxially loaded blocks. Additionally, wafer- and die-level surface non-uniformities are clearly defined, and the possible causes of non-uniformities at each level are identified in terms of the geometric and process parameters. Moreover, a multi-scale Cu dishing model is

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introduced by integrating these parameters with the feature-level dishing model. Experimental and analytical means of determining the model parameters are outlined, and the models are validated by polishing experiments on 100 mm patterned wafers. Finally, possible approaches for minimizing Cu dishing are discussed based on the pattern geometry, model parameters, and process conditions.

II. Definition of Non-uniformities at Various Scales

A. The Preston Equation

The local material removal rate (MRR) in CMP is expressed by the Preston equation [13]:

$$MRR \equiv \left|\frac{dh}{dt}\right| = k_p \cdot p \cdot v_R \tag{1}$$

where h is the thickness of the layer removed, t the polishing time, p the pressure, v_R the relative velocity, and k_p the Preston constant.

Although the Preston equation represents the local material removal rate at any point on the wafer, it does not explain the actual material removal mechanism. There have been many studies to explain the wear mechanism in CMP by investigating contacts among the pad, abrasives, and the wafer surface. Nevertheless, several researchers have experimentally demonstrated that the above functional relation is generally valid in CMP at many scales [14]-[17]. The Preston constant, obviously, is not a fundamental constant. It depends on the pad/wafer contact condition, slurry concentration and chemistry, abrasive size and shape, pad stiffness and surface topography, and so on. Thus, any variation in these quantities at any scale is expected to result in non-uniformity in material removal rate at that scale.

The most challenging part of Cu CMP is that there are at least three different materials, Cu, dielectric and barrier layer, to be polished—sequentially or simultaneously. Therefore, the ratios of material removal rates, or selectivities, become important factors in characterizing non-uniformity. The selectivities of Cu, oxide and barrier layer are obtained by blanket wafer polishing, under the same process or experimental conditions. Since the definition of selectivity is based on blanket wafer experiments, with the same nominal pressure and relative velocity, they are the ratios of Preston constants. Thus, the selectivities in Cu CMP are defined as:

$$S_{Cu/ox} \equiv \frac{MRR_{Cu}}{MRR_{ox}} = \frac{k_{p_{Cu}}}{k_{p_{ox}}},\ S_{b/ox} \equiv \frac{MRR_b}{MRR_{ox}} = \frac{k_{p_b}}{k_{p_{ox}}} \tag{2}$$

where the subscripts *Cu, b, ox*, respectively, represent copper, barrier and oxide.

The selectivity depends both on the hardness of the material polished and the chemistry of the slurry [18]-[20].

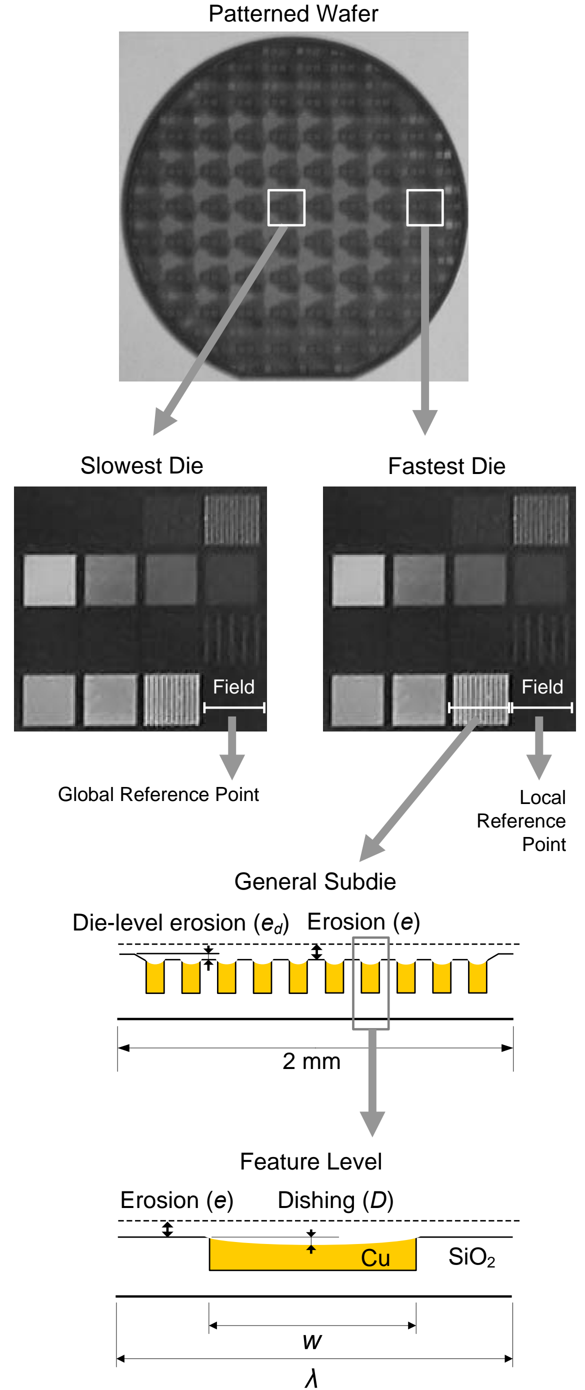


Fig. 2. Definition of non-uniformities at the various levels.

For instance, hydrogen peroxide, a common additive in commercial Cu slurries, reacts with Cu and forms a soft layer so that the material removal rate of Cu increases and thus $S_{Cu/ox}$ too increases.

B. Wafer-level (Inter-Die) Variation

Fig. 2 exemplifies effects of non-uniformity at wafer-, die- and feature-levels. The primary problem in Cu CMP is that the material removal rate across the wafer is nonuniform for various reasons: non-uniform pressure and velocity distributions and even the Preston constant [21]-

[23]. In this paper, we focus on the maximum non-uniformity due to dishing. Thus the wafer-level non-uniformity factor β is defined as the ratio of the material removed at the slowest and the fastest field regions, respectively, in a wafer. As shown in Fig. 2, the edge region of the wafer polishes faster and hence erosion and dishing are the greatest in the outer dies.

The wafer-level non-uniformity factor β is defined as

$$\beta \equiv \frac{\Delta h_{sf}}{\Delta h_{ff}} \quad (0 < \beta \leq 1) \tag{3}$$

where Δh_{sf} and Δh_{ff} are the thicknesses of material removed in the slowest and the fastest field regions, respectively.

In a patterned wafer, it is important to differentiate between the wafer-level non-uniformity and the die-level non-uniformity. The simplest way to do this is to compare a subdie of the same pattern geometry in each die. Neither the fastest nor the slowest region in a die may be a field region. Nevertheless, it is convenient to select a field region in each die as a reference point and ignore the pattern geometry effect as shown in Fig. 3. If $\beta = 1$, there will be only die-level non-uniformity. This means that a subdie at the same relative position in each die on a wafer will have the same non-uniformity. If $\beta < 1$, subdies in each die will have different non-uniformities. Therefore, it is important to consider β for characterizing non-uniformity at both die- and feature-levels.

C. Die-level (Inter-Subdie) Variation

In addition to the wafer-level non-uniformity, there are die-level non-uniformities in each die on the wafer. The die-level variation mainly depends on the pattern geometry and the materials in contact with the pad at each polishing height. To express pattern geometry at die-level of complex chip-style patterns, it is required to define a characteristic area that can be considered as a separate region in a die in terms of an average pressure.

The average pressure in the characteristic area mainly depends on the area fraction, A_f, of Cu in the underlying pattern. This area fraction can be expressed as the ratio of the Cu interconnects area, A_{Cu}, to the total characteristic area, A_{total}.

$$A_f \equiv \frac{A_{Cu}}{A_{total}} \quad (0 \leq A_f \leq 1) \tag{4}$$

If $A_f = 0$, the region is an oxide field region and there are no Cu lines within the area. On the other hand, if $A_f = 1$, the entire area is monolithic Cu.

In this study, each die in a patterned wafer consists of 16 separate subdies with various periodic patterns as shown in Fig. 2, and thus each subdie will be assumed as the characteristic area. Thus, the area fraction A_f of a subdie for linear features may be defined as:

$$A_f = \frac{w}{\lambda} \quad (0 \leq A_f \leq 1) \tag{5}$$

where w is the Cu linewidth and λ the pitch of the underlying pattern geometry in a Cu damascene structure.

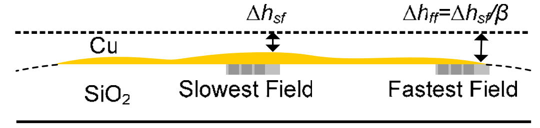


Fig. 3. Definition of wafer-level non-uniformity factor a patterned wafer: Material removal rate ratio of the field region at the slowest die with respect to the field region at the fastest die.

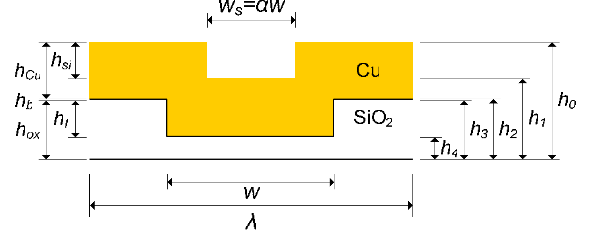


Fig. 4. Definition of pattern geometry in Cu damascene structure, based on the Cu interconnect linewidth, w, pitch, λ and Cu deposition factor α.

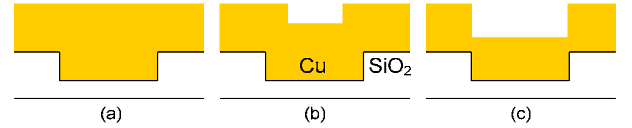


Fig. 5. Effect of Cu deposition factor, α, and initial step-height, h_{si}:(a) α=0 and h_{si}= 0, (b) 0<α<1 and 0<h_{si}<h_I, and (c) α=1 and h_{si}= h_I .

D. Feature-Level Variation

Feature-level pattern geometry is represented by the linewidth and the step height. Due to the different characteristics of the Cu deposition processes, such as physical vapor deposition (PVD) and electroplating, the surface Cu topography is generally different from the underlying trench pattern. The "surface linewidth", w_s, and the initial step height, h_{si}, may be smaller than the underlying Cu linewidth, w and the thickness, h_I, as shown in Fig. 4. The Cu deposition factor α may be defined as:

$$\alpha \equiv \frac{w_s}{w} \quad (0 \leq \alpha \leq 1) \tag{6}$$

Thus, if $\alpha = 0$, the initial Cu surface topography is flat regardless of the underlying pattern geometry as in Fig. 5(a), and if α =1 and h_{si} =1, the initial surface topography is a true replica of the underlying trench pattern as in Fig. 5(c). Additionally, the deposited Cu thickness, h_{Cu}, may also vary depending on the deposition processes. In PVD, h_{Cu} remains the same regardless of the underlying patterns. In electroplating, however, h_{Cu} varies depending on the pattern geometry.

III. Multi-scale Cu Dishing Model

A. Feature-level Pressure Calculation

The material removal rate at any instant is essentially based on the local pressure distribution at each height stage. The local pressure distribution however changes as the surface profile changes due to polishing.

Both the pressure at the high- and low-features, p_h and p_l, generally vary with time, for the polishing rate depends on the pad/abrasives/wafer contact condition. Initially, the pad contacts the top of the wafer surface, which is filled with Cu of certain topography representing the initial area fraction and the initial step-height. The low-feature may or may not support normal load depending on the step-height at any given time. Therefore, it is necessary to determine the relationship between the contact pressure and the step-height to predict the surface profile at any given polishing time. Furthermore, the Preston constant is also different as the material changes from Cu to barrier layer, and from barrier layer to oxide.

B. The Feature-level Step-Height Model

It has been proposed in the past that dishing of Cu lines is due to the elastic deformation of a smooth polishing pad. One approach is to assume that the elastic deformation of the homogeneous, monolithic pad, δ, itself as Cu dishing [3]. This model, however, grossly underestimates dishing. Another approach is to relate the pressure on the Cu interconnect by assuming that the pad deforms as discrete, uniaxially loaded blocks [11], [12]. We adopt this model in the following derivation. In this model, two material structures, Cu and oxide, are assumed as shown in Fig. 6.

The key assumptions of the approach are:

- The pad is an isotropic elastic material.
- The pad surface is perfectly smooth.
- The wafer surface always remains horizontal.
- The pad deforms as separate uniaxially-loaded blocks under the uniform pressure boundary condition.
- The deformation is plane-strain.
- The pad-surface in x-direction is stress-free and does not expand: $\sigma_x = \tau_{xy} = \tau_{xz} = 0$ and $\nu = 0$.
- The bottom of each block remains at the same level and is free to move horizontally.

The step-height, $h_s(t)$, is defined as the height difference between the high- and low-features at any given time, t.

$$h_s(t) \equiv h_h(t) - h_l(t) \tag{7}$$

where h_h and h_l, respectively, are the polishing surface heights of the high- and low-features relative to the bottom of the oxide.

The material removal rates at the high- and low-features can be expressed by the Preston equation as:

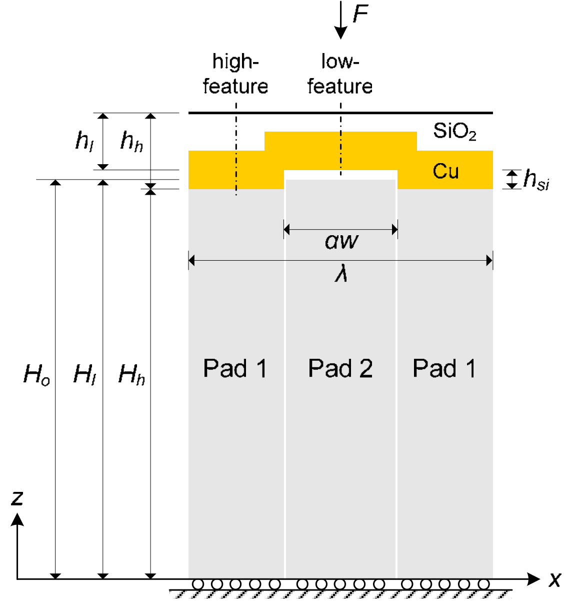


Fig. 6. Schematic of a feature-level elastic block Cu dishing model in Cu CMP.

$$\frac{dh_h}{dt} = -k_{p_h} p_h(t) v_R, \quad \frac{dh_l}{dt} = -k_{p_l} p_l(t) v_R \tag{8}$$

where k_{p_h} and k_{p_h} are the Preston constant, and p_h and p_l are the pressure at the high- and low-features.

1) Stage 1: Initially, i.e., without any load, the pad only contacts the high-feature. When the load is applied, the low-feature may or may not contact the pad, depending on the initial step-height. If the load is sufficiently high to deform the pad at the high-feature more than the initial step-height, then the pad will touch the low-feature. On the contrary, if the load is low, the deformation of the pad at the high-feature is less than the initial step-height, thus the load will be supported by the high-feature-only. In stage 1, we will consider the latter case.

Force equilibrium at the initial contact area requires:

$$p_h(1 - \alpha w / \lambda) + p_l(\alpha w / \lambda) = p_{av} \tag{9}$$

where p_h and p_l are the pressures at the high- and low-feature, respectively. Since only the high-feature contacts the pad, $p_l = 0$. Therefore,

$$p_h = \frac{p_{av}}{1 - \alpha w / \lambda} \tag{10}$$

Since the pad is assumed to deform as separate blocks, the displacements at the high- and low-features can be expressed as:

$$\delta_h \equiv H_o - H_h = \frac{p_h}{E_p} H_o, \ \delta_l = 0 \tag{11}$$

where E_p is the Young's modulus of the pad material, H_o is the undeformed pad thickness. Therefore, the requirement to start with stage 1 can be expressed as:

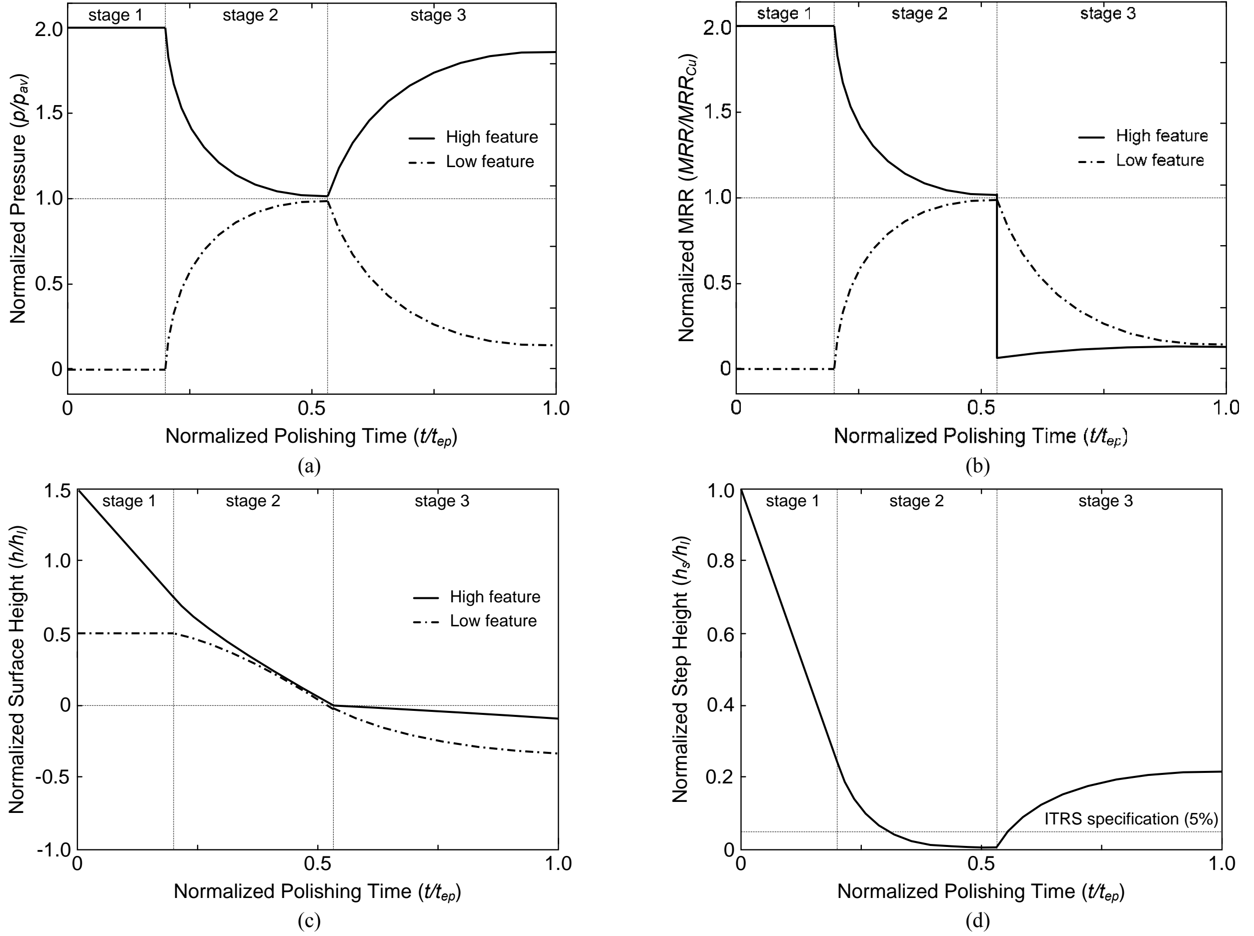


Fig. 7. Time evolution of (a) pressure, (b) material removal rate, (c) polishing surface height and (d) step-height based on the feature-level elastic block dishing model. Selected model parameters are: MRR_{Cu}=484nm/min, MRR_{ox}=34 nm/min, w=100μm, λ=200μm, α=1, β=0.8, E_p=300MPa, p_{av}=28kPa, and H_o=1.3mm.

$$h_{si} > \delta_{h_{\max}} = \frac{H_o}{1 - \alpha w / \lambda}\left(\frac{p_{av}}{E_p}\right) \tag{12}$$

where h_{si} is the initial step-height for each pattern.

Now, material removal rates at the high- and low-feature are expressed by the Preston equation as:

$$\frac{dh_h}{dt} = -k_{p_h}\left(\frac{p_{av}}{1 - \alpha w / \lambda}\right)v_R$$
$$\frac{dh_l}{dt} = 0 \tag{13}$$
$$\frac{dh_s}{dt} = \frac{dh_h}{dt} - \frac{dh_l}{dt} = -k_{p_h}\left(\frac{p_{av}}{1 - \alpha w / \lambda}\right)v_R$$

The step-height can be solved with the initial condition $h_s(0) = h_{si}$.

$$h_s(t) = h_{si} - k_{p_h}\left(\frac{p_{av}}{1 - \alpha w / \lambda}\right)v_R \cdot t \tag{14}$$

The end of stage 1, t_1, is defined as when h_s reaches the pad deformation $\delta_{h_{\max}}$, $h_s(t_1) = \delta_{h_{\max}}$, and the low-feature, too, starts supporting the normal load. Thus,

$$t_1 = \frac{h_{si} - \delta_{h_{\max}}}{k_{p_h}\left(\frac{p_{av}}{1 - \alpha w / \lambda}\right)v_R} \tag{15}$$

Thus, for $0 < t < t_1$, the normal load is supported by the high-feature only, and the pressure and material removal rate at the high-feature are constant. The step-height decreases linearly with time and the low-feature remains unpolished as shown in Fig. 7.

2) Stage 2: As the pad contacts low features, too, they get polished. This is designated as stage 2. The material being polished at both high- and low-features in this stage is Cu. The end of stage 2 is marked by the polishing time, t_2, when the pad surface at high-feature reaches the oxide surface.

Deformations of the pad at the high- and the low-features in this stage can be expressed as:

$$H_o - H_h(t) = \frac{H_o}{E_p}\,p_h(t),\;\; H_o - H_l(t) = \frac{H_o}{E_p}\,p_l(t) \tag{16}$$

where H_h and H_l are the deformed pad thicknesses at the high- and low-features, respectively.

Since both the high- and low-feature are in contact with the pad, the step-height can be expressed by thickness difference of the high- and low-features, and the pressure difference as:

$$h_s(t) = h_h(t) - h_l(t) = H_l(t) - H_h(t) \tag{17}$$

and

$$p_h(t) - p_l(t) = \frac{E_p}{H_o} h_s(t) \tag{18}$$

By combining (18) with the force equilibrium in (9), the pressure and the material removal rate at the high- and low-features at any given time t can be expressed as a function of the step-height :

$$\begin{aligned} p_h(t) &= p_{av} + (\alpha w/\lambda)\frac{E_p}{H_o} h_s(t) \\ p_l(t) &= p_{av} - (1-\alpha w/\lambda)\frac{E_p}{H_o} h_s(t) \end{aligned} \tag{19}$$

$$\begin{aligned} \frac{dh_h}{dt} &= -k_{p_h}\left[p_{av} + (\alpha w/\lambda)\frac{E_p}{H_o} h_s(t)\right]v_R \\ \frac{dh_l}{dt} &= -k_{p_l}\left[p_{av} - (1-\alpha w/\lambda)\frac{E_p}{H_o} h_s(t)\right]v_R \end{aligned} \tag{20}$$

The step-height, h_s, is expressed by the first-order ordinary differential equation (ODE) as:

$$\begin{aligned} &\frac{dh_s}{dt} + \left\{\left[(1-\alpha w/\lambda)k_{p_l} + (\alpha w/\lambda)k_{p_h}\right]\frac{E_p v_R}{H_o}\right\}h_s \\ &\quad = \left[k_{p_l} - k_{p_h}\right]p_{av}v_R \end{aligned} \tag{21}$$

In this stage, the material being polished at the high- and low-feature in the fastest die are the same, i.e. Cu: $k_{p_h} = k_{p_l} = k_{p_{Cu}}/\beta$. Thus, equation (21) is rewritten as:

$$\frac{dh_s}{dt} + \left(\frac{k_{p_{Cu}}E_p v_R}{\beta H_o}\right)h_s = 0 \tag{22}$$

At the onset of stage 2, $t = t_1$, the low-feature barely contacts the pad: $h_s(t_1) = \delta_{h_{\max}}$. Therefore, the general solution for step-height in stage 2, $t_1 < t < t_2$, is expressed as:

$$h_s(t) = h_s(t_1)exp\left(-\frac{t-t_1}{\tau_1}\right),\ \tau_1 = \frac{\beta H_o}{k_{p_{Cu}}E_p v_R} \tag{23}$$

Stage 2 ends when the pad reaches the top of oxide at the high feature, the general solution for t_2 can be solved by the condition: $h_h(t_2) = h_h(0) - h_{Cu}$.

The step-height when $t = t_2$ represents the minimum dishing due to the initial surface topography, and is written as:

$$h_s(t_2) = h_s(t_1)exp\left(-\frac{t_2-t_1}{\tau_1}\right) \tag{24}$$

Therefore, for $t_1 < t < t_2$, the normal load is supported by both high- and low-features, and the pressure and material removal rates at the high- and low-features depend on the step-height. The polishing surface at high-feature decreases faster than that at low-feature, and thus the step height gradually decreases. The step-height at the end of stage 2, $h_s(t_2)$, is given by the ratio of the polishing interval $t_2 - t_1$ to the time constant τ_1. For example, if $(t_2 - t_1)/\tau_1 > 4$, $h_s(t_2)$ is less than 2% of the maximum pad deformation, $\delta_{h_{\max}}$.

3) Stage 3: As the polishing surface at the high-feature reaches the top of oxide, the step-height by definition is Cu dishing. In this stage, the materials being polished at the high- and low-feature are oxide and Cu, respectively: $k_{p_h} = k_{p_{ox}}/\beta$ and $k_{p_l} = k_{p_{Cu}}/\beta$. Furthermore, the linewidth is changed to the designed Cu linewidth, w, instead of αw. Thus, the force equilibrium at the contact area can be rewritten as:

$$p_h(1-w/\lambda) + p_l(w/\lambda) = p_{av} \tag{25}$$

The pressure and the material removal rate in the oxide and Cu regions in stage 3 can be represented by the step-height as in (19) and (20). By writing (21) with the condition that when $t = t_2$, $h_s = h_s(t_2)$, the step-height when $t > t_2$, can be solved as:

$$h_s(t) = h_s(t_2) + [h_o - h_s(t_2)]\left\{1 - exp\left[-\left(\frac{t-t_2}{\tau_2}\right)\right]\right\} \tag{26}$$

$$h_s(t_2) = \left(\frac{1}{1-\alpha w/\lambda}\right)\left(\frac{p_{av}}{E_p}\right)H_o exp\left(-\frac{t_2-t_1}{\tau_1}\right) \tag{27}$$

$$h_o \equiv \left[\frac{S_{Cu/ox}-1}{(1-w/\lambda)S_{Cu/ox}+w/\lambda}\right]\left(\frac{p_{av}}{E_p}\right)H_o \tag{28}$$

$$\tau_2 \equiv \left[\frac{S_{Cu/ox}}{(1-w/\lambda)S_{Cu/ox}+w/\lambda}\right]\left(\frac{\beta H_o}{k_{p_{Cu}}E_p v_R}\right) \tag{29}$$

In stage 3, pressure in the oxide region, now the high-feature, is greater than that in the Cu region, low-feature. However, the material removal rate depends on both the Preston constant and pressure. Now the Preston constant ratio or selectivity, $S_{Cu/ox}$, between oxide and Cu comes into consideration. If $S_{Cu/ox} = 1$, the pad sees the oxide and Cu as the same material in terms of polishing, the material removal rate ratio is just that of pressure. Thus, the step-height approaches zero with the same time constant as of stage 2. If the product of the pressure and the Preston constant for Cu is greater than of oxide, Cu polishes faster than the oxide. Thus, the step-height increases with polishing time.

C. Cu Dishing Model

Based on the non-uniformity definition in Fig. 2, the final dielectric erosion, e, and Cu dishing, D, can be expressed as the height at high-feature and the step-height at the process end-point, t_{ep} as:

$$e \equiv h_h(t_2) - h_h(t_{ep}) \tag{30}$$

$$D \equiv h_s(t_{ep}) \tag{31}$$

We focus on Cu dishing in this paper. The dielectric erosion model based on step-height calculation is left for future research. Copper dishing at the endpoint can be expressed by the step-height model as:

$$D = h_s(t_2) + [h_o - h_s(t_2)]\left\{1 - exp\left[-\left(\frac{t_{ep} - t_2}{\tau_2}\right)\right]\right\} \tag{32}$$

Ideally, the endpoint is when the excess Cu at the high-feature is completely removed: $t_{ep} = t_2$. Cu dishing in this case is represented as the initial Cu dishing, D_i:

$$D_i \equiv h_s(t_2) = \left(\frac{1}{1 - \alpha w / \lambda}\right)\left(\frac{p_{av}}{E_p}\right)H_o exp\left(-\frac{t_2 - t_1}{\tau_1}\right) \tag{33}$$

Due to the wafer- and die-level non-uniformites, the true process endpoint is the time when the excess Cu in the field region of the slowest die is completely removed. That is,

$$t_{ep} = \frac{h_{Cu}}{k_{p_{Cu}} p_{av} v_R} \tag{34}$$

Cu dishing approaches an asymptotic value, h_o, as t_{ep} increases. This asymptotic dishing, D_∞, is defined as:

$$D_\infty \equiv h_o = \left[\frac{S_{Cu/ox} - 1}{(1 - w/\lambda)S_{Cu/ox} + w/\lambda}\right]\left(\frac{p_{av}}{E_p}\right)H_o \tag{35}$$

The dimensionless time interval, $t_d^* \equiv (t_{ep} - t_o)/\tau_2$ is an index of how close Cu dishing is to D_∞. For example, if $t_d^* > 4$, the Cu dishing, D approaches to D_∞ within 2%. Cu dishing D, D_i and D_∞ are expressed in dimensionless form D^*, D_i^* and D_∞^*, the ratio between dishing and the nominal Cu interconnect thickness, h_I.

$$D^* \equiv \frac{D}{h_I},\; D_i^* \equiv \frac{D_i}{h_I},\; D_\infty^* \equiv \frac{D_\infty}{h_I} \tag{36}$$

Therefore, Cu dishing in (32) is represented in dimensionless form as:

$$D^* = D_i^* + \left(D_\infty^* - D_i^*\right)\left[1 - exp\left(-t_d^*\right)\right] \tag{37}$$

IV. Parameter Sensitivity Analysis

The present model shows that Cu dishing is strongly dependent upon a large number of geometrical and process parameters, as shown in Fig. 8. To decrease Cu dishing, all the three terms, D_i^*, D_∞^* and t_d^* need to be reduced.

First, the selectivity between Cu and oxide should be decreased to reduce D_∞^* so that the total dishing becomes less time-sensitive as shown in Fig. 8(a). If $S_{Cu/ox} = 1$, material removal rates in the Cu and oxide regions are the same, which means that the pad sees this region as a field region in so far as material removal rate is concerned. Therefore, there is no dishing developed: $D_\infty^* = 0$ thus, $D^* = D_i^*$. From an earlier erosion model and the present dishing model, however, the role of slurry selectivity on the non-uniformity seems to be contradictory. High selectivity minimizes dielectric erosion, whereas low selectivity minimizes Cu dishing. Therefore, it is hard to find an optimum selectivity that minimizes both erosion and dishing in single-step polishing.

Second, D^* decreases as p_{av}/E_p decreases as shown in Fig. 8(b). Thus, to decrease dishing, one may use either a stiff pad or low-pressure polishing, or both. Furthermore, as the pad thickness, H_o, is decreased, Cu dishing, too, is decreased. However, the extent to which the pad thickness can be decreased is limited by the yield strength of the pad, σ_Y, by:

$$H_o > \frac{E_p}{\sigma_Y}\delta_{h_{\max}} \tag{38}$$

Third, the wafer-level non-uniformity factor β affects Cu dishing. Cu dishing decreases as β increases as shown in Fig. 8(c). To eliminate the wafer-level non-uniformity, β should be unity. This is more difficult as the size of wafer increases, for the slurry is fed from the outside of wafer.

Moreover, even though the wafer-level non-uniformity is minimum, i.e., β =1, there could be still Cu dishing in each subdie if $\alpha > 0$. This means that even if the field regions in all dies polish uniformly, Cu dishing can still develop due to the die-level variations of initial the topography. But if $\alpha = 0$ and $\beta = 1$, then the total dishing time becomes zero and there is no dishing across the wafer: $t_d^* = 0$ and thus $D^* = 0$ as shown in Fig. 8(d). Therefore, dishing can be minimized by arranging $\alpha = 0$ and β =1, independent of slurry selectivity.

V. Experimental Validation

A Cu damascene structure was designed and fabricated to investigate the effects of the various parameters on wafer-, die- and pattern-level erosion and dishing. The 100 mm wafer comprised 60 dies, and each die in turn had 16 subdies. Fig. 9 shows the pattern layout in a die.

The interconnect deposition factor α for several patterns was obtained by profilometetry and Scanning

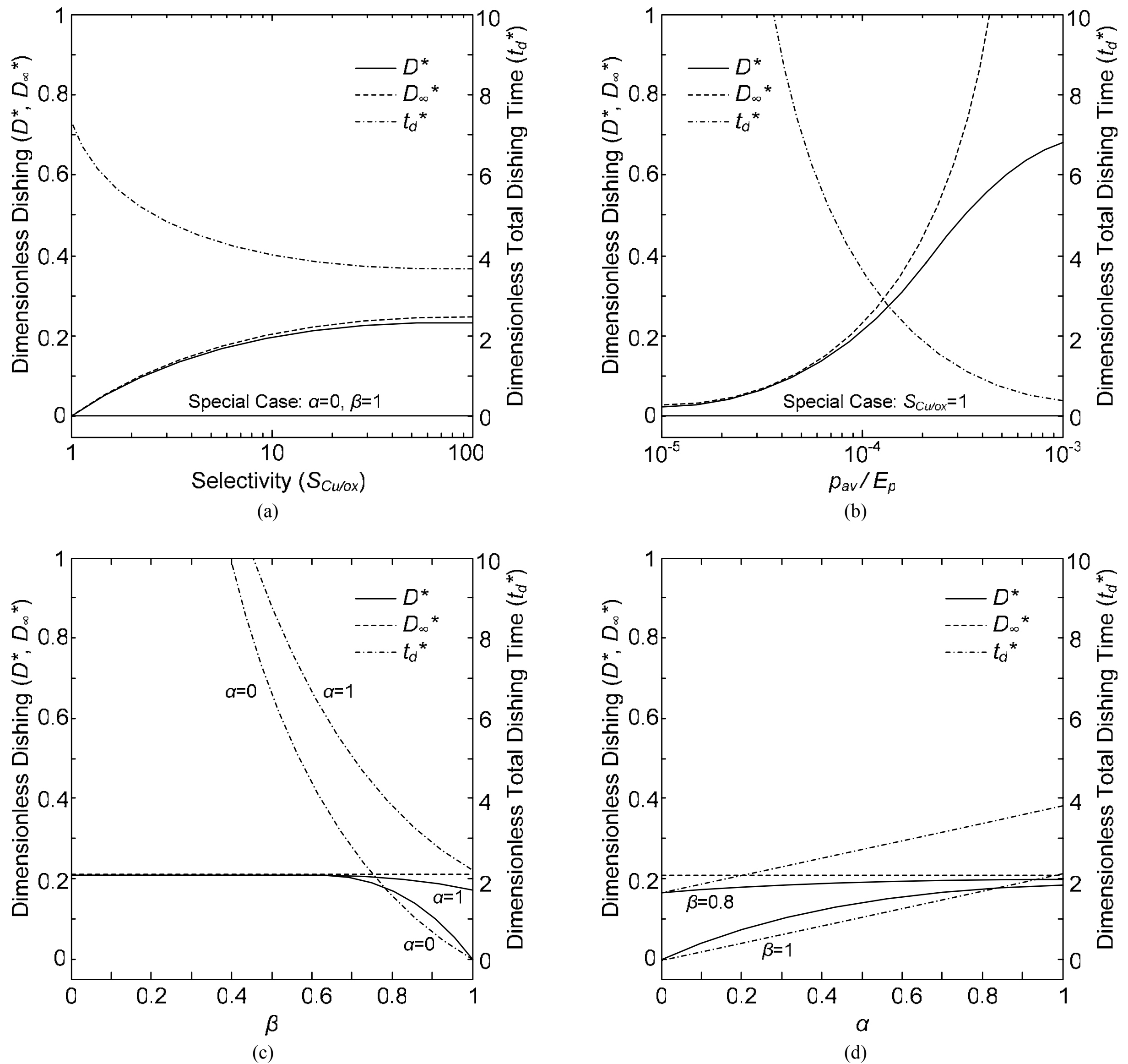


Fig. 8. Effect of model parameters, (a) $S_{Cu/ox}$, (b) p_{av}/E_p, (c)α and (d)β on Cu dishing when w=100μm, λ=200μm, E_p=300MPa, p_{av}=28kPa, and H_o=1.3mm.

Electon Microscopy (SEM). Fig. 10 shows the SEM micrographs of various patterns with the same area fraction (0.5) but of different linewidths (0.5, 2 and 100 μm). The measurements show that α is dependent on the Cu linewidth, w. The selectivity $S_{Cu/ox}$ was determined from the average material removal rates in blanket Cu and oxide wafer polishing experiments.

Experiments were conducted on a rotary 100mm CMP machine with the materials and the conditions listed in Table I and II. To validate the present model, a set of single-step polishing experiments was performed. The same CMP apparatus, and experimental conditions with the blanket wafer polishing experiments, listed in Table II, are used.

The wafer-level non-uniformity factor β in a patterned wafer was obtained by comparing the polishing times between two selected points, the field regions of the fastest slowest dies on the same wafer. Fig. 11 shows the Cu patterned wafers after 3, 4, and 5min of polishing. Photographs of the wafers show that the edge is polished faster than the center area as polishing time increases. In this Cu CMP experiment, β is about 0.8. Finally, Cu dishing was measured by a surface profilometer at the Cu line at the center of each subdie.

After determining all the model parameters, they have been used for calculating dielectric erosion and Cu dishing based on the present model. Fig. 12 compares the developed model and experimental data for Cu dishing. The developed Cu dishing is expressed in a dimensionless form, D^*, the ratio of dishing to the designed Cu interconnect thickness, or the trench depth.

Both the model and the experimental data show that dishing increases as Cu linewidth increases. In the model, this is explained by the Cu deposition factor, α as described in Fig. 8(d). In the submicron region, α is close to zero, and thus, the total dishing time, t_d^*, is smaller than

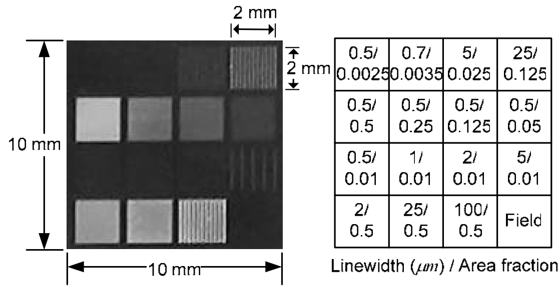


Fig. 9. Schematics of the mask layout and pattern geometry layout for experimental set with MIT-ME mask.

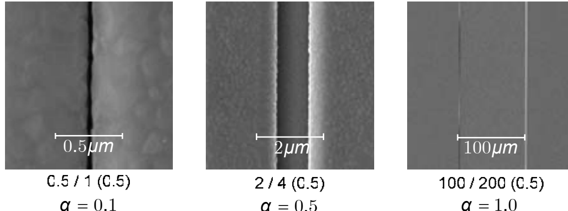
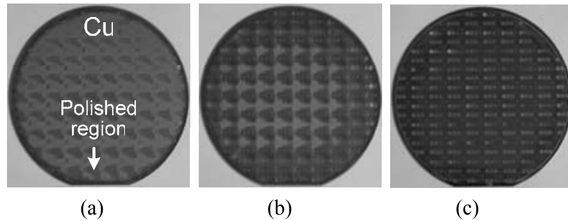


Fig. 10. SEM micrographs for the effect of interconnect deposition factor, α, (a) λ=1μm, w=0.5μm, α = 0.1, (b) λ=4μm, w=2μm, α = 0.8, and (c) λ=200μm, w=100μm, α = 1.



(a) (b) (c)

Fig. 11. Observation of the effect of wafer-level non-uniformity factor, β in Cu patterned wafer polishing at (a) t=3min, (b) t=4min and (c) t=5min.

TABLE I
MATERIAL PROPERTIES

Property	Value
Mask	MIT-ME
Cu deposition	PVD
Cu thickness (nm)	1500
Barrier Layer (nm)	20 (Ta)
SiO_2 trench (nm)	1000
Pad	IC1400
Slurry	iCue5001

TABLE II
EXPERIMENTAL CONDITIONS

Parameter	Value
Diameter of Wafer (mm)	100
Normal Load (N)	228
Pressure (kPa)	28
Rot. Speed (rad/s)	7.8
Linear Velocity (m/s)	0.70
Duration (sec)	60-360
Slurry Flow (ml/sec)	3.3

the global interconnect region, where α is close to one. However, since the wafer-level non-uniformity factor β is 0.8, there is still a significant Cu dishing in the submicron region. In the experiments, however, Cu dishing in the dense sub-micron Cu line region is small even with high selectivity, $S_{Cu/ox}$=14.4. For larger linewidths, on the contrary, Cu dishing is more significant and close to the model values.

The discrepancy between the model and the data in the submicron linewidth region may be due to the following reasons. First, the data in the submicron Cu linewidth

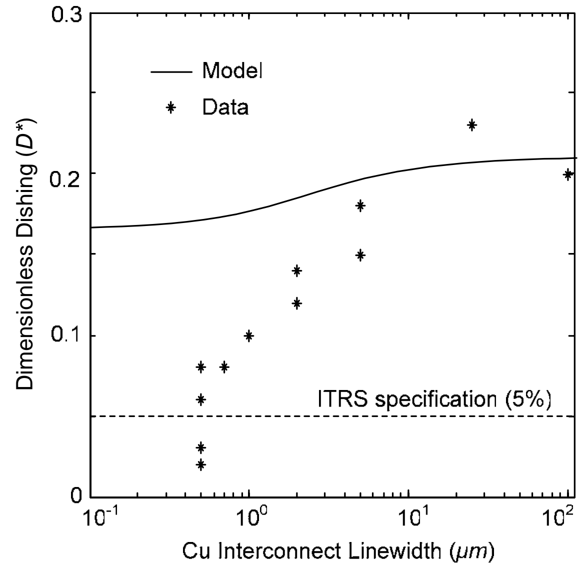


Fig. 12. Experimental results for Cu dishing in a single-step Cu CMP. The model parameters are: MRR_{Cu}=484nm/min, MRR_{ox}=34 nm/min, β=0.8, E_p=300MPa, p_{av}=28kPa, and H_o=1.3mm.

region may not be accurate due to the limit on the measurement resolution of the profilometer. For more accurate data, it is required to use the atomic force microscope (AFM) to determine the surface profile more accurately.

Second, the model assumes that the pad deforms as dicrete uniaxially-loaded blocks under the uniform pressure boundary condition. Clearly, this is a very rough approximation, but may be appropriate in the global wiring region. For large linewidths, the real pad/wafer contact area is small due to surface roughness and thus each contact can be treated as separate block. In the submicron region, however, if the real contact area is greater than the Cu linewidth, the elastic deformation model of a homogeneous, monolithic pad may be more appropriate than the separate pad block model.

Therefore, it appears that dishing in the global wiring-level and in the submicron, device-level cannot be explained by a single model. Nevertheless, since it is well known that Cu dishing is significant in the global-wiring level, the developed model adequately explains dishing where it is a major issue.

VI. SUMMARY

In this paper, a multi-scale Cu dishing model in CMP is proposed by a systematic characterization and modeling of dishing in single-step Cu CMP. The plausible causes of dishing at wafer-, die- and feature-level are identified in terms of the geometric and process parameters. Such parameters include: Cu interconnect deposition factor, α, wafer-level non-uniformity factor, β, selectivity between Cu and oxide, $S_{Cu/ox}$, the Young's modulus of the pad, E_p, and so on.

To model wafer-, die- and feature-level non-uniformities, three separate points in a wafer are

considered. First, to calculate the wafer-level non-uniformity, field regions in the slowest and the fastest die are considered. These two field regions are defined as the global reference point and local reference point, respectively. Additionally, to calculate die-level non-uniformities, the general feature in the fastest die, which is the same die with the local reference point, is considered. Feature-level non-uniformity is characterized as Cu dishing, by calculating the pressure on the Cu lines. The pad is assumed to deform as discrete, uniaxially loaded blocks. Additionally, the effects of wafer- and die-level non-uniformities are characterized by tracking the surface profile at these three locations while polishing.

Physical significances of model parameters are investigated based on the developed model. The role of slurry selectivity on the non-uniformity is explained. High selectivity minimizes dielectric erosion, whereas low selectivity minimizes Cu dishing. Therefore, it is hard to find an optimum selectivity that minimizes both erosion and dishing in single-step polishing. Alternatively, another approach to reduce dishing has been proposed. The wafer-level non-uniformity factor β must be increased and the deposition factor α reduced to minimize both dielectric erosion and Cu dishing, regardless of slurry selectivity.

Experimental and analytical means of determining the model parameters are outlined. The interconnect deposition factor α was obtained by profilometry and SEM. The chemical and chemo-mechanical effects are included as slurry selectivities and were obtained by the average material removal rates from polishing experiments 100mm blanket Cu and oxide wafers. The wafer-level non-uniformity factor β in a patterned wafer was obtained by comparing the polishing times between two selected points, the field regions in the fastest and the slowest dies on the same wafer. Finally, the developed Cu dishing model is validated by data from single-step Cu CMP experiments on 100mm patterned wafers.

Although developed model suggests guidelines to reduce dishing, there are several issues that require further investigation. First, the Cu dishing model should be integrated with dielectric erosion model, for the local pressures on the Cu and oxide regions are interdependent. Second, to consider a realistic pad surface profile in the model, a new contact condition comprising the pad, abrasives and the wafer needs to be developed.

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