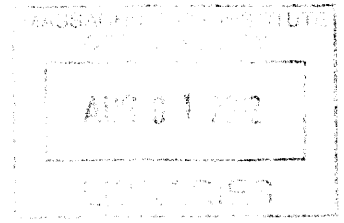


High Frequency AC Power Converter For Low Voltage Circuits

ARCHIVES



by

Nathaniel Jay Tobias Salazar

S.B., Massachusetts Institute of Technology 2011

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

May 2012

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Abstract

This thesis presents a novel AC power delivery architecture that is suitable for VHF frequency (50-100MHz) polyphase AC/DC power conversion in low voltage integrated circuits. A complete AC power delivery architecture was evaluated demonstrating the benefits of delivering power across the interconnect at high voltage and lower current with on- or over-die transformation to low voltage and high current. Two approaches to polyphase matching networks in the transformation stage are compared: a 3-phase system with separate single-phase matching networks and individual full bridge rectifiers, and a 3-phase delta-to-wye matching network and a 3-phase rectifier bridge. In addition, a novel switch-capacitor rectifier capable of 3V, 1W output, was evaluated as an alternative circuit to the diode rectifiers.

A 50MHz prototype of each version of the system was designed and built for a 12:1 conversion ratio with 24V_{pp} line-to-line AC input, 2V DC output and 0.7W output power. The measured overall system efficiency is about 63 % for the 3-phase delta system. Although the application is intended for an integrated CMOS implementation, this thesis primarily focuses on discrete PCB level realizations of the proposed architectures to validate the concept and provide insights for future designs.

Thesis Supervisor: David J. Perreault
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Project Advisor: Wei Li
Title: Doctoral Candidate

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Chapter 1

Introduction

As the performance and complexity of microprocessors increases, the power consumed by them tends to increase as well. A strategy in processor design has been to reduce the core voltage to offset this trend. Despite the reduction in voltage, the total current consumed by the transistors progressively increases. As seen in Figure 1.1, according to the International Technology Roadmap for Semiconductors (ITRS) 2011, the current drawn by high performance microprocessors is currently over 150A and will continue to increase to upwards of 200A by 2020. The increase in total current increases the power losses by the square of the DC current due to resistance of the interconnect and tends to require more of the limited I/O interconnect pin or bumps of the microprocessor. In addition, about 2/3 of the total pins in integrated packages are already used for power and ground [1]. This requirement grows with higher complexity designs which leads to higher power and current demand. Chip power demand has skyrocketed and is approaching the $100W/cm^2$ limit of air cooling [2].

This increased demand to deliver more current while achieving higher performance on the future of computation systems poses a major challenge for CMOS scaling and energy delivery given the current devices and conversion topologies. In order to reduce the loss in the interconnect and minimize the number of necessary power supply pins, one strategy is to deliver power across the interconnect at high voltage and low current with on- or over-die transformation to the low voltage and high current requirement at the core circuits. Voltage conversion ratios

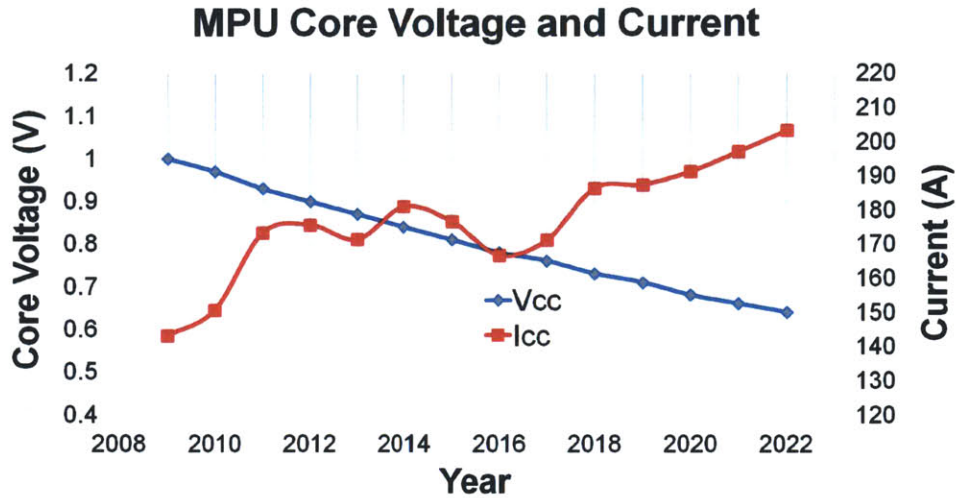


Figure 1.1: International Technology Roadmap for Semiconductors (ITRS) 2011

from 4:1 to more than 12:1, power conversion densities from $1W/mm^2$ to above $10W/mm^2$ and efficiencies greater than 90 percent are desired for local on-die conversion. To date, these requirements have not been satisfied by any conversion system [3] [4] [5] [6]. Current integrated power converters can only maintain good power density and efficiency at small transformation ratios (e.g., 2:1). Meeting all requirements of conversion ratio, power density, and efficiency requires switching at VHF frequencies into the tens of Megahertz. On-chip Si transistor designs are capable of either efficient high-frequency switching or high blocking voltage, but not both. A new architecture is needed to break the tradeoff.

1.1 Architecture Background

Over a hundred years ago, the “War of the Currents” took place between George Westinghouse and Thomas Edison over the means of electric power distribution. Edison promoted low voltage direct current (DC) while Westinghouse championed an alternating current (AC) scheme [7]. However, the DC system suffered two major disadvantages: 1. the distribution range was limited and had a high cost penalty on the required amount of conductor and 2. Higher

distribution voltages could not be easily implemented with the DC system because an efficient, low-cost technology did not exist to convert down large transmission voltage to small utility voltages. Alternatively, the AC system had the advantage of using a transformer to easily step down a high transmission voltage to low voltages for customer loads. This huge advantage of easily converting high-voltage low-current sinusoidal power over distribution lines greatly reduced the conduction loss and conductor cost. It was this fact that led to AC power delivery dominating modern electric-power transmission systems.

The problem of delivering power across the interconnects to a microprocessor is very similar. Delivery of power to the die at the low core voltage requires a large chip pin count (analogous to the high conductor cost in Edison’s system), that could be better used for I/O and computation. Current DC systems lead to voltage drops and conductor loss on die and across the interconnect. Although set at much different scales, the lessons and techniques learned from the "War of the Currents" can be used to address the challenges in creating an efficient high conversion ratio power converter on die.

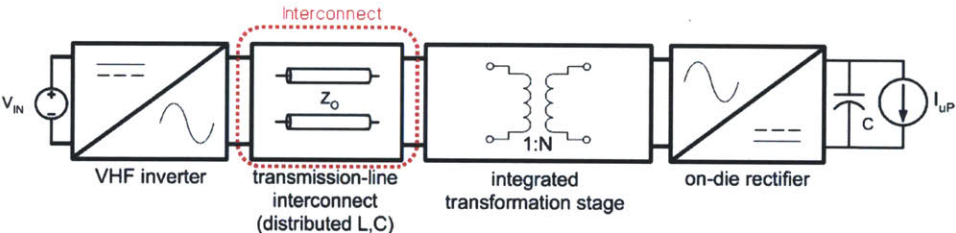


Figure 1.2: Sample Architecture of AC Power Delivery System

Figure 1.2 shows the three major blocks of a DC-DC converter: an inverter stage, transformation stage, and rectification stage. A standard buck converter is not suitable as a high conversion ratio on-die power converter because it has no transformation stage. Thus, the inverting and rectifying devices all see both high current and high voltage which leads to high switching losses. DC-DC architectures with a transformation stage (e.g. coupled-inductor buck, flyback, etc.) can operate using only low voltage rectifier devices. However, they require coupled magnetics (transformers) which are not readily realized on die. Moreover, the inverter

devices still must be both fast and provides high blocking voltages, which are also unavailable in conventional processes. Magnetic based high conversion ratio converters are thus not suitable for on-die power conversion in modern CMOS processes.

Reminiscent of the “War of the Currents,” a possible approach is high-voltage low-current ac distribution across the interconnect, with local on-die transformation and rectification. A version of this concept has been previously proposed [8], but does not provide any enabling means of realizing the high-frequency on-die magnetic transformers needed to accomplish such a topology. This limitation aside, ac distribution in this application has several important merits: It allows high-voltage low-current distribution, enables the use of low-voltage CMOS rectifiers on die, and allows the inverter to be placed off die where size and loss are less important and where it can be effectively realized in a non-CMOS device process.

An alternative to magnetic transformers for voltage transformation is the use of matching networks, which require only inductors and capacitors to realize. With the emergence of high efficiency, high power density integrated inductors at VHF frequencies such as those developed in [9], an AC power delivery system starts to become practical. In [9], a Q of 66 at 100 MHz was reported, and inductors having Q of over 100 are under development. These quality factors are sufficient for constructing high-efficiency matching networks [10].

A full AC power delivery architecture for low-voltage applications shown in Figure 1.3 is considered in this thesis. High-voltage discrete power devices can be used for the off-die VHF inverter stage producing high-voltage, low-current sinusoidal power to be delivered across the interconnect. Inductor/Capacitor passive matching networks are used to transform the power to low-voltage, high current and is then rectified local to the low voltage core circuits to complete the AC power delivery system. To the author’s knowledge, no in-depth analysis of the proposed AC power delivery architecture has been published, nor has the feasibility of the approach been validated. This thesis presents an investigation of the achievable performance of such a system within currently available technology, along with a trade-off comparison among different implementation possibilities. Although the main application for the converter

architecture is for an integrated manifestation, this Master’s thesis primarily focuses on a discrete experimental validation of the feasibility of VHF AC power delivery. This thesis work has been carried out in conjunction with MIT Doctoral Candidate Wei Li who is also considering the integrated implementation of the system.

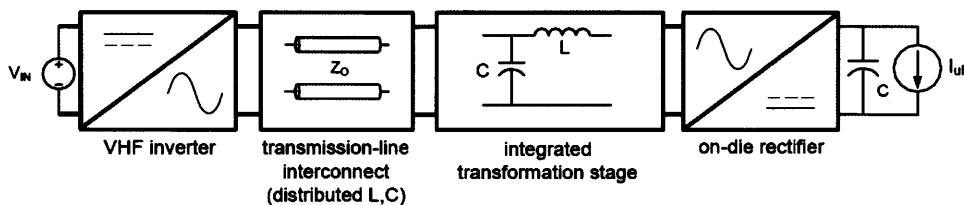


Figure 1.3: Sample Architecture of AC Power Delivery System

1.2 Thesis Objectives, Contribution, and Organization

The goal of this thesis is to explore the performance of a very high frequency (VHF, 30-300MHz) converter for integrated AC power delivery with the following specifications:

- Conversion ratio: $\geq 5:1$ (up to 12:1)
- Power density $\geq 1W/mm^2$ (to $> 10W/mm^2$)
- Efficiency: $\geq 90\%$

Chapter 2 will discuss the theory and operation of matching networks in RF circuits and the design considerations needed for efficient power converter applications. Section 2.1 will discuss the theory in single phase configurations. Then Section 2.2 will expand that theory into polyphase matching network configurations.

In Chapter 3, the design of the rectification stage is discussed. Several types of polyphase rectifiers are considered, highlighting the advantages and limitations of each topology. Section 3.1 will include a discussion of modeling the rectifier needed for designing the transformation stage and detailed analysis of of the essential parameters governing the choice and selection of

the switching components. In addition to standard rectifier circuits, Section 3.2 will introduce a novel switched-capacitor power rectifier topology.

Two different approaches to three-phase AC power delivery are considered. Chapter 4 discusses the design and layout considerations for a three phase topology with separate single phase branches and a three phase topology with delta-wye connections. Photographs with labelled components are presented along with schematics illustrating the critical loops from a layout perspective. Section 4.1 also discusses the method used to generate the three phase input from a single phase RF power amplifier.

Chapter 5 presents the experimental measurements and evaluations of the converters. Important characteristics such as efficiency and power are evaluated.

Finally, Chapter 6 concludes the thesis with a summary of the contributions of this work and a discussion of possible future research directions.

Chapter 2

Matching Networks

The transformation stage of the DC-DC converter of Figure 1.2 is the critical block in achieving the high transformation ratios desired for delivering power to low voltage microprocessors. Indeed, in discrete DC-DC power converters one of the advantages of an AC intermediate stage is the ability to easily achieve high voltage transformation ratios using a magnetic transformer. These transformers often require magnetic cores, and high magnetic coupling of windings which are not readily available on-die. An alternative is a matching network [12], [10] or impedance conversion network [11], which involve passive inductors and capacitors to realize. This chapter discusses the theory of matching network operation and its application in AC power delivery systems.

2.1 Single Phase Matching Networks

A matching network is a passive circuit typically used in communications applications to match impedances between a source and a load necessary to achieve maximum possible transfer of power and/or transform a loading impedance to a desired value [12], [13]. A common example is at the front end of a sensitive RF receiver where very small input signals and power levels require that all available power be transferred. In addition to communication/RF applications, matching networks find many useful applications in power electronics such as

resonant inverters, rectifiers, and dc-dc converters where large voltage transformations are required.

There are two basic matching network topologies that we will consider here; the low-pass and high pass single-stage L-section matching networks shown in Figure 2.1. The networks could be used to either step up or step down the load impedance to match the source impedance, depending on which side is connected to the load or the source [12]. T or Π networks also exist but necessarily have lower efficiency than the L -sections for a given component Q [14] and were thus not considered for the transformation stage. The low pass configuration of Figure 2.1(a) steps up the load impedance Z_L by adding a series leg impedance and steps down the source impedance with a shunt capacitor. Similarly, the high pass configuration of Figure 2.1 (d) steps up the load impedance with a series leg while stepping down the source impedance with a shunt inductor. The load impedance can also be stepped down to a lower source impedance using the low pass configuration of Figure 2.1(b) and the high pass configuration of Figure 2.1 (c). Using a similar qualitative analysis, the load impedance is decreased by a shunt impedance, then a series leg is used to match the reactances.

2.1.1 Theory and Design

The L-section using generic impedances is shown in Figure 2.2. These impedances can be manifested as a capacitor $X = \frac{1}{j\omega C}$ or inductor $X = j\omega L$. The design procedures are well outlined in [12] and [13] and proceeds as follows. Given the necessary resistance transformation ratio or voltage transformation and ignoring parasitic resistances in the passive components

$$\frac{R_p}{R_s} = \frac{V_p^2}{V_s^2} \quad (2.1)$$

after which a quality factor for the transformation is a "transformation Q " defined as

$$Q_T = \sqrt{\frac{R_p}{R_s} - 1} \quad (2.2)$$

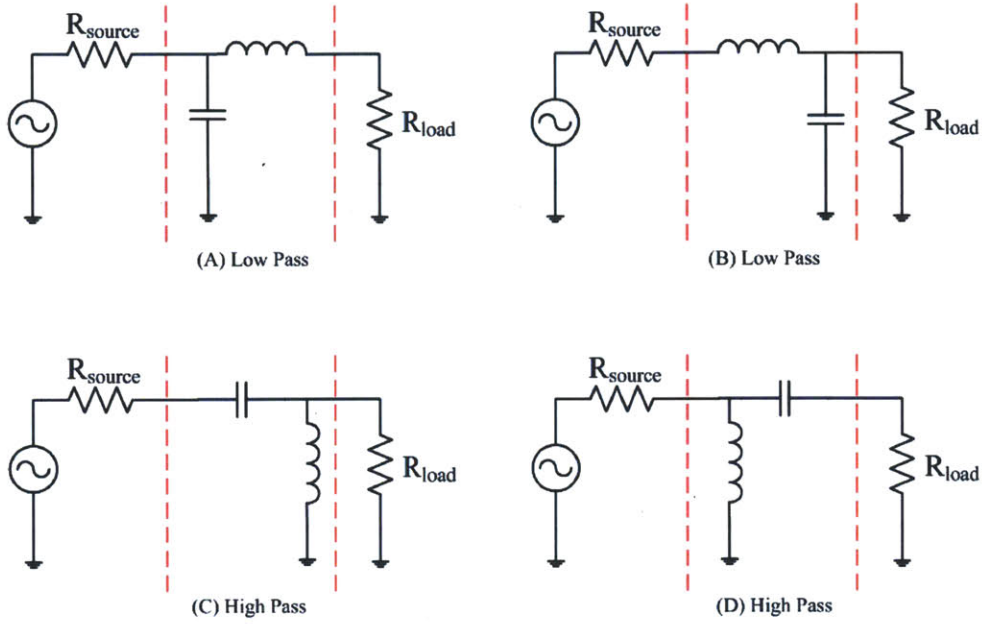


Figure 2.1: L Network

and a series leg quality factor of

$$Q_s = \frac{X_s}{R_s} \quad (2.3)$$

and a shunt leg quality factor of

$$Q_p = \frac{R_p}{|X_p|^*} \quad (2.4)$$

Here Q_s is the quality factor of the series leg, Q_p is the quality factor of the shunt leg, R_p is the matched shunt resistance, R_s is the matched series resistance, X_p is the shunt reactance, and X_s is the series reactance. The notion of quality factor is convenient because, given these definitions, the L-section component values can be computed using the constraint

$$Q_T = Q_s = Q_p \quad (2.5)$$

Plugging in Equations 2.2-2.4 and assuming a low pass filter topology where X_p is a

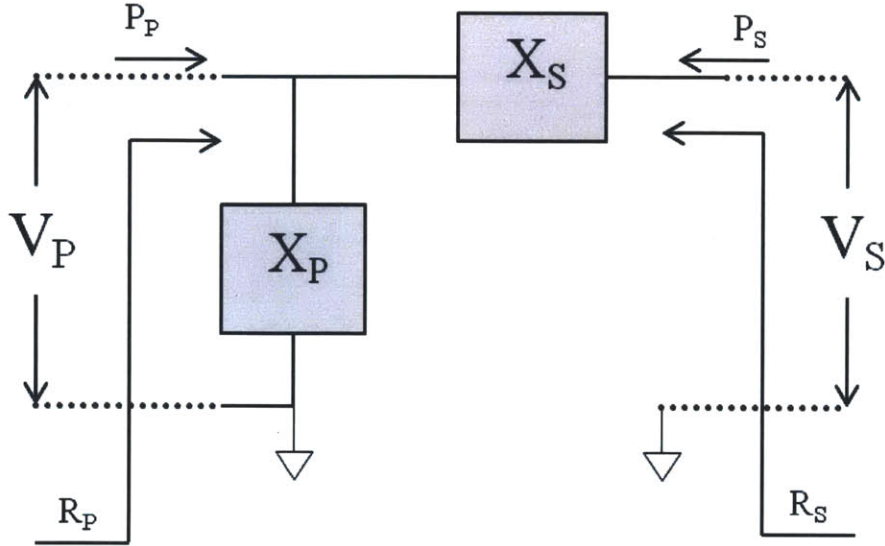


Figure 2.2: Generic L Section

capacitor with capacitance C and X_S is an inductor with inductance L , L and C can be computed as follows:

$$L = Q_T \cdot \frac{R_S}{2\pi f}; \quad C = Q_T / (R_P \cdot 2\pi f) \quad (2.6)$$

From equation 2.6 we note that the sizes of both inductor and capacitor increases with transformation quality factor which is almost linearly related to the voltage transformation ratio. Additionally, the sizes of both components decreases with increasing frequency. This fact is a great motivation to strive for higher operating at frequencies such as VHF.

2.1.2 Efficiency

Here the matching network reactances are designed to attain the targeted transformation ratio neglecting losses in the matching network itself. Perreault and Han in [10] provide a good framework for analyzing the efficiency of the matching network. The following approximation is used: once the circuit is designed on a no-loss basis, the inductor and capacitor losses and circuit efficiency are then calculated based on the losses induced by the currents flowing through

the inductor resistance R_L and capacitor resistance R_C . This approximation is based on the assumption that the branch currents do not change significantly with the presence of small parasitic resistances [14]. Figure 2.3 illustrates the two L-section versions with the parasitic resistances and reactances included for each branch.

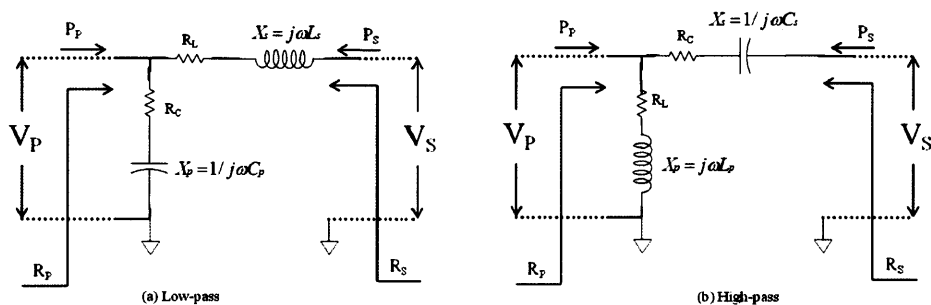


Figure 2.3: L-section matching networks with parasitic resistances and reactances

For low voltage power delivery, the low pass matching network with the left port of 2.3(a) attached to the source and the right port attached to the load is desired as this produces a *stepdown* voltage transformation. In this case, P_p is positive and P_s is negative. The quality factor of the inductor is given by $Q_L = |X_s|/R_L = \omega L_s/R_L$. The quality factor of the capacitor is given by $Q_C = |X_p|/R_C = 1/\omega C_p R_C$. With these definitions in place, it can be shown [10] that

$$|P_s| = 0.5 I_s^2 R_s, |P_p| = \frac{V_p^2}{2R_p} \quad (2.7)$$

$$|P_p| = |P_s| + \frac{Q}{Q_L} |P_s| + \frac{Q}{Q_C} |P_p| \quad (2.8)$$

$$\eta = \frac{|P_s|}{|P_p|} = \frac{1 - \frac{Q}{Q_C}}{1 + \frac{Q}{Q_L}} \quad (2.9)$$

Where η is efficiency of the matching network and Q is the transformation quality factor. For completeness, the formula for the high-pass version with source and load in the same configuration can be calculated as:

$$|P_p| = |P_s| + \frac{Q}{Q_C}|P_s| + \frac{Q}{Q_L}|P_p| \quad (2.10)$$

$$\eta = \frac{|P_s|}{|P_p|} = \frac{1 - \frac{Q}{Q_L}}{1 + \frac{Q}{Q_C}} \quad (2.11)$$

It is common in high efficiency matching networks that $Q/Q_L \ll 1$ and $Q/Q_C \ll 1$ which leads to the approximation that the efficiency is approximately

$$\eta \approx 1 - \frac{Q}{Q_L} - \frac{Q}{Q_C} \quad (2.12)$$

Additionally, for most practical systems $Q_C \gg Q_L$, indicating that inductor loss is the dominant loss mechanism in a matching network. This also leads to the additional approximation of

$$\eta \approx 1 - \frac{Q}{Q_L} = 1 - \frac{\sqrt{\frac{R_p}{R_s} - 1}}{Q_L} \quad (2.13)$$

Thus, in a matching network design, the inductor quality factor is the limiting factor that sets the upper bound on the total efficiency of the matching network. Equation 2.13 indicates that the matching network efficiency is a function of the inductor quality factor Q_L and the transformation ratio. Figure 2.4 from [10] plots the matching network efficiency versus transformation ratio for three different inductor quality factors and for one-, two-, and three-stage designs. It is clear that matching network efficiency decreases with increasing transformation ratio, and decreases at a faster rate with lower inductor quality factor. Thus, for a single stage matching network, to obtain good efficiency requires an inductor with a high quality factor and a low transformation ratio.

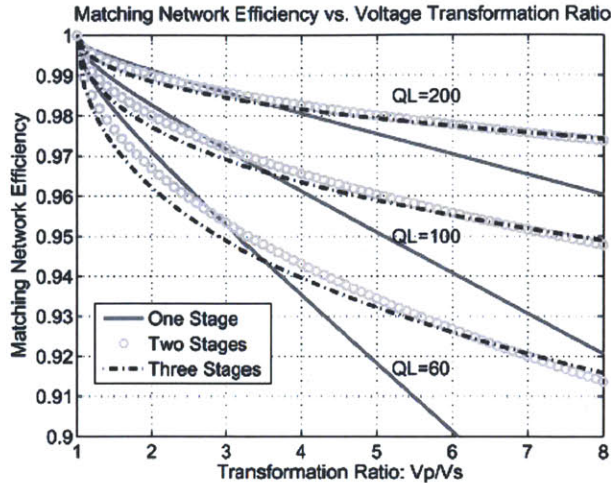


Figure 2.4: Matching Network efficiency versus transformation ratio V_p/V_s . Adapted from [10]

2.1.3 High Q Inductor

High efficiency, high-power density integrated inductors that operate at VHF frequencies are emerging. Integrated inductors such as those in [9] have been and continue to be developed. This has made the development of high efficiency matching networks and AC power delivery systems to be more practical. In [9] and shown in figure 2.5, an integrated inductor with a Q of 66 at 100 MHz was reported, and inductors having quality factors of over 100 are under development. These quality factors are sufficient for constructing high-efficiency matching networks [10].

2.1.4 Matching Network Optimization

For an integrated AC power delivery system, high efficiency, large transformation ratio, and minimum area is desired. Based on the preceding analysis, an analysis was done seeking the optimized operating power levels for a given transformation ratio and component characteristics. Using the characteristics of a standard TSMC process with $1nF/mm^2$ MiM capacitance density and results produced by [9] for a Thin-film V-Groove inductor, the plot shown in Figure 2.6 was produced.

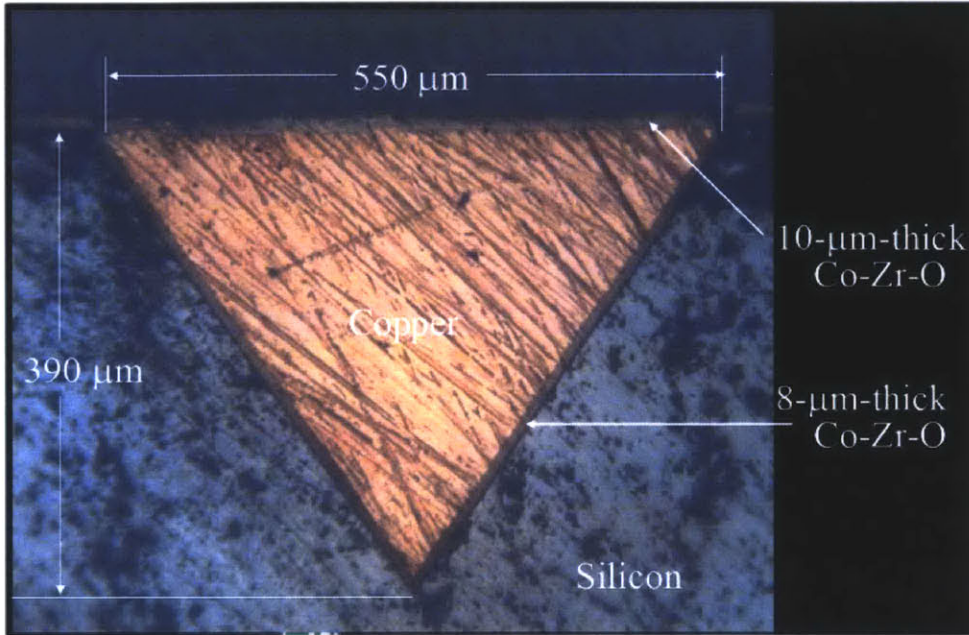


Figure 2.5: Photo courtesy of Prov. Sullivan, Thayer School of Engineering at Dartmouth. Low-loss inductor suitable for VHF operation and 3D integration. [9]

With larger power levels, the matching network inductor size decreases while the capacitor size increases. Efficiency decreases monotonically due to the smaller quality factor in larger capacitors. The optimal area density occurs at a power level of about 2.3W which balances the area of the inductor and capacitor.

2.2 Polyphase Matching Networks

The preceding analysis holds for conventional single-phase matching networks. In typical AC power distribution systems, polyphase power transmission is used because it reduces conduction loss in the system, has nearly constant power flow [16], and reduces harmonics which eases filtering requirements at the load. These advantages in polyphase systems can be leveraged in our integrated AC power delivery system. This sections analyzes the theory and design tradeoffs of polyphase matching matching networks. A discussion of 3-phase system analysis is first introduced. The theory is then generalized to different number of phases and applied

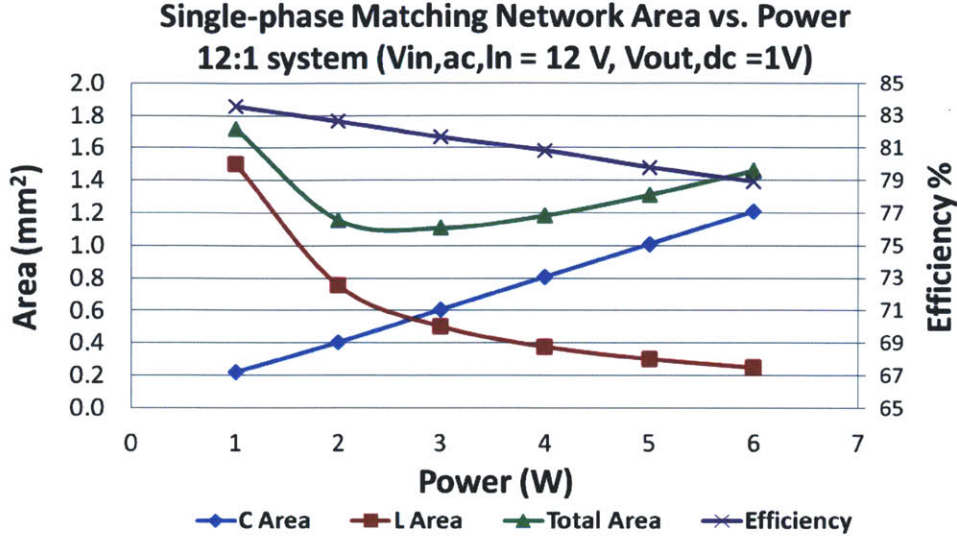


Figure 2.6: Operating power optimization for single phase matching network based on area and efficiency.

to the transformation stage of our AC power delivery system.

2.2.1 Three-Phase Circuits Background

Three-phase electric power is a common method of AC power generation, transmission, and distribution [17]. It is a common form of polyphase power systems and is most widely used by grids to transfer power. Other applications include powering motor systems and other heavy industrial loads. Three phase systems was first presented and patented by Nikola Tesla in 1888. Three-phase system analysis is well outlined in [15] and [16] and proceeds as follows. Consider the arrangement of three voltage sources a , b , and c . The source's line to neutral voltages are

$$v_{an} = V \cos(\omega t) = \text{Re}[V e^{j\omega t}] = V \angle 0^\circ \quad (2.14)$$

$$v_{bn} = V \cos(\omega t - \frac{2\pi}{3}) = \text{Re}[V e^{j\omega t - \frac{2\pi}{3}}] = V \angle -120^\circ \quad (2.15)$$

$$v_{cn} = V \cos(\omega t + \frac{2\pi}{3}) = \text{Re}[V e^{j\omega t + \frac{2\pi}{3}}] = V \angle +120^\circ \quad (2.16)$$

Where V is the amplitude of the sinusoidal voltage and the complex forms and phasor forms are shown. The three-phase set can be attached to a Y-connected (or “wye-connected”) load as shown in Figure 2.7. If the load is balanced with equal impedance of Z_Y on each phase then the line currents can be written as

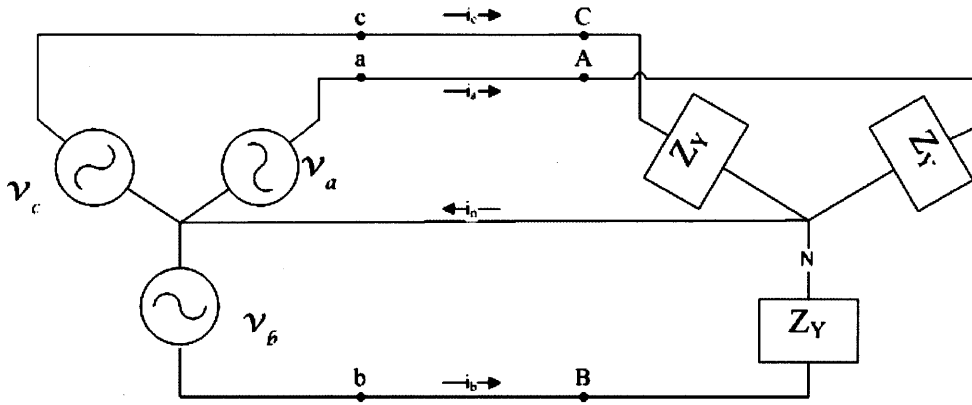


Figure 2.7: Three-phase Y connected source feeding into a Y connected balanced load.

$$i_a = \text{Re}[\frac{V}{Z_Y} e^{j\omega t}] = \frac{V}{Z_Y} \angle 0^\circ \quad (2.17)$$

$$i_b = \text{Re}[\frac{V}{Z_Y} e^{j\omega t - \frac{2\pi}{3}}] = \frac{V}{Z_Y} \angle -120^\circ \quad (2.18)$$

$$i_c = \text{Re}[\frac{V}{Z_Y} e^{j\omega t + \frac{2\pi}{3}}] = \frac{V}{Z_Y} \angle 120^\circ \quad (2.19)$$

Given these equations, it is easily shown in [15] and [16] that the sum of the power through each phase is given by a constant value:

$$P_{Tot} = 3x \frac{|V|^2}{2Z_Y^*} \quad (2.20)$$

The current through the neutral wire is given by the sum of the current in each line and is found to be zero for a balanced three-phase load.

$$i_n = i_a + i_b + i_c = \text{Re}\left[\frac{V}{Z}(e^{j\omega t} + e^{j\omega t - \frac{2\pi}{3}} + e^{j\omega t + \frac{2\pi}{3}})\right] = 0 \quad (2.21)$$

This result can also be seen from a phasor point of view. The current through the neutral wire is the sum of the phasors of each line current. If a diagram was drawn connecting the phasors for the line currents in a balanced set, a closed triangle is formed denoting that the neutral line current is zero. This is true for any balanced non-zero load impedance. If the three-phase set was not balanced because of mismatch in the load impedance, line impedance, or voltages, then some non-zero current would flow through the neutral wire.

The analysis thus far highlights some of the advantages of a three-phase system: 1) The total instantaneous power delivered by a three-phase generator under balanced operating conditions does not vary with time, but is a constant [15]. Single phase systems oscillates between zero and twice average power which creates huge demands on output filtering. In addition, a neutral wire is not needed since there is zero current in balanced loads. The lack of a neutral return path reduces the requirements on the scarce I/O pin real estate.

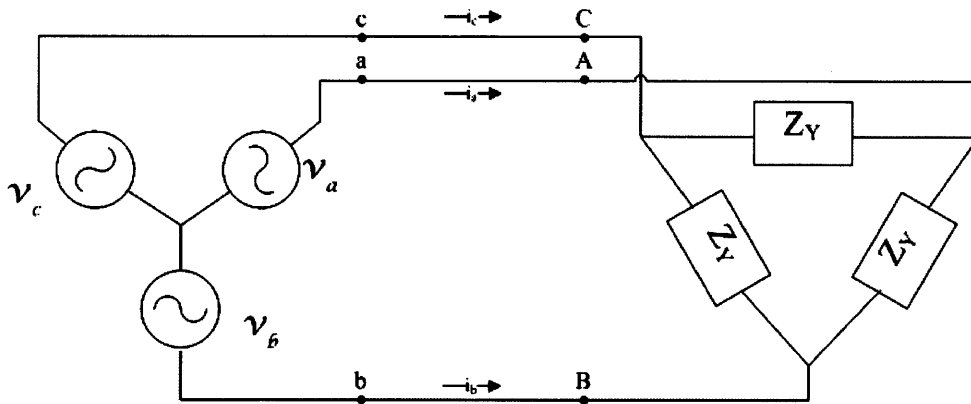


Figure 2.8: Three-phase Y connected source feeding into a Δ connected balanced load.

The load can also be configured in a Δ configuration as shown in Figure 2.8. The Δ load has certain advantages that will be seen in later in this chapter. When analyzing a Δ

configuration, the line-line voltages and currents are considered. As shown in [15] and [16] the line-line voltages are found by taking the difference of line-neutral voltages

$$v_{ab} = v_a - v_b = \text{Re}[V(1 - e^{-j\frac{2\pi}{3}})e^{j\omega t}] = \text{Re}[\sqrt{3}Ve^{j\frac{\pi}{6}}e^{j\omega t}] \quad (2.22)$$

$$v_{bc} = v_b - v_c = \text{Re}[V(e^{-j\frac{2\pi}{3}} - e^{j\frac{2\pi}{3}})e^{j\omega t}] = \text{Re}[\sqrt{3}Ve^{-j\frac{\pi}{2}}e^{j\omega t}] \quad (2.23)$$

$$v_{ca} = v_c - v_a = \text{Re}[V(e^{j\frac{2\pi}{3}} - 1)e^{j\omega t}] = \text{Re}[\sqrt{3}Ve^{j\frac{5\pi}{6}}e^{j\omega t}] \quad (2.24)$$

These phasor equations highlights a useful relationship between line-to-neutral and line-to-line voltages. The line-to-line voltage has a magnitude that is *larger* than the line-to-neutral or line-ground voltage by a factor of $\sqrt{3}$ with a phase shift of 30° leading. The line-line voltages themselves form a three phase *delta* set just as the line-to-neutral voltages form a *wye* connection. Many power systems components such as sources, transformer windings, and loads can be configured to convert between the two connections.

2.2.2 Three Phase Matching Network

The preceding analysis of matching network theory and three phase theory can be used to develop a design strategy for a three-phase matching network set. In each of the three phase “L-section” matching networks shown in Figure 2.9, there is a shunt capacitor on the primary side and a series inductor feeding into each leg of the secondary side for a “wye” configured load. On the primary side, there is freedom to configure the shunt capacitors in either a “delta” or “star” configuration.

In the star connected capacitor network, similar characteristics as the “wye” configuration from Section 2.2.1 are shown. Strictly speaking, the voltage at the capacitor common point (the “wye” point) is zero for a balanced set with no harmonics, but harmonics may be present. The neutral point can either be floating or tied to a fixed potential such as ground (The

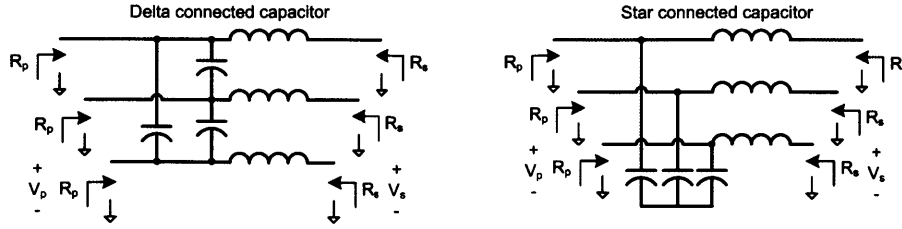


Figure 2.9: Delta vs. Star Matching Network Comparison.

behavior is the same with no harmonics present; with harmonics present, the behavior changes depending on whether the “wye” point is connected to ground or not.). Therefore, substrate referenced capacitors can be used in this configuration. The capacitor and inductor values can be computed similar to the methodology in Section 2.1:

$$Q_T = \sqrt{\frac{R_p}{R_s} - 1} = \sqrt{\frac{V_p^2}{V_s^2} - 1} \quad (2.25)$$

$$L = Q_T \cdot \frac{R_s}{2\pi f}; \quad C = Q_T / \frac{R_p}{2\pi f} \quad (2.26)$$

Where Q_T is the transformation quality factor, R_s is the impedance seen at each phase of the load, and R_p is the impedance seen at the source to neutral, V_s is the target step down voltage for each phase, and V_p is the line-neutral input voltage for each phase. To form a balanced set, each inductor has the same value L and each capacitor has the same value C .

For the delta configured capacitor network, the capacitance and inductance values can be calculated as follows:

$$Q_T = \sqrt{\frac{R_p}{R_s} - 1} = \sqrt{\frac{V_p^2}{V_s^2} - 1} \quad (2.27)$$

$$L = Q_T \cdot \frac{R_s}{2\pi f}; \quad C = Q_T / \frac{R_p / [\sqrt{3}]^2}{2\pi f} \quad (2.28)$$

Where the variables are the same as in the star connection, especially noting that V_p and R_p

are the primary side input voltages and impedances to ground. The $\sqrt{3}$ factor comes from the fact that line-to-line voltages exhibit a $\sqrt{3}$ increase in voltage as compared to line-to-neutral as shown in equations 2.22 to 2.24. Thus, the capacitance value decreases in a three phase delta configuration but requires capacitors having a factor of $\sqrt{3}$ larger voltage rating; the energy stored in the capacitors is the same for either selection. In the case where capacitor breakdown is not a consideration in a particular integrated process, the delta network provides higher power density as it uses smaller capacitor values. We also note that the inductance value does not change when converting between star and delta configurations. Figure 2.10 shows the delta and star configured three-phase matching networks in our AC power delivery block schematic.

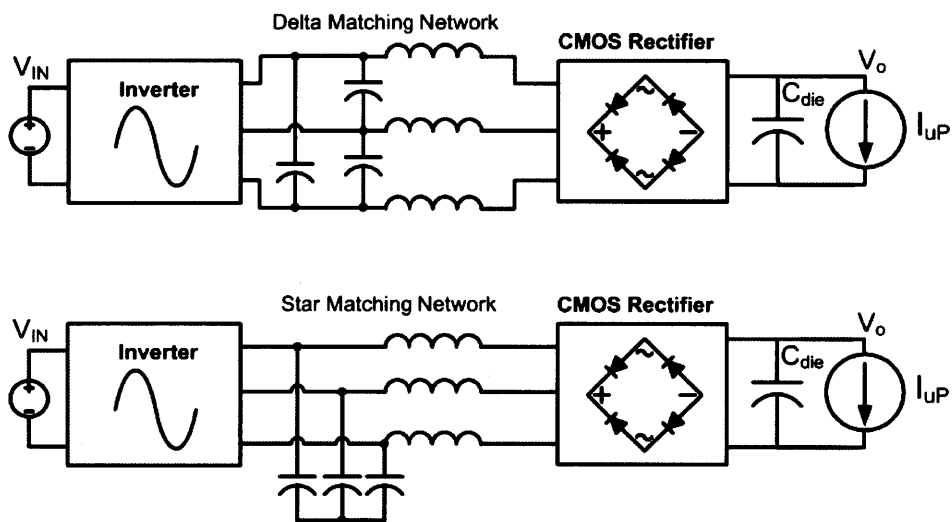


Figure 2.10: Delta and Star connections for Three Phase Matching Network

2.2.3 Polyphase Comparison

Given the analysis of three phase systems in the previous sections, it is useful to compare the three phase topologies to other polyphase systems. A comparison was done on several polyphase AC delivery systems ranging from 1-phase, 3-phase, 4-phase, and 6-phase systems. Figure 2.10 shows the topologies used for each number of phase. In general, each topology

has sources connected in a *delta*-like fashion, ie. each sinusoidal source (inverter) is directly connected on top of the another source and each is shunted by the capacitor of the matching network for that phase. The inductors of the matching networks act as current sources feeding into each totem of a bridge rectifier which behaves as a *wye*-like load from the transformation stage's perspective. The location of the interconnect in which the I^2R losses we're trying to minimize is shown in Figure 2.10 for each m-phase system. It is the node between the high voltage - low current phase-shifted set and the matching network.

The efficiency and areas was computed using typical process parameters with the prototype topologies including the matching network, rectifier, and output filter capacitor stages. This comparison is shown in Figure 2.12. The test systems considered included the efficiencies and area of the delta-connected matching network with MIM capacitors, a half bridge rectifier, MOS capacitor output filter capacitor. The systems were designed to each have a 1V output voltage with a 2 Watt load operating at 100MHz as this operation was found in the previous section to exhibit the optimal area and efficiency in a single-phase matching network. The conversion ratio is the peak-to-peak voltage of the AC input to the DC output voltage.

For fair comparison among the polyphase systems, the total area of the interconnect conductor is fixed for each of the systems with unit resistance R. Splitting the interconnect conductor area for polyphase systems implies that the resistance per line increases for higher number phase. Consider a system comparison without a transformation stage, equal power output, and AC sources connected off-die. As shown in equation 2.29, the power loss in the interconnects are the same for each of the m-phase systems if the line-neutral voltages remain equal.

$$I_{ac} = \frac{\pi P}{mV_o}; P_{loss} = \frac{1}{2} \cdot m \cdot I_{ac}^2 \cdot mR = \frac{\pi^2}{2} \cdot P^2 \cdot \frac{R}{V_o^2} \quad (2.29)$$

Assuming that the capacitor characteristics in this comparison has the ability to block all voltages, the delta-source configuration is chosen so as to maximize power density. The inductor data is based on information from [9]. The capacitors used for the matching networks

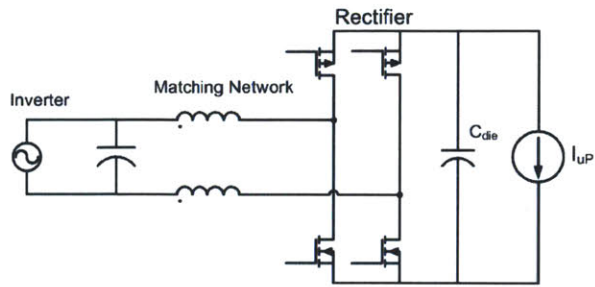
were $1fF/\mu m^2$ MiM capacitors. A MOS capacitor is used for the output filter capacitance and an IBM 65nm process was used for transistor characteristics. Rectifier area and device losses are kept constant for each polyphase system because the output power is held constant. Since the ripple and harmonics are different among each system, the filtering requirements and thus the capacitor size changes.

The optimal polyphase system is also related to capacitor breakdown voltage and component quality factors. As shown in Equation 2.30, in designing the components for the delta matching network, the inductor value does not change with number of phases. However, the capacitance of the delta matching network shows a reduction in capacitance by $[2\sin(\frac{\pi}{m})]^2$ as compared with the star connected matching network for less than $m=6$ phases. Smaller capacitance required in the delta configuration can mean that higher power densities can be achieved (given that the voltage breakdown of the capacitor is not a consideration for the particular process of interest). However, along with smaller capacitance, delta-configured polyphase operation also results in an increase in blocking voltage on the capacitors by a factor of $2\sin(\frac{\pi}{m})$. Therefore, the available capacitor characteristics in a given process must be considered when deciding on the number of phases in a polyphase topology.

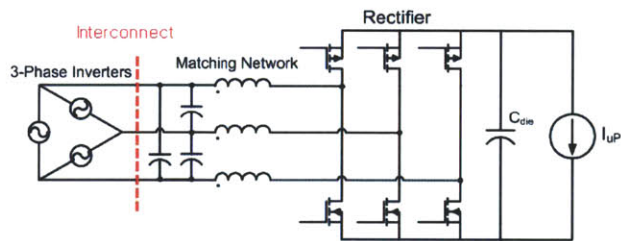
$$L = Q_T \cdot \frac{R_s}{2\pi f}; \quad C = Q_T / \frac{R_p / [2\sin(\frac{\pi}{m})]^2}{2\pi f} \quad (2.30)$$

As shown in Figure 2.12 the three-phase system does indeed exhibit the optimal efficiency and area for any transformation ratios of 2.5, 4, and 6:1. As expected the efficiency of the power delivery systems monotonically decreases for increasing transformation ratios due to the decreased efficiency in the matching network highlighted by [10]. With the three phase topology, a lower output capacitance value is required which better utilizes the MIM capacitors. The comparison predicts that the three phase matching network can achieve 84% efficiency with a 6 to 1 transformation ratio and comes close to achieving a power density of $1 W/mm^2$ with the transformation, rectification, and output filtering capacitor stages. As noted in the previous section, another advantage to three-phase systems is the cancellation of every third

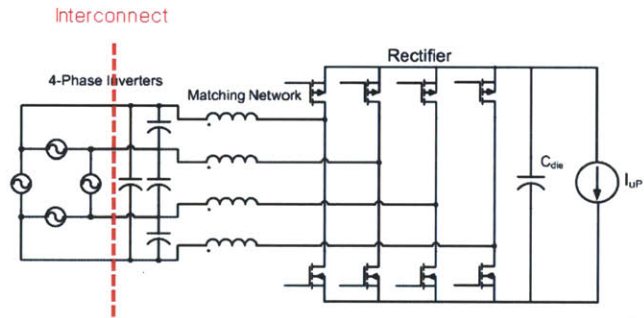
harmonic in the line-line voltages which reduces the requirements on the output filter of the inverter.



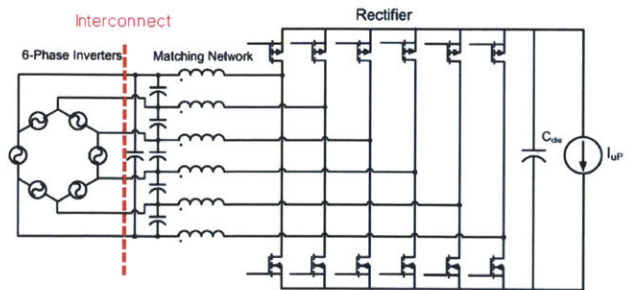
(a) Single Phase Full Bridge System (180° two-phase)



(b) Three Phase System with Delta Configured Sources



(c) Four Phase System with Delta Configured Sources



(d) Six Phase System with Delta Configured Sources

Figure 2.11

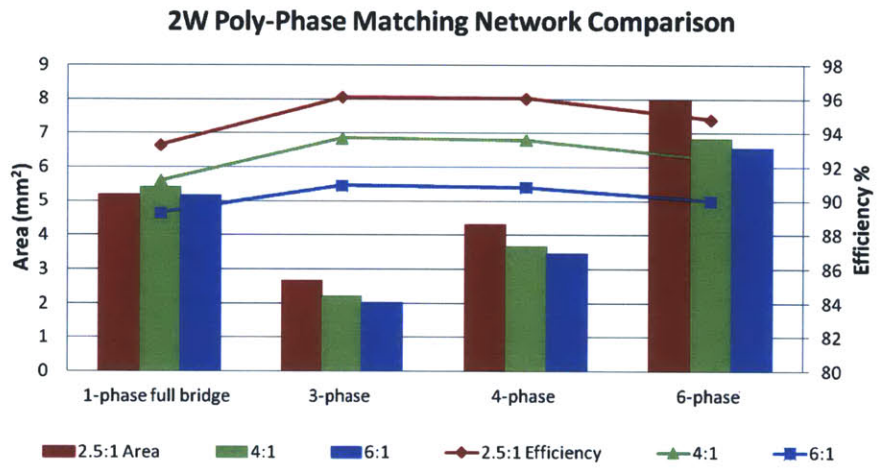


Figure 2.12: 2 Watt Size and Efficiency Comparison for Various Poly-Phase System

Chapter 3

Rectification Stage

A rectification stage is commonly used in power circuits to convert alternating current (AC) to direct current (DC). Rectifiers have also been used in RF communication receivers to convert some bipolar signal to a rectified signal of a constant polarity. The physical switch manifestation of a rectifier can take many forms which include vacuum tube diodes, solid state diodes, silicon controlled rectifier, and CMOS. Among the many types of rectifiers, we first consider two common types: half-wave and full-wave bridge rectification. In half-wave rectification of a single-phase signal only the positive half of the AC wave is passed while the other half is blocked. In full-wave rectification, both sides of the AC input wave are converted to a positive polarity at its output producing a higher voltage. The advantage of a half-wave rectifier includes smaller device count and less loss due to diode drops at the expense of operating on only half of the input waveform. A full-wave rectifier takes advantage of the entire power signal at the expense of a higher device count (unless the full-wave rectifier is center tapped) and two device (e.g., diode) drops. A transformer is often included at the front-end of a rectifier.

This chapter will discuss some basic rectifier topologies and the characteristics most important for high efficiency rectification. The analysis technique of modelling the rectifier as an equivalent resistance will be discussed. This is necessary because our AC power delivery system treats the rectification stage as the load from the matching network's perspective. Constraints and specifications needed in choosing components will be covered. The chapter will conclude

with an introduction of a novel switched-capacitor rectifier that offers higher input swing and larger step down conversion.

3.1 Impedance Matching

As mentioned in a previous section, the matching networks for each phase in the three-phase system feed into each half bridge rectifier. The rectifier act as the load. Together, the three half bridge rectifiers are tied to the same output creating a three-phase bridge rectifier. When designing the matching network we had matched the source (or primary impedance) to a load (or secondary) impedance. Although the rectifier is a switching circuit, a formulation must be developed to model the rectification stage as an impedance in order to design the matching network. This has often been done for resonant power converters, for example in [19], [20]. This section develops that formulation for the basic half bridge rectifier.

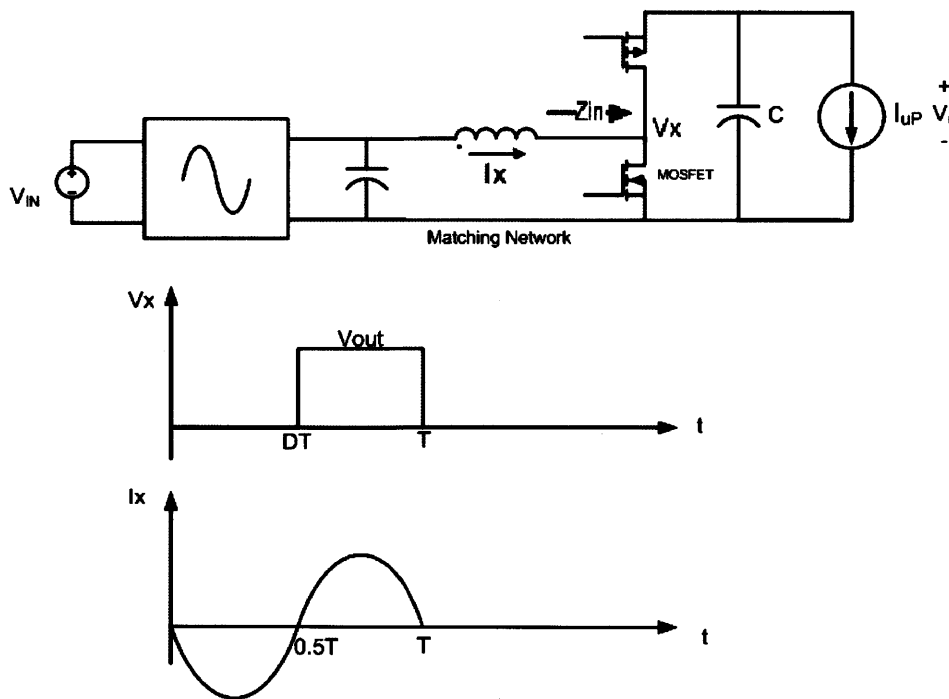


Figure 3.1: Input Voltage and Current of a Half Bridge Rectifier

Figure 3.1 shows the voltage and input current of a half bridge rectifier in one phase of a AC power delivery system. The capacitor C is assumed to be large such that the ripple on the output is negligible and is held at voltage V_{out} . During the negative portion of the input current waveform, the bottom MOSFET in the half bridge is on and the V_x node in the Figure is tied to ground. During the positive portion of the input current waveform, the top MOSFET in the halfbridge is on and the V_x node is tied to the output which is set to V_{out} .

To compute Z_{in} we must first calculate the first harmonic of the V_x voltage as follows:

$$\begin{aligned}
 a_1 &= \frac{2}{T} \int_0^T V_x \sin(\omega t) dt \\
 &= \frac{2}{T} \int_0^{DT} V_{out} \sin(\omega t) dt \\
 &= \frac{V_{out}}{\pi} \cdot (1 - \cos(2\pi D)) \\
 &= 2V_{out}/\pi \text{ for } D = 0.5
 \end{aligned} \tag{3.1}$$

Where D is the duty ratio of the rectifier. Assuming D=0.5, we obtain our first harmonic to be $2V_{out}/\pi$. To find the average current of i_x using charge balance as follows:

$$\begin{aligned}
 i_{out} * T &= i_x \int_0^{DT} \sin(\omega t) dt \\
 i_{out} &= i_x (1 - \cos(2\pi D)) / 2\pi \\
 i_x &= i_{out} \cdot 2\pi / (1 - \cos(2\pi D)) \\
 i_x &= \pi i_{out}
 \end{aligned} \tag{3.2}$$

With the above two equations we can now calculate the half bridge rectifier input impedance

$$Z_{in} = V_x / I_x$$

$$Z_{in} = \frac{V_x}{I_x} = \frac{2}{\pi^2} \frac{V_{out}}{I_{out}} \tag{3.3}$$

The Z_{in} equation is for a half bridge rectifier and can now be used in designing a matching network for our AC delivery system. The design will be discussed in the next chapter. A similar procedure can be used to derive a input impedance of a single phase full bridge rectifier.

$$\begin{aligned}
 a_1 &= \frac{2}{T} \int_0^T V_x \sin(\omega t) dt \\
 &= \frac{2V_{out}}{\pi} \cdot (1 - \cos(2\pi D)) \\
 &= 4V_{out}/\pi \text{ for } D = 0.5
 \end{aligned} \tag{3.4}$$

$$\begin{aligned}
 i_{out} \cdot T &= i_x \int_0^T \sin(\omega t) dt \\
 i_{out} &= 2i_x(1 - \cos(2\pi D))/2\pi \\
 i_x &= i_{out} \cdot \pi/(1 - \cos(2\pi D)) \\
 i_x &= \frac{1}{2}i_{out}
 \end{aligned} \tag{3.5}$$

$$Z_{in} = \frac{V_x}{I_x} = \frac{8}{\pi^2} \frac{V_{out}}{I_{out}} \tag{3.6}$$

Equations 3.3 and 3.6 will be used in the Design chapter 4 to calculate the matching network component values for the Delta-Wye and the Three-Parallel Single-Phase topologies, respectively.

3.1.1 Component Selection

Component selection for the rectification stage is very important as it directly affects the efficiency of the rectifier. Discrete CMOS inverters and schottky diodes were considered for the rectifier switches. For the components we ideally seek large current capability, low on-state voltage (same as low on-resistance for a MOS device operated synchronously), and low capacitance. On-resistance is the primary cause of conduction loss and parasitic capacitance

is the main cause of dynamic power loss. Thus, minimizing the total loss owing to these two parameters is sought. However, in modern semiconductors, these parameters tradeoff with each other, ie. when conduction loss is minimized, capacitance typically increases and vice versa. The power dissipation in a discrete CMOS inverter can be analyzed as shown below:

$$\begin{aligned} R_{on,p} &= (V_{cc} - V_{OH})/I_{OH} \\ R_{on,n} &= V_{OL}/I_{OL} \end{aligned} \quad (3.7)$$

$$\begin{aligned} I_{rms} &= \frac{I_{pk}}{\pi} \\ P_{C,pd} &= V_{cc}^2 \cdot C_{pd} \cdot freq \\ P_{diss,n} &= I_{rms}^2 R_{on,n} \\ P_{diss,p} &= I_{rms}^2 R_{on,p} \end{aligned} \quad (3.8)$$

$$Power_{out} = \frac{I_{pk} V_{cc}}{\pi} \quad (3.9)$$

$$Efficiency = Power_{out}/(Power_{out} + P_{C,pd} + P_{diss,n} + P_{diss,p})$$

Where V_{cc} is the supply voltage, V_{OH} is the high output voltage, V_{OL} is the low output voltage, I_{OH} is the nominal current through the PMOS when output is high, I_{OL} is the nominal current through the NMOS when output is low, I_{pk} is the maximum current through the devices, and C_{pd} is the power dissipation capacitance. These parameters can be found in a typical datasheet for a discrete CMOS half bridge (inverter).

Similar calculations can be done for a Schottky diode rectifier.

$$\begin{aligned} P_{diss,C} &= C_T \cdot V_R^2 freq \\ P_{diss,cond} &= V_f \cdot \frac{I_{pk}}{\pi} + I_{pk}^2 \frac{R_S}{4} - I_{pk} \cdot 0.01 \cdot \frac{R_S}{4} \end{aligned} \quad (3.10)$$

$$Power = \frac{I_{pk}}{\pi} V_R \quad (3.11)$$

$$Efficiency = Power/(Power + 2P_{diss,cond} + 2P_{diss,C})$$

Where C_T is the diode capacitance, V_R is the diode reverse voltage.

3.2 Switch Capacitor Power Rectification

Figure 3.2 shows a sample schematic of our proposed switched-capacitor rectifier. It is a two-level switched-capacitor rectifier, thus it has a $2V_o$ voltage swing at the input of a rectifier, thus providing a $\frac{V_{dc}}{V_{in, fundamental}} = \frac{\pi}{4} : 1$ fundamental AC-to-DC conversion which results in step-down in the rectification stage.

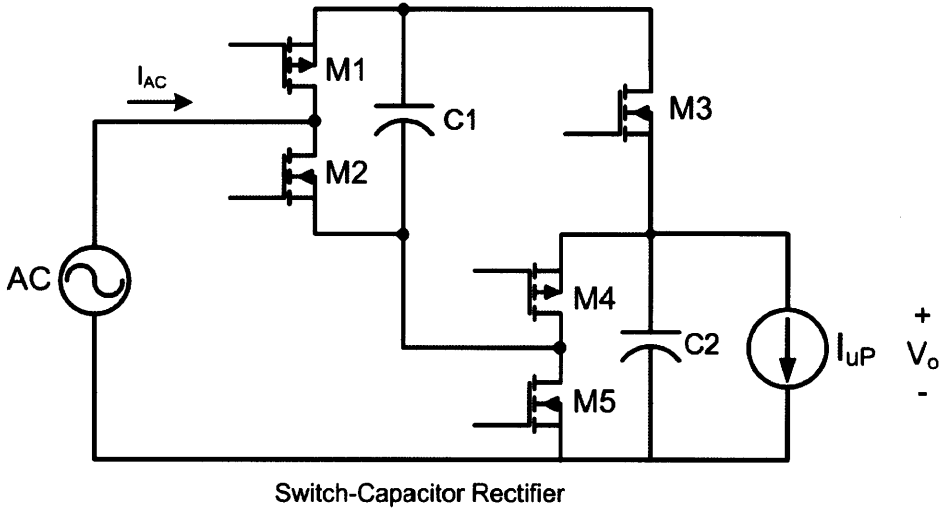


Figure 3.2: Sample Schematic of Two-level Switched-Capacitor Rectifier

Figure 3.3 describes the switched-capacitor rectifier switch operation and Figure 4 describes the theoretical switching and voltage waveforms. When the input ac current is positive, S1s are closed and S2s are open, positive current charges C1 and C2 and supports the load current. When the input current is negative, S1s are open and S2s are closed. In this case, C1 and C2 are connected in parallel to support the load. From the switched-capacitor rectifier operation, we can see that all the devices only need to block the low output voltage level. As a result, low voltage CMOS device can be used to provide fast switching speed. Moreover, device M3 sits on top of the dc output voltage, so it can be driven easily. In addition, the first level devices M1 and M2 can be made to be self-driven by the output voltage. As a result, a 2-level

switched-capacitor rectifier can be controlled simply. Higher level switched-capacitor rectifiers can provide higher step-down ratios. But a higher-level rectifier requires a higher device count and greater control complexity.

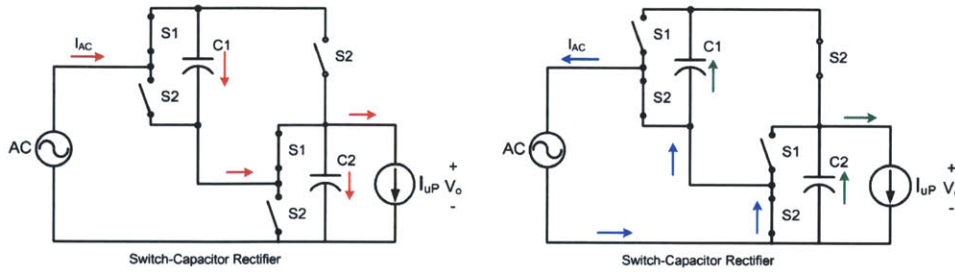


Figure 3.3: Switched-Capacitor Rectifier Switch Operation

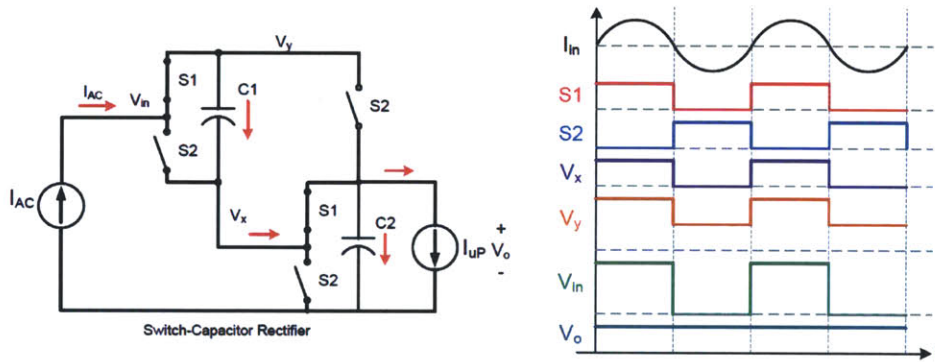


Figure 3.4: Switched-Capacitor Rectifier Operation Waveforms

The switched-capacitor structure can be extended to full-wave rectification or to any number of phases. Higher order switched-capacitor rectifiers can achieve even larger step down ratios at the expense of control complexity and component count. To further explore the functionality of the switched-capacitor rectifier and validate the concept, a two-level full bridge switched-capacitor rectifier prototype was built with discrete components and will be further validated in an IC implementation. The topology tested shown in Figure 5 below. The integrated rectifier was designed for a 2.5V output voltage operating at a 50MHz switching frequency.

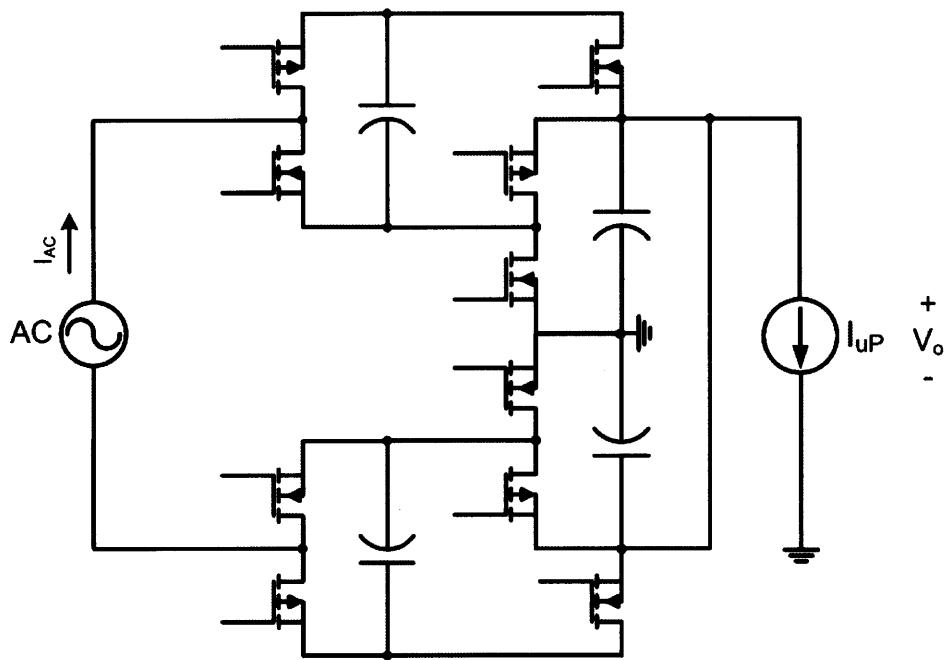


Figure 3.5: Sample Architecture of AC Power Delivery System

Chapter 4

Design and Layout

In order to validate the feasibility of delivering polyphase AC power at VHF frequencies and rectification for low-voltage dc output, a discrete experimental prototype was designed. Although the converter architecture is targeted for a low-voltage integrated process, the prototype is implemented with discrete components purely to validate the concept and provide insights for future designs. Given the available components, we do not pursue the performance and power density expected in an integrated system.

Two different approaches to three phase AC power delivery are considered. This chapter discusses the design and layout considerations for a three phase topology with separate single phase full bridge branches and a three phase topology with delta-wye connected matching network. Photographs with labelled components are presented along with schematics illustrating the critical loops from a layout perspective. Complete EAGLE schematics and layouts are provided in the Appendix. Section 4.1 begins by discussing the method used to generate the three phase input from a single phase RF power amplifier.

4.1 Generating Three Phase Power

4.1.1 Matching Network Phase Shifting

There are several ways to generate three phase power. Two methods considered are T matching networks for a specified phase shift and coaxial cables of precisely cut lengths. Coaxial cables were eventually used for the final PCB test board. However we will first discuss the T matching network for a specified phase shift and discuss the practical issues involved in such a method. We will then proceed with the design process for the coaxial cable method.

Figure 4.1 shows the general form of a T matching network. Like the L-section matching network, regardless of the generator input impedance, the output load can be modified by the matching network so that the load and source impedances are equal ensuring maximum power transfer. The T matching network is often used to match two low-valued impedances when high-Q arrangement is needed [12]. The T networks was not considered in Chapter 3 because it is generally less efficient than an L-section. However, for our application the efficiency of the transformation stage and rectification stage is the primary concern, and the ability of a T section to provide a specified phase shift of interest.

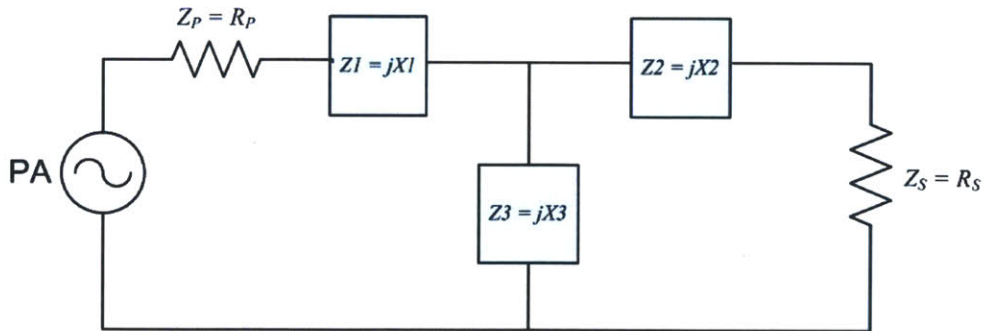


Figure 4.1: General Form of the T impedance-matching network

Given this topology, source and load resistances, operating frequency, and the necessary phase shift, [14] derives the reactances necessary for each block of the T network. These formulas assume the T network is a lossless structure, ie. parasitic resistances, inductances, or

capacitances are negligible. The equations are given below.

$$X_3 = -\frac{\sqrt{R_S R_P}}{\sin\theta} \quad (4.1)$$

$$X_1 = -\frac{R_P}{\tan\theta} + \frac{\sqrt{R_S R_P}}{\sin\theta} \quad (4.2)$$

$$X_2 = -\frac{R_S}{\tan\theta} + \frac{\sqrt{R_S R_P}}{\sin\theta} \quad (4.3)$$

Where θ is the desired phase shift and θ is positive if the load current lags and negative if the load current leads the input current. If the value for the reactance X is positive, then an inductor with the calculated reactance at the operating frequency is used. Similarly, if the reactance X is negative, then a capacitor with the calculated reactance is used.

In designing the phase shifting circuits, the target source and load impedance must first be known. A single power amplifier with an output impedance of 50Ω is used as the AC power source for our testing purposes. To obtain maximum power transfer, an equivalent impedance of 50Ω must be seen from the point of view of the power amplifier. To satisfy this constraint, we design for an equivalent impedance of 150Ω looking into each phase. From the point of view of the power amplifier, three 150Ω impedances in parallel looks like 50Ω . For reasons discussed in a following section, the load impedance required for the phase splitting network is 400Ω . For this matching requirement, the transformation quality factor is $\sqrt{\frac{400}{150}} - 1 = 1.291$.

Using these source and load design impedances, a T network was designed. One L-section was designed for an in-phase matching. A -120° and $+120^\circ$ network was designed to complete the balanced three phase splitting network. Our system operates at 50MHz which has a period of $T = 20\text{ns}$. Given this our networks should result in a -6.6ns , 0s , and $+6.6\text{ns}$ delay/lead.

T-section Lag Network

$$\begin{aligned}
 X_3 &= -\frac{\sqrt{R_S R_P}}{\sin\theta} = -\frac{\sqrt{150\Omega \cdot 400\Omega}}{\sin 120^\circ} \\
 &= -282.8\Omega \\
 &\rightarrow C = 11.2\text{pF} \\
 X_1 &= -\frac{R_P}{\tan\theta} + \frac{\sqrt{R_S R_P}}{\sin\theta} = -\frac{150\Omega}{\tan 120^\circ} + \frac{\sqrt{150\Omega \cdot 400\Omega}}{\sin 120^\circ} \\
 &= 369.4\Omega \\
 &\rightarrow L_1 = 1.17\mu\text{F} \\
 X_2 &= -\frac{R_S}{\tan\theta} + \frac{\sqrt{R_S R_P}}{\sin\theta} = -\frac{400\Omega}{\tan 120^\circ} + \frac{\sqrt{400\Omega \cdot 150\Omega}}{\sin 120^\circ} \\
 &= 513.8\Omega \\
 &\rightarrow L_2 = 1.63\mu\text{F}
 \end{aligned} \tag{4.4}$$

T-section Lead Network

$$\begin{aligned}
 X_3 &= -\frac{\sqrt{R_S R_P}}{\sin\theta} = -\frac{\sqrt{150\Omega \cdot 400\Omega}}{\sin(-120^\circ)} \\
 &= 282.8\Omega \\
 &\rightarrow L = 900\text{nF} \\
 X_1 &= -\frac{R_P}{\tan\theta} + \frac{\sqrt{R_S R_P}}{\sin\theta} = -\frac{150\Omega}{\tan - 120^\circ} + \frac{\sqrt{150\Omega \cdot 400\Omega}}{\sin - 120^\circ} \\
 &= -369.4\Omega \\
 &\rightarrow C_1 = 8.6\text{pF} \\
 X_2 &= -\frac{R_S}{\tan\theta} + \frac{\sqrt{R_S R_P}}{\sin\theta} = -\frac{400\Omega}{\tan - 120^\circ} + \frac{\sqrt{400\Omega \cdot 150\Omega}}{\sin - 120^\circ} \\
 &= -513.8\Omega \\
 &\rightarrow L_2 = 6.2\text{pF}
 \end{aligned} \tag{4.5}$$

L-section In-Phase Network

$$\begin{aligned} L_s &= \frac{QR_s}{\omega} = 1.291 \cdot 150\Omega / (2\pi \cdot 50MHz) = 616nH \\ C_p &= \frac{Q}{R_p\omega} = 1.291 / (400\Omega \cdot 2\pi \cdot 50MHz) = 10.3pF \end{aligned} \tag{4.6}$$

Equation 4.4 describes the design for the 6.6ns *lag* network. Equation 4.5 describes the 6.6ns *lead* network. And equation 4.6 describes the 0s in-phase L-section network. Figure 4.2 shows the complete phase shifting matching network schematics with the calculated impedances replaced with the corresponding passive device.

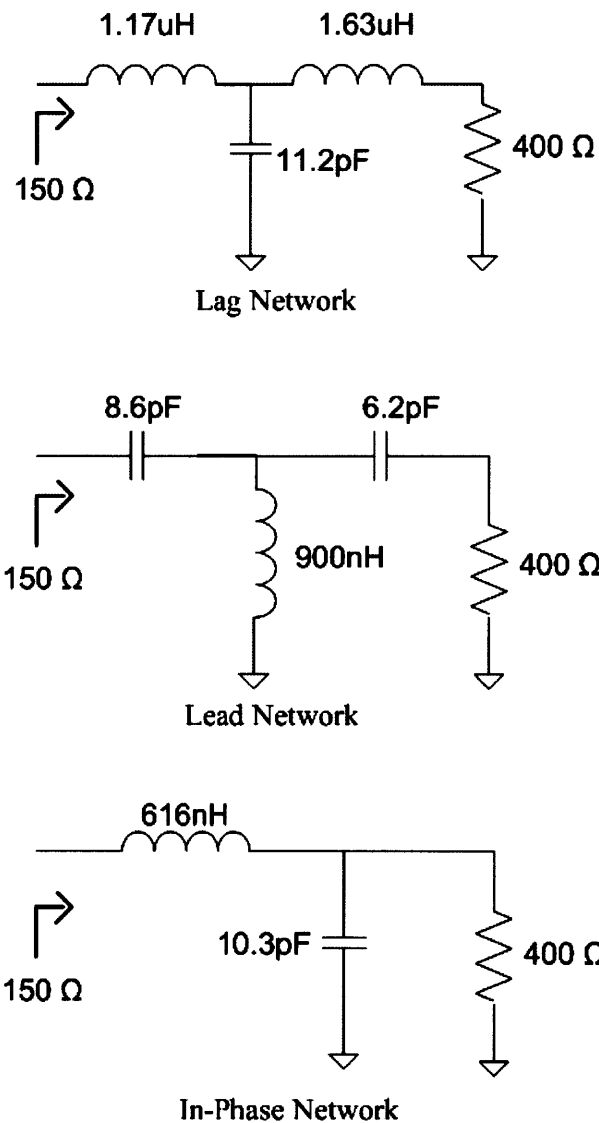


Figure 4.2: Schematic For Possible Three-Phase Phase-Shifting network

This design exhibits accurate matching and phase shifting in simulation. However, this method of generating balanced three phase power was not used in the test board due to a few practical issues. The calculated capacitances are very small and around the same value as the parasitic capacitances between pads on a PCB. For example, a general rule of thumb for FR-4 PCB boards is that inter-pad capacitance is about 10-20pF. Since our calculated capacitances are 10pF, tuning the capacitance value would be fairly difficult and lead to unbalanced phase

shifting. Therefore another method of splitting and phase shifting was used.

4.1.2 Coaxial Cable Phase Shifting

Coaxial cable is characterized by an inner conductor surrounded by a flexible dielectric insulating layer, which is then surrounded by metallic conducting shield. The term *coaxial* is used to describe the fact that the inner and outer conductor share the same geometric axis. Coaxial cable is typically used as transmission line for RF signals because, in an ideal cable, the electromagnetic fields carrying the signal exist only in between the inner and outer conductors. This results in efficient power transmission and resilience to external electromagnetic interference. This makes makes coaxial cables an excellent choice for our VHF application.

The coaxial cable is a type of transmission line and can thus be modelled as a distributed L-C ladder with some finite distributed series resistance and shunt conductance. For our purposes we assume resistances are zero and the characteristic impedance is set only by the inductances and capacitances. The shunt capacitance per unit length and series inductance per unit length are fundamental electrical parameters that can be calculated with geometric and material constants as shown below [21]:

$$\frac{C}{l} = \frac{2\pi\epsilon_0\epsilon_r}{\ln(D/d)} \quad \text{F/m} \quad (4.7)$$

$$\frac{L}{l} = \frac{\mu_0\mu_r}{2\pi} \ln(D/d) \quad \text{H/m} \quad (4.8)$$

Where ϵ_0 is the dielectric constant of free space, ϵ_r is the relative dielectric constant of the insulating layer, μ_0 is the permeability of free space, μ_r is the relative permeability of the insulator, D is the inside diameter of the shield, and d is the outside diameter of the inner conductor.

Derived electrical parameters such as characteristic impedance and delay of a segment of coaxial can also be solved as shown below:

$$Z_0 = \sqrt{\frac{L}{C}} \quad \Omega \quad (4.9)$$

$$Delay = \sqrt{LC} \quad \text{seconds} \quad (4.10)$$

Where Z_0 is the characteristic impedance in ohms and the delay is in seconds. One notices that the characteristic impedance is independent of the length of the coax segment. The L and C used for the delay are measured for the same length. Thus the delay is ideally linearly dependent on the length of the coax segment. We use this fact to create our balanced three-phase delay.

In terms of design, coaxial cable datasheets typically specify the characteristic impedance and capacitance per 1 foot. With these parameters known, delay and corresponding cable length can be calculated as follows.

$$\begin{aligned} L/l &= (C/l) \cdot Z_0^2 \quad \text{H/ft} \\ Delay/l &= \sqrt{\frac{L}{l} \cdot \frac{C}{l}} \quad \text{seconds/ft} \\ length &= (delay) / \frac{Delay}{l} \end{aligned} \quad (4.11)$$

For our system, we design for 0s, 6.66ns, and 13.32ns delays which will satisfy 0° , 120° , and 240° phase shifting. For the coaxial cable, Pomona Electronics 2249 series RG-58C 50Ω cable was used. The datasheet indicates a capacitance per foot of $C/l = 30.8pF$. The inductance per foot and the delay per foot can be calculated as:

$$\begin{aligned} L &= CZ_0^2 = 30.8pF/ft \cdot (50\Omega)^2 = 77nH/ft \\ Delay/ft &= \sqrt{LC} = \sqrt{30.8pF/ft \cdot 77nH/ft} = 1.54ns/ft \end{aligned} \quad (4.12)$$

A foot of coaxial cable is used for the in phase (0s delay) so as to achieve proper impedance matching among phases. Thus we add an additional 1ft to each of the calculated coaxial

lengths for the 120° and 240° delays.

$$6.66ns \rightarrow 4.32 + 1 = 5.32ft; \quad 13.32ns \rightarrow 8.64 + 1 = 9.64ft \quad (4.13)$$

These lengths were used as they provided surprisingly accurate delay. The final coaxial cable three phase power splitting network is shown below.

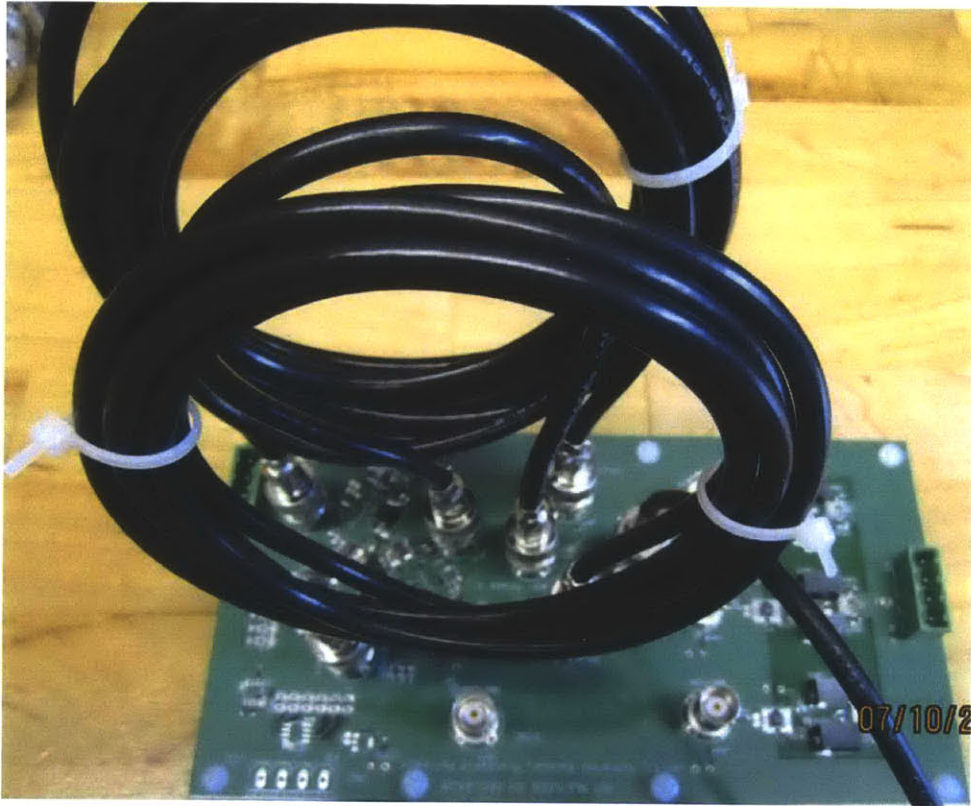


Figure 4.3: Coaxial Cable Setup for Three Phase generation

To obtain maximum power transfer, the impedance looking into the coaxial cable splitting network must equivalently be equal to the power source's impedance i.e., 50Ω of the power amplifier. Thus an extra 100Ω resistor is placed in series with each coaxial cable. The 50Ω characteristic impedance of the coaxial cable plus the 100Ω resistance appears as 150Ω looking into each branch of the phase-shifting network. Three 150Ω branches in parallel appear as 50Ω , theoretically achieving maximum power transfer.

4.1.3 Isolation Transformer

This section discusses the analysis for the choice of an isolation transformer front-end. After the three phase power is split with the coaxial cables, floating outputs are then generated with a set of RF transformers. Using transformers allows the AC power for each phase to be modelled as current sources and allows the sources to easily be reconfigured as Y or Δ sources.

In order to get efficient power transfer through the transformation stage and to minimize unnecessary ringing due to parasitic effects, we include series capacitances to cancel out leakage inductance in the transformer. To do this, the leakage inductance need to be measured.

Using an impedance analyzer and the setup shown below in Figures 4.4 and 4.5 the leakage inductances on both sides of the transformer can be measured. The Agilent 4395A Network Analyzer was used for impedance measurements. For the setup in Figure 4.4 with the secondary shorted, the inductance seen at the primary can be approximated as

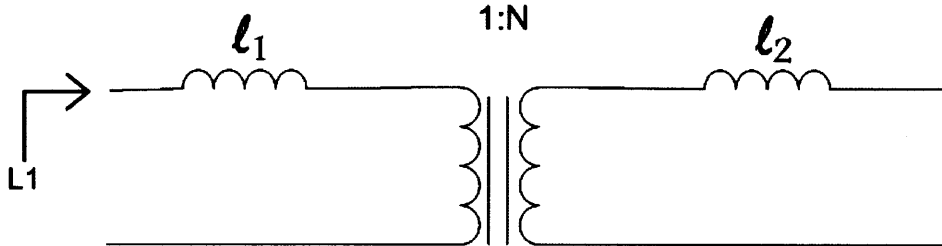


Figure 4.4: Leakage test setup with secondary shorted. Coilcraft WBC1-8L 1:8 Impedance Ratio. Measured $L_1 = 17.6\text{nH}$. $l_1 = 14.5\text{nH}$

$$L_1 = l_1 + \frac{l_2}{N^2} \quad (4.14)$$

Where l_1 and l_2 are the primary side and secondary side leakage inductances, respectively, and N is the voltage transformation ratio in the transformer. With the secondary end shorted the leakage inductance alone is reflected across the transformer with the leakage impedance being divided by the square the transformation ratio. On the primary side $\frac{l_2}{N^2}$ is now in parallel with the magnetizing inductance. The magnetizing inductance is assumed to be much larger

than $\frac{l_2}{N^2}$ so the magnetizing inductance can approximately be ignored, leaving l_1 and $\frac{l_2}{N^2}$. L_1 was measured to be 17.6nH at 50MHz. Using the assumption that $8l_1 = l_2$ and equation 4.14, the primary side leakage inductance is calculated to be 14.5nH. A capacitance of 680pF is used to resonate the primary side leakage inductance at 50MHz.

A similar analysis can be done the setup in Figure 4.5. With the primary side shorted the leakage measured on the secondary can be approximated as below:

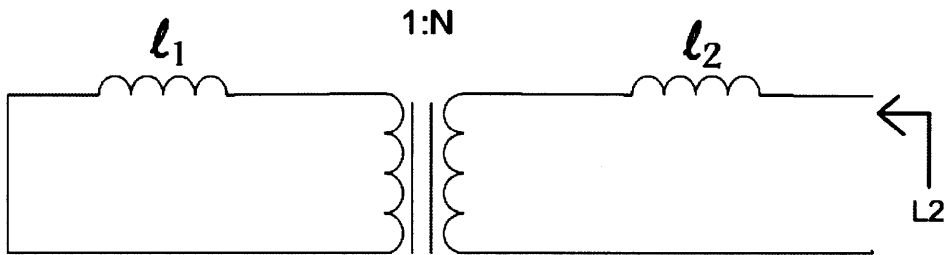


Figure 4.5: Leakage test setup with secondary shorted. Coilcraft WBC1-8L 1:8 Impedance Ratio . Measured $L_2 = 130.4\text{nH}$. $l_2 = 156\text{nH}$

$$L_2 = l_2 + N^2 l_1 \tag{4.15}$$

With the primary shorted, the primary side leakage inductance is transformed over to the primary side with a multiplier factor of N^2 leaving $N^2 l_1$ and l_2 as seen from the secondary. L_2 is measured to be 130.4nH. Using Equation 4.15, the secondary leakage inductance is calculated to be 156nH. A capacitance of 68pF is used to resonate out the secondary side leakage inductance for the delta-wye system as shown in Figure 4.9. To maintain symmetry in the parallel single-phase system, the leakage cancelling capacitor is split on both ends of the secondary as shown in Figure 4.7. Half of the 156nH secondary-side leakage is modelled to appear on each end of the secondary. Thus a capacitance to cancel $78\text{nH} \rightarrow 129\text{pF}$ is calculated. A capacitance of 130pF is the available value used on the PCB.

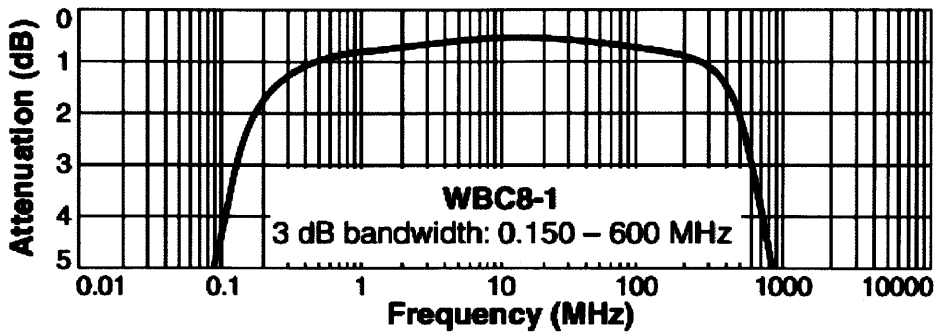


Figure 4.6: Frequency Response for Coilcraft WBC8-1L Mini Wideband Transformer Taken from Datasheet

The transformer chosen is the Coilcraft WBC8-1L Mini Wideband Transformer. The datasheet for the WBC series transformer provides plots of attenuation insertion loss over frequency as shown in Figure 4.6. At 50MHz, the insertion loss is approximately 0.63dB of attenuation. Solving for efficiency in $-0.63dB = 20\log(\eta)$ results in an expected efficiency of approximately $\eta = 93\%$

4.2 Three Phase - Separate Single Phase

The Delta-Wye System operates at 50MHz with input peak-to-peak line-to-line AC voltage of 24V and the DC output voltage of 2V. Output power is 0.7W, which is limited by the discrete RF transformers. Infineon BAT60A diodes are used for the rectifier since discrete CMOS rectifier having appropriate characteristics were not available. Figure 4.7 shows the schematic of a 3-phase system with separate single-phase matching networks and individual full bridge rectifiers. 39pF ATC 700A capacitors and 130nH Coilcraft Maxi Spring air core inductors were used to form each of the separate single-phase $\frac{3\pi}{2}$ matching network. The full-bridge rectifier provides a fundamental ac-to-dc conversion of $\frac{4}{\pi}$. Together, the matching network and the rectifier stage provides an overall voltage conversion ratio in the AC system of 6:1.

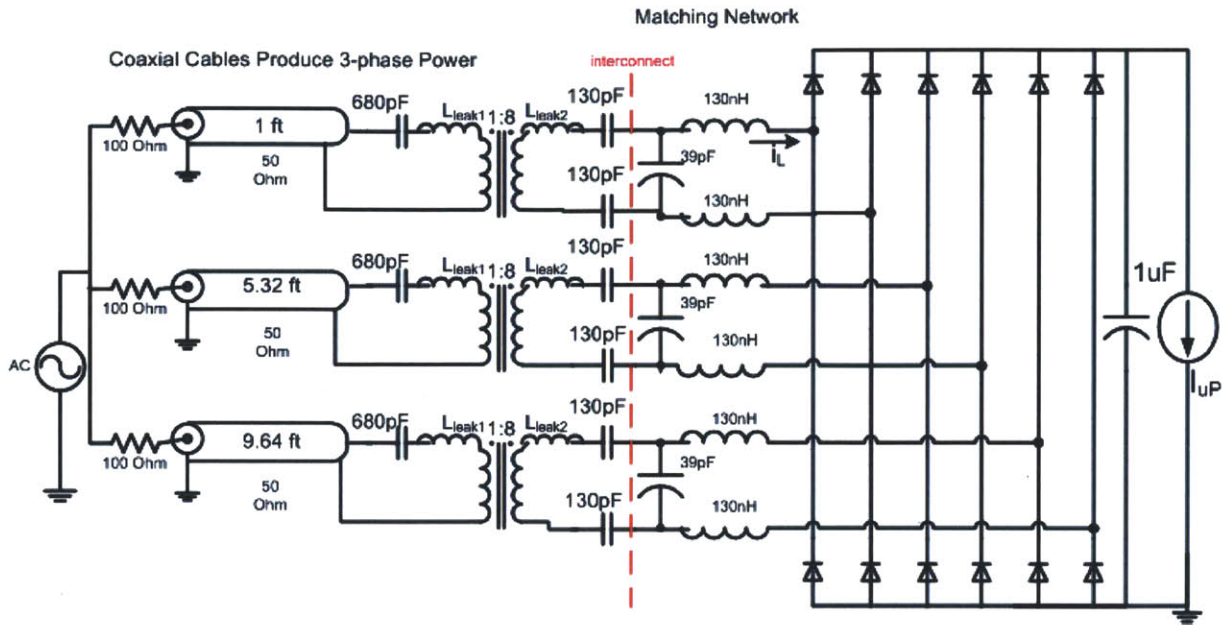


Figure 4.7: Parallel Single Phase Full Bridge Test Schematic

4.2.1 Efficiency

A prediction of the efficiency can be calculated using equation 2.11. From the datasheet, the 130nH Coilcraft Maxi Spring inductor has a quality factor of approximately 100 at 50MHz and the 39pF ATC 700A capacitor has a quality factor of approximately 1000 at 50MHz. The transformation Q_T is $\sqrt{(\frac{3\pi}{2})^2 - 1} \approx 4.6$. The expected efficiency is then calculated as follows:

$$\eta \approx (1 - \frac{Q_T}{Q_L}) / (1 + \frac{Q_T}{Q_C}) = (1 - \frac{4.6}{100}) / (1 + \frac{4.6}{1000}) = 95\% \quad (4.16)$$

4.2.2 Layout

The two three-phase variations were designed on one PCB, a top level of which is shown in the Appendix in figure B.1. The Appendix also shows the EAGLE PCB layout for each layer of the design. Figure 4.8 shows a closeup of the parallel single-phase system. As can be seen in figure 4.8, ground plane area is minimized under or near the matching network and rectifier so as to minimize parasitic shunt capacitance to ground. Also each phase is designed identically

so as to ensure symmetry and ensure balanced three-phase legs. The area between each bridge rectifier and the output capacitance is also made to be as small as possible. That area is a high frequency high current loop and can thus create an inductance. Keeping this areas as small as possible reduces parasitic inductance and ringing at the output.

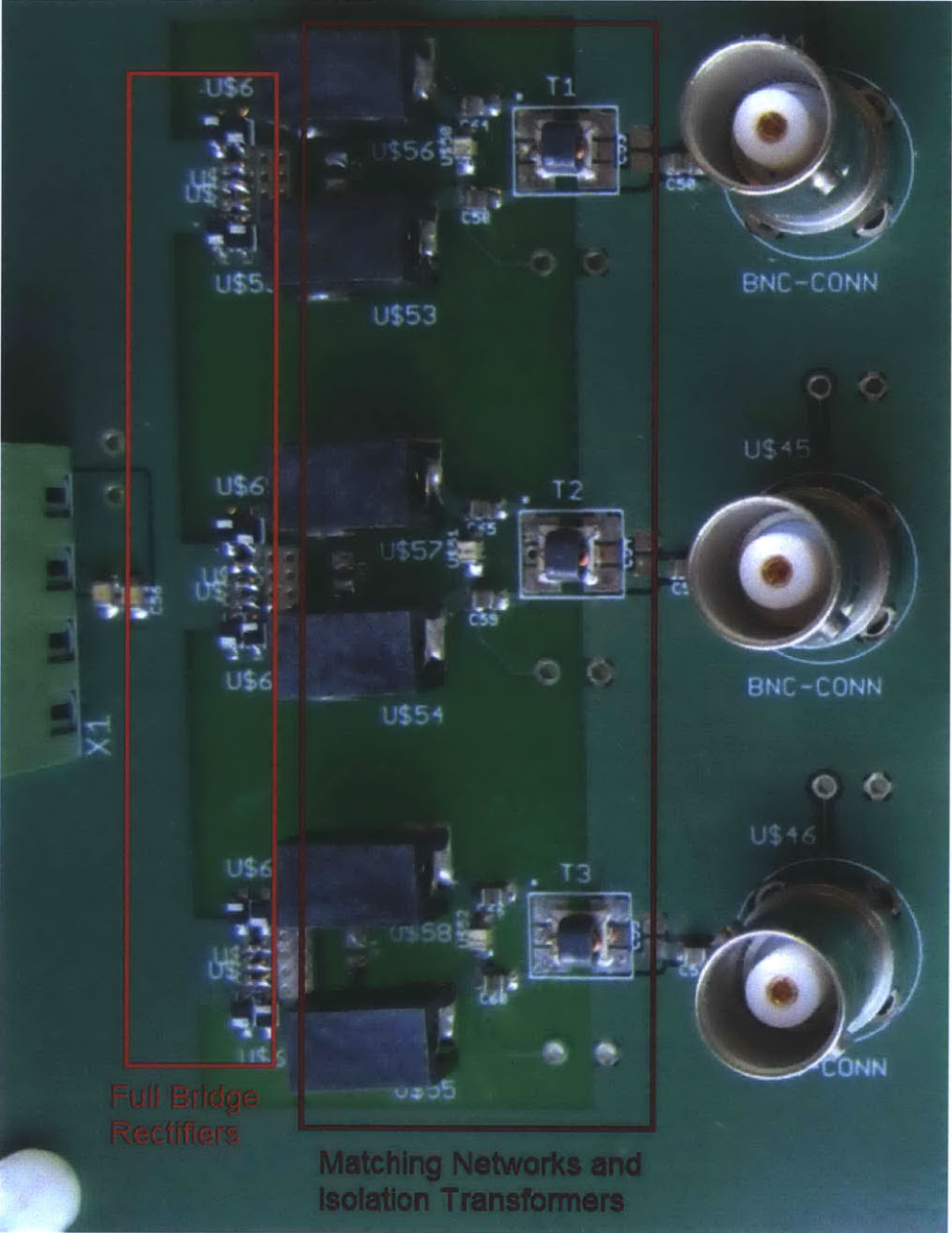


Figure 4.8: Parallel Single Phase Full Bridge Test PCB. A complete schematic with component values and board layout information can be found in appendix B

4.3 Three Phase - Delta-Wye Version

The Delta-Wye System operates at 50MHz with input peak-to-peak line-to-line AC voltage of 24V and the DC output voltage of 2V. Output power is 0.7W, which is limited by the discrete RF transformers. Infineon BAT60A diodes are used for the rectifier since discrete CMOS rectifier having appropriate characteristics were not available. Figure 4.9 shows the schematic of the 3-phase Δ -to- Y impedance matching system. 39pF ATC capacitors and 82nH Coilcraft Midi Spring air core inductors were used to form the three-phase matching network with a $\sqrt{3}\pi : 1$ voltage conversion ratio. The Δ to Y configuration provides a voltage conversion of $\sqrt{3}:1$. The rectifier stage provides an additional fundamental peak-to-peak AC-DC conversion of $\frac{4}{\pi} : 1$. Thus the total overall voltage conversion ratio for the entire system is $\sqrt{3}\pi \cdot \sqrt{3} \cdot \frac{4}{\pi} : 1 = 12 : 1$

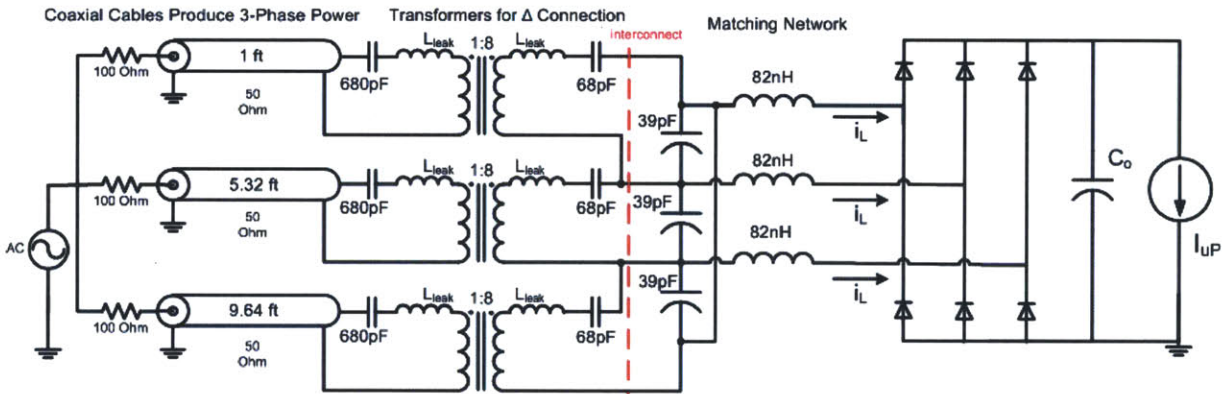


Figure 4.9: Delta-Wye System Schematic

4.3.1 Efficiency

A prediction of the efficiency for the delta-wye system can be calculated similar to that of the parallel single-phase system using equation 2.11. From the datasheet, the 82nH Coilcraft Midi Spring inductor has a quality factor of approximately 90 at 50MHz and the 39pF ATC 700A capacitor has a quality factor of approximately 1000 at 50MHz. The transformation Q_T is $\sqrt{(\frac{\sqrt{3}\pi}{2})^2 - 1} \approx 5.35$ The expected efficiency is then calculated as follows:

$$\eta \approx (1 - \frac{Q_T}{Q_L}) / (1 + \frac{Q_T}{Q_C}) = (1 - \frac{5.35}{90}) / (1 + \frac{5.35}{1000}) = 93.5\% \quad (4.17)$$

4.3.2 Layout

Figure 4.10 shows a closeup of the delta-wye system. The main design consideration for the delta-wye system is to maintain symmetry among each leg of the three phase set. All signal paths and parasitics in each phase must be as equal as possible. The difficulty lies in the geometry of the Δ configuration of the transformers and matching network capacitors. The solution was to form the Δ geometry at the center and lay the matching network inductor and rectifiers radially outward as shown in 4.10. The input signal is transferred through the isolation transformer with C_{match} shunting the secondary, forming the sides of the Δ . L_{match} connect at the vertices. As seen in Figure B.9 of the Appendix, the bottom layer is used as the power plane to collect the output voltage at the rectifier output. Similar to the full-bridge rectifier layout, the output filter capacitance is split up so as to be placed close to the rectifier and minimize the rectifier/capacitor inductance loop. The top layer is used as the ground plane to provide a ground potential for the transformer primary and secondary center-tap.

Chapter 5

Experimental Results

This chapter presents experimental results for the AC power delivery prototype. The measurement and experimental setup is discussed in Section 5.1. Output waveforms for both the Parallel Single-Phase and the Delta-Wye systems are presented in Section 8.2.

5.1 Measurement Setup

A block diagram for the measurement setup is shown in Figure 5.1. The frequency and amplitude of the sinusoidal input voltage is set by the Agilent 33250A 80MHz Function/Arbitrary Waveform Generator. That signal is fed into an Amplifier Research Model 10W1000 power amplifier. The sinusoidal power is sent through a Bird Series 5010 directional power sensor which measures the amount of power reflected back into the power amplifier and the amount of power delivered to the circuit board. The information is read by a Bird Model 5000-EX digital power meter. For measurement, a Tektronix TDS7254B digital phosphor oscilloscope is used along with the Tektronix P6158 20x low capacitance probe. The P6158 is especially designed for high-speed applications so as to not unnecessarily load the circuit under test at high frequency.

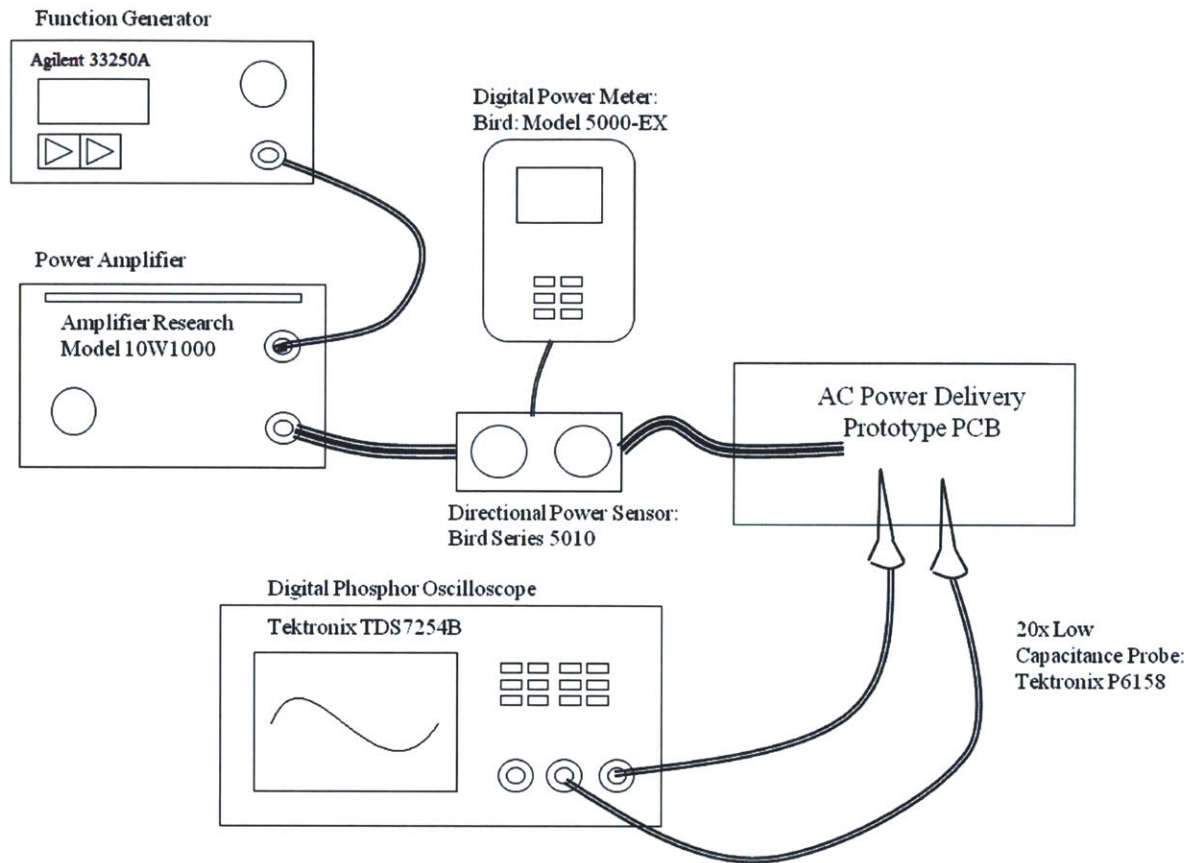


Figure 5.1: Block diagram of measurement setup

5.2 Converter Waveforms

Figures 5.2 to 5.5 shows the experimental waveforms of the three-phase systems described in Chapter 4. Both three-phase systems in Figure 5.2 and 5.3 show the same 3-phase $24 V_{pp}$ line-to-line voltages AC input voltage and 2V DC output voltage. The full bridge rectifiers in the parallel single-phase system show the positive and negative V_o swing on the input of the rectifier. The Y-connected three-phase rectifier in the delta-wye system show only ground to V_o swing on the input of the rectifier.

In addition, the line-to-neutral voltage of the two AC systems are shown in Figures 5.4 and 5.5. The parallel single phase system shows 6V line-to-neutral input voltages, and the three-

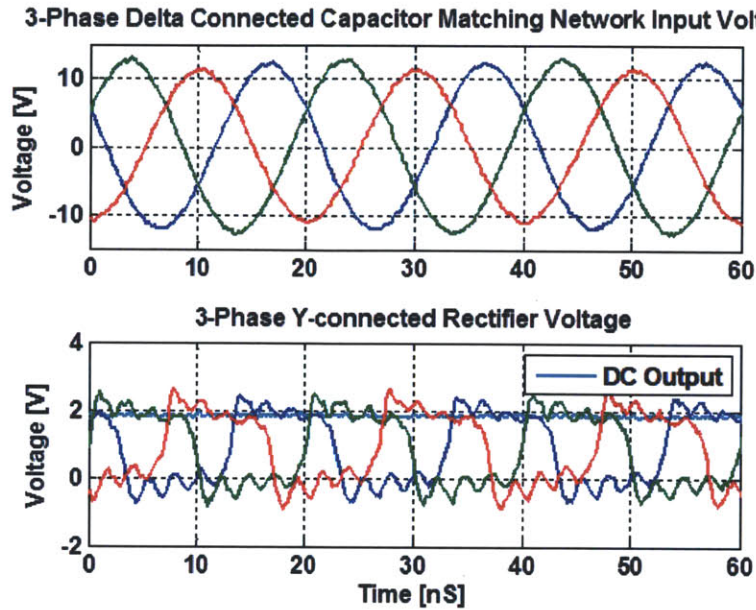


Figure 5.2: Resulting Line-Line Voltage Waveforms for Delta-Wye System

phase matching network with Δ connected capacitors shows 7V ($12V_{pk,line-line}/\sqrt{3} = 6.928V_{pk}$) line-to-neutral AC voltage on the input due to the Δ connection.

The measured overall system efficiency is about 70% for the three-phase system with parallel single-phase matching networks and about 63% for the three-phase delta-wye system. This matches the calculated performance (estimated transformer efficiency is 93%, matching network efficiency is about 95% for the single phase and 93.5% for the delta network, and the rectifier efficiency is about 80% for the full bridge and 75% for the three-phase bridge).

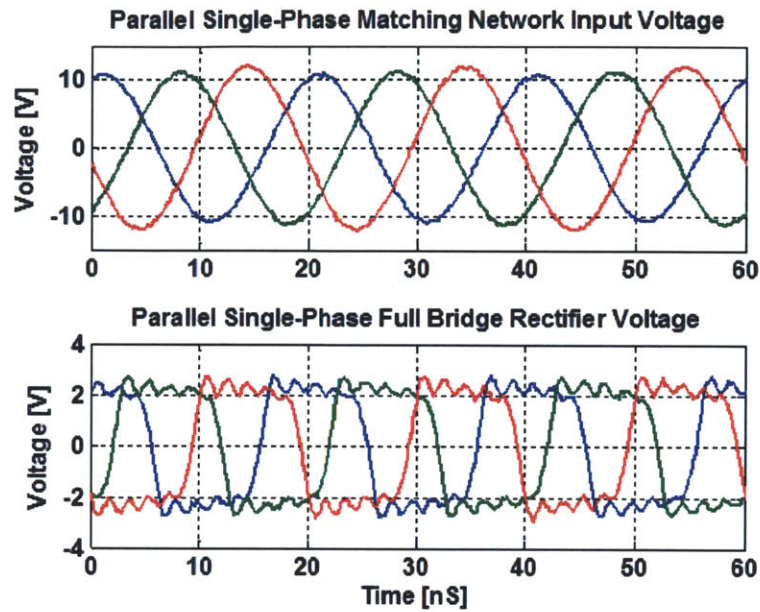


Figure 5.3: Resulting Line-Line Voltage Waveforms for Parallel Single Phase System

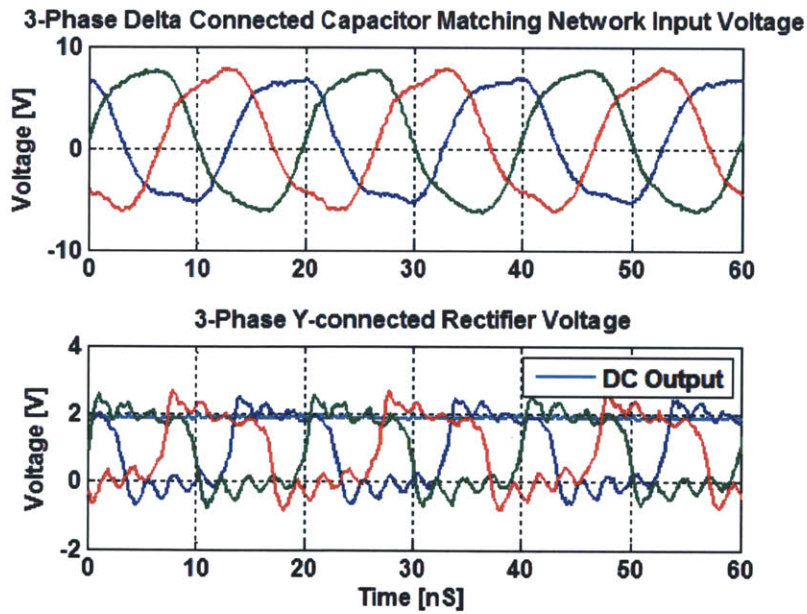


Figure 5.4: Resulting Line-Neutral Voltage Waveforms for Delta-Wye System

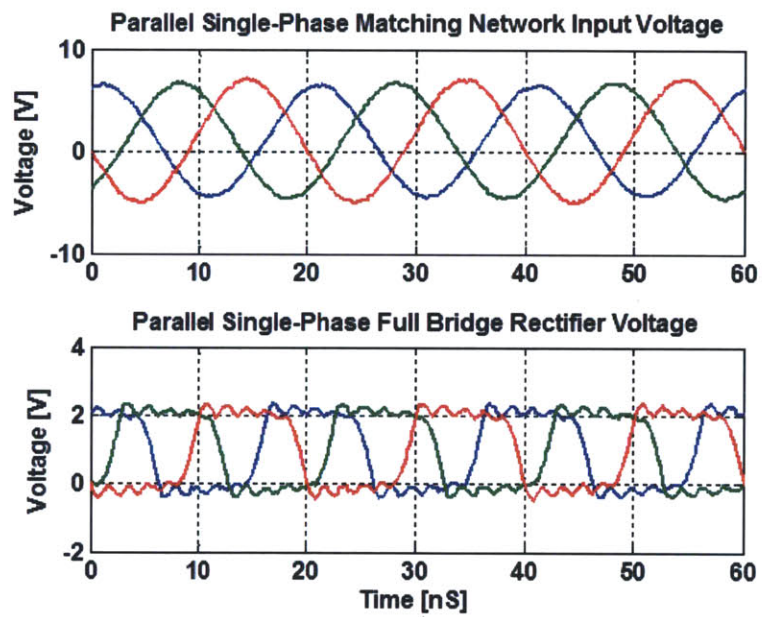


Figure 5.5: Resulting Line-Neutral Voltage Waveforms for Parallel Single Phase System

Chapter 6

Summary and Conclusions

6.1 Thesis Summary and Contribution

This thesis presents an AC power delivery architecture for low-voltage electronics. Analysis reveals that such a system is feasible, and that polyphase RF power delivery is advantageous. A discrete prototype at 50MHz has been designed and built to demonstrate and verify the concept. With the AC power transformation and rectifier stage on die, this architecture has the potential to not only help reduce pin count and interconnect loss for microprocessors, it is also suitable for other portable electronics and applications where high power density is desired.

6.2 Future Work

Although this Master's thesis focused on a discrete prototype, the target application is power delivery for integrated low voltage circuits. An integrated implementation of the entire system including, matching network, bridge rectifiers, switched-capacitor rectifier, and control circuitry is currently being pursued by Doctoral Candidate Wei Li. The integrated rectifier is being designed in a TSMC 0.25um process. The target output voltage is 2.5V operating at 50MHz switching frequency. The integrated system is being designed to output 2W per phase for a total of 6W and is to be reconfigurable as a three-phase bridge rectifier or into

three separate full-bridge rectifiers. The integrated full-bridge switched-capacitor rectifier is designed for a 4W output power.

Further work can be done to implement an integrated inverter stage. GaN power devices have been developed that offer fast, high-voltage switching with close integration with CMOS devices. The architecture considered in this thesis is directly applicable to the design of a GaN-Si DC-DC converter.

Appendix A

Voltage Controlled Delay Circuit for IC

The target application for this architecture are integrated low voltage circuits. The full system integrated implementation is being pursued by Doctoral candidate Wei Li. As part of the control system, a variable delay circuit is needed to tune the switching cycles for the CMOS rectifier. A low voltage, low-power CMOS delay element based on [18]. The circuit explored is based on a CMOS thyristor concept and offers variable delay based on a control current. The circuit claims to offer negligible static power, low dynamic power consumption, and operation at low voltage. In [18] a prototype delay element was demonstrated with a 0.8 μ m process and claims a delay range of 2.6ns to 76.3ms. Thus, this topology is very suitable for our requirements and was explored as a possible delay circuit. The integrated circuit is to be designed in a TSMC 0.25 μ m process and is to have a delay range from 0ns to 10ns, ie. 0 to a half a switching period.

Figure A.1(a) shows a simplified half circuit operation of the delay element, demonstrating its similarity to a thyristor. Figure A.2 shows a more complete schematic of the delay element with static triggering. The output is taken at either Q or \bar{Q} . The delay time is controlled by a current source which can be implemented using a voltage controlled current source as shown in Figure ??(b). The current source is based on a typical temperature compensated

current source whose current is determined by a resistor [22]. The circuit is made to be voltage controlled by implementing the resistor with a transistor operating in the triode region.

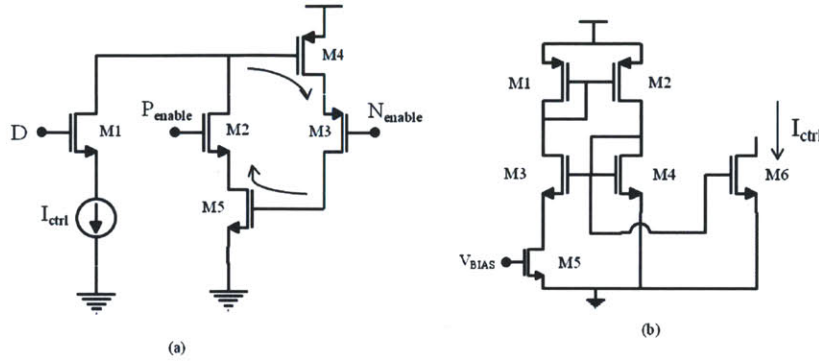


Figure A.1: Thyristor variable delay concept. (a) Half-circuit of the delay element. (b) Linear FET control current implementation

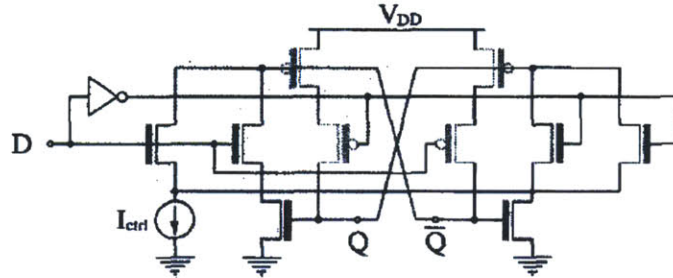


Figure A.2: Thyristor variable delay circuit with static triggering. Taken from [18]

A design was simulated using the Cadence environment with a TSMC 0.25um process. The delay was measured at V_{ctrl} increments of 0.1V and is plotted below. Although promising, the topology is very sensitive to stray parasitics and temperature. At 50MHz, the regeneration time of the thyristor approached the few nanoseconds which resulted in unreliable delay times. Once layed out, parasitic capacitances and resistances affected the delay time and overall operation greatly. Thus, a simpler delay topology requiring additional analog-to-digital converters was used for the integrated design which will be discussed in Li's Doctoral thesis.

Appendix B

PCB Layout

This appendix provides images of the PCB layout for the converter prototype. The PCB layout was made using EAGLE Layout Editor from Cadsoft Computer, Inc. Also included are the final EAGLE schematics associated with the PCB layouts.

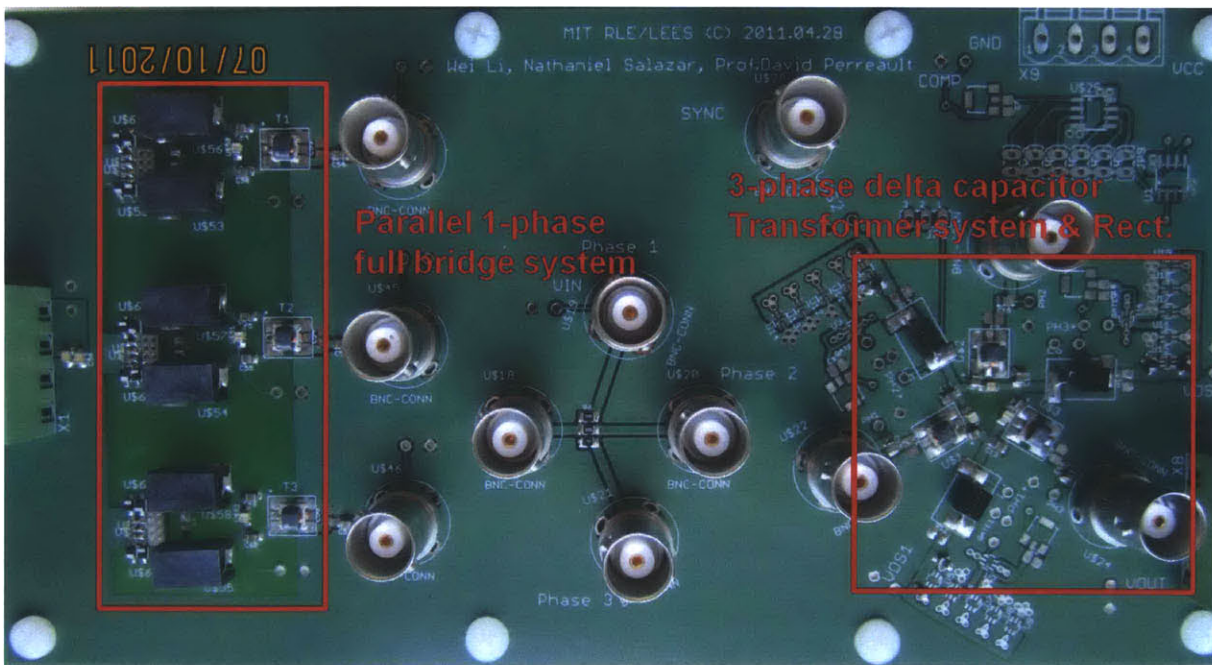


Figure B.1: Prototype PCB of both the Parallel Single-Phase and Delta-Wye Systems

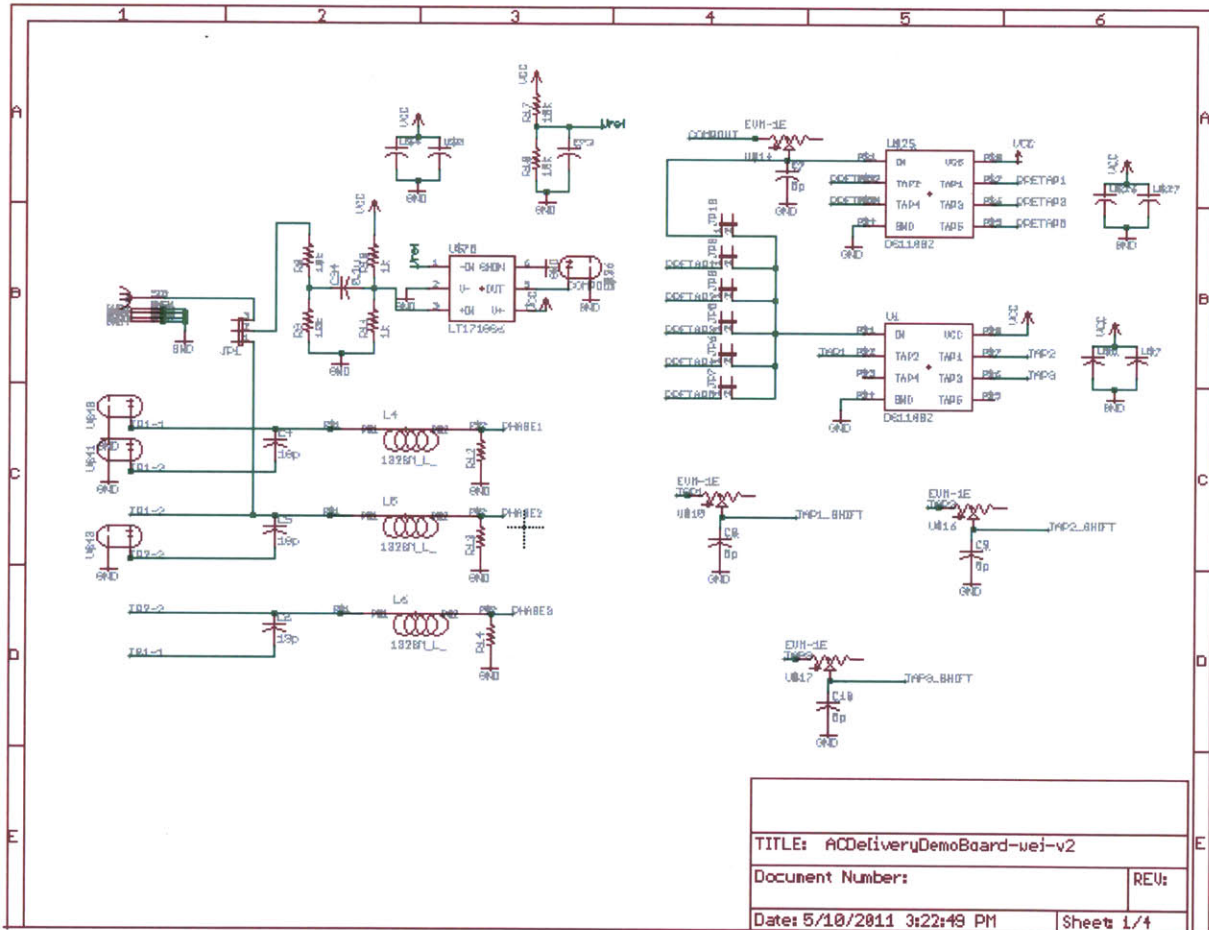


Figure B.2: Eagle schematic for Delta-Wye System including control and drive circuitry for CMOS rectifier option

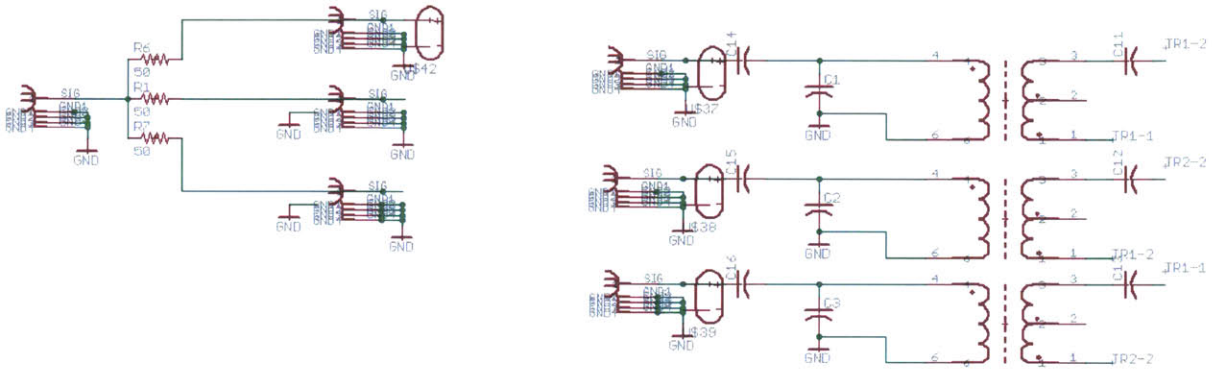


Figure B.3: Coaxial BNC Connectors and Transformer for Delta-Wye System Eagle Schematic

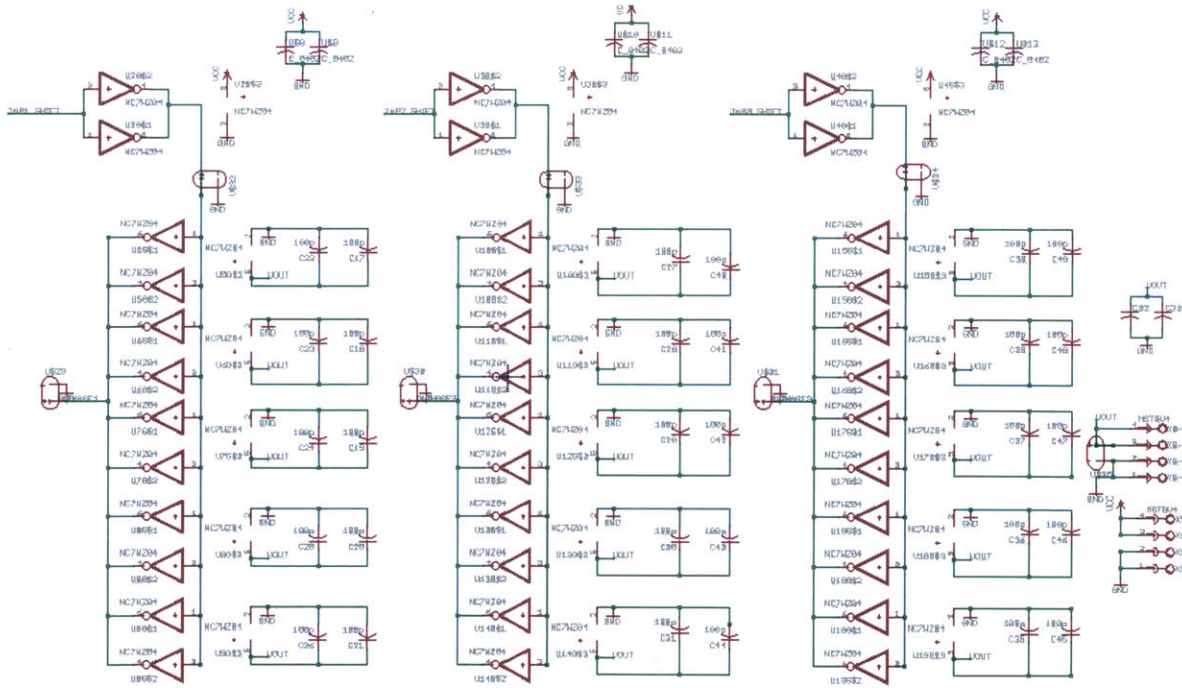


Figure B.4: CMOS Inverter Rectifier Option Eagle Schematic

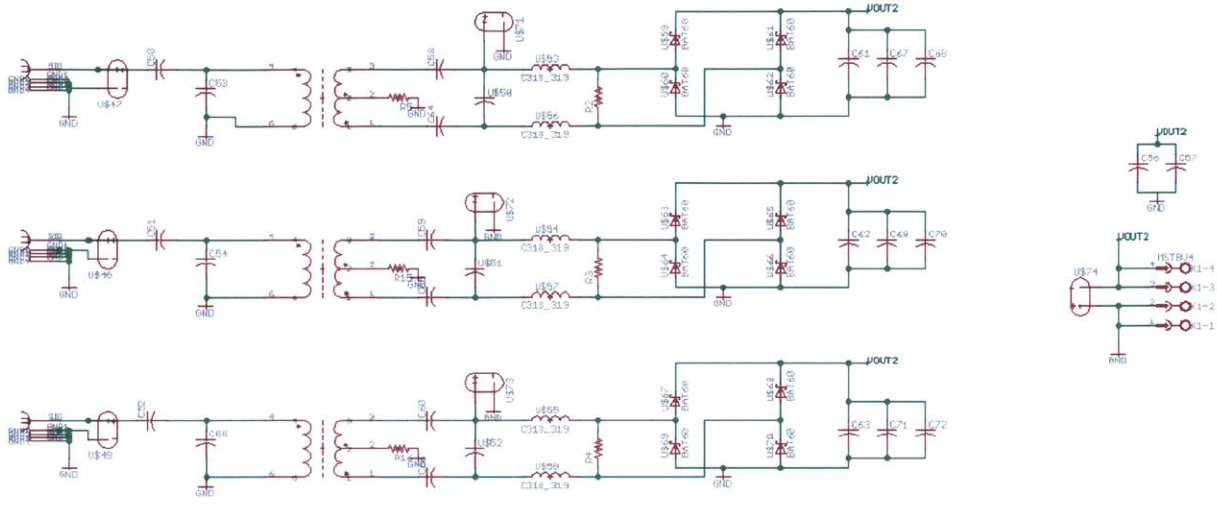


Figure B.5: Three Phase - Parallel Single-phase System Eagle Schematic

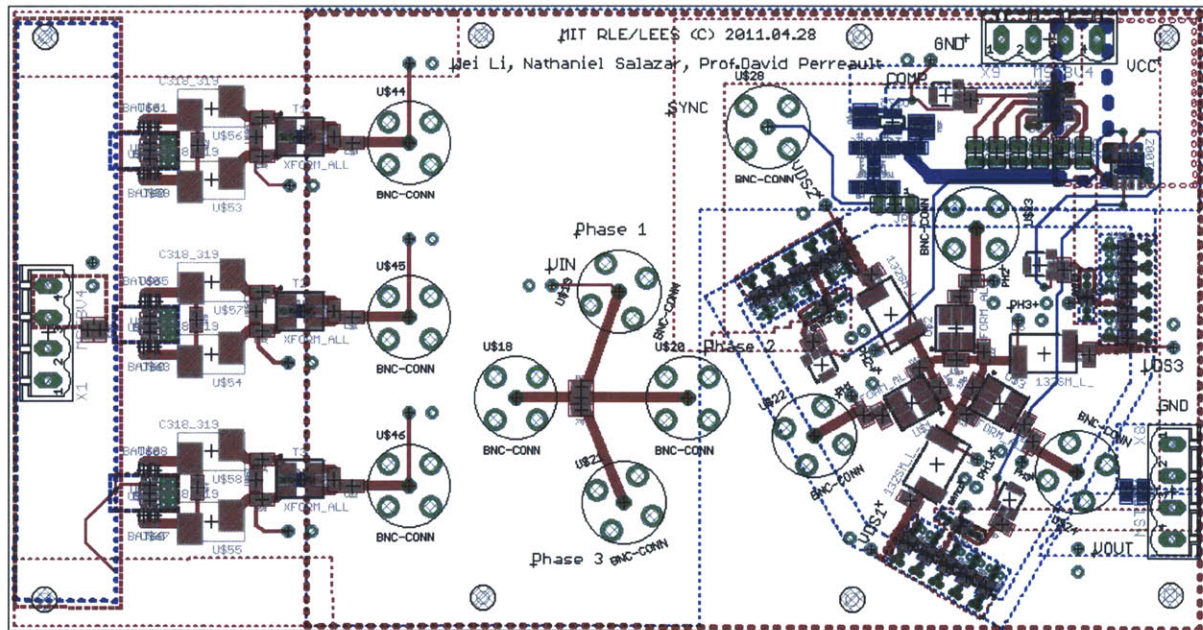


Figure B.6: Prototype PCB Layout

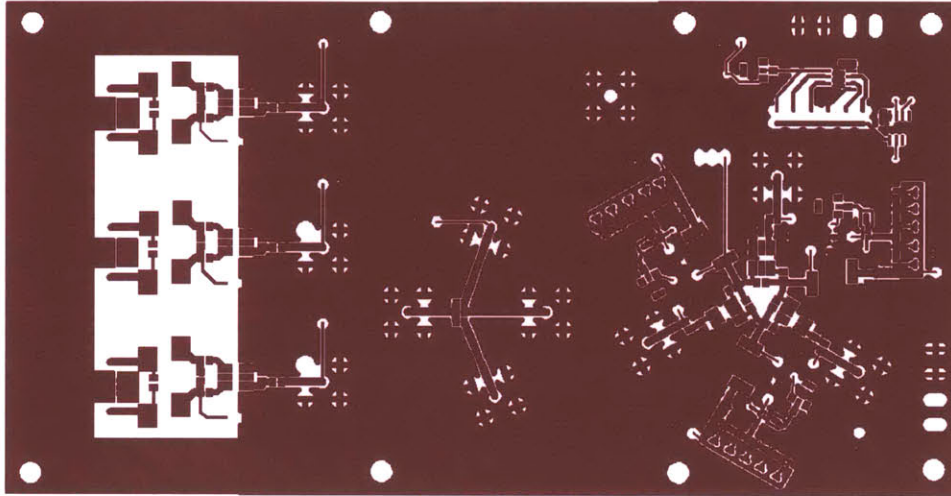


Figure B.7: Prototype PCB, top side

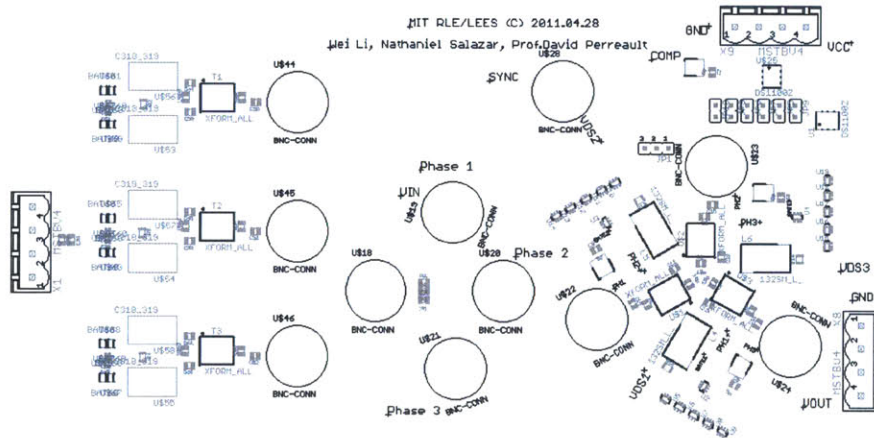


Figure B.8: Prototype PCB, top silkscreen

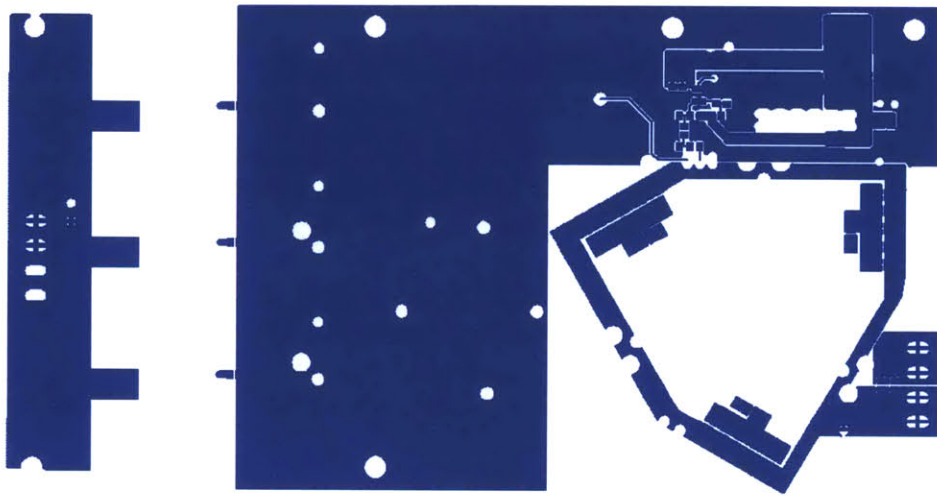


Figure B.9: Prototype PCB, bottom side

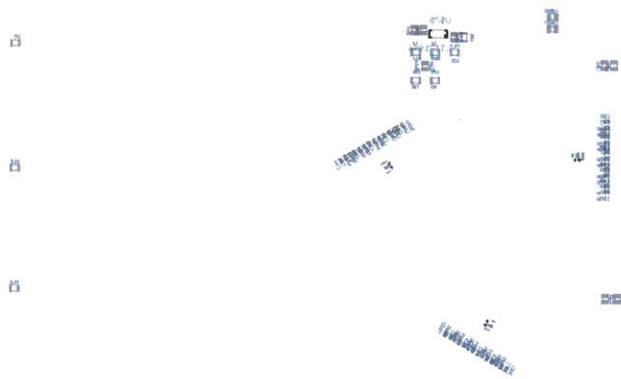


Figure B.10: Prototype PCB, bottom silkscreen

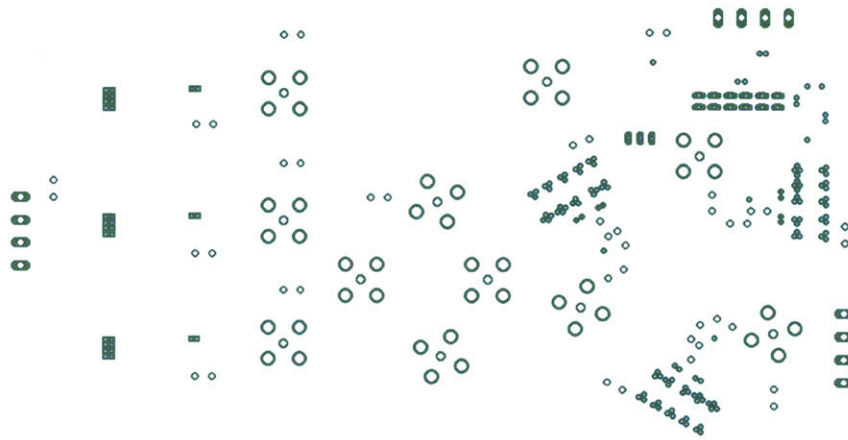


Figure B.11: Prototype PCB, pads and vias

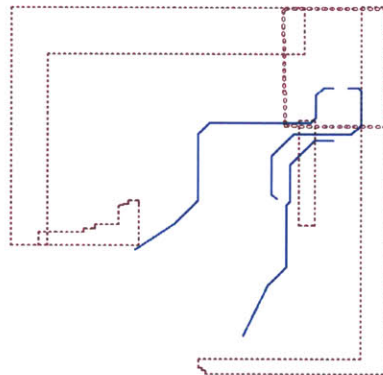


Figure B.12: Prototype PCB, layers 2 and 3

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