High Efficiency Resonant dc/dc Converter for Solar Power Applications

by

Wardah Inam

B.S., GIK Institute of Engineering Sciences and Technology (2010)

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2013

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Abstract

This thesis presents a new topology for a high efficiency dc/dc resonant power converter that utilizes a resistance compression network to provide simultaneous zero voltage switching and near zero current switching across a wide range of input voltage, output voltage and power level. The resistance compression network maintains desired current waveforms over a wide range of voltage operating conditions. The use of on/off control in conjunction with narrowband frequency control enables high efficiency to be maintained across a wide range of power levels. The converter implementation provides galvanic isolation and enables large (greater than 1:10) voltage conversion ratios, making the system suitable for large step-up conversion in applications such as distributed photovoltaic converters.

Three 200 W prototypes were designed, built and tested. The first prototype was made as a proof of concept and operated at a switching frequency of 100 kHz. It had an efficiency of 93.5% (at 25 V input and 400 V output). The second prototype was operated at a switching frequency of 500 kHz and had an efficiency of 93% (at 25 V input and 400 V output). The high frequency losses caused by the ringing in voltage and current due to the resonating parasitics of the transformer were removed with the help of a matching network in the third prototype. This final prototype operated at a switching frequency of 500 kHz and showed that over 95% efficiency is maintained across an input voltage range of 25 V - 40 V (at 400 V output) and over 93.7 % efficiency across a wide output voltage range of 250 V - 400 V (at 25 V input). These experimental results demonstrated the effectiveness of the proposed design.

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Acknowledgement

I want to thank my advisors Prof. Perreault and Prof. Afridi for their guidance and constant encouragement. I looked forward to the weekly meetings because not only did I learn a lot in them but also because the discussions were highly valuable in chalking out what needed to be done. I would also like to acknowledge Masdar Institute for funding this project.

Moreover, I want to thank my group mates Alex Jurkov, Seungbum Lim, Wei Li, Minjie Chen, Anthony Sagneri, Brandon Pierquet, Jackie Hu, David Giuliano and John Ranson for helping me out whenever I asked for it and also for letting me borrow their test equipment.

My lab mates Shahriar Khushrushahi, Richard Zhang, David Jenicek, Kendall Nowocin, Samantha Gunter, Juan Santiago, Sam Chang, Uzoma Orji, Muhammad Araghchini, Jouya Jadidian, Jiankang Wang for making the work place fun. Also, I want to especially thank all my friends who have always been there for me.

Finally, I want to thank my family for all their love and support. My parents have always tried to handle everything for me and I have never had to worry about much because of them. I cannot thank them enough for all they have done for me. Also, I want to sincerely thank my sisters who I have always counted on for laughter and support.

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Chapter 1

Introduction

The power electronics community is constantly striving towards developing higher power density and higher efficiency converters. High power density is achieved by operating converters at a high switching frequencies; this reduces the numerical values of the passive (filtering) components, and - ideally- their size. High efficiency is achieved by utilizing switching topologies with ideally lossless passive components (in reality these components are not lossless). In order to have high efficiency a trade-off between conduction and switching loss has to be made in order to minimize the total loss. Soft switching reduces the switching loss by utilizing Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) techniques, which greatly reduce the overlap of current and voltage waveforms at switching transitions. Conduction loss is reduced by using devices with low effective resistance and by selecting topologies that require relatively low (average and RMS) currents to process a given amount of power.

In recent years, many advances have been made in the materials and fabrication technologies of the power devices being used in power converters. These advances have resulted in lower loss and smaller devices. For example, Gallium Nitride and Silicon Carbide devices which have recently become commercially available offer many advantages compared to the conventional Silicon devices.

In power converters, transistors are mostly used as the active switches. They have conduction loss in the on state and switching loss during the switching transitions. Diodes are used as uncontrollable switches (e.g., for rectification). They exhibit both conduction loss and switching loss. Capacitors and inductors are used as energy storage devices. They are ideally lossless components but have losses due to parasitics. Transformers are used to step up or step down the voltage. These are also ideally lossless, but in practice exhibit core loss and winding loss. In a high efficiency converter, all these losses have to be reduced to the maximum extent possible, and the contributions of various loss mechanisms trade off against each other to achieve overall minimum loss.

1.1 Motivation and Previous Work

High-voltage-gain dc/dc converters are found in a variety of applications. For example, to connect photovoltaic panels to the grid, interface circuitry is needed. Some architectures for this purpose incorporate dc/dc converters to boost voltage of individual photovoltaic panels to a high dc-link voltage, with follow-on electronics for converting dc to ac (e.g., [1, 2]). The step up dc/dc converter is a critical part of this system, and must operate efficiently for a large voltage step up and for a wide voltage range (e.g., at the converter input and/or output depending upon the system). Furthermore, to be compact it must operate at high switching frequencies. In conventional hard-switched power converters, the overlap of current and voltage is large during switching, resulting in significant power loss, especially at high frequencies. When the frequency is increased this loss quickly becomes the dominant loss in the converter. Soft switched resonant converter topologies providing Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) can greatly reduce loss at the switching transitions, enabling high efficiency at high frequencies (e.g., [3,4]). Unfortunately, while many soft-switched resonant designs achieve excellent performance for nominal operating conditions, performance can degrade quickly with variation in input and output voltages and power levels. Limitations on the efficient operating range of resonant converters are tied to both converter structure and control.

Numerous control techniques are possible for compensating variations in input voltage, output voltage, and power level. These include frequency control [3,4], phase-shift PWM control [5], asymmetric duty cycle PWM control [6], and on-off or "burst" control [7]. Each of these control techniques – in conjunction with conventional resonant tank structures – imposes significant design limits. For example, the conventional Series Resonant Converter (SRC) [4] requires wide-band frequency variation to control the power when the load or input voltage varies such that the magnetics cannot be optimally designed. To maintain zero-voltage switching the frequency must increase to reduce power, hurting the efficiency at light load. For a full-bridge version of the SRC, phase-shift control can be used to control the power and reject conversion ratio variations (e.g., [5]). However, this results in asymmetrical current levels in the switches at the switching instants, with the switches in the leading leg turning off at high currents. The effective impedance of the rectifier in a resonant converter also often causes challenges, as effective rectifier impedance varies with operating conditions.

This thesis introduces a new high-efficiency resonant dc/dc converter topology that seeks to overcome the above-mentioned challenges. This converter operates with simultaneous zero-voltage switching and near

zero-current switching across a wide range of input voltage, output voltage and power levels, resulting in low switching losses.

1.2 Research Background

The dc/dc converter consists of an inverter, a transformation stage and a rectifier stage as shown in Figure 1.1.

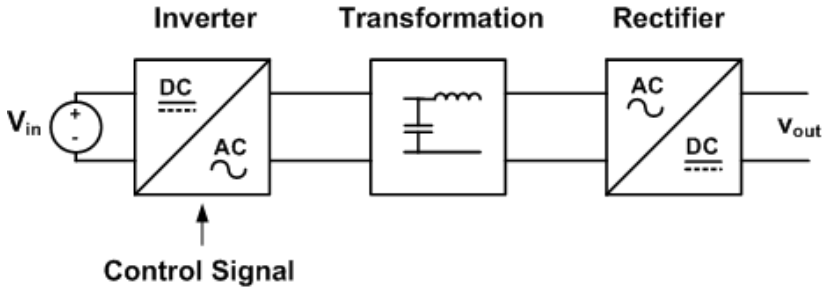


Figure 1.1: Architecture of proposed dc/dc converter

This soft-switched behavior (with both ZVS and near ZCS) is a key advantage of the proposed architecture. In conventional circuits without such measures, switching loss can become an important circuit loss. For example, if a transistor is turned on under voltage, the energy stored in the switch capacitance is dissipated as heat in the switch. Moreover, as illustrated in Figure 1.2, because the switching transition is not instantaneous, there is overlap during which both transistor voltage and current are high as it transitions from high voltage to low voltage and zero current to high current. A similar overlap loss exists at switch turn-off.

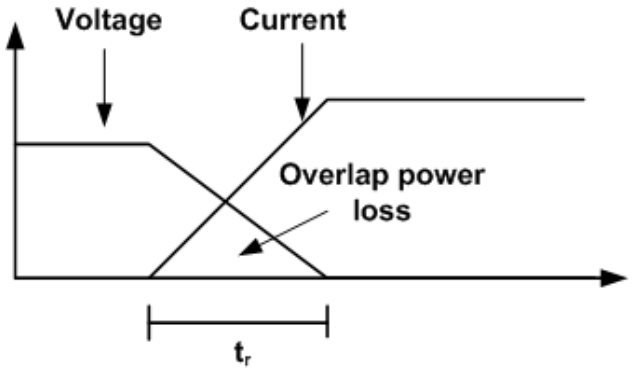


Figure 1.2: Power loss due to the overlap of current and voltage at turn-on

In the topology presented here, the switching loss is reduced by providing zero-voltage switching at both turn-on and turn-off, and near-zero-current switching at both switching instants. This eliminates capacitive discharge loss at switch turn-on (as switches do not turn on under voltage) and provides near zero overlap loss, as both current and voltage are low during the switching transition.

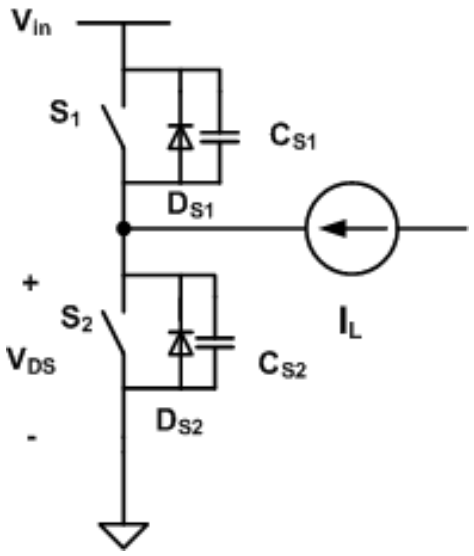


Figure 1.3: Schematic of an inverter leg to illustrate soft switching

To understand this, consider the half bridge shown in Figure 1.3, where the inductor is modeled as a current source. Here each MOSFET has been modeled as a parallel combination of a switch, a diode, and a capacitor. Suppose the top switch (S_1) is conducting and the bottom switch (S_2) is off, and we need to transition in to the opposite state. First the top switch is turned off while there is current flowing in the inductor. The top switch will turn off under zero voltage due to the snubbing action of capacitor C_{S1}. Before the bottom switch is turned on there is a period of time when both switches are off, called "dead time". Since the current in the inductor cannot change instantaneously, it will discharge the bottom capacitor C_{S2} as long as the current in the inductor is negative. Once the capacitor is discharged and the voltage across it is zero the diode D_{S2} will start to conduct at this instant the switch S_2 is turned on under zero voltage. If the switch is turned on before the capacitor V_{DS} is fully discharged it will discharge through the switch and cause resistive loss. The energy loss is directly proportional to the frequency of switching and the output capacitance of the transistor and is given by:

$$E_{on} = \frac{1}{2} C V^2 f \tag{1.1}$$

At turn-off the current through the transistor does not instantaneously drop to zero. As the current is decreasing the voltage starts to rise and this overlap causes power loss. For Zero Current Switching the current in the switch should be zero before the switch is turned off. Figure 1.4 shows sinusoidal current flowing through the inductor.

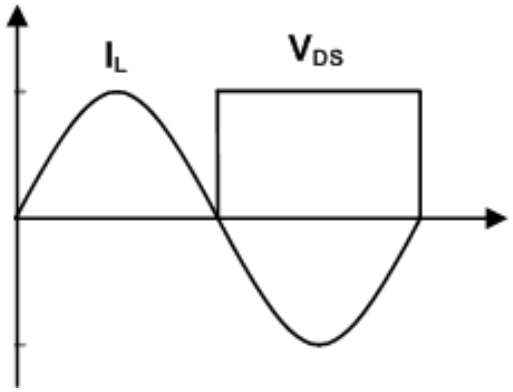


Figure 1.4: Current in the inductor and voltage across the bottom switch are in phase

For ZCS the current should be in phase with the voltage i.e. the network input should look resistive to the half bridge. However, to obtain ZVS at turn on the current has to be non zero and negative thus we cannot have both ZVS and ZCS at the same time. To minimize the switching loss at both transitions we have to operate with ZVS and near ZCS, i.e. the current in the switch is almost zero before it is turned off. Minimum loss is achieved by having enough current to charge/discharge the capacitors during the turn on transition but small enough to obtain near ZCS.

1.3 Contributions and Organization of the Thesis

The goal of this thesis is to design, build and test a new dc/dc converter topology providing high efficiency over a wide input voltage, output voltage and power range at high frequency. This converter operates with simultaneous zero-voltage switching and near zero-current switching over its entire operating range, resulting in low switching losses.

The application chosen to test this dc/dc converter prototype is a two stage grid connected photovoltaic power converter as shown in Figure 1.5. The focus of the thesis is only on the dc/dc converter. The application provides the design specifications for the prototype.

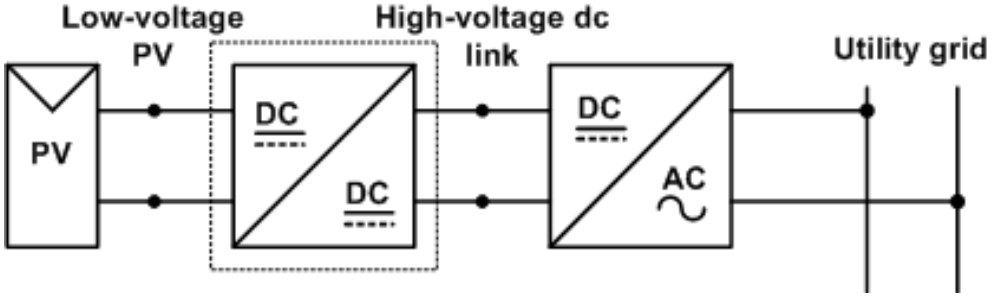


Figure 1.5: Block diagram of a grid-connected PV system

The specifications for the designed dc/dc converter are:

- Input Voltage Range: 25 V - 40 V
- Output Voltage Range: 250 V - 400 V
- Power Range: 20 W - 200 W

The remainder of this thesis is organized as follows.

In Chapter 2, the new topology is introduced. The operation of each stage of the converter (inverter, transformation and rectifier stage) is discussed and the operating benefits of the topology are described.

In Chapter 3, the first prototype of the proposed topology is introduced. This prototype works at 100 kHz switching frequency and is used as a proof of concept. This chapter includes the detailed design strategy of how the various elements of the approach are selected. It also includes the design of the components used in the converter. Moreover, the experimental results for the prototype are presented.

In Chapter 4, the second prototype of the proposed converter is introduced and discussed. It highlights the design at a higher frequency (500 kHz). Experimental results are presented that illustrate some undesirable effects. These limitations are removed in the final prototype.

In Chapter 5, the final prototype is presented. This overcomes some of the problems faced with the first two prototypes and the design changes are discussed. It also shows the experimental results highlighting the advantages of using this particular topology.

Chapter 6 summarizes the lessons learned and advantages of the new topology. It concludes with future research directions.

In the Appendices, experimental results, code for the design of various components, the circuit simulations, and the layout files for the experimental prototypes are provided.

Chapter 2

Resistance Compression Network Converter

In this thesis we introduce a new topology for a dc/dc resonant power converter which utilizes a resistance compression network (RCN) to provide soft switching (ZVS and near ZCS) over a wide input voltage, output voltage and power range. The circuit topology naturally provides desirable waveform shaping over the input and output voltage range. The converter operates at nearly fixed frequency, varying frequency over a narrow band (from 425 kHz to 500 kHz), i.e., a ratio of 1.176 to limit maximum delivered power. Output power control is dominantly achieved through on-off control at a frequency far below the switching frequency.

In this chapter the individual blocks making up the converter are discussed, the function and the purpose of each component is analyzed. The detailed design will be provided in the next chapter.

The proposed topology has two variants. The first topological variant is used in the first and second prototype. This is presented in Figure 2.1. It consists of a full-bridge inverter (S_1-S_4), a transformer for voltage step up and isolation, two series resonant tanks (L_r, C_r and L_{r2}, C_{r2}) [4] for filtering purposes, a resistance compression network (L_s and C_s) [8,9] which limits the power flow to the output in a desirable manner as the voltage conversion ratio varies, and a pair of diode half-bridge rectifiers.

However, in this design the parasitic leakage inductance of the transformer undesirably rings with its secondary side winding capacitance at the switching transitions, creating large ringing in the current and voltage waveforms and high-frequency losses. If the transformer can be made with small parasitics this topology can be used successfully.

To avoid this ringing, a second topological variant is introduced. This is shown in Figure 2.2 and is used in the final prototype converter. It consists of a full-bridge inverter (S_1-S_4), a matching network (L_{rp} and C_{rp}) [10] to act as a filter and also to provide a voltage gain, a transformer, a

resistance compression network (L_s and C_s), a series resonant tank (L_r and C_r), two dc blocking capacitors (C_{DC}) and a pair of diode half-bridge rectifiers.

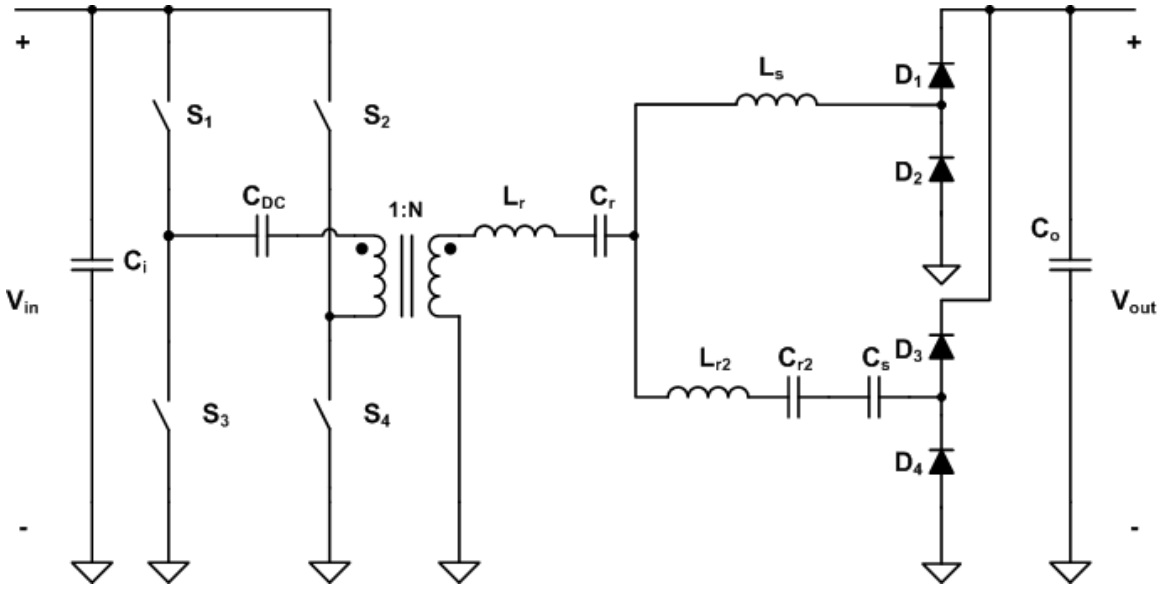


Figure 2.1: Topology of the first variant of the proposed RCN converter. This variant was used in first prototype converters

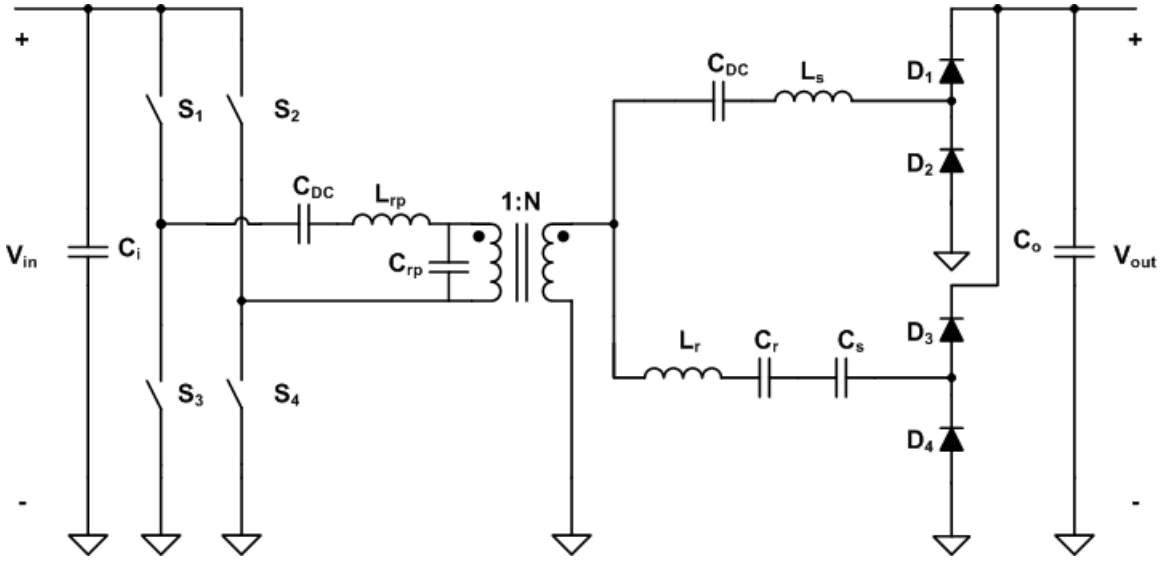


Figure 2.2: Topology of the second variant of the proposed Resistance Compression Network (RCN) converter

This chapter examines each portion of the converter and discusses the different design options for the transformation stage while highlighting the implications of the final design. The inverter stage and rectifier stage are discussed first, followed by a discussion of the transformation stage. Following this, we describe the control approach used in the converter.

2.1 Inverter Stage

The inverter stage consists of a full-bridge inverter as shown in Figure 2.3. It consists of two legs each with a pair of switches. Each switch can be a single transistor or multiple transistors in parallel. The switches are driven by gate drivers that are controlled by a microcontroller.

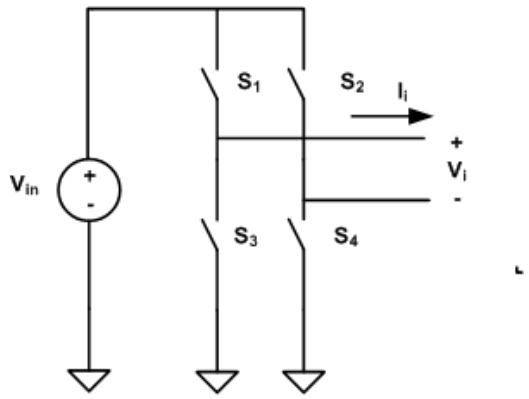


Figure 2.3: Full bridge inverter

A dc voltage V_{in} is applied to the input of the full-bridge inverter. The output V_i is a square wave of $\pm V_{in}$ as shown in Figure 2.4. This large gain is valuable as we are designing a high gain dc/dc converter. In a half-bridge inverter (with a pair of capacitors in one leg) the voltage output varies from $\pm V_{in}/2$ so it does not provide as large an ac output voltage.

The main handle for power control is on-off control (i.e., by gating the converter on and off at a modulation frequency that is much lower than the switching frequency [2,11]). Narrow band frequency control is used to limit the variation in maximum power when the input voltage varies.

The two switches in each leg are driven by 50% duty ratio square-pulse waveforms that are 180° out of phase with each other. The two legs are driven with 180° phase difference. So the inverter outputs a 50% duty ratio square wave. Switch S_1 and S_4 are turned on at the same time for approximately half the switching cycle. Before S_2 and S_3 are switched on there is a period of

'dead-time' where all the switches are off. This eliminates the possibility of both switches in a single leg turning on simultaneously and shorting the input source. It also provides adequate transition time for zero-voltage turn on of switches to be achieved. After this short dead-time (usually 1% of the switching cycle) S_2 and S_3 are switched on. The resonant components following the inverter shape the current to an approximately sinusoidal waveform as shown in Figure 2.4. In the actual converter the current leads the voltage slightly in order to get ZVS.

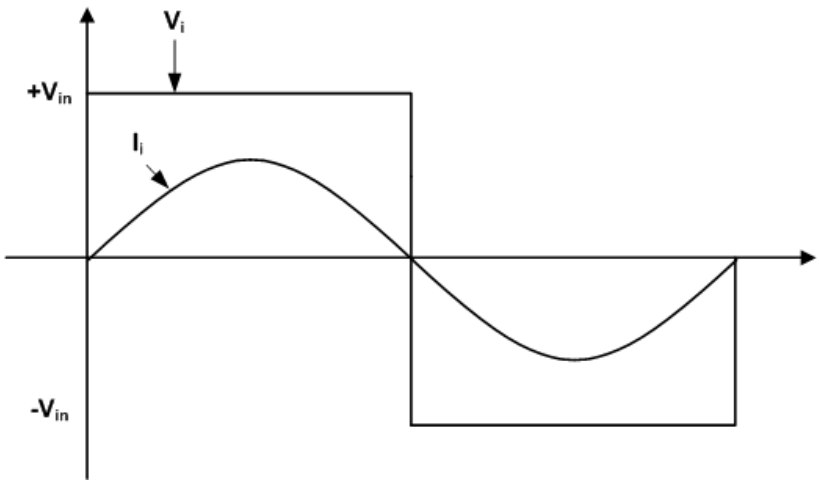


Figure 2.4: Inverter output voltage and current

2.2 Rectifier Stage

At the switching frequency (fundamental frequency) the half-bridge rectifiers can be modeled as equivalent resistors, as shown in Figure 2.5. Their effective resistance is given by [9]:

$$R_L = \frac{4V_{out}^2}{\pi^2 P} \tag{2.1}$$

where V_{out} is the converter output voltage and P is the switching-cycle-average power processed by an individual rectifier. The fundamental harmonic of the voltage is in phase with the current and this transfers the power as illustrated in Figure 2.6. The diode capacitance has been ignored in this simplified analysis.

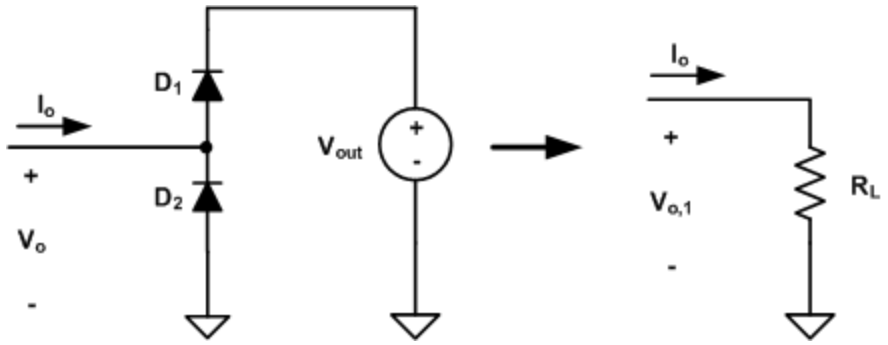


Figure 2.5: Half-bridge inverter implemented with a pair of diodes and the equivalent fundamental harmonic model

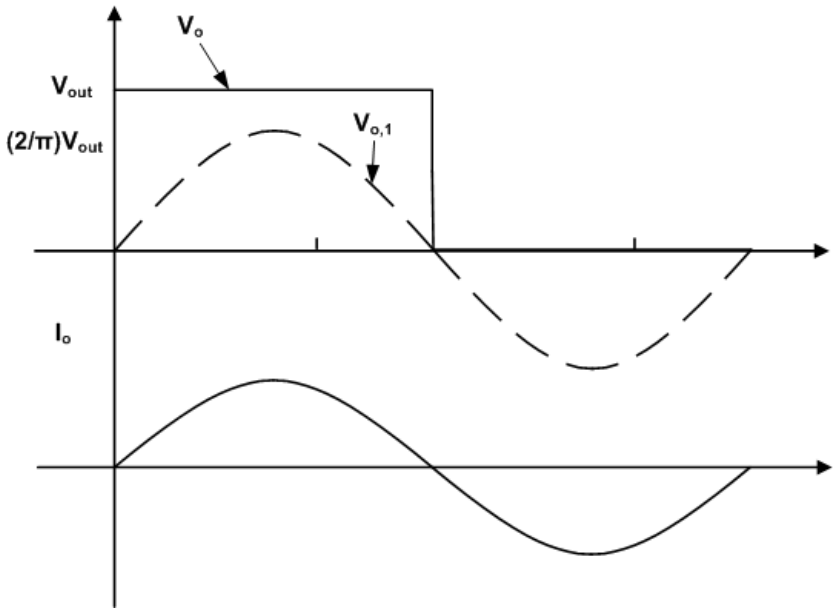


Figure 2.6: Voltage and current waveforms at the rectifier input. The fundamental component of the rectifier input voltage $V_{o,1}$ is also illustrated

2.3 Transformation Stage

Two variants of the transformation stage are presented in this thesis. The first variant is used in the first and second prototype converters. With this design the parasitic leakage inductance of the transformer undesirably rings with its secondary side winding capacitance at the switching transitions. The transformer has to be carefully designed in order to mitigate this ringing. The

second variant is used in the third prototype. This utilizes a matching network to remove the ringing.

2.3.1. First Variant of the Transformation Stage

In this section the first prototypes transformation stage will be discussed. The transformation stage is shown in Figure 2.7. It consists of a transformer, series resonant tanks and a resistance compression network. These are discussed below.

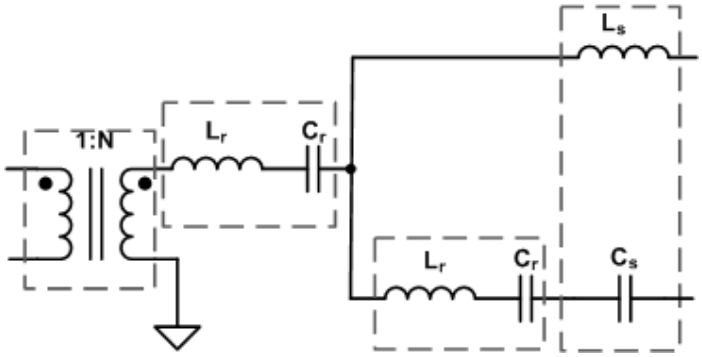


Figure 2.7: Transformation stage of the first and second prototypes

Transformer

A step up transformer is needed to efficiently provide the required voltage transformation. The output voltage of the transformer is ideally N times the input voltage ($V_x = NV_i$), i.e., it provides a gain of N. Ideally, a transformer is lossless but in practice it has loss, and also has imperfect magnetic coupling. At high frequencies, parasitic capacitances of the transformer also become important. A T-model of the transformer has been used in this thesis. It has leakage inductances (Lp_l and Ls_l), magnetizing inductance (L_u), and parasitic capacitances (C_p , C_s and C_{ps}). The transformer model is shown in Figure 2.8.

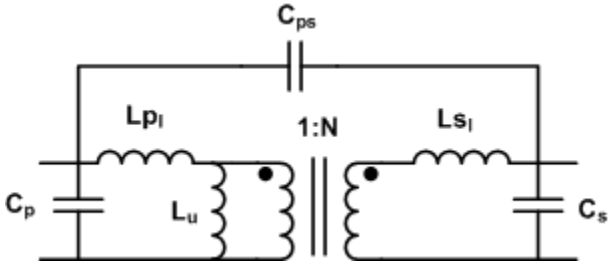


Figure 2.8: A model for the transformer

Lp_l and Ls_l oscillate with C_s to provide the undesirable ringing. A tradeoff between the gain of the transformer and impedance of the resistance compression network is made. If a higher value of N is chosen a lower value of X (impedance of the RCN) can be selected for the same power output. However, N has to be greater than $\frac{V_{out}}{2V_{in\_min}}$ as derived from Equation 2.5.

Series Resonant Tank

A series resonant tank consists of an inductor L_r and a capacitor C_r in series with the load. They have conjugate impedances at the resonant frequency. Since the tank appears as a short circuit at the switching frequency, it is treated as such in the following analysis. At all other frequencies, it provides high impedance path and is used as a filter to shape the current waveform. The tank appears inductive at switching frequencies above the resonant frequency while it appears capacitive below resonance.

Resistance Compression Network

A resistance compression network (RCN) consists of two conjugate impedances (+jX and -jX) as shown in Figure 2.9.

The input impedance of the RCN looks purely resistive and is given by:

$$Z_i = \frac{X^2 + R_L^2}{2R_L} \tag{2.2}$$

where X is the reactive impedance magnitude of the RCN elements (L_s and C_s) at the switching frequency. The use of the resistance compression network reduces the variation in effective load impedance seen by the inverter, since Z_i is relatively insensitive to changes in resistance R_L, caused by variations in output power and/or output voltage. It also serves to limit the instantaneous output power across the operating range by providing a specified loading characteristic.

The value of the impedance X is selected in such a way so as to limit the output power to its desired maximum values P_{max} , at the minimum input voltage, V_{in_min}. Since the power deliver capability of the converter increases with input voltage, this ensures that the converter can deliver the maximum desired power across its entire input voltage range.

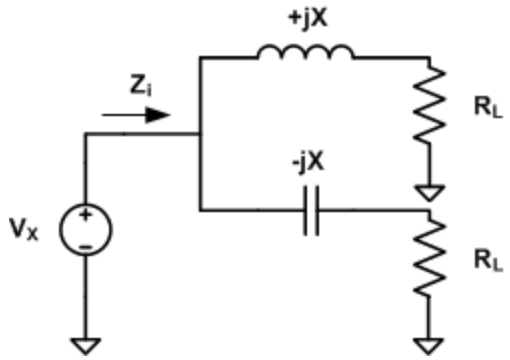


Figure 2.9: Fundamental Frequency model of the RCN converter

To find the value of X (the impedance of the RCN), an expression of power is derived. The output voltage of the inverter V_i is a square wave of magnitude $\pm V_{in}$. The fundamental harmonic component of the square wave has a peak value of $\frac{4}{\pi}V_i$ so the RMS value is given as $\frac{4}{\pi\sqrt{2}}V_i$.

So the power into the transformation stage is given as

$$P_{in} = \frac{V_x^2}{2Z_i} \tag{2.3}$$

where $V_x = NV_i$. The power output is given as

$$P_{out} = \frac{4V_{out}^2}{\pi^2 R_L} \tag{2.4}$$

Assuming no power loss and equating P_{in} and P_{out}, the expression for power interms of circuit parameters is given as:

$$P = \frac{1}{X}\sqrt{\frac{4V_o^2V_x^2}{\pi^2} - \frac{16V_o^4}{\pi^4}} \tag{2.5}$$

X is chosen to get $P_{\max}$ at V_{in_min}.

As shown in Figure 2.10, the RCN reduces the change in variation of R_L. In the Figure 2.10 $R_L$varies by a factor of 4 (from 0.5X to 2X) while Z_i only changes by a factor of 1.25. This helps to ensure Zero Voltage Switching (ZVS) over a wide range of output voltage.

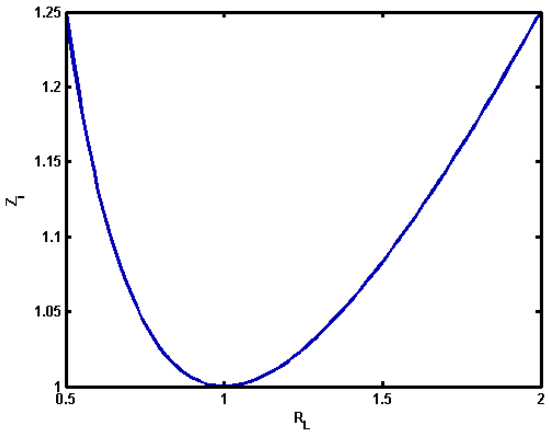


Figure 2.10: Variation in input impedance, Z_i, of the resistance compression network as the load resistance R_L varies. Z_i is plotted assuming the reactance has a value of 1Ω

2.3.2. Second Variant of the Transformation Stage

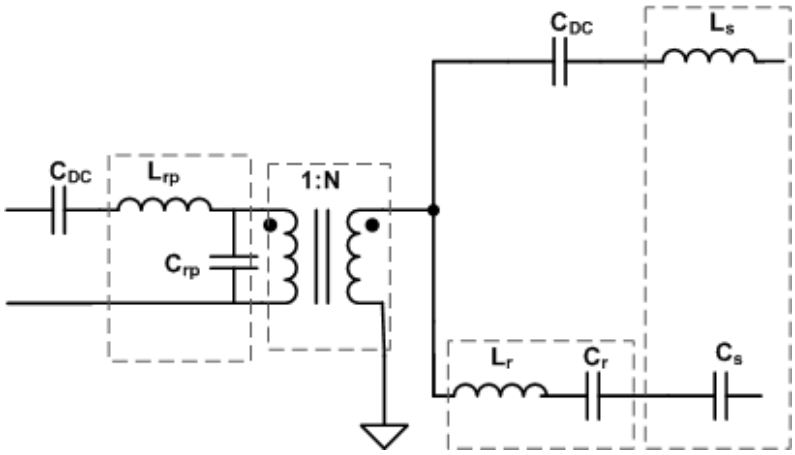


Figure 2.11: Transformation stage used in the final prototype

One issue with the high-turns-ratio step up transformers that are used in many topologies is that the parasitic leakage inductance of the transformer can undesirably ring with its secondary side winding capacitance at the switching transitions, creating large ringing in the current and voltage waveforms and high-frequency losses. In our design this ringing is avoided by incorporating a matching network ($L_{rp}$and C_{rp}) at the primary side of the transformer as illustrated in Figure 2.11. This matching network both provides filtering of the inverter voltage and gives a voltage gain [10]; hence reducing the turns ratio (1:N) requirement on the transformer. Also the parasitic winding capacitance is usefully absorbed in the capacitance of the matching network.

To find the gain of the matching network we model the load that the matching network sees at the fundamental switching frequency as a resistor, as show in Figure 2.12.

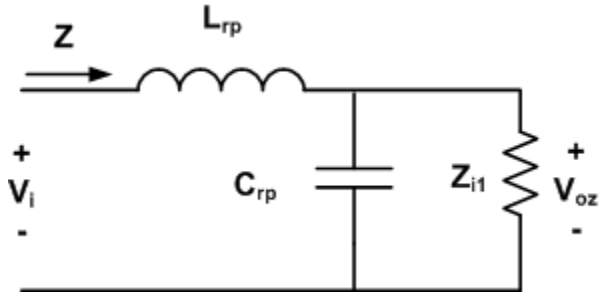


Figure 2.12: Matching network with equivalent impedance

As Z_{i1} $(= Z_i/N^2)$ varies with changes in power, the gain varies:

$$G = \frac{1}{\sqrt{(\frac{\omega L_{rp}}{Z_{i1}})^2 + (1 - \omega^2 L_{rp} C_{rp})^2}} \tag{2.6}$$

With this additional gain the transformer turns ratio can be decreased to N/G which helps to decrease the number of turns on the transformer. Also, the output voltage V_{OZ} is sinusoidal in this case and the series resonant tank on the secondary side of the transformer can be omitted.

The values of L_{rp} and C_{rp} have to be chosen so that the input to the matching network looks resistive and the transistors turn off at near-zero current. The impedance at the input of the matching network is given by:

$$Z = \frac{j\left(X_{Lrp} {Z_{i1}}^2 + X_{Crp}^2 X_{Lrp} - X_{Crp} {Z_{i1}}^2\right) + X_{Crp}^2 Z_{i1}}{{Z_{i1}}^2 + X_{Crp}^2} \tag{2.7}$$

For resistive input,

$$X_{Lrp} = \frac{X_{crp} Z_{i1}^2}{{X_{crp}}^2 + {Z_{i1}}^2} \tag{2.8}$$

2.4 Control Approach

For this topology, the power is regulated using on-off control. This is also called burst mode control or bang-bang control. The advantage of using on-off control is that the magnetics are designed for only a single frequency (a high frequency) while the power is regulated by turning the devices on and off at a lower frequency. Moreover, the power is transferred only in the fraction of the time the converter is on which results in high efficiency at even light loads. The power output is controlled by the duty ratio of the on-off modulation frequency.

The on-off modulation frequency has its own corresponding loss. The higher the modulation frequency the greater the loss. The output capacitance is sized according to the modulation frequency. With lower modulation frequency larger capacitor has to be used. The duty ratio of the modulation also determines the loss. Very small or large duty ratio results in greater loss as the converter is in steady state for a shorter time. So, in order to minimize the total loss both the modulation frequency and duty ratio have to be considered.

2.5 Summary

This chapter illustrates the design consideration for the proposed topology. It provides a general analysis of the three stages of the converter. In the following chapters the detailed design of these stages will be provided for a grid-connected dc/dc converter.

Chapter 3

The First Converter Prototype

In this chapter the detailed design of the first prototype of the resistance compression network (RCN) dc/dc converter is presented. The specifications for this prototype are given in Table 3.1. The schematic of the design is shown in Figure 3.1. The components selection for the prototype is described in the following sections of this chapter.

Table 3.1: Specifications for the first prototype

Parameter	Value
Input Voltage Range, V_{in}	25 V - 40 V
Output Voltage Range, V_{out}	400 V
Frequency	100 kHz
Output Power Range	20 W - 200 W

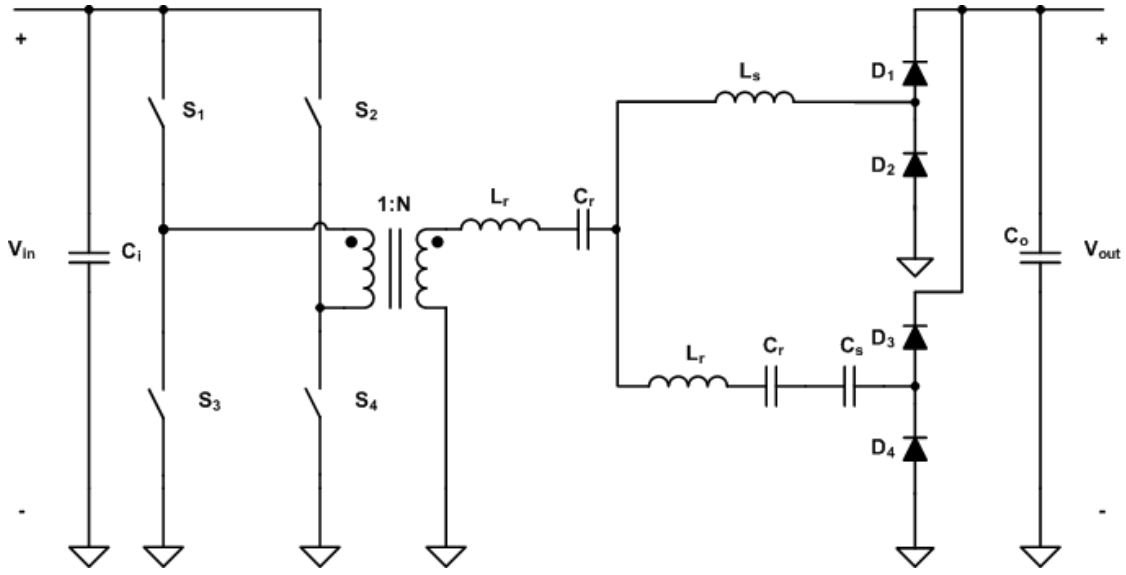


Figure 3.1: First prototype of the RCN Converter

This converter has been simulated in LTspice (The simulation files are provided in Appendix C and Figure C.1 has the reference designators for these waveforms). Simulation models of the converter show near ZCS switching. Moreover, the currents at the switching transitions are in the correct direction to provide ZVS turn on with capacitive snubbing across the devices. The LTSPICE simulation waveforms of the voltage across switch S_3, the gate voltage to S_3 and the input current to the primary of the transformer are shown in Figure 3.2 In this simulation an ideal transformer has been used.

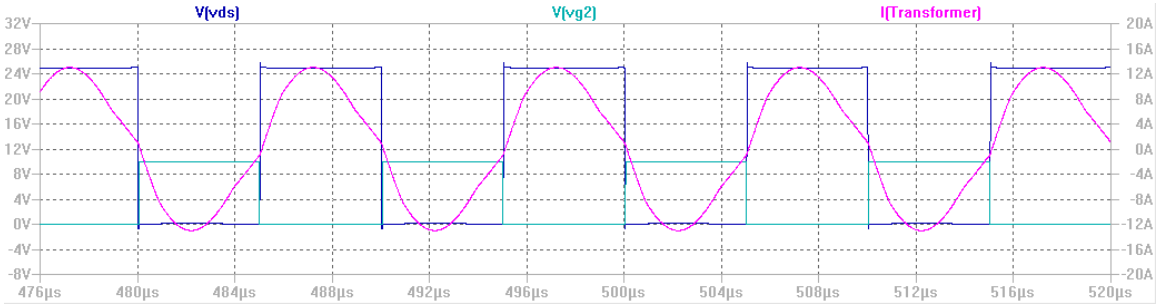


Figure 3.2: Simulation waveforms of current and voltage with an ideal transformer model. V(vds): Voltage across switch S_3. V(vg2): Voltage of the gate drive of S_3. I(Transformer): The current at the primary of the transformer

To find the value of X (the impedance of the RCN), the expression of power that was derived in Chapter 2 is used.

$$P = \frac{1}{X}\sqrt{\frac{4V_o^2V_x^2}{\pi^2} - \frac{16V_o^4}{\pi^4}} \tag{3.1}$$

X has been chosen to get 200 W output power with 25 V input.

$$X = \frac{1}{200}\sqrt{\frac{4(400)^2(1000)^2}{\pi^4} - \frac{16(400)^2}{\pi^4}} = 243.17\Omega \tag{3.2}$$

When the input voltage varies from 25 V to 40 V the output power increases from 200 W to maximum power. In Figure 3.3 transformer turns ratio of 10 has been selected and shows the output power variation.

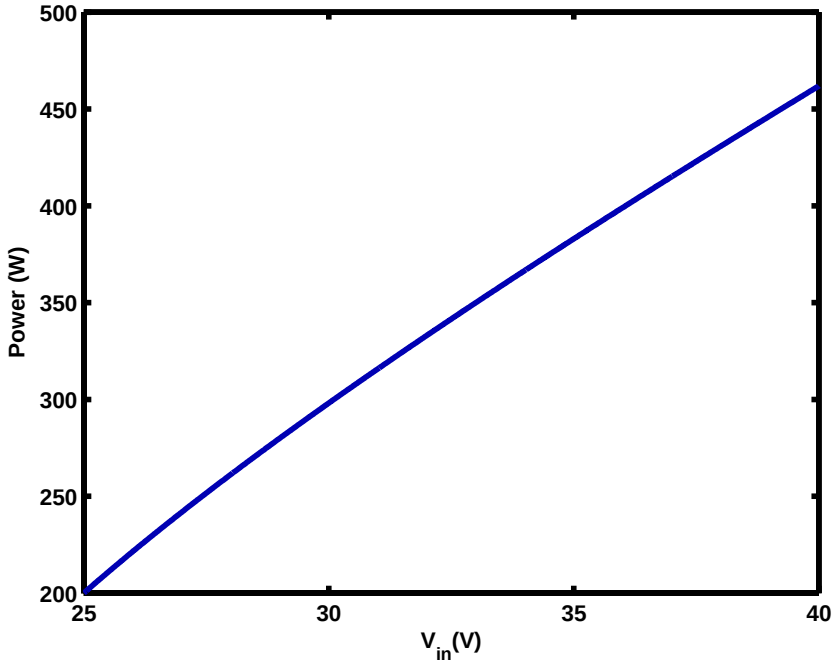


Figure 3.3: Plot of voltage (V_{in}) and power (P_{out})

3.1 Inverter Stage

For the full-bridge inverter EPC's enhancement mode GaN transistors EPC2001 were selected with 100V blocking capability and an average current capability of 10A. These devices were preferred over state-of-the-art silicon transistors as they have a lower RQ product (On state resistance times total charge required to turn the device on and off) and are smaller in size. Hence, better performance was expected of them.

The LM5113 has been chosen as the gate driver. It is specially designed for the EPC GaN devices. It is a 100 V bridge driver with an integrated high-side bootstrap diode. It also has under-voltage lockout capability.

The transistors are switched at 100 kHz using a TMS320F28335 microcontroller. It has PWM modules that can easily be programmed to produce the required waveforms with a minimum 10 ns dead time. The microcontroller code is given in Appendix B.

3.2 Rectifier Stage

The pair of diode half-bridge rectifiers are modeled as resistors. The rectifier resistance varies by the following expression as previously derived:

$$R_L = \frac{4V_{out}^2}{\pi^2 P} \tag{3.3}$$

As P varies from 200 W to 461 W, R_L varies from 324 Ω to 140 Ω as seen in Figure 3.4.

Silicon Carbide Schottky diodes (C3D02060E) are used. These are 2 A devices with 600 V blocking capability.

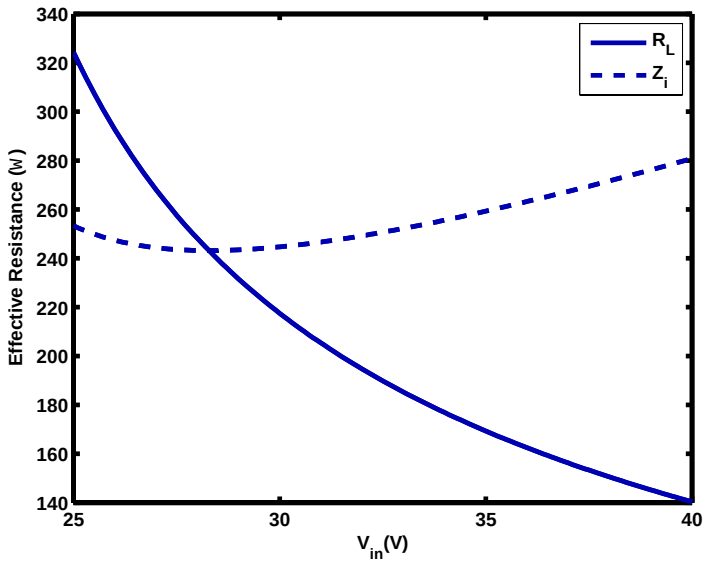


Figure 3.4: R_L and Z_i variation with respect to variation in input voltage

3.3 Transformation Stage

3.3.1 Resistance Compression Network

The resistance compression network consists of an inductor L_c and a capacitor C_c whose impedance have equal magnitude, i.e., $\omega L_c = 1/\omega C_c = X$.

The expression as derived before is for the effective input impedance of the resistance compression network is:

$$Z_i = \frac{X^2 + R_L^2}{2R_L} \tag{3.4}$$

Z_i varies less as compared to R_L as shown in Figure 3.4. The inductor for the resistance compression is 372 µH. The total loss for 372 µH inductor is 1.1747 W with a maximum current of 1.85 A at a maximum input voltage of 40 V. Figure 3.5 shows the different cores considered. The core used is RM12A160 with 48 turns of wire. The wire is 40 AWG 125 strands litz wire which is 2.928 m in length.

For the capacitor C_c, mica dielectric capacitors of 6.8 nF capacitance are used.

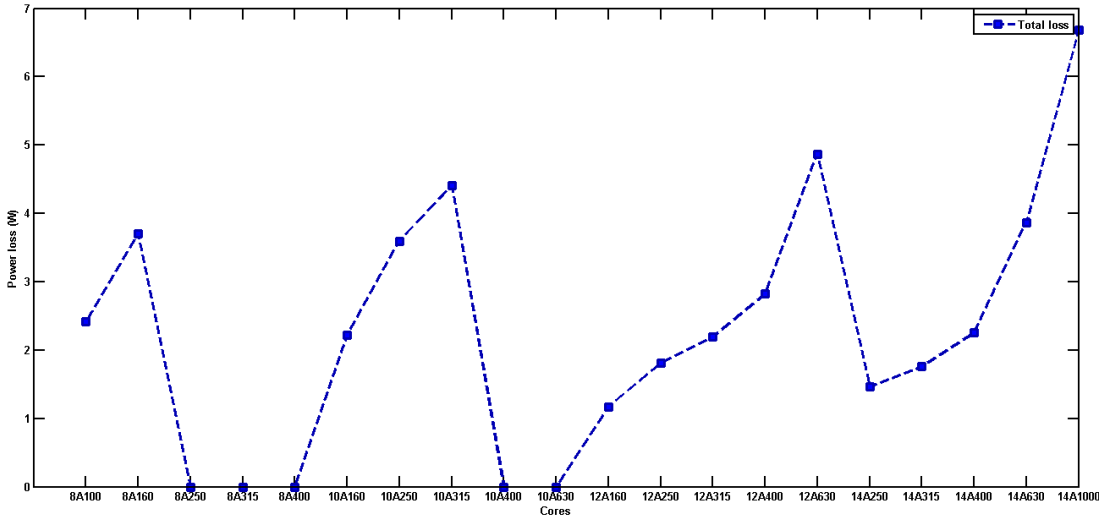


Figure 3.5: Total power loss of 372uH inductor vs cores of different gaps and sizes at 40V input

3.3.2 Series Resonant Tank

The series resonant tank consists of an inductor L_r and capacitor C_r that have equal impedances (L_r= 506.6µH, C_r= 5nF, $|Z_L|=\omega L_r = |Z_c|\frac{1}{\omega C_r}$=318.3 at 100 kHz) at the resonant frequency and are placed in series with the load.

At the resonant frequency

$$Z_r(\omega_o) + Z_c(\omega_o) = 0 \tag{3.5}$$

For the design of the inductor RM8, RM10, RM12 and RM14 gapped Ferrite 3F3 cores are considered. Inductors of 506 µH inductance are used for the resonant tank. For 506 uH inductor RM12A160 is selected as seen in Figure 3.6. Some cores are rejected because their flux density exceeds the saturation flux density (B_{sat}) or their temperature exceeds the allowed temperature. They are replaced by zero power dissipation as show in Figure 3.6. The total loss for 506 µH inductor is 2.175 W with a maximum current of 2.07 A at a maximum input voltage of 40 V. It has 56 turns using a 40AWG 100 strands litz wire. It is 3.146 m in length. RM12A160 which has the gap size of 0.058 inches is used. There is a limit to the increase in gap size as fringing and leakage becomes dominant. The MATLAB code for this is given in Appendix B.

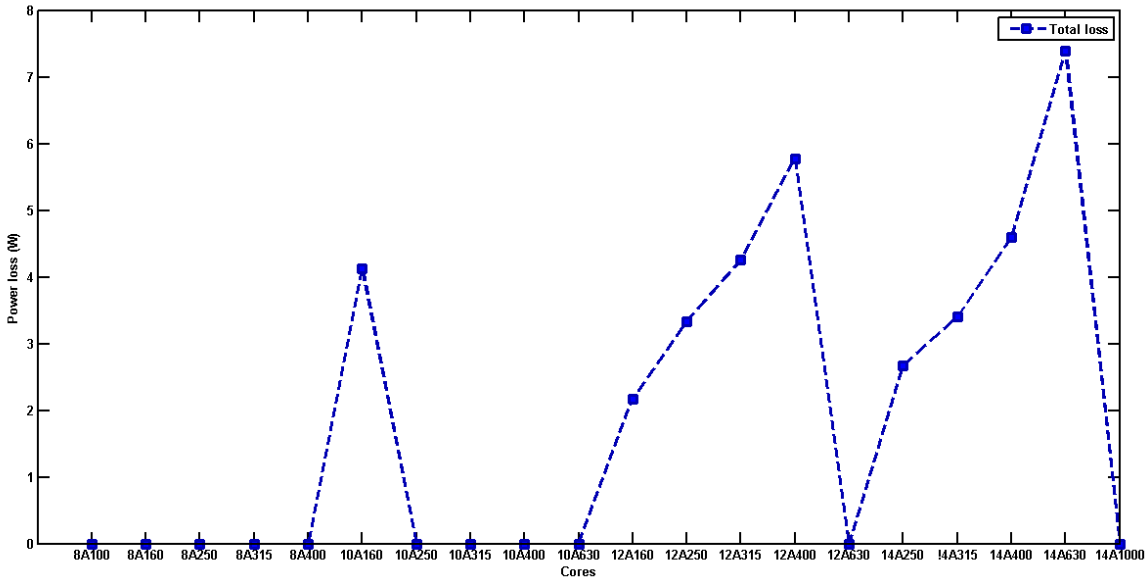


Figure 3.6: Total power loss of 506 µH inductor vs cores of different gaps and sizes at 40 V input

For the capacitance high Q and very stable mica dielectric capacitors are used. 5nF capacitance is need to resonate with 506 µH inductor at 100 kHz.

3.3.3 Transformer

To select the transformer turns ratio, the trade-off between the losses in the parasitics of the transformer and the parasitic resistance of the RCN have to be considered. By increasing the transformer turns ratio and accordingly decreasing the reactance level of RCN we can reduce the maximum output power at 40 V (Figure 3.7).

To have power output of 200 W at 25 V input a particular value of N and X is chosen (Equation.3.1). If N is increased, X needs to decrease in order to have the same power (200 W at 25 V input). However, as X decreases the power output at 40 V input also decreases (Equation.3.2).

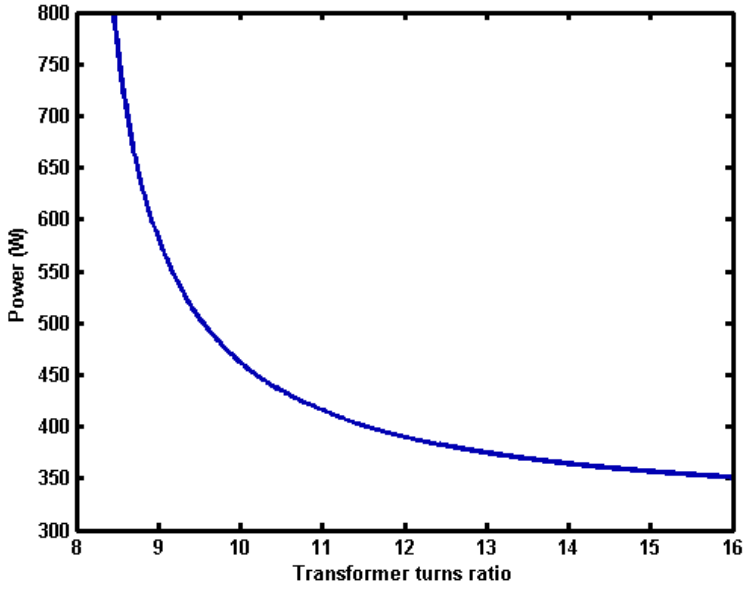
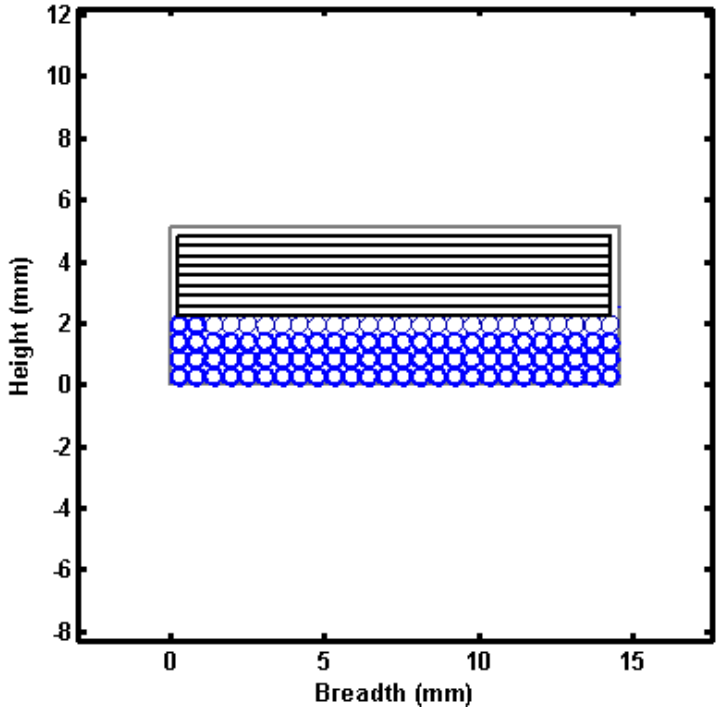


Figure 3.7: The output power versus transformer turns ratio (N) for V_{in}= 40 V

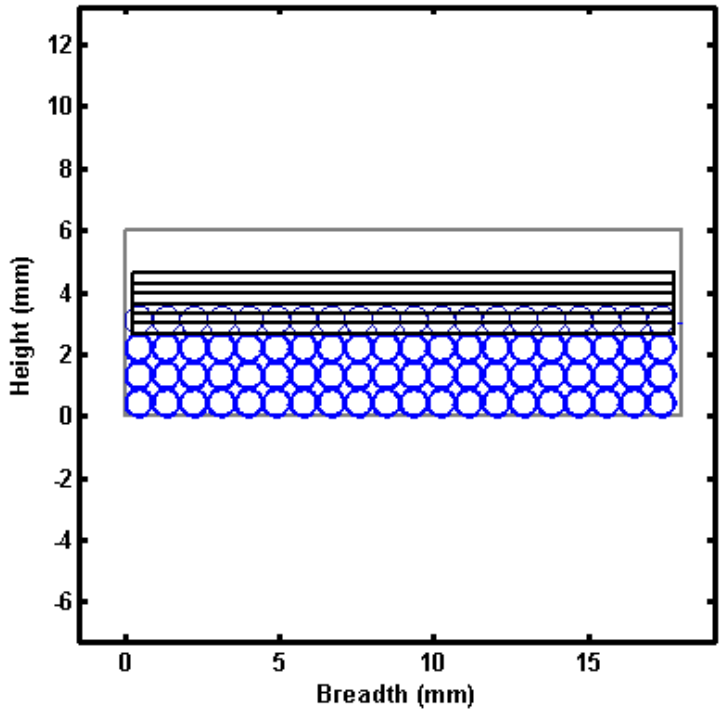
Transformer turns ratio of 10 was selected as a reasonable trade-off between the two losses in transformer and inductor, as described below. Considering the power requirements, three core sizes were shortlisted out of which RM10 is the smallest and RM14 is the largest. 3F3 core material was selected given the selected operating frequency of 100 kHz.

The loss in a transformer can be divided into core loss and copper loss. A good design usually balances the two to minimize the overall loss. By increasing the number of turns wound on the transformer core (increasing copper loss) the magnetic field density can be decreased (decreasing core loss). In Figure 3.8 (a) the cross-section of RM12 core window is shown. The blue (thick outline) circles represent the cross-section of litz wire that is used for secondary winding and the black rectangles are the copper foil that is used for primary winding. The blue (thin outline) circles are the cross-section of the total number of turns of litz wire that can fit if half of the total area is allocated for the secondary winding. Both designs in Figure 3.8 are optimized to minimize

the loss. The number of turns of the windings (which corresponds to the length of the wire) and diameter of litz wire (which corresponds to number of strands of wire) varies in both designs.



(a)



(b)

Figure 3.8: Cross-section of core window (a) RM 12 (b) RM 14

For core material Ferrite 3F3, 3C90 and 3C94 were considered as possible options. Figure 3.9 is the plot of core loss versus the change in temperature for these three materials. Ferrite 3F3 was selected because it has the least loss a wide opearting temperature range of operation and there is more experimental data for parameter extraction available [12].

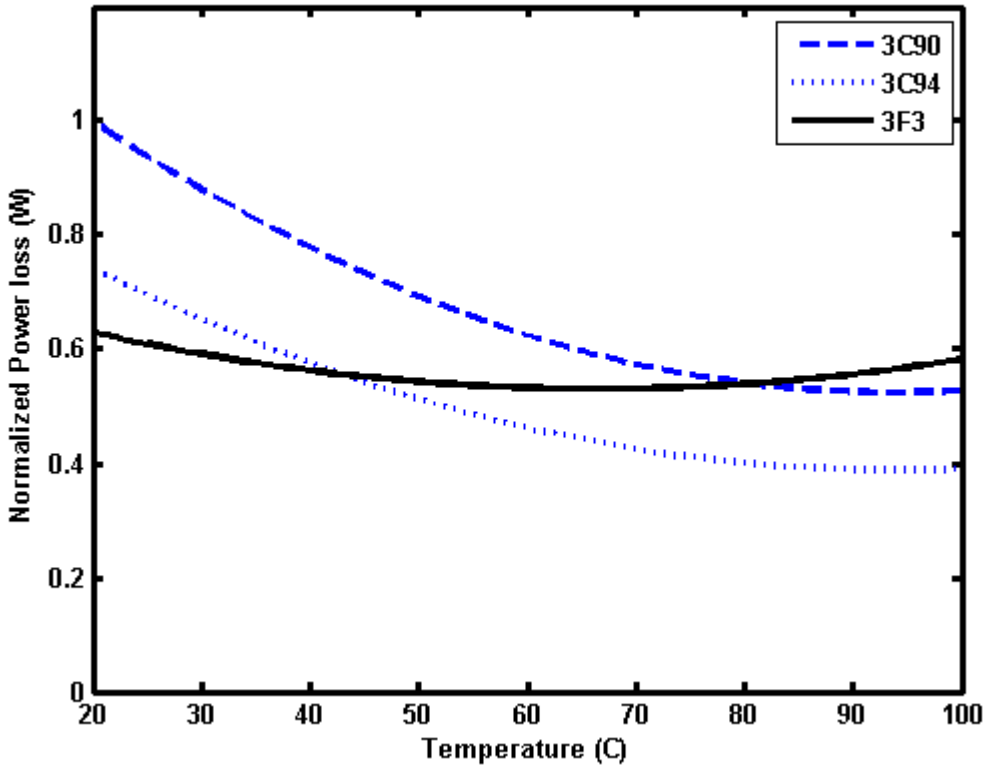


Figure 3.9: Normalized power loss versus temperature variation for different ferrite materials

The cores loss is given by:

$$P_{max} = C_m f^x B_{max}^y (c_{t_0} - c_{t_1} T + c_{t_2} T^2) \tag{3.6}$$

C_m, x, y, c_{t_0}, c_{t_1} and c_{t_2} are parameters found by curve fitting of the measured power loss data. f is frequency, B_{max} is the maximum flux density and T is the temperature [12]. The design selected has RM12 core with 8 turns of primary winding and 80 turns of secondary winding. For the primary copper foil is used which is 0.488 m in length, 254 µm (10 mils) in thickness and

0.01405 m in width. For secondary winding, 40 AWG litz wire is used which is 4.88 m in length with 30 strands in parallel.

The transformer that was built according to the procedure stated above was characterized using an impedance analyzer (Agilent 4395A). It was found to have a primary side leakage inductance of 0.689 µH and primary side magnetizing inductance of 258.218 µH. It has a secondary leakage inductance of 78.8 µH. The primary winding capacitance is 3234 pF and the secondary winding capacitance is 12.8 pF. The T model for the transformer is shown in Figure 3.10.

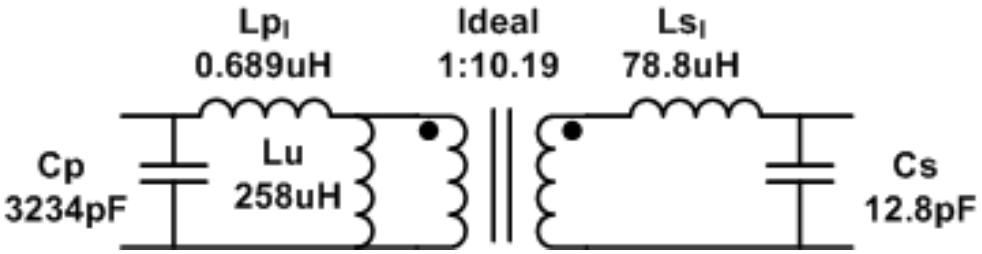


Figure 3.10: Transformer model with parasitics

When the transformer model is introduced in the LTspice simulation ringing can be seen as shown in Figure 3.11. The effects of these parasitics will be seen in the experimental results (Section 3.4).

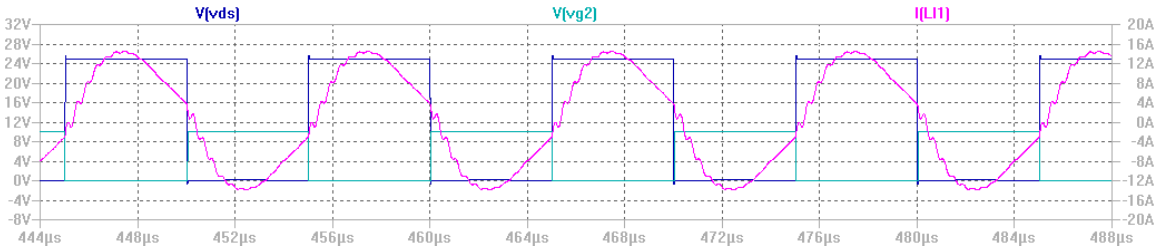


Figure 3.11: Simulation waveforms of current and voltage with a non-ideal transformer model. V(vds): Voltage across switch S_3. V(vg2): Voltage of the gate drive of S_3. I(Ll1): The current at the primary of the transformer

3.4 Experimental Setup and Results:

The experimental prototype is shown in Figure 3.12. The components selected for the prototype are listed in

Table 3.2.

The input voltage is provided by HP 6012A DC power supply with voltage regulation. For the load, thick film power resistors (TGH series by Ohmite) are used. These are mounted on a large heat sink and cooled using a fan. A power analyzer (Yokogawa WT1800) is used to measure the efficiency. The converter voltage and current waveforms are obtained using Tektronix mixed signal oscilloscope (MSO 4054B).

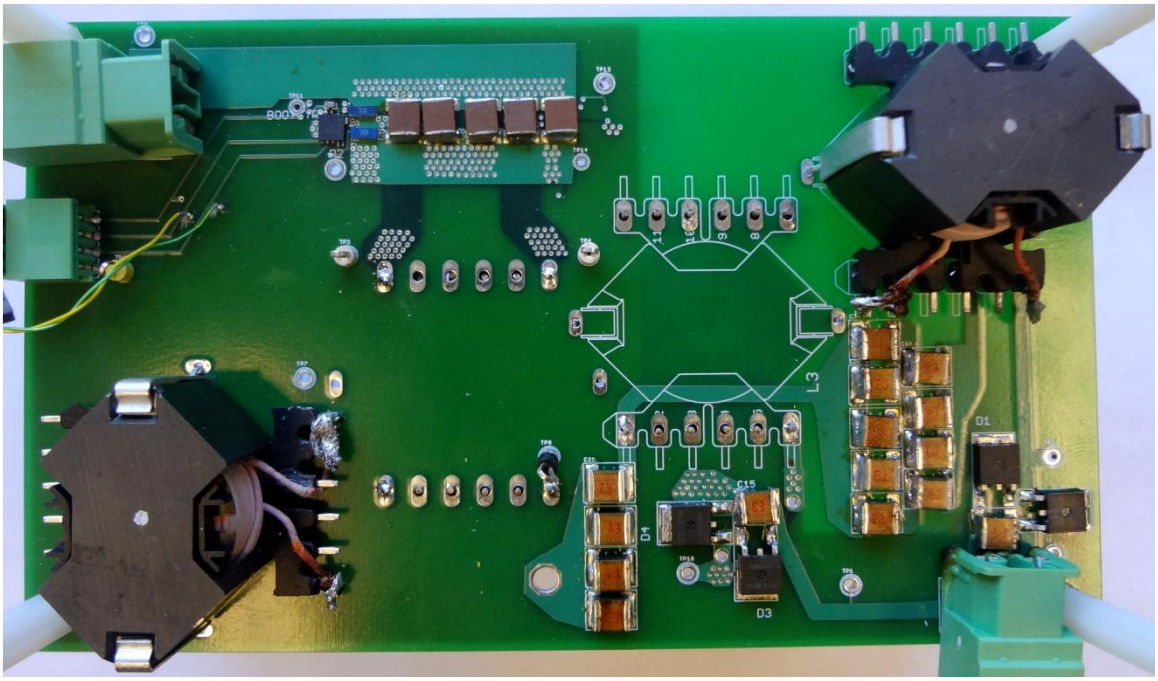


Figure 3.12: First prototype board of the RCN converter

Table 3.2: Components used in the experimental prototype

Components	Type
Transistors	GaN HEMTS -EPC 2001,
Diodes	SiC schottky Diode- C3D02060E
Transformer	RM12 3F3 core, Copper foil (8 turns, 14.05mm width, 10 mils thickness) and litz wire (80 turns, 40AWG, 30 strands in parallel)
Capacitors	C_s: 6.8nF, C_r :5nF , Mica capacitor
Inductors	L_s: 372uH, RM12A160 3F3 core, litz wire (48 turns, 40AWG, 125 strands in parallel) L_r: 506uH, RM12A160 3F3 core, litz wire (56 turns, 40AWG, 100 strands in parallel)
Drivers	LM5113
Controller	TMS320F28335

The experimental voltage and current waveforms are shown in Figure 3.13. The schematic of Figure 3.14 illustrates the measured voltages and currents and their polarity.

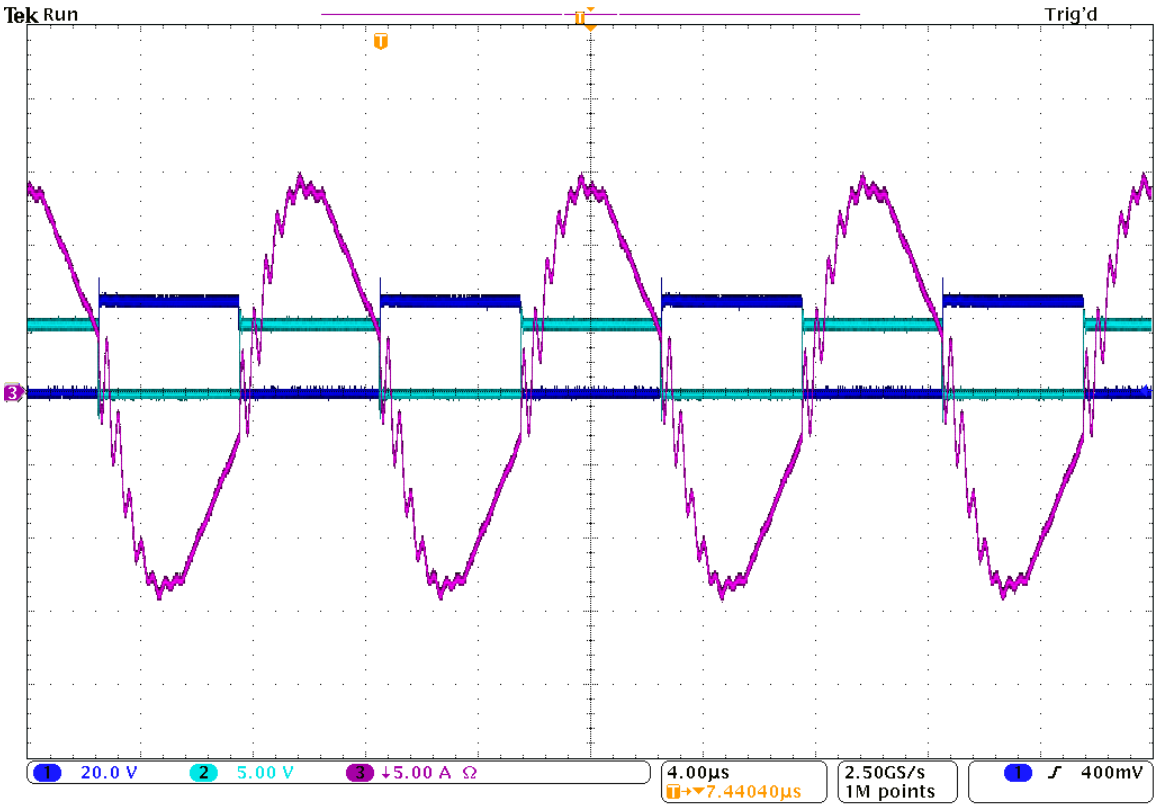


Figure 3.13: (1)V_{DS},Voltage across switch S_3 (2)V_{GS}, Gate source voltage of switch S_3 and (3)I, Current at the primary of the transformer with 25V input voltage and 400V output voltage.

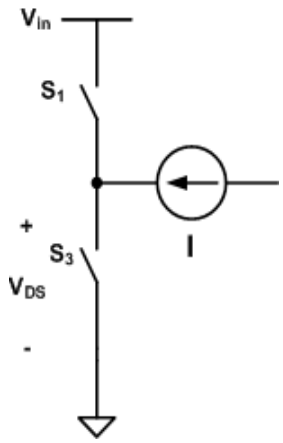


Figure 3.14: Schematic of the current and voltages being measured

In Figure 3.15 near Zero Current Switching can be seen. It is switching at 25% of the peak current. In Figure 3.16 ZVS can be observed. The voltage V_{DS} decreases to zero before the gate signal V_{GS} is applied to switch the transistor on.

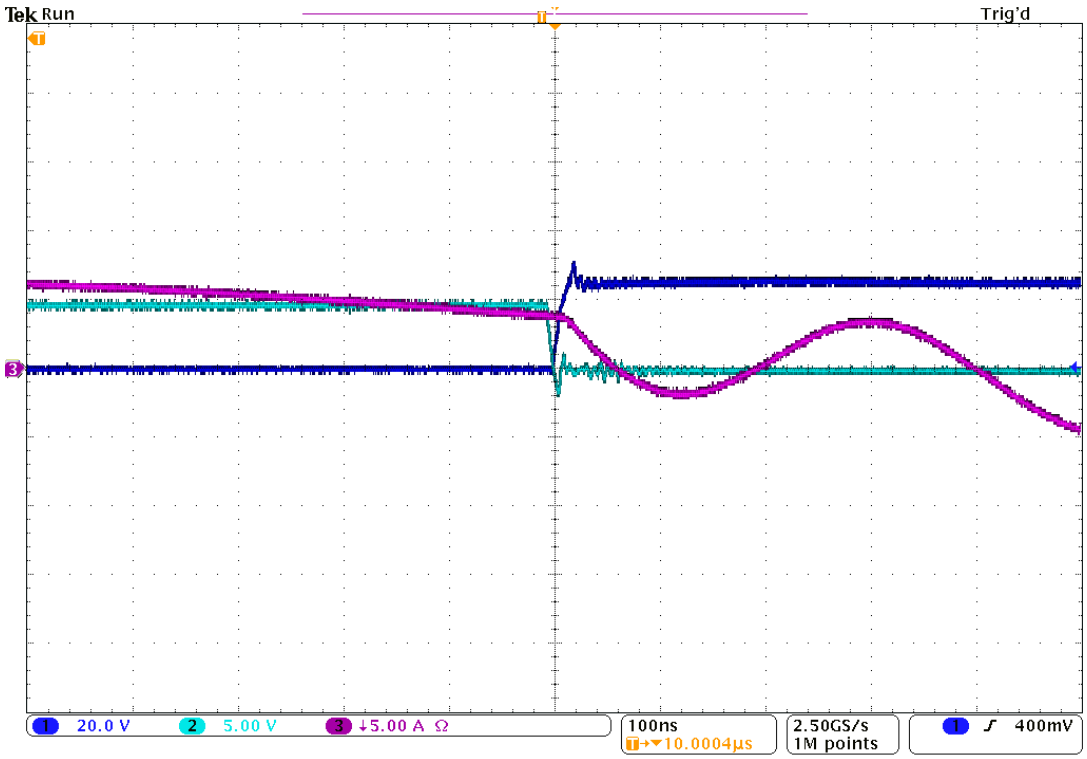


Figure 3.15: (1)V_{DS}, across switch S_3 (2)V_{GS} for switch S_3 and (3)I at turn off

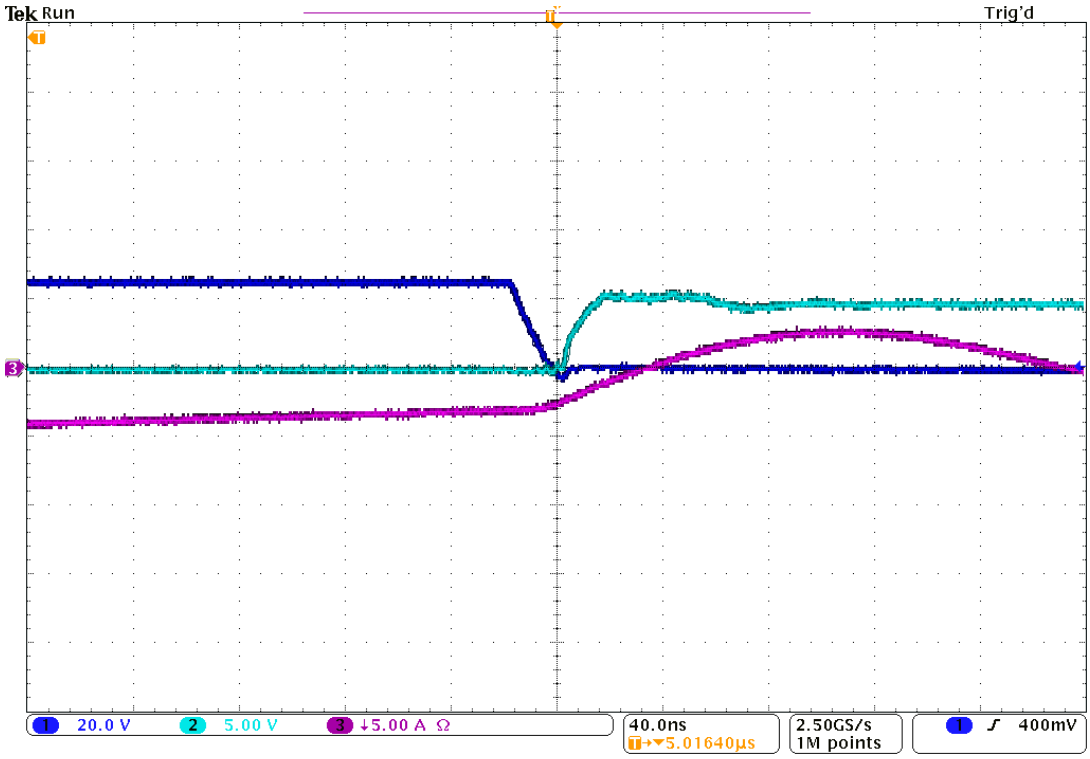


Figure 3.16: (1)V_{DS}, across switch S_3 (2)V_{GS} for switch S_3 and (3)I at turn on

A prototype is built as a proof of concept of the proposed architecture and design methodology. It is designed to operate at a switching frequency of 100 kHz. The efficiency of the prototype converter was measured. It has 93.5% efficiency for continuous operation at 25V input voltage and 400V output voltage. The transistors switch at 25% of peak current at 25V input. Due to the transformer parasitics, ringing is observed in the voltage and current waveforms. However, the prototype proved successful in showing that the new topology works and can be used for high-gain and high-efficiency dc/dc resonant power converters.

Chapter 4

The Second Converter Prototype

An important consideration for the second prototype is the switching frequency. In this chapter we first discuss the effect of switching frequency on the losses in the individual components of the converter. The losses increase with increase in frequency for some components while they decrease for others. The frequency that minimizes the total loss in the converter is chosen as the switching frequency of the converter. A second prototype designed for this optimal switching frequency is presented in the later parts of this chapter along with its experimental results.

In the following sections we discuss the dependence of losses on switching frequency in each of the three stages of our converter: Inverter stage, Rectifier Stage and Transformation Stage.

4.1 Inverter Stage

The main loss in the inverter stage is due to the transistors. In a transistor there is conduction loss and switching loss. The conduction loss is not depended on frequency and is estimated by:

$$P_{tran_{cond}} = I_{rms}^2 R_{DS(ON)} \tag{4.1}$$

The switching loss is a function of frequency. At turn on, without ZVS, the loss is due to the capacitor discharging through the resistance of the transistor. This loss is dependent on the energy stored in the capacitor at the switching transition.

$$P_{tran_{on}} = 0.5 C_{oss} {V_{in}}^2 f \tag{4.2}$$

where C_{oss} is the output capacitance of the transistor, V_{in} is the voltage across the transistor before it is turned on and f is the switching frequency.

Figure 4.1 and Figure 4.2 illustrate the current through the switch and the current through the two output capacitors of the transistors in one of the legs of the inverter during the turn off transitions. To simplify the analysis the assumption is made that that the current flowing in the inductor does not change during the transition. The power loss in the transition during turn-off can be calculated from:

$$P_{tran-off} = (\int_0^{t_{off}} v_{sw} i_{sw}.dt)\, f \tag{4.3}$$

During the turn-off transition the transistor current, i_{sw}, and voltage, v_{sw}, are given by:

$$i_{sw} = I_0\left(1 - \frac{t}{t_f}\right) \tag{4.4}$$

$$v_{sw} = \frac{I_0 t^2}{4C_{oss}t_f} \tag{4.5}$$

where I_0 is the current in the inductor and switch at the start of the transition and t_f is the fall time. Hence, the power loss in the transistor during turn-off is given by:

$$P_{tran\_soff} = \frac{I_0^2 t_f^2 f}{48C_{oss}} \tag{4.6}$$

So this loss is also directly proportional to switching frequency. Transistor turn-off loss can be decreased by aiming for near zero-current-switching (near ZCS) as in this case I_0 is very small (relative to the peak switch current).

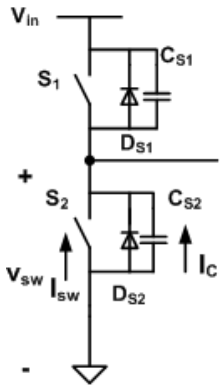


Figure 4.1: Circuit schematic of one leg of the inverter

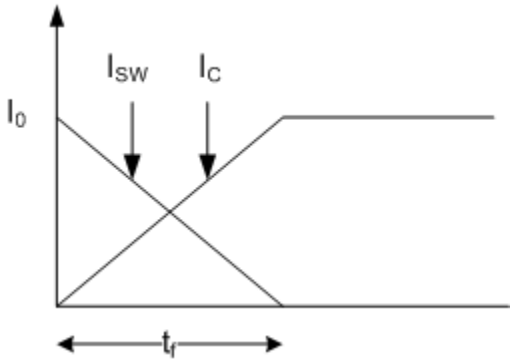


Figure 4.2: Current through the switch and capacitors of one leg of the inverter during turn-off

In our prototypes we have used 100 V/ 10 A, Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) from EPC (EPC2001). The parameter values for these transistors that impact loss are given in Table 4.1.

Table 4.1: Parameters of interest of GaN EPC2001 devices

Parameter	Value
$R_{DS(ON)}$	9.1 mΩ
C_{oss}	550 pF (at 25 V V_{DS})
Q_g	8.5 nC (at 5 V V_{GS})

To decrease the device loss further, transistors can be paralleled. In Figure 4.3, up to 4 transistors are paralleled and the device loss is estimated. The conduction loss decreases as the current through each switch decreases by $1/k$ (where k is the number of transistors paralleled). The turn-on loss of each transistor remains the same so having k transistors increases the total turn-on loss

by k. Another way to look at it is that the effective capacitance increases by k as the capacitances are paralleled. The turn-off loss decrease by 1/ k as the loss is directly proportional to I_0^2/C_{oss} (I_L decreases by 1/ k and the effective capacitance increases by k).

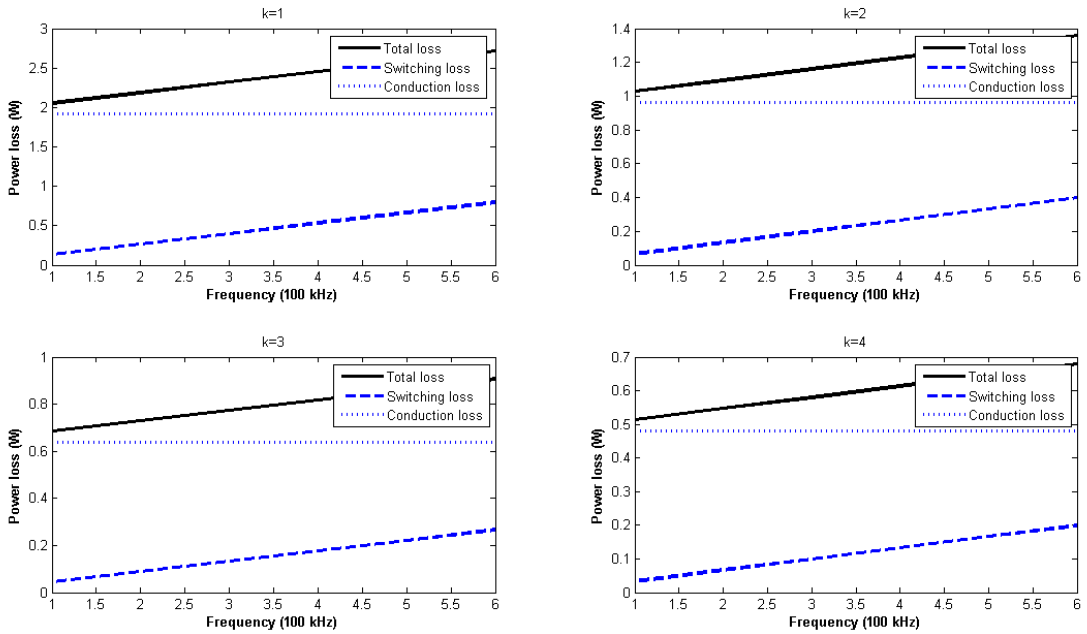


Figure 4.3: Active device loss under soft switching when 'k' devices are paralleled

The transistors also have gating loss due to the charging and discharging of the gate capacitance. This loss is also a function of frequency and is given by:

$$P_{gate} = 2Q_g V_{GS} f \tag{4.7}$$

Where Q_g is charge needed to turn the device fully on and V_{GS} is the gate to source voltage when the device is on.

4.2 Rectifier Stage

The loss in the rectifier stage is due to the four diodes. Diodes have conduction and switching losses. The diodes conduction loss is not a function of frequency, while its switching loss is directly proportional to the switching frequency.

The conduction loss is given by:

$$P_{d\_cond} = I_{rms}^2 R_T + I_{avg} V_T \tag{4.8}$$

where V_T is the on-state voltage drop and R_T is the on-state resistance. Both V_T and R_T are temperature dependent.

For hard-switched case the switching loss is given by:

$$P_{d\_sw} = 0.5 C_d V_r^2 f \tag{4.9}$$

where C_d is the capacitance of the diode, V_r is the reverse blocking voltage. In the proposed topology the diodes are soft-switched (near ZVS and near ZCS) so the loss decreases.

Considering all these losses, a switching frequency of 500 kHz was chosen. This highlights the advantages of using this topology to reduce switching loss at higher frequencies.

4.3 Transformation Stage

Most of the losses in the transformation stage are caused by the magnetic components (transformer and inductors). Some losses are caused by capacitors. The transformer is made by winding primary and secondary windings around a magnetic core. The primary and secondary windings are made of, copper foil and litz wire, respectively. Inductors are made by winding litz wire around the magnetic core. Both core and winding have associated losses and both of these losses are functions of frequency.

4.3.1. Core loss

Core losses are due to hysteresis loss (due to rotation of magnetic domains) and eddy current loss (due to the currents induced by the changing magnetic fields in the conducting magnetic core). Both of these losses are a function of frequency and the total core loss per unit volume can be estimated using the Steinmetz equation:

$$P_{\{max\}} = C_m f^x B_{max}^y (c_{t_0} - c_{t_1} T + c_{t_2} T^2) \quad (4.10)$$

C_m, x, y, c_{t_0}, c_{t_1} and c_{t_2} are parameters found by curve fitting of the measured power loss is frequency, B_{max} is the maximum flux density and T is the temperature [12]. The parameters in the Steinmetz equation depend on the frequency range of interest. For 3F3 material in the frequency range of our interest, the Steinmetz parameters are given in

Table 4.2

Table 4.2: Steinmetz Parameters for 3F3 material

Parameter	$f < 300$ kHz	300 kHz $< f <$ 500 kHz	$f > 500$ kHz
C_m	0.25×10^{-3}	2×10^{-5}	3.6×10^{-9}
x	1.63	1.8	2.4
y	2.45	2.5	2.25
c_{t_0}	1.26	1.28	1.14
c_{t_1}	1.05×10^{-2}	1.05×10^{-2}	0.81×10^{-2}
c_{t_2}	0.79×10^{-4}	0.77×10^{-4}	0.67×10^{-4}

If the maximum magnetic flux density B_{max} was constant, P_{core} would increase with increasing frequency. However, the inductance of the inductors is inversely proportional to the switching frequency, so when frequency increases, the inductance decreases. Hence, if the core size does not change the maximum flux density decreases. So the core losses do not change monotonically with frequency as can be seen in Figure 4.4 and Figure 4.5.

Figure 4.4 shows the variation in transformer loss with frequency, while Figure 4.5 shows this variation in loss for the resonant inductors. The transformer and inductor designs in Figure 4.4 and Figure 4.5 have not been optimized at every frequency. For example, the peak in power loss at 300 kHz in Figure 4.4 is because the core loss and copper loss are significantly different.

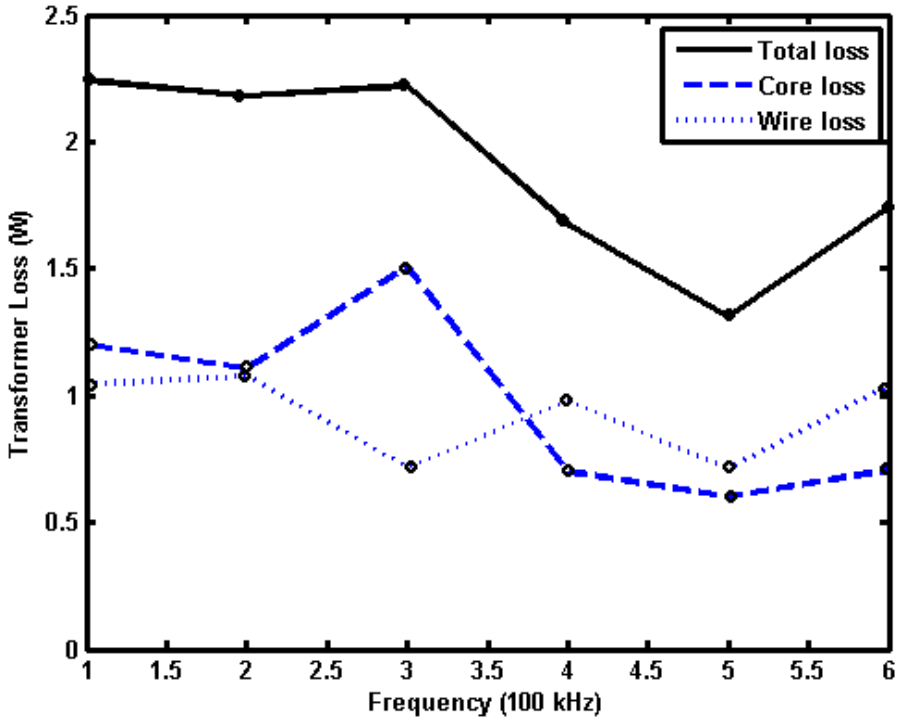


Figure 4.4: Transformer loss as a function of frequency

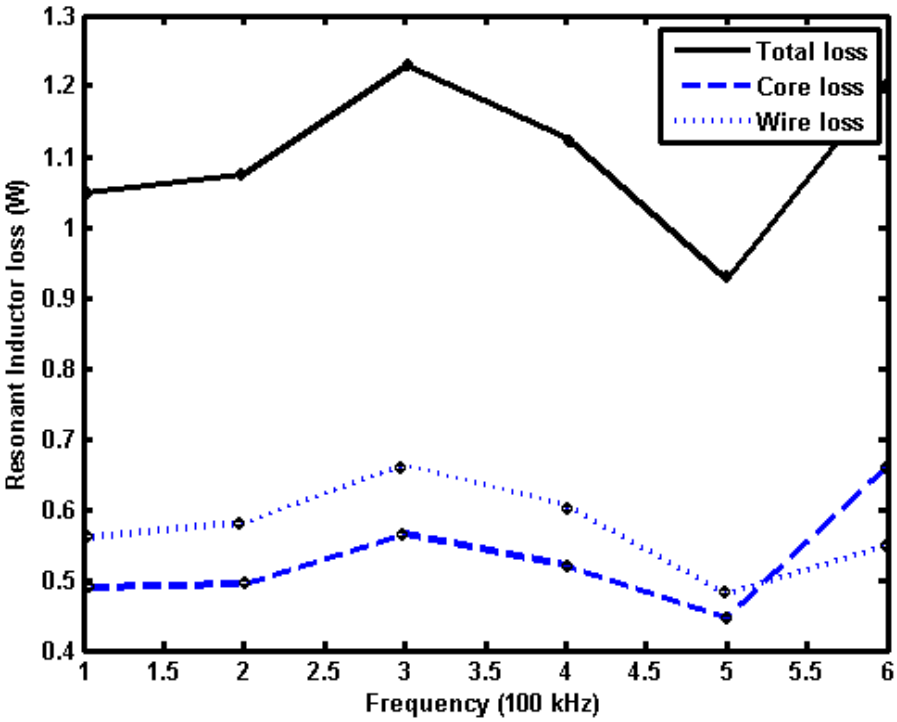


Figure 4.5: Resonant inductor loss with varying frequency

4.3.2. Winding loss

Litz wire is used for the secondary winding of the transformer and for the windings of the inductors. Litz wire has insulated thin strands of wire twisted together to help reduce losses due to skin and proximity effect. As frequency increases the skin depth decreases, so finer strand litz with more wires in parallel has to be used.

The loss in a litz wire is given by [13].

$$P_{w\_litz} = I_{rms}^2 R_{dc} Fr \tag{4.11}$$

Here R_{dc} is the dc resistance of the wire ($R_{dc} = \frac{\rho l}{nA}$), l is the length of the wire, A is the cross-sectional area of a single litz strand and Fr is an approximation that relates the dc los with ac loss when the current is sinusoidal

$$Fr = 1 + \frac{\pi^2 w^2 \mu^2 {n_s}^2 n^2 dw^6}{768 \rho^2 B_w^2} \tag{4.12}$$

Here n is the number of litz strands in the wire, d_w is the diameter of the strand, n_s is the number of turns of wire, and B_w is the breadth of the core window area. This expression shows that winding loss increases with increase in frequency, however, the diameter of strands (d_w) used decreases (as lower gauge wires are used). This results in an increase in the number of strands (n_s).

Copper foil is used for the primary winding of the transformer. If the width of the copper foil (d) is approximately equal to the skin depth (δ) then the power loss can be approximated by

$$P_{w\_foil} = I_{rms}^2 R_{dc} (\frac{d}{\delta}) \tag{4.13}$$

In Figure 4.6, the total loss is provided (This figure does not include capacitive loss, diode loss and the board trace loss.). The comparison of device loss in hard-switched converter and soft-switched converter is also given. The device loss is the loss in the transistors of the four switches

of the inverter. The magnetic loss is the inductor and transformer loss. As shown in the Figure 4.6, the device losses increase with frequency while the magnetic loss in general decreases with frequency. The limited availability of the wire gauges and number of strands per litz wire were taken in to account while estimating the magnetic loss.

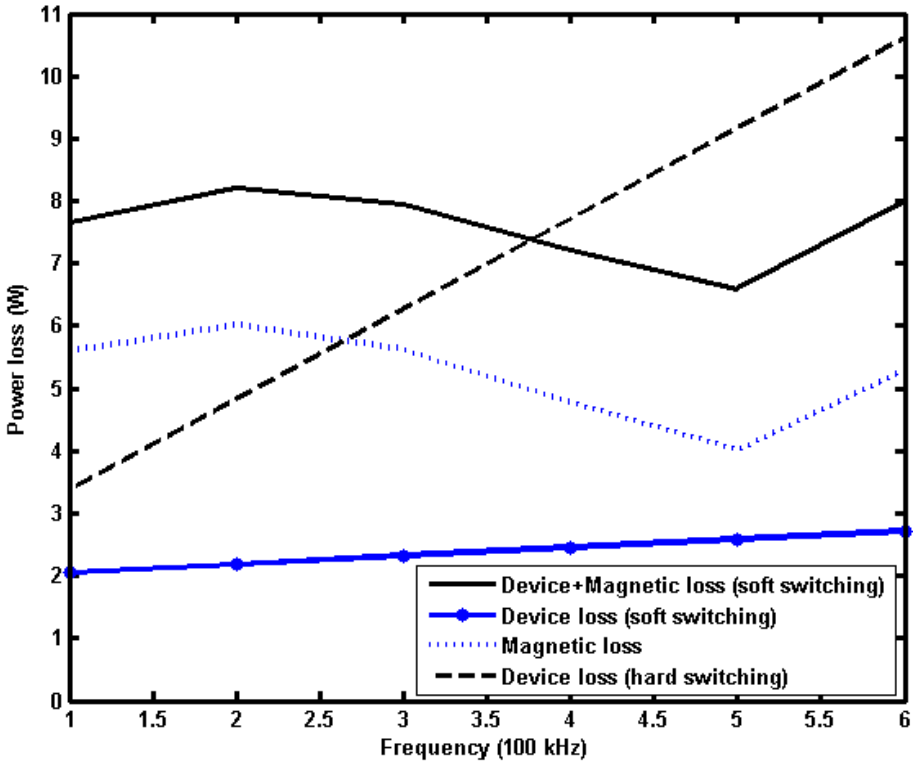


Figure 4.6: Comparison of power loss in hard switched and soft switched converters

4.3.3. Capacitor Loss

Conduction loss is the dominant loss in capacitors. It is due to the equivalent series resistance (ESR), R_{ESR} of the capacitor. As, the ESR varies with frequency, the frequency of operation determines the type of capacitor used.

The loss can be estimated as:

$$P_{cap} = I_{rms}^2 R_{ESR} \tag{4.14}$$

Figure 4.7 shows the variation in ESR of mica dielectric capacitors, as given in the datasheet of type MC mica dielectric capacitors. These capacitors are much suitable at a higher frequency but they have been used due to their high stable capacitance value characteristics.

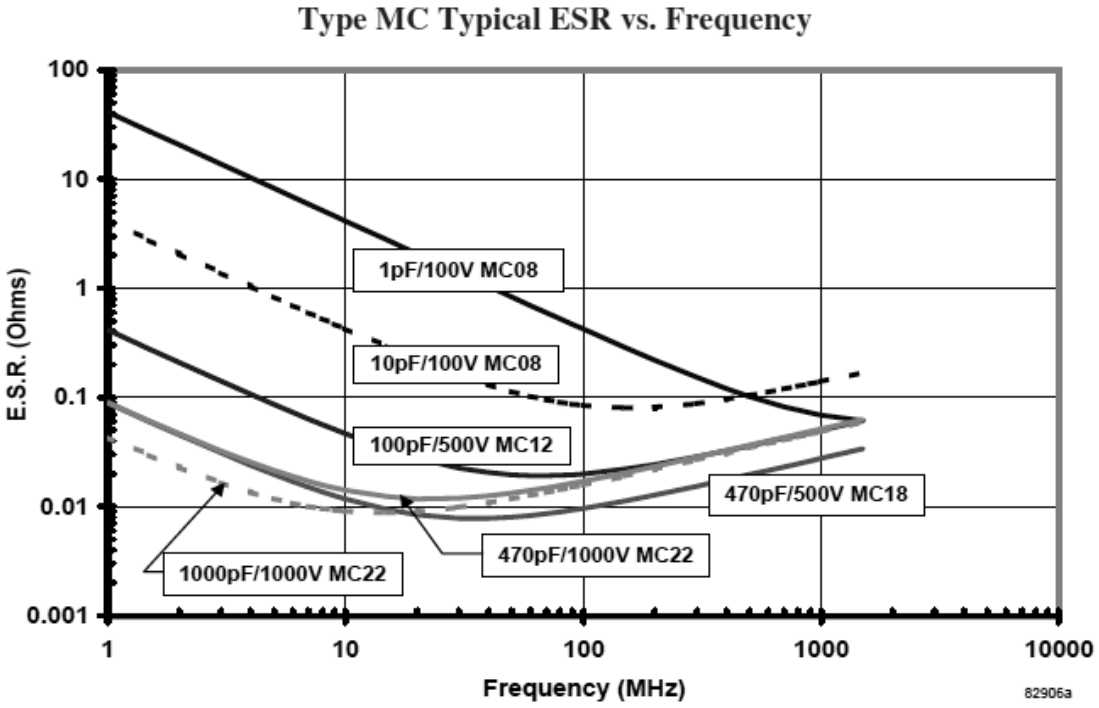


Figure 4.7: Equivalent Series Resistance (ESR) as a function of frequency for mica dielectric capacitors.

4.4 Design of Second Prototype

The second prototype was designed using the same methodology presented in Chapter 2 and 3. However, in this case 500 kHz switching frequency was used. Hence, the value of inductance and capacitance decreased by a factor of 5. All the magnetic components were redesigned. The transformer was wound using Litz wire with thinner wires and thinner copper foil. The inductors were also wound using Litz wire with thinner strands. However, the size of the core was not changed as the objective was to enhance efficiency rather than decrease size. Two transistors were used in parallel to further reduce the loss. The prototype board was also redesigned to achieve less parasitics in order to minimize the loss. The components used in the second prototype are listed in Table 4.3.

It was predicted that with these changes a much higher efficiency would be achieved, however, due to the increased ringing of the parastics of the transformer this was not seen. An efficiency of 93% at 25V input was recorded.

Table 4.3: Components used in the experimental prototype

Components	Selected Parts
Transistors	GaN HEMTS -EPC 2001, 2 in parallel per switch
Diodes	SiC schottky Diode- C3D02060E
Transformer	RM12 core, Copper foil (4 turns, 5 mils width, 3 mils thickness, 3 foils in parallel) and litz wire (40 turns, 46AWG, 220 strands in parallel)
Capacitors	C_s: 1300pF, Mica capacitor, C_r: 1000pF (560pF capacitor used as both are in series)
Inductors	L_s: 77.9uH, RM12A080 3F3 core, litz wire (31 turns, 46AWG, 450 strands in Parallel) L_r: 103uH, RM12A060 3F3 core, litz wire (41 turns, 46AWG, 450 strands in Parallel)
Drivers	LM5113
Controller	TMS320F28335

4.5 Experimental Results

A photograph of the experimental prototype is shown in Figure 4.8. The board is smaller than the first prototype.

The current and voltage waveforms from the experimental setup are shown in Figure 4.9 and Figure 4.10. Figure 8 shows the gate voltages of switch S_1 and S_3, the voltage across switch S_3 and the current entering the primary of the transformer. Figure 4.10 shows these same waveforms during the turn-on and turn-off transitions. During turn on ZVS can observed while at turn off near ZCS is seen.

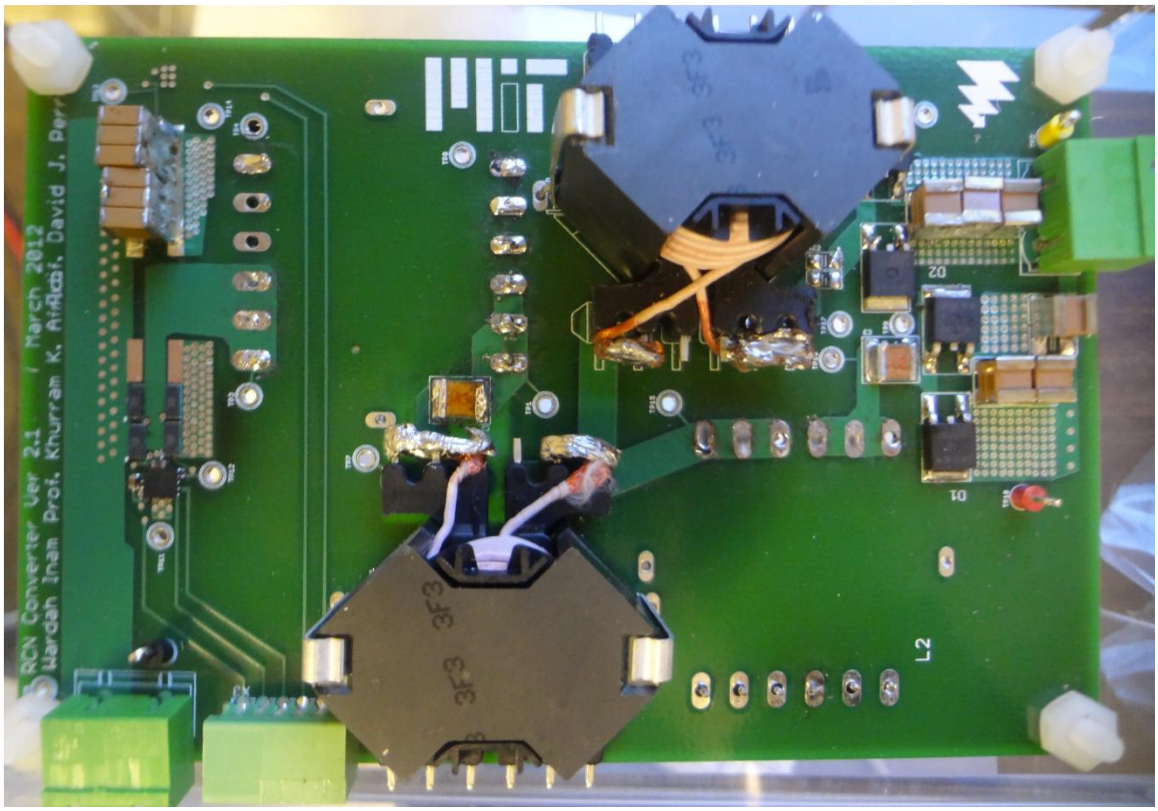


Figure 4.8: Second prototype experimental board

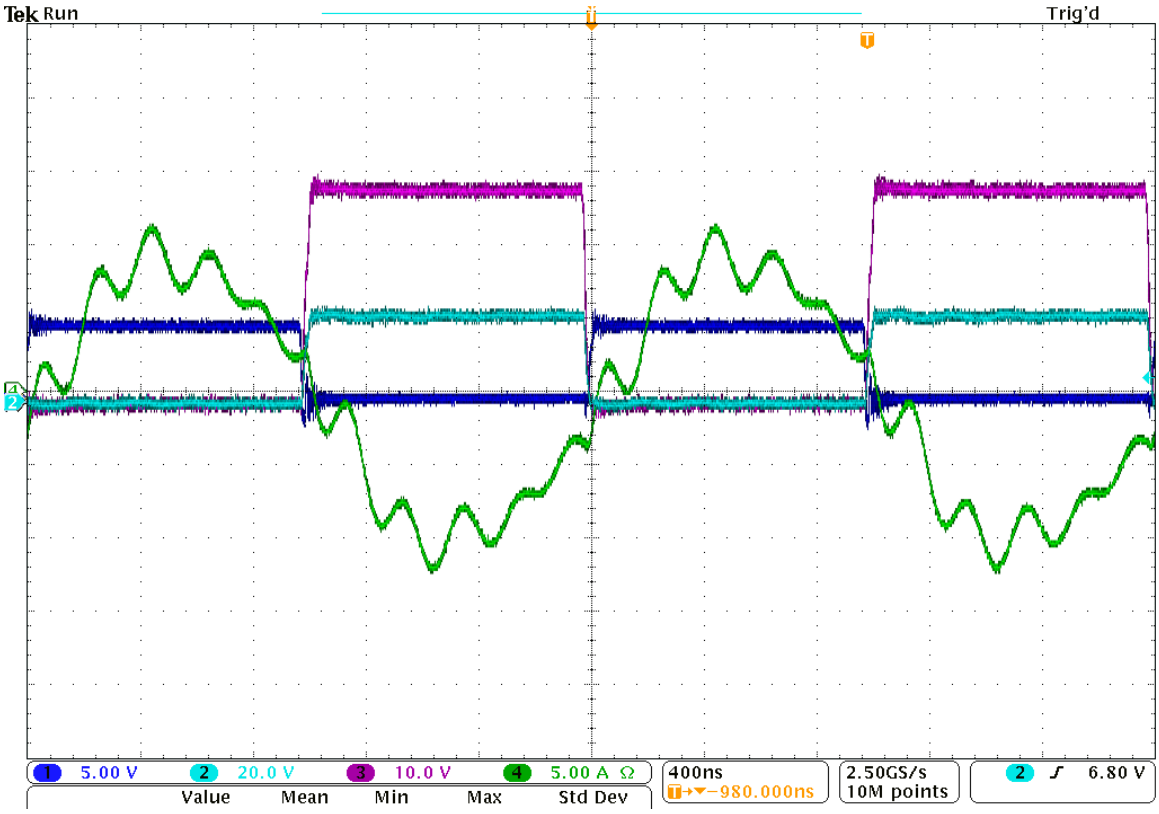
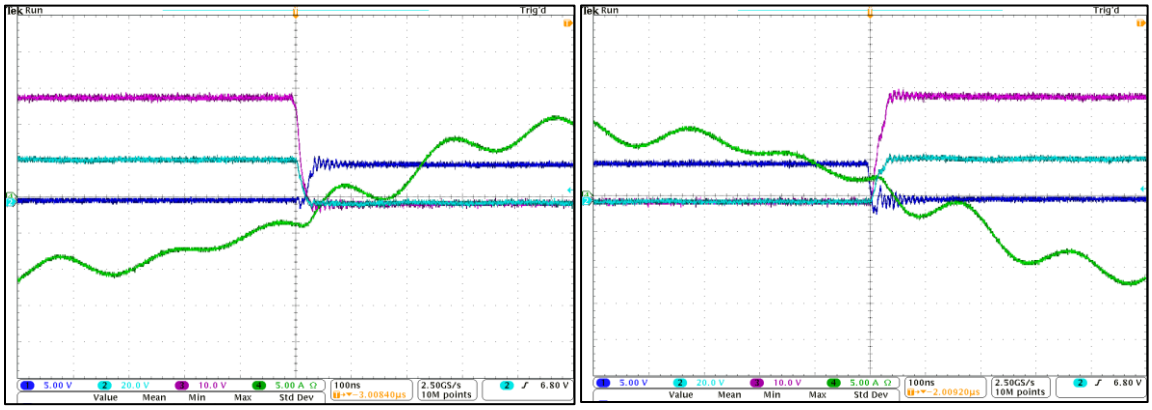


Figure 4.9: (1) Gate voltage (V_{GS_2}) of switch S_3 (2)Voltage (V_{DS}) across switch S_3 and (3) Gate voltage (V_{GS_1}) of switch S_1 (4) Current at the primary of the transformer with 25 V input voltage



(a) (b)

Figure 4.10: Soft switching at (a) Turn-off transition (b) Turn-on transition

An increase in ringing in the current waveform can also be seen in Figure 4.9 and Figure 4.10. This causes additional high frequency loss. This ringing is removed in the third prototype by introducing a matching network in the proposed topology. The prototype had an efficiency of 93%. This next chapter focuses on removing this ringing and enhancing the converter efficiency in the third prototype.

Chapter 5

Third Converter Prototype

The efficiency of the second prototype was lower than expected due to the excessive ringing in its current waveform. In fact its efficiency was even lower than the first prototype. In this chapter the third and final prototype is presented. The second prototype had a slightly different transformation stage than the first two prototypes. Its transformation stage included a matching network (that also acted as a parallel resonant tank) on the primary side of the transformer instead of the series resonant tank on the secondary side of the transformer, as shown in Figure 5.1. The following sections discuss the design details and the experimental prototype.

5.1 Transformation Stage Redesign

The only differences between the second and the third prototype are in the transformation stage. These differences are:

- Introduction of a matching network, which also displaces a series resonant tank
- Reduction of the turn ratio of the transformer

The matching network is placed at the output of the inverter. As discussed in Chapter 2, the matching network consists of an inductor L_{rp} and a capacitor C_{rp} as shown in Figure 5.2. In Figure 5.2 the load Z_{i1} in parallel with the capacitor models the circuit to the right of the matching network (transformer, RCN and rectifier stage) at the switching frequency. The matching network not only provides filtering, but also provides a voltage gain that reduces the voltage gain requirement of the transformer. The matching network is show in Figure 5.2.

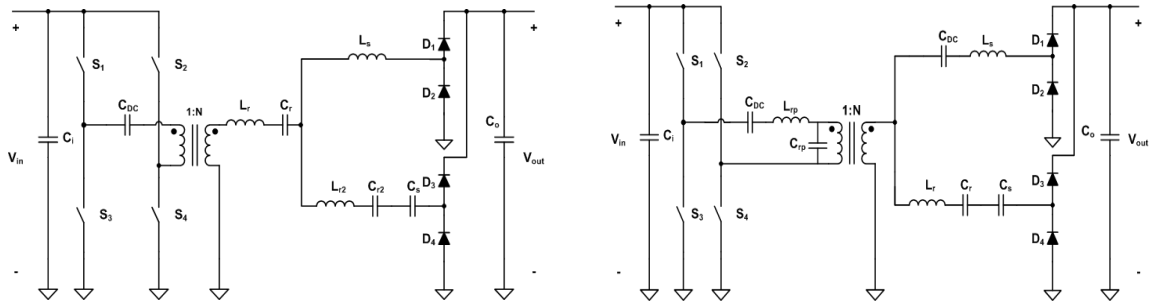


Figure 5.1: (a) Circuit topology of 1st and 2nd Prototype (b) Circuit topology of 3rd Prototype

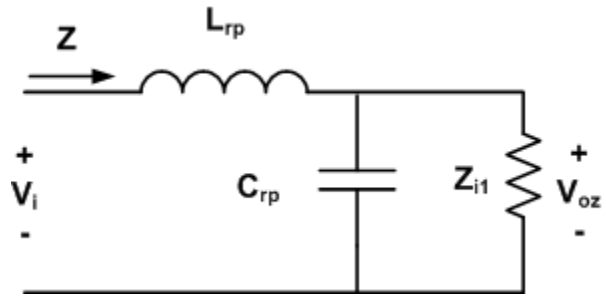


Figure 5.2: Matching network with equivalent impedance

The gain of this matching network is given by:

$$G = \frac{1}{\sqrt{(\frac{\omega L_{rp}}{Z_{i1}})^2 + (1-\omega^2 L_{rp} C_{rp})^2}}. \tag{5.1}$$

where ω is the angular (switching) frequency and L_{rp} , C_{rp} and Z_{i1} are shown in Figure 5.2. The input impedance of the matching network is given by:

$$Z = \frac{j\left(X_{Lrp} {Z_{i1}}^2 + X_{Crp}^2 X_{Lrp} - X_{Crp} {Z_{i1}}^2\right) + X_{Crp}^2 Z_{i1}}{{Z_{i1}}^2 + X_{Crp}^2} \tag{5.2}$$

.

To choose the values of L_{rp} and C_{rp} , in the start it was assumed that $X_{Lrp}\left(= \omega L_{rp}\right) = X_{crp}\left(= \frac{1}{\omega C_{rp}}\right)$. This choice results in a simplified expression for the gain of the matching network:

$$G_s = \frac{Z_{i1}}{\omega L_{rp}} \tag{5.3}$$

However, if $X_{Lrp} = X_{crp}$, then the impedance looking into the matching network is inductive and is given by:

$$Z = \frac{j\left(X_{Crp}^3\right) + X_{Crp}^2 Z_{i1}}{{Z_{i1}}^2 + X_{Crp}^2} \tag{5.4}$$

.

This results in the input current of the matching network leading its input voltage by an angle θ given by:

$$\theta = \tan^{-1}\left(\frac{X_{crp}}{Z_{i1}}\right) \tag{5.5}$$

.

Since the current needs to be in phase with the fundamental of the voltage to achieve near zero-current switching in the inverter so $X_{Lrp} = X_{crp}$ cannot be used in the actual design of the matching network and this assumption is made as only the starting point to simplify the analysis.

The values of the components of the matching network (L_{rp} and C_{rp}) are found assuming the combined gain of the matching network and transformer is equal to the gain of the transformer in the first two prototypes (i.e. gain of 10). The values of L_{rp} and C_{rp} that satisfy this criteria for different values of matching network gain are shown in Figure 5.3. Note as the gain of the matching network G increases, the gain of the transformer decreases by a factor of G.

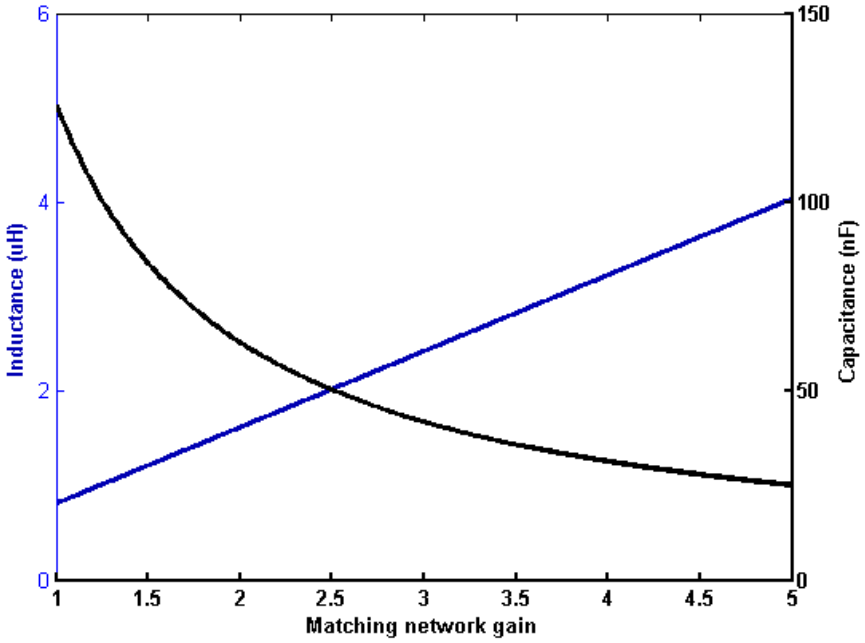


Figure 5.3: Required inductance and capacitance values of L_{rp} and C_{rp}, respectively, as a function of gain of the matching network

An optimal value of the matching network gain G is chosen to keep the total losses in the inductor and the transformer to a minimum. If more gain is provided by the matching network, the value of inductance needed increases and the losses in L_{rp} also increase. However, this results in a decrease in the gain of the transformer. Hence, the number of secondary turns in the transformer decrease, which decrease the winding loss. However, the volts seconds at the transformer primary increase thus increasing the core loss. Therefore, these losses need to be traded in identifying the optimal value of G (between 1.5 and 2, as this decreases the gain of the transformer approximately by half). As the starting point, G= 1.75 is chosen, this value of G corresponds roughly a value of 70 nF for C_{rp} (See Figure 5.3) and $X_{crp}\left(=\frac{1}{\omega_o C_{rp}}\right)$ is 4.54 Ω. For the input impedance of the matching network to be purely resistive the reactance of the inductor L_{rp} has to satisfy:

$$X_{Lrp} = \frac{X_{Crp} Z_{i1}^2}{{X_{Crp}}^2 + {Z_{i1}}^2} \tag{5.6}$$

For this converter Z_{i1} is 7.07 Ω at an input voltage of 25 V.

The actual gain of the matching network with the above values of Z_{i1}, L_{rp} and C_{rp} at 25 V input is:

$$G = \frac{1}{\sqrt{(\frac{\omega L_{rp}}{Z_{i1}})^2 + (1-\omega^2 L_{rp} C_{rp})^2}} = 1.7. \tag{5.7}$$

This gain is fairly constant across variation in input and output voltage as the resistance compression network (RCN) reduces the variation in the value of load Z_{i1}. The most significant advantage of the matching network is that the ringing caused by the transformer leakage inductance resonating with the secondary winding capacitance is not present. The inductor of the matching network adds to the leakage inductance of the transformer which increases the total inductance and thus decreasing the resonant frequency. This is shown in Figure 5.4.

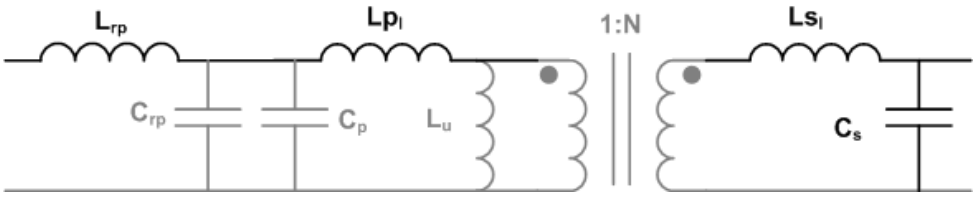


Figure 5.4: Inductance of the matching network adds to the leakage inductance of the transformer. This mitigates the ringing observed in the previous prototypes.

5.2 Simulation Results

The simulation waveforms for converter with the matching network are shown in Figure 5.5. It shows the input voltage, the input current and the output voltage of the matching network. As can be seen from Figure 5.5, the ringing in the current has been eliminated. Also, unlike in the case of the first two prototypes primary-side voltage of the transformer (which is the same as the output voltage of the matching network) is near sinusoidal.

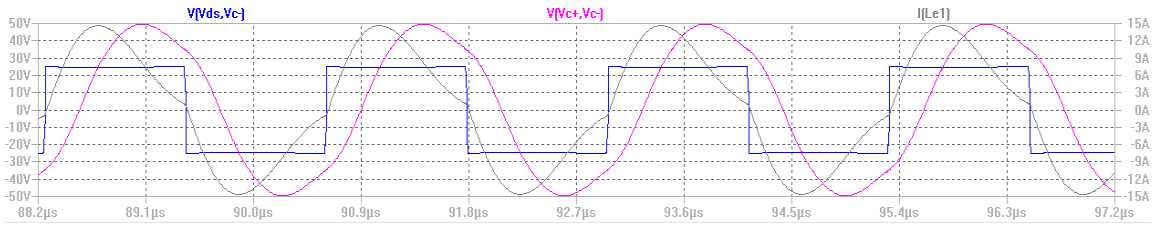


Figure 5.5: Input voltage, V(Vds,Vc-), Output voltage, (Vc+, Vc-), and input current, I(Le1), of the matching network

5.3 Experimental Prototype and Results

The components used in the third prototype are listed in Table 5.1

Table 5.1: Summary of components of the third experimental prototype

Components	Type
Transistors	GaN HEMTS -EPC 2001, 2 in parallel per switch
Diodes	SiC schottky Diode - C3D02060E
Transformer	RM12 core, Copper foil (4 turns, 5 mils width, 3 mils thickness, 3 foils in parallel) and litz wire (24 turns, 46AWG, 450 strands in parallel)
Capacitors	C_s: 1300pF, Mica capacitor, C_r:1000pF (560pF cap was used as both are in series)
Inductors	L_{rp}: 1 µH, RM12A115 3F3 core, litz wire (3 turns, 46AWG, 3600 strands in parallel). Ls: 78 µH, RM12A080 3F3 core, litz wire (28 turns, 46AWG, 450 strands in parallel) Lr: 101 µH, RM12A060 3F3 core, litz wire (41 turns, 46AWG, 450 strands in parallel)
Drivers	LM5113
Controller	TMS320F28335

To test the performance of this converter the input voltage was varied from 25 V to 40 V while the output was fixed at 400 V. In a second set of experiments the output voltage was varied from 250 V to 400 V with the input fixed at 25 V. The input and output current and voltage were measured to determine the efficiency.

5.3.1. Input variation

The input was varied from 25 V to 40 V with output voltage fixed at 400 V. The scope images for 25 V, 32.5 V and 40 V were collected. The worst case currents at the switching transitions are 15.7% of peak current at $V_{in} = 25$ V, 13.6% at $V_{in} = 32.5$ V and 18.9% at $V_{in} = 40$ V. By adjusting the converter switching frequency over a narrow range from 425 kHz to 500 kHz the maximum instantaneous power is controlled across input voltage (with higher frequencies for lower voltages) as voltage increases.

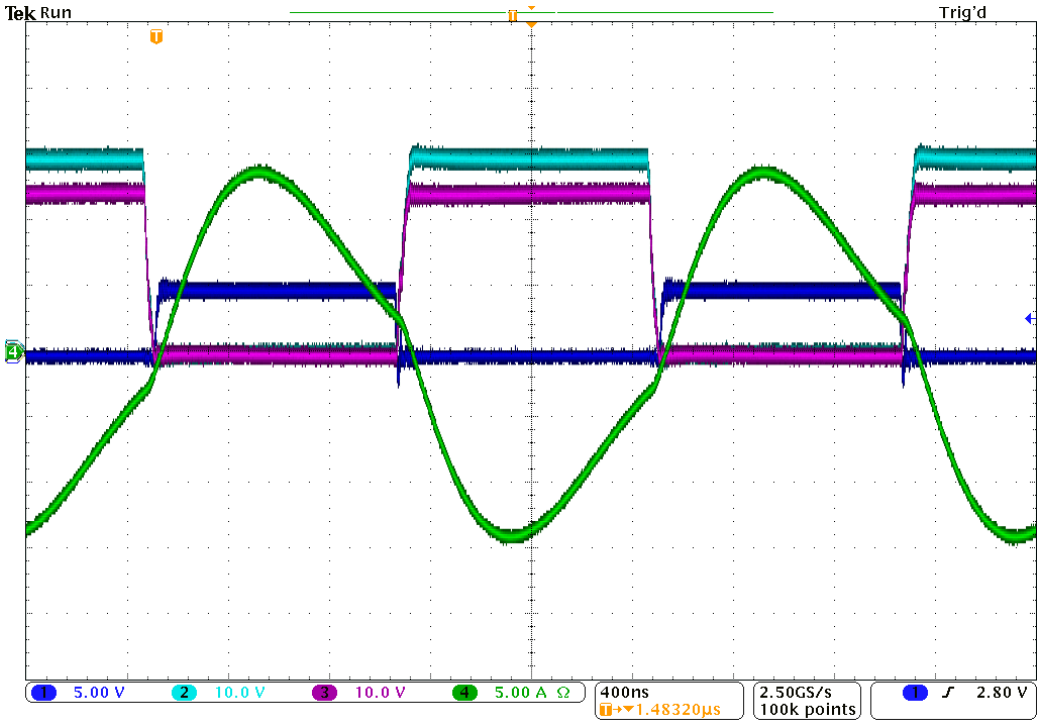
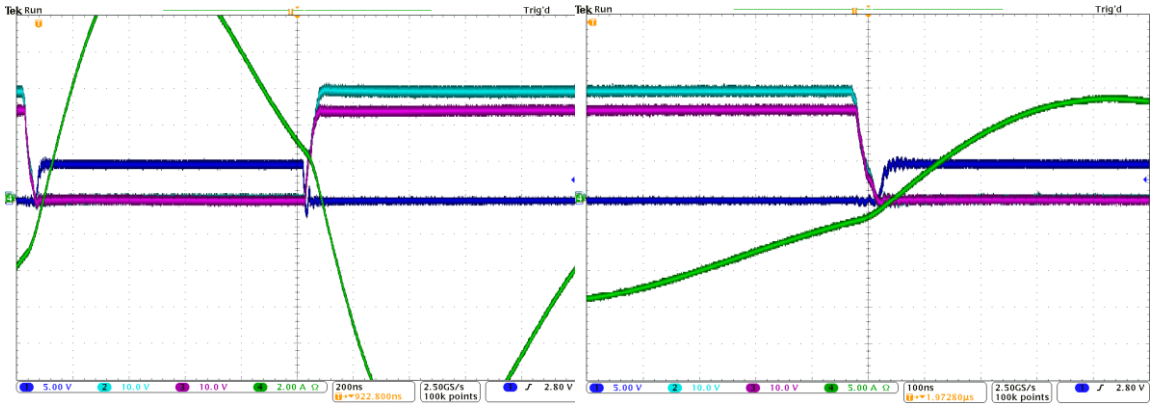


Figure 5.6: (1) Gate voltage (V_{GS_2}) of switch S_3 (2) Gate voltage (V_{GS_1}) of switch S_1 (3)Voltage (V_{DS}) across switch S_3 and (4) Input current of the parallel tank with 25 V input voltage

For 25 V input the current and voltage waveforms are shown in Figure 5.6 and Figure 5.7. In Figure 5.6 two periods of the switching cycle are shown. The input current of the parallel tank (green waveform) appears to be nearly sinusoidal and the ringing observed in the previous two prototypes is no longer present.

When the gate voltage (blue waveform) is applied to switch S_3, the switch starts to conduct and the current flows through it and into the parallel tank. In the next half cycle, the gate voltage (turquoise waveform) is applied to switch S_1 and S_1 starts to conduct so the current flows through it and in to the parallel tank.

In Figure 5.7 (a) the turn off transition of switch S_3 is shown. The turn-off current through switch S_3 is very small compared to the maximum current in the switch (15.7% of the maximum). In Figure 5.7 (b) the turn-on transition of switch S_3 is shown. Before the switch is turned on the voltage across the switch falls to zero.



(a) (b)

Figure 5.7: Soft switching at (a) Turn-off transition (b) Turn-on transition

For 32.5 V input voltage, the waveforms are shown in Figure 5.8. In this case the switching frequency is 425 kHz. The input current to the parallel tank (green waveform) is nearly sinusoidal but less than at 25 V input voltage. This is due to the fact that we are switching below resonance. However, both ZVS and near ZCS are observed. For 40 V, the waveforms are shown in Figure 5.9 and Figure 5.10. In this case the switching frequency is also 425 kHz.

The waveforms for the output variation are given in the Appendix A.

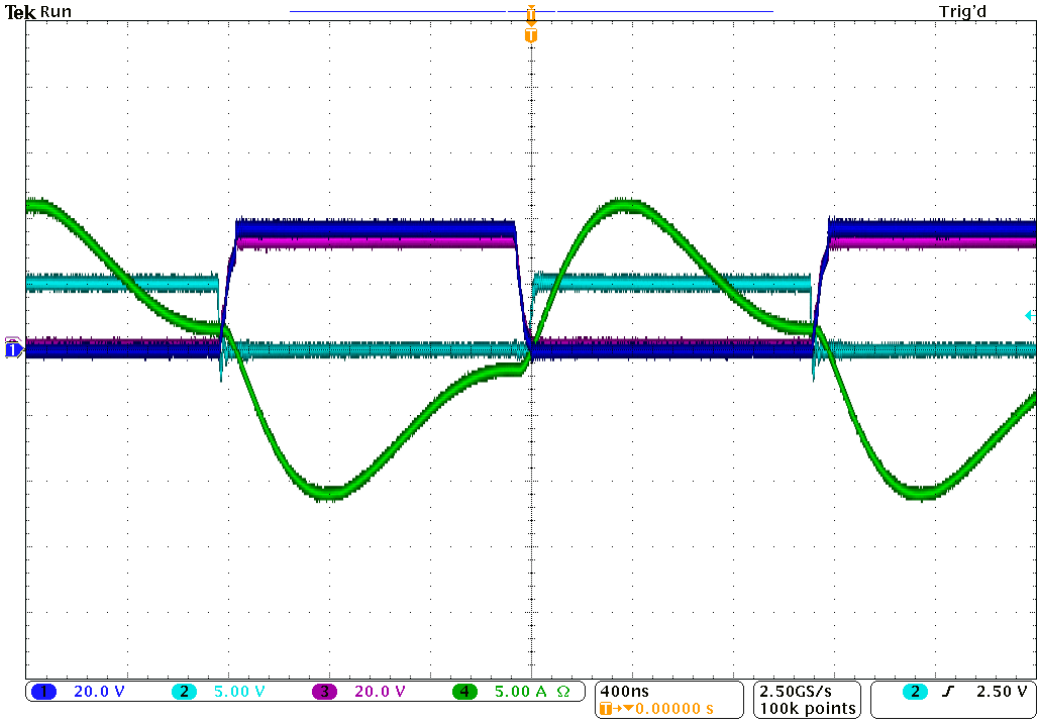


Figure 5.8: (1) Gate voltage (V_{GS_1}) of switch S_1 (2) Gate voltage (V_{GS_3}) of switch S_3 (3)Voltage (V_{DS}) across switch S_3 and (4) Input current of the parallel tank with 32.5 V input voltage

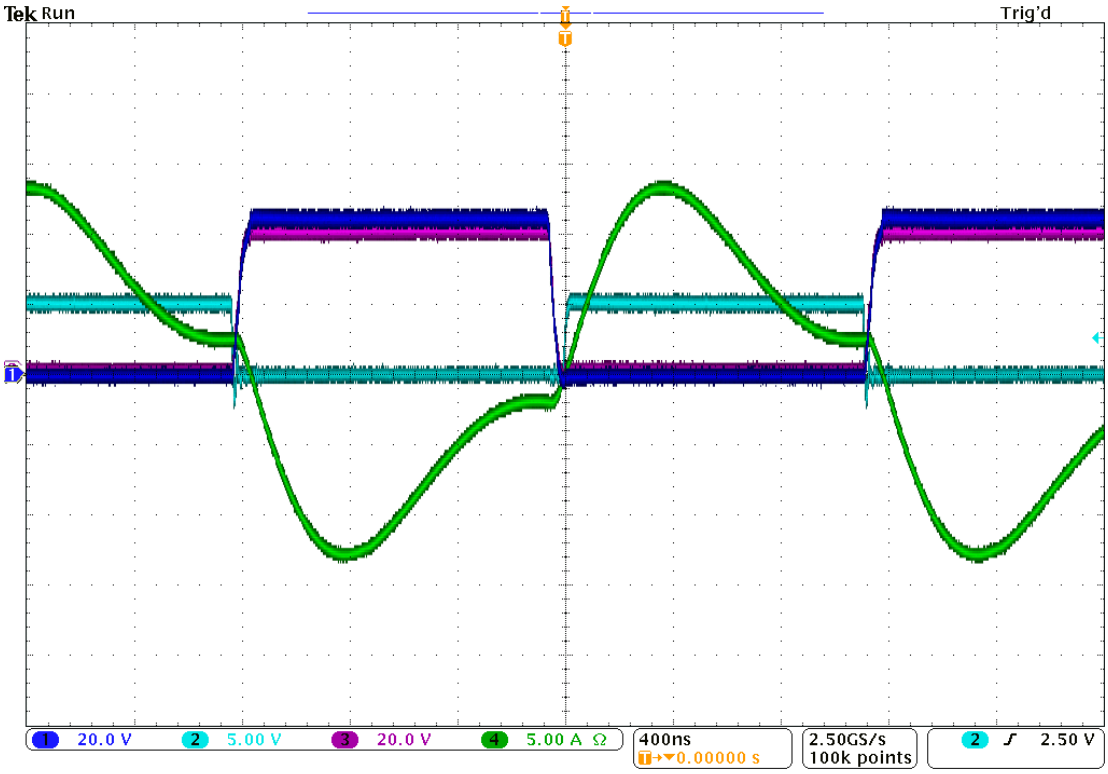
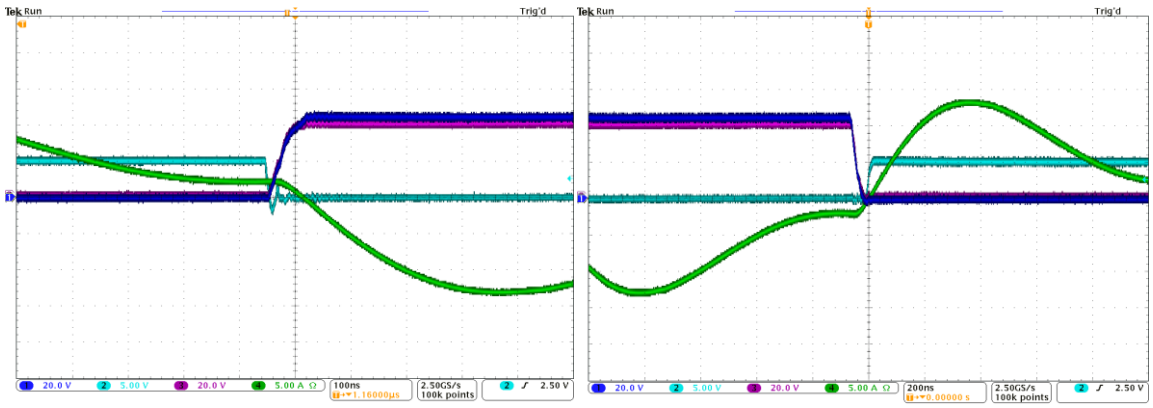


Figure 5.9: (1) Gate voltage (V_{GS_1}) of switch S_1 (2) Gate voltage (V_{GS_3}) of switch S_3 (3)Voltage (V_{DS}) across switch S_3 and (4) Input current of the parallel tank with 40V input voltage



(a) (b)

Figure 5.10: Soft switching at (a) Turn-off transition (b) Turn-on transition

5.4 Efficiency

The measured efficiency of the converter as a function of input voltage and output voltage is shown in Figure 5.11 and Figure 5.12, respectively. As can be seen from Figure 5.11 the efficiency of the converter varies from 95% to 95.64% and maximum output power varies from 200 W to 325 W across the full range of input voltage with the output voltage at 400 V. Figure 5.11 also shows how output power varies with the change in input voltage again with output voltage at 400 V. This is the maximum power that can be delivered by this converter at the corresponding input voltage. The output power can be regulated to a desired level through the use of on-off control as discusses earlier in Chapter 2. When the output voltage is varied from 400 V to 250 V with input votlage held at 25 V, the ouptut power decreases slightly from 203 W to 195 W, as shown in Figure 5.12. Also the efficiency of the converter drops from 95% to 93.7% with the change in output voltage (see Figure 5.12) . This is because the current flowing through the circuit now increases. These results demonstrate that the proposed topology can offer high efficieny, ZVS and near ZCS operation over a wide input and output voltage range.

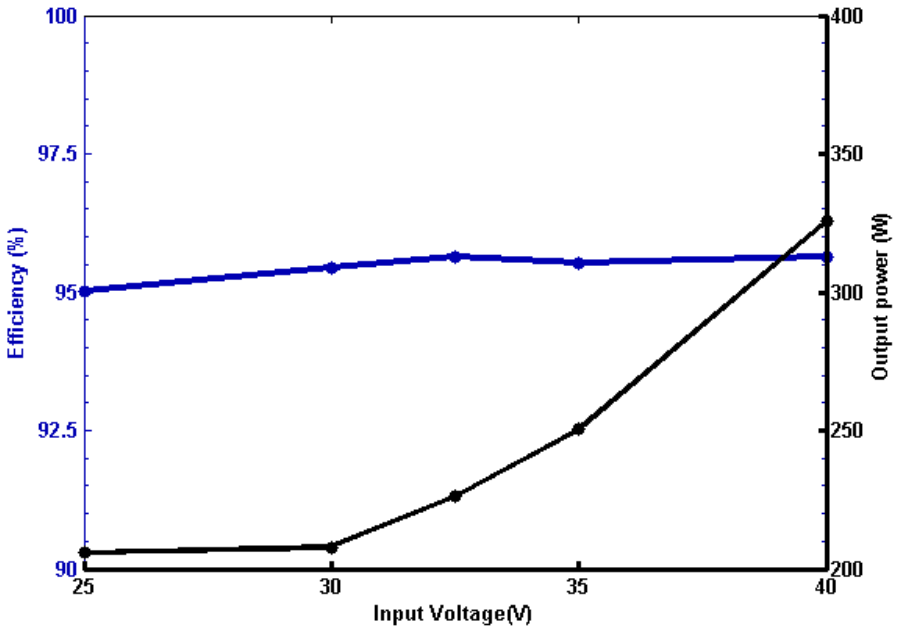


Figure 5.11: Measured efficiency and output power versus input voltage variation (with output voltage at 400 V)

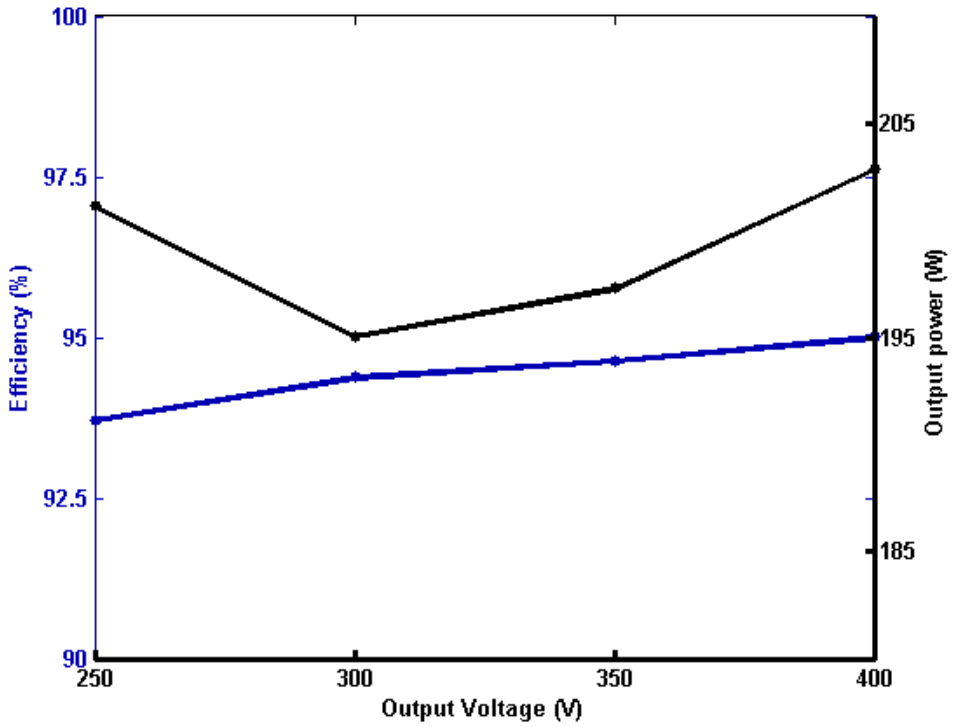


Figure 5.12: Measured efficiency and output power versus output voltage variation (with input voltage at 25 V)

Chapter 6

Summary and Conclusion

This chapter summarizes the work presented in this thesis and highlights its contributions. It also identifies future work that can result in valuable contributions to knowledge.

6.1 Thesis Summary

This thesis presents a new resonant dc/dc converter topology that utilizes a resistance compression network to provide simultaneous zero voltage switching and near zero current switching across a wide range of input and output voltage and power levels.

Chapter 1 introduces the concepts used in this thesis for reducing switching losses to minimize total losses. The magnetics are designed to shape the current in order to achieve soft switching over the entire range of operation. Zero Voltage Switching is obtained by letting the voltage across the switch ring to zero before it is turned on. Zero Current Switching is obtained by turning off the switch when the current through it is almost zero. This reduces the overlap of current and voltage waveforms thus decreasing the power loss.

Chapter 2 presents the new topology proposed in this thesis. It is a dc/dc resonant power converter which utilizes a resistance compression network to provide soft switching over a wide input voltage, output voltage and power range. The three stages of the converter (inverter stage, transformation stage and rectifier stage) are optimally designed to reduce the overall loss. The inverter is a full-bridge inverter, the transformation stage consists of a step up transformer for gain, series resonant tank for filtering and resistance compression network to limit the maximum output power and to reduce the effect of the change of load. The rectifier stage consists of two half bridge diode rectifiers. Two variants of the topology are presented.

Chapter 3 provides detailed design of the first prototype. This is designed for solar power applications where interface circuitry is needed to connect photovoltaic panels to the grid. This

dc/dc converter is used to boost voltage of individual photovoltaic panels to a high dc-link voltage, with follow-on electronics for converting dc to ac. This prototype was designed as a proof of concept and its performance showed the advantage of using the proposed topology to reduce the switching losses.

Chapter 4 presents the design and experimental results of the second prototype. The effect of frequency on the component losses is discussed. With increases in frequency the switching losses increase. The magnetics have to be optimally designed to reduce the total losses. This converter operates at 500 kHz. However, the transformer parasitics resonate to cause undesired ringing resulting in high frequency losses and lowered efficiency.

Chapter 5 discusses the final prototype. It provides details of including a matching network in order to mitigate the ringing caused by resonating parasitics of the transformer. It achieves high efficiencies over the input and output voltage range thus demonstrating the effectiveness of the approach.

6.2 Thesis Conclusion

The proposed converter overcomes the challenges faced by many previously-reported resonant converters, and achieves very high efficiency by maintaining ZVS and near ZCS over a wide input and output voltage and power range. It utilizes Resistance Compression Network (RCN) to successfully reduce the affect of the change of load.

Many high gain dc/dc converters using transformers face the issue of resonating parasitics causing high frequency ringing. This was mitigated by incorporating a matching network. This technique can also be used in other high gain converters.

The experimental results from a 200 W prototype show that the converter mainatains an efficiency of over 95% across its entire input voltage range (25 V – 40 V) at the designed output voltage of 400 V, and an efficiency of over 93.7% even as output voltage is reduced down to 250 V, demonstrating the successful application of this approach.

6.3 Recommendations for Future Work

This thesis has presented one successful implementation of the resistance Compression Network (RCN) dc/dc converter. However, other implementations of this concept still need to be explored.

Diode half bridge rectifiers were used in this converter. Other rectifier approaches can also be studied. Synchronous rectification (using actively controlled switches) also seems like a viable option.

In general, the techniques provided in this thesis are not limited to grid connected dc/dc converters for solar applications and they can be extended to many other applications.

Appendix A

A.1 Waveforms for the Variation of the Output Voltage

The scope waveforms for the third prototype with variable output are given in this section.

Figure A. 1, shows current and voltage waveforms for 25 V input and 250 V output at 200 W power level. Figure A. 2 has 300 V output voltage and Figure A. 3 has 350 V output voltage. The switching frequency is kept constant as the output voltage varies.

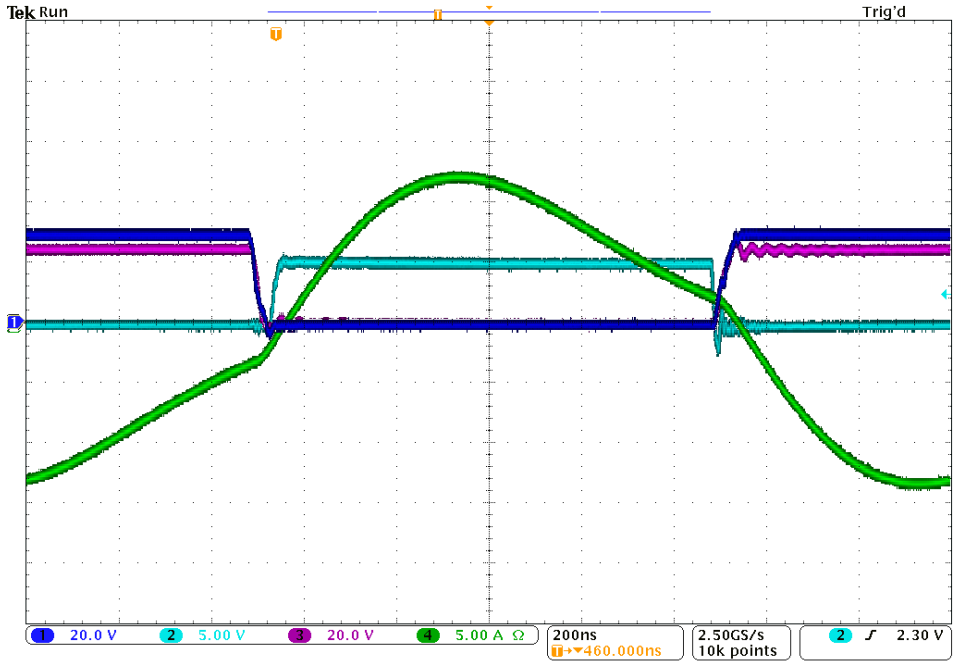


Figure A. 1: (1) Gate voltage (V_{GS_1}) of switch S_1 (2) Gate voltage (V_{GS_3}) of switch S_3 (3)Voltage (V_{DS}) across switch S_3 and (4) Input current at the primary of the transformer with 25 V input voltage and 250 V output voltage

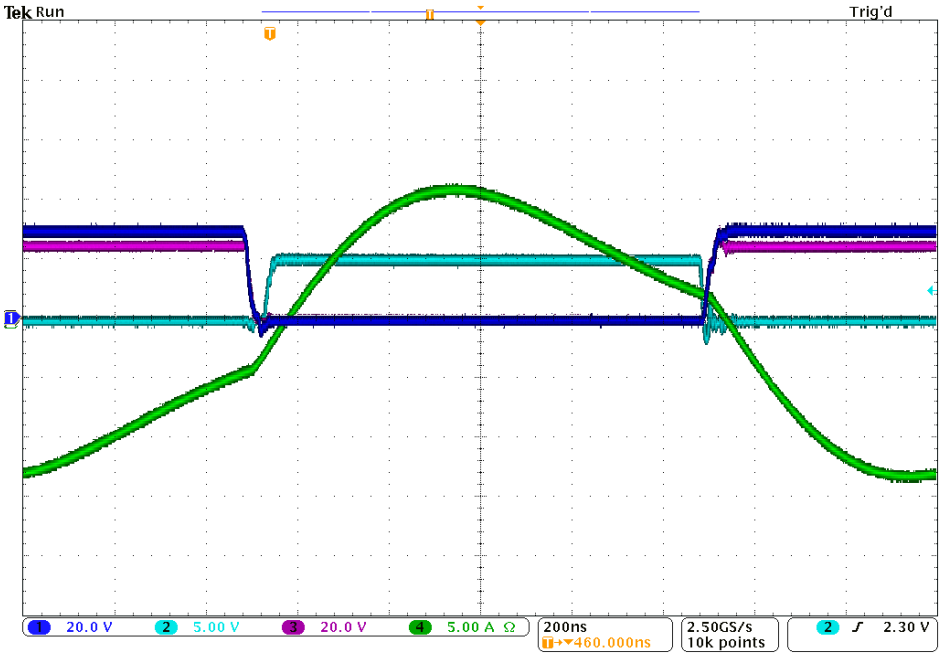


Figure A. 2: (1) Gate voltage (V_{GS_1}) of switch S_1 (2) Gate voltage (V_{GS_3}) of switch S_3 (3)Voltage (V_{DS}) across switch S_3 and (4) Input current at the primary of the transformer with 25 V input voltage and 300 V output voltage

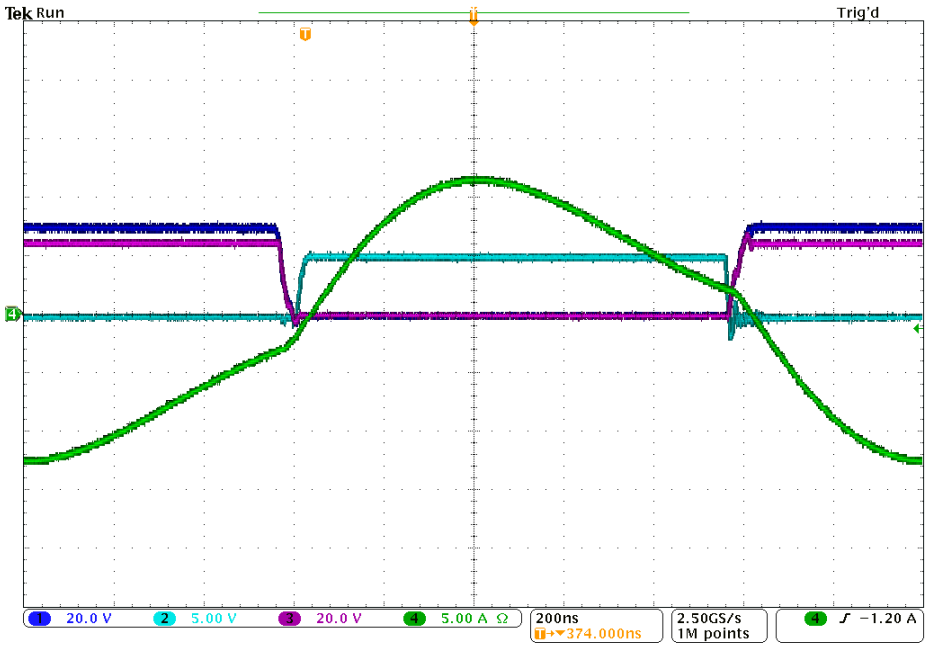


Figure A. 3: (1) Gate voltage (V_{GS_1}) of switch S_1 (2) Gate voltage (V_{GS_3}) of switch S_3 (3)Voltage (V_{DS}) across switch S_3 and (4) Input current at the primary of the transformer with 25 V input voltage and 350 V output voltage

Appendix B

B.1 MATLAB Script for the Design of an Inductor for the First Prototype

```
%Design of inductor for RCN converter prototype 1
%--------------------------------------------------
%Operating parameters
clc
clear all
fsw= 100000; % Switching frequency
L=506 *10^-6;% Inductance
Imax=2.07; %Max Current

Irms=1.426; %RMS current
Bmax=0.3; %Max acceptable B (T)
Jmax=500*10^4; % A/m^2

w=2*pi*fsw;
mu=4*pi*10^-7; % Permittivity of free space
%--------------------------------------------------
%3F3 core parameters
Cm=0.25*10^-3;
x= 1.63;
y= 2.45;
ct2= 0.79*10^-4;
ct1=1.05*10^-2;
ct0=1.26;
T=50; %Temperature

%-------------------------------------------------------

%Cores of different size and different gap size

cores = [....
'RM08A100' ; 'RM08A160' ; 'RM08A250' ; 'RM08A315'; 'RM08A400' ;
....
'RM10A160' ; 'RM10A250' ; 'RM10A315' ; 'RM10A400'; 'RM10A630' ;
....
'RM12A160' ; 'RM12A250' ; 'RM12A315' ; 'RM12A400';
'RM12A630';....
'RM14A250' ; 'RM14A315' ; 'RM14A400' ; 'RM14A630'; 'RM141000'];

%AL is mH for 1000 Turns
Al = [100 ; 160 ; 250 ; 315 ; 400;...
    160 ; 250 ; 315 ; 400; 630;...
```

```
    160 ; 250 ; 315 ; 400; 630;...
    250; 315; 400; 630; 1000];

% A is effective core area in cm^2
A= [
       0.52 ; 0.52 ; 0.52 ; 0.52 ; 0.52;...
       0.83 ; 0.83 ; 0.83 ; 0.83;0.83 ; ...
       1.46 ; 1.46 ; 1.46 ; 1.46;1.46 ; ...
       1.98; 1.98; 1.98; 1.98; 1.98 ];

%core volume in cm^3
V= [2.440 ; 2.440 ;2.440 ;2.440 ;2.440;...
      4.310 ;4.310 ;4.310 ;4.310 ;4.310 ; ...
       8.340 ;  8.340; 8.340 ;  8.340 ;  8.340;...
        13.90 ; 13.90 ; 13.90 ; 13.90 ; 13.90 ];

%Mean Length per turn in m
MLT=[ 42; 42; 42; 42; 42;
    52 ; 52 ;52 ;52 ;52 ;
    61; 61; 61; 61; 61;
    71; 71; 71; 71; 71]*10^-3;

% % wa is core (bobbin) winding area
% wa=[30.9; 30.9;30.9;30.9;30.9;
%     44.2; 44.2; 44.2; 44.2; 44.2;
%     75; 75; 75;  75; 75; ]*10^-3;

% Rth is core thermal resistance in deg. C / W
Rth= [38 ; 38 ;38 ;38 ;38 ;
    30; 30; 30; 30; 30;
    23; 23; 23; 23; 23;
    19; 19; 19; 19; 19];

%Dimensions of the core
%Breadth of the bobbin
Bbob=[8.83; 8.83; 8.83; 8.83; 8.83; 10; 10; 10; 10; 10; 14.55;...
    14.55; 14.55; 14.55; 14.55; 18; 18; 18; 18; 18]*10^-3;
%Height of the bobbin
hbob=[3.475; 3.475; 3.475; 3.475; 3.475; 4.25; 4.25;...
    4.25; 4.25; 4.25; 5.1;  5.1; 5.1; 5.1; 5.1; 6; 6; 6; 6;
6]*10^-3;
%Breadth of the winding Area
BWindA=[ 10.8; 10.8; 10.8; 10.8; 10.8; 12.1; 12.1; 12.1; 12.1;
12.1;...
    16.8; 16.8; 16.8; 16.8; 16.8; 20.8; 20.8; 20.8; 20.8;
20.8]*10^-3;

%Wire
Wawg=40;%AWG of wire
%Number of Strands
n_strands=[3 4 5 6 7 8 9 10 15 20 25 30 40 50 60 75 100 125 150
175];
```

```
%Overall diameter of wire
od_litz= [7 8 9 10 11 11 12 13 16 18 20 22 26 29 31 35 40 45 50
54]*10^-5*2.54;

d=7.5*10^-2/sqrt(fsw); % Skin depth

rho=1.68*10^-8; % Resistivity of copper

dw=(2.54e-2)* 0.0050.*(92).^((36.-Wawg)./39); %Diameter of strand
Aw=pi*dw^2/4; %Cross-section area of strand
%-----------------------------------------------------------------
------------


for i = 1:20,

    N(i) = round(1000*sqrt(1000*L/Al(i))); % Number of turns of
wire

    B(i)= Al(i)*N(i)*Imax/A(i)*1e-5; % Peak B (Confirm that  its
not peak to peak ??)

    Pv(i)= (Cm*((fsw)^x)*((B(i))^(y))*(ct0-ct1*T+ct2*T^2))*1e-3;
    Pc(i)=Pv(i)*V(i); % Power loss in core

  %To find which strand wire can fit
for j=1:length(od_litz)
    n_turns_b(j)= floor(Bbob(i)/od_litz(j)) ; %Number of wires
that can fit in the breadth of core
    n_turns_h(j)=floor(hbob(i)/od_litz(j));
    n_turns(j)= n_turns_b(j)*n_turns_h(j); % Total number turns
that can fit in the core

    if n_turns(j)<N(i) %The number of turns that can fit
decreases as overall diameter of wire increases
    break              % When the number of  turns is less than
the required turns break the loop
    end
end

if j==1
    disp(['Litz cant fit ']); %if litz wire cannot fit at all
   j=2; %For consistency of the code
end
 litz_strands(i)=n_strands(j-1); % Get wire which has a diameter
less than the wire which broke the loop (So it can fit)
 %-----------------------------------
 lengthw(i)= MLT(i)*N(i); %Lenght of wire
 Resdc1(i)=rho*lengthw(i)/Aw;%DC Resistance of one wire
 Res(i)= Resdc1(i)/litz_strands(i);% Accounting skin effects
```

```
 Fr(i)=1 +
((pi^2*w^2*(mu)^2*N(i)^2*(litz_strands(i)).^2*(dw).^6)/(768*rho^2
*(BWindA(i)).^2));%Pac/Pdc

 Pw(i)=Irms^2*Res(i)*Fr(i); %Power loss in wire

 Ptot(i)= Pc(i)+Pw(i); %Total power loss
 Ptota(i)=Pc(i)+Pw(i) ; %Only accepted ones

     if B(i)> Bmax,
        disp([cores(i,:),' Rejected: Exceeds Bmax']);
        Ptota(i)=0;
     end;

Trise(i)= Ptot(i)* Rth(i); %Calculate the temperature rise

       if Trise(i)>150,
          disp([cores(i,:),' Rejected: Exceeds Max
temperature']);
          Ptota(i)=0;
      end;

end

%Plot the total loss, wire loss and core loss
p=plot([1:20], Ptot,'--rs',[1:20],Pw,'--bs',[1:20], Pc,'--gs',
'MarkerFaceColor','b','MarkerSize',4);
hleg1 = legend('Total loss','Winding loss',' Core loss');
set(gca,'XTick',1:1:20)
set(gca,'XTickLabel',{'8A100' ; '8A160' ; '8A250' ; '8A315';
'8A400' ; ...
'10A160' ; '10A250' ; '10A315' ; '10A400'; '10A630' ; ...
'12A160' ; '12A250' ; '12A315' ; '12A400'; '12A630';...
 '14A250'; '!4A315'; '14A400'; '14A630'; '14A1000'})
xlabel('Cores', 'fontweight','bold')
ylabel('Power loss (W)','fontweight','bold')
set(gca,'linewidth',2,'fontweight','bold')
set(p,'LineWidth',2.5)
figure

%Plot the accepted core's total loss
p=plot([1:20], Ptota,'--
rs','MarkerFaceColor','b','MarkerSize',8);
hleg1 = legend('Total loss');
set(gca,'XTick',1:1:20)
set(gca,'XTickLabel',{'8A100' ; '8A160' ; '8A250' ; '8A315';
'8A400' ; ...
'10A160' ; '10A250' ; '10A315' ; '10A400'; '10A630' ; ...
'12A160' ; '12A250' ; '12A315' ; '12A400'; '12A630'; ...
 '14A250'; '!4A315'; '14A400'; '14A630'; '14A1000'})
xlabel('Cores','fontweight','bold')
ylabel('Power loss (W)','fontweight','bold')
```

```
set(gca,'linewidth',2,'fontweight','bold')
set(p,'color', [0 0 0.7],'LineWidth',2.5)


% Find the core with minimum loss
for i=1:20;
    if Ptota(i)==0
        Ptota(i)=100;
    end
    [minP, I]=min(Ptota);
end
%Display the core with minimum loss
disp(['Using ',cores(I,:),' core'] );
disp(['The total loss is ',num2str(Ptota(I)),'W. The core loss is
',num2str(Pc(I)),'W and the copper loss is ', num2str(Pw(I)),'W']
);
disp(['Using ', num2str(Wawg),'AWG wire with ', num2str(N(I)),'
turns and of ',num2str(lengthw(I)),'m length. There are ',
num2str(litz_strands(I)),' strands in parallel' ]);
```

B.2 MATLAB Script for the Design of the Transformer

```
%%Design of Transformer

%%This script is used to design the transformer used and estimate
the
%%power loss. It tries to minimize the total loss by balancing
the copper
%%and core loss. It takes input of the cores, litz wire and foils
available
%%and optimizes the design considering these practical
limitations

%-----------------------------------------------
clc
clear all
%-----------------------------------------------

core='Rm12'; %Choose Core
%-----------------------------------------------

% Converter Parameters
Vo=400;
Vi=25; % Varies from 25-40
n=10; % Transformer turns ratio

%Converter Values
```

```
Iprms=10; % Max rms current through primary
Isrms= 1; % Max rms current through secondary
Pin=200;


switch core
    case 'Rm14'
    %Core Values RM14
    MLT=[71]*10^-3;
    Bbob=[18]*10^-3;
    hbob=[6]*10^-3;
    Ve= [13900]*10^-9;
    Amin=[168]*10^-6;
    BWindA=[20.8]*10^-3; % Breadth f winding area

    case 'Rm12'
    %Core Values RM12
    MLT=[61]*10^-3;
    Bbob=[14.55]*10^-3;
    hbob=[5.1]*10^-3;
    Ve= [8340]*10^-9;
    Amin=[125]*10^-6;
    BWindA=[16.8]*10^-3; % Breadth f winding area

    case 'Rm10'
    %Core Values RM10
    MLT=[52]*10^-3;
    Bbob=[10]*10^-3;
    hbob=[4.25]*10^-3;
    Ve= [4310]*10^-9;
    Amin=[89.1]*10^-6;
    BWindA=[12.1]*10^-3; % Breadth f winding area
    otherwise
        warning('Unexpected core');
end

%3F3 parameters (frequency dependent)
%100-300kHz, 300-500kHz and 500-1000kHz
Cm=[0.25*10^-3; 2*10^-5; 3.6*10^-9];
x=[1.63; 1.8; 2.4];
y=[2.45; 2.5; 2.25];
ct2= [0.79; 0.77; 0.67]*10^-4;
ct1=[1.05; 1.05; 0.81]*10^-2;
ct0=[1.26;1.28;1.14];

T=80;% Temperature

step=0.1; % step size for Bmax


mu=4*pi*10^-7; % Permittivity of free space
rho=1.68*10^-8; % Resistivity of Cu
```

```
mil=25.4*10^-6; % 1 mil in meters


widthpw=Bbob-1*10^-3; % Width of primary wire

n_strands=[3 4 5 6 7 8 9 10 15 20 25 30 40 50 60 75 100 125 150
175 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550
575 600];

od_litz1= [7 8 9 10 11 11 12 13 16 18 20 22 26 29 31 35 40 45 50
54 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135
140]*10^-5*2.54;% 40Awg
od_litz2= [6 7 7 8 9 9 10 10 13 15 16 18 23 23 25 28 32 36 40 43
48 52 56 60 64 68 72 76 80 84 88 92 96 100 104 108 112]*10^-
5*2.54;%42 Awg;
od_litz3=[4 5 6 6 7 7 8 8 10 11 13 14 16 18 20 22 25 28 31 34 37
40 43 46 49 52 55 58 61 64 67 70 73 76 79 82 86]*10^-5*2.54;% 44
AWG
od_litz4=[3.5 4 4.5 5 5.5 5.5 6 6.5 8 9 10 11 13 14 16 17 20 22
25 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60]*10^-
5*2.54;%46 AWG
od_litz5=[3 3 3.5 4 4.5 4.5 5 5 6.5 7 8 9 10 11 13 14 16 18 20 21
22 23 25 26 28 29.2 30.3 31.3 32.3 33.3 34.3 35.2 36.2 37.1 37.9
38.8 39.6]*10^-5*2.54; %48 AWG
Wawg_a=[40; 42; 42; 42; 46; 46];
od_litz_a= [od_litz1; od_litz2;
od_litz2;od_litz2;od_litz4;od_litz4];
thickpw_a= [mil*10 mil*5 mil*5 mil*5 mil*3 mil*3];
%%

for i=1:1:6;

    f=i*100*10^3;% Frequency of operation
    w= 2*pi*f;

    if f<=300000    % To decide 3F3 Coefficients
    fv=1;
    elseif f<=500000;
    fv=2;
    elseif f>500000;
    fv=3;
    end

skindepth(i)=7.5*10^-2/sqrt(f); %Skin depth for copper
flux_linkage= Vi/(2*f); % Flux linkage for square wave
l=ones(1,15); %Variable to store the number of copper foils used
in parallel

%%This is used to split copper loss and core loss equal. If the
minimum
%%loss can not be practically achieved it is rejected and a
higher loss
```

```
%%value is used.

for g=1:1:15

A_loss(g)=g*0.2; % Acceptable loss
Loss_core(g)= A_loss(g)/2; %Core loss
Loss_copper(g)= A_loss(g)/2; %Copper loss
%%For each loss value b is varied. The value that minimizes the
total loss
%%is chosen
    for Bmax=10:step:300
        B(g)=Bmax;
        Pc(g)= (Cm(fv)*f^(x(fv))*(B(g)*10^-3)^(y(fv))*(ct0(fv)-
ct1(fv)*T+ct2(fv)*T^2))*10^3*Ve*1.5; % Power dissipated in core
        if Pc(g)>Loss_core(g)
        break
    end
end

A_Bmax(g)= (B(g))*10^-3; % Acceptable Bmax

np(g)= round(flux_linkage/(2*A_Bmax(g)*Amin)); % Number of turns
of primary winding
ns(g)=n*np(g); % Number of turns of secondary winding

%% Estimating Loss in Primary wire
Lenpw(g)=MLT*np(g)*1.5; %Length of primary wire
Rdcp(g)= rho*Lenpw(g)/(skindepth(i)*widthpw);% Resistance of wire
Ppw(g)=Iprms^2*Rdcp(g)*2;%Factor of 2 take other high frequency
effects in to account
if (thickpw_a(i)*np(g)*1.3)>(hbob/2)
    disp('Warning:Primary wire does not fit in allocated area')
end

h_pw(g)=(thickpw_a(i)+4*mil)*np(g);

%Number of copper foils to be paralled
for k=2:5
    if(h_pw(g)*1.5*k)<(hbob/2)% If it fits half of the core area
        Rdcp(g)= (rho*Lenpw(g)/(skindepth(i)*widthpw))/k;
        l(g)=k;
        Ppw(g)=Iprms^2*Rdcp(g)*2; %Factor of 2 to take account of
other losses
    end
end

%Display warning
if Ppw(g)>(Loss_copper/2)
     disp([' Warning: Primary wire loss ',num2str(Ppw(g)),'W
exceeds Acceptable loss']);
end
```

```
%Loss in Secondary wire
Lensw(g)=MLT*ns(g)*1.5;%Length of secondary wire
dc(i)=(2.54e-2)* 0.0050.*(92).^((36.-Wawg_a(i))./39); %Diameter
of strand
Resdc1(g) = (Lensw(g)*rho)/(pi*(dc(i)^2)/4);% Resistance of 1
wire

%%Calculating the number of litz strands of secondary winding
od_litz=od_litz_a(i,:);
for j=1:length(od_litz)
    n_turns_b(j)= floor(Bbob/od_litz(j)) ;
    n_turns_h(j)=floor((hbob/2)/od_litz(j));
    n_turns(j)= n_turns_b(j)*n_turns_h(j);

    if n_turns(j)<ns
     break
    end
end

if j==1
    disp([' Litz cant fit ']);
    j=2;
end
litz_strands(g)=n_strands(j-1);

%Display warning
 if (h_pw(g)*1.25*l(g)+n_turns_h*od_litz(j))>hbob
    disp('Rejected: Wires cannot fit in allocated area');
 end

%Calculating secondary winding loss
Rdc_s(g)= Resdc1(g)/litz_strands(g);
Pdc_s(g) = Isrms^2*Rdc_s(g);% DC power loss
Fr(g)=1 +
((pi^2*w^2*(mu)^2*ns(g)^2*(litz_strands(g)).^2*(dc(i)).^6*2)/(768
*rho^2*(BWindA).^2));%Pac/Pdc
Psw(g)=Pdc_s(g)*Fr(g)*1.5; % AC power loss

P_cu(g)=Ppw(g)+Psw(g);

P_tot(g)=P_cu(g)+Pc(g);
end

%Display the results
[minP, In]=min(P_tot);
Ptot(i)=minP;
Pcore(i)=Pc(In);
Pwire(i)=P_cu(In);
disp([' ']);
disp(['Total Loss= ', num2str(Ptot(i)),'W']);
disp(['Core loss= ', num2str(Pcore(i)), 'W', ' and Copper loss=
', num2str(Pwire(i)) ,'W']);
```

```
disp(['Primary loss= ', num2str(Ppw(In)), 'W', ' and Secondary
loss= ', num2str(Psw(In)) ,'W']);
disp(['Using ',num2str(np(In)),' turns with ',num2str(l(In)), '
foils in parallel in primary and ',num2str(ns(In)),' turns with
',num2str(litz_strands(In)),' strands of litz wire for secondary
of ',num2str(Wawg_a(i)),' AWG']);

end
```

B.3 MATLAB Script for the Design of an Inductor for the Second and Third Prototype

```
%%Design of inductor

%%This script is used to design the inductor. It tries to
minimize the total
%%loss by balancing the core and copper loss. It takes input of
core data
%%and litz wire available
%-----------------------------------------------------
clc
clear all


I=1.3; %Max current
Irms=0.9; % RMS current
Bmax=300; %Maximum B field
Jmax=500*10^4; % J=A/m^2

mu=4*pi*10^-7; % Permittivity of free space
%-----------------------------------------------------
%%3F3 core parameters

Cm=[0.25*10^-3; 2*10^-5; 3.6*10^-9];
x=[1.63; 1.8; 2.4];
y=[2.45; 2.5; 2.25];
ct2= [0.79; 0.77; 0.67]*10^-4;
ct1=[1.05; 1.05; 0.81]*10^-2;
ct0=[1.26;1.28;1.14];

T=80; %Temperature
%-----------------------------------------------------------

%Cores of different size and different gap size

cores = [....
```

```
'RM08A100' ; 'RM08A160' ; 'RM08A250' ; 'RM08A315'; 'RM08A400' ;
....
'RM10A160' ; 'RM10A250' ; 'RM10A315' ; 'RM10A400'; 'RM10A630' ;
....
'RM12A060'; 'RM12A080';'RM12A100';'RM12A120';'RM12A140';....
'RM12A160';'RM12A250' ; 'RM12A315' ; 'RM12A400'; 'RM12A630';....
'RM14A250' ; 'RM14A315' ; 'RM14A400' ; 'RM14A630'; 'RM141000'];

%AL is mH for 1000 Turns
Al = [100 ; 160 ; 250 ; 315 ; 400;...
    160 ; 250 ; 315 ; 400; 630;...
    60; 80; 100; 120; 140; 160 ; 250 ; 315 ; 400; 630;...
    250; 315; 400; 630; 1000];

% A is effective core area in cm^2
A= [
       0.52 ; 0.52 ; 0.52 ; 0.52 ; 0.52;...
       0.83 ; 0.83 ; 0.83 ; 0.83;0.83 ; ...
       1.46 ; 1.46 ; 1.46 ; 1.46;1.46 ;1.46 ; 1.46 ; 1.46 ;
1.46;1.46 ; ...
       1.98; 1.98; 1.98; 1.98; 1.98 ];

%core volume in m^3
V= [ 2.440 ; 2.440 ;2.440 ;2.440 ;2.440;...
      4.310 ;4.310 ;4.310 ;4.310 ;4.310 ; ...
      8.340 ;  8.340; 8.340 ;  8.340 ;  8.340; 8.340 ;  8.340;
8.340 ;  8.340 ;  8.340;...
        13.90 ; 13.90 ; 13.90 ; 13.90 ; 13.90 ]*10^-6;

%Mean length per turn in m
MLT=[ 42; 42; 42; 42; 42;
    52 ; 52 ;52 ;52 ;52 ;
    61; 61; 61; 61; 61;61; 61; 61; 61; 61;
    71; 71; 71; 71; 71]*10^-3;

% Rth is core thermal resistance in deg. C / W
Rth= [38 ; 38 ;38 ;38 ;38 ;
    30; 30; 30; 30; 30;
    23; 23; 23; 23; 23; 23; 23; 23; 23; 23;
    19; 19; 19; 19; 19];
%Dimensions of the core
Bbob=[8.83; 8.83; 8.83; 8.83; 8.83; 10; 10; 10; 10; 10; 14.55;...
    14.55; 14.55; 14.55; 14.55;14.55; 14.55; 14.55; 14.55;1.455;
18; 18; 18; 18; 18]*10^-3;
hbob=[3.475; 3.475; 3.475; 3.475; 3.475; 4.25; 4.25;...
    4.25; 4.25; 4.25; 5.1;  5.1; 5.1; 5.1; 5.1;5.1;  5.1; 5.1;
5.1; 5.1; 6; 6; 6; 6; 6]*10^-3;
BWindA=[ 10.8; 10.8; 10.8; 10.8; 10.8; 12.1; 12.1; 12.1; 12.1;
12.1;...
    16.8; 16.8; 16.8; 16.8; 16.8;16.8; 16.8; 16.8; 16.8; 16.8;
20.8; 20.8; 20.8; 20.8; 20.8]*10^-3;
```

```
%Dimensions of the wires
n_strands=[3 4 5 6 7 8 9 10 15 20 25 30 40 50 60 75 100 125 150
175 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550
575 600 625 650 675 700 725 750 775 800 825 850 875 900 925 950
975 1000 1050 1100];
od_litz1= [7 8 9 10 11 11 12 13 16 18 20 22 26 29 31 35 40 45 50
54 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140
145 150 155 160 165 170 175 180 185 195 200 205 210 215 220 225
230 235]*10^-5*2.54;% 40 AWG
od_litz2= [6 7 7 8 9 9 10 10 13 15 16 18 23 23 25 28 32 36 40 43
48 52 56 60 64 68 72 76 80 84 88 92 96 100 104 108 112 116 120
124 128 132 136 140 144 148 152 156 160 164 168 172 176 180
184]*10^-5*2.54; %42 AWG
od_litz3=[4 5 6 6 7 7 8 8 10 11 13 14 16 18 20 22 25 28 31 34 37
40 43 46 49 52 55 58 61 64 67 70 73 76 79 82 86 90 94 98 100 102
104 106 108 112 112 112 112 112 112 112 112 112 112]*10^-5*2.54;
%44 AWG
od_litz4=[3.5 4 4.5 5 5.5 5.5 6 6.5 8 9 10 11 13 14 16 17 20 22
25 26 28 30 32 34 36 38 40 42 44 46 41.2 42.4 43.5 44.7 45.8 46.9
47.9 48.9 50 50.9 51.9 53.8 54.7 55.6 56.3 57.4 58.3 59.1 59.9
60.8 61.8 62.8 63.8 64.8 65.8]*10^-5*2.54;%46 AWG
od_litz5=[3 3 3.5 4 4.5 4.5 5 5 6.5 7 8 9 10 11 13 14 16 18 20 21
22 23 25 26 28 29.2 30.3 31.3 32.3 33.3 34.3 35.2 36.2 37.1 37.9
38.8 39.6 40.4 41.2 42 42.8 43.5 44.3 45 45.7 46.4 47.1 47.8 48.5
49.2 49.8 50.5 51.1 52.4 53.6]*10^-5*2.54; %48 AWG

Wawg_a=[40; 42; 42; 42; 46; 46];
od_litz_a= [od_litz1; od_litz2;
od_litz2;od_litz2;od_litz4;od_litz4];

X=324;% Imepdance of theinductor

%-----------------------------------------------------------------
-----
%%

for g=1:1:6

f=g*100*10^3; % Switching frequency
w=2*pi*f;

fsw=f
L=X/w;

%To decide the parameters of the 3F3 core
if f<=300000
fv=1;
elseif f<=500000;
        fv=2;
elseif f>500000;
    fv=3;
end
```

```
rho=1.68*10^-8; % Resistivity of copper

od_litz=od_litz_a(g,:);
dw(g)=(2.54e-2)* 0.0050.*(92).^((36.-Wawg_a(g))./39); %Diameter
of strand
Aw=pi*(dw(g))^2/4;%Cross-sectional area of strand

for i = 1:25,%For all cores available

N(i) = round(1000*sqrt(1000*L/Al(i))); % Number of turns of wire
B(i)= (Al(i)*N(i)*I/A(i))*1e-2; % Peak B

%Estimate loss of core
Pv(i)= (Cm(fv)*((fsw)^x(fv))*(B(i)*10^-3)^(y(fv))*(ct0(fv)-
ct1(fv)*T+ct2(fv)*T^2))*1e3; %Density of core loss
Pc(i)=Pv(i)*V(i)*1.5; % Power loss in core


%%To find the number of strands of wire that can fit

for j=1:length(od_litz)
    n_turns_b(j)= floor(Bbob(i)/(od_litz(j))) ; %Number of wires
that can fit in the breadth of core
    n_turns_h(j)=floor(hbob(i)/(od_litz(j)));
    n_turns(j)= n_turns_b(j)*n_turns_h(j); % Total number turns
that can fit in the core

    if n_turns(j)<N(i) %The number of turns tha can fit decreases
as overall diameter of wire increases
        break              % When the number of  turns is less
than the required turns break the loop
    end
end

if j==1
    disp(['Litz cant fit ']); %if litz wire cannot fit at all
    j=2; %For consistency of the code
end
 litz_strands(i)=n_strands(j-1); % Get wire which has a diameter
less than the wire which broke the loop (So it can fit)

 %%Estimate the loss in wire
 lengthw(i)= MLT(i)*N(i); %Length of wire
 Resdc1(i)=rho*lengthw(i)/Aw;%DC Resistance of one wire
 Res(i)= Resdc1(i)/litz_strands(i);% Accounting skin effects
 Fr(i)=1 +
((pi^2*w^2*(mu)^2*N(i)^2*(litz_strands(i)).^2*(dw(g)).^6)/(768*rh
o^2*(BWindA(i)).^2));%Pac/Pdc
 Pw(i)=Irms^2*Res(i)*Fr(i)*2; %Power loss in wire
```

```
 Ptot(i)= Pc(i)+Pw(i); %Total power loss
 Ptota(i)=Pc(i)+Pw(i) ; %Accepted loss

        if B(i)> Bmax,
%         disp([cores(i,:),' Rejected: Exceeds Bmax']);
           Ptota(i)=100; %Accepted loss
       end;
end

%Display the design selectred and its loss
[minP, In]=min(Ptota);
P(g)=minP;
Pcore(g)=Pc(In);
Pwire(g)=Pw(In);
flux(g)=B(In);
turns(g)=N(In);

disp(['Using ',cores(In,:),' core'] );
disp(['The total loss is ',num2str(Ptota(In)),'W. The core loss
is ',num2str(Pc(In)),'W and the copper loss is ',
num2str(Pw(In)),'W'] );
disp(['Using ', num2str(Wawg_a(g)),'AWG wire with ',
num2str(N(In)),' turns and of ',num2str(lengthw(In)),'m length.
There are ', num2str(litz_strands(In)),' strands in parallel' ]);
end
```

B.3 Code Composer v1.4 Code for TMS320F28335 Digital Signal Controller

```
// Author: Wardah Inam
//###########################################################################
//
// FILE:    Edit_2833xEpwmDeadBand.c
// TITLE:   PWM  with dead band for Fullbridge
//
//     ePWM1: Active high complementary PWMs
//     ePWM2: Active high complementary PWMs
//
//       EPWM1A is on GPIO0
//       EPWM1B is on GPIO1
//
//       EPWM2A is on GPIO2
//       EPWM2B is on GPIO3
//
//###########################################################################

#include "DSP28x_Project.h" // Device header file

// Functions
```

```
void InitEPwm1(void);
void InitEPwm2(void);


interrupt void xint1_isr(void);
interrupt void xint2_isr(void);
volatile Uint32 Xint1Count;
volatile Uint32 Xint2Count;


// Global variables

#define EPWM1_DB   0x004  //40ns deadband
#define EPWM2_DB   0x004

void main(void)
{
// Initialize System Control
// PLL, Watch Dog, enable Peripheral Clocks
   InitSysCtrl();

// Initialize GPIO pins for ePWM1 and ePWM2
   InitEPwm1Gpio();
   InitEPwm2Gpio();

// Initialize the PIE control registers to their default state.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   DINT;
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell
Interrupt
// Service Routines (ISR)
   InitPieVectTable();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
   EDIS;

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW; // This is needed to write to EALLOW protected
registers
   PieVectTable.XINT1 = &xint1_isr;
   PieVectTable.XINT2 = &xint2_isr;
   EDIS;   // This is needed to disable write to EALLOW protected
registers

   Xint1Count = 0; // Count Xint1 interrupts
```

```
   Xint2Count = 0; // Count Xint2 interrupts


 // Enable Xint1 and XINT2 in the PIE: Group 1 interrupt 4 & 5
// Enable int1 which is connected to WAKEINT:
   PieCtrlRegs.PIECTRL.bit.ENPIE = 1;          // Enable the PIE
block
   PieCtrlRegs.PIEIER1.bit.INTx4 = 1;          // Enable PIE 1
INT4
   PieCtrlRegs.PIEIER1.bit.INTx5 = 1;          // Enable PIE 1
INT5
   IER |= M_INT1;                              // Enable CPU int1
   EINT;                                       // Enable Global
Interrupts


   EALLOW;
   GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 0;         // GPIO
   GpioCtrlRegs.GPADIR.bit.GPIO4 = 0;          // input
   GpioCtrlRegs.GPAQSEL1.bit.GPIO4 = 0;        // Xint1 Synch to
SYSCLKOUT
   GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 0;         // GPIO
   GpioCtrlRegs.GPADIR.bit.GPIO7 = 0;          // input
   GpioCtrlRegs.GPAQSEL1.bit.GPIO7 = 0;        // Xint1 Synch to
SYSCLKOUT
   EDIS;


   EALLOW;
   GpioIntRegs.GPIOXINT1SEL.bit.GPIOSEL = 4;   // Xint1 is GPIO4
   GpioIntRegs.GPIOXINT2SEL.bit.GPIOSEL = 7;   // Xint2 is GPIO6
   EDIS;

 // Configure XINT1&2
   XIntruptRegs.XINT1CR.bit.POLARITY = 0;      // Falling edge
interrupt
   XIntruptRegs.XINT2CR.bit.POLARITY = 0;      // Falling edge
interrupt

   XIntruptRegs.XINT1CR.bit.ENABLE = 1;        // Enable Xint1
   XIntruptRegs.XINT2CR.bit.ENABLE = 1;        // Enable Xint2

//Call function

   InitEPwm1();
   InitEPwm2();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
   EDIS;
```

```
// IDLE loop. Loop forever
   for(;;)
   {
       asm("           NOP");
   }

}
void InitEPwm1()
{

   EPwm1Regs.TBPRD = 150;                           // Set timer
   period- TPWM=2*TBPRD*TBCLK
   EPwm1Regs.TBPHS.half.TBPHS = 0x0000;             // Phase is 0
   EPwm1Regs.TBCTR = 0x0000;                        // Clear
counter

   // Setup TBCLK
   EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
   EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;          // Disable
phase loading
   EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;         // Clock ratio
to SYSCLKOUT
   EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;            // Slow so we
can observe on the scope

   // Setup compare
   EPwm1Regs.CMPA.half.CMPA = 75;

   // Set actions
   EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
   EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;


   EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
   EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;

   // Active high complementary PWMs - Setup the dead band
   EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
   EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
   EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
   EPwm1Regs.DBRED = EPWM1_DB;
   EPwm1Regs.DBFED = EPWM1_DB;

}

void InitEPwm2()
{

   EPwm2Regs.TBPRD = 150;                           // Set timer
period
   EPwm2Regs.TBPHS.half.TBPHS = 0x0000;              // Phase is 0
```

```
   EPwm2Regs.TBCTR = 0x0000;                      // Clear
counter

   // Setup TBCLK
   EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
   EPwm2Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable
phase loading
   EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio
to SYSCLKOUT
   EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Slow so we
can observe   on the scope

   // Setup compare
   EPwm2Regs.CMPA.half.CMPA = 75;

   // Set actions
   EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;              // Set PWM2A
on Zero
   EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;

   EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;             // Set PWM2A on
Zero
   EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;

   // Active high complementary PWMs - Setup the deadband
   EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
   EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
   EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
   EPwm2Regs.DBRED = EPWM2_DB;
   EPwm2Regs.DBFED = EPWM2_DB;

}

//External button to turn off top switches and turn on bottom
switches to have zero output of the inverter

interrupt void xint1_isr(void)
{
     Xint1Count++;

     EALLOW;

     GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 0;  // All GPIO
     GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 0;  // All GPIO
     GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 0;  // All GPIO
     GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 0;  // All GPIO

     GpioCtrlRegs.GPADIR.bit.GPIO0 =1;   // All outputs
     GpioCtrlRegs.GPADIR.bit.GPIO1 =1;   // All outputs
     GpioCtrlRegs.GPADIR.bit.GPIO2 =1;   // All outputs
     GpioCtrlRegs.GPADIR.bit.GPIO3 =1;   // All outputs
```

```
    EDIS;
    GpioDataRegs.GPACLEAR.bit.GPIO0 = 1; //
    GpioDataRegs.GPASET.bit.GPIO1 = 1; //
    GpioDataRegs.GPASET.bit.GPIO2 = 1; //
    GpioDataRegs.GPACLEAR.bit.GPIO3 = 1; //
    // Acknowledge this interrupt to get more from group 1
     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;

}

//External button to output square wave of the inverter
interrupt void xint2_isr(void)
{

// Initialize System Control
// PLL, WatchDog, enable Peripheral Clocks
   InitSysCtrl();

// Initialize GPIO pins for ePWM1 and ePWM2
   InitEPwm1Gpio();
   InitEPwm2Gpio();

// Initialize the PIE control registers to their default state.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   DINT;
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell
Interrupt
// Service Routines (ISR)
   InitPieVectTable();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
   EDIS;

   // Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW; // This is needed to write to EALLOW protected
registers
   PieVectTable.XINT1 = &xint1_isr;
   PieVectTable.XINT2 = &xint2_isr;
   EDIS;   // This is needed to disable write to EALLOW protected
registers



   // Enable Xint1 and XINT2 in the PIE: Group 1 interrupt 4 & 5
// Enable int1 which is connected to WAKEINT:
```

```
   PieCtrlRegs.PIECTRL.bit.ENPIE = 1;          // Enable the PIE
block
   PieCtrlRegs.PIEIER1.bit.INTx4 = 1;          // Enable PIE
Gropu 1 INT4
   PieCtrlRegs.PIEIER1.bit.INTx5 = 1;          // Enable PIE
Gropu 1 INT5
   IER |= M_INT1;                              // Enable CPU int1
   EINT;                                       // Enable Global
Interrupts


    EALLOW;
   GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 0;         // GPIO
   GpioCtrlRegs.GPADIR.bit.GPIO4 = 0;          // input
   GpioCtrlRegs.GPAQSEL1.bit.GPIO4 = 0;        // Xint1 Synch to
SYSCLKOUT only
   GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 0;         // GPIO
   GpioCtrlRegs.GPADIR.bit.GPIO7 = 0;          // input
   GpioCtrlRegs.GPAQSEL1.bit.GPIO7 = 0;        // Xint1 Synch to
SYSCLKOUT only
   EDIS;

    EALLOW;
   GpioIntRegs.GPIOXINT1SEL.bit.GPIOSEL = 4;   // Xint1 is GPIO4
   GpioIntRegs.GPIOXINT2SEL.bit.GPIOSEL = 7;   // Xint2 is GPIO59
   EDIS;

   // Configure XINT1&2
   XIntruptRegs.XINT1CR.bit.POLARITY = 0;      // Falling edge
interrupt
   XIntruptRegs.XINT2CR.bit.POLARITY = 0;      // Falling edge
interrupt

     XIntruptRegs.XINT1CR.bit.ENABLE = 1;        // Enable Xint1
     XIntruptRegs.XINT2CR.bit.ENABLE = 1;        // Enable Xint2

//Call function
   InitEPwm1();
   InitEPwm2();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
   EDIS;


   Xint2Count++;
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;

}


//===========================================================
```

Appendix C

C.1 LTSpice netlist for the first prototype

```
XX3 Vds Vg2 0 fet
XX1 N002 N004 Vds fet
XX4 N006 V4d 0 fet
XX2 N002 V3d N006 fet
V3 Vg2 0 PULSE(0 10 {td} 10n 10n {5u-td} {1/Fs} {Fs})
V1 N004 Vds PULSE(0 10 {ts+td} 10n 10n {5u-td} {1/Fs} {Fs})
V4 V4d 0 PULSE(0 10 {td+ts} 10n 10n {5u-td} {1/Fs} {Fs})
V2 V3d N006 PULSE(0 10 {ts+ts+td} 10n 10n {5u-td} {1/Fs} {Fs})
Vin N002 0 25
L3 RTANKO N009 372µ Rser={w*372u/200}
C4 N005 RTANKO 7n
D1 N003 N001 D
D2 0 N003 D
D3 N009 N001 D
D4 0 N009 D
R3 N003 0 1Meg
R4 N009 0 1Meg
XX6 Vds N006 N007 0 transformer params: n={TF_gain}
Cds4 N006 0 430p
Cgs4 V4d 0 850p
Cgd4 N006 V4d 20p
Cds1 N002 Vds 430p
Cds3 Vds 0 430p
Cds2 N002 N006 430p
Cgd1 N002 N004 20p
Cgd2 N002 V3d 20p
Cgd3 Vds Vg2 20p
Cgs1 N004 Vds 850p
Cgs3 Vg2 0 850p
Cgs2 V3d N006 850p
Vo N001 0 400
C1 N001 N003 24p
C6 N003 0 24p
C7 N001 N009 24p
C8 N009 0 24p
L2 RCNM N003 506µ Rser={w*506u/200}
C3 RCNM N005 5n
Cr1 N008 N007 5n Rpar=100Meg
Lr1 N008 RTANKO 506µ Rser={w*506u/200}
* block symbol definitions
.subckt fet D G S
```

```
S1 S D G S MOSFET
D1 S D D
.model MOSFET SW(Ron=9.1m Roff=10Meg Vt=1.3 Vh=-1)
.model D D(Vfwd=0.7 Ron=1m )
.ends fet
.subckt transformer v1p v1n v2p v2n
E1 N001 v2n v1p v1n {n}
F1 v1p v1n Vsense {n}
Vsense N001 v2p 0
.param n 1
.ends transformer
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.param TF_gain 10
.param Fs 100000
.tran 0 2m 1m 10n
.param td 50n
.param deg 180
.param ts {deg*pi/(180*2*pi*{Fs})}
.param w {2*pi*Fs}
.model D1 D(Vfwd=1.7 Ron=1m)
.model D2 D(Vfwd=1.7 Ron=1m)
.model D3 D(Vfwd=1.7 Ron=1m)
.model D4 D(Vfwd=1.7 Ron=1m)
.backanno
.end
```

The schematic is shown in Figure C. 1. The MOSFET model used is shown in Figure C. 2 and the ideal transformer model is shown in Figure C. 3

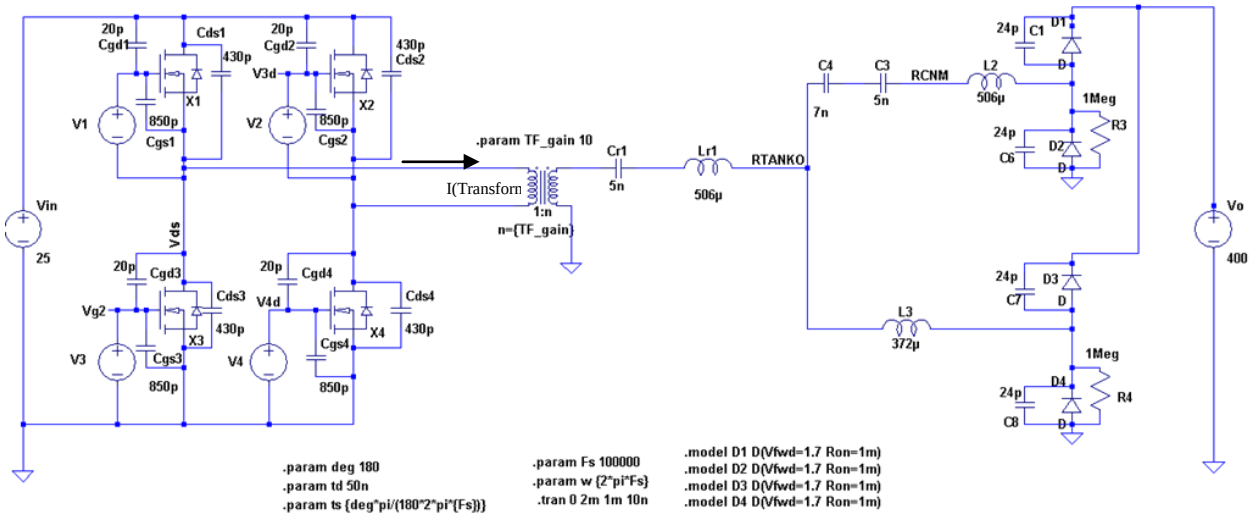


Figure C. 3: LTSPICE simulation for first prototype

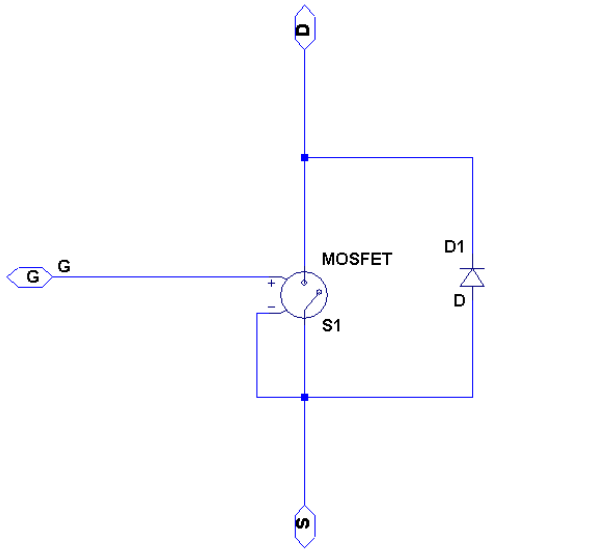


Figure C. 4: MOSFET model used in the simulation

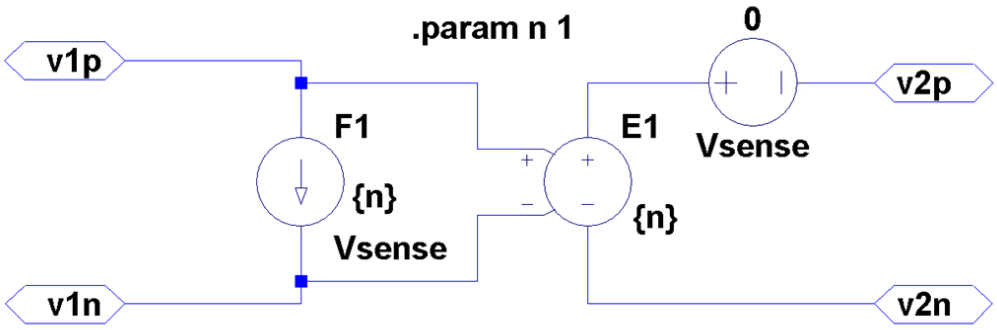


Figure C. 3: Transformer model used in the simulation

C.2 LTSpice Netlist for the Final Prototype

```
*
C:\Users\wardah\Dropbox\Research\LTspice\ICR1\Current\6_4_500k_pa
rallel.asc
XX1 Vc+ Vc- N002 0 transformer params: n={TF_gain}
L1 N009 N008 {X/w} Rser={X/200}
C1 N004 N003 {1/(X*w)}
Cr1 N005 N004 {1/(X2*w)} Rpar=100Meg
Lr1 N002 N003 {X2/(w)} Rser={X2/200}
```

```
D1 N005 N001 D
D2 0 N005 D
D3 N008 N001 D
D4 0 N008 D
R1 N005 0 1Meg
R2 N008 0 1Meg
Le1 Vds N007 {0.946u} Rser={Xe/200}
C6 Vc+ Vc- {1/(Xe*w)}
Cr2 N009 N002 {1u} Rpar=100Meg
Vout N001 0 400
XX10 Vds Vg2 0 fet
XX11 Vt3 v1 Vds fet
XX12 Vc- V4d 0 fet
XX13 Vt3 V3d Vc- fet
V1 Vg2 0 PULSE(0 5 {td} 5n 5n {1/(2*Fs)-td} {1/Fs} {Fs})
V6 v1 Vds PULSE(0 5 {ts+td} 5n 5n {1/(2*Fs)-td} {1/Fs} {Fs})
V7 V4d 0 PULSE(0 5 {td+ts} 5n 5n {1/{2*Fs}-td} {1/Fs} {Fs})
V8 V3d Vc- PULSE(0 5 {ts+ts+td} 5n 5n {1/(2*Fs)-td} {1/Fs} {Fs})
Vin2 Vt3 0 25
Cds1 Vc- 0 430p
Cgs1 V4d 0 850p
Cgd1 Vc- V4d 20p
Cds2 Vt3 Vds 430p
Cds3 Vds 0 430p
Cds4 Vt3 Vc- 430p
Cgd2 Vt3 v1 20p
Cgd3 Vt3 V3d 20p
Cgd4 Vds Vg2 20p
Cgs2 v1 Vds 850p
Cgs3 Vg2 0 850p
Cgs4 V3d Vc- 850p
XX14 Vt3 v1 Vds fet
Cds5 Vt3 Vds 430p
Cgd5 Vt3 v1 20p
Cgs5 v1 Vds 850p
XX15 Vds Vg2 0 fet
Cds6 Vds 0 430p
Cgs6 Vg2 0 850p
XX16 Vt3 V3d Vc- fet
Cds7 Vt3 Vc- 430p
Cgd6 Vt3 V3d 20p
Cgs7 V3d Vc- 850p
XX17 Vc- V4d 0 fet
Cds8 Vc- 0 430p
Cgs8 V4d 0 850p
Cgd7 Vc- V4d 20p
Cgd8 Vds Vg2 20p
C2 N005 0 24p
C3 N001 N005 24p
C4 N001 N008 24p
C5 N008 0 24p
C7 Vc+ N007 10µ
```

```
* block symbol definitions
.subckt transformer v1p v1n v2p v2n
E1 N001 v2n v1p v1n {n}
F1 v1p v1n Vsense {n}
Vsense N001 v2p 0
.param n 1
.ends transformer

.subckt fet D G S
S1 S D G S MOSFET
D1 S D D
.model MOSFET SW(Ron=9.1m Roff=10Meg Vt=1.3 Vh=-1)
.model D D(Vfwd=0.7 Ron=1m )
.ends fet

.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.param TF_gain 5
.param Fs 500000
.tran 0 4m 3.8m 10n
.options plotwinsize=0
.param td 20n
.param deg 180
.param ts {deg*pi/(180*2*pi*{Fs})}
.param w {2*pi*Fs}
.param X 201
.param X2 318
.param Xe 4.54
.model D1 D(Vfwd=1.7 Ron=1m)
.model D2 D(Vfwd=1.7 Ron=1m)
.model D3 D(Vfwd=1.7 Ron=1m)
.model D4 D(Vfwd=1.7 Ron=1m)
.backanno
.end
```

Appendix D

Board layouts for the first and second prototype are given. For the third prototype, the board of second prototype was altered.

The images of the PCB schematic and board layout for the converter prototypes are shown. The PCB layout was made using CadSoft's EAGLE PCB design software.

D.1 Schematic and Board Layout for the First Prototype

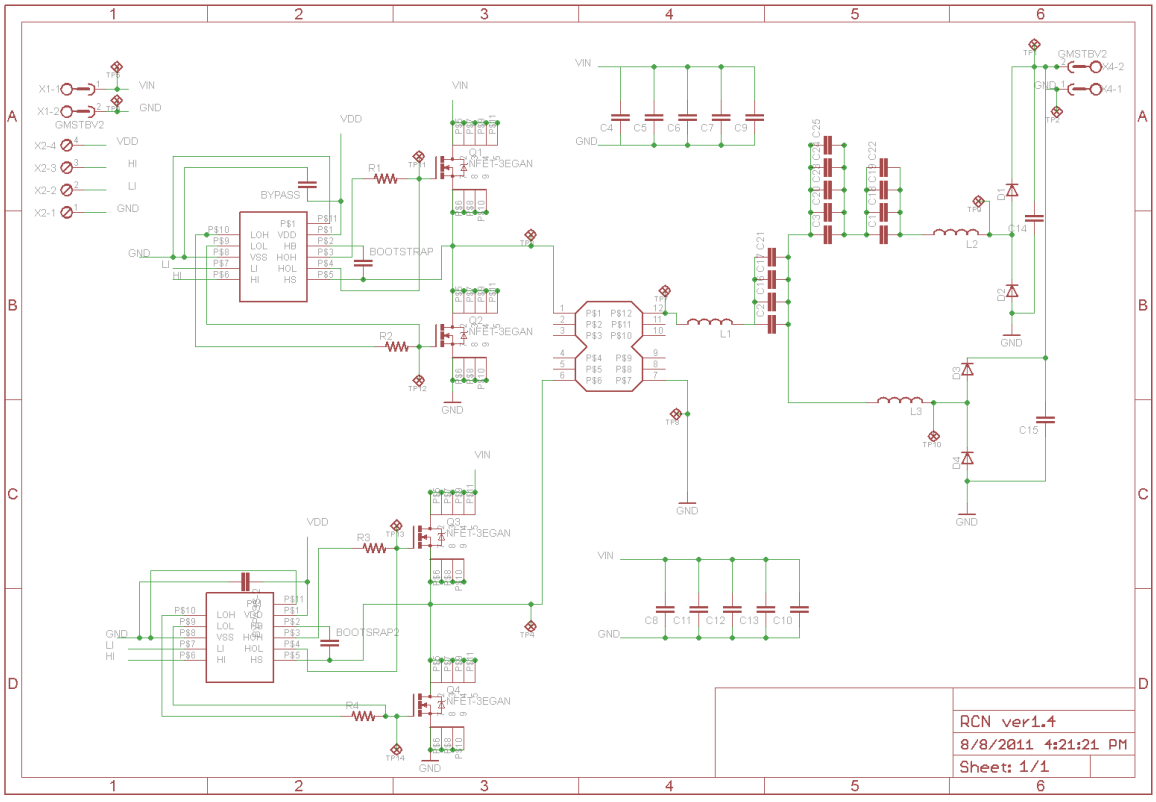


Figure D. 1: Schematic of the first prototype

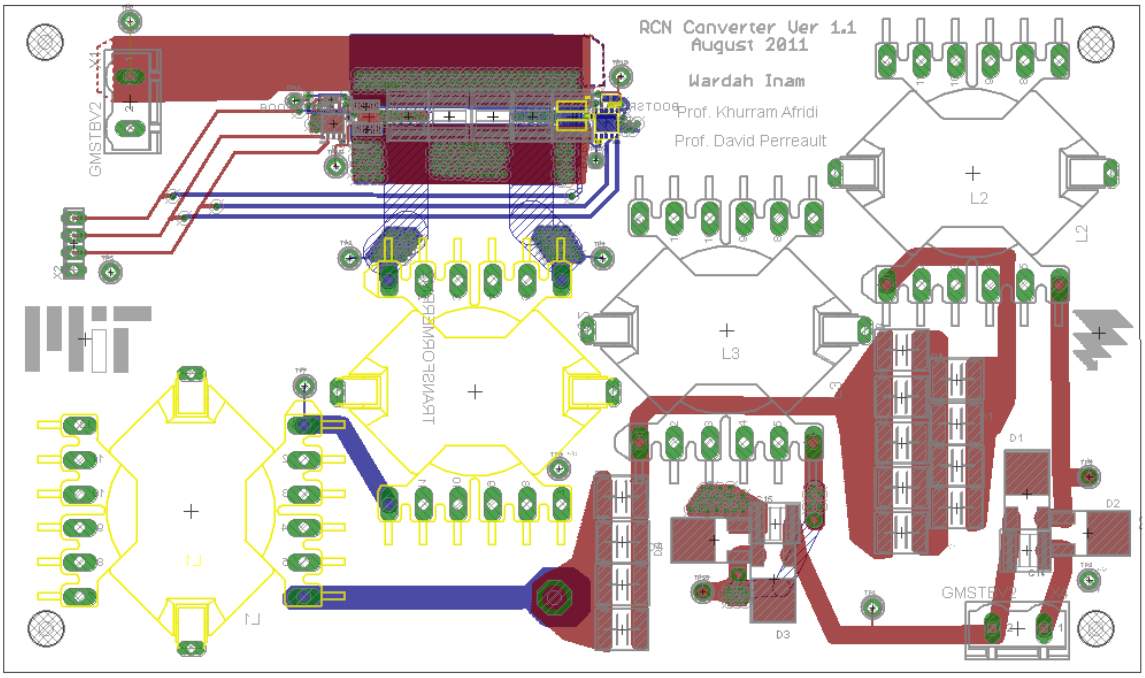


Figure D. 2: Four layer board layout. (The ground layer is not shown for clarity)

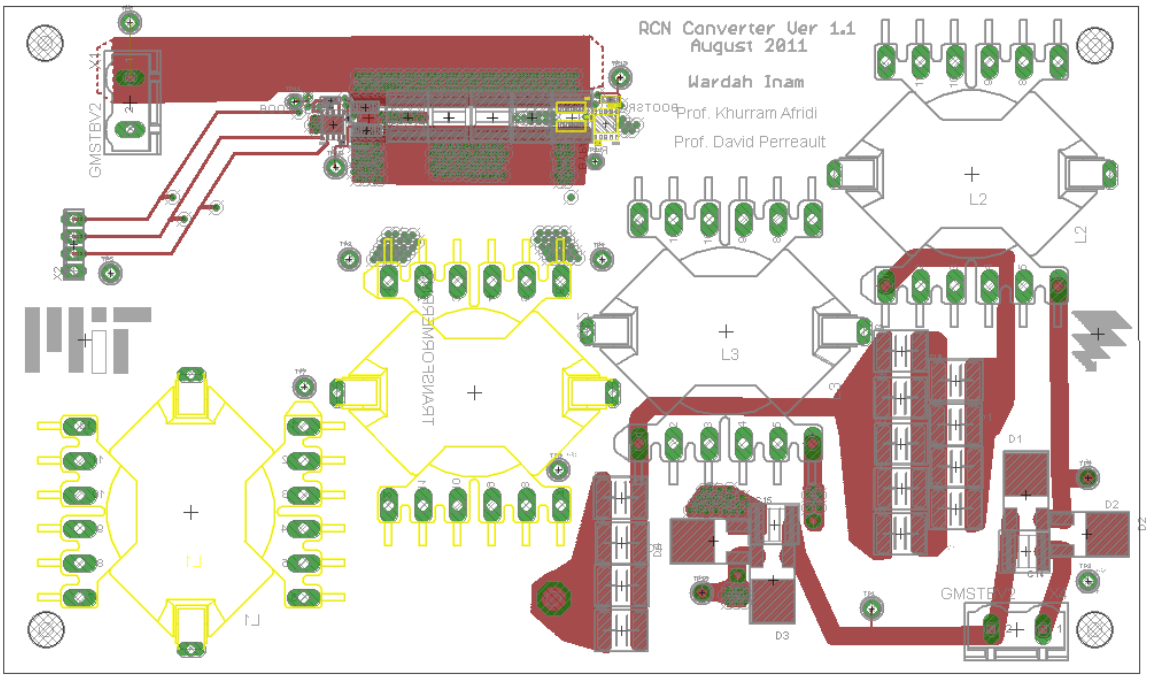


Figure D. 3: Top layer

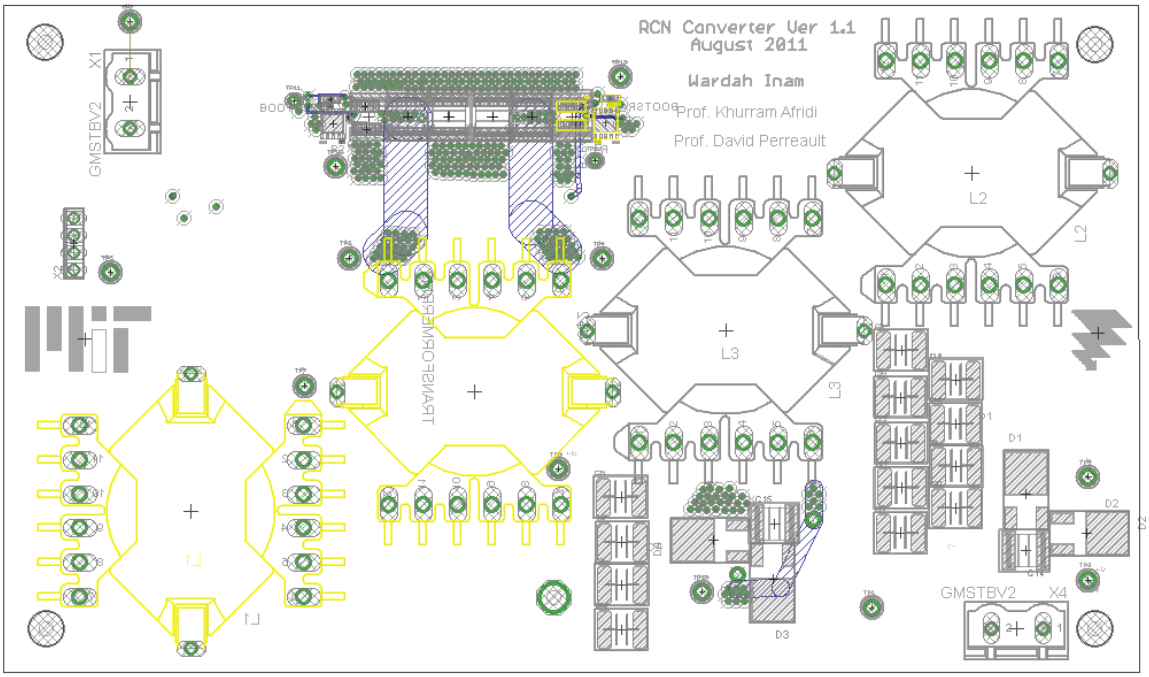


Figure D. 4: Second layer

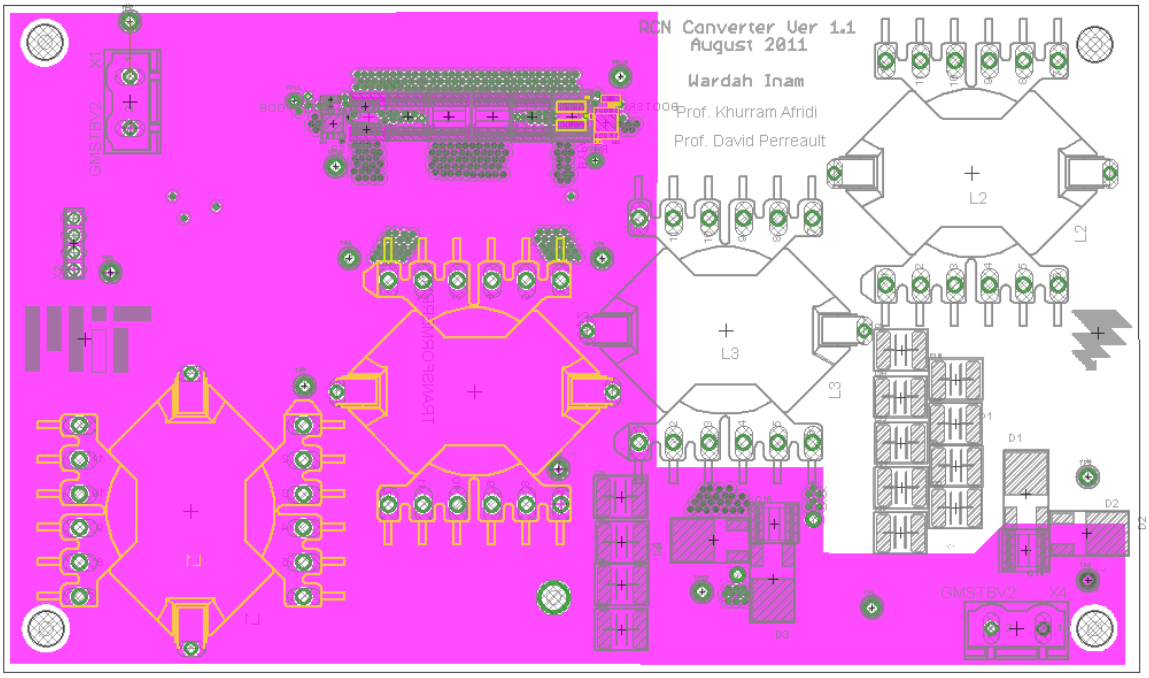


Figure D. 5: Third layer (Ground)

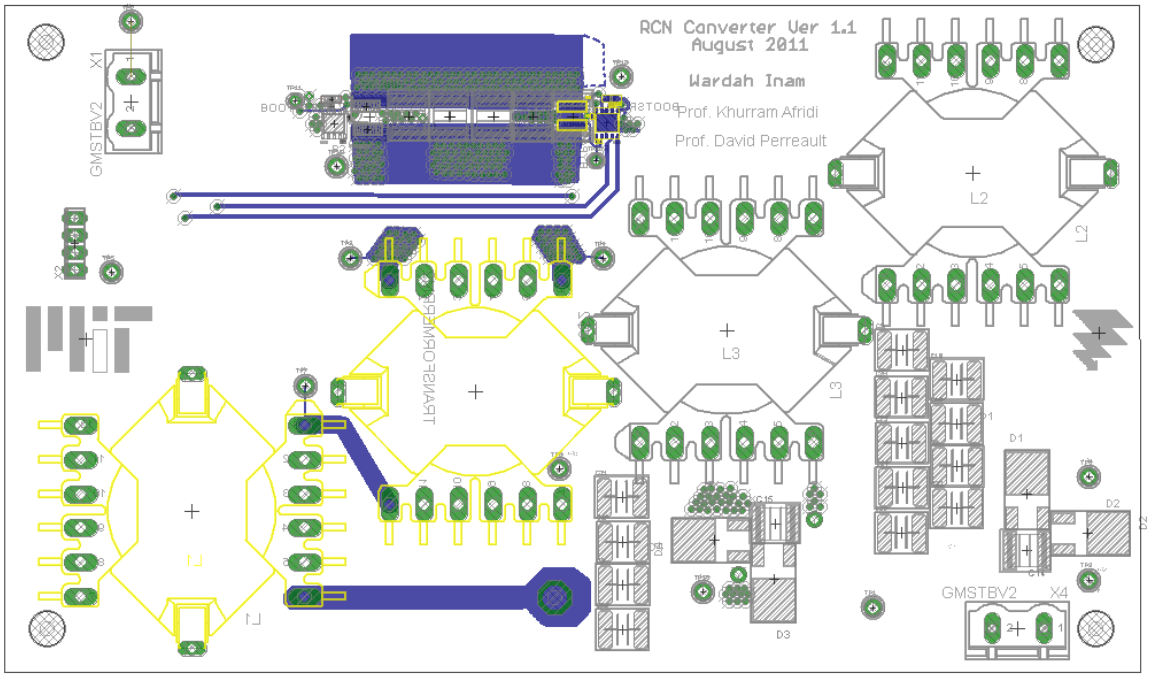


Figure D. 6: Bottom layer

D.2 Schematic and Board Layout for the Second Prototype

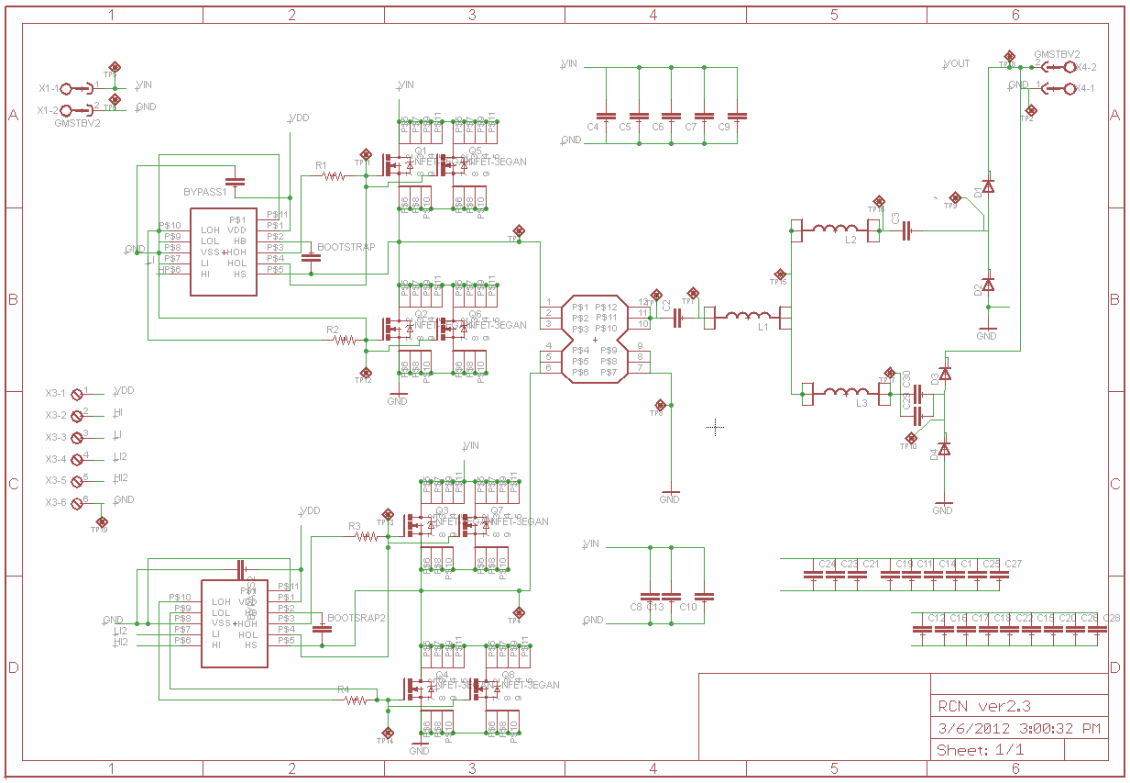


Figure D. 7: Schematic of the second prototype

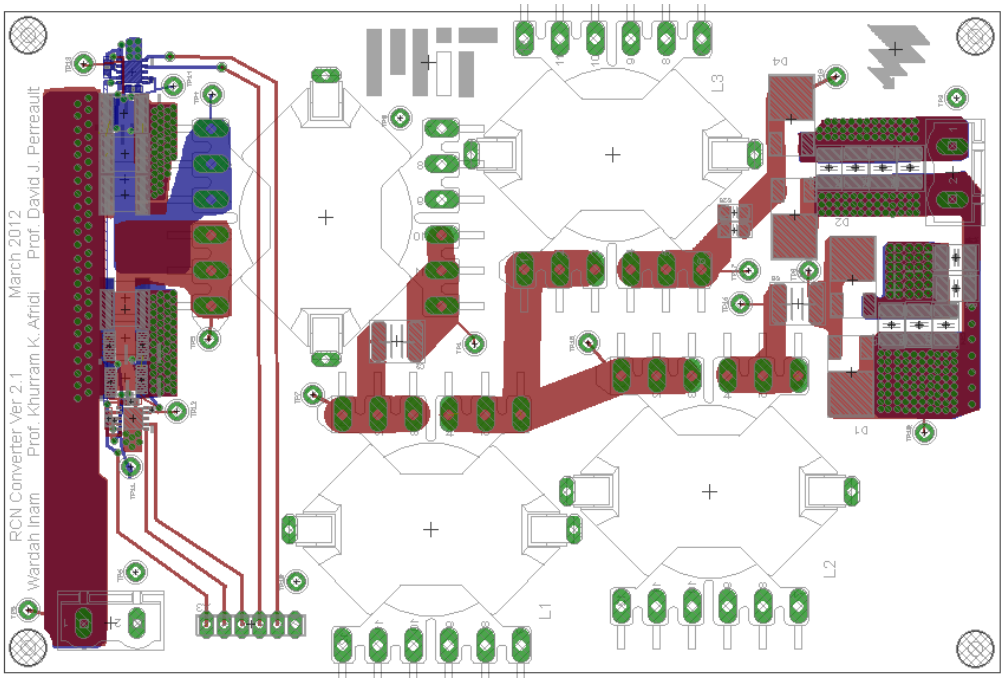


Figure D. 8: Four layer board layout for second and third prototype (Ground layer not shown for clarity)

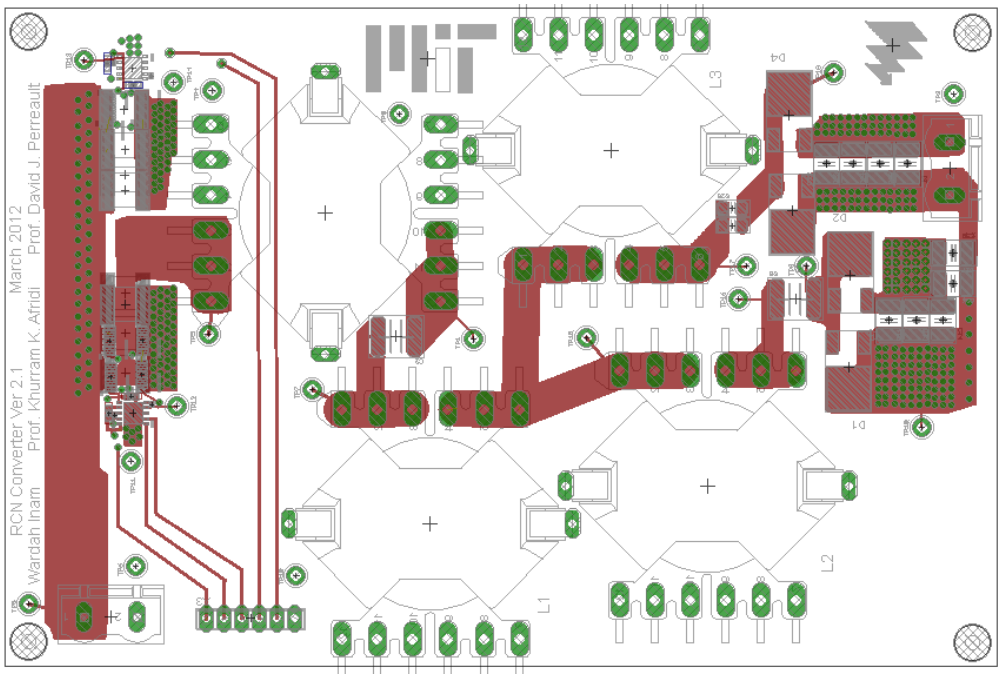


Figure D. 9: Top layer

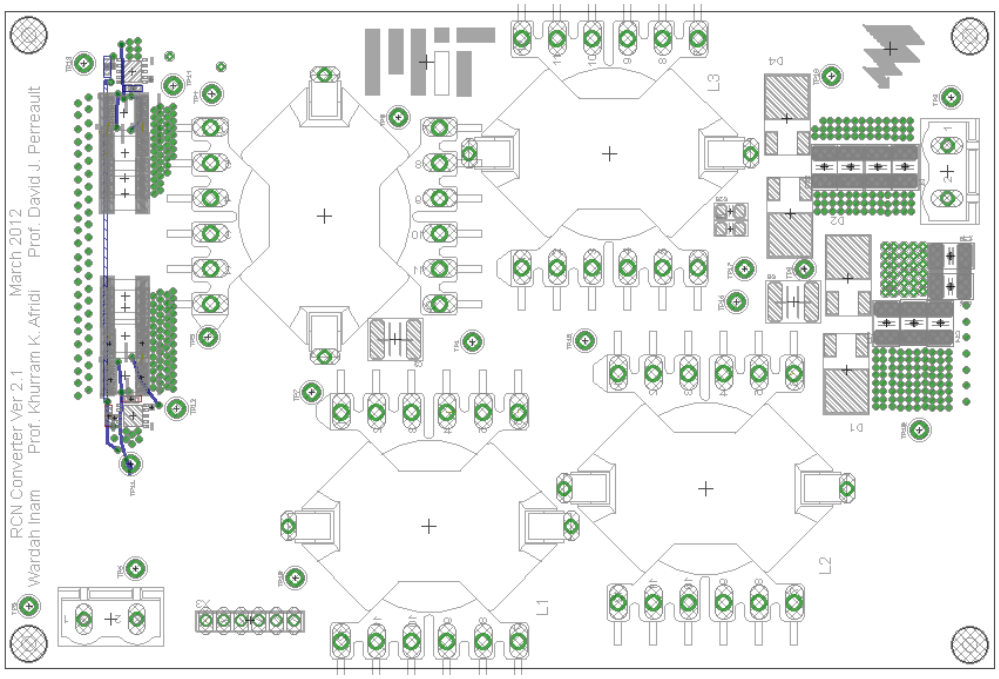


Figure D. 10: Second layer

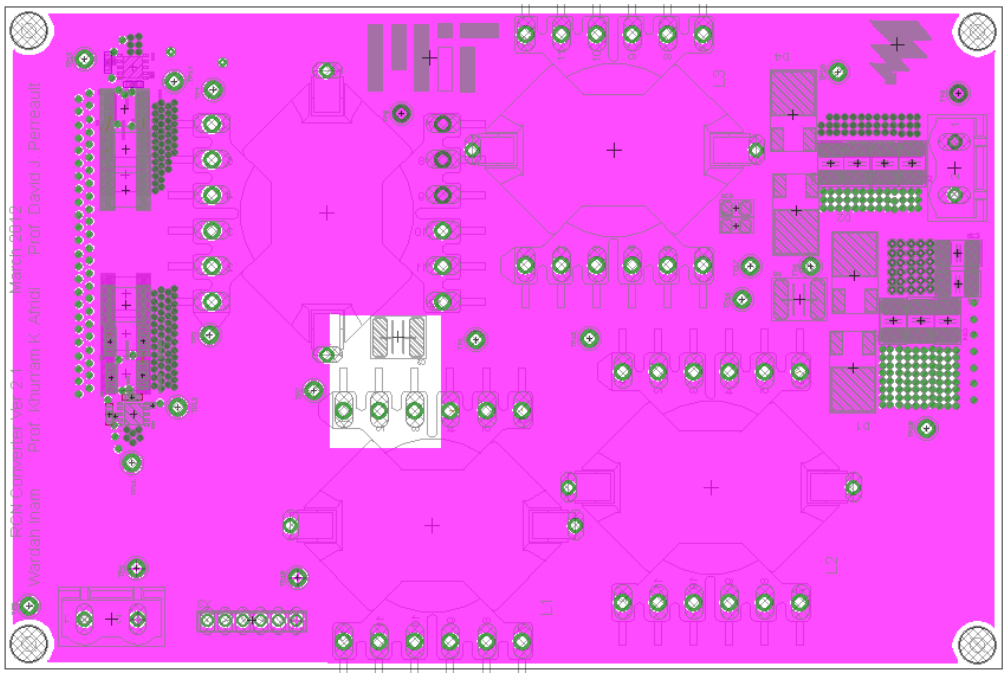


Figure D. 11: Third layer (Ground layer)

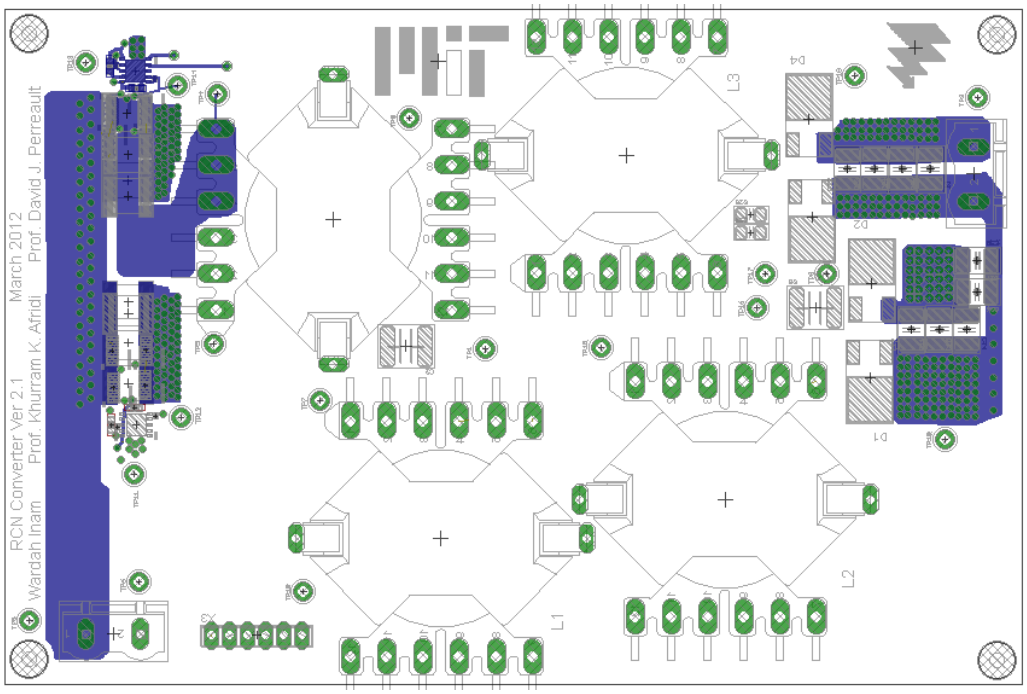


Figure D. 12: Bottom layer

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