Wafer Bonding of Processed Si CMOS VLSI and GaAs for Mixed Technology Integration

by

Edward Robert Barkley

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Author .....
Department of Electrical Engineering and Computer Science
September 27, 2001

Certified by .....
Clifton G. Fonstad, Jr.
Professor of Electrical Engineering
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

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Abstract

The successful bonding of bare thinned Si SOI wafers to bare GaAs wafers in previous research has proven to be an important first step in achieving integration of Si electronics with GaAs optoelectronic devices. The thinning of the SOI wafer has been shown to be a successful solution to the problem of the thermal expansion coefficient mismatch between Si and GaAs, allowing for the potential dense integration of mixed optoelectronic and electronic technologies. This research takes the next logical step toward that end by bonding Si wafers with simulated full back-end processing to GaAs wafers. The back-end processing simulation consists of depositing 1000Å of Al, patterning the Al into 5μm serpentine lines on a 5μm pitch, covering the Al with a PECVD oxide, and performing CMP planarization of the oxide. The 1000Å variations caused by the Al layer are consistent with surface profiles taken from fully processed SOI wafers obtained from IBM. The result is that these "simulation" wafers model the difficulties presented with bonding fully processed wafers; namely the temperature constraints caused by the existence of buried Al metal and the topography created by the patterned metal. The entire process, including the bonding and post-bond anneal, is carried out at temperatures below 450°C, making it compatible with a fully processed SOI CMOS wafer. The use of dielectric CMP has become a common back-end processing step. The wafer bonding in this work relies on CMP technology to planarize PECVD oxide deposited on the bonding surface of both wafers. The combination of CMP with post CMP cleaning methods results in a PECVD oxide surface with an order of magnitude reduction in the r.m.s. roughness, rendering the surface smooth enough to facilitate wafer bonding. The future goal of this project is to bond fully processed Si CMOS wafers to GaAs wafers containing optoelectronic devices and to test the feasibility of creating interconnects through the bond interface.

Thesis Supervisor: Clifton G. Fonstad, Jr.
Title: Professor of Electrical Engineering

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I would like to use this section of the thesis to give credit to those whose support, guidance, help, encouragement, and prayers have been greatly appreciated during the last two years and without whom, none of this would have been possible.

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Chapter 1

Introduction

1.1 The Role of Integration

The invention of the transistor in 1947 is often considered the beginning of the age of information. We live in a world dominated and controlled by electronic components containing millions of transistors all working together to perform some function and our world would be vastly different without that one device. However, we would be remiss if we failed to consider the importance of not only the device, but also the technology that allows for millions of these devices to be combined together into one system. This is the highly technical invention of integration; simple in concept, but extremely advanced in implementation. The integrated circuit was invented in 1958 by Jack Kilby and while the transistor has been improved upon, it is really the improvements since 1958 in integration technology that has allowed for the production of components that perform more complicated functions, in less time, in a smaller space, and at a smaller cost consequently outperforming and replacing a previous generation of components. Integration is the key, and without it, a single transistor has very limited applications.

1.2 Optoelectronic Integration

OptoElectronic Integrated Circuits or OEICs, circuits with devices capable of converting between electrical and optical signals, are presently the focus of much research. Like with electronics, research is being focused not just on the fundamental optical devices themselves (lasers, modulators, VCSELs, LEDs, detectors, waveguides, etc.), but also on the integration

of these devices not only with each other but also with electronic circuits and devices. The ultimate goal of such research is the development of what might be called an Opto-Electronic Very Large Scale Integration Integrated Circuit or OE-VLSI IC. An OE-VLSI IC would be very useful in communication systems, biomedical or general imaging, and displays. Another interesting application, which has served as a recent motivation for OE integration research is to optically distribute the clock (or any other signals which must be sent over relatively long distances) in conventional IC's by adding the necessary OE components to the original IC design resulting in an OE-VLSI IC with capabilites for optical signal distribution.

1.3 Mixed Technology Integration

Research efforts aimed at developing a feasible OE-VLSI IC inevitably fall into the much more general area of research known as mixed technology integration which involves the integration of various technologies which are based on different material systems. This is a result of the lack of a material that is simultaneously optimimum for fabricating optical, optoelectronic, and electronic devices and components. For low power, high density processing and memory, silicon is well established as the material of choice. However, in terms of performing optoelectronic functions, silicon is only marginally useful as a detector and is incapable of stimulated emission of light. Instead, a direct bandgap material must be integrated into the system in order to fabricate a laser. The most popular materials for performing this function are GaAs and InP. Both GaAs and InP have material properties that differ from silicon making the integration a difficult task. Integration techniques aimed at combining these dissimilar materials can be divided into three categories; heteroepitaxy on silicon, hybrid integration, and quasi-hybrid integration.

1.3.1 Heteroepitaxy on Si

The most direct approach to integrating two materials in semiconductor processing is to epitaxially grow one of the materials on the other material, which is known as heteroepitaxy. Heteroepitaxy of GaAs on Si has been extensively studied. The majority of the literature on this topic is found mostly in the late 1980s [2]. Direct growth of GaAs on Si was mostly unsuccessful because of the expected heteroepitaxial problems created by a 4% lattice mismatch, large thermal expansion mismatch, polar/non-polar interface problems,

antiphase disorder, and cross-doping. Heteroepitaxy using intermediate layers, the development of surface cleaning techniques, and growth on off direct <100> orientation resulted in epitaxial films with higher quality, but devices fabricated in heteroepitxial GaAs on Si were still inferior to devices resulting from conventional GaAs approaches [3]. Research is still being conducted in this area [26] with improved results, but high efficiency continuous wave (CW) laser operation is still elusive and lasers fabricated from GaAs on Si suffer from rapid burnout.

It is obvious that the differences in the material properties of GaAs and Si make the specific heteroepitaxy of GaAs on Si a difficult task. Perhaps more importantly, heteroepitaxy is a material specific solution and what may work for GaAs on Si will most likely not work for heteroepitaxy of other materials. Consequently its primary disadvantage is that it is not a generic solution for dissimilar materials integration. Its decisive advantage is that if it is successful, it is a solution that can be easily scaled to account for variations in conventional GaAs and Si processing.

1.3.2 Hybrid Integration

The most commonly accepted and commercially supported method for integrating optoelectronic III-V materials with Si electronics is hybrid integration. The advantage of hybrid integration is that it simultaneously allows for the electronic and optoelectronic components to be fabricated on the optimum substrate. For instance, the emitters, modulators, or detectors are fabricated using the GaAs or InP material system and the silicon electronics is fabricated using conventional silicon processing techniques. The integration may be at the board level, in which case the components are packaged separately, or it may be at the chip level, in which case the separate OE and electronic chips are part of a multichip package. This technique is both speed and density limited by the fact that the OE and electronic devices are contained on separate chips and are connected off chip through wire bonds or printed circuit board traces.

Perhaps deserving of a separate classification is the hybrid integration technique known as flip-chip bonding. The advantages of flip-chip bonding are that the electrical connections between the two chips are very short ($\sim$ 15–50μm) and the area rather than just the perimeter of the chip is used for interconnections allowing for a greater I/O (input/output) count. The flip-chip technique [31] involves bonding rows or 2-D arrays of OE devices to

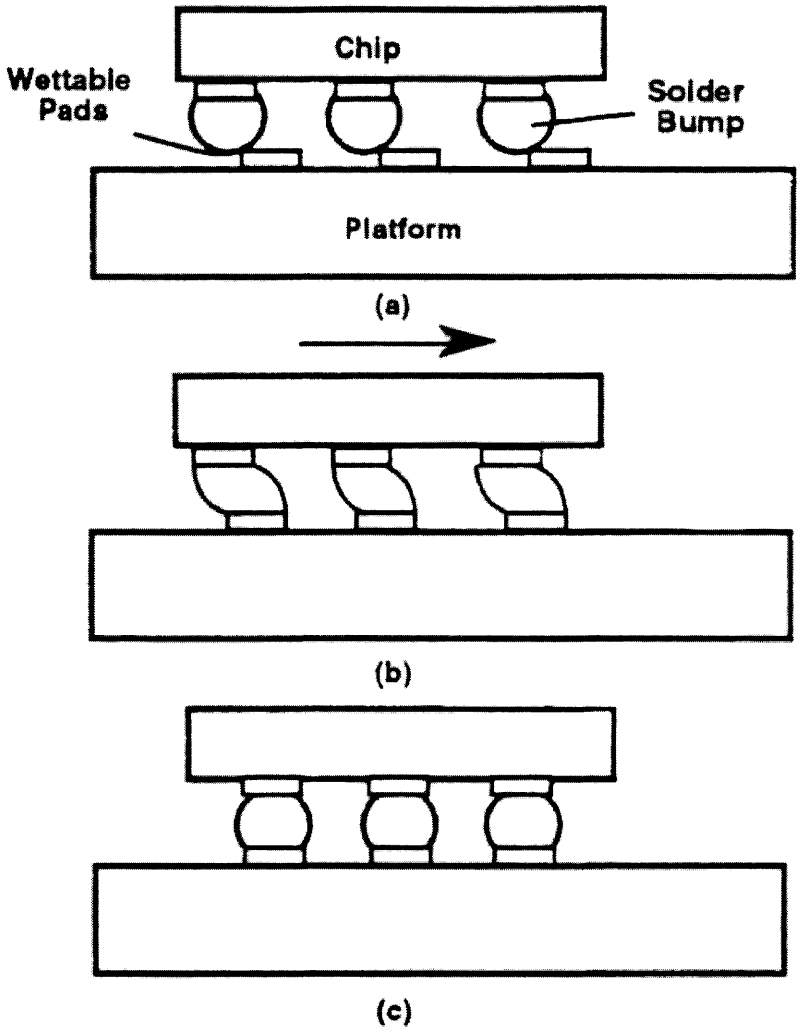


Figure 1-1: Solder Ball Bonding Process [31].

exposed upper metal layer bonding pads of, for instance, a Si CMOS IC. First, OE devices are fabricated on a transparent or sacrificial substrate with patterned solder bumps on each bonding pad. This substrate is then flipped over and positioned so that the solder bumps are in approximate alignment with a solder-wettable metallization pattern on the pads of the Si chip. Alloys of lead and tin are frequently used as solder bumps with wettable metals such as Cu on the pads of the Si chip. Thermal cycles are used to reflow the the solder bumps, allowing the surface tension of the solder bumps to pull the chip into position [32] and complete all of the connections (Figure 1-1). An epoxy may be flowed around the solder balls under the OE chip for mechanical support. The OE substrate is then etched away or

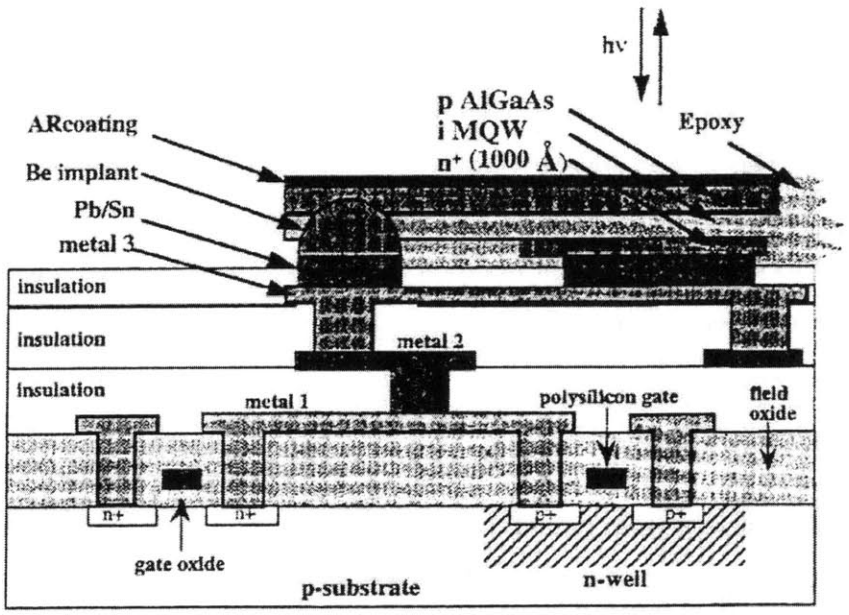


Figure 1-2: MQW Modulator flip-chip bonded to a Si CMOS IC [13].

as stated earlier, may be left if it is transparent to the wavelengths of interest. Figure 1-2 shows a MQW modulator bonded onto a Si CMOS IC.

A parameter worth mentioning for the sake of later comparisons is the pitch of the OE devices and the pad dimensions. Typical pad dimensions are 100μm x 100μm and a typical pad-to-pad pitch is 250μm.

1.3.3 Quasi-Hybrid Integration

The closest packing of devices is achieved with monolithic integration, and the most profound example is present day Si CMOS memory modules in which separate transistors may be packed together a few hundred nanometers apart. Monolithic integration refers to the fabrication of all of the separate devices on the same material or substrate (Si in the case of the memory modules). As implied earlier, an integration scheme such as monolithic integration does not allow for the separate optimization of both electronic and OE device fabrication. At a level of device packing density that fits somewhere between monolithic and hybrid integration is what may be called quasi-hybrid integration. It is hybrid in that the separate OE and electronic devices are grown or implanted in separate materials. However

with quasi-hybrid integration, the OE devices become a more intimate part of the Si chip or substrate as compared with even flip-chip bonding. For instance, the OE devices may be separately incorporated into the dielectric stack of the Si chip, or the wafer capable of containing OE (i.e. GaAs) devices may be bonded to the Si chip directly without the use of solder balls. This second approach involving wafer bonding of GaAs to Silicon is the focus of the work presented in this thesis. This approach has all the advantages of flip-chip bonding as far as separate device optimization is concerned, with the additional advantage of a higher packing density and scalability.

1.4 Research Context

In order to fully understand the goal of this research, it is necessary to mention the previous research conducted as a part of this OE-VLSI project. It is also necessary to explain where this work is leading since it only represents a part of the total OE-VLSI process and is in many ways, an exercise with the purpose of learning more about the problems that may be encountered in such a process.

1.4.1 Building from the SonG Foundation

This work is the second part in the project aimed at developing a Silicon-on-GaAs (SonG) OE-VLSI IC via wafer bonding. The first part of the project was to demonstrate the wafer bonding of bare GaAs to bare Silicon SOI (Silicon On Insulator) wafers [15]. This work [14] was successfull and as will be explained later, many of the techniques learned then were applied to this part of the project. This current work takes the next logical step towards developing an OE-VLSI IC by attempting to bond fully processed silicon CMOS SOI wafers to bare GaAs wafers. The GaAs wafers were obtained (received as a gift from Vitesse Semiconductor Corporation) with a deposited and planarized PECVD oxide. Fully processed wafers were used to replicate the actual conditions that would exist in fabricating an OE-VLSI IC from a silicon CMOS wafer. The wafers were obtained from IBM Fishkill Research Labs. They are processed on SIMOX (Separation by IMplantation of OXygen) wafers and contain test circuitry and devices. A cross section of an IBM SOI wafer is shown in Figure 1-4. These wafers were used simply because they are "real world" wafers and any problems that may be encountered in an actual OE-VLSI process were encountered using

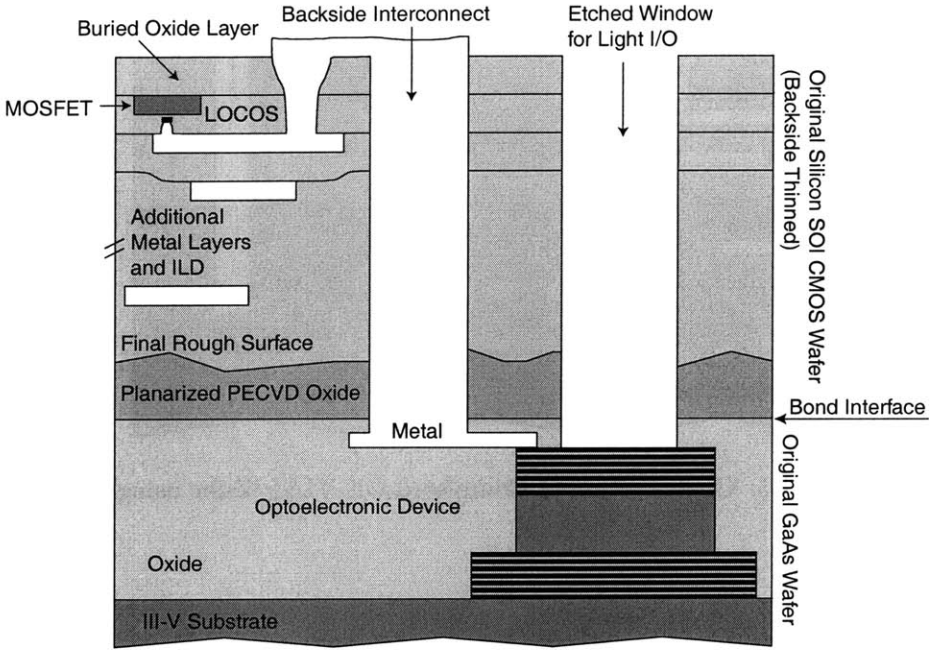


Figure 1-3: Cross-Section of Completed OE-VLSI Wafer.

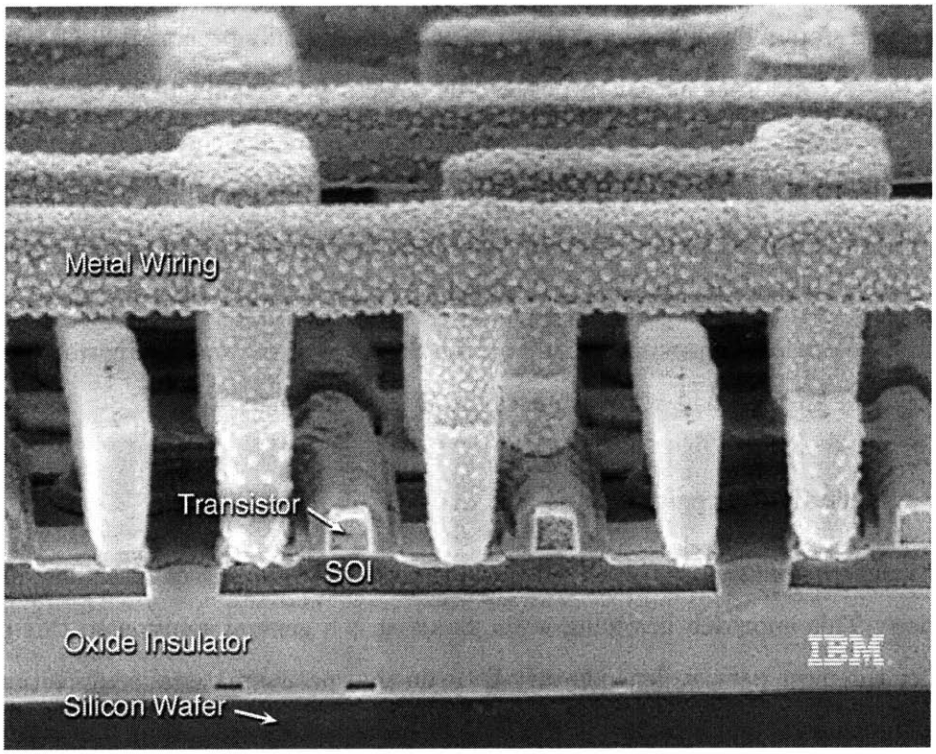


Figure 1-4: Cross-Section of IBM SOI wafer.

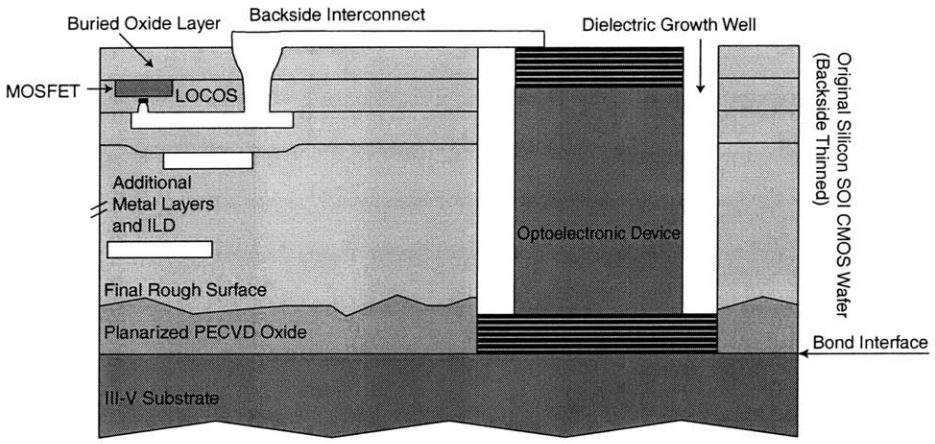


Figure 1-5: Cross-Section of Completed OE-VLSI Wafer using EoE.

these wafers.

1.4.2 The Completed OE-VLSI IC

The final step in this project, which will be elaborated upon in the Future Work section, takes the final step in developing an OE-VLSI IC: bonding fully processed Si CMOS wafers to GaAs wafers containing actual optoelectronic devices and making all necessary electrical connections between the devices on the two wafers. Figure 1-3 shows an idealized cross-section of the resulting OE-VLSI IC. An alternate approach involves the use of the Epitaxy on Electronics (EoE) technique. In this case, growth wells would be etched through the silicon wafer, exposing the GaAs wafer surface. Devices would then be grown in these wells and all electrical connections made on the backside of the wafer. Figure 1-5 shows a cross-section of an OE-VLSI IC which uses the EoE technique.

1.4.3 Alternative Applications

As mentioned previously, this work falls into the general category of dissimilar materials integration. This approach involving wafer bonding is a general solution to this problem in that for the most part, it depends very little on the specific material composition of the wafers. The actual bond interface is PECVD oxide deposited on both of the wafers to be bonded. As long as PECVD oxide can be deposited on the specific material, this work could be extended to that material system. In addition, the problem of adding devices or

circuitry directly on top of existing circuitry is the exact problem addressed in 3D integration research. Consequently, this work, although specific in the materials being used (Si and GaAs) and the application of focus (OE integration) has the feel of a more general research effort in these other areas.

1.5 Thesis Organization

As previously stated, this work is the second part of the wafer bonding OE-VLSI project. The remaining chapters of this thesis will detail each of the steps in this process and the reasoning or theory behind each step. Before actually getting into the processing steps, Chapter 2 explains some of the general wafer bonding theory which is really what guided the formulation of the entire integration process. Chapters 3–5 deal with the actual processing steps themselves (low temperature oxide deposition and planarization, surface preparation and low temperature wafer bonding and anneal, and backside wafer thinning and high temperature anneal). In each chapter, some general theory or reasoning is given for the respective step followed by the processing details, the results, and an interpretation of the results. Chapter 6 deals with an alternative to conventional direct wafer bonding in which an intermediate Spin-On-Glass (SOG) layer was used like an adhesive to help bond the wafers. Chapter 7 concludes the thesis and discusses potential future work on this project.

1.6 Lab Facilities

The majority of the work for this thesis was carried out in the Microsystems Technology Laboratories (MTL). The work was split between both the Integrated Circuits Laboratory (ICL) and the Technology Research Laboratory (TRL), both of which are subsections of MTL. The AFM characterization was performed using the Shared Experimental Facilities (SEF) which is part of the Center for Materials Science and Engineering (CMSE). Finally, some use was made of Professor Fonstad's group laboratories.

Chapter 2

Wafer Bonding

Wafer bonding is a technique that is currently employed in the fabrication of MicroElectroMechanical Systems (MEMS) and in the production of Silicon on Insulator (SOI) wafers. The term "wafer bonding" refers to the process of bringing two wafers together into intimate contact to form an initial room temperature bond and any subsequent processing designed to strengthen the bond. Older wafer bonding techniques required the application of an externally applied electric field or hydrostatic pressure in order to achieve the initial intimate contact. However in 1985-86, Lasky et al. and Shimbo et al. reported successful wafer bonding without externally applied forces. It was found that two flat, smooth, hydrophilic surfaces when brought together will spontaneously bond at room temperature [17]. The forces involved in the initial room temperature bond are mainly short-range intermolecular and interatomic forces such as van der Waals, capillary, and electrostatic forces [19].

2.1 The Conventional Wafer Bonding Process

While wafer bonding has many applications, each with its own set of specific steps, there are a few basic steps that are general to most applications. The following [18] gives an account of the general process. First, the two wafer bonding surfaces must be made flat and smooth. Standard commercially available prime-grade polished wafers have a mean surface microroughness of a few angstroms. The microroughness of the surfaces may be as high as 5Å. If the microroughness is any higher, some elastic deformation of the wafers must occur in order for the wafers to bond. The application of pressure could be used to facilitate this deformation. If the wafers are not sufficiently smooth, some combination

of depositing an oxide or SOG followed by planarizing via CMP must be included in the process. Once the wafers are sufficiently smooth, the surface chemistry must be altered to achieve the correct type of surface termination. This step is further explained later. The wafers are then contacted. The contacting usually occurs at room temperature. The wafers may be simply contacted by hand or with a bonding machine. The wafer bonding occurs in the form of a contact wave which starts at the point where the two wafers first touch and spreads out to the edges. This wave can usually be seen as it travels at speeds on the order of a few cm/s. The bonding wave pulls the wafers together and pushes air out from between the two wafers. The advantage of using a bonding machine is that it is best to start the contacting in the middle of the wafers so that the contacting wave may spread out evenly to the edges. The machine usually has spacers that hold the edges apart until the centers of the wafers are brought into contact. The spacers are then removed allowing the contacting wave to spread. If there are multiple points of initial contact, as may be the case with manual bonding, the contacting wave could surround certain areas of the wafers resulting in trapped bubbles. Once the wafers undergo this initial room temperature bond, the bond is usually strengthened with higher temperature anneals. Depending on the application, the wafers could be annealed at temperatures as high as 1100°C [17]. Another common final step that may go before or after the high temperature bond anneal is the thinning of one of the wafers. This is done for functional reasons with SOI fabrication technologies in order to expose the Si device layer. It may also be done to alleviate stresses in the bonded wafer pair due to bowing. The bowing may be a results of mismatches between the two wafers in the coefficient of thermal expansion (CTE). It may also be the result of bowing over small length scales that occured during the bonding process to account for microroughness of the wafers. Whatever the reason, the built in elastic energy required to deform the wafers lowers the surface energy of the bond, and thinning one of the wafers minimizes this elastic energy. This results in a stronger bond.

2.2 Low Temperature Wafer Bonding

While a high temperature anneal increases the bond strength, such thermal cycles are not always necessary depending on the particular application. In fact, the application may set some upper limit on the temperature that can be withstood. Such is the case with certain

SOI wafer fabrication techniques in which elevated temperature exposure has a detrimental effect on implanted or diffused etch stop layers via diffusive broadening [4]. This is also the case with a particular subset of wafer bonding, often called heterobonding, in which the wafers being bonded are composed of dissimilar materials. Without taking special precautions, differences in the thermal coefficents of expansion (α) of the two materials will result in potentially destructive compressive or tensile stresses at elevated temperatures ($> 200°C$). This was the case with the wafer bonding of GaAs ($\alpha_{GaAs} = 6.86 \cdot 10^{-6} C^{-1}$) to Si ($\alpha_{Si} = 2.6 \cdot 10^{-6} C^{-1}$) as presented in this thesis. Because it was not possible to perform high temperature bond strengthening anneals, it was necessary to fully understand the inital room temperature bond and to closely monitor the relevant parameters of the wafers. For this reason it will be useful to discuss the basic chemistry of wafer bonding [30] and the impact that the state of the bonding surfaces and the annealing times and temperatures have on the wafer bonding results. The process used in this work was formed based on theory found in the wafer bonding literature. The following explanations taken from the literature [28, 29, 24, 30] give theoretical explanations which have been formulated based on the results of a significant number of experiments. These experiments mostly involved Si-Si bonding of wafers with thin native oxide layers. This is not the identical situation faced in this work in which low temperature deposited oxides were used, however, the relevant chemistry should be quite similar.

2.3 Wafer Bonding Chemistry

As previously stated, wafer bonding without an adhesive is feasible and is a result of the short range intermolecular and interatomic attraction forces between the bonding surfaces. This is theoretically true for any two solids but it requires the mating surfaces to be perfectly clean as is usually only the case in an ultrahigh vacuum (UHV) system. In an ambient other than UHV the mating surfaces are usually terminated by foreign species [30]. The surface termination in a typical room ambient may, however, be controlled by various chemical treatments. These treatments may serve the additional purpose of cleaning the surface of undesireable organic or ionic species.

2.3.1 Hydrophilic vs. Hydrophobic Surfaces

The state of the wafer surface and how the surface is chemically terminated determines the success of the bond and the resulting bond strength. In most cases and in the case of this work, the bonding surface of each wafer is some type of silica. It has been found that for bonding, the most relevant classification for the surface chemistry of the wafer is whether the surface is hydrophilic or hydrophobic. A hydrophobic surface repels water whereas a hydrophilic surface retains water. A more scientific comparison is that for a hydrophobic surface, the water to solid surface interfacial free energy is higher than for a hydrophilic surface. A wafer surface is made hydrophilic or hydrophobic by dipping the wafer in a chemical bath. For example, a piranha clean (3:1 H_2SO_4:H_2O_2) will make the wafer surfaces hydrophilic whereas an HF dip creates a hydrophobic surface. As a result of a hydrophilic treatment, the surface of the wafer is fully hydroxylated meaning that the surface is terminated by hydroxyl (OH) groups. The presence of these groups terminating the SiO_2 surface implies the presence of silanol groups (SiOH). At relative humidities greater than about 50% [30] the surface becomes hydrated (owing to its hydrophlicity) when the oxygen atom in adsorbed water molecules forms a hydrogen bond with the hydrogen atom in the silanol groups [24]. When two such surfaces are brought into contact, a group of water molecular triplets (three water molecules hydrogen bonded together) will complete a link of hydrogen bonds between the two wafer surfaces (Figure 2-1). This is because the free energy for a water triplet is less than the free energy for three separate water molecules [8]. At this point, a water assisted bond, SiOH$\cdots$(HOH)$\cdots$OHSi bridges the gap between the two wafers (the length of this trimer bond is $\sim$10Å.

A similar situation occurs for hydrophobic wafers prepared by an HF dip. As previously mentioned, the literature deals primarily with Si-Si bonding without any intermediate oxide layer. However, in the case of hydrophilic surface termination as described above, the Si wafer is covered with a thin native oxide that grows during the hydrophilic chemical dip. Consequently, the case of bare Si-Si hydrophilic wafer bonding is very similar to the case in this work in which the bonding occurs between two silicon oxide films. However, for Si-Si hydrophobic wafer bonding, the HF dip removes any native oxide and the bonding occurs between the purely Si surfaces. Therefore, it is more difficult to compare Si-Si hydrophobic wafer bonding as presented in the literature with hydrophobic SiO_2-SiO_2 bonding. The

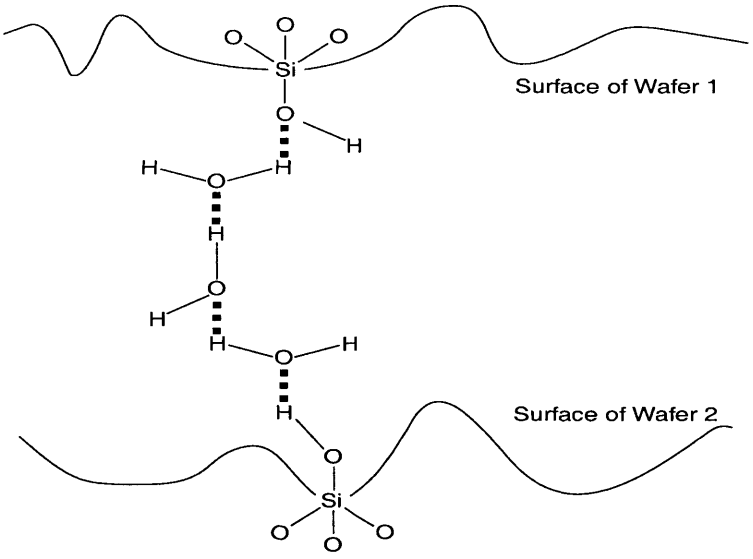


Figure 2-1: A water trimer completing a link of hydrogen bonds between two hydrophilic surfaces.

comparison is not far off, however, because in both it is the dangling Si atom either as a part of the oxide or as a part of the silicon crystal that is involved in the surface termination and bonding. That said, a comparison can be made between hydrophilic and hydrophobic Si-Si wafer bonding as presented in the literature. And this comparison may be extended to hydrophilic and hydrophobic SiO_2-SiO_2 wafer bonding.

Following the HF dip and contact, three HF molecules bridge the gap between the two hydrophobic wafers. The energy of the H-F hydrogen bond is 6.7 kcal/mol whereas the energy of the H-O hydrogen bond which links the hydrophilic surfaces is 10kcal/mol. Consequently, at low temperatures after initial contact, hydrophilic wafers bond with a stronger bond than hydrophobic wafers.

2.3.2 Bond Strengthening

The second stage of the bond formation process for hydrophlic surfaces occurs in the range from room temperature to 110°C. At this point two reactions are occuring that increase the bond strength [28]. The first is the slow fracture effect of Si–O–Si bonds on both bonding

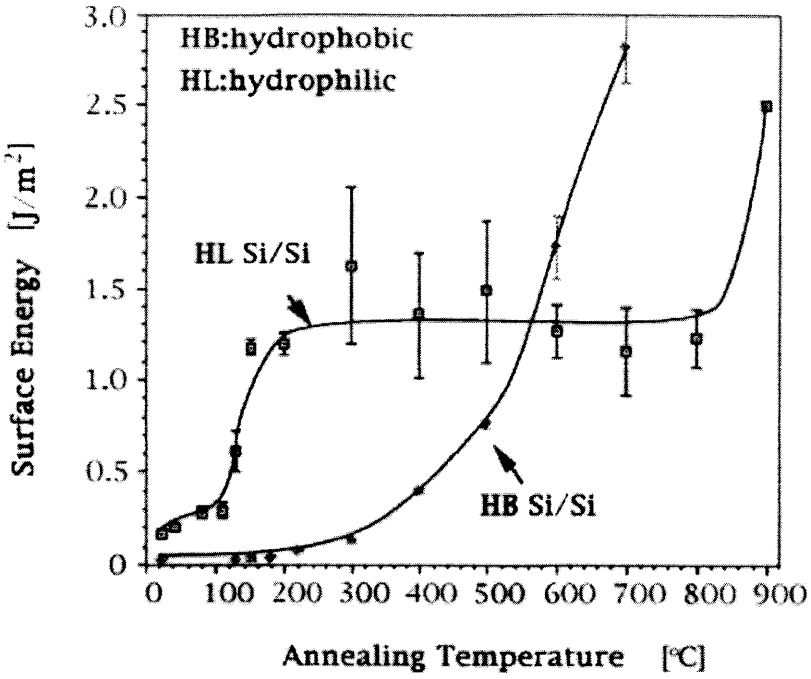


Figure 2-2: Surface energy vs. annealing temperature for hydrophilic and hydrophobic wafer bonding [29].

surfaces via attack by the interface water [28],

$$Si{-}O{-}Si + HOH \rightarrow Si{-}OH + HO{-}Si \tag{2.1}$$

This reaction applies for each surface independent of the other wafer surface. In other words, the Si–O–Si bonds are not across the gap between the two wafers but rather refer to just one wafer. This results in more silanol groups available for supporting bonds across the gap. The second reaction is the actual rearrangement of the water molecules to form more stable hydrogen bonded structures [28].

The third stage of the bond formation process for hydrophilic surfaces occurs in the range from 110°C to 150°C. At this stage, strong siloxane (Si-O-Si) bonds may form from the following reaction [28],

$$Si{-}OH + HO{-}Si \rightleftharpoons Si{-}O{-}Si + H_2O \tag{2.2}$$

In this case, the Si–O–Si are gap bridging bonds which could be written more explicitly as

Si_A–O–Si_B where the subscripts A and B refer to the two wafers being bonded, A and B. As long as the water can diffuse out to the edges of the wafer or through the oxide, the reaction will proceed mostly from left to right. At temperatures above 150°C most of the water has been desorbed from the bonding interface and the silanol groups have formed siloxane groups. Consequently, the bond strength does not increase above 150°C. Not until the oxide starts to reflow at temperatures above 800°C does the bond strength increase for hydrophilic wafer bonding. The bond strength (surface energy) dependence on annealing temperature for hydrophilic wafer bonding is compared with hydrophobic wafer bonding in Figure 2-2. As previously mentioned, the wafer bonding of GaAs to Si must be kept as low as possible because of the mismatch in coefficient of thermal expansion. It is very clear from Figure 2-2 that hydrophilic surface preparation should, therefore, be used and that anneals need be no higher than 150−200°C.

Chapter 3

Low Temperature Oxide Deposition and Planarization

As mentioned in the last chapter, the two wafers for bonding must be flat with microcroughness on the order of only a few angstroms. The processed Si wafers as they came from IBM were neither locally nor globally smooth. While Si processing is a fairly planar process in that surface variations are less than a micron, this is still three orders of magnitude too rough for wafer bonding. The final microroughness or topography on the wafer is caused by a combination of the multiple layers of metal used in the process and the microroughness of the final deposited passivation layer. In the case of the particular wafers used, passivation cuts had also been made resulting in many deep ($\sim 1\mu$m) holes in the passivation layer. Some type of intermediate layer had to be applied and planarized back in order to remove the roughness. This is a common problem in silicon processing encountered after each layer of metallization is applied. The common solution is to deposit a low temperature oxide and then use a CMP (Chemical-Mechanical Polishing) tool to polish back the deposited oxide. In this case of wafer bonding with the processed wafer, the oxide serves two purposes. As just said it acts as the film to be planarized. In addition, it is the final bonding surface of the wafer and all of the bonds between the two wafers occur between atoms or molecules present in the oxide and on the surface of the oxide as described in the previous chapter.

3.1 The Choice of a Suitable Oxide

The most crucial factor that limits the field of available oxides for this process is the simple fact that the Si wafers contain processed circuitry. These wafers are fully front- and back-end processed. High temperatures ($> 660°$) would melt the aluminum metallization and higher temperatures ($> 800°$) would result in dopant redistribution. Consequently, a low temperature deposited oxide must be used. It was important to know exactly what was the maximum temperature that could be withstood. This is because the general rule is that the higher the temperature of deposition or densification anneal, the higher the oxide quality. The film quality or density is important for the bonding step. The more dense the film, the more potential silanol groups available for bond formation and the stronger the resulting bond.

3.1.1 Aluminum-Silicon Eutectic Behavior

The matter of determining the maximum allowable oxide deposition or densification temperature requires looking at the aluminum-silicon system [10]. The aluminum silicon contacts of all the parts of an integrated circuit are adversely affected at the lowest temperatures. The eutectic point (lowest temperature at which the Al-Si alloy is in the liquid state) occurs at 88.7% Al and 11.3% Si at a temperature of 577°C as shown in the phase diagram in Figure 3-1. However, problems such as spiking may occur at even lower temperatures. Between 400°C and the eutectic temperature, the solubilibty of silicon in aluminum ranges from 0.25% to 1.5% by weight. Spiking occurs when the diffusion of silicon into aluminum at these temperatures is localized at certain points along the contact. The aluminum then spikes back into the silicon regions. If deep enough, these spikes may short out junctions below the contact. These problems are encountered in standard Si processing when the contacts are annealed between temperatures of 450°C and 500°C. Measures are usually taken to alleviate the spiking such as deposition of aluminum with 1% silicon by weight. Consequently it is safe to assume that temperatures as high as 450°C, the low temperature side of the annealing range of temperatures, will have no adverse affects on the contacts or any other part of the circuitry. This temperature was chosen as the maximum temperature that the procesed Si wafers could endure for any processing prior to bonding with the GaAs wafer.

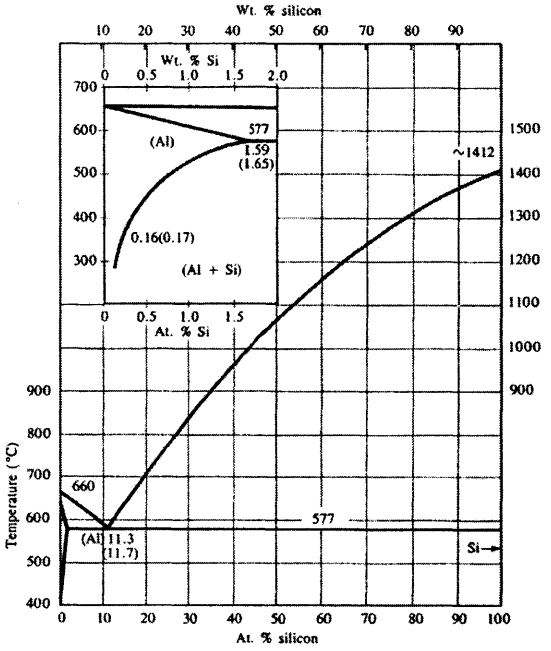


Figure 3-1: Aluminum-Silicon phase diagram [10].

3.1.2 Low Temperature Oxides

Because of this temperature constraint, it was necessary to deposit a low temperature oxide to act as the planarizing and bonding film. Low temperature oxide deposition systems have been developed in order to meet the common need to deposit an oxide at temperatures below 450°C. The most common type of system is a Plasma Enhanced Chemical Vapor Deposition (PECVD) system. Chemical Vapor Deposition (CVD) involves the transportation of reacting gaseous species to a surface (i.e. the wafer surface), the adsorption of the species on the surface, a heterogenous surface reaction catalyzed by the surface resulting in a deposited solid, and desorption of the gaseous reaction products away from the surface [21]. The temperature affects the equilibrium quantity of free radicals available to promote film deposition. To obtain sufficiently high growth rates, the gases used in typical CVD reactors must be at a certain temperature. This temperature can be lowered with the use of a low pressure plasma. The plasma in a PECVD system is formed by placing an RF electric field across a gas resulting in an ionized gas containing an equal density of gas ions and free electrons. A typical PECVD radial flow reactor is shown in Figure 3-2.

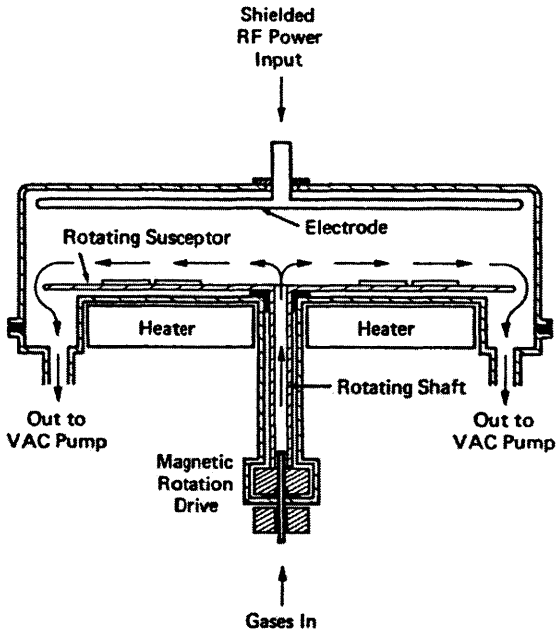


Figure 3-2: A typical radial flow PECVD reactor [20].

At lower pressures, the mean free path of electrons in the plasma is larger than that of the ions. Given a greater mean free path over which to be accelerated by a high electric field, the electrons will be accelerated to higher velocities. When electrons collide with the heavier species in the plasma such as the gas molecules, atoms, or ions, the electrons lose little energy and the heavier species gain little energy. The result is high energy electrons and lower energy gaseous species. If the electron density is low compared to the density of the gaseous species, the gas may have a low average temperature even though the electrons have a high temperature. These high temperature electrons promote a higher than equilibrium quantity of free radicals. The result is deposition of a solid at growth rates which are equivalent to the rates obtained using regular thermal CVD, but at temperatures which can be lower [20].

PECVD Film Stress

When SiO_2 films are deposited by PECVD, the films exhibit intrinsic tensile or compressive stress. This stress causes the wafer to bow. Tensile stress causes a concave bow and compressive stress causes convex bowing. The type of stress is determined by the details

of the deposition process such as the presence of various impurities [11]. This bowing must be counteracted in order for initial room temperature wafer bonding to occur. The energy required to "un-bow" the wafers must be less than the surface bonding energy for the bond to occur. If the wafers do bond, the bond strength is decreased because of the bowing. This bowing is in addition to wafer bowing that may exist for the plain silicon or GaAs wafer itself. If the film stress is compressive (as it is for the PECVD oxide film deposited for this work), it is advantageous to use a wafer that initially has a convex bow. Some cancellation may occur resulting in less final wafer bow. The details of the bowing effects the bonding results. As will be seen later on, bonding two silicon wafers both with PECVD oxide results in unbonded regions around the edges because the oxide on both wafers is under compressive stress (convex bowing). This deposited film stress induced wafer bowing sets an upper limit on the amount of deposited oxide that can be withstood. In addition to increased microroughness, the greater the amount of deposited oxide the greater the wafer bowing. Therefore, it is necessary to to deposit the minimum amount of oxide possible.

3.2 Dielectric Chemical Mechanical Planarization

The planarization of a dielectric such as a PECVD oxide may be performed with a technique known as Chemical Mechanical Planarization (CMP). As the name suggests, CMP uses a combination of chemical reactions and mechanical abrasions to remove or polish the oxide layer. In most cases the goal of a CMP step is to remove global roughness and/or local microroughness from the oxide surface resulting in a perfectly flat surface. In modern Si IC processing CMP is used to planarize the wafer between each metal deposition step and may also be used for Shallow Trench Isolation (STI) planarization [6] and for damascene Cu metal back-end processing. A schematic of a typical rotary CMP system is shown in Figure 3-3. The system consists of a rotating table with an affixed replaceable pad. A rotating head picks up the wafer and rotates the wafer on the rotating pad. CMP is usually carried out in the presence of a tiny grit-containing polishing liquid slurry which provides the chemical polishing action and in addition to the pad, provides the mechanical polishing action. Within a CMP system, the type of slurry, type of pad, pad revolutions per minute (rpm), head rpm, and downforce (the force applied by the head to the wafer against the pad) may all be varied to achieve the desired results. Because the goal of a typical CMP

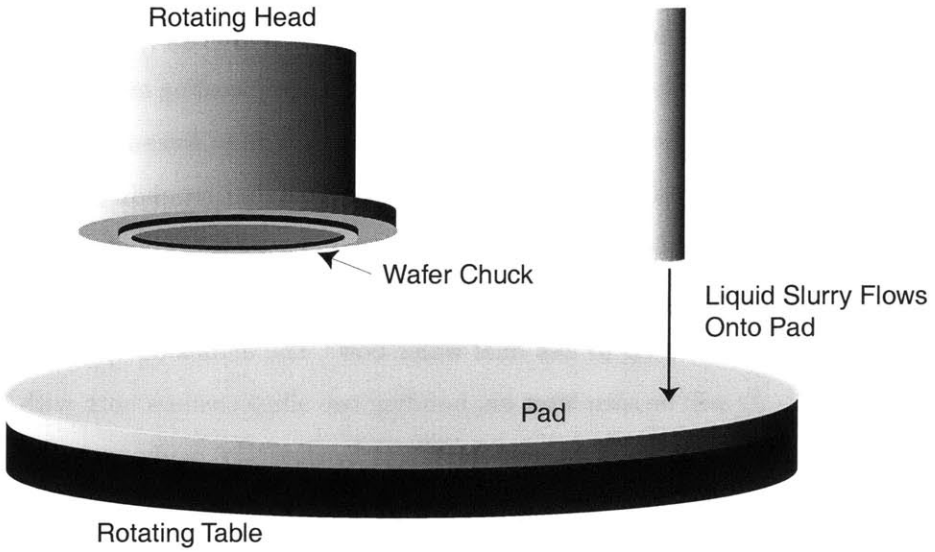


Figure 3-3: Basic Components of a Rotary CMP System.

step (i.e. inter-metal dielectric planarization) is to achieve global variations of less than 1000Å across a wafer that may be 200mm, CMP is a very sensitive step. Not only must the above parameters be determined, but the age of the pad and the pad condition will also affect CMP results. Inevitably, the determination of the proper values for the above parameters must be done emperically with dummy wafers. However, there are some general principles that apply in any CMP system that may be used as a guide. These rules apply to the polish rate and the uniformity of this rate across the wafer.

As would be expected, the faster the wafer and pad rotate, and the higher the down force, the higher the polishing rate. The uniformity depends on both the pad hardness, down force, and the density of the structure to be polished. In general, the higher the density, the lower the polish rate. This density is the density inside a square region that has been termed the *density window*. The length of a side of the density window is called the interaction distance. An intuitive physical interpretation of the interaction distance is the macroscopic distance over which the pad bends and conforms to the wafer surface and is typically several mm [25]. This means that for die larger than the density window and with nonuniform pattern density, the planarization will not be uniform. This is certainly the case with the IBM wafers in which the die are about 20mmx20mm and have varying denisty as will be shown graphically later. In the ideal case of a perfect polishing system,

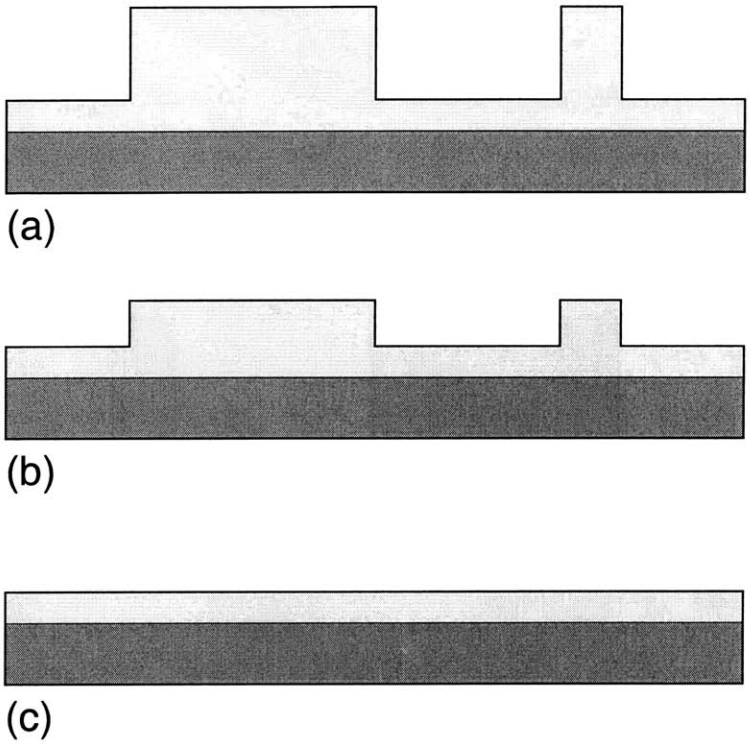


Figure 3-4: Ideal Polishing of raised features: (a) Before Polishing (b) Partially Polished, the raised features are polished back but the lower areas aren't polished at all (c) After polishing

only the highest features are removed and lower areas do not polish away at all (Figure 3-4). In reality, both the raised and lowered features are polished, and planarity is achieved gradually because the polish rate is higher for raised features than for the sunken areas (Figure 3-5). This difference in polish rate between two features of different heights is a function of the height difference and the pad hardness. The harder the pad, the less the pad deforms. This means that areas of the wafer that are raised will etch faster than areas that are sunken. If the pad is less firm, it may be able to deform into the sunken areas resulting in an even removal of oxide instead of the desired planarizing action.

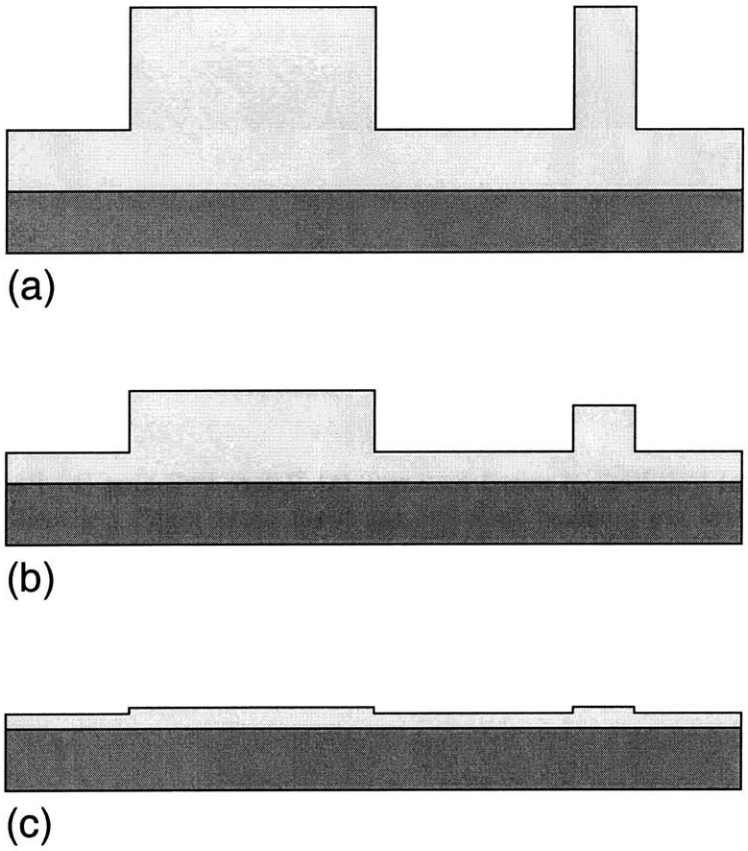


Figure 3-5: Actual Gradual Polishing of raised features: (a) Before Polishing (b) Partially Polished, both the raised and lowered features are polished, but the raised features are polished back at a higher rate than the lower areas (c) After polishing

3.3 Procedure and Results

3.3.1 Wafer Cutting, Cleaning, and Profilometry

The first step in this processed Si CMOS wafer bonding process involves cleaning and characterizing the surface of the processed wafers. The wafers were originally 8" diameter wafers, but they had to be laser cut by an outside source to 4" diameter wafers for processing in MTL. Consequently the wafers had to be immediately cleaned upon entry into the lab. Once the wafers were cleaned, it was necessary to determine the surface profile. The profile guides the deposition process and the CMP processing steps. This initial profiling was performed using a KLA Tencor P-10. This tool is useful for looking at features on length scales from 1μm to several millimeters and has a vertical resolution of better than 100Å. Upon general inspection of the IBM wafers with a microscope, it was clear that there were three different areas in which different topography was expected. The first area consisted of dense metal lines where each metal layer had been used and was tightly packed. The second area consisted of the test devices in which there were only a few thick metal lines. However, the most prominent feature on the wafers existed in this area. The passivation cuts made through the passivation layer to the upper metal probing pads were about 1μm deep, about $50\mu m \times 50\mu m$, and were set on approximately a 150μm pitch. Unfortunately, these passivation cuts are an artificial source of topography. Normally, these "cuts" would be made after the wafer bonding process and would not come into play at this point. However, it is possible to bond wafers together that are flat except for some cavities as long as the surface area covered by the cavities is small compared to the surrounding flat area. This is quite usually the case with wafer bonding for MEMs applications. The third type of area consisted of little or no features other than the layers of films and dielectrics that made up the dielectric stack. A surface profile taken with the P-10 profile is shown in Figure 3-6 for each area type shown along side a picture of the area taken through a microscope. The details of the IBM back-end process used for these wafers is proprietary information. However, it can be assumed that some combination of planarizing via CMP or Spin-On Glass (SOG) was used because areas I and III showed total surface height variations on the order of only 1000Å. This is small compared with the typical thickness of upper metal layers which may exceed 5000Å. Had passivation cuts not been made, the total surface profile would have been merely the 1000Å variations.

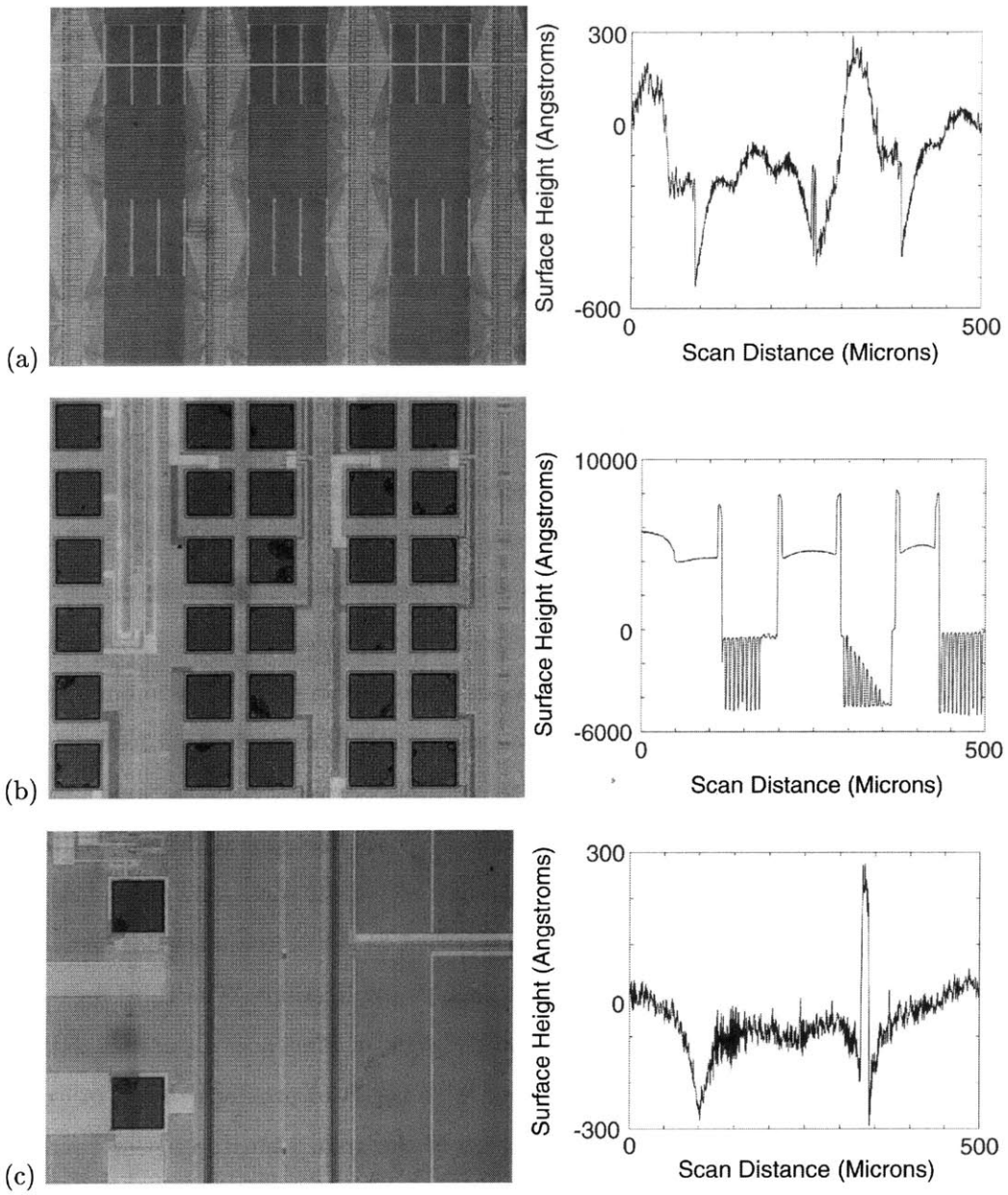


Figure 3-6: Microphotographs of three different typical areas of the IBM wafers along with the respective profile trace: (a) dense metallization (b) probing pads (c) low pattern density area.

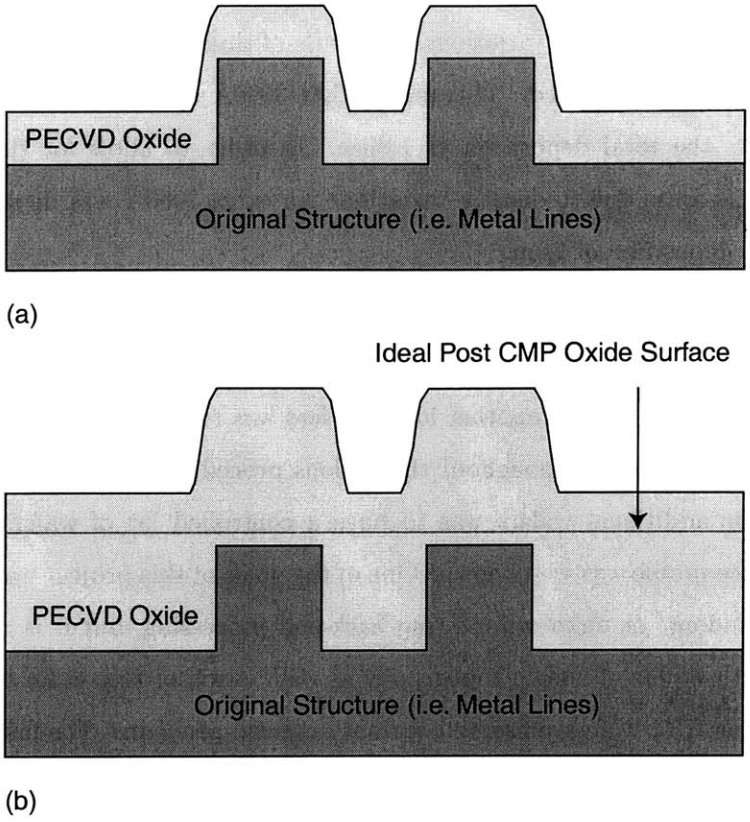


Figure 3-7: (a) Conformal covering of features (b) Overcovering for subsequent sacrificial polish back.

This profile information is useful in determining the amount of oxide that should be deposited. It is not possible, nor is it necessary for the case of wafer bonding to fully remove all of the features and be left with an atomically smooth surface. This is especially the case when starting with a wafer that is fully processed and has many topographical features. Therefore, it was necessary to choose the features that must be removed. As previously mentioned, it is possible to bond wafers with small cavities. Consequently, it was decided that it would not be necessary to polish back the full depth of the passivation cuts. This left the fairly random variations everywhere else on the wafers as the features of concern. As mentioned, these variations were on the order of 1000Å. This is actually small compared with the depth of the passivation cuts. Because PECVD oxides coat conformally, (Figure 3-7) it was necessary to deposit at least 1μm just to fill the passivation cuts. Some of the cuts seemed to be as deep as 1.2μm, so to be on the safe side, approximately 1.5μm

would have filled the openings. In addition to filling the openings, there must be enough oxide to CMP away the 1000Å variations. As a rule of thumb, for every xÅ in topography, 3xÅ of oxide should be removed. This means that 3000Å of oxide should be removed by CMP. This puts the total deposition at 1.8μm. In order to allow for the case of over-polishing in some areas due to density variations, an extra 2000Å was deposited, resulting in a total oxide deposition of 2μm.

3.3.2 Simulation Wafers

In addition to the IBM wafers, another lot of wafers was run through the same processing steps, and will be mentioned thoughout the various procedure sections of this thesis. The purpose of these additional wafers was to have a controlled lot of wafers for which the beginning surface profile was well known. One of the goals of this project was to bond using wafers with "random" or unknown existing back-end processing, but it is useful along the way to work with wafers of known topography as well. Another reason for these additional wafers is that the IBM wafers presented various artificial problems. For instance, the IBM wafers were thicker (700μm thick) than standard 4" wafers (500μm thick). This presents some problems with wafer handling and bonding. Also, as already mentioned, the IBM wafers had passivation cuts made to probing pads in the upper metal layer. This is because these wafers were tested with probe stations at IBM prior to being offered for this project. There are a few other issues with using the IBM wafers, and they will be discussed in some of the sections dealing with the results. These additional wafers could be called simulation wafers because they were designed to simulate the final topography of the IBM wafers. As discussed in the profiling section, the IBM wafers contained maximum surface height variations of approximately 1000Å. In order to simulate these conditions, 1000Å of aluminum was deposited and patterened on standard 4" silicon wafers. The pattern consisted of some low density metallization and areas of serpentine wiring 5μm wide set on a 5μm pitch. Surface profiles for the simulation wafers are shown in Figure 3-8

3.3.3 Low Temperature Oxide Deposition

The oxide deposition is a rather straightforward step. The 2μm of PECVD oxide was deposited using a Novellus Concept One CVD system with a silane source. A pre-deposition clean is required. Because of the existence of exposed aluminum on the wafers, the typical

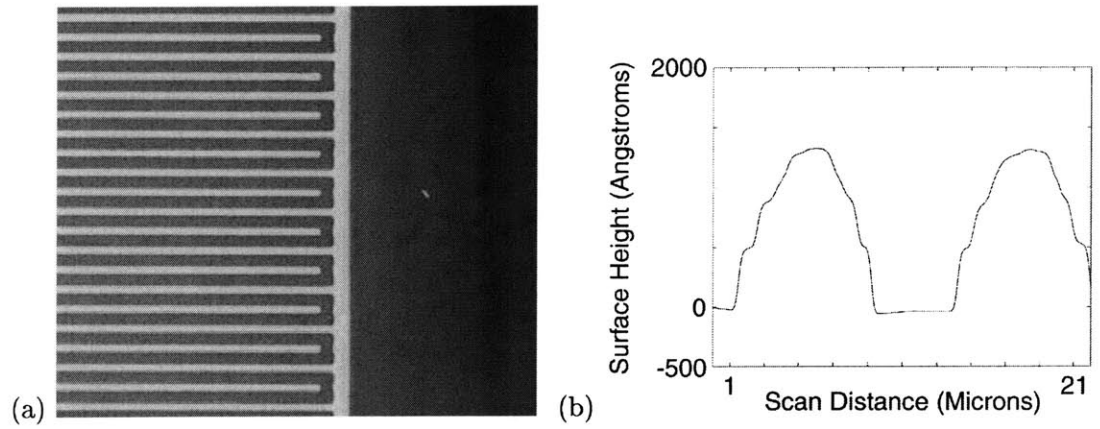


Figure 3-8: Microphotograph of a simulation wafer and the corresponding surface profile.

cleaning method of sulfuric acid and hydrogen peroxide (3:1 H_2SO_4:H_2O_2) cannot be used because it viciously attacks aluminum. However, a commercially available cleaning and stripping agent called Nanostrip which contains, among other things, sulfuric acid and hydrogen peroxide can be used since it only mildly attacks aluminum. Once the oxide is deposited, it is necessary to again look at the new profile. The PECVD oxide coats conformally, but can slightly change the surface profile. Figure 3-9 shows the surface profile for various features on the IBM wafers after the oxide deposition. Figure 3-10 shows the surface profile for the simulation wafers after the oxide deposition. For comparison, Figure 3-11 shows the surface profile for a bare silicon wafer with 2μm of oxide. This is helpful in seeing what of the surface profile is due to underlying topography versus what variations the oxide itself contributes. It should be mentioned that some of the higher frequency components of these surface profiles may be attributed to noise from vibrations in the room, but longer wavelength (in the lateral dimesnion) variations greater than 100Å in amplitude (the vertical dimension) are certainly real structure.

To obtain accuracy on the order of an angstrom, an AFM (Atomic Force Microscope) must be used. In Chapter 2, it was shown that the length of the water trimer bond between two wafers is approximately 10Å, meaning that each wafer should have an r.m.s. microroughness of about 5Å to obtain a strong bond. An AFM was used to determine the microroughness of wafers at various stages. It can be seen from Figure 3-12 that even when deposited on a plain wafer that is initially very flat, the PECVD oxide is not perfectly

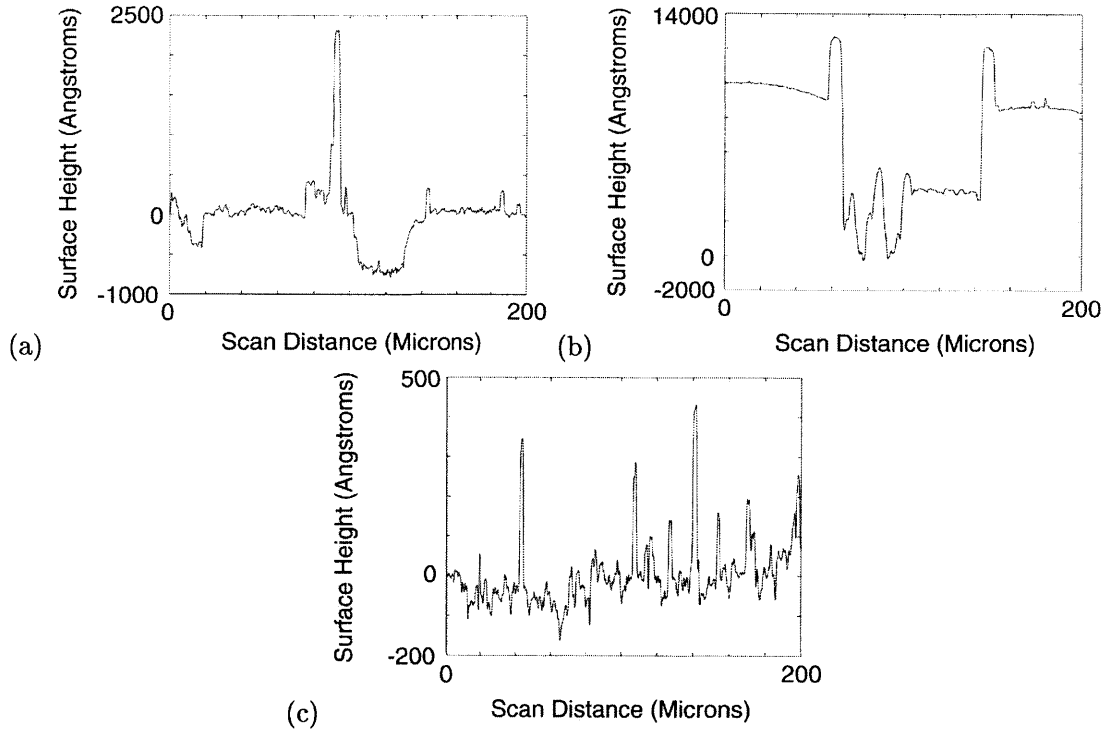


Figure 3-9: Surface profiles for the three different areas of the IBM wafers after the PECVD oxide deposition: (a) dense metallization (b) probing pads (c) low density area.

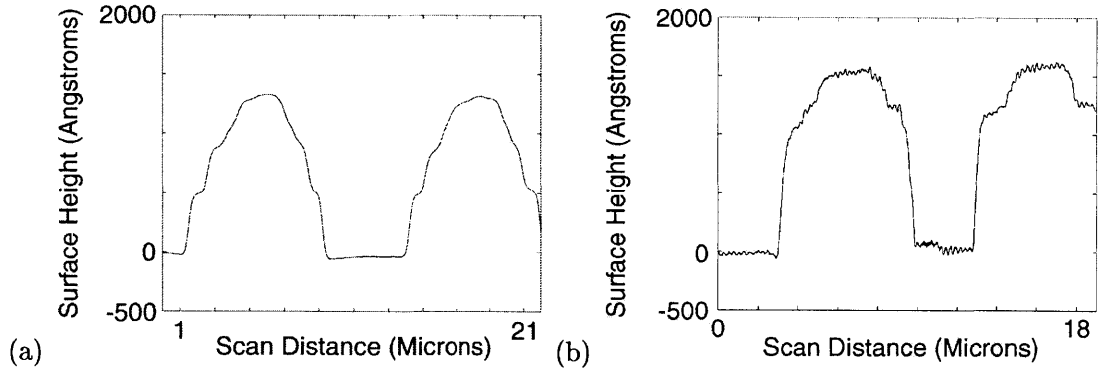


Figure 3-10: Surface profiles for the simulation wafers: (a) before PECVD oxide deposition, repeated here for comparison (b) post PECVD oxide deposition.

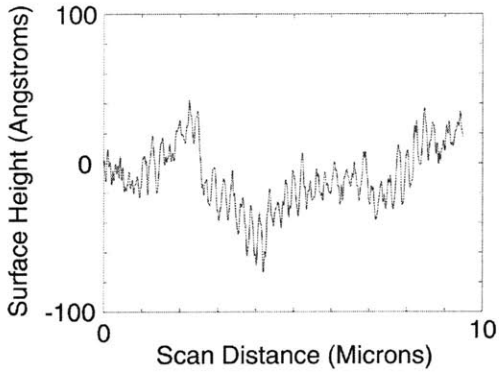


Figure 3-11: Surface profiles for a bare wafer with 2μm of PECVD oxide

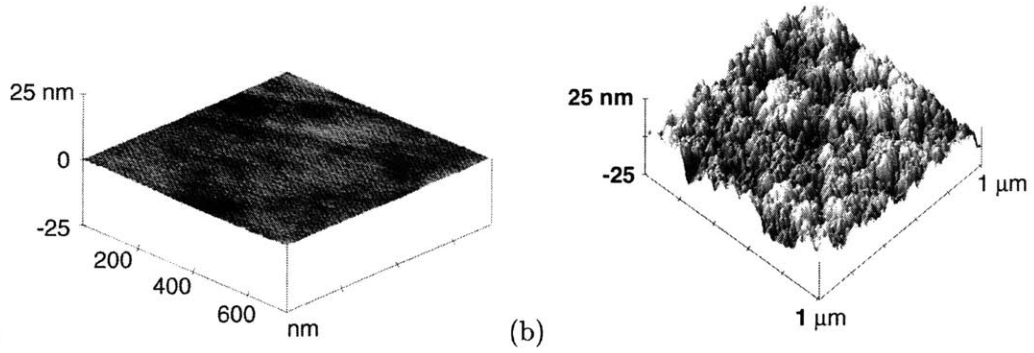


Figure 3-12: AFM images shown on the same vertical scale for (a) a bare test grade silicon wafer surface, and (b) a surface of 2μm of PECVD oxide deposited on a bare test grade silicon wafer.

flat. The r.m.s. roughness of the plain silicon wafer was 1.4Å. After the deposition of 2μm of oxide, the r.m.s. roughness increased to 40Å. It is this microroughness that must be removed by the CMP process in addition to some of the longer range (hundreds of microns) surface variations as shown by the P10 profiles in order to obtain a strong bond.

3.3.4 Low Temperature Oxide Anneal

Before moving on to the CMP, the topic of oxide densification or annealing must be discussed. As-deposited PECVD films usually tend to exhibit some undesireable characteristics, such as an increased tensile stress during subsequent high temperature processing and a high hydrogen content [9]. Some of these characteristics can be improved with an anneal. Often, this anneal must be kept to fairly low temperatures depending on the details of the metals used in the back-end processing. Some researchers [22] have had success using RTA (Rapid Thermal Annealing) in which, as the name implies, the wafer is exposed to high temperatures for only a short time (less than a minute). This is sometimes enough to anneal out the defects in the film without affecting the contacts. Whatever the method and details, the post deposition anneal is a common step. For this process, the goal of the anneal is to promote the outgassing of any gases (most likely H_2) that became trapped in the oxide during the deposition. Without this step, outgassing may occur during post-bond anneals in which case the gas cannot easily escape and may create voids in the bond or even full debonding of the wafers. The temperature used for this step was 450°, which was the maximum allowable temperature for this process as determined earlier in this chapter.

3.3.5 CMP

Once the wafers are profiled and measured with the AFM, the next step is to polish back the oxide layer to obtain a smooth surface for bonding. A recursive polishing and profiling process is used until the profile is sufficiently flat. The CMP tool used was a Strasbaugh 6EG with modifications for processing 4" wafers. The slurry used for polishing the oxide was Semi-Sperse D7000 from Cabot Microelectronics. As previously mentioned, at least 1000Å needed to be polished back in order to remove the roughness from the underlying metal layers on the IBM wafers. The simulation wafers were also used at this stage which made it easy to see the features and the subsequent removal of the features after polishing. Again, the simulation wafers contained about 1200Å of aluminum serpentine wiring. This

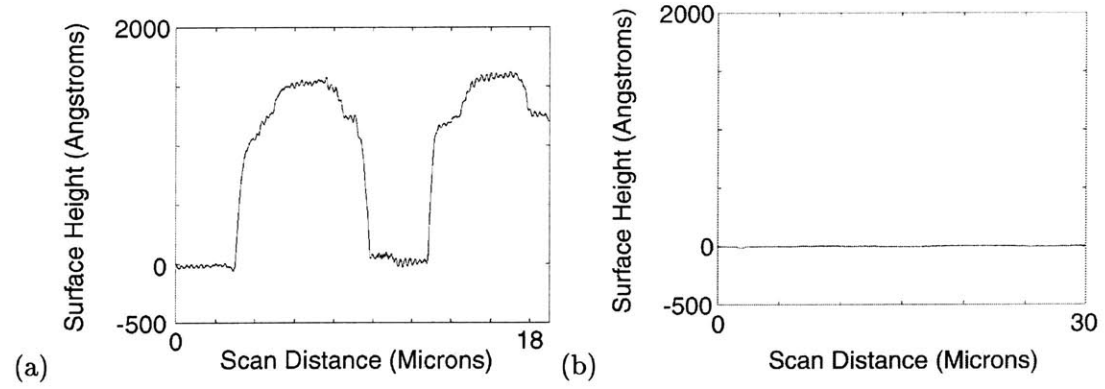


Figure 3-13: Surface profiles shown on the same vertical scale for (a) the simulation wafers after oxide deposition, and (b) the simulation wafers after CMP planarization.

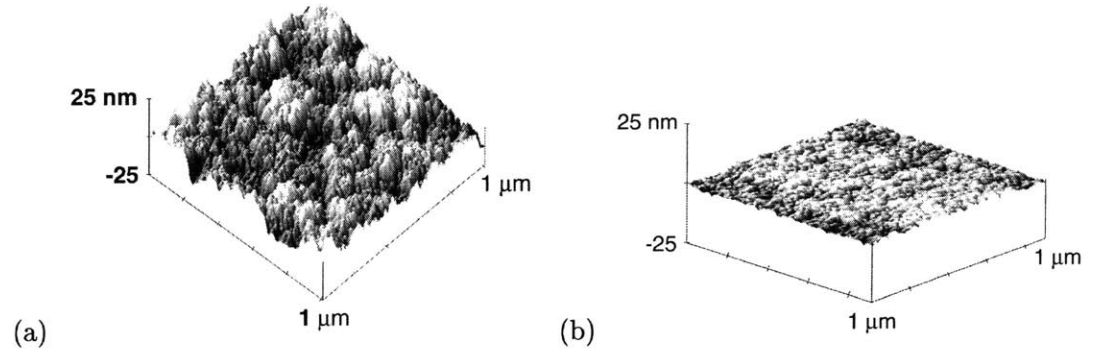


Figure 3-14: AFM images shown on the same vertical scale for (a) the surface of 2μm of PECVD oxide deposited on a test grade Si wafer, and (b) the surface of the same wafer after CMP planarization.

created topography on the order of that for the IBM wafers. The wafers were sufficiently flat after removal of about 3000Å of oxide. The recipe details can be found in the appendix. Surface profiles of the simulation wafers taken after polishing are shown in Figure 3-13. The microroughness of the PECVD oxide, however, is removed after just one polishing. An image taken by the AFM shown in Figure 3-14 illustrates the change in surface roughness. Surface profiles taken from the IBM wafers after CMP are shown in Figure 3-15.

3.3.6 Slurry Removal and Post CMP Cleaning

The task of post CMP cleaning involves the removal of leftover slurry particles on the wafer after the CMP step. The Semi-Sperse D7000 slurry used for this research contained silica

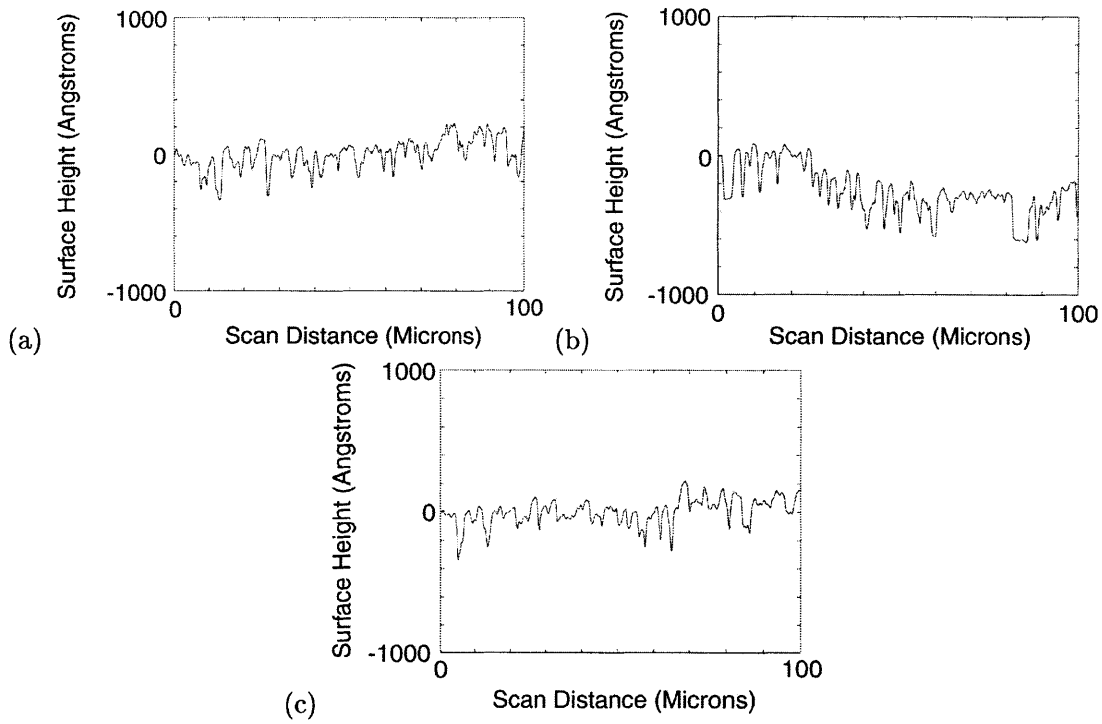


Figure 3-15: Surface profiles shown on the same vertical scale for the IBM wafers for three different areas (a) dense metallization (b) probing pads and (c) low density area.

particles ranging in size from 150–350nm. Obviously, the presence of such particles is a problem for wafer bonding in which the roughness must be less than 1nm. The clean is well known to be a difficult step because it is different from the typical problem of the removal of ionic or organic contaminents. Slurry is an alkaline solution (containing KOH) with suspended solid silica particles (SiO_x). Some of these silica particles remain on the wafer after the CMP step. The adhesion of the particles to the wafer surface may be attributed to at least four different interactions: chemical bonding, electrostatic forces, van der Waals forces [23], and van der Waals assisted embedding of the particle into the wafer surface caused by the pressure applied during CMP [1]. The electrostatic forces arise from an arrangement of charge on the slurry particle called the electrical double layer. The layer consists of charges on the slurry particles (H+ or OH-) and a cloud of oppositely charged ionic species from the slurry solvent which are attracted to the charges on the slurry. The potential difference between these two layers is called the zeta potential and provides the mechanism for adhesion of the slurry particles to the wafer surface. The H+ or OH- charge on the slurry particle is related to the pH of the surrounding solvent and may be altered by changing the pH. The pH at which the net charge on the particle is zero is called the isoelectric point. Silicon dioxide has an iep at pH$\sim$3 [23]. Consequently, a strong acid like HCL, which is a good electrolyte, is useful in removing the slurry particles. HCL is part of the SC2 RCA clean which will be mentioned in the next chapter.

Removing the embedded particles requires different tactics. Commercial techniques used for removing such particles range from the use of brush systems, megasonic cleaning, carbon dioxide stream cleaning or some combination of these cleans. Due to the non-availability of such systems, it was necessary to find an alternative. It was found that HF could be used to etch away the embedded particles since they are composed of silica. Unfortunately, this also etches the oxide itself which increases the microroughness. Consequently, there is a tradeoff between microroughness and particle count. All particles can be removed or etched with a long HF etch, but the microroughness becomes too high to obtain a good bond. If the etch is too short, the microroughness is small but too many particles remain. In order to determine the optimum etch time a simple experiment was performed. Wafers were CMP'd and then exposed to a solution of 50:1 H_2O:HF for various times. The samples were then examined with an AFM (Atomic Force Microscope). Various 10μm x 10μm areas were scanned. The particle count and r.m.s. roughness were recorded for each sample. The r.m.s.

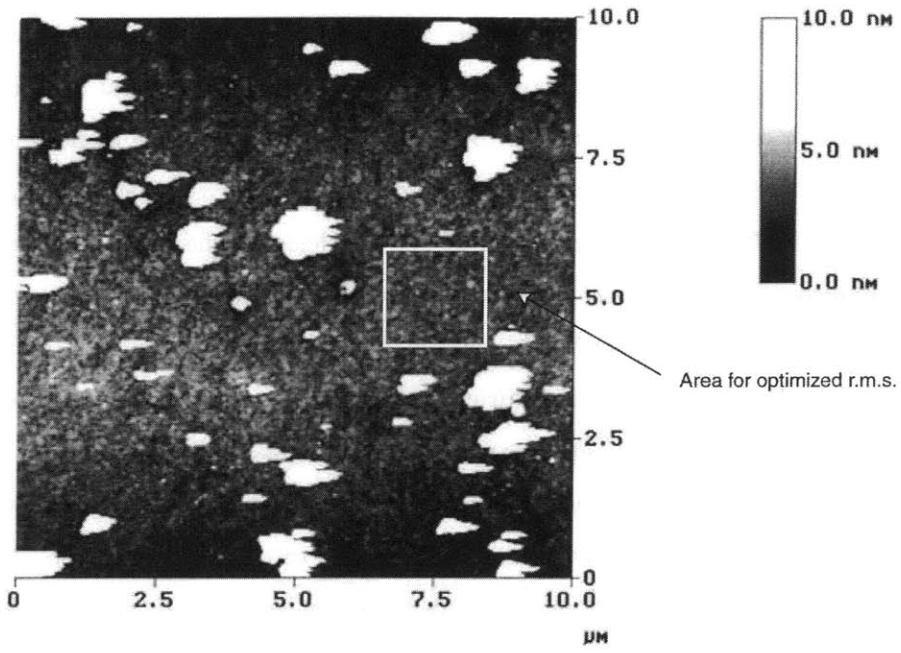


Figure 3-16: Top view AFM image of wafer with slurry particles. The box area, which is free of slurry particles, is the area used to calculate r.m.s. roughness neglecting slurry particles. Slurry particles are the white marks (note color scale applies for z direction, out of the page).

roughness was found only for areas that contained no slurry particles (see FIGURE 3-16). This eliminated the effect of the slurry particles on the roughness calculations. The results are shown in table 3.1. This table shows that most particles are removed within the first 45 seconds. The remaining particles are most likely embedded in the oxide. These embedded particles are progressively etched as can be seen by the decreasing average particle height. In practice, the best bonds were found for wafers with a 30 seconds HF etch. A discussion of the pre-bond clean which includes this HF etch follows in the next chapter.

50:1 Slurry Removal			
Etch Time (sec)	Particles per $100\mu m^2$	R.M.S. Roughness (Å)	Particle Height (nm)
0	50	3.0	50–100
15	30	3.5	30–40
30	10–15	3.5	15–25
45	2–5	3.5–4.0	5–20
60	1–3	4.5	3–8
75	0–1	4.5	8
135	0	6.5	N/A
255	0	12.5	N/A

Table 3.1: HF slurry removal statistics.

Chapter 4

Surface Preparation and Wafer Bonding

Once the wafers to be bonded are sufficiently planar, the wafer surfaces must be chemically treated in order to obtain the correct surface termination for bonding. In addition, it is the purpose of this chemical treatment to act as a final clean of any organic or ionic species on the wafer surfaces that may interfere with the bonding. As explained in Chapter 2, hydrophilic surfaces result in the strongest bonds when post-bond annealing is restricted to low temperatures ($< 200°C$). Consequently, it is desireable to find a chemical treatment or combination of treatments that results in a hydrophilic surface. Hydrophilicity, however, is a relative term. While one surface may be hydrophilic compared to another very hydrophobic surface, it may be slightly hydrophobic compared with yet another more hydrophilic surface. In the literature, one very common and rather simple technique is used to measure the relative hydrophilicity or hydrophobicity of a surface, the water drop contact angle measurement.

4.1 The Water Drop Contact Angle Measurement

The degree of hydrophilicity of a surface may be determined using the contact angle measurement. A small water droplet is placed on the surface and the angle between the surface and the water droplet is measured (Figure 4-1). The smaller the angle, the more hydrophilic the surface. The greater the angle, the more hydrophobic the surface. The water droplet must be kept small enough so that the shape of the drop is not significantly distorted by

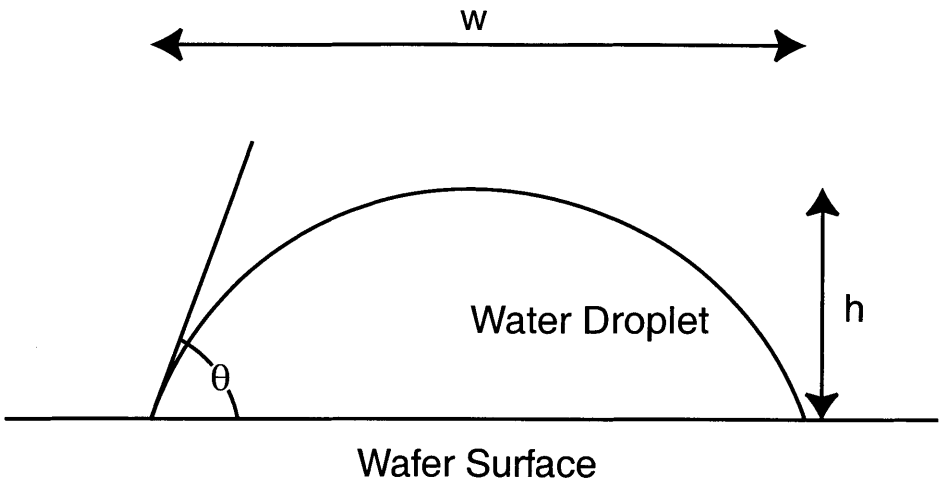


Figure 4-1: Water Droplet Contact Angle.

gravity. In the literature, water droplets of volume on the order of 5 μL are typically used [37]. The shape of the water droplet is determined by the minimization of all of the interfacial free energies associated with the drop. There is an energy per unit area value associated with each interface. There are three interfaces, the water to solid, the water to air, and the air to solid interface. In this case, the solid refers to the surface under consideration. For smooth and homogenous surfaces, the contact angle at the three phase line (Solid, Liquid, and Vapor) is given by Young's equation [34]:

$$cos\theta = (\gamma_{SV} - \gamma_{SL})/\gamma_{LV} \tag{4.1}$$

where θ is the contact angle and γ is the interfacial free energy for the interface denoted by the subscripts (S = Solid, L = Liquid, and V = Vapor). Stated differently, the contact angle is the angle that corresponds to the droplet shape that minimizes the total interfacial free energy. Again, the equation applies for a perfectly smooth surface and neglects the gravitational potential energy of the droplet. However, relative values of experimentally measured contact angles for small droplets can be used to compare the degree of hydrophilicity of a non-ideal surface. The more hydrophilic the surface, the lower the value for γ_{SL} and consequently, the smaller the contact angle θ. It is important to be able to make such a comparison because for wafer bonding, it is desireable to have a hydrophilic surface and it

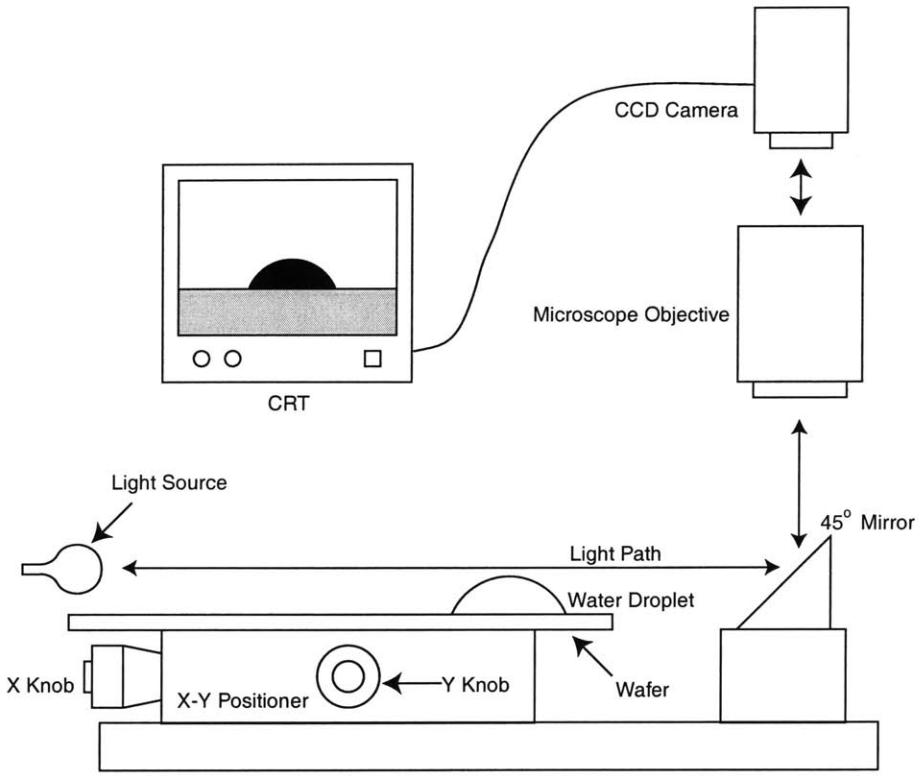


Figure 4-2: Contact angle measurement setup.

is possible that a more hydrophilic surface (i.e. smaller contact angle) results in a stronger bond.

4.1.1 Measurement Setup and Details

In order to determine the contact angle, a simple setup was constructed. The setup consists of an x–y positioner, a 45° mirror, a light source, and a microscope connected to a CCD camera and CRT. A drop of DI water is then transferred from a glass pipet to the wafer surface. The water drop can be used if it is less than 4 mm in diameter. A schematic of the setup is shown in Figure 4-2. The CRT provides a flat surface upon which to make measurements of the water droplet. In practice it is difficult to measure the angle directly with a protractor. It is much easier to measure the height and width to determine a ratio $M = h/w$. Then assuming that the droplet forms a section of a perfect sphere, the contact

Treatment	Chemistry	Duration (min)	Contact Angle θ
Piranha	H_2SO_4:H_2O_2 3:1	10	3
		1	3
Nanostrip	Not Available	10	6.1
		1	6.3
DI water	H_20	5	11
Hydrofluoric Acid	40:1 H_20:HF	0.5	25
SC1 of RCA	H_20:H_2O_2:NH_4OH 5:1:1	5	3.1
SC2 of RCA	H_20:H_2O_2:HCL 6:1:1	5	2.3
SC1 then SC2	Same as Above	5 then 5	3
No Treatment	N/A	N/A	28

Table 4.1: Contact anlges for various common chemical cleaning treatments

angle may be calculated using the following formula [33]:

$$\theta = cos^{-1}(\frac{0.25 - M^2}{0.25 + M^2}) \tag{4.2}$$

The point of this experiment was to determine which of several chemical treatments could be used as both a final pre-bond clean and surface activation treatment. Wafer pieces were prepared from a wafer upon which 3μm of PECVD oxide were deposited. The pieces were then each exposed to different common cleaning chemical treatments to determine which created the most hydrophilic surface. It should be mentioned that each treatment was followed by a short rinse in DI water except for the HF dip. For the purposes of creating a hydrophilic surface, a DI water rinse does not signicantly change the surface chemistry since by definition, the hydrophilic surface already contains adsorbed water molecules. However, an HF dip, which has been included for the sake of comparison, creates a hydrophobic surface and a subsequent DI rinse will alter the surface making it less hydrophobic or more hydrophilic. The chemical treatments are compared in Table 4.1. The original concern and motivation for performing this experiment was that there may be a large difference in the contact angle from one treatment to the next. However, it is clear from the table that any of the treatments, other than the HF dip and DI water alone are sufficient to create a hydrophilic surface. This means that the second criterion for selecting a chemical treatment, the ability of the treatment to sufficiently clean the surface becomes the important factor. It is well known in semiconductor processing that the most thorough clean is a combination of SC1 followed by SC2, more commonly known as an RCA clean. The SC1 helps remove

organic species while the SC2 treatment removes ionic species [7]. In practice, however, not all of these cleans are compatible with GaAs or even silicon wafers that contain buried metal. It was found that for the simulation wafers, the aluminum could be etched through the covering PECVD oxide. Apparently the oxide is not dense enough too block the acids from etching the aluminum. Consequently, while the RCA clean could be used for the silicon wafers containing just the PECVD oxide, the simulation wafers and IBM wafers could only be exposed to a 3 minute piranha clean. The situation is even more difficult for the GaAs wafers. GaAs is etched by most acids. Consequently, only a short (1 min) SC2 clean was used for the these wafers.

4.2 Surface Energy Measurement

In order to obtain quantitative results for wafer bonding such as the bond strength, the surface energy may be approximated by the crack-opening method, first described by Maszara *et al* and based on earlier work by Metsik [29]. A higher surface energy means a stronger bond. The crack-opening method involves the insertion of the tip of a razor blade (or other sharp narrow object) between the bonded wafers in order to partially separate or debond the wafers. Using an IR camera, the length of the crack can be measured (Figure 4-3). From the Young's Modulus of the wafers, and the geometry of the wafers and the crack, the surface energy of the bonded interface may be determined with the following formula:

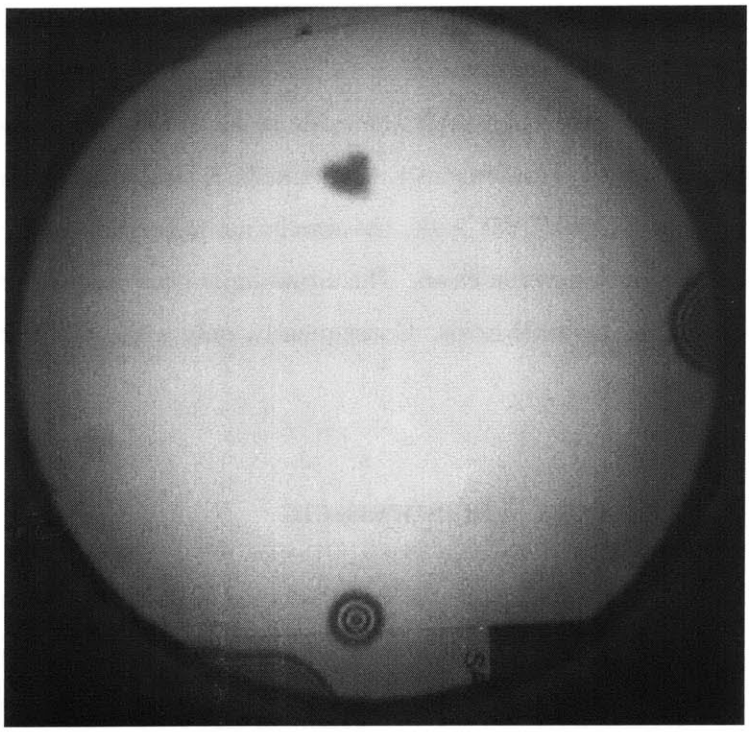
$$\gamma = \frac{3Ed^3y^2}{32L^4} \tag{4.3}$$

where E is Young's modulus for the wafer material, d is the wafer thickness, y is the thickness of the blade, and L is the length of the crack. This is illustrated in Figure 4-4. If the two wafers are composed of different materials and have different thicknesses, as is the case for the bonding of the IBM wafers to the GaAs wafers, a modified formula is used. The formula for a single bent wafer, in which one wafer is held flat to a vacuum chuck and only the other wafer is allowed to bend is [27]

$$\gamma = \frac{3Ed^3y^2}{16L^4} \tag{4.4}$$

where the symbols apply as before and d and E refer to the bent wafer thickness and

(a)



(b)

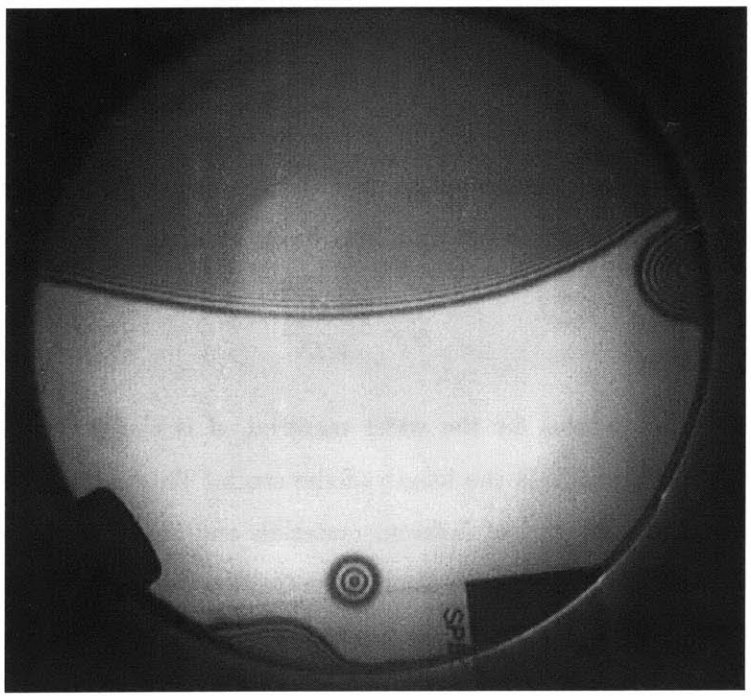


Figure 4-3: (a) IR image of bonded wafer pair and (b) same pair with razor blade inserted. For this 10cm wafer, the crack (dark region) length is ~4.2cm corresponding to a surface energy of $2mJ/m^2$.

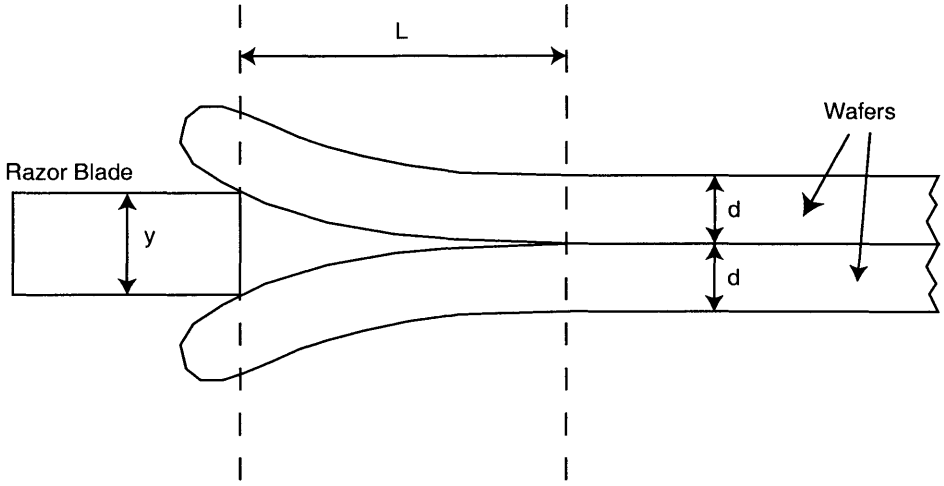


Figure 4-4: Crack opening method: relevant parameters.

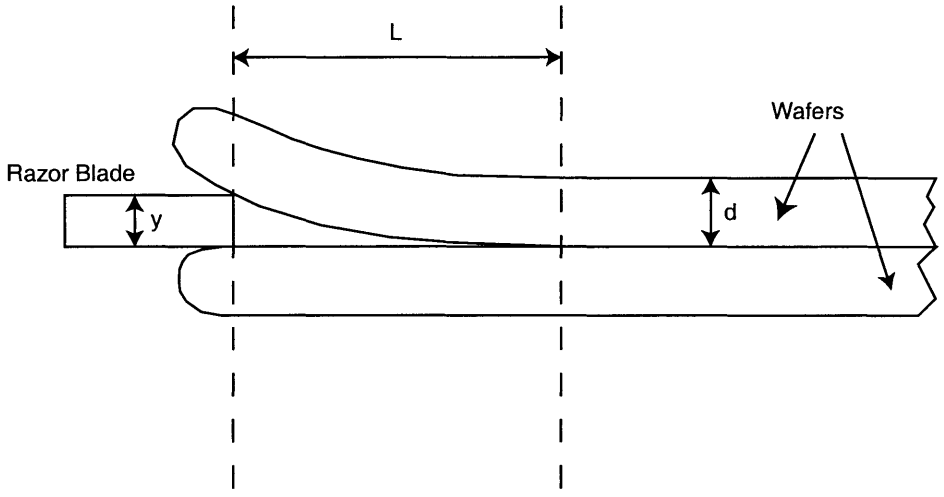


Figure 4-5: Crack opening method for only one wafer bent.

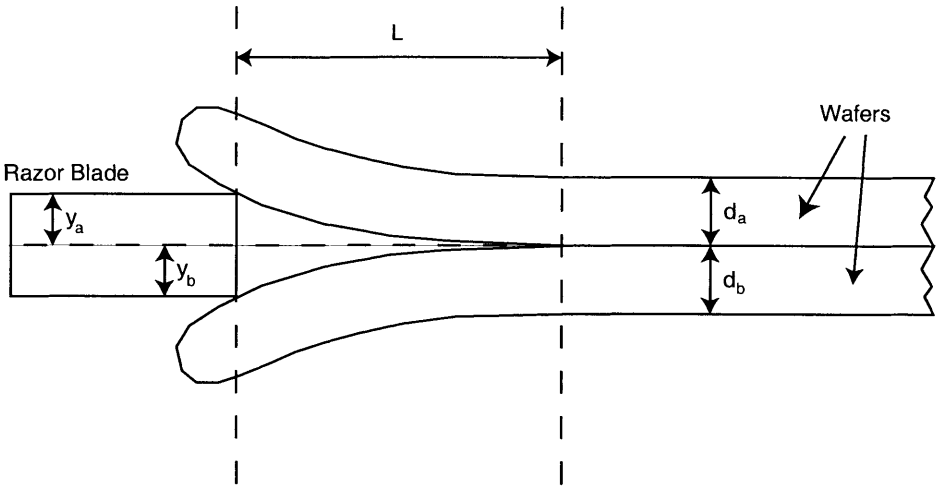


Figure 4-6: Crack opening method: wafers with different properties.

Young's modulus. See Figure 4-5. The case of bending for both wafers may then be broken down into two single-bent wafers. The only difference is that each wafer does not bend one half the width of the inserted blade, but rather some fraction of the blade's width (Figure 4-6). We know that the total surface energy is the sum of the two single-bend energies:

$$\gamma = \gamma_a + \gamma_b \tag{4.5}$$

where

$$\gamma_a = \frac{3E_a d_a^3 y_a^2}{16L^4} \tag{4.6}$$

$$\gamma_b = \frac{3E_b d_b^2 y_b^2}{16L^4} \tag{4.7}$$

where γ_a refers to the energy determined from bending wafer a a distance y_a, and γ_b refers to the energy determined from bending wafer b a distance y_b. But the force applied to the blade by the top wafer must equal the force applied by the bottom wafer. Given that the same bonded area and crack length applies for each wafer, the surface energies must be equal:

$$\gamma_a = \gamma_b \tag{4.8}$$

$$\frac{3E_a d_a^3 y_a^2}{16L^4} = \frac{3E_b d_b^3 y_b^2}{16L^4} \tag{4.9}$$

Wafer	Young's Modulus	Thickness
Standard 4" Si	165 GPa	525μm
IBM SOI	165 GPa	700μm
GaAs	85.5 GPa	500μm

Table 4.2: Parameters required for wafer bond surface energy calculations.

Solving for y_a gives

$$y_a = \sqrt{\frac{E_b d_b^3}{E_a {d_a}^3}}\ y_b \tag{4.10}$$

By definition

$$y = y_a + y_b \tag{4.11}$$

Combining equations 4.11 and 4.10 gives

$$y = y_b \left(1 + \sqrt{\frac{E_b d_b^3}{E_a {d_a}^3}}\right) \tag{4.12}$$

Rearranging gives

$$y_b = \frac{y}{1 + \sqrt{\frac{E_b d_b^3}{E_a {d_a}^3}}} \tag{4.13}$$

Combining equations 4.5 and 4.8 gives

$$\gamma = 2\gamma_b = 2\gamma_a \tag{4.14}$$

Combining equations 4.7, 4.13, and 4.14 gives

$$\gamma = 2\gamma_b = \frac{6E_b d_b^3 \left(\frac{y}{1+\sqrt{E_b d_b^3 / E_a {d_a}^3}}\right)^2}{16L^4} \tag{4.15}$$

Equation 4.15 is an equation for the surface energy that may now be used for the normal crack opening method in which both wafers are free to bend. The relevant parameters required for the case of Si-GaAs bonding for both the simulation wafers and the IBM wafers is given in Table 4.2.

4.3 Procedure and Results

4.3.1 Surface Preparation and Bonding

Immediately prior to bonding, the wafers are cleaned using the appropriate clean discussed earlier. The wafers are then immediately transferred to the wafer bonder in a clean box devoted solely to bonding. The wafer bonding was performed on an Electronic Visions EV450 and AB1-PV Bonder. The bonder performs two primary functions. It keeps the wafers separated at the edges until contact is initiated at the center of the two wafers. The bonder also allows the application of force by applying pressure via a pressure chamber. The wafers are then removed from the bonder and are viewed with an IR camera. The IR camera shows whether or not the wafers have bonded. If there are any voids in the bond, they can be seen through the IR camera. A typical picture of bonded wafers was shown in Figure 4-3(b) for a Si-Si direct hydrophilic bonded wafer pair. The voids are obviously not desireable. In most cases, the voids are due to the presence of hydrocarbon contaminants on the bonding surface of the wafers [28]. It is therefore important to minimize the chances for contamination between the final pre-bond clean and the initial wafer contact. A potential source of hydrocarbons is the Teflon wafer carriers used to carry the wafers. Although not used for this work, it is believed [28] that quartz wafer carriers may minimize void formation. In addition to voids, it is common to see wafers bonded in the center only with no bonding at the edges (Figure 4-7). This is caused by bonding two convex wafers. This was often seen for bonding silicon wafers with PECVD oxide at the interface.

4.3.2 Low Temperature Bond Anneal

As discussed in Chapter 2, the wafer bond may be strengthened with an anneal following the room temperature bond. The target temperature at which the surface energy of Si–Si direct hydrophilic bonded wafers saturates is 150°C. It is less likely that there is such a drastic saturation value for the case of PECVD oxide at the bond interface. Nonetheless, this is a safe temperature for the Si–GaAs wafer bond. At temperatures above 200°C, there is a risk of breakage or debonding. For the test cases in which the bonding occured between two silicon wafers, the anneal was a straightforward step and was carried out in a furnace. For Si–GaAs anneals, the temperature was ramped slowly (10°C/hr) from R.T. to 150°C on a hot plate. The temperature was then held at 150°C for 50 hours before being slowly

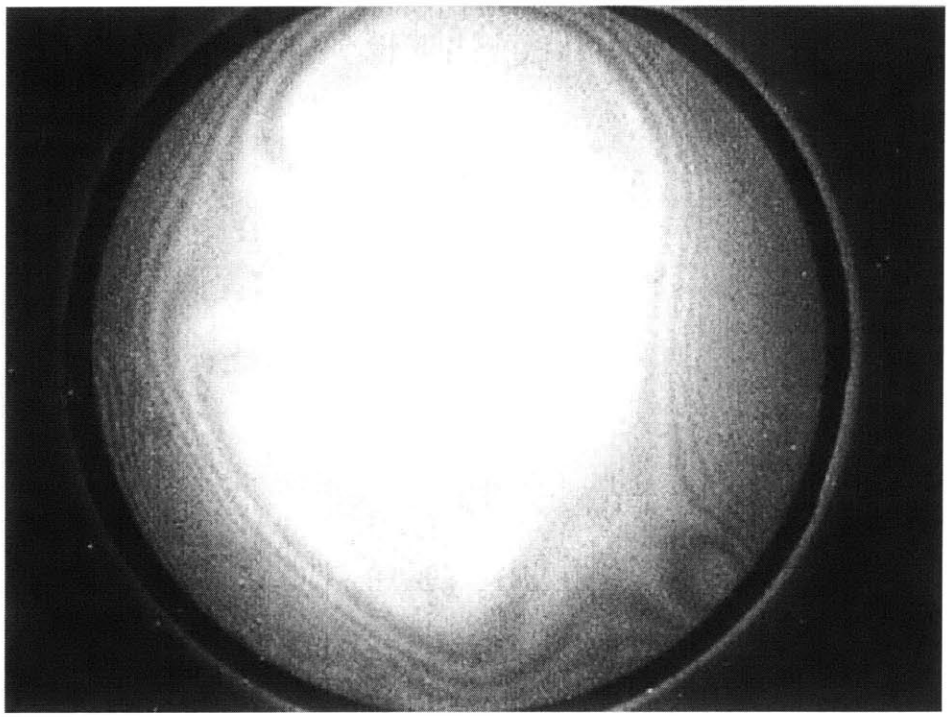


Figure 4-7: Convex bowed wafers bonded only in the middle.

ramped back down to R.T. A long anneal is required to insure the full fracturing of siloxane bonds on each wafer surface and the subsequent formation of siloxane bonds across the bond interface. This phenomena of gradual surface energy increase over long anneals under 150°C was studied for Si–Si direct wafer bonding [27]. It was found that the bond surface energy increased by as much as a factor of three after an anneal of 50 hours and completely saturated after 100 hours.

4.3.3 Bonding Results

In order to obtain successful bonding of GaAs to the IBM wafers or the simulation wafers, it was necessary to first verify the bonding procedure with "easier" combinations of wafers. In order to verify the bonding with PECVD oxide on the surface of both wafers, silicon wafers containing just PECVD oxide were bonded together. This eliminated many of the factors that made the bonding of the IBM wafers to the GaAs wafers so difficult, such as cleaning difficulties, increased IBM wafer thickness, and thermal coefficient mismatch. It also allowed for a determination of the "best case" bond strength for bonding fully processed

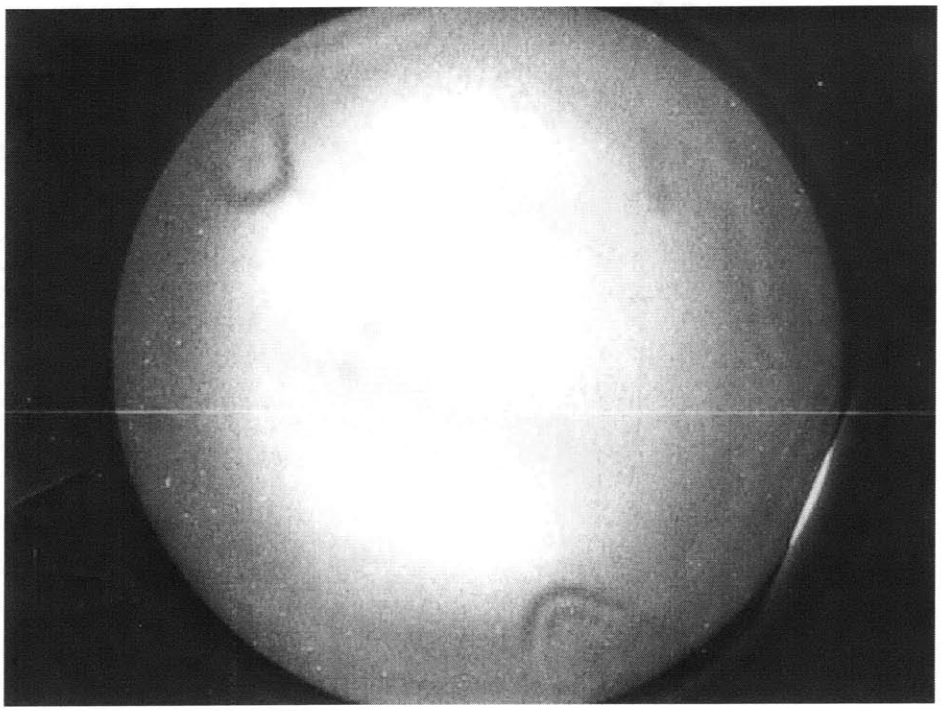


Figure 4-8: Successful Si–Si bonded wafers with PECVD oxide at the interface.

Si CMOS wafers to GaAs wafers. The procedure used for this bond is given in Appendix A. Figure 4-8 shows the bonded pair. Notice the very few voids and the good edge bonding. This bond was annealed at 450°C which is the maximum temperature to which fully front and back-end processed wafers can be exposed.

The next step was to bond GaAs to Si, again with the Si wafers containing just PECVD oxide. The pair bonded successfully. This is a very important result. It demonstrates that the issue of differing thermal expansion coefficients may be avoided because of the success of this low temperature bonding procedure. It means that low temperature PECVD oxide, although initially not suitable for bonding, can be planarized sufficiently for wafer bonding. This Si–GaAs pair is shown in Figure 4-9. The voids are minimal, but the edges are not completely bonded. Again, this is a result of wafer bowing. The next step was to bond the simulation wafers containing metallization to GaAs. This bond was also successful and is shown in Figure 4-10. In addition to the thermal expansion coefficient mismatch, and a more difficult CMP step, the difficulties with this bond are that both the Si wafer and the GaAs wafer can only withstand short pre-bond cleans. The signifigance of this successful

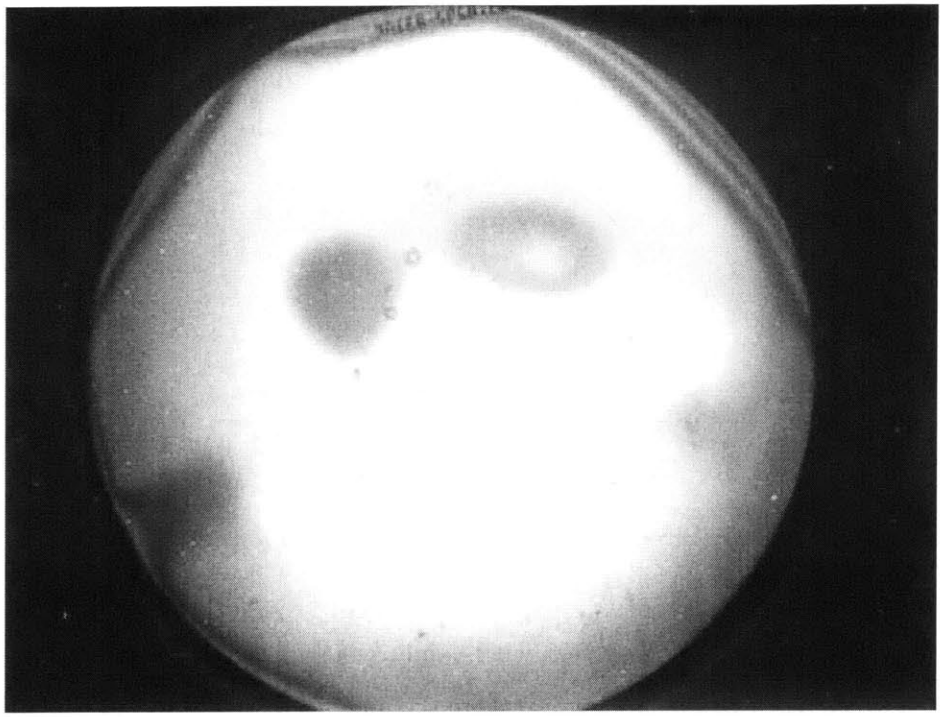


Figure 4-9: Successful Si–GaAs bonded wafers with PECVD oxide at the interface.

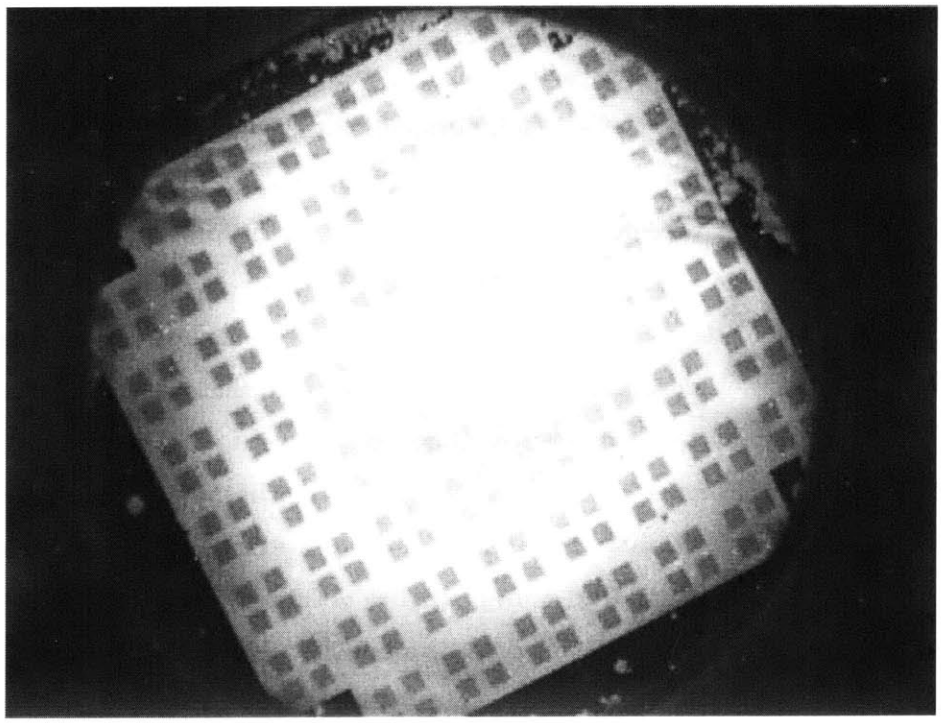


Figure 4-10: Successful metal containing Si–GaAs bonded wafers.

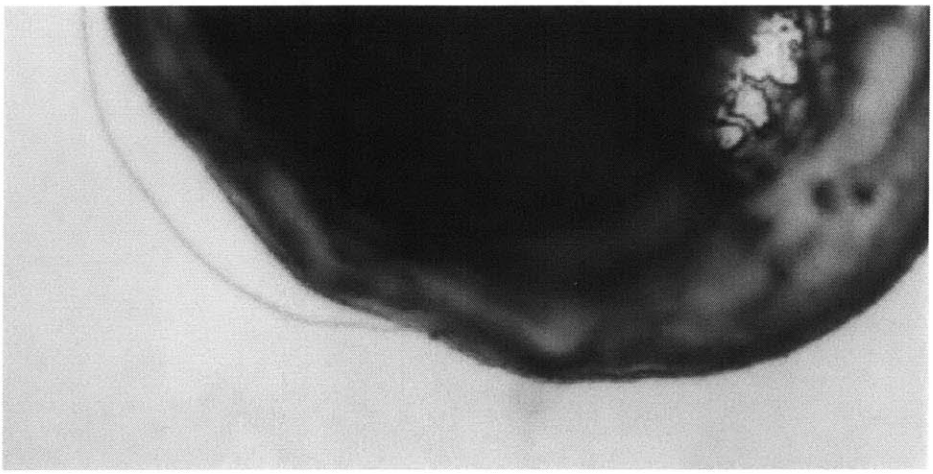


Figure 4-11: Piece of silicon embedded in oxide of wafer surface.

bond is that the complications present with bonding metallized Si wafers to GaAs wafers have been overcome with this low temperature bonding process. This is an essential result for this project and is the desired result for the stage of the work presented by this thesis.

Finally, the thick IBM wafers were bonded to GaAs. This bond was not successful. Upon closer examination of the IBM wafers, several large bumps were found on each wafer (Figure 4-11. Some of the bumps were as high as 60μm above the wafer surface. The bumps are believed to be pieces of silicon that flaked off the edges (see Figure 4-12) of the wafer during the laser cutting process. The pieces would have been very hot, hot enough to become embedded in the oxide surface. In an attempt to fix this problem, the upper oxide layers were removed from one IBM wafer down to the metal layers. It was hoped that the bumps were not lodged deeply into the surface and that they may be removed when the oxide was etched away. Unfortunately, they were deep enough that the etch had no effect. This is a problem that must be addressed in future runs in order to obtain a successful bond using the IBM wafers. However, as stated earlier, the bonding of the "simulation" wafers to GaAs demonstrates the important result that back-end processed wafers can be bonded to GaAs. And it implies that if the IBM wafers were free of the bumps, they could be bonded to GaAs using the same process. Table 4.3 lists all of the relevant bonding combinations and their respective results.

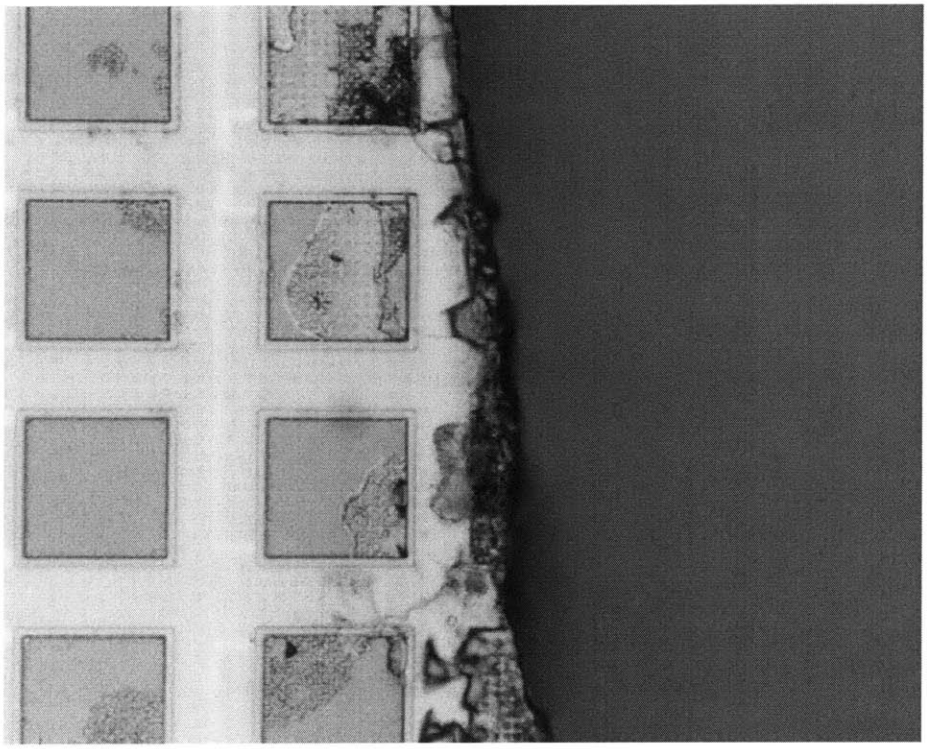


Figure 4-12: Laser cut edge of IBM wafer. Likely source of bumps on the wafer surface.

Wafer 1	Wafer 2	Anneal Temperature	Bond Strength
Si w/ PECVD	Si w/ PECVD	450°C	200 mJ/m^2
Bare Si	Si w/ PECVD	450°C	20 mJ/m^2
Bare Si	Bare Si	Room Temp.	20 mJ/m^2
Si w/ PECVD	Si w/ PECVD	Room Temp.	6.9 mJ/m^2
Si w/ PECVD	GaAs	150°C	5 mJ/m^2
Si w/ PECVD covered Al	GaAs	150°C	4.8 mJ/m^2
IBM wafer	GaAs	N/A	0 (no bond)

Table 4.3: Wafer Bonding Results

Chapter 5

Spin-On Glass and Indirect Wafer Bonding

The previous chapters deal with direct or nearly direct wafer bonding. Typically, direct wafer bonding refers to the bonding of two completely bare wafers without the use of an intermediate layer. The process explained in the previous chapters is direct in that no bonding agent or layer is applied between the two PECVD oxide layers. While the oxide layer was deposited to act as the bonding surface for the processed Si CMOS wafer, it basically serves as the planarizing layer and wouldn't be needed if the wafers were flat to begin with. Because direct wafer bonding requires tight control over the planarity, cleanliness, and surface chemistry of the wafers for bonding, it can be a difficult and involved process. A potentially less complex alternative to direct wafer bonding is indirect wafer bonding. Indirect wafer bonding involves the use of an intermediate layer which acts as a bonding agent.

5.1 Spin-On Glass

Spin-On Glass (SOG) is a silicon and oxygen-containing compound that is spun onto a wafer in solution. In its initial form, the SOG chemistry may include organic groups such as methyl. Upon exposure to relatively low temperatures (150–200°C), the SOG undergoes condensation polymerization to form plastic-like layers. At slightly higher temperatures (400–500°C), the SOG undergoes pyrolysis resulting in an inorganic glass with silicon dioxide-like characteristics [5]. SOG is used most commonly as part of the inter-metal di-

electric stack. Because it is applied in the liquid state and is then cured, SOG is useful for planarizing without the need for CMP. When used in conjunction with CMP, high degrees of planarization may be obtained.

5.2 Bonding with SOG

SOG is in many ways well suited for use in the wafer bonding of processed Si to GaAs. The entire process, from spin-on to pyrolysis, occurs at low temperatures as required for this particular Si–GaAs bond. Also, because the SOG is applied as a liquid, it can flow in and around features present on the IBM wafers. The SOG spin-on process results in film thicknesses on the order of 3000–5000Å. The SOG is therefore capable of flowing and filling steps up to these heights. How well features are filled depends on the specific geometry of the steps and the surface tension of the SOG in its initial state. Finally, the SOG can be used like an adhesive. If two surfaces are coated with SOG and brought together before carrying out the SOG cure (condensation polymerization and pyrolysis), the surfaces will stick together. The SOG may then be cured with the result being a strong permanent bond between the two surfaces. It is this adhesive bonding action that was exploited for the purposes of wafer bonding.

5.2.1 SOG Bonding Procedure

The SOG bonding was attempted for Si–Si wafer bonding to test its feasibilty for wafer bonding in general. The SOG used was SOG type 400FA-4000 from Filmtronics. The same Filmtronics SOG was successfully used for bonding GaAs to quartz substrates [16]. Successful attempts have been made less recently to bond Si–Si [36] and Si–Si_3N_4 [35] using SOG. In general, the procedure for bonding with spin-on glass was similar for each of these papers. Usually, only the details of the spin-on procedure and cure times and temperatures were altered as required for the particular SOG used. The same procedure was followed for this work. The SOG (1mL per 4" wafer) was applied to the wafer using a pipet and then spun-on using the recipe found in Appendix B. The curing process which would typically be used for the 400FA-4000 SOG is a hot plate treatment at 180°C, then 250°C and finally the final cure in a furnace at 400°C with N_2 ambient for 30 minutes. After the initial low temperature hot plate treatments, the SOG has a plastic-like nature. At this point, some

of the solvents have been driven off and the condensation-polymerization has begun. It is now that the two wafers are brought together for bonding. At this stage, the film can still be deformed allowing it to fill in and around any microstructures. If the SOG is fully cured at the final temperature, it will be hardened like the PECVD glass in the earlier chapters. This would require CMP to get the film perfectly flat and so there would be no real advantage to using SOG. For the bonding process, SOG was spun onto both wafers. Each wafer was separately cured on a hot plate at 180°C. The wafers were then manually placed together. The bonded pair was cured on a hot plate at 250°C while pressure was manually applied with a quartz plate. The bonded pair was then placed in a furnace for the final 400°C cure. The bond strength was then tested using a razor blade. But the bond was so strong that the wafer actually chipped away rather then bending away. The wafers were separated by carefully slicing around the entire circumference of the bonded pair. The bond was obviously very strong, much stronger than any bond obtained using the conventional direct bonding procedure.

5.2.2 SOG Results: Outgassing Damage

When considering the problem of wafer bonding simply from the mechanical standpoint of sticking two wafers together, it seems like a simple adhesive like an epoxy could be used. This certainly would work for low temperatures, and some epoxies do have good enough dielectric properties. However, unlike SiO_2, they are not fully stable at high temperatures. At elevated temperatures substances such as epoxies begin to outgas. In the case of wafer bonding, the gases have no place to go and result in bubble formation in the epoxy. This is also the case with SOG. During the hot plate and furnace curing process, gaseous products of the polymerization and pyrolyzation reactions escape from the SOG [12]. This places a restriction on the final curing temperature for the separated wafers just prior to bonding. It must be made as high as possible to ensure maximum outgassing, but low enough for the wafers to still bond together. The maximum temperature was found to be about 250°C. However, even at this temperature, there was still enough subsequent outgassing to form significant voids in the SOG. Images of the bubbles in the SOG can be seen in Figure 5-1. When the bonded wafers were split apart, it was clear from the remaining patterns on the two wafers that the SOG had actually cracked apart and not debonded from the Si surface. A closeup of the cracks in the SOG can be seen in Figure 5-2. This again shows the strength

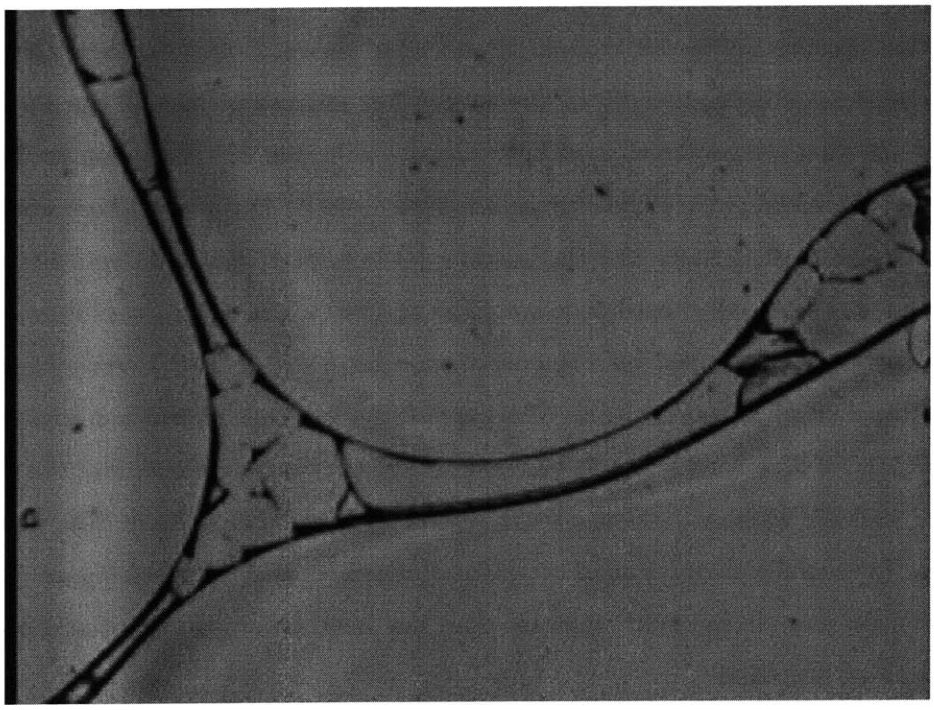


Figure 5-1: Bubbles in the SOG.

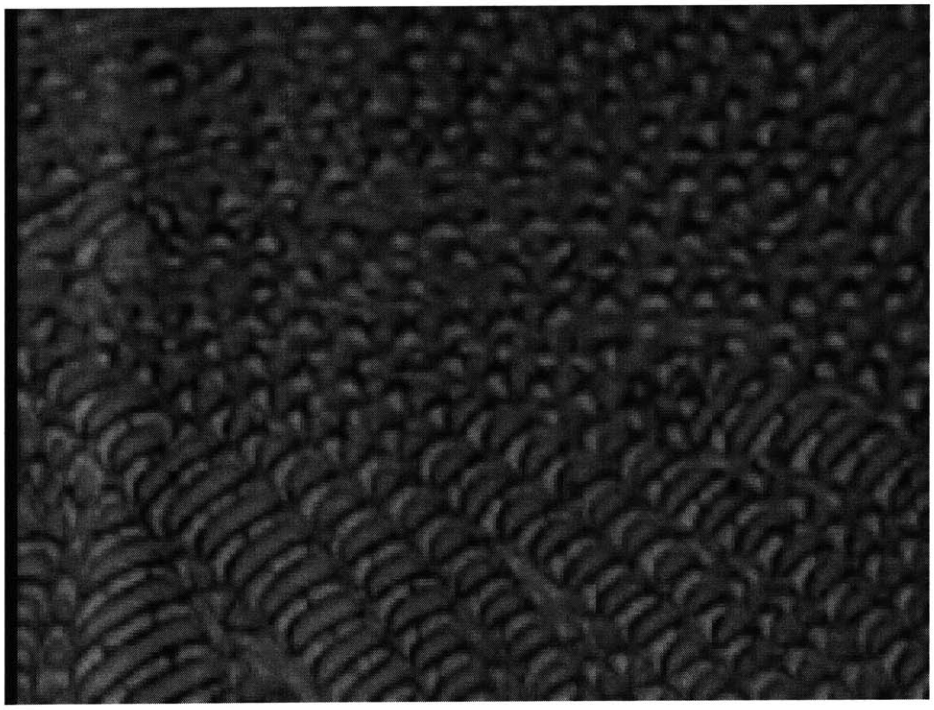


Figure 5-2: Close-Up of Cracked SOG.

of the bond. Unfortunately, the problem of the bubble formation would most likely make the processing of backside contacts made through the bond interface extremely difficult at best. It is likely that the parts of the thinned silicon wafer above the bubbles would crack off.

5.3 SOG Future Work

It is possible that the problem of outgassing could be minimized with either a different SOG or a different curing procedure. In addition, it would be worthwhile to go through the backside thinning and interconnect procedure to see what problems, if any, the bubbles cause. As mentioned earlier, others have had success using SOG for wafer bonding. However, no mention was made of this outgassing problem. Given that a very similar procedure was followed with the same SOG from Filmtronics, it is likely that this problem existed in those cases as well. It is important for this work to realize that the wafer bond must do more than simply provide a mechanical sticking force since electrical connections must eventually be made through the bond interface.

Chapter 6

Conclusion

6.1 Summary of Accomplishments

While the ultimate goal of bonding fully processed IBM wafers to GaAs wafers was not achieved, several key accomplishments demonstrate the feasibility of such a bond. First, the bonding of two wafers both containing PECVD oxide on the surface was demonstrated. The additional fact that this was caried out entirely below 450°C is important. If there were no temperature constraints, both the oxide densification and wafer bond anneal would have been carried out at much higher temperatures ($\sim$ 1000°C). While this would have most likely improved the bond strength and uniformity, it was shown to be unnecessary. Second, the bonding of Si–GaAs was demonstrated with PECVD oxide at the interface. Anneals as high as 150°C were reached resulting in a relatively strong bond. Finally, the successful bonding of the "simulation" Si–GaAs shows that beck-end processed wafers can be planarized sufficiently and bonded to GaAs.

6.2 Pitfalls and Potential Improvements

There are a number of key problems that led to the unsuccessful bonding of the IBM wafers to GaAs. The root of the problem is that the IBM wafers were originally 8" wafers and only 4" wafers can be processed in MTL. This problem is fundamentally linked to the point of this research. If not clear by now, the point was to demonstrate that fully processed commercial SOI Si CMOS wafers could be bonded to GaAs without changing any of the well-developed Si processsing techniques. In other words, the wafers could be taken as is at

the end of the standard processing and then planarized and bonded to GaAs. The key here is that this is an optoelectronic integration process that does not require any overhauls to commercial processes already in place. But to show this requires the use of actual wafers from a recent SOI process. However, no current commercial SOI processes are being run on 4" wafers. So the laser cutting was the only solution. Now that the flaking problem has been identified and can be addressed, the laser cutting should be a good solution. A possible solution is to coat the surface of the wafers with a thick protective layer of for instance, photoresist, that could be removed post laser cutting. This layer would act as a barrier, catching any flakes and stopping them from damaging the wafer surface. The additional complication caused by the 8" IBM wafers is that 8" wafers are thicker than 4" wafers, which makes the wafer bonding more difficult. It is possible that this problem could be solved with backside grinding to thin the wafer from a thickness of 700μm to the 4" standard 500μm thickness.

Another problem that should be addressed is the wafer bowing. A possible solution to the bowing caused by stressed PECVD oxide is to deposit oxide on both sides of the wafer. This stress on one side of the wafer would cancel out the stress on the other side. Also, the use of prime grade instead of test grade silicon wafers would insure less initial bowing.

A problem that was partially dealt with is the problem of post CMP cleaning in which leftover slurry particles are removed from the wafer surface. Etching with HF is an unfortunate solution because it increases the roughness of the oxide surface. If the particles could be removed without any etching, the real power of the CMP step would be much more apparent. There are also slurries that are specifically designed for minimizing surface roughness. It is very likely that the use of such slurry would result in better bonding.

Finally, both the GaAs and metallized silicon wafers were not passivated well enough to allow for long pre-bond cleans. It is likely that longer more aggressive cleans would have resulted in stronger bonds. This problem could be solved by depositing thick nitride on the backside of the GaAs wafers and over the metal layers on the silicon wafers.

6.3 Future Work

In Chapter 1, this work was placed in the context of a much larger project to achieve a fully integrated VLSI OEIC with wafer bonding. Some diagrams were shown that illustrate

the final cross section of such a system. However, there are still many steps between the successful bonding achieved in this work and the diagrams from Chapter 1.

6.3.1 Bond Strength and Backside Processing

This first step is to verify that the wafer bond is strong enough to withstand the processing that follows the bonding step. It must be able to withstand the backside thinning, metal deposition, photolithographic, and etching processes that would be involved in making the backside interconnects. Eventually, the bonded pair would be exposed to wafer cutting in a die saw as one of the final steps. In general, it would be helpful to identify a minimum bond strength required for the above processing steps. In addition to the question of bond strength, the problem of voids must be examined. The voids must be reduced or eliminated if possible. If they cannot be eliminated, their effects on the subsequent processing must be studied. It is possible that the voids would just be a yield problem in which only die covering areas with no voids would be useful.

Although it is becoming more common, the idea of processing on both sides of a wafer is by no means standard. It will be important to examine the quality of the buried oxide layer to see if it will have any effect on the backside process. It is expected that the best results would be obtained for SOI wafers in which the BOX (Buried OXide) layer is grown rather than implanted, as is the case with SIMOX wafers.

6.3.2 Bonding with OEIC's

Unlike Si CMOS procesing, which is a very planar process, the processing of optoelectronic devices involves tall devices which may be several microns in height. This work dealt with surface variations on the order of 0.1μm. The jump to several microns will be difficult and will require a well developed planarization process. It is possible that SOG will play a role in this task. Also, some consideration must be made of how to place or include the optical I/O paths. This was shown as a deep etch in the diagrams in Chapter 1, but this may need to be further developed. Finally, optoelectonic and electronic devices heat up during operation. This may also have an effect on the bond interface and the vias across the interface. It is clear that this project is not yet complete, but this work has demonstrated an important step in the process.

Appendix A

Detailed Processing Flow

As mentioned in the introductory chapter, the work for this thesis was carried out mostly in MTL (the Microsystems Technology Laboratory) which is divided into 3 separate labs. In particular, two of these labs, TRL (the Technology Research Laboratory) and ICL (the Integrated Circuits Laboratory) were used for much of the processing steps. The AFM (Atomic Force Microscope) measurements were made in the CMSE SEFs (Center for Materials Science Engineering Shared Experimental Facilities). The following tables provide the step-by-step processing flow that gave the best results for wafer bonding. Included in the tables are the basic purpose for the step, the type of machine used, and the facility where the step was performed. In all cases, the processes described below for the IBM wafers were also applied for dummy wafers (Si wafers with only the PECVD oxide and the simulation wafers described in Chapter 3). For completeness, the process described for the GaAs wafers includes processing not performed by the author (denoted with a *). Finally, the bonding and post-bonding process is included which applies in general to the low temperature bonding of any two wafers.

IBM–GaAs Wafer Bond			
GaAs Wafer Preparation			
Processing Step	Purpose	Machine Used	Facility
Backside SiN_x	Provides barrier against etching of GaAs during cleaning treatments	PlasmaQuest PECVD	TRL
15 sec. 50:1 HF:H_2O	Removal of Slurry Particles	Acid Hood	TRL
Solvent Clean	Removal of organic contaminants	Acid Hood	TRL
Nanostrip Dip	PECVD Oxide surface activation	Acid Hood	TRL

Table A.1: Process for preparing GaAs wafers for bonding

IBM–GaAs Wafer Bond			
IBM Wafer Preparation			
Processing Step	Purpose	Machine Used	Facility
10 min. Nanostrip	Aluminum Safe Post Laser Cut Clean	Acid Hood	TRL
Global Surface Profiling	Identification of prominent features and determination of necessary oxide thickness	Tencor P10	ICL
PECVD Oxide Deposition	Acts as sacrificial planarizing layer and bonding surface	Novellus Concept One	ICL
Global Surface Profiling	Identification of any changes in features due to oxide deposition	Tencor P10	ICL
Oxide Anneal	Permit outgassing of oxide prior to bonding	Diffusion Tube	TRL
Chemical Mechanical Planarization	Remove oxide microroughness and topography caused by underlying metal	Strasbaugh 6EG	ICL
30 sec 50:1 HF:H_2O	Slurry particle removal	Acid Hood	TRL
3 min. Piranha	Oxide Surface Activation*	Acid Hood	TRL

Table A.2: Process for preparing IBM (or Si) wafers for bonding (* RCA clean instead of piranha for Si wafers with PECVD oxide only).

Wafer Bonding and Post Bond Process			
GaAs Wafer Preparation			
Processing Step	Purpose	Machine Used	Facility
Wafer Bond	Initiate Room Temperature Bond	Electronic Visions EV450 and AB1-PV Bonder	TRL
Take IR Image	Verify bond success	IR Lamp and IR Camera	TRL
Anneal Bonded Pair	Strengthen room temperature bond (siloxane bond formation)	Diffusion Tube	TRL
KOH Treatment*	Backside thin the Si wafer substrate	Acid Hood	ICL

Table A.3: Process for bonding and post bond processing (* Never actually did because of failed bond for IBM wafers.

SOG Wafer Bonding Process			
Processing Step	Purpose	Machine Used	Facility
Deposit 1mL SOG to both wafers	Applied for spin-on	Pipet	TRL
Spin-On	Evenly apply SOG	Spinner	TRL
Low temp hot plate	Begin cure and promote outgassing	Hot plate	TRL
Bond Wafers w/ manual pressure	Initiate Room Temperature Bond	Quartz plate and hot plate	TRL
400°C furnace treatment	Final cure of SOG and bond	Diffusion Tube	TRL

Table A.4: Process for bonding with SOG

Appendix B

Process Recipes

The following tables give the recipes and/or chemistry used to perform the various processing steps described in Appendix A.

The CMP parameters in the following table apply for a Strasbaugh 6EG model. Based on experience with this CMP, it is likely that the following recipe would only give the same results if one were to use this particular 6EG. The following is at least a good starting point. For short polishes under one minute, it is likely that this would be sufficient. Longer times may require more tweaking to obtain good uniformity.

Chemical Mechanical Polishing			
Parameter	Step 1	Step 2	Step 3
Process Time (sec)	10	x*	120
Polish Press. (psi)	12	15	17
Polish Press. Ramp (sec)	2	5	5
Ring Press. (psi)	0	0	0
Back Press. Zone 1 (psi)	0	0	0
Back Press. Zone 2 (psi)	0	5	5
Back Press. Ramp (sec)	1	5	5
Spindle Speed CCW (rpm)	30	75	75
Table Speed CCW (rpm)	15	15	15
Slurry (mL/min)	150	150	150

Table B.1: CMP Recipe (* polishing rate $\sim$ 3300Å/min)

PECVD Oxide Deposition	
Temperature (°C)	400
Pressure (Torr)	2.7

Table B.2: PECVD Chamber Parameters

Wafer Bonding	
Action	Value
Pump On	1 mbar
Pump Off	N/A
Purge On	N_2
Wait	1 min
Purge Off	N/A
Pump On	$5 \cdot 10^{-3}$ mbar
Electrode Down	150
Flags Out	N/A
Electrode Down	4000
Wait	2 min
Electrode Up	N/A
Vent On	N/A
Wait	2 min
Vent Off	N/A

Table B.3: Bonding Recipe

Pre-Bond Clean for Si Wafers with PECVD Oxide Only		
Chemistry	Temp (°C)	Time
SC1 H_2O:H_2O_2:NH_4OH 5:1:1	75	10 min
H_2O:HF 50:1	RT	30 sec
SC2 H_2O:H_2O_2:HCl 6:1:1	75	15 min

Table B.4: Pre-Bond Clean Recipe for Si Wafers

Pre-Bond Clean for IBM wafers		
Chemistry	Temp (°C)	Time
H_2O:HF 50:1	RT	30 sec
Piranha H_2SO_4:H_2O_2 3:1	Exothermic ($\sim$ 80)	3 min

Table B.5: Pre-Bond Clean Recipe for IBM and simulation Wafers

Pre-Bond Clean for GaAs wafers		
Chemistry	Temp (°C)	Time
H_2O:HF 50:1	RT	30 sec
SC2 H_2O:H_2O_2:HCl 6:1:1	75	15 min

Table B.6: Pre-Bond Clean Recipe for GaAs Wafers

Oxide Anneal	
Temperature	450°C
Ambient	50% N_2
Time	14 hr

Table B.7: Oxide Anneal Recipe

Si–Si Bond Anneal	
Temperature	450°C
Ambient	50% N_2
Time	12 hr

Table B.8: Si–Si Bond Anneal Recipe

Si–GaAs Bond Anneal	
Peak Hot Plate Temperature	150°C
Ramp Up/Down	10°C/hr
Time at Peak Temp.	50 hrs

Table B.9: Si–GaAs Bond Anneal Recipe

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