

# Design of Class E Resonant Rectifiers for Very High Frequency Power Conversion

by

Juan Antonio Santiago-González

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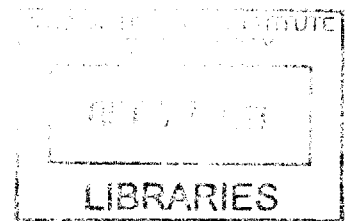
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Signature of Author \_\_\_\_\_  
Department of Electrical Engineering and Computer Science  
August 30, 2013

Certified by \_\_\_\_\_  
David J. Perreault  
Professor of Electrical Engineering and Computer Science  
Thesis Supervisor

Certified by \_\_\_\_\_  
Khurram K. Afridi  
Visiting Associate Professor of Electrical Engineering and Computer Science  
Thesis Supervisor

Accepted by \_\_\_\_\_  
Leslie A. Kolodziejski  
Professor of Electrical Engineering and Computer Science  
Chair, Department Committee on Graduate Students



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Juan Antonio Santiago-González

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Master of Science

## **Abstract**

Resonant rectifiers have important applications in very-high-frequency power conversion systems, including dc-dc converters, wireless power transfer systems, and energy recovery circuits for radio-frequency systems. In many of these applications, it is desirable for the rectifier to appear as a resistor at its ac input port. However, for a given dc output voltage, the input impedance of a resonant rectifier varies in magnitude and phase as output power changes.

In this thesis, a design method is introduced for realizing single-diode “shunt-loaded” resonant rectifiers, or class E rectifiers, that provide near-resistive input impedance over a wide range of output power levels. The proposed methodology is demonstrated experimentally for 10:1 and 2:1 power range ratios at 30 MHz input frequency. Some design limitations are found and explained. Additionally, the performance of Schottky diodes in very high frequency (VHF) rectifiers is explored. It has been found that diodes have increased losses when switched at VHF and this phenomenon varies by manufacturer and device specifications. A study of diodes in Class E rectifiers is conducted to assess their performance in VHF rectification. Some good diodes are identified for VHF operation, including both commercial Si and SiC Schottky diodes and experimental GaN diodes. The foundations are laid for developing a library of diodes useful for this application.

The resonant rectifier design methodology presented in this thesis uses a graphical approach based on normalized design curves. It enables a fast design with only a small amount of calculations needed and yields good accuracy in the final circuit. It is hoped that this design approach and the insights available from the design curves will prove to be useful in designing resonant rectifiers in applications that require resistive rectifier loads.

Thesis Supervisor: David J. Perreault

Title: Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Khurram K. Afridi

Title: Visiting Associate Professor of Electrical Engineering and Computer Science

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## Chapter 1: Introduction

Power conversion systems are often the bottleneck in the miniaturization of electronic devices, such as laptop computers and smart phones. The size of power conversion systems is generally dominated by the size of the passive energy-storage components: inductors and capacitors, which store and release energy during each switching cycle [1,2,3]. The size of the passive energy-storage components is a function of how much energy is stored in them, which for a given level of output power is a function of the switching frequency with which energy is processed. High frequency operation of a circuit leads to energy storage components storing less energy per cycle, which in turn leads to smaller values of capacitance and inductance and thus smaller component size. Hence, to decrease size and increase power density, the power conversion circuits must operate at high frequencies. Another advantage of high-frequency operation is that air core inductors can be used if the switching frequency is high enough, thus eliminating magnetic core losses.

The limitation on increasing switching frequency comes from the increase in frequency-dependent losses, such as transistor switching losses. The switching losses can be reduced by implementing soft-switching techniques such as zero voltage switching (ZVS) [4,5], in which the switch voltage is held close to zero during switch transitions. The power conversion circuit has to be specially designed to operate efficiently under high frequency switching (e.g., see [3] and references therein). Resonant converters readily operate under ZVS conditions and high frequency leading to high efficiency and power density. Resonant power converters [4-7] are circuits that process power in a sinusoidal or quasi-sinusoidal form. Resonant dc-dc converters typically consist of an inverter stage, a transformation stage and a rectification stage, as shown in Fig. 1. Resonant rectification is the main focus of this thesis.

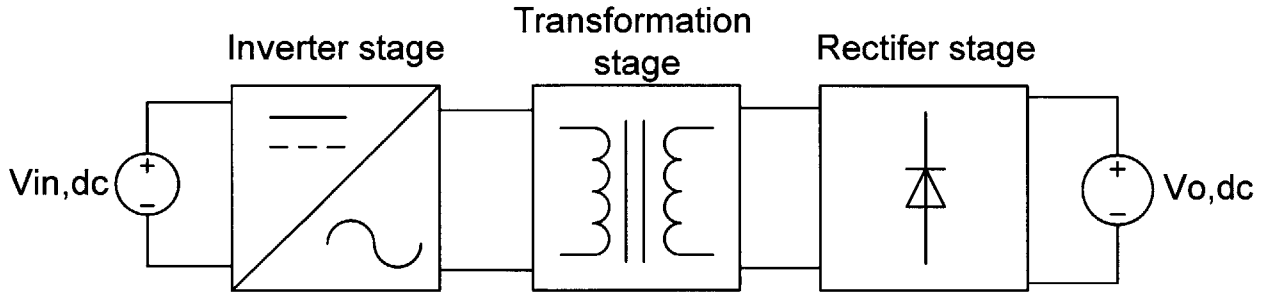


Figure 1.1. Typical architecture of a resonant dc-dc converter.

## 1.1 Motivation

Resonant rectifiers have important applications in power conversion systems operating at frequencies above 10 MHz. Applications for these circuits include very-high-frequency dc-dc converters [4,5,7-12], wireless power transfer systems [8], and energy recovery circuits for radio-frequency systems [9,10]. In many of these applications, it is desirable for the rectifier to appear as a resistive load at its ac input port. For example, in some very-high-frequency dc-dc converters, proper operation of the inverter portion of the circuit can depend upon maintaining resistive (but possibly variable) loading in the rectifier stage. In still other applications it is desired to have an input impedance that is resistive and approximately constant across operating conditions [9,10]; this can be achieved by combining a set of resonant rectifiers having variable resistive input impedances with a resistance compression network [9,11,12]. In all these systems, however, it is desirable to maintain resistive input impedance of the rectifier as the operating power varies.

Resonant rectifiers have been explored in a variety of contexts [13-26]. The traditional design of a class E rectifier, or shunt-loaded resonant rectifier, utilizes a (large) choke inductor at its output and does not provide near-resistive input impedance [7,13]. This thesis introduces a design method for realizing class E rectifiers that provide near-resistive input impedance over a wide range of output power levels. The selection of a diode is also critical in very high frequency (VHF) designs (30-300 MHz). The performance of many diodes degrades as switching frequency increases [14], and this phenomenon is also explored in this thesis through evaluation of different commercial and research diodes.

In summary, in realizing resonant dc-dc converters, the resonant rectifier is a very important aspect that has not been explored thoroughly at VHF frequencies. This thesis has two objectives: (i) the design optimization of the class E rectifier for near-resistive input over a wide range of power and (ii) diode performance at VHF in resonant rectifiers.

## 1.2 Past Work

Resonant rectifiers have been investigated in many contexts over the years [4-9,13-30]. In this thesis, we focus on the class E rectifier, or shunt-loaded resonant rectifier. Class E operation first became known through the class E inverter, a high frequency, high efficiency power amplifier requiring only a single switch and achieving ZVS [31]. Subsequently, various works on the class E rectifier were published, including its use in conjunction with the class E inverter to make dc-dc converters (e.g. [7,13,25,26]). The class E rectifier can be thought of as the counterpart of the class E inverter through “bilateral inversion” [32] or “time-reverse duality” [33] as illustrated in [7,13]. Most published works incorporating class E rectifiers have experimental results with circuits operating under 5 MHz of input ac frequency and deliver loads in the tens of watts or less [7,13, 15-23,26] (exceptions to this include [24,25]). Some designs are made specifically to operate under ZVS condition (or low  $\partial v/\partial t$  during turn on) for synchronous rectification [16,18]. Synchronous rectification is the use of an active switching device, such as a MOSFET, to perform the rectification in place of a diode. This provides control over the duty ratio and increases efficiency of the rectifier (lower forward voltage drop) but adds complexity and gating losses.

The modeling and experimental realization of most rectifiers found in the literature involve a resistive load [13, 15-17, 21-23] and a choke inductor at the output for low current ripple [7,13]. Input impedance of the rectifier is analyzed and simulated but never measured [13,17,24]. Also the effect of switching device capacitance was explored [21] and used to regulate the output voltage [22,23].

Three recent works stand out, and exemplify the need for the research and issues investigated in this thesis. The first one is a 100 MHz class E dc-dc converter [24]. The rectifier is designed to match the impedance of the inverter for optimum operation, but the circuit only operates at one power level and the overall efficiency was around 50%. The second work is a

study of the reverse recovery effect on Si, SiC and GaN diodes [27]. The tests are done on a boost converter application at 0.5, 1 and 2 MHz. Results showed that on Si diodes the reverse recovery effect has significant losses at the high frequencies considered, while the effect's losses are very small on SiC and GaN diodes.

In summary, the work presented in this thesis investigates the design of class E resonant rectifiers at HF (3-30 MHz) and VHF (30-300 MHz) frequencies. The modeling and design of such rectifiers is considered for operation to provide resistive input impedance over a wide operating power range. This is useful for the design of many kinds of dc-dc converter [9,11,12,34]. The thesis also investigates the performance of diodes for resonant rectification at VHF. The characteristics of diodes for this operating regime have not been thoroughly explored to date. Experimental performance evaluation is provided in this thesis for both commercially available diodes and select research devices.

### **1.3 Thesis Objective**

The purpose of this thesis is to provide a methodology for designing class E rectifiers by choosing the passive components such that the input impedance of the rectifier looks near-resistive for a wide operating power range. Also, a library of diode performance in VHF resonant rectification is provided for selecting the proper switching device. By using the material in this thesis, a designer will be able to choose an appropriate diode and the rectifier inductor and capacitor for minimal input phase over a given power range. This is very useful in dc-dc converter applications and other applications where the output dc voltage is constant.

### **1.4 Thesis Organization**

The remainder of the thesis is organized as follows: In chapter 2 we discuss the operation of the resonant class E rectifier and analyze its electrical behavior. The rectifier design method is developed and discussed thoroughly including simulation results. Chapter 3 provides the experimental validation of the design methodology. The experimental setup and procedure are discussed in detail along with experimental results. Chapter 4 explores the performance of commercially available Si Schottky diodes in resonant rectifiers at VHF. This chapter focuses on

low power devices, with a blocking voltage ranging from 60 V to 100 V and nominal current ratings of 1 A to 3 A. Results are discussed and a small library of commercially available diodes useful in VHF is developed. Chapter 5 continues the analysis started in the previous chapter but as applied to higher voltage and higher power diodes, with blocking voltages ranging from 500 V to 600 V and nominal current ratings of 4 A to 5 A. Chapter 6 concludes this work and summaries relevant findings.

## Chapter 2: Class E Rectifier Analysis and Design

The class E rectifier is a single diode “shunt loaded” rectifier. In traditional designs [7,13,16], the output inductor is a choke inductor carrying dc current into a resistive load. In the design presented here, the output inductor is a resonant inductor and the output voltage is constant for all power levels (i.e., a constant-voltage load). This is appropriate to the needs of dc-dc converters [4,5,7-12] and rectifiers for energy recovery systems [9,10] among other applications.

In the following sections, the circuit operation is described and the circuit state equations are derived. These equations are used to develop a set of plots that provide a graphical method of designing class E rectifiers optimized for near-resistive input impedance over a set of pre-specified power ranges. The plots are validated with SPICE simulations.

### 2.1 Class E Rectifier Operation and Analysis

A class E resonant rectifier driven by a sinusoidal current source is shown in Fig. 2.1. Modeling the input source as a sinusoidal current source is appropriate for analysis purposes, as in most applications the source feeding the class E resonant rectifier is sinusoidal and/or the rectifier is provided with a high Q ( $Q > 3$ ) series resonant tank at its input which makes the current nearly sinusoidal. In the proposed design the rectifier input series resonant tank is tuned on resonance at the desired operating frequency, with a sufficiently high loaded quality factor that the input current is substantially sinusoidal. This is similar to the design of class E inverters for variable-load operation as described in [11]. Hence, for analysis the input source will be assumed to be of the form  $i_{IN} = I_{IN} \sin(\omega t + \phi)$  where  $I_{IN}$  is the amplitude of the input current,  $\omega$  its angular frequency and  $\phi$  its phase. Having a non-zero phase ( $\phi$ ) associated with the input current allows us to define the time axis in such a way that time  $t = 0$  corresponds to the instant when the diode turns off.

The operation of the resonant rectifier is illustrated in Fig. 2.2, where we have assumed the diode to be ideal (excepting the diode capacitance, which is absorbed as part of the circuit operation). We are able to disregard the effect of the input-side resonant tank as the input current is sinusoidal and the input network is tuned on resonance. The diode turns off when

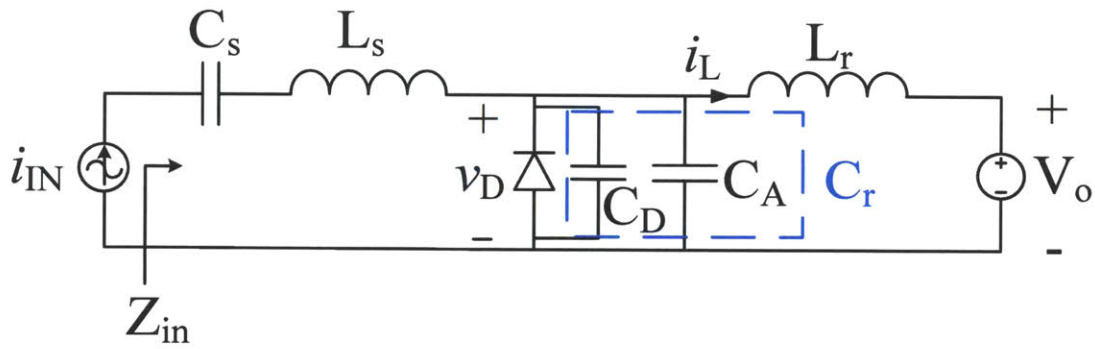
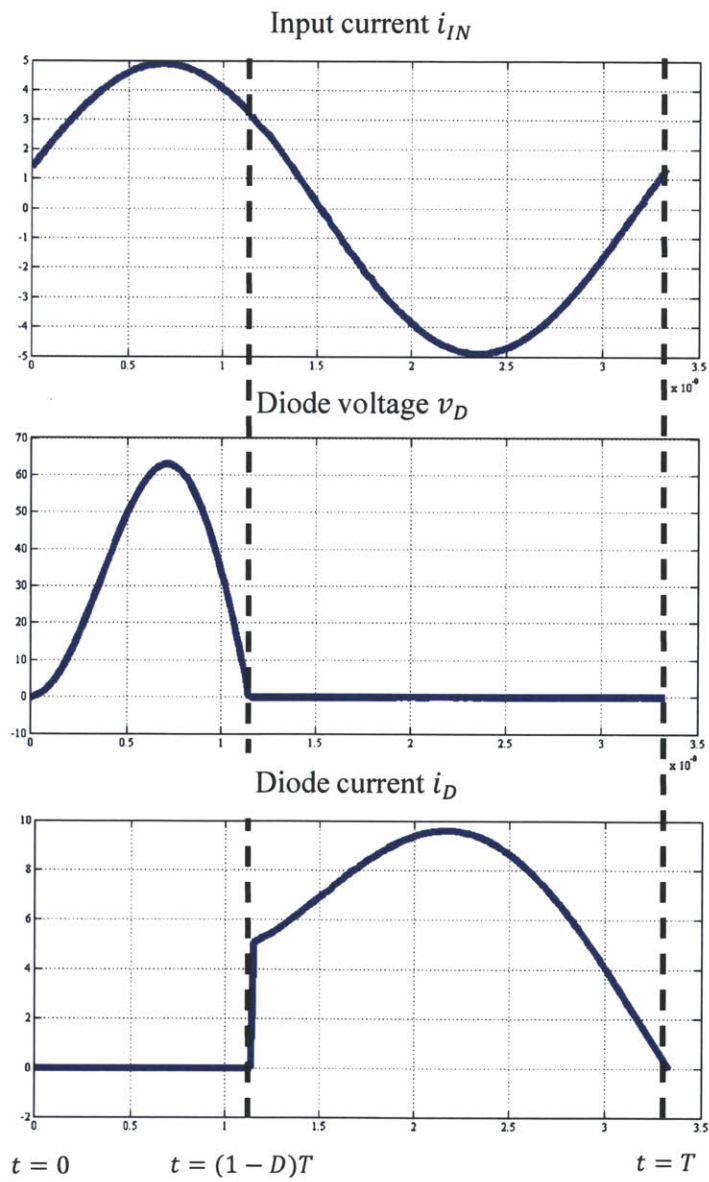


Figure 2.1. Class E rectifier driven by a current source.



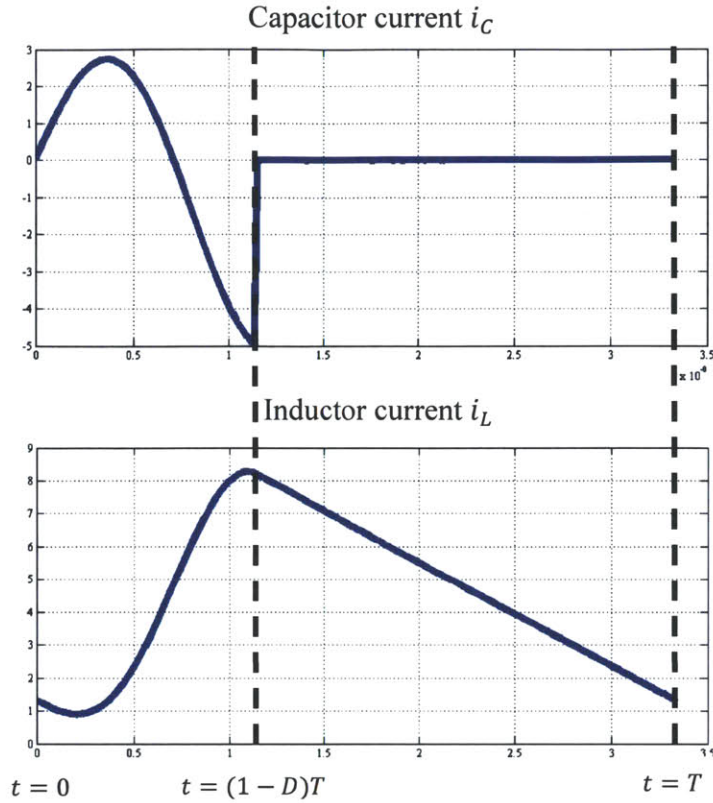


Figure 2.2. Class E resonant rectifier waveforms; from the top: (a) Input current, (b) diode voltage, (c) diode current, (d) capacitor current, and (e) inductor current.

the current through it ( $i_L - i_{IN}$ ) reaches zero (at  $t = 0$ ). At this instant the capacitor across the diode starts charging with zero initial current. As a result the reverse voltage across the diode increases slowly with an initial  $dv/dt$  equal to zero. The diode turns on when the reverse voltage across it returns to zero at  $t = (1-D)T$ , where  $T = (2\pi/\omega)$  is the period of the drive current and  $D$ , the duty ratio, is defined as the fraction of the period the diode stays on.

The inductor current ( $i_L$ ) waveform shown in Fig. 2.2 differs from that of a traditional class E rectifier. In a traditionally-designed class E rectifier, a large inductor is used at the output so that the inductor current is nearly constant. However, by relaxing this design constraint to allow a substantial ac current component in  $i_L$ , we open up the possibility of designing a class E rectifier with near-resistive input impedance. As the input filter network is tuned on resonance, the input impedance of the rectifier at the drive frequency is the ratio of the fundamental component of the diode voltage  $v_D(t)$  (and input voltage) to the fundamental component of the input current  $i_{IN}(t)$  (which has amplitude  $I_{IN}$ ). Since  $v_D$  is non-sinusoidal, its fundamental component needs to be extracted from its waveform. For this purpose, we develop an analytical

expression for the waveform of  $v_D$ . The reverse diode voltage waveform across the full period is given by:

$$v_D(t) = \begin{cases} \frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} \left[ \sin(\omega t) \sin(\phi) - \frac{Z_r}{\omega L_r} \sin(\omega_r t) \sin(\phi) + \cos(\omega_r t) \cos(\phi) - \cos(\omega t) \cos(\phi) \right] \\ -V_O \cos(\omega_r t) - I_{IN} Z_r \sin(\omega_r t) \sin(\phi) + V_O & \text{for } 0 \leq t \leq (1-D)T \\ 0 & \text{for } (1-D)T \leq t \leq T. \end{cases} \quad (1)$$

Here:

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (2)$$

is the resonant frequency of the  $L_r$ - $C_r$  resonant network and

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad (3)$$

is the characteristic impedance of the network.

The expression for  $v_D$  contains three unknowns: diode on-state duty ratio<sup>1</sup>  $D$ , input current amplitude  $I_{IN}$  and input current phase  $\phi$ . The values of these unknowns need to be determined before we can compute the fundamental component of  $v_D$ . For this we need to also develop an expression for the current in inductor  $L_r$ . To calculate the current, the circuit has to be analyzed in its diode-off and diode-on states. The inductor current  $i_L$  when the diode is off is given by:

$$i_{L,off}(t) = \frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} [\cos(\omega_r t) \sin(\phi) - \cos(\omega t) \sin(\phi) + \frac{\omega L_r}{Z_r} \sin(\omega_r t) \cos(\phi) - \sin(\omega t) \cos(\phi)] - \frac{V_O}{Z_r} \sin(\omega_r t) + I_{IN} \cos(\omega_r t) \sin(\phi) \quad \text{for } 0 \leq t \leq (1-D)T \quad (4)$$

and the inductor current when the diode is on is given by:

---

<sup>1</sup> The duty ratio -or fraction of the cycle during which the diode conducts- is of interest because it determines the limits of integration during fundamental frequency component extraction.

$$i_{L,on}(t) = -\frac{V_o}{L_r} \left[ t - \frac{2\pi(1-D)}{\omega} \right] + i_{L,off} \left( t = \frac{2\pi(1-D)}{\omega} \right) \quad \text{for } (1-D)T \leq t \leq T. \quad (5)$$

In addition, the class E rectifier circuit of Fig. 2.1 must satisfy three constraints. The first constraint is that the diode voltage  $v_D$  has to be zero when the diode turns on. The second constraint is that the average value of  $v_D$  has to be equal to the output voltage  $V_o$  (because the average voltage across inductor  $L_r$  is zero). The third constraint is that the average of inductor current  $i_L$  has to be equal to the output power  $P_o$  divided by the output voltage. In summary:

$$v_D \left( t = \frac{2\pi(1-D)}{\omega} \right) = 0, \quad (6)$$

$$\frac{1}{T} \int_0^T v_D(t) dt = V_o, \quad (7)$$

$$\frac{1}{T} \int_0^T i_L(t) dt = \frac{P_o}{V_o}. \quad (8)$$

By applying these constraints to (1), (4) and (5), we can derive three independent equations in terms of the three unknowns ( $D$ ,  $I_{IN}$  and  $\phi$ ) and  $\omega$ ,  $P_o$ ,  $V_o$ ,  $L_r$  and  $C_r$ <sup>2</sup>:

$$\begin{aligned} & \frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} \left[ \sin(2\pi(1-D)) \sin(\phi) - \frac{Z_r}{\omega L_r} \sin\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \right. \\ & \left. \sin(\phi) + \cos\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \cos(\phi) - \cos(2\pi(1-D)) \cos(\phi) \right] \\ & - V_o \cos\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) - I_{IN} Z_r \sin\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \sin(\phi) + V_o = 0 \end{aligned} \quad (9)$$

<sup>2</sup> Note that  $Z_r$  and  $\omega_r$  used in (9)-(11) are functions of  $L_r$  and  $C_r$ .

$$\begin{aligned}
& \frac{1}{T} \left[ \frac{I_{IN} \omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} \left[ \frac{-\cos(2\pi(1-D)) \sin(\phi)}{\omega} + \right. \right. \\
& \frac{Z_r}{\omega \omega_r L_r} \cos\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \sin(\phi) + \frac{\sin\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \cos(\phi)}{\omega_r} \\
& \left. \left. - \frac{\sin(2\pi(1-D)) \cos(\phi)}{\omega} \right] - \frac{V_o}{\omega_r} \sin\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \right. \\
& \left. + \frac{I_{IN} Z_r}{\omega_r} \cos\left(\frac{\omega_r}{\omega} 2\pi(1-D)\right) \sin(\phi) + V_o \frac{2\pi(1-D)}{\omega} \right. \\
& \left. - \left( \frac{I_{IN} \omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} \left[ \frac{-\sin(\phi)}{\omega} + \frac{Z_r \sin(\phi)}{\omega \omega_r L_r} \right] + \frac{I_{IN} Z_r}{\omega_r} \sin(\phi) \right) \right] = V_o \quad (10)
\end{aligned}$$

$$\begin{aligned}
& \frac{1}{T} \left[ \frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} \left[ \frac{\sin\left(\omega_r \frac{2\pi(1-D)}{\omega}\right) \sin(\phi)}{\omega_r} - \frac{\sin(2\pi(1-D)) \sin(\phi)}{\omega} \right. \right. \\
& \left. \left. - \frac{\omega L_r}{\omega_r Z_r} \cos\left(\omega_r \frac{2\pi(1-D)}{\omega}\right) \cos(\phi) + \frac{\cos(2\pi(1-D)) \cos(\phi)}{\omega} \right] \right. \\
& \left. + \frac{V_o}{\omega_r Z_r} \cos\left(\omega_r \frac{2\pi(1-D)}{\omega}\right) + \frac{I_{IN}}{\omega_r} \sin\left(\omega_r \frac{2\pi(1-D)}{\omega}\right) \sin(\phi) \right. \\
& \left. - \left( \frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1} \left[ -\frac{\omega L_r}{\omega_r Z_r} \cos(\phi) + \frac{\cos(\phi)}{\omega} \right] + \frac{V_o}{\omega_r Z_r} \right) \right. \\
& \left. - \frac{V_o}{2L_r} \left[ \frac{2\pi D}{\omega} \right]^2 + i_{L,off} \left( t = \frac{2\pi(1-D)}{\omega} \right) \left( \frac{2\pi D}{\omega} \right) \right] = \frac{P_o}{V_o} \quad (11)
\end{aligned}$$

These three equations, (9)-(11), can be solved numerically to find  $D$ ,  $I_{IN}$  and  $\phi$  for given values of  $\omega$ ,  $P_o$ ,  $V_o$ ,  $L_r$  and  $C_r$ . These equations were coded in Matlab and solved using the *fsolve* function (see Appendix A.1 for the Matlab code). This numerical approach is similar to the one used in [28-30]. The magnitude and phase of the input impedance are obtained by numerically extracting the fundamental Fourier series component of  $v_D$  and comparing it to the fundamental of  $i_{IN}$ .

In this application  $\omega$ ,  $V_o$  and the maximum value of  $P_o$  are fixed. For a given  $L_r$ ,  $C_r$  pair, the code sweeps power over a given range and calculates the maximum value of phase of the input impedance. This is repeated for a range of values of  $L_r$  and  $C_r$  to determine the variation in maximum amplitude of input impedance phase with variations in values of  $L_r$  and  $C_r$ . This analysis was done for four different power range ratios (ratio of maximum to minimum power Pmax:Pmin of 2:1, 5:1, 10:1 and 20:1).

These results were used to generate a set of normalized relationships that define the values for  $L_r$  and  $C_r$  that give the smallest deviation (in phase) from resistive operation over a specified operating power range ratio. This information is plotted in normalized form in three graphs (Figs. 2.3-2.5) that aid in the design of resonant class E rectifiers: (i) *maximum absolute value of input impedance phase vs. normalized capacitance*, (ii) *normalized peak diode reverse voltage vs. normalized capacitance*, and (iii) *normalized inductance vs. normalized capacitance*. The next section discusses the design of the class E rectifier using these plots.

## 2.2 Design Methodology

The design of the class E rectifier begins with its frequency  $f(= \omega/2\pi)$ , dc output voltage  $V_o$  and output power  $P_o$  specifications. These specifications can be used in conjunction with Figs. 2.3-2.5 to identify component values that minimize the worst case input impedance phase for a given power range ratio ( $P_{\max}:P_{\min}$ ).

Figure 2.3 shows the absolute value of the maximum input impedance phase vs. normalized capacitance, for four different power range ratios (2:1, 5:1, 10:1 and 20:1). The capacitance is normalized as follows:

$$C_n = C_r \frac{2\pi f V_o^2}{P_{o,max}}, \quad (12)$$

where  $P_{o,max}$  is the maximum (rated) output power. The plot shows that to minimize the input impedance phase, the capacitance should be selected as a minimum within other design constraints (such as device voltage rating, etc.). The value of capacitance obtained with this

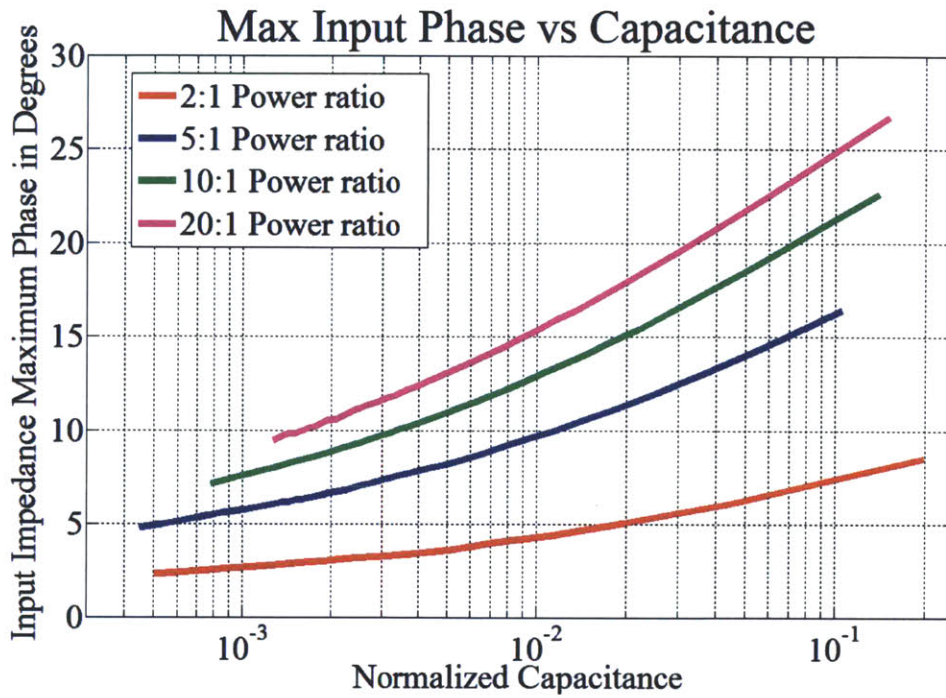


Figure 2.3. Worst-case phase angle magnitude across the specified operating conditions vs. normalized capacitance for different power ranges ratios ( $P_{max}:P_{min}$ ).

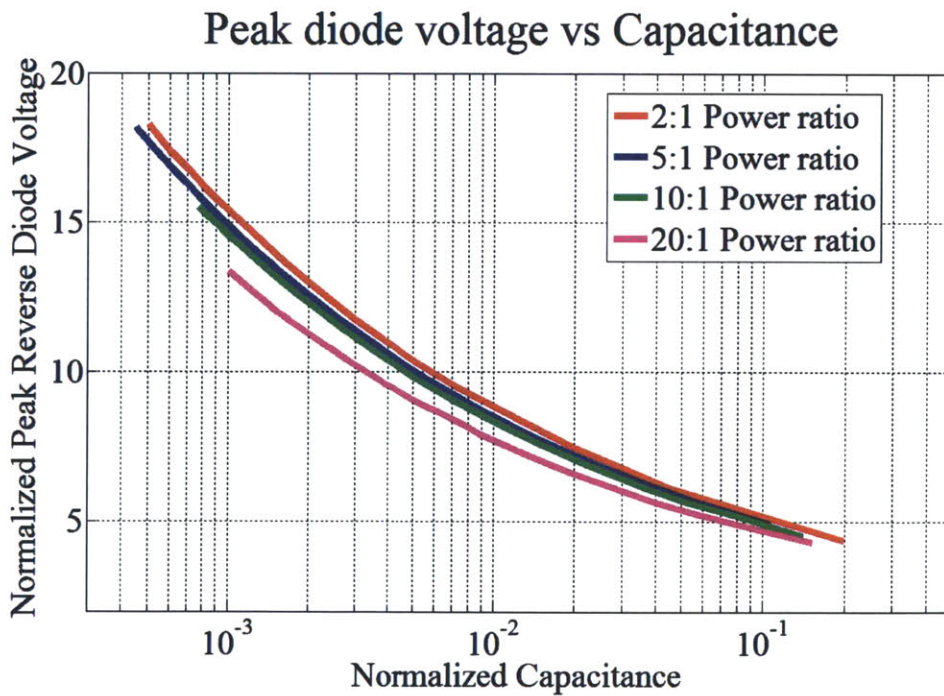


Figure 2.4. Maximum normalized peak reverse diode voltage vs. normalized capacitance for different power ranges ( $P_{max}:P_{min}$ ).

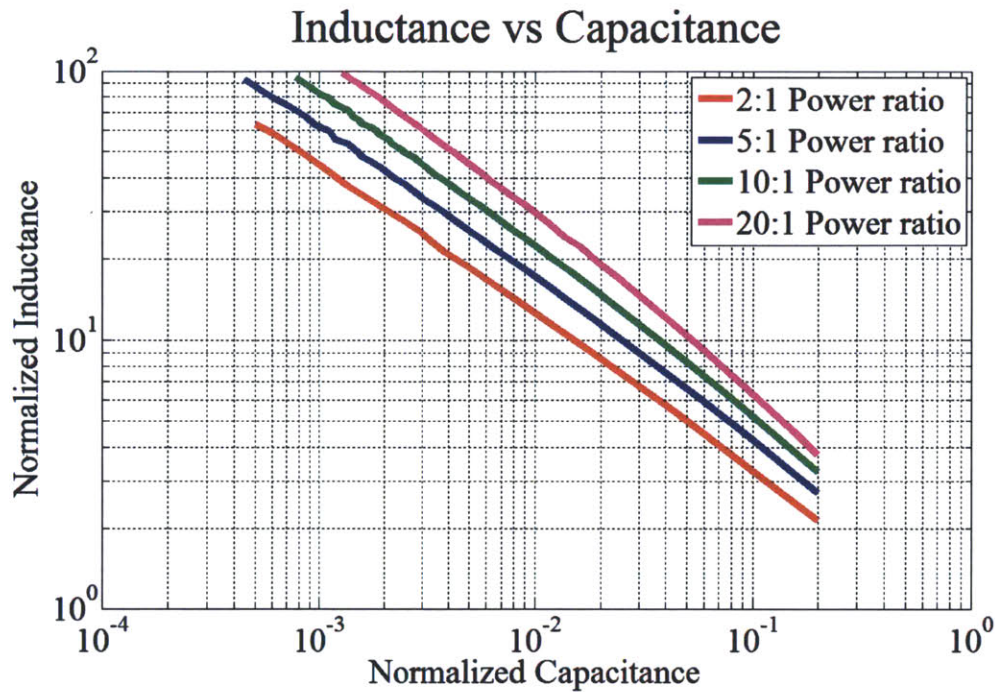


Figure 2.5. Normalized inductance vs. normalized capacitance for different power ranges ratios ( $P_{\max}:P_{\min}$ ).

methodology includes the intrinsic capacitance of the diode, any stray capacitance and any additional capacitance if needed. Hence,  $C_r$  cannot be chosen to be smaller than the intrinsic capacitance of the diode. A value of capacitance above this level should be chosen based on the acceptable value of maximum input impedance phase.

The next step is to select an appropriate diode. The required voltage rating of the diode for the selected normalized capacitance can be determined from Fig. 2.4. Figure 2.4 plots the normalized diode peak reverse voltage vs. normalized capacitance. The voltage is normalized to the dc output voltage:

$$V_{D,n} = \frac{V_{D,pk}}{V_o}, \quad (13)$$

where  $V_{D,pk}$  is the diode peak reverse voltage. The normalized reverse voltage blocking capability must be greater than what is indicated by Fig. 2.4 for the selected diode. The voltage stress on the diode is reduced as capacitance increases. Hence, Fig. 2.4 gives a minimum achievable

capacitance value for a given diode peak reverse voltage rating. Once the diode is selected, one can check Fig. 2.3 to ensure that the maximum input phase of the rectifier is within acceptable limits. If not, one might want to change the diode for one with a higher voltage rating and/or lower capacitance.

The next step is to select an appropriate value of  $L_r$ . Figure 2.5 shows a plot of normalized inductance vs. normalized capacitance. The inductance is normalized as follows:

$$L_n = L_r \frac{2\pi f P_{o,max}}{V_o^2}. \quad (14)$$

From this chart one determines the appropriate value of inductance  $L_r$  that will yield the most resistive input impedance across operating power for the selected capacitance.

Finally, the input  $L_s$ - $C_s$  filter is chosen so that the resonant frequency is equal to  $f$  and it provides an adequate  $Q$  to achieve the desired spectral purity of the rectifier input waveforms for the application in question. We can quantify the relationship as:

$$\sqrt{\frac{L_s}{C_s}} = QR_{min}, \quad (15)$$

where  $L_s$  and  $C_s$  are the input filter inductance and capacitance, respectively,  $Q$  is the quality factor of the filter and  $R_{min}$  is the minimum value (at rated power) of the magnitude of rectifier input impedance  $Z_{in}$ . The following section has a design example using this methodology that validates the approach.

### 2.3 Design Example and Simulation Results

This section demonstrates the use of the design methodology described above in the design of a class E rectifier. The example we consider at first is that of a class E resonant rectifier operating at a frequency of 30 MHz with output voltage of 12 V dc and output power ranging from 18 W down to 1.8 W (i.e., a 10:1 power range ratio). We would like the input impedance of the rectifier to be as resistive as possible (i.e., minimize the worst-case phase angle amplitude of the input impedance) over the entire power range, while using a 60 V diode with nominal capacitance of 80 pF (based on the PMEG6020EPA diode which has average current rating of 2A). Thus, the normalized peak diode voltage capability is about 4 (assuming we allow only up to around 48 V peak with appropriate margin). From Fig. 2.4, the corresponding normalized capacitance  $C_n$  is 0.2. From Fig. 2.3 the expected maximum absolute value of input impedance phase angle is about  $25^\circ$ . From Fig. 2.5 the normalized inductance is 3.5. De-normalizing the L and C values, the inductance  $L_r$  comes out to be 149 nH and the capacitance  $C_r$  comes out to be 132.6 pF. The value of  $C_r$  is greater than the 80 pF intrinsic capacitance of the diode. The input LC filter is designed with a Q of 3 and  $R_{\min}$  of  $19 \Omega$ , leading to a  $C_s$  of 93 pF and  $L_s$  of 302 nH. We also designed another rectifier with the same specifications except the power range ratio is 2:1. Only the value of  $L_r$  changed to 89 nH and the expected maximum value of impedance change is  $9^\circ$ . Table 2.1 summarizes the design and parameters for the rectifiers to be simulated.

Table 2.1. Class E Rectifier Parameter Values Used in the Simulation.

Parameter	Value for 10:1 Power Range	Value for 2:1 Power Range
$P_o$	18-1.8 W	18-9 W
$V_o$	12 V	12 V
$f$	30 MHz	30 MHz
$L_s$	302 nH	302 nH
$C_s$	93 pF	93 pF
$L_r$	149 nH	89 nH
$C_r$	132.9 pF	132.9 pF
$C_D$	80 pF	80 pF
$C_A$	52.9 pF	52.9 pF

Figures 2.6-2.8 show the SPICE simulation of our designed class E rectifier using the parameters given in Table 2.1 for 10:1 power range ratio. Figure 2.6 shows the peak diode voltage to be around 51 volts, which is well within the diode specifications and well matching the predicted peak voltage of 48 V for  $C_n = 0.2$  in this design. Figure 2.7 shows the input current to the rectifier, which contains low harmonic content at full power and gets distorted as power decreases. Figure 2.8 shows the inductor current with substantial ac current component.

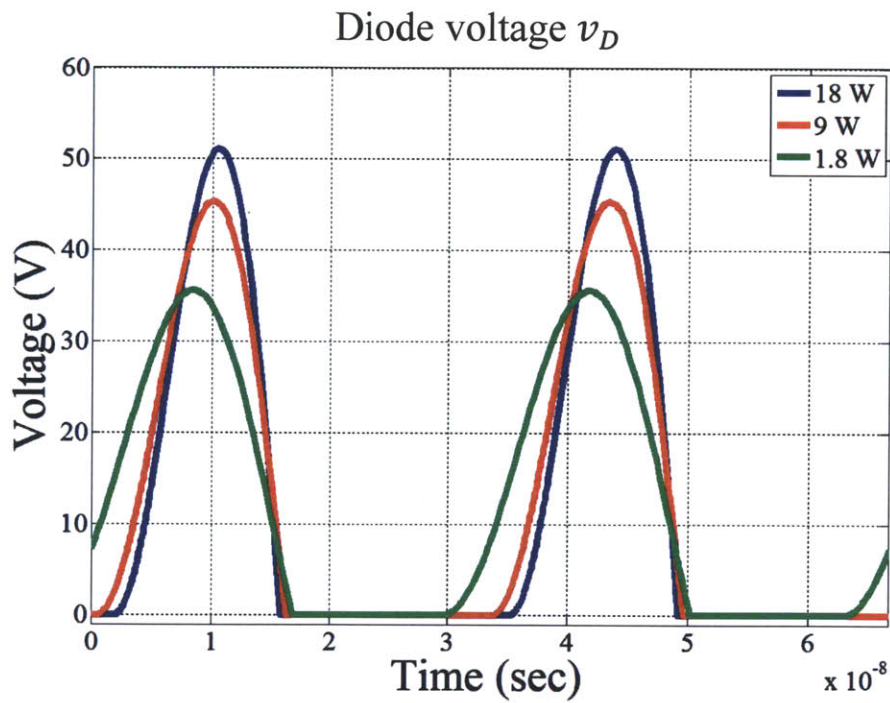


Figure 2.6. Time-domain simulation using SPICE of the diode voltage at 18 W, 9 W and 1.8 W of output power.

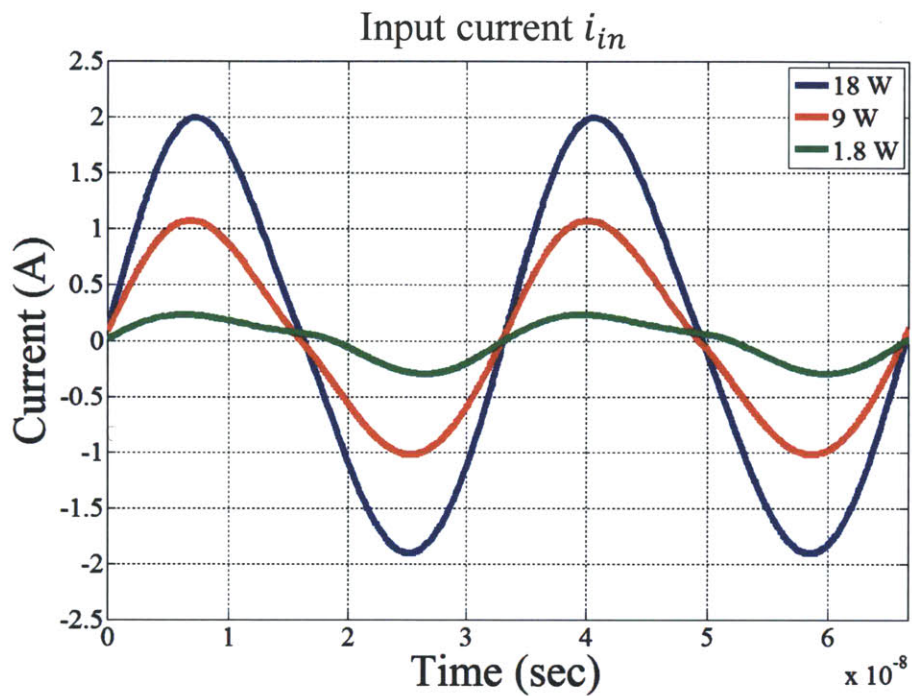


Figure 2.7. Time-domain simulation using SPICE of input current at 18 W, 9 W and 1.8 W of output power.

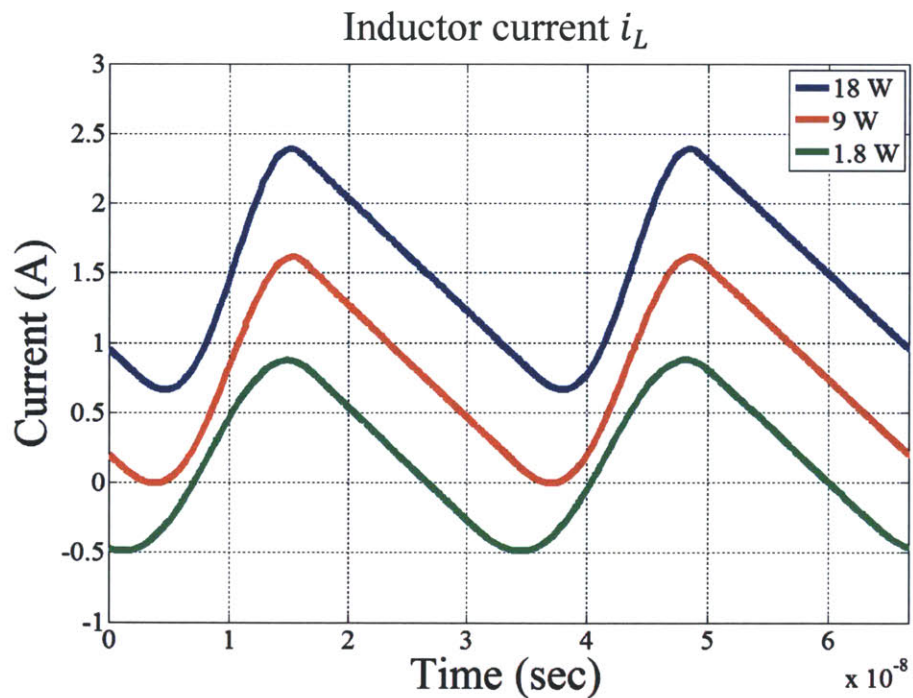
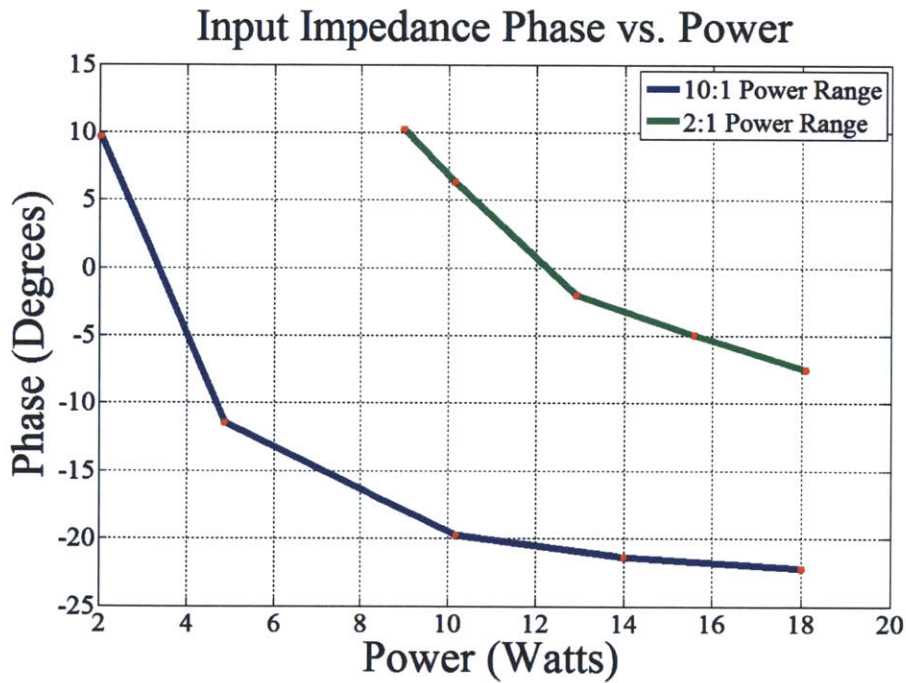
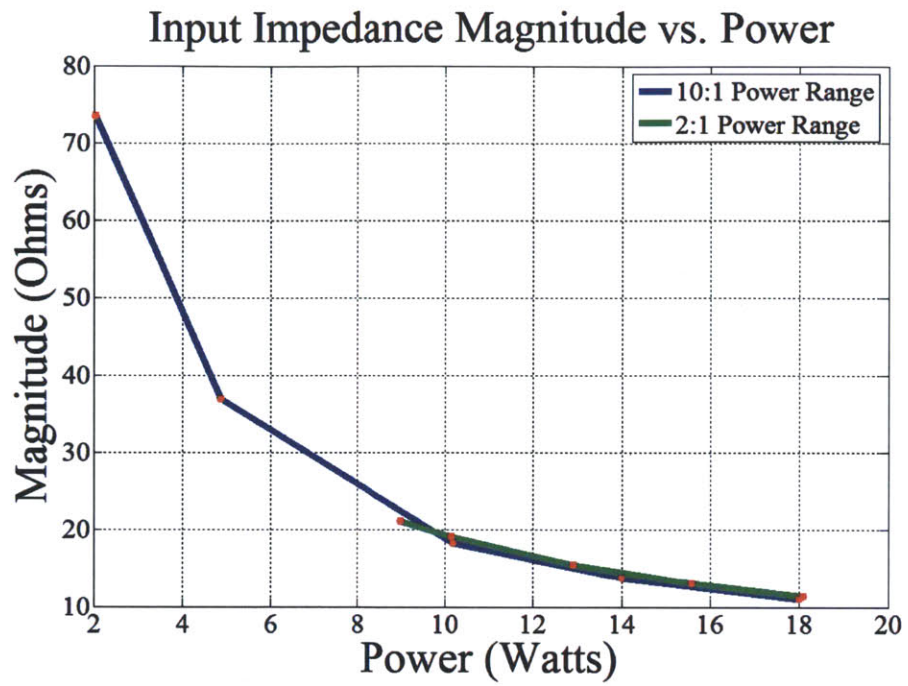


Figure 2.8. Time-domain simulation using SPICE of inductor current at 18 W, 9 W and 1.8 W of output power.

Figure 2.9 shows the phase and magnitude of the input impedance of the rectifier for 10:1 and 2:1 power range ratios. The impedance magnitude is inversely proportional to output power. The impedance is capacitive at high power and becomes inductive at low power. The maximum input impedance phase amplitude found by time-domain simulations across the specified operating power range is very close to the  $22^\circ$  predicted by the design graph in the 10:1 power range ratio. The 2:1 power range ratio curve has a maximum impedance phase of  $10^\circ$  which is in close agreement with the predicted  $9^\circ$ . The simulated results show that our design procedure works accurately, at least for idealized diode characteristics. It also shows that it is easier to get near resistive input impedance behavior for smaller operating power range ratios.



(a)



(b)

Figure 2.9. Resonant rectifier's simulated input impedance as a function of output power: for 10:1 and 2:1 power range ratios: (a) input impedance phase angle and (b) input impedance magnitude.

## Chapter 3: Experimental Validation of Class E Rectifier

In the previous chapter a methodology was introduced for designing class E rectifiers to provide near-resistive input for across a range of operating power levels. The design methodology minimizes the worst case value of input impedance phase for a specified power range ratio. It can likewise be used to maximize the power range ratio that can be achieved for a desired maximum amount of input impedance phase variation. This is useful in many applications, such as in developing dc-dc converters where it is desired to load the inverter stage with a rectifier that appears near resistive across a range of operating conditions.

In this chapter the design methodology will be validated experimentally with several designs. As the design methodology assumes a constant (linear) device capacitance, the effects of the diode non-linear junction capacitance on the design approach will be explored. Section 3.1 explains the experimental setup for the rectifier test, while sections 3.2 and 3.3 present and discuss the experimental results for high capacitance and near-resistive designs, respectively.

### 3.1. Experimental Setup

The class E resonant rectifier was designed using the methodology presented in chapter 2. Figure 3.1 shows the schematic of the class E rectifier. A wire and a current probe are added at the input to measure the input current. A TCP0030A 120 MHz current probe is used to measure the current. The inductance added by the current probe is used as part of the input filter inductance  $L_S$ . An additional inductance  $L_{ADD}$  is introduced to achieve the value of  $L_S$ . The cathode-to-anode (ground) voltage of the diode  $v_D$  is measured with an oscilloscope using a 500 MHz, 3.9 pF TPP0500 voltage probe.

The circuit parameters are input frequency of 30 MHz, output voltage of 12 V, maximum output power of 15 W and a 10:1 power range ratio. The diode used is an SS16 from Vishay. This diode is rated at 60 V of peak reverse voltage and 1 A of average forward current. The diode capacitance was approximated to be a constant 47 pF. This value is obtained from the device datasheet's capacitance-voltage (C-V) curve for the average diode voltage in this circuit (i.e., the output voltage).

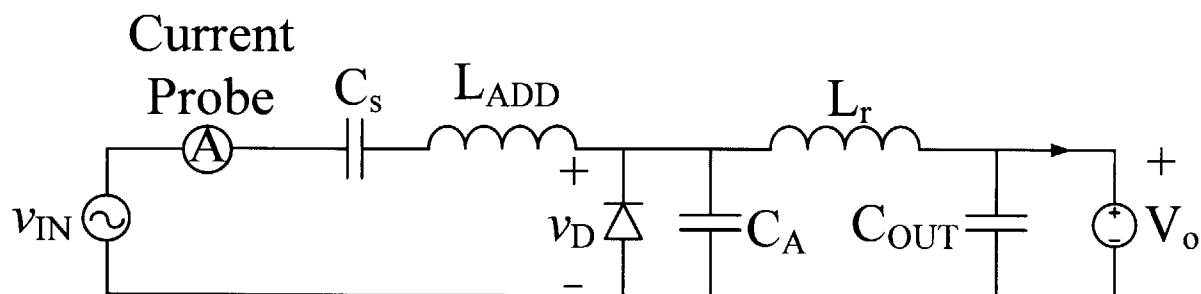


Figure 3.1. Class E resonant rectifier schematic. Includes the current probe to measure the input current.

Table 3.1. Rectifier circuit parameters. High capacitance design.

Parameter	Design Value	Circuit Implementation
$P_O$	15-1.5 W	15-1.5 W
$V_O$	12 V	12-13 V 10x SMBJ5349B in parallel
$f$	30 MHz	30 MHz
$L_S$	307 nH	306 nH
$L_{Probe}$	-	60 nH (approx.) Wire and current probe
$L_{ADD}$	-	246 nH Coilcraft MAXI Spring
$C_S$	91 pF	91 pF ATC 600S
$L_r$	51 nH	48 nH Coilcraft MIDI Spring
$C_r$	477 pF	477 pF
$C_D$	47 pF	47 pF Vishay SS16
$C_A$	430 pF	430 pF ATC 100B
$C_{OUT}$	20 $\mu$ F	20 $\mu$ F TDK Ceramic Cap

The first circuit is built to validate the design methodology under ideal conditions so is designed with a big shunt capacitance  $C_A$  to minimize the effect of the diode capacitance variability. The total  $C_r$  chosen to be 477 pF, which is about ten times the diode effective capacitance, and this means  $C_A$  is 430 pF. The input filter was tuned at 30 MHz with a  $Q$  of 3. Following the procedure described in chapter 2, for a 12 V output, maximum output power of 15 W, a power range ratio of 10:1, and a total rectifier capacitance of 477 pF, we get a rectifier inductance of  $L_r = 50$  nH. For this design, the expected maximum phase is predicted to be about  $30^\circ$  over a 10:1 power range ratio (from 1.5 W to 15 W), with a maximum of peak diode voltage predicted to be 38 V. Table 3.1 summarizes the rectifier parameters and Fig. 3.2 shows the rectifier circuit board. (The layout files for the circuit board are provided in Appendix B.1 and B.2.)

Figure 3.3 shows the block diagram of the experimental setup for determining input impedance. The rectifier is driven by a power amplifier (ar 150A100B) with a sinusoidal input from a signal generator (BK Precision 4087). The load of the rectifier is a zener bank that consists of 10 SMBJ5349B diodes connected in parallel and mounted to a heat sink. The output dc voltage and current are measured with multimeters (Agilent U3606A and 34401A), the rectifier voltage is measured with a (10x, 500 MHz) oscilloscope probe model TPP0050, and the rectifier input current is measured with the TCP0030A current probe.

The effective rectifier impedance is defined as the complex ratio of rectifier fundamental input voltage  $v_{IN}$  to rectifier fundamental input current  $i_{IN}$ . The input impedance is found by measuring the input voltage and current at different output power levels, extracting the fundamental frequency component of each signal through Fourier analysis in MATLAB, and taking the ratio of the two. (It is noted that the rectifier input voltage and the diode voltage ideally have the same fundamental, as the input tank is tuned on resonance. As described below, in some cases input impedance is estimated using measurements of diode fundamental voltage as the "input" voltage.). The ratio of the fundamental voltage amplitude to fundamental current amplitude is the magnitude of the impedance and the phase shift between the fundamental voltage and current signals is the impedance phase. In order to measure the phase accurately, it is important that the oscilloscope and its probes are calibrated and deskewed with good precision before each test. The oscilloscope used is a Tektronix MSO 4054B, the current probe is the TCP0030A and the voltage probe is the TPP0500. The delay between the probes needs to be adjusted (deskewed) to get an accurate phase measurement.

A circuit that aids in calibrating the oscilloscope was developed. The circuit was built on a similar board to the rectifier and consists of the same input LC filter of the rectifier (including the current probe) with a  $50\ \Omega$  RF load. The circuit was tuned appropriately at the fundamental switching frequency so that at 30 MHz the impedance seen at the input is a pure  $50\ \Omega$  resistive load. Figure 3.4 shows the impedance measurement of the calibration circuit. The calibration circuit is connected to the power amplifier and driven by a small amount of power and the delay on the current and voltage probes is adjusted so that the signals overlap and have zero phase shift between them. This sets the scope to the zero phase or resistive impedance: any variation on the phase will be caused by the rectifier circuit. The next section discusses the experimental results.

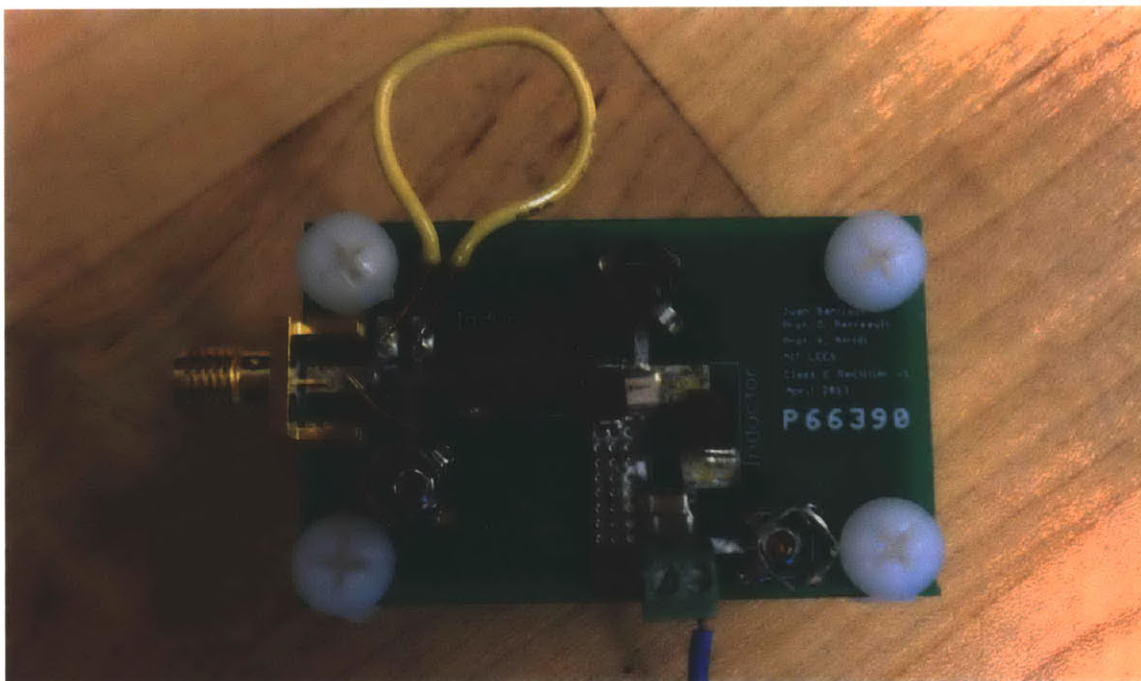


Figure 3.2. Class E resonant rectifier rated for 15 W, 12 V output voltage and 30 MHz switching frequency.

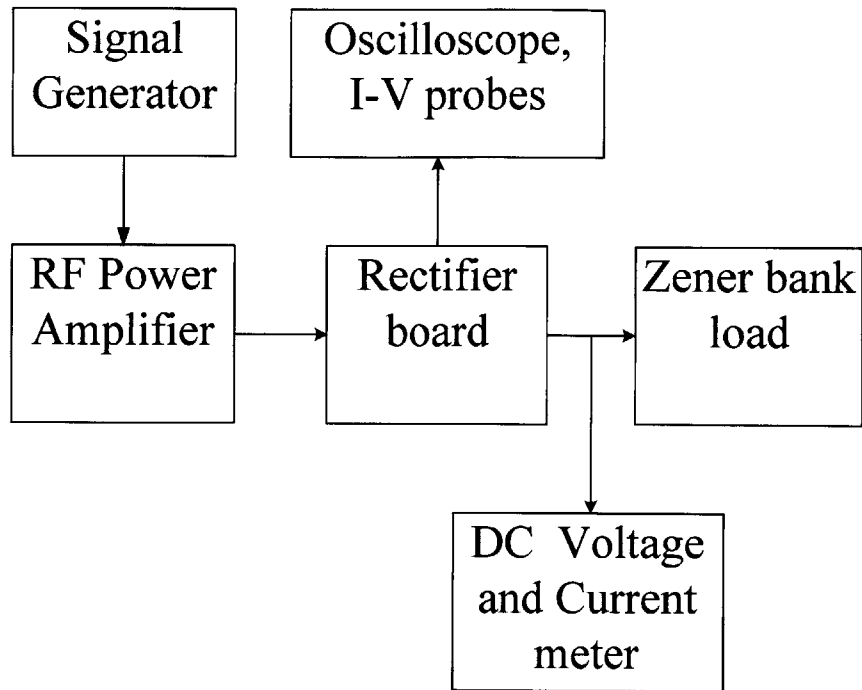


Figure 3.3. Block diagram of the rectifier impedance test setup.

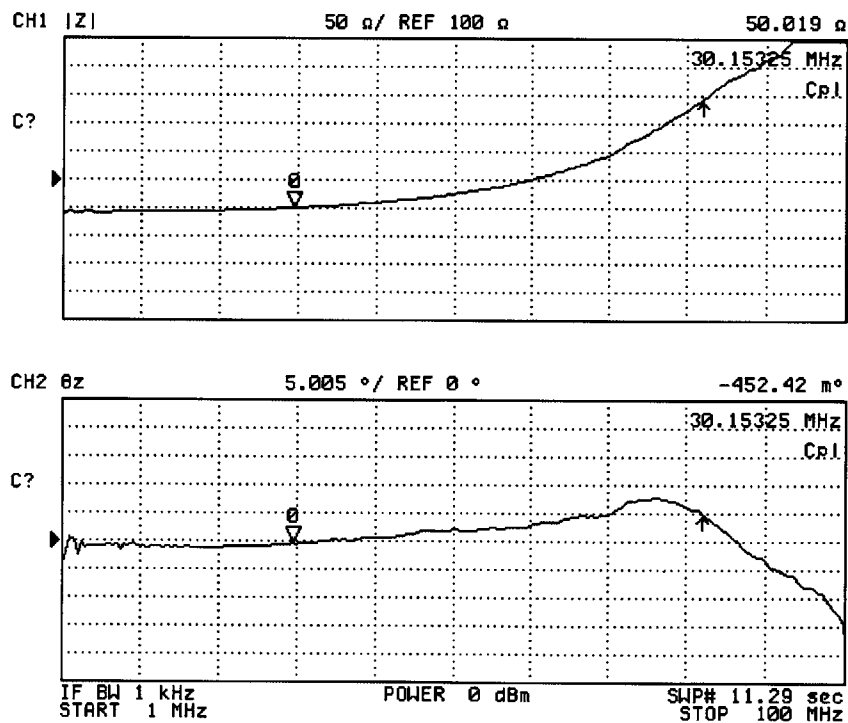


Figure 3.4. Oscilloscope calibration circuit input impedance. At 30 MHz the circuit looks like a 50  $\Omega$  resistive load. All higher harmonics are effectively suppressed by the higher impedance of the circuit. This plot was taken from an Agilent 4395 impedance analyzer.

### 3.2. High capacitance design

The waveforms of the calibration circuit are shown in Fig. 3.5. The delay between the voltage and current probe was adjusted to get zero phase with a resistive load. The input impedance of the rectifier was measured using voltage measurements in two places: at the diode (assuming no phase contributions by the input LC filter) and at the input of the rectifier (including the filter). Ideally the fundamental voltage measured at these two locations should be nearly identical, as the input tank is (ideally) tuned on resonance. One measurement is done to prove the theory developed in chapter 2 with the experimental data, and another measurement is made as in a real application that includes filtering. The data is measured with the oscilloscope and processed in Matlab for fundamental frequency component extraction. (The code for this is provided in Appendix A.2)

Figure 3.6 shows a plot of the impedance phase vs. power and Fig. 3.7 plots the measured impedance magnitude vs. power. Simulation results are also plotted; the simulation is ideal, including only a linear device capacitance of 47 pF, and does not include parasitic inductances, diode forward drop, output voltage increase with power due to zener diode impedance or other non-idealities. The plot shows that the maximum impedance phase is  $30^\circ$ , which confirms our expected value from the design plots in chapter 2 (predicted values of  $30^\circ$  for operation from 1.5 W to 15 W).

Figure 3.8 is a screenshot of the diode voltage and input current at full power. The peak diode voltage is 42 V, which is very close to the value of 38 V predicted using Fig. 2.4 in chapter 2 for this design. It is suspected that this small deviation is due to the increase in output voltage (above 12 V) owing to the nonzero impedance of the zener bank load. A simulation that includes the output voltage increase to 13 V at full power shows the peak diode voltage is increased to 40 V. This confirms our expected value of peak diode voltage based on the design plots from chapter 2. Figs. 3.9 and 3.10 show the diode voltage and input current waveforms for 5.9 W and 1.44 W output power, respectively.

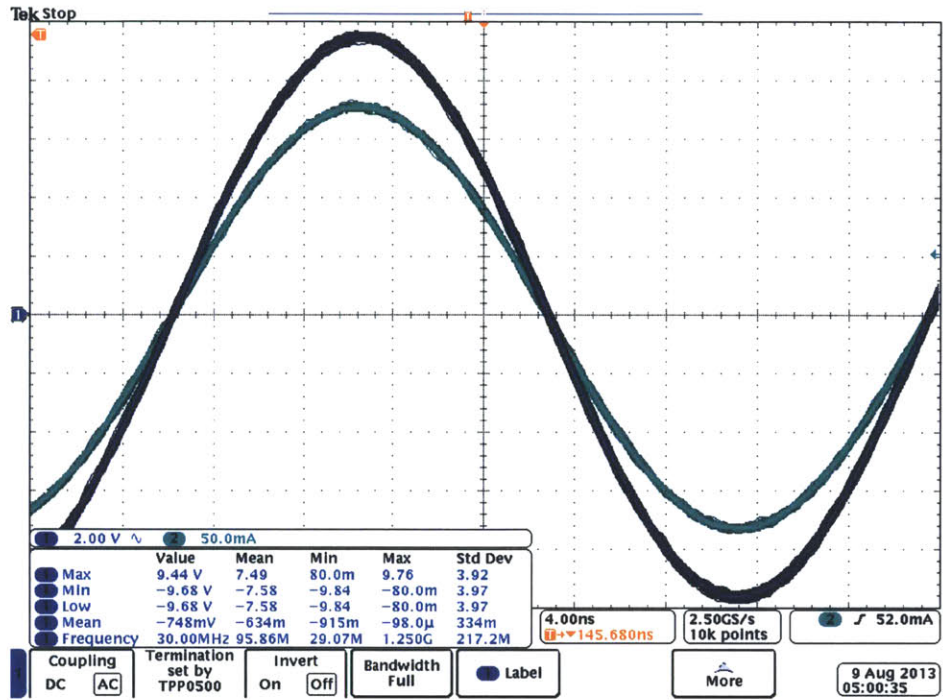


Figure 3.5. Calibration circuit voltage (dark blue) and current (light blue) waveforms. The oscilloscope is calibrated so that the waveforms are in phase with a 50 Ω load at 30 MHz.

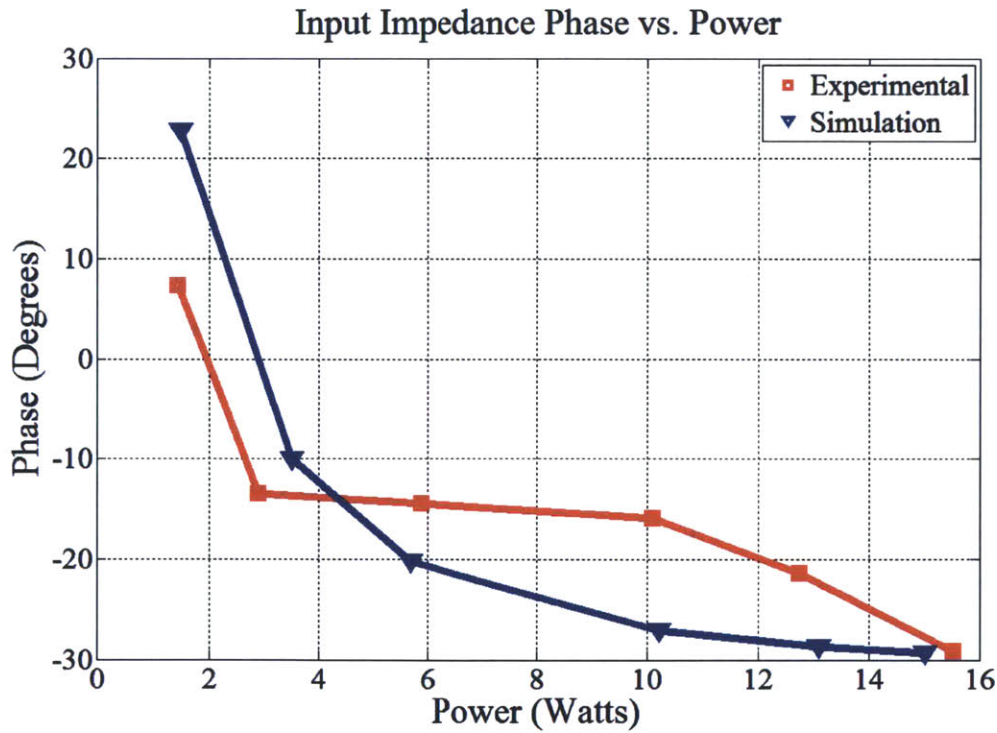


Figure 3.6. Input impedance phase vs. output power with rectifier fundamental voltage measured at the diode. The red curve is the measured experimental data and the blue curve is the simulation data. The maximum absolute phase over the specified power range is 30°.

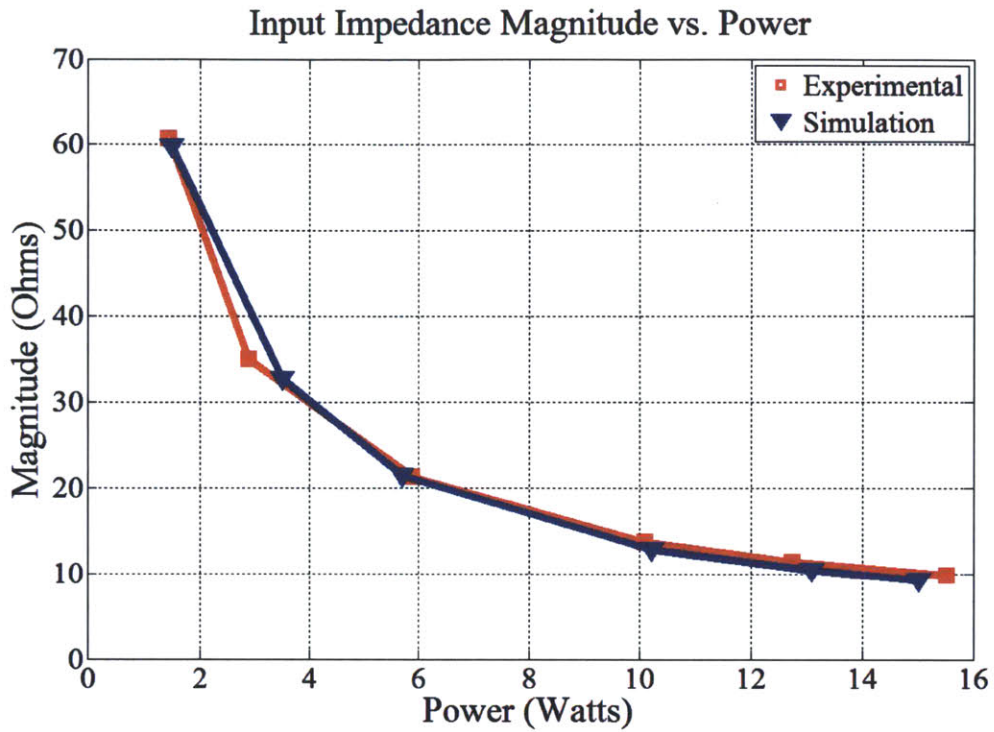


Figure 3.7. Input impedance magnitude vs. power output with “input” voltage measured at the diode. The red curve is the measured experimental data and the blue curve is the simulation data.

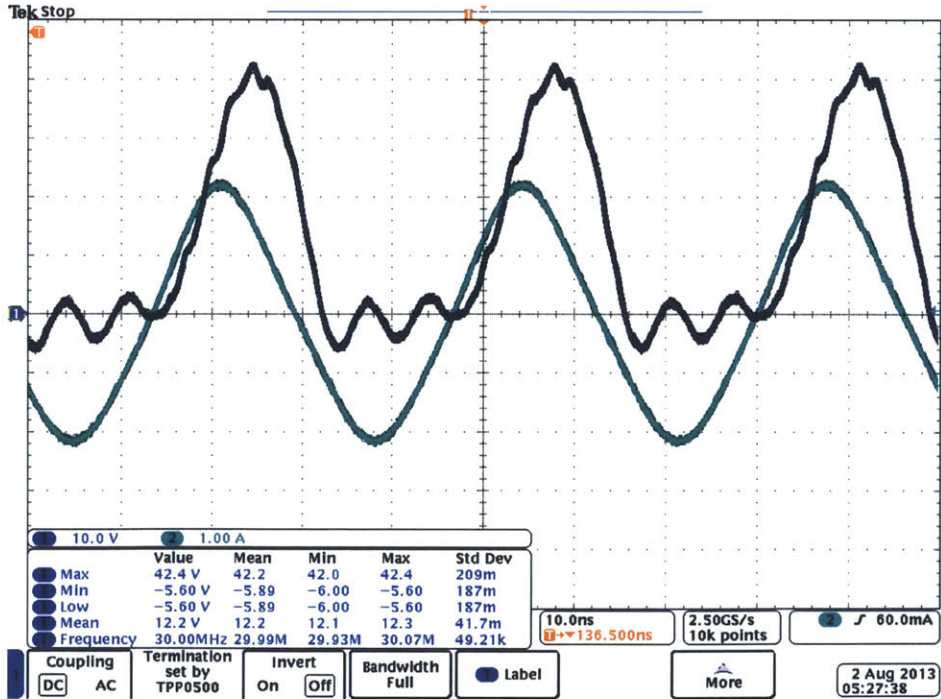


Figure 3.8. Diode voltage (dark blue) and input current (light blue) at full power, 15.53 W for the circuit of Fig. 3.1 and values in table 3.1. The peak diode voltage is 42 V.

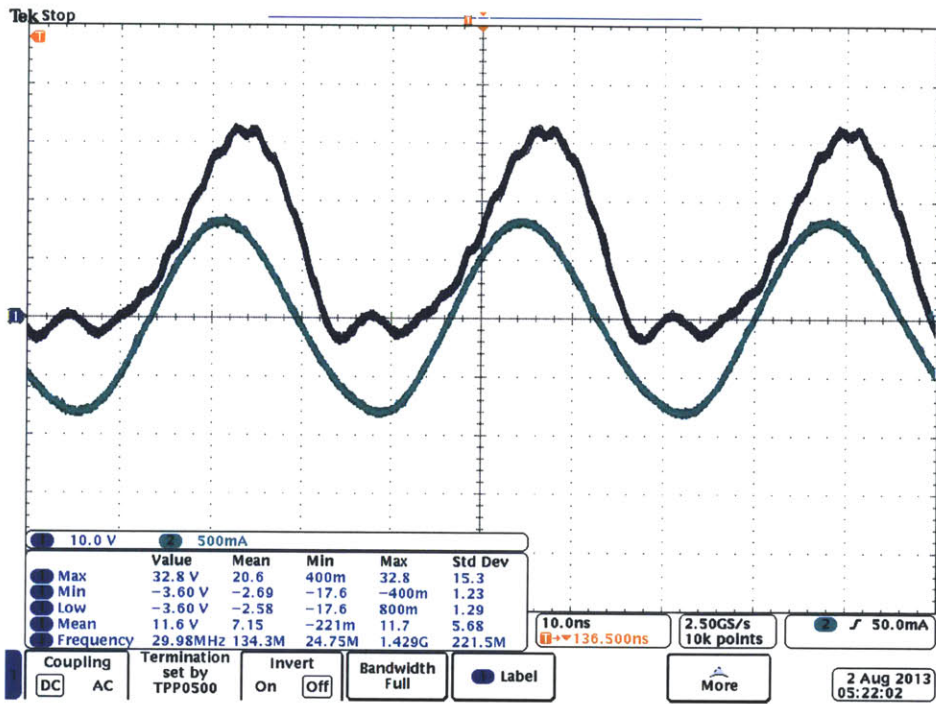


Figure. 3.9. Diode voltage (dark blue) and input current (light blue) at medium power, 5.9 W for the circuit of Fig. 3.1 and values in table 3.1. The peak diode voltage is 32 V.

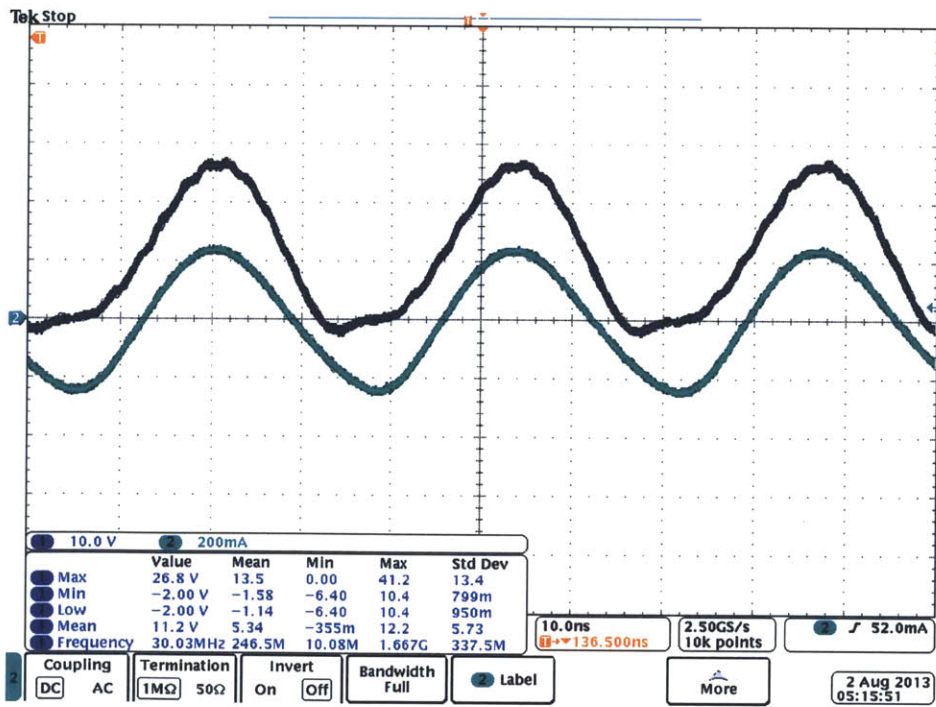


Figure. 3.10. Diode voltage (dark blue) and input current (light blue) at minimum power, 1.44 W for the circuit of Fig. 3.1 and values in table 3.1. The peak diode voltage is 27 V.

The impedance measured including the LC input filter (i.e., with rectifier input voltage measured at the input of the LC tank) is shown in Figs. 3.11 and 3.12. The magnitude of the impedance matches well with the simulation, but the phase deviates at high power. This could be attributed to mismatch between the operating frequency and the input filter’s resonant frequency. For a second iteration a tunable inductor was used to replace the inductor  $L_{ADD}$  of Fig. 3.1. The inductor is a winding on a plastic shell with a core that one can move inside and change the permeability of the inductor. The inductor used was a Coilcraft 142-05J08L unshielded 10 mm tunable inductor. Figures 3.13 and 3.14 show the impedance after tuning the filter inductance to achieve a better response. The experimental data follows the simulation results. The results confirm the effectiveness of the design approach.

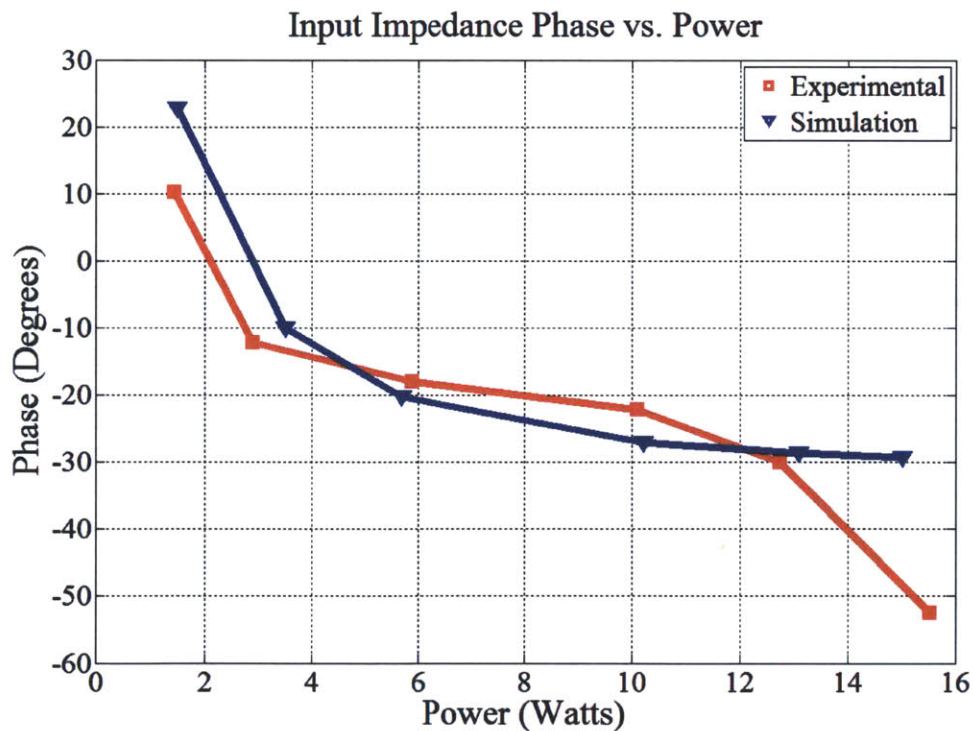


Figure 3.11. Input impedance phase vs. output power with voltage measured at the input port for the circuit of Fig. 3.1 and values in table 3.1. The red curve is the measured experimental data and the blue curve is the simulation data.

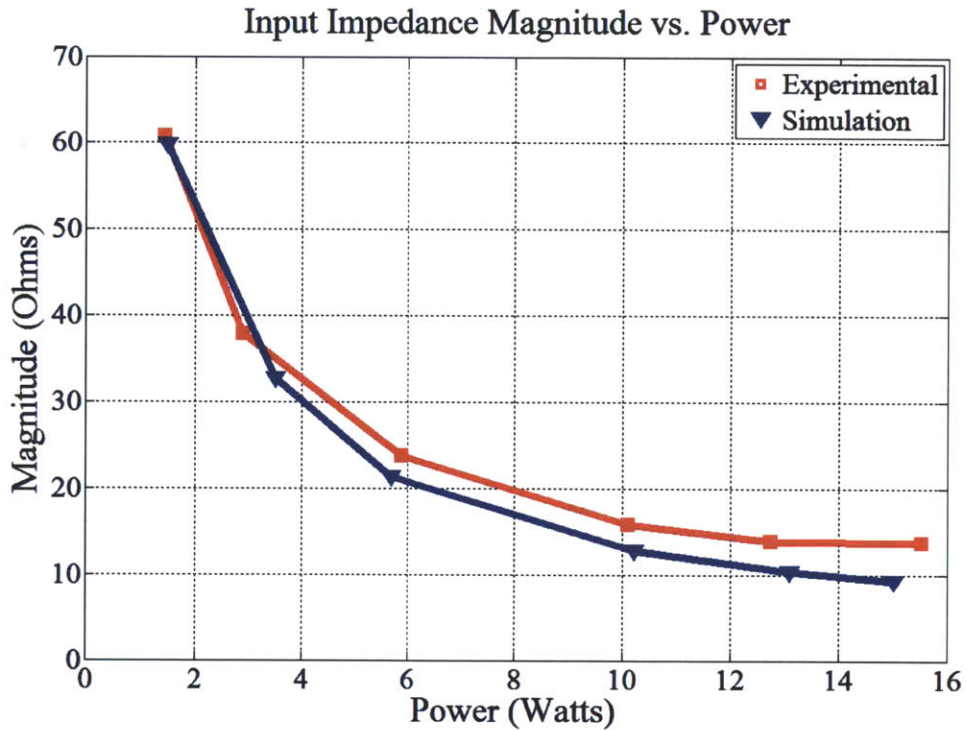


Figure 3.12. Input impedance magnitude vs. output power with voltage measured at the input port for the circuit of Fig. 3.1 and values in table 3.1. The red curve is the measured experimental data and the blue curve is the simulation data.

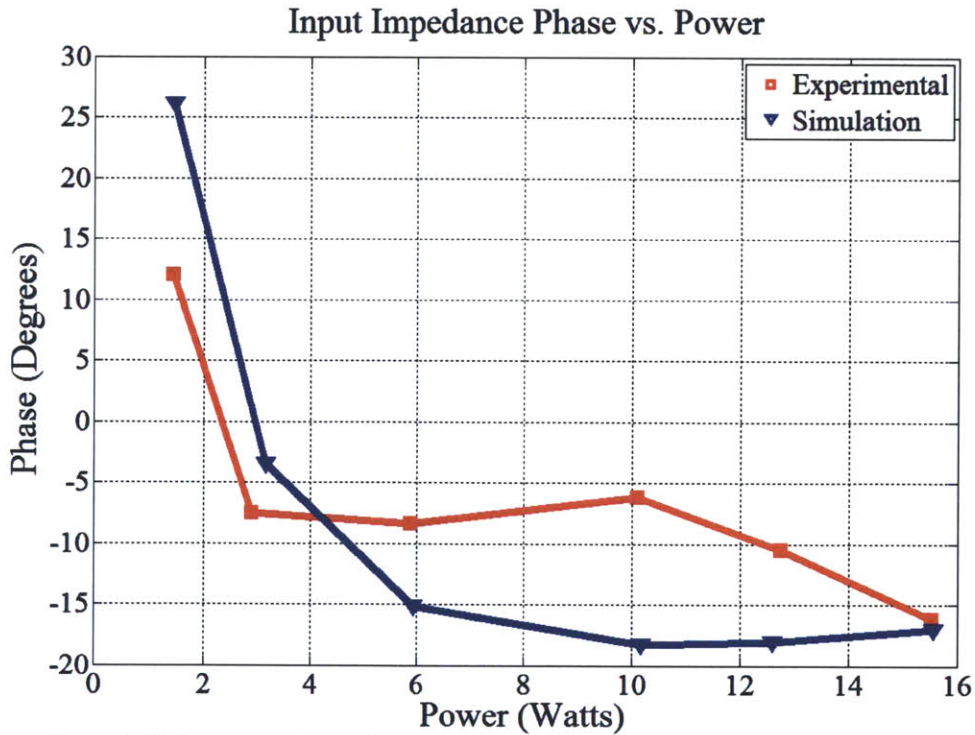


Figure 3.13. Input impedance phase vs. output power with voltage measured at the input port with adjusted  $L_{ADD}$  for the circuit of Fig. 3.1 and values in table 3.1. The red curve is the measured experimental data and the blue curve is the simulation data.

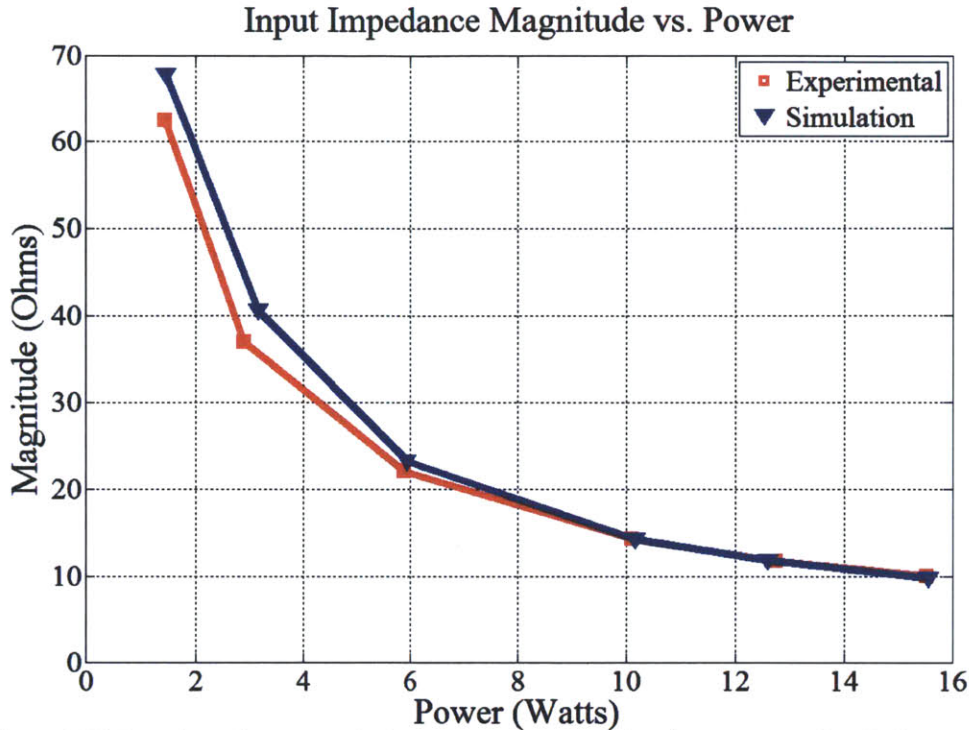


Figure 3.14. Input impedance magnitude vs. output power with voltage measured at the input port with adjusted  $L_{ADD}$  for the circuit of Fig. 3.1 and values in table 3.1. The red curve is the measured experimental data and the blue curve is the simulation data.

### 3.3 Near-resistive input design

A second rectifier circuit was designed for near-resistive behavior (low phase shift) using the design approach of chapter 2. The specifications are input frequency of 30 MHz, output voltage of 12 V, max output power of 12 W, power range ratio of 2:1 and a maximum allowed phase shift of  $10^\circ$ . Following the design method described in chapter 2, with  $C_n$  equal to 0.2 and  $L_n$  equal to 2.1, the expected value of maximum phase shift is  $9^\circ$  and the expected peak diode voltage is 53 V. The diode used is the same as in the previous design, Vishay's SS16. Table 3.2 summarizes the circuit parameters. All the following impedance data is measured using voltage measurements at the diode cathode node. In the previous section it was proven that measuring voltage at the cathode is equivalent to measuring it at the input port for our input impedance analysis purposes, and simultaneously we can monitor the diode reverse voltage and make sure it does not exceed the rated value. Figures 3.15 and 3.16 show the experimental and simulation impedance data. The points do not match very well and the maximum phase shift exceeds  $10^\circ$  at

low power level. This shows one of the limitations of the design methodology: the effect of the diode junction capacitance.

The design methodology assumes a constant diode capacitance, but this assumption is valid when the external capacitance is considerably higher than the assumed constant value of the diode capacitance or when the actual diode capacitance is nearly constant with voltage. In the diode tested, the capacitance varies between 210 pF and 19 pF between 0.1 V and 60 V. As the capacitance varies over the switching cycle, the diode voltage waveform varies from that of a system having a constant diode capacitance. A simulation is prepared with  $C_A = 85.9$  pF (additional shunt capacitance),  $L_r = 89.13$  nH, a constant diode capacitance  $C_D$  of 47 pF and a variable  $C_D$  of  $222.95/(1+v_D/0.9511)^{0.5987}$  pF. The variable capacitance model was derived from a curve fitting of the C-V plot on the datasheet of an SS16 diode, while the constant value was taken from the same plot at the average diode voltage. Figure 3.17 shows the peak diode voltage simulation results for the two diode capacitance models at the same output power (18 W) and output voltage (12 V) levels. It is clear that the behavior of the circuit changes depending on the capacitance model used.

Moreover, as power varies, the *effective* value of the diode capacitance varies, changing the input impedance from what would be predicted by the curves of Chapter 2. For example, consider again the SS16 diode, which has a capacitance vs. voltage approximately as illustrated in Fig. 3.18. If the external capacitance is comparable in magnitude to the diode capacitance at a dc output voltage of 12 V, the capacitance on the cathode node is dominated by the external capacitance when the diode voltage is high. As power goes down, the peak voltage on the diode decreases and the node capacitance increases and is dominated by the diode nonlinear capacitance. This makes the impedance of the circuit slightly unpredictable by using the method from chapter 2. The effect can also be seen on Fig. 3.19. The peak diode voltage at full power was predicted to be 53 V which is acceptable for the SS16 (a 60 V diode), but the experimental value is 60.6 V. The simulation with increased output zener voltage of 12.7 V yielded 54.4 V of peak diode voltage, an increase of 2.64% which is still less than the 14.3% increase present in the experimental data. This increase in peak diode stress is also due to lower node capacitance at high voltages. These phenomena are not present in the high capacitance design seen in the previous subsection, as the capacitance was dominated by the linear external capacitance.

In summary, all the predictions by the design methodology are accurate for the case where the total capacitance across the diode (including diode capacitance) does not vary much with voltage (e.g., owing to using substantial external linear capacitance or having a diode with only small capacitance variation). However, it may not be very accurate for the case where the effective capacitance across the diode varies substantially with voltage. This presents a limitation in the design method, but further iterations on the design could yield better results.

Table 3.2. Rectifier circuit parameters for a design with small external capacitance across the diode.

<b>Parameter</b>	<b>Design Value</b>	<b>Circuit Implementation</b>
$P_O$	12-6 W	13-6 W
$V_O$	12 V	12-12.7 V 10x SMBJ5349B in parallel
$f$	30 MHz	30 MHz
$L_S$	307 nH	306 nH
$L_{Probe}$	-	60 nH (approx.) Wire and current probe
$L_{ADD}$	-	246 nH Coilcraft MAXI Spring
$C_S$	91 pF	91 pF ATC 600S
$L_r$	133 nH	130 nH Coilcraft MAXI Spring
$C_r$	88.4 pF	89 pF
$C_D$	47 pF	47 pF Vishay SS16
$C_A$	41.4 pF	42 pF ATC 100B
$C_{OUT}$	20 $\mu$ F	20 $\mu$ F TDK Ceramic Cap

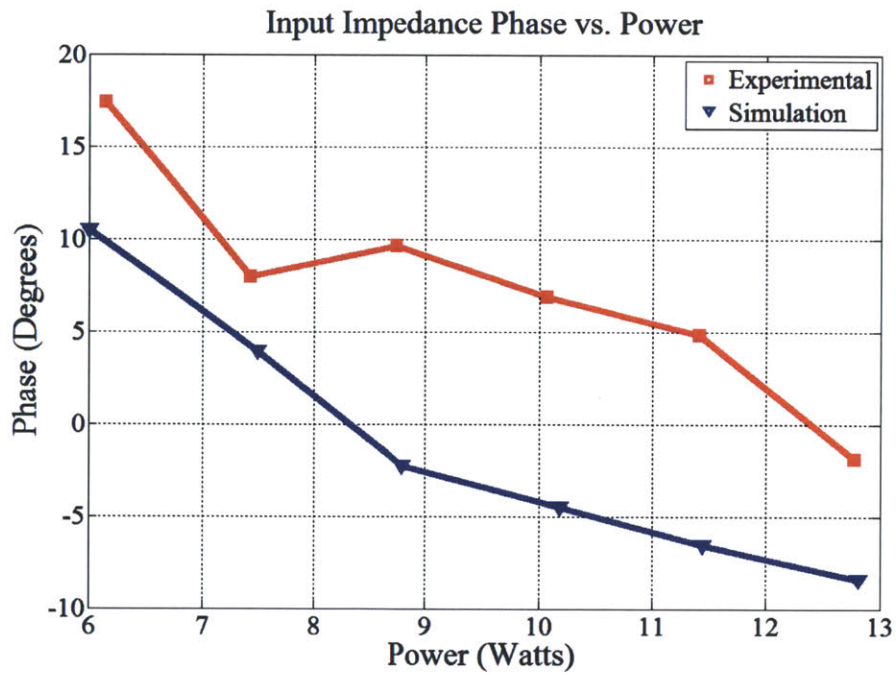


Figure 3.15. Input impedance phase vs. power measured at the diode voltage node for the circuit of Fig. 3.1 and values in table 3.2. The red curve is the measured experimental data and the blue curve is the simulation data.

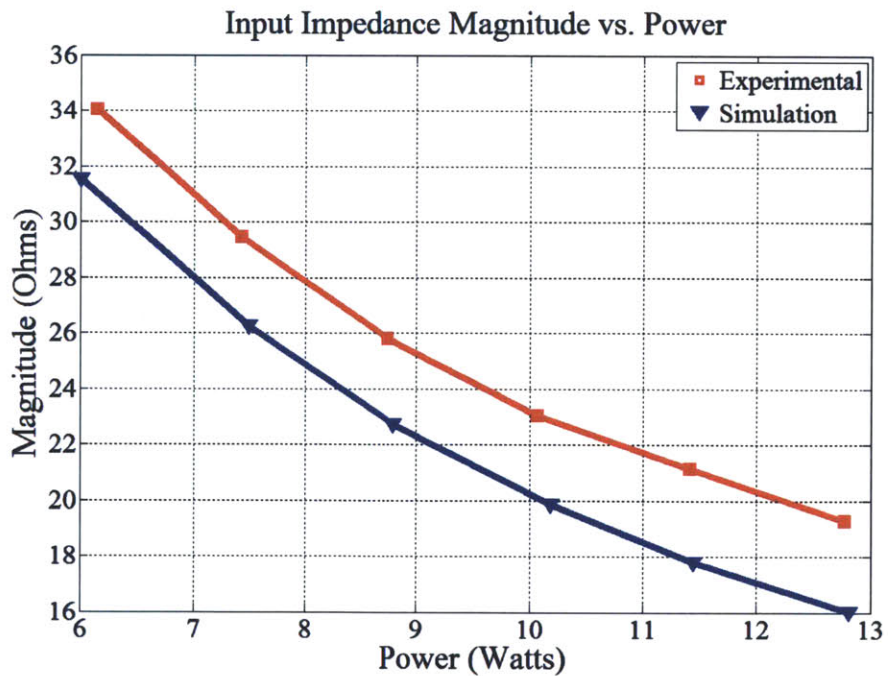


Figure 3.16. Input impedance magnitude vs. power measured at the diode voltage node for the circuit of Fig. 3.1 and values in table 3.2. The red curve is the measured experimental data and the blue curve is the simulation data.

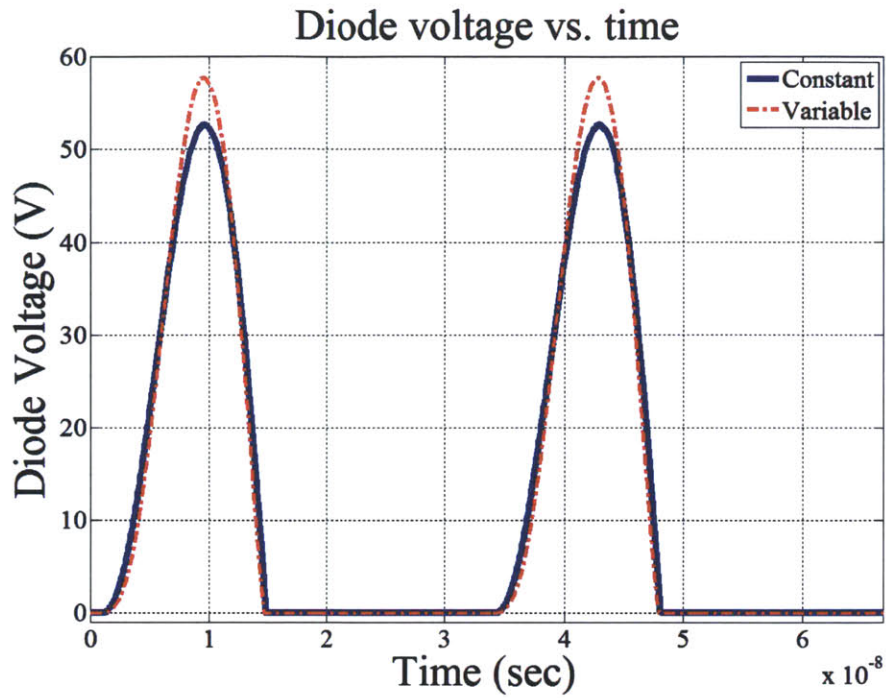


Figure 3.17. Diode voltage vs. time simulation results for a constant capacitance and for a variable capacitance. The range of the diode capacitance is 210 to 19 pF, and the constant value is 47 pF. The external capacitance is 86 pF. At higher voltage, the variable capacitance is lower and thus the reverse voltage peaks higher.

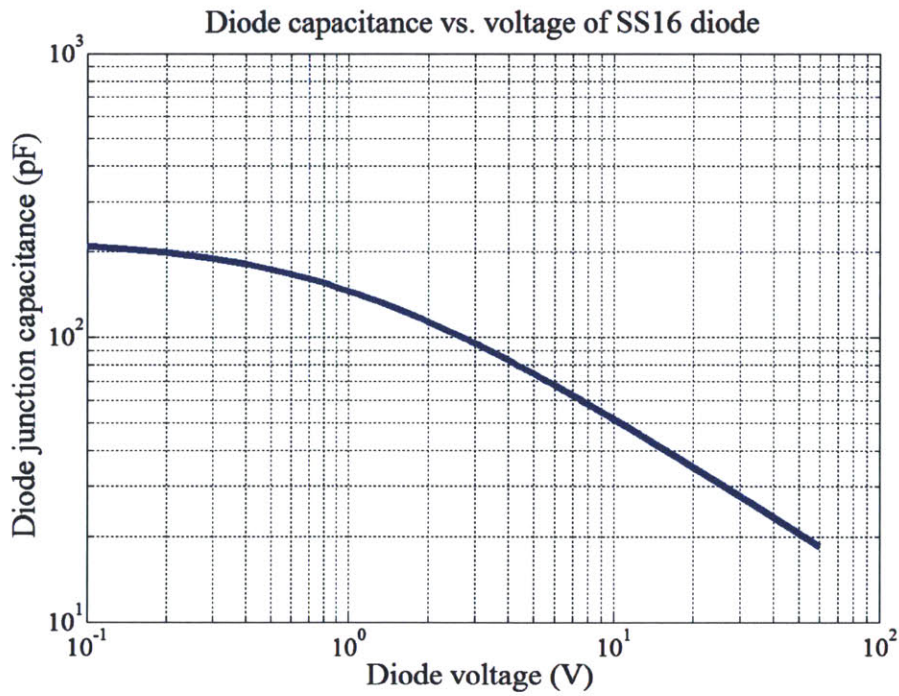


Figure 3.18. Diode junction capacitance vs. diode voltage for an SS16 diode. Plotted from a curve fit to the datasheet C-V plot.

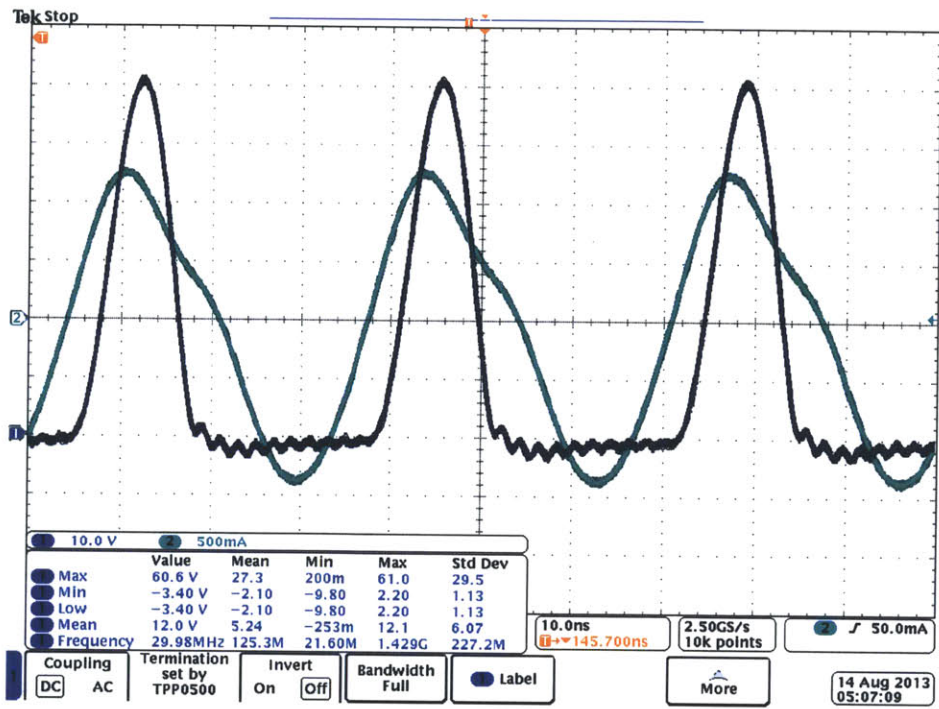


Figure 3.19. Diode voltage (dark blue) and input current (light blue) at full power, 12.77 W for the circuit of Fig. 3.1 and values in table 3.2. The peak diode voltage is 60.6 V.

## Chapter 4: Low Voltage Diode Performance at VHF

As the operating frequency of power conversion circuits increase, the speed of switching devices must increase too. Practical semiconductor switching devices have finite switching speeds as the circuit pumps charge in and out of them. Schottky barrier diodes (SBD), or simply Schottky diodes, are special diodes optimized for use in fast rectification circuits [1,2,35]. These are majority carrier devices with guard rings between the electrodes and semiconductor. Majority carrier devices have little or no reverse recovery effect, improving diode turn-on and turn-off time and decreasing switching losses. Also, the forward voltage drop of the Silicon (Si) Schottky diode is lower than a Si PIN diode. The guard rings increase the reverse breakdown voltage of the diode so that it can handle more stress. Schottky diodes are the most commonly used diode in high frequency rectification circuits, and power rectifiers operating at VHF, UHF and beyond have been built with Si Schottky diodes [4,5,8-11,13,22-24,26, 28-30].

Despite the suitability of some Schottky diodes for operation at very high frequency, it has been observed that while some commercial devices operate very well at VHF, others suffer from extremely high loss [14]. Worse, still, which devices are suitable for VHF operation is not readily determined from device datasheets. This thesis therefore tests a range of devices to identify commercial devices providing good performance. Diode performance will be evaluated based on power dissipated for a given output power level. Measuring ac voltage and current in VHF circuits is very challenging, especially because of the added parasitics or loading effect of the measurement instruments and the high bandwidth needed to capture real circuit responses. These instruments are costly and need careful calibration. In this work a thermal characterization method is adopted to measure diode power dissipation, lowering the difficulty of said measurement.

In the following sections, the performance of commercial low voltage Schottky diodes in VHF frequencies is tested in a resonant rectifier application. We focus on 60 V and 100 V breakdown devices operating at up to a few Amps of current. (Higher power devices are the focus of the next chapter.) The experimental setup is explained and the results are discussed. This chapter seeks to create a library of characterized commercial diodes that are useful for resonant rectification at VHF.

## 4.1 Motivation

In [14], the performance of power Schottky diodes at VHF was explored for the purpose of finding useful diodes for a dc-dc converter incorporating a resonant rectifier. It was found that for many diodes operating at VHF in resonant rectifiers, the loss and temperature rise can be much higher than anticipated based on the datasheet or simulation models. The temperature of the diodes tested rose considerably more sharply than predicted, and the overall circuit losses were much higher, and the diodes had to be substantially derated from their datasheet values to be used at VHF. This phenomenon occurred when driven at high frequencies (75 MHz), but at dc the diodes performed as expected from datasheet values [14]. This presumably reflects the fact that the diodes were designed with the intent for only moderate frequency operation (e.g., of up to a few MHz), consistent with conventional power converter designs.

To try and override this problem, the selected diode in [14] was derated far from its nominal current carrying capacity in order to avoid these high losses, and multiple diodes were placed in parallel to both achieve the required current and spread out the dissipation. This was done at the expense of needing to sustain the capacitance of multiple diodes. This worked, but is undesirable when the goal is to reduce converter size and component count. It was also noted that the deviation from desired behavior was quite diode dependent, with some diodes performing much worse than others. This could be attributed to differences in diode design (including doping profiles, the application of guard rings, etc.), but it is difficult to assess since device details are not publically available.

This chapter investigates a variety of Si Schottky diodes to identify those that perform well at VHF frequencies, and to identify practical current limits of various diodes (for acceptable loss) at these frequencies (This chapter focuses on diodes rated at 60 V and 100 V and up to a few Amps; the following chapter addresses higher voltage diodes, including GaN and SiC Schottky diodes.). A series of experiments are performed on various diodes with different ratings and packaging specifications. Results are included in the thesis as a library of diode characteristics for high frequency rectifiers.

## 4.2 Experimental Setup

The performance of each diode is evaluated based on the percentage of output power dissipated in the diode. Voltage and current waveforms are difficult to measure at VHF, and it is consequently difficult to measure loss through such electrical measurements. In our rectifier topology (see Fig. 4.1) the diode anode is grounded, thus making voltage measurement across the diode a relatively easy task given the correct instruments. On the other hand, measuring current is very challenging in this configuration. Adding a current probe to measure the current through the diode would add too much inductance and disrupt proper operation of the device.

Because of this challenge, we have adopted a thermal characterization approach to measure the losses in the diodes [14]. The diode is placed on the board and a dc current is carried through it. The current is gradually increased in fixed steps and the diode voltage and the temperature of the case of the diode is measured after a settling time of 5 minutes. This provides a case temperature-power loss profile of the diode: a known amount of power is dissipated in the diode and this corresponds to certain diode case temperature rise. Based on this relationship, we can find the losses in the diode when operating in VHF by only measuring the diode case temperature rise. (This does presume that the diode case temperature is not substantially affected by loss in other components. It is believed that this is a good approximation for the test setup.)

All diodes are tested in a class E resonant rectifier [7,13,16] as seen in Fig. 4.1. The VHF diode performance test is conducted by driving the rectifier in steps of 0.2 A of average diode current. The diode case temperature is measured in every step after a settling time of 5 minutes. The experiment continues until any one of three things happens: (i) case temperature rise exceeds 45°C, (ii) reverse diode voltage exceeds the rated value, or (iii) diode average current exceeds the datasheet rated value. Table 4.1 shows the list of diodes to be tested, their ratings and the junction capacitance at the average diode voltage (i.e., 12 V, which is the output voltage of the class E rectifier). This capacitance value is used to represent the non-linear diode capacitance with a constant value for ease of design. This value is obtained from the diode's C-V curve in its datasheet.

The rectifier is designed such that the components used are the same for all diodes for a given frequency. This way, the diodes will have similar voltage and current waveforms and the

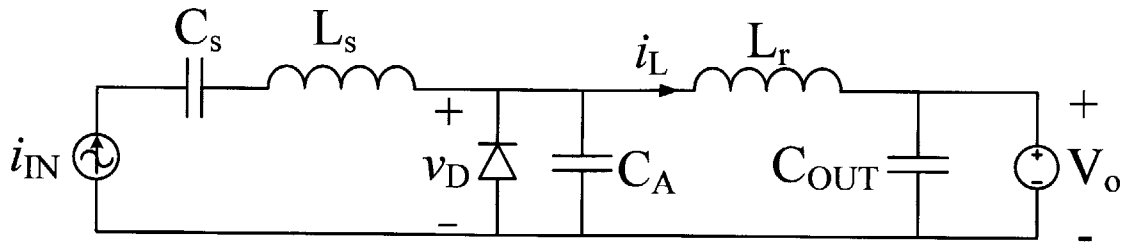


Figure 4.1. Class E rectifier used to test the performance of low voltage diodes in VHF rectification.

diode dissipation would be independent of the circuit parameters. The additional capacitance in the rectifier  $C_A$  was chosen to be 200 pF and is fixed for all diodes, independent of the junction capacitance. The variation in diode junction capacitance among devices, and differences in diode capacitance nonlinearity with voltage had little impact on the performance of the diode. As an example, the MSS1P6 (27 pF at 12 V) has a peak reverse voltage of 59.3 V at 1 A of average current while the PMEG6030EP (105 pF at 12 V) has 56 V of peak reverse voltage at the same current in the rectifier. This shows that both diodes have a few volts of variation in peak reverse voltage while delivering the same current. Thus we can safely assume the effect of the difference in junction capacitance among devices is negligible, owing to the fact that the large external capacitor  $C_A$  substantially swamps the differences.

The diodes were tested operating at four frequencies: 30 MHz, 50 MHz, 75 MHz, and 100 MHz. The rectifiers were designed based on the PMEG6020EPA diode following the methodology described in chapter 2 for 5:1 power range ratio. The capacitance  $C_A$  was fixed across all diodes and for all frequencies at 200 pF. The inductance was selected appropriately for each frequency (based on the PMEG6020EPA diode, which has an intrinsic capacitance of 80 pF at 12 V). The input filter was designed to resonate at the operating frequency with a Q factor of 8 (with effective load resistance of  $V_o^2/P_{O,max}$ ) for high input current purity. Table 4.2 summarizes the rectifier parameters and Fig. 4.2 shows the rectifier board. Note that the LC input filter is off board. The board schematic and layout are shown in appendix B, Figs. B.3 and B.4. The experiments conducted here thus compare the performance of diodes in a particular rectifier circuit, as described above. However, it is believed that their performance in this circuit well reflects their relative suitability across a wide range of VHF rectifier designs.

Table 4.1. Diodes to be tested and their respective junction capacitance (evaluated at a bias voltage of 12 V).

<b>Diode</b>	<b>Rating</b>	<b>Capacitance</b>
PMEG6020EPA	60 V, 2 A	80 pF
10MQ100	100 V, 1 A	20 pF
S100	100 V, 1 A	67 pF
SS16	60 V, 1 A	47 pF
STPS1H100A	100 V, 1 A	36 pF
PMEG6030EP	60 V, 3 A	105 pF
MSS1P6	60 V, 1A	27 pF

Table 4.2. Rectifier circuit parameters

<b>Parameter</b>	<b>30 MHz</b>	<b>50 MHz</b>	<b>75 MHz</b>	<b>100 MHz</b>
$L_S$	265 nH	160 nH	106 nH	80 nH
$C_S$	100 pF	64 pF	42 pF	32 pF
$C_A$	200 pF	200 pF	200 pF	200 pF
$L_r$	62 nH	22 nH	10 nH	5 nH
$C_{OUT}$	20 uF	20 uF	20 uF	20 uF
$V_o$	12 V	12 V	12 V	12 V

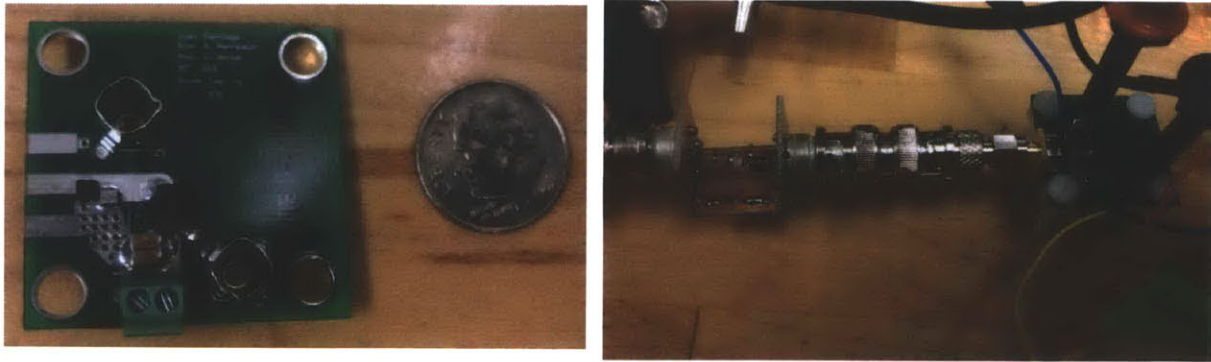


Figure 4.2. Class E rectifier used to test the performance of low power diodes in VHF rectification. On the left is the rectifier board with a dime for size scale. On the right is the rectifier board with the input LC filter off board.

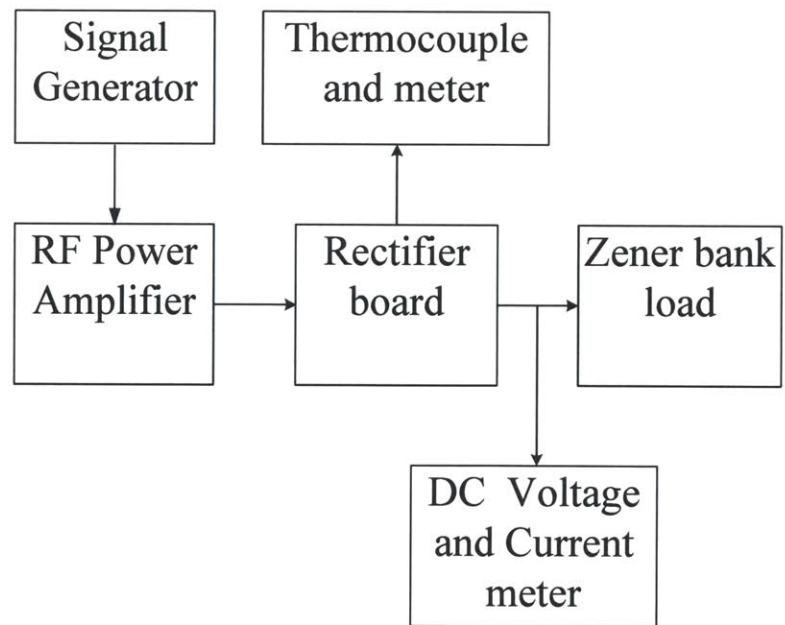


Figure 4.3. Experimental setup block diagram.



Fig. 4.4. On the left: (a) Signal generator and power amplifier. On the right: (b) Zener load and heatsink.

Figure 4.3 shows a block diagram of the experimental setup for diode testing. The signal generator (BK Precision 4087) is connected to a radio frequency (RF) power amplifier (AR 150A100B) and drives the resonant rectifier. Both instruments are shown in Fig. 4.4a. The rectifier is loaded by a zener bank load (10x SMBJ5349B in parallel) that maintains the dc output voltage approximately constant over the power range, shown in Fig. 4.4b. A K-type thermocouple is placed over the case of the diode and it's connected to a thermometer (Digi-Sense Scanning Thermometer). Output dc voltage and current are also measured with multimeters (Agilent U3606A and 34401A). The following section has the results of the diode testing.

### 4.3 Results

Presented here are the results of testing on the seven diodes listed in Table 4.1. All seven devices are Schottky barrier diodes (SBD). Figures 4.5 to 4.16 show the losses of each diode as a function of average diode current for the operating frequencies of 30 MHz, 50 MHz, 75 MHz and 100 MHz, respectively. The losses are presented in two ways: diode power dissipation and the dissipation as a percentage of output power. The latter representation is useful because not all diodes have the same ratings and thus each circuit has different achievable output power. The legend on the plots has the part number, manufacturer and rating of each diode. The four 60 V devices performed substantially better than the 100 V devices (at a dc output voltage of 12 V, which was within the operating range of both 60 V and 100 V devices). At 30 MHz, the best

diode is NXP's PMEG6030EP because it has the least losses for a wide current range. At 50 MHz the PMEG6020EPA proved to be the best with the least losses over the entire current range. The 75 MHz and 100 MHz tests show an outstanding performance from both Vishay's SS16 and the PMEG6020EPA. Figure 4.17 shows the diode dissipation at maximum power as a function of frequency for the 60 V diodes. The plot shows a clear increase in losses proportional to frequency. Appendix C shows the complete data gathered from the diode testing.

Figure 4.18 shows a sample waveform for illustration purposes. This is the diode voltage waveform of the SS16 diode operating in the test circuit at 50 MHz. During conduction time there is a ringing caused by the inductance of the diode package. Figure 4.19 shows the SPICE model of the diode, which consists of an ideal diode, junction capacitance and package inductance. Figure 4.20 shows the results of the simulation which are in good agreement with the experimental waveform.

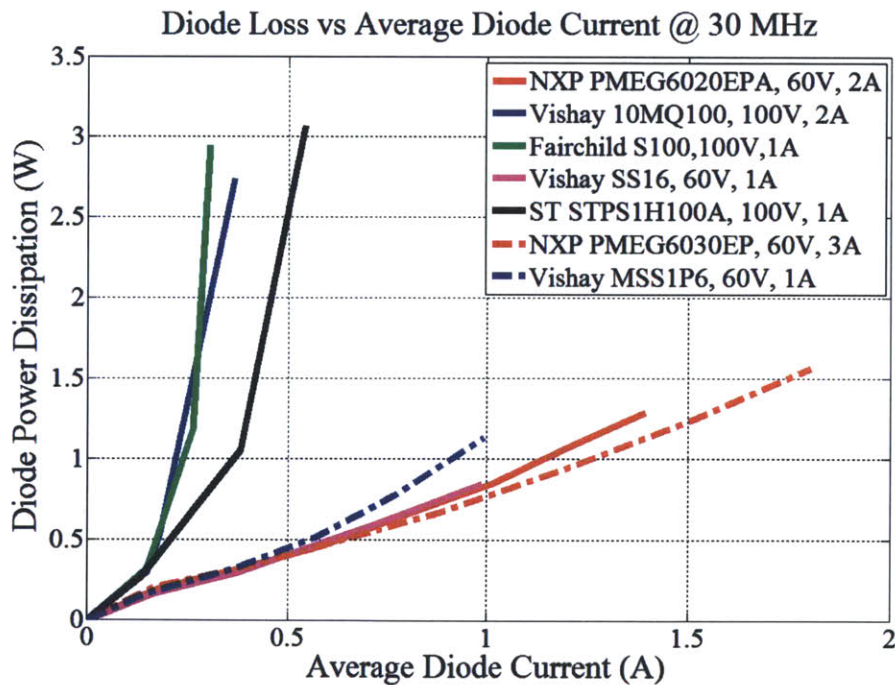


Figure 4.5. Diode power dissipation vs. average diode current for different diodes at 30 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 30 MHz

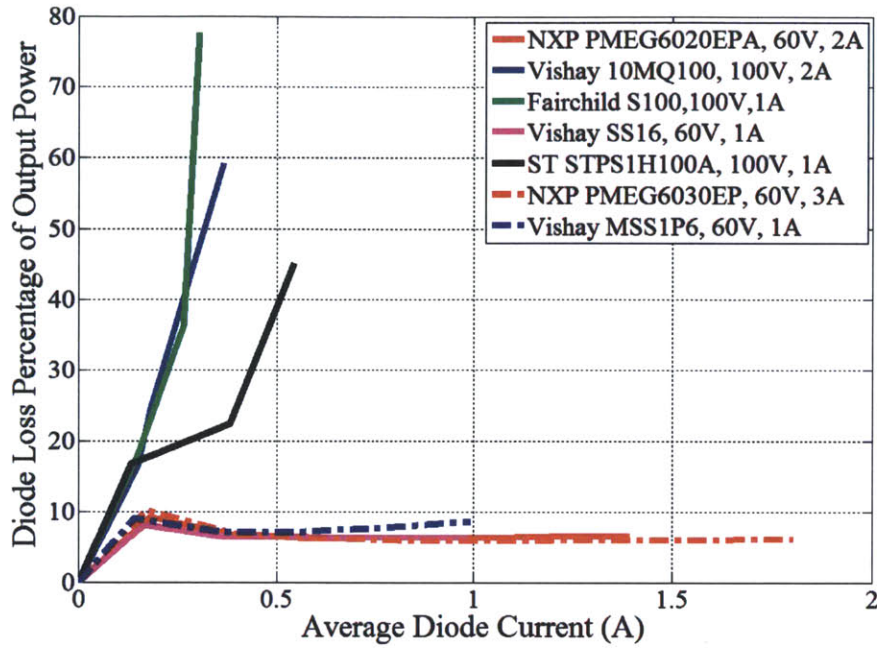


Figure 4.6. Diode loss percentage of output power vs average diode current for different diodes at 30 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 30 MHz

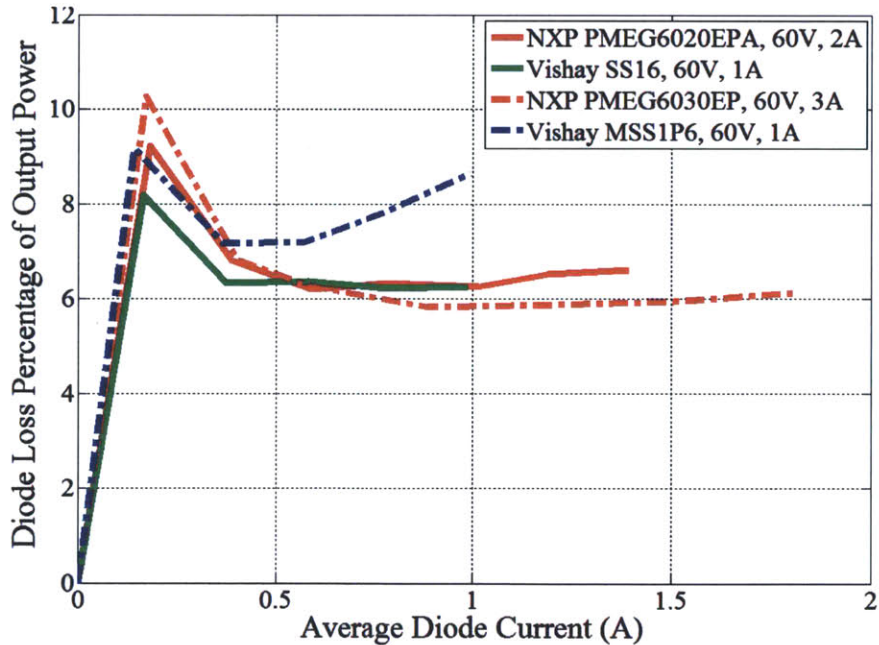


Figure 4.7. Diode loss percentage of output power vs average diode current for different diodes at 30 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V. This chart shows a zoomed-in view of the performance of the 60 V diodes.

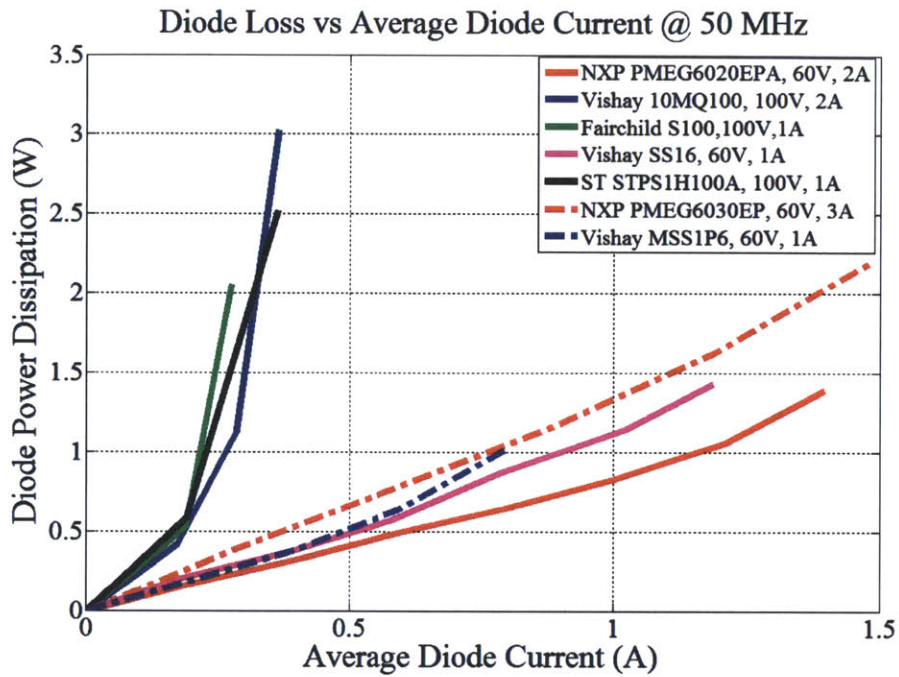


Figure 4.8. Diode power dissipation vs. average diode current for different diodes at 50 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

### Diode Loss Percentage of Output Power vs. Average Diode Current @ 50 MHz

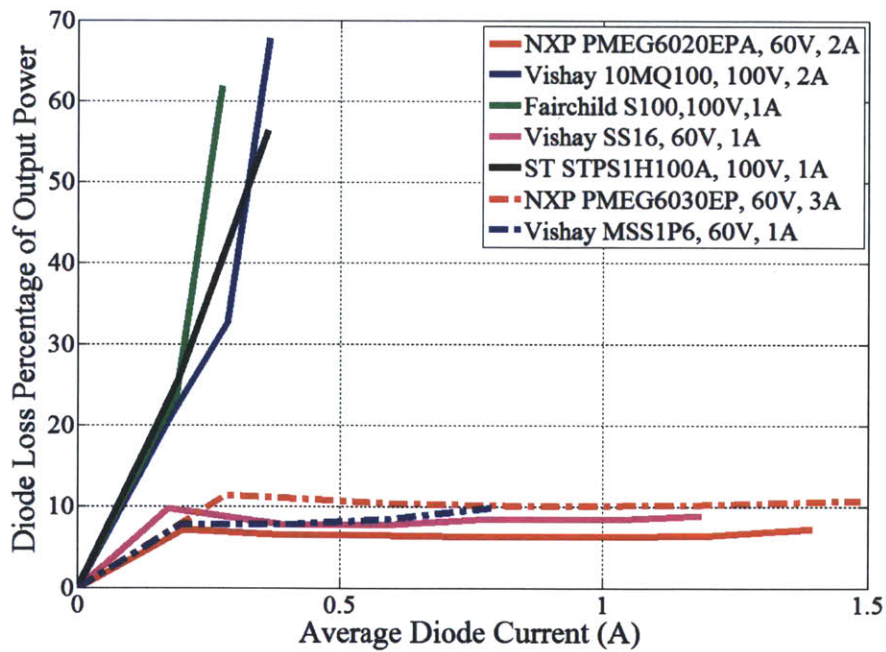


Figure 4.9. Diode loss percentage of output power vs average diode current for different diodes at 50 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 50 MHz

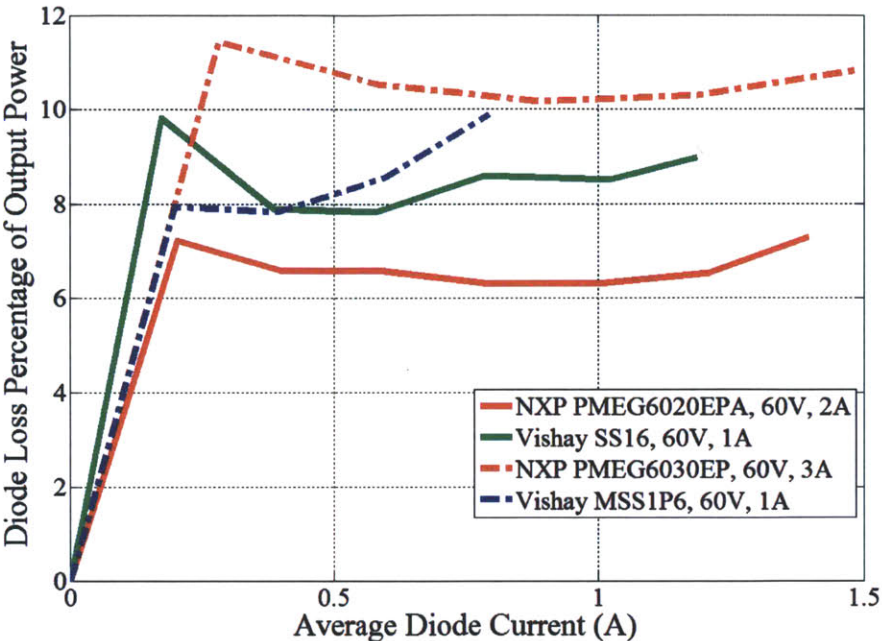


Figure 4.10. Diode loss percentage of output power vs average diode current for different diodes at 50 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V. This chart shows a zoomed-in view of the performance of the 60 V diodes.

Diode Loss vs Average Diode Current @ 75 MHz

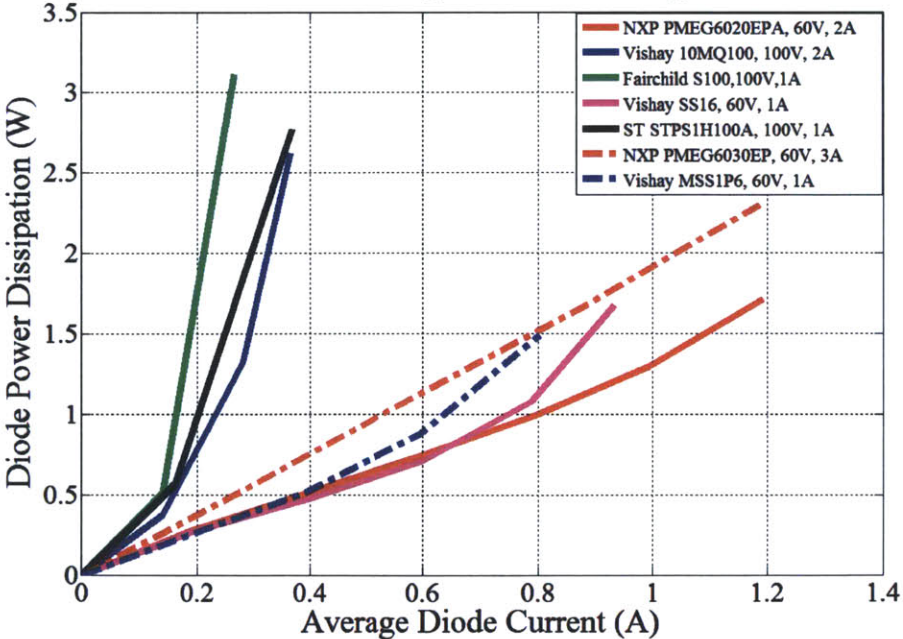


Figure 4.11. Diode power dissipation vs. average diode current for different diodes at 75 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 75 MHz

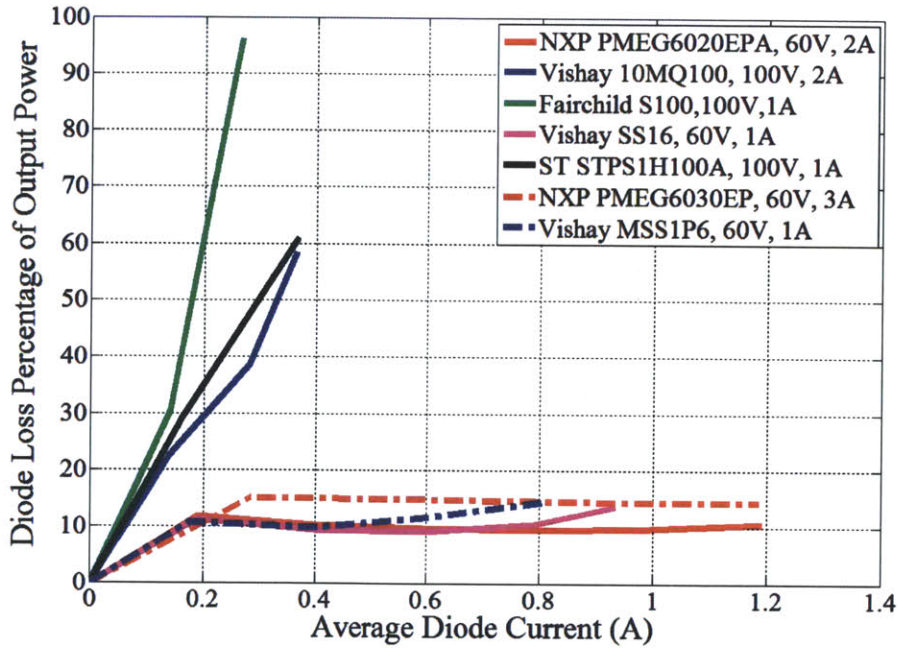


Figure 4.12. Diode loss percentage of output power vs average diode current for different diodes at 75 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 75 MHz

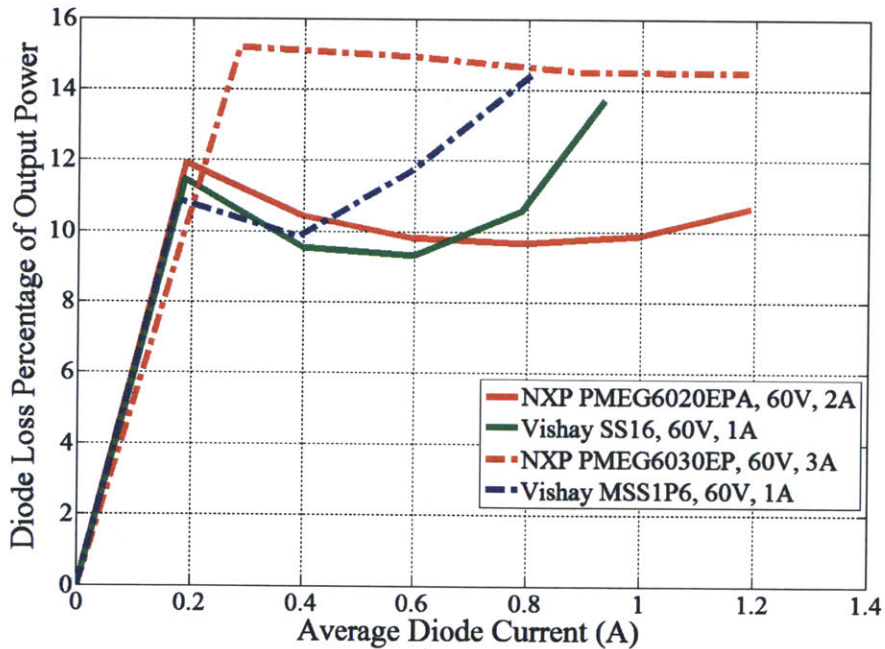


Figure 4.13. Diode loss percentage of output power vs average diode current for different diodes at 75 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V. This chart shows a zoomed-in view of the performance of the 60 V diodes.

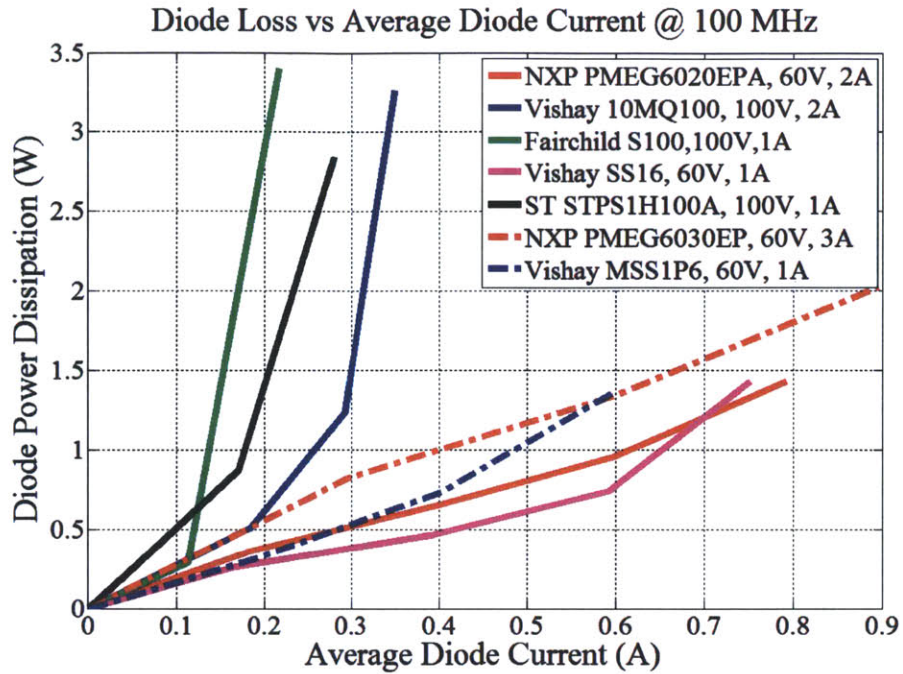


Figure 4.14. Diode power dissipation vs. average diode current for different diodes at 100 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 100 MHz

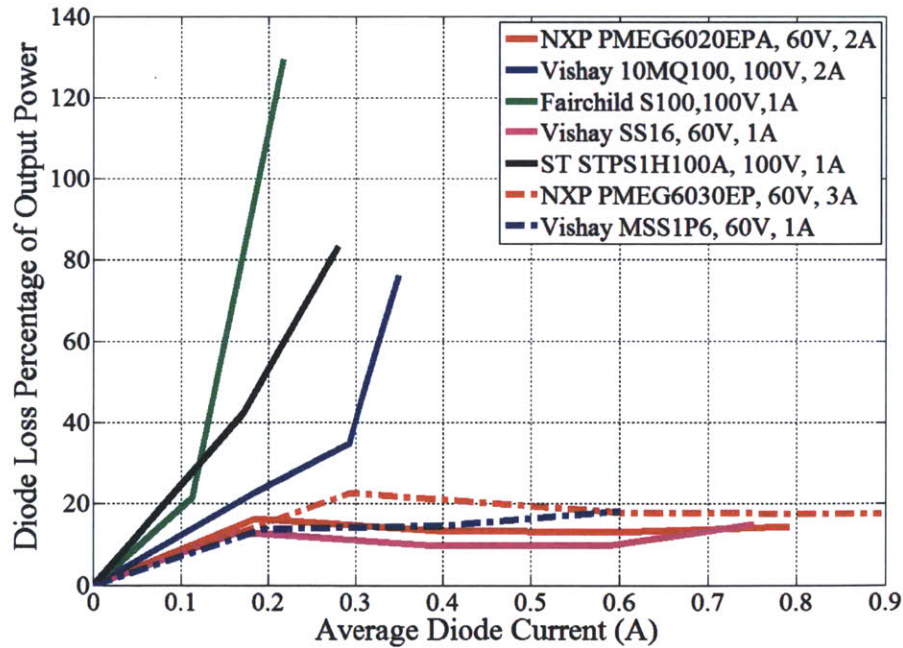


Figure 4.15. Diode loss percentage of output power vs average diode current for different diodes at 100 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

Diode Loss Percentage of Output Power vs. Average Diode Current @ 100 MHz

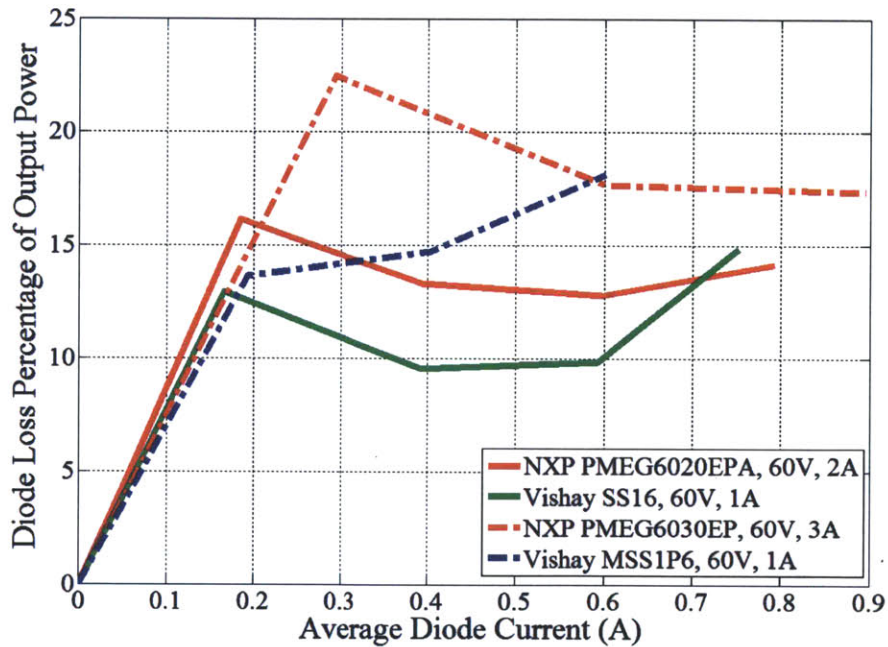


Figure 4.16. Diode loss percentage of output power vs average diode current for different diodes at 100 MHz as tested in a class E resonant rectifier circuit with an output voltage of 12 V. This chart shows a zoomed-in view of the performance of the 60 V diodes.

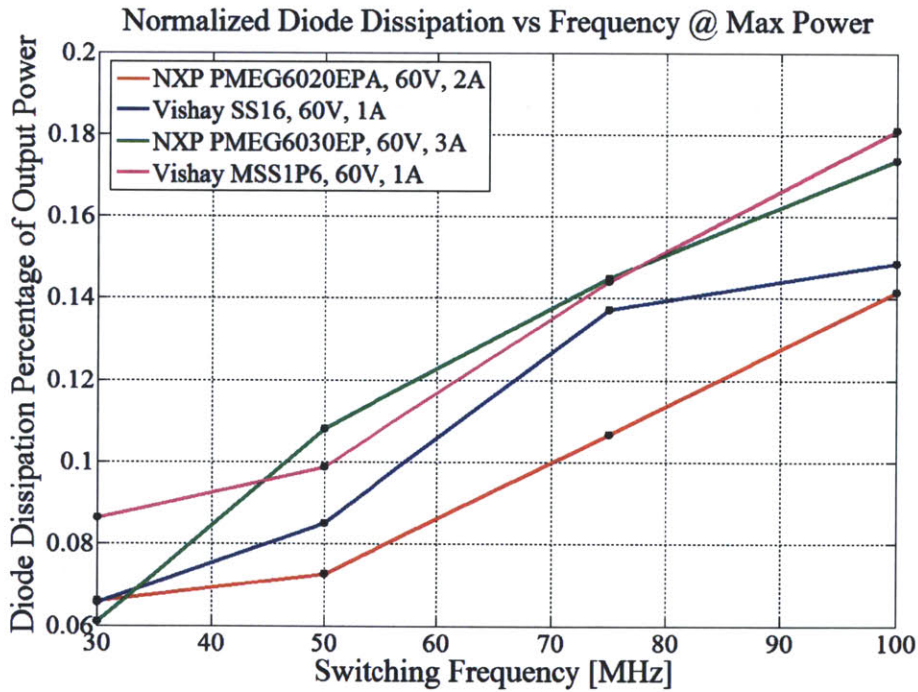


Figure 4.17. Diode loss percentage of output maximum power vs frequency for the 60 V diodes as tested in a class E resonant rectifier circuit with an output voltage of 12 V.

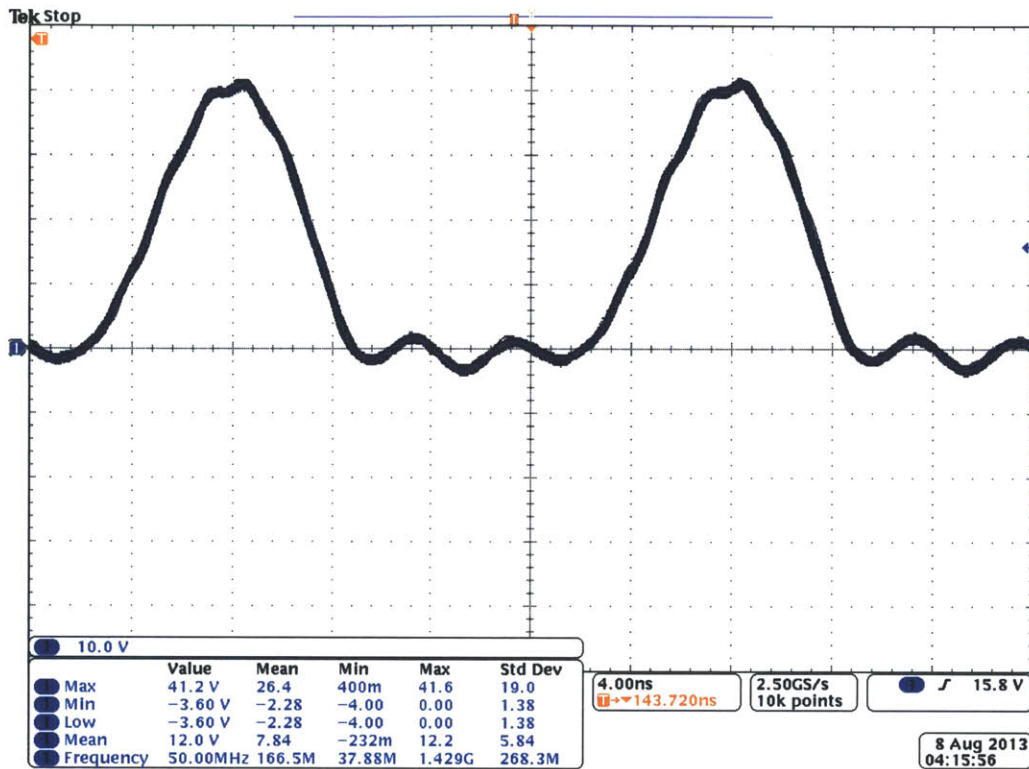


Figure 4.18. Diode voltage waveform at 50 MHz and 12.76 W output power for the Class E rectifier. The rectifier parameters were  $L_s=160$  nH,  $C_s=64$  pF,  $C_A=200$  pF, and  $L_r=22$  nH. The diode used is the SS16.

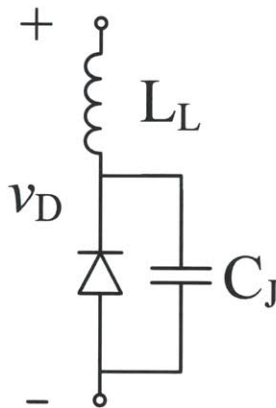


Figure 4.19. Spice model of the SS16 diode. The simplified model includes a lead inductance  $L_L(1$  nH), a (constant) junction capacitance  $C_J(47$  pF) (linear), and an ideal diode.

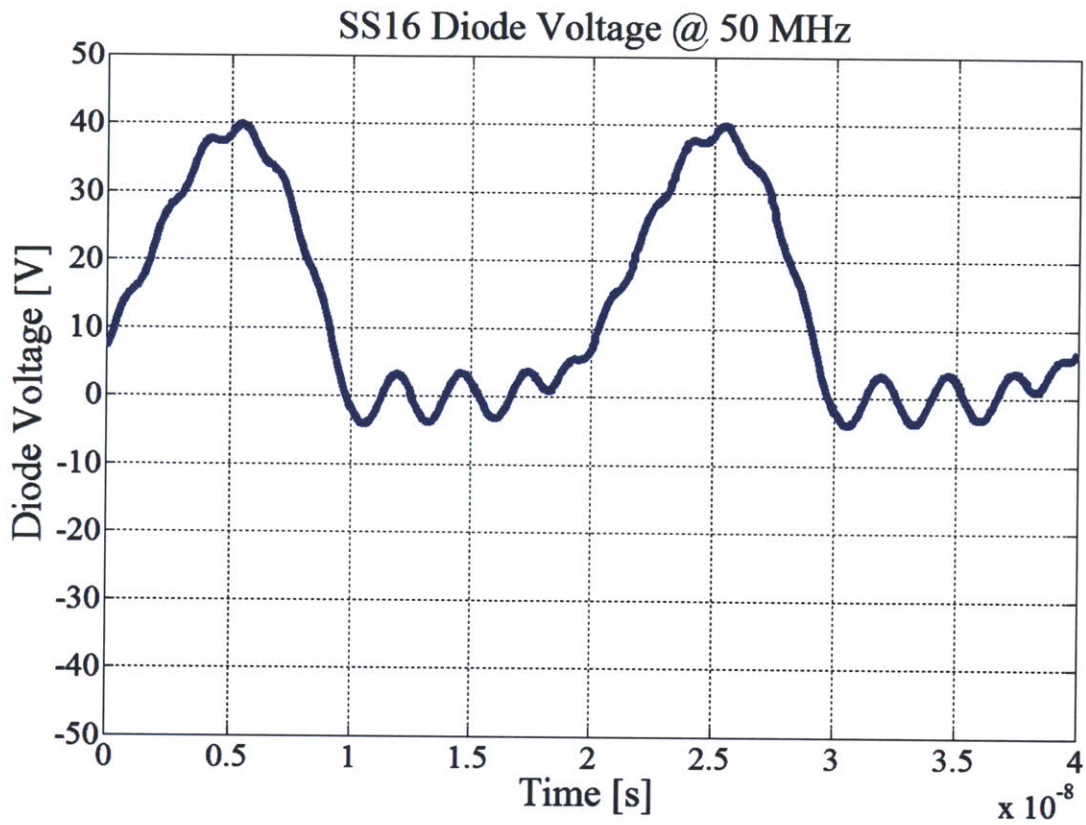


Fig. 4.20. Spice simulation of diode voltage including junction capacitance and lead and bondwire inductance.

## Chapter 5: High Voltage Diode Performance at VHF

In the previous chapter we studied the performance of Si Schottky diodes in very high frequency (VHF) resonant rectification (30-300 MHz). It has been found that some diodes do not perform as models predict when operating at VHF frequencies [14]. Although the loss mechanisms have not as yet been accurately identified, effort has been made to identify some commercially available diodes that are useful for this application. We have setup an experiment to test several diodes in a resonant rectifier application. So far we have studied the performance of low voltage diodes (60-100V). In this chapter we extend our studies to high voltage devices (600 V).

In the following sections, the performance of high voltage Schottky diodes in VHF frequencies is tested in a resonant rectifier application. The focus is on Schottky diodes in Wide Bandgap Material Systems (SiC and GaN). The experimental setup is explained and the results are discussed. This work is a contribution to the creation of a library of commercial diodes that are useful in VHF rectification.

### 5.1 Motivation

This work is an extension of the efforts described in the previous chapter. Diode performance is evaluated based on percentage of output power dissipated in the diode as a function of average diode current in a class E resonant rectifier. Measuring voltage and current in VHF circuits is very challenging, especially because of the added parasitics or loading effect of the measurement instruments and the high bandwidth needed to capture real circuit responses. These instruments are costly and need careful calibration. In this work a thermal characterization method is adopted to measure the diode's power dissipation, lowering the difficulty of said measurement.

A full knowledge of the device capacitance is needed to properly design the rectifier. In this chapter, we test both commercial SiC Schottky diodes and experimental GaN Schottky diodes developed by a commercial device manufacturer. As complete data for the experimental devices was not available, they were characterized prior to use. We have measured the capacitance of the experimental diodes to obtain accurate capacitance and voltage characteristics.

A special setup was designed to measure the capacitance-voltage relationship at voltages up to 400 V using an impedance analyzer.

Diodes of different types and from different manufacturers have been tested. These include four GaN SBD (Schottky barrier diode), four SiC SBD and four Si FRD (fast recovery diodes). All diodes are tested with the same circuit and board and similar device packages so that each one has similar circuit losses, heat sinking properties and parasitics. Useful results were obtained from eight of these diodes.

## 5.2 Diode Capacitance Measurement

In this section we describe the method for measuring diode capacitance across a wide voltage range. The components in circuits operating in VHF usually are small and their values are comparable to device parasitics or parasitics caused by the circuit board. This means circuit board layout and component selection are a very important part of designing resonant circuits that often need to be tuned at one frequency for proper operation. Thus, it is important to characterize the diodes for their intrinsic capacitance and package inductance values. The commercial diodes evaluated in this work had datasheets with capacitance data and came packaged in industry standard TO-220 package. The experimental GaN diodes had to be measured to experimentally acquire the junction capacitance values at the voltage values of interest.

The impedance analyzer utilized here (Agilent 4395A) has an input voltage limit of 45 V, but the diodes under test are 600 V devices. A small circuit was designed to measure the diode capacitance at voltages up to 400 V. Figure 5.1 shows the diode capacitance measurement circuit schematic. The dc voltage source is connected in series with a large-valued resistor ( $>1 \text{ M}\Omega$ ) and the impedance analyzer is coupled to the diode through a large-valued series capacitor ( $\sim 1 \text{ }\mu\text{F}$ , ceramic). This circuit is best described as two separate circuits: a dc equivalent circuit and an ac one.

Figure 5.2a shows the dc equivalent circuit. The dc supply charges capacitance  $C_{\text{BIG}}$  and reverse biases the diode. The capacitance  $C_{\text{BIG}}$  looks like an open circuit at dc and protects the impedance analyzer from the high voltage from the supply. The ac equivalent of the circuit is

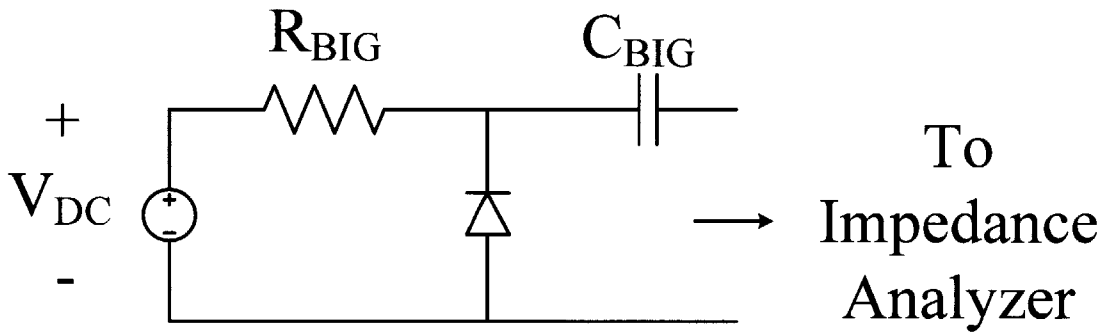


Fig. 5.1. Capacitance measurement circuit schematic. In the system,  $R_{BIG} = 10 \text{ M}\Omega$ , and  $C_{BIG} = 1 \text{ }\mu\text{F}$ .  $C_{BIG}$  was a ceramic capacitor.

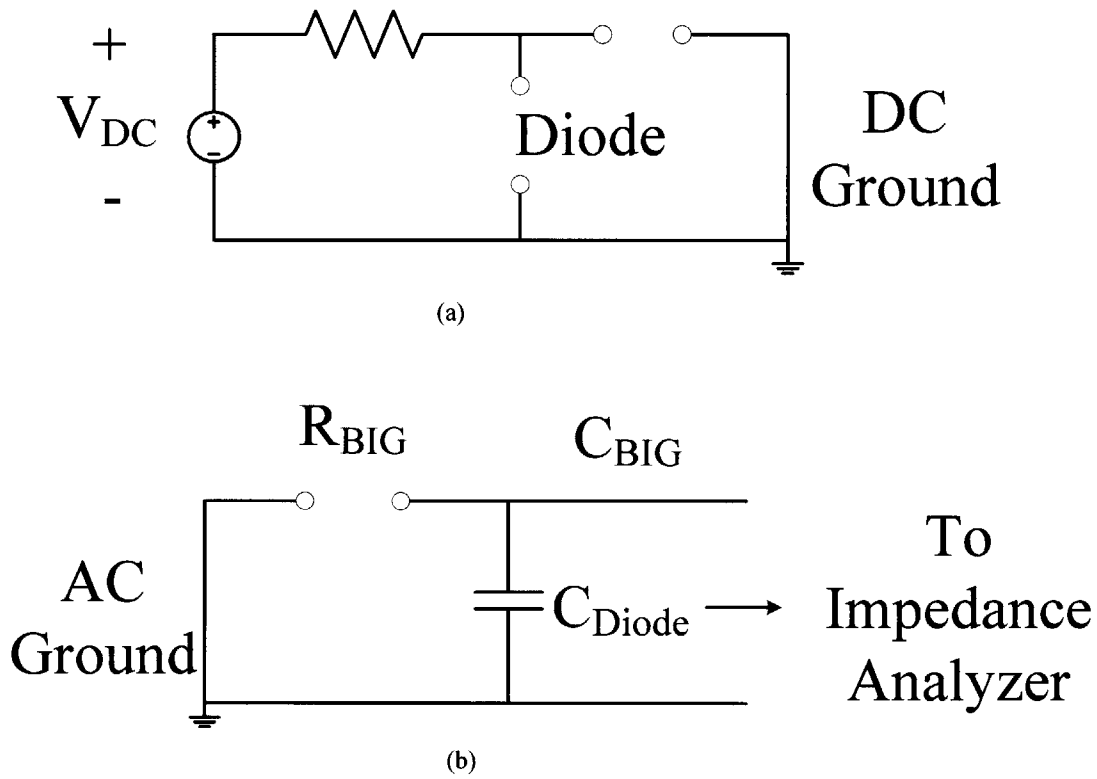


Fig. 5.2. Capacitance measurement circuit equivalent models. From the top: (a) dc equivalent circuit and (b) ac equivalent circuit.

shown in Fig. 5.2b. The resistor  $R_{\text{BIG}}$  behaves like high impedance to the ac source (the impedance analyzer) and looks like an open circuit. Resistor  $R_{\text{BIG}}$  has to be selected to have high resistance ( $>1 \text{ M}\Omega$ ). The capacitance  $C_{\text{BIG}}$  behaves like a short circuit for high frequency signals. It is important that  $C_{\text{BIG}}$  is selected several order of magnitudes bigger than the maximum capacitance of the diode (which is usually in the hundreds of picofarads range). The impedance analyzer will see the series equivalent of capacitor  $C_{\text{BIG}}$  and the capacitance of the diode and, if  $C_{\text{BIG}}$  is high enough, the analyzer will only measure the diode capacitance. The capacitance measurement is repeated for various values of dc voltage starting from zero, with small steps during the first 20 V and then bigger steps are made until a 400 V bias is reached. The capacitance testing results for the experimental diodes are provided in Appendix C.3.

### 5.3 Diode Performance Measurement

This section describes the diode testing procedure. All diodes are tested in a class E resonant rectifier, as shown in Fig. 5.3<sup>3</sup>. The performance of each diode is evaluated based on the percent of diode power dissipation normalized to output power. Electrical waveforms in VHF are very difficult to measure. As stated in the previous chapter, in this topology the diode anode is grounded thus making voltage measurement across the diode a relatively easy task given the correct instruments. On the other hand, measuring current is very challenging in this configuration. Adding a current probe to measure the current through the diode would add too much inductance and disrupt proper operation of the device. Because of this challenge, we have adopted a thermal characterization approach to measure the losses on the diode [14]. The diode is placed on the board, with its appropriate heatsink, and a dc current is applied to it. The current is gradually increased in fixed steps and the temperature of the case of the diode is measured after a settling time of 5 minutes. This provides a case temperature-power loss profile of the diode: a known amount of power is dissipated on the diode and this corresponds to certain diode case temperature rise. Using this relationship now we can find the losses on the diode when operating in VHF by only measuring the diode case temperature rise.

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<sup>3</sup> No external capacitance is added to the diode in order to maximize device stress during the test.

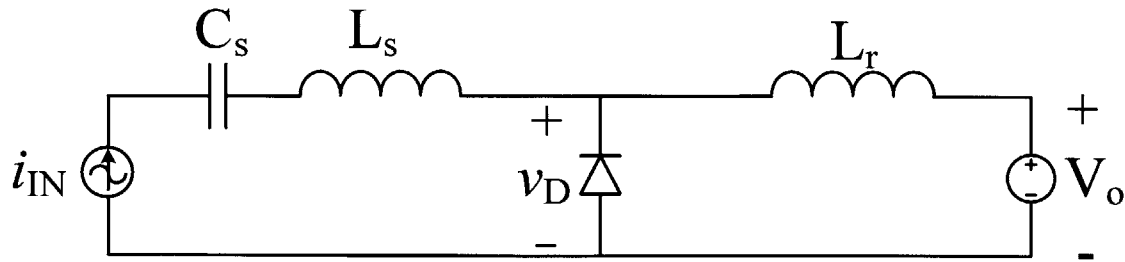


Fig. 5.3. Class E resonant rectifier circuit schematic

The VHF diode performance test is performed over a 10:1 output power range ratio with the output voltage held constant. The output power is increased in fixed steps and the diode case temperature is recorded after a settling time of 5 minutes. In the following section the experimental setup is explained in detail

## 5.4 Experimental Setup

### 5.4.1 Capacitance Measurement

The capacitance measurement circuit is shown in Fig. 5.4. The resistor used is a 10 M $\Omega$  resistor, and the blocking capacitance was 0.5  $\mu$ F (consisting of 4 ceramic capacitors rated at 250 V). The circuit connects to the impedance analyzer (Agilent 4395A) via the two lower copper traces, one connected to one plate of the diode bank and the other to the anode of the diode. The copper traces connect directly to the clamps of the analyzer connection fixture making a low inductance connection with the analyzer port. The external wires connect to the high voltage power supply. The four GaN-SBD experimental diodes were characterized with this circuit.

### 5.4.2 Diode Performance

The diodes were tested in a class E resonant rectifier; the schematic is shown in Fig. 5.3. The rectifier was built following the methodology described in chapter 2. The circuit parameters are input frequency of 30 MHz, 60 V output dc voltage, and 10:1 output power range with maximum power of 60 W. The input L-C filter is tuned at 30 MHz with a Q factor of 3. The filter consists of a MAXI spring air core inductor from Coilcraft of 307 nH ( $L_s$ ) and a 91pF

ceramic capacitor from ATC ( $C_S$ ). Table 5.1 shows the eight diodes tested and their capacitance at the diode average voltage. The capacitance data on the GaN devices was obtained from direct measurements, while the data from the commercial devices was obtained from the manufacturer's datasheet.

In this performance test, we wanted to compare all the diodes using the same circuit to generate similar loss profiles in each case. First, no external capacitance is added to the diode. This condition provides the highest voltage stress possible on the diode and minimizes the shunt capacitance. The GaN-SBD C was used as the base design, and it has a nominal capacitance  $C_r$  of 60 pF. For this capacitance the appropriate value of inductance  $L_r$  was 422nH. It was implemented using another MAXI spring air core inductor. An output capacitor is placed with a capacitance of 4.4  $\mu$ F (TDK, 100V, ceramic) to help stabilize the output voltage. The circuit parameters are summarized in Table 5.2. The rectifier is shown in Fig. 5.5.

Figure 5.6 shows a block diagram of the experimental setup for the diode testing procedure. The signal generator (BK Precision 4087) is connected to the radio frequency (RF) power amplifier (ar 150A100B) and drives the resonant rectifier, shown on Fig. 5.7a. The rectifier is loaded by a zener bank load (20x SMBJ5371B in parallel) that maintains the voltage approximately constant at 60 V over the power range (see Fig. 5.7b). A K-type thermocouple is placed over the case of the diode and it is connected to a thermometer (Digi-Sense Scanning Thermometer). Output dc voltage and current are also measured with multimeters (Agilent U3606A and 34401A). The following section has the results of the diode testing.



Fig. 5.4. Capacitance measurement circuit. GaN-SBD D is in place.

Table 5.1. Diodes tested in class E rectifier and their capacitance at diode average voltage. All diodes rated at 500 V.

<b>Diode</b>	<b>Capacitance @ 60 V</b>
GaN-SBD A	36 pF
GaN-SBD B	33 pF
GaN-SBD C	60 pF
CREE C3D04060A (SiC)	37 pF
ST Micro STPSC606D (SiC)	57 pF
ROHM SCS106AG (SiC)	52 pF
Infineon IDH12SG60C (SiC)	75 pF
Power Integrations QH05TZ600 (Si)	8 pF

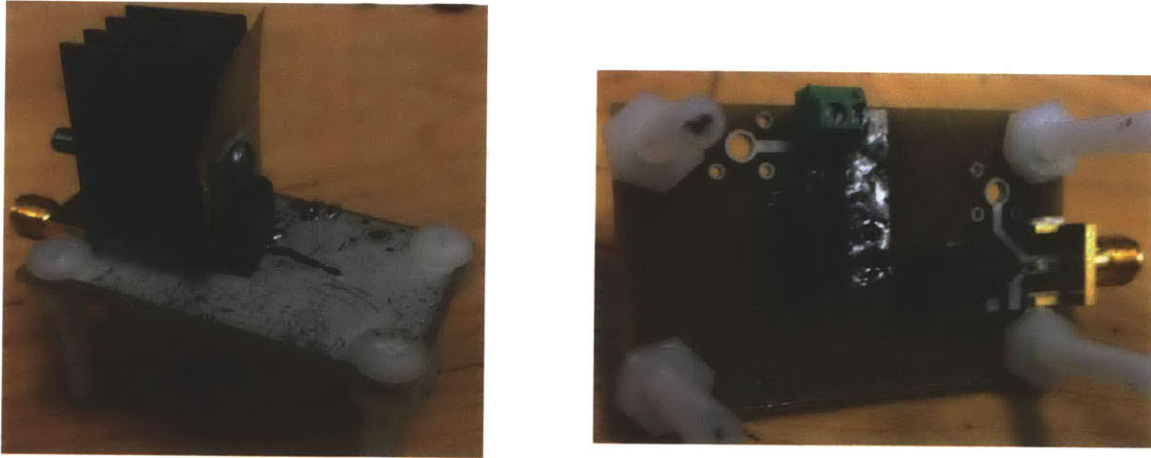


Fig. 5.5. Class E resonant rectifier circuit. The left picture shows the rectifier board with the TO-220 package diode and its heatsink. On the right the underside of the board is shown. This board was designed for through-hole devices. The diode leads were cut to reduce inductance.

Table 5.2. Rectifier circuit parameters

Parameter	Value
$f_{in}$	30 MHz
$V_O$	60 V
$P_{O, max}$	60 W
$L_r$	422 nH
$L_s$	307 nH
$C_s$	91 pF
$C_{OUT}$	4.4uF

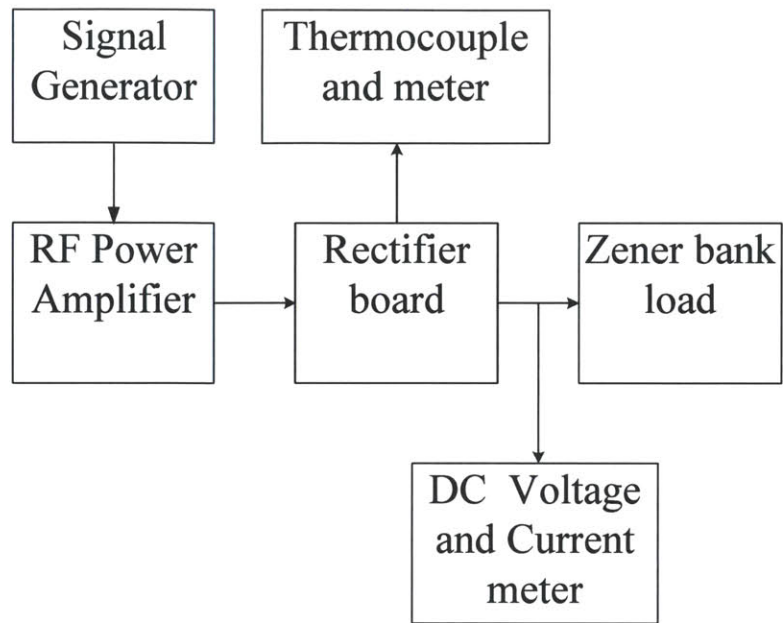


Fig. 5.6. Experimental setup block diagram

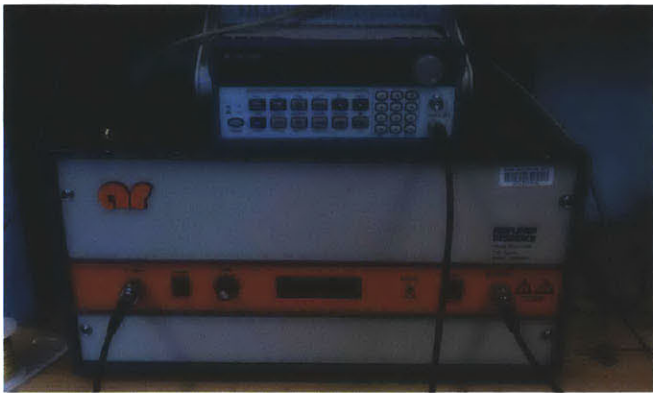


Fig. 5.7. On the left: (a) Signal generator and power amplifier. On the right: (b) Zener load and heatsink.

## 5.5 Results

### 5.5.1 Capacitance Measurement

The four GaN-SBD diodes (named 'A' through 'D'), nominally rated for 600 V and 5 A, were tested for their intrinsic capacitance voltage (C-V) dependence. All four diodes were tested from 0 to 400 V. In typical diode C-V curves, the change in capacitance is very sharp at low voltages and slowly asymptotes to a low value of capacitance as the voltage increases. Because of this behavior, many points with small voltage steps were taken during low voltage (from 0 to 20 V) to capture the characteristics while at higher voltages the steps were larger because of small changes in capacitance. Figures 5.8-5.11 show the C-V curves for the diodes A, B, C and D, respectively.

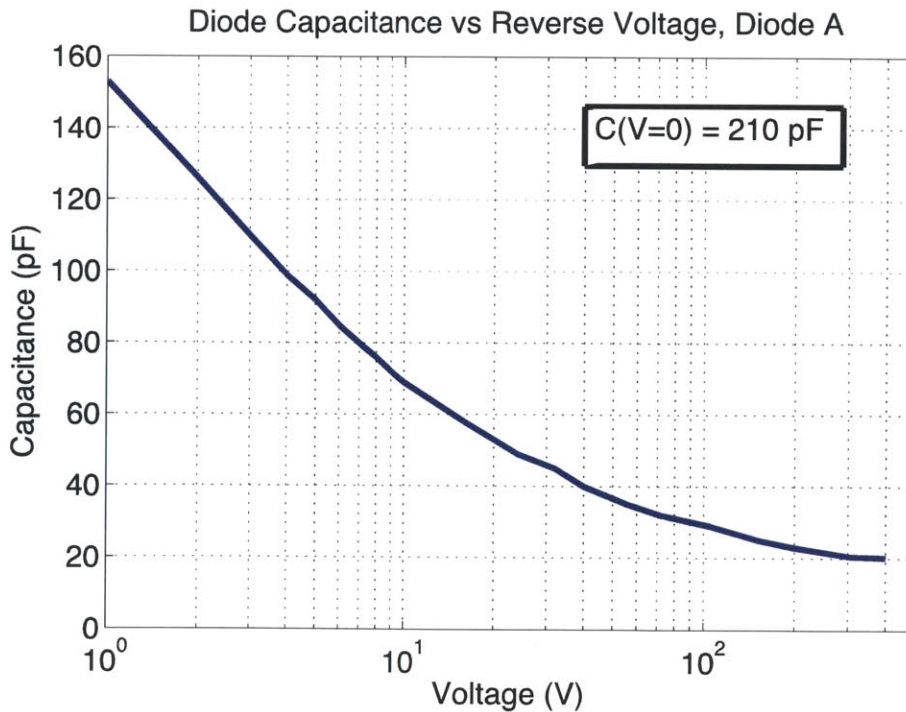


Fig. 5.8. Capacitance vs. reverse voltage curve of GaN-SBD diode A

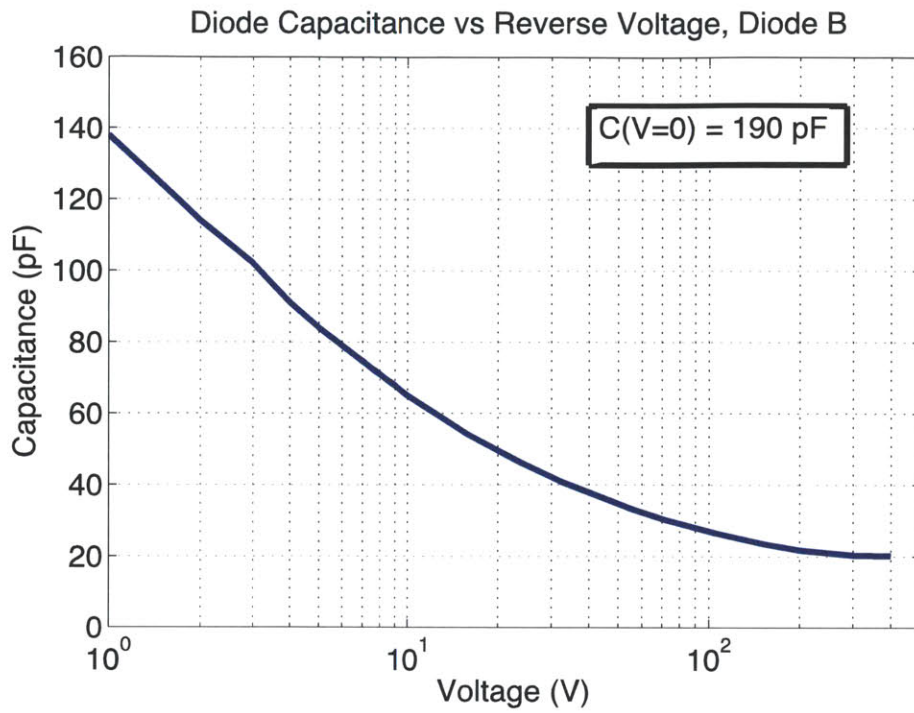


Fig. 5.9. Capacitance vs. reverse voltage curve of GaN-SBD diode B

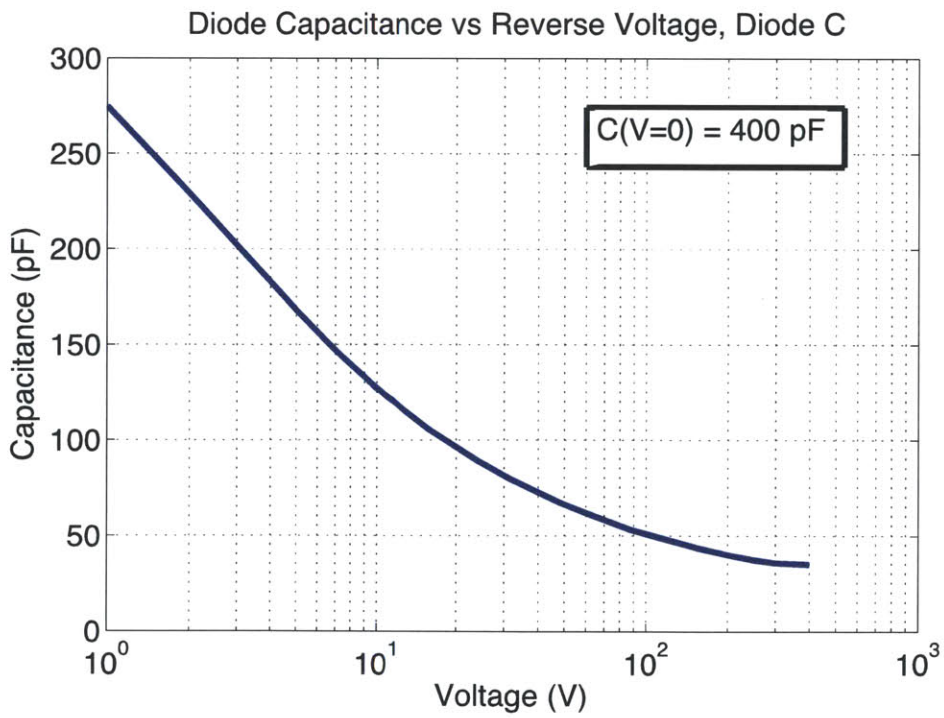


Fig. 5.10. Capacitance vs. reverse voltage curve of GaN-SBD diode C

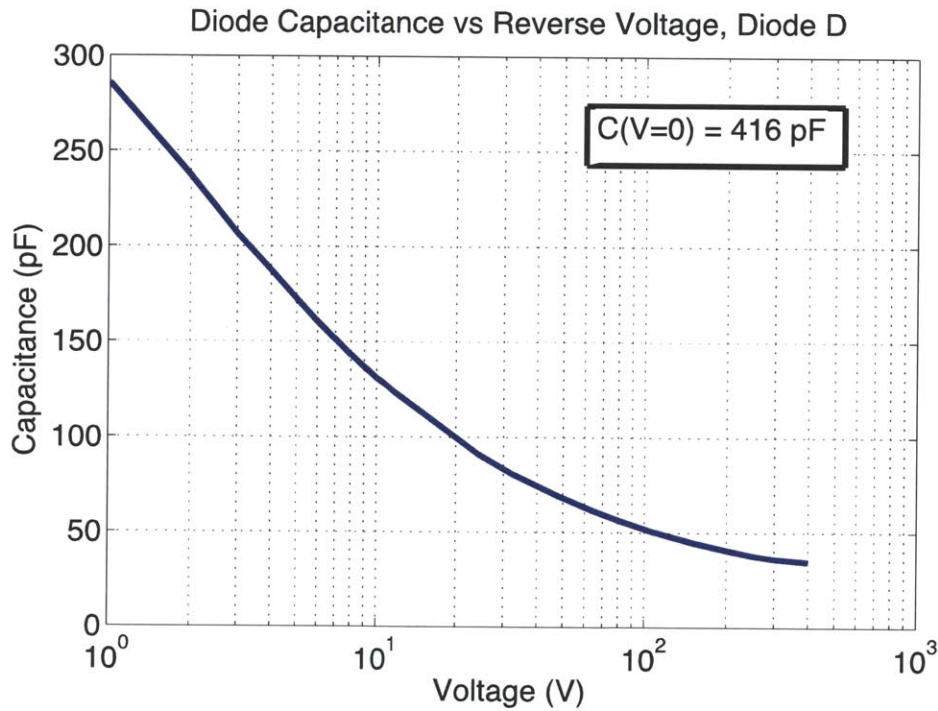


Fig. 5.11. Capacitance vs. reverse voltage curve of GaN-SBD diode D

### 5.5.2 Diode Performance Measurement

Twelve high voltage diodes were tested for their VHF resonant rectifier performance. This thesis presents the performance results of the eight most relevant diodes (the list is shown in Table 5.1). The results from GaN-SBD D were omitted because its characteristics are very similar to that of GaN-SBD C. Also, three of the Si-FRD diodes did not work at VHF and no data could be taken. Figure 5.12 shows the diode dissipation vs. average diode current. Figure 5.13 shows a plot of diode dissipation as a percentage of output power vs. average diode current, and Fig. 5.14 is a zoom-in on the high power tail end of said plot. The worst performance were by the Power Integrations device (QH05TZ600), which is a Si-FRD, and the Infineon SiC-SBD (IDH12SG60C) and CREE SiC-SBD (C3D04060A). The diode with the least losses (best performance) were the GaN-SBD A and C. The least lossy SiC diode was the ROHM device (SCS106AG). Table 5.3 summarizes the findings from the test.

The diode voltage waveform for GaN-SBD B is shown in Fig. 5.15, as an example. The oscilloscope screenshot looks very much like the typical class E rectifier diode voltage waveform,

as expected. Figure 5.16 shows a zoom in on the conduction time of the diode. There is a slight “bump” on the diode voltage before settling on forward voltage drop. It is believed that this is an effect of the lead inductance of the diode. The large  $di/dt$  of the diode current makes the inductor provide a big spike of negative voltage. This was corroborated in SPICE by simulating the diode with the lead inductance. Figure 5.17 shows the SPICE model of the diode used to simulate the effect of diode junction capacitance and lead and bondwire inductance. It is the same model used in the previous chapter, the figure is reproduced here for convenience. The simulated diode voltage waveform is in Fig. 5.18. The “bump” appears in the simulation as predicted. Even though the values are not exactly matched (and the exact package and loop inductance in the circuit is not known), the “bump” effect is present in forward conduction which is suggestive that it is an inductance issue. It is notable that the die size of these diodes is actually quite small, suggesting that much smaller packages with lower inductances could be used.

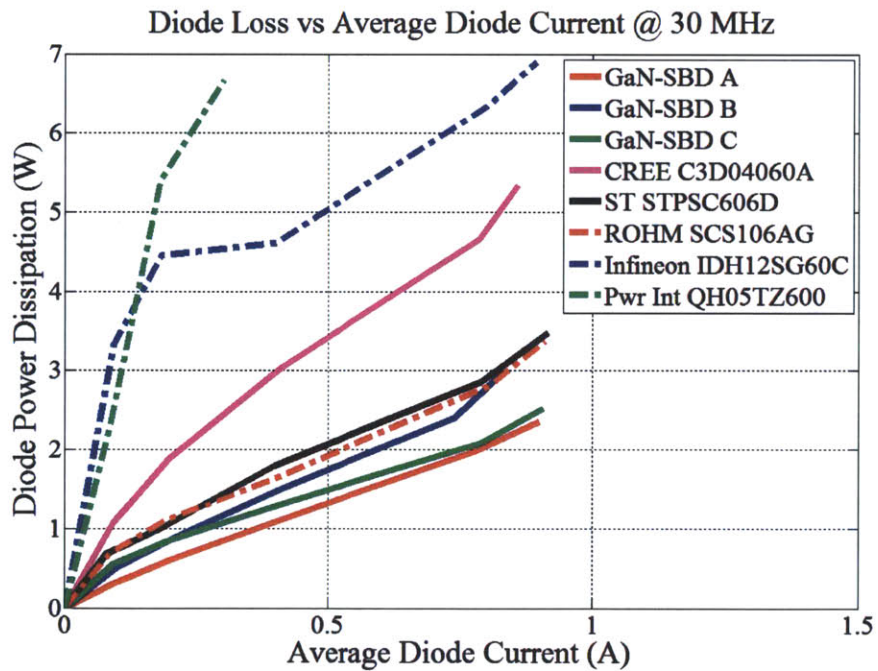


Fig. 5.12. Diode performance plot. Diode dissipation vs. average diode current.

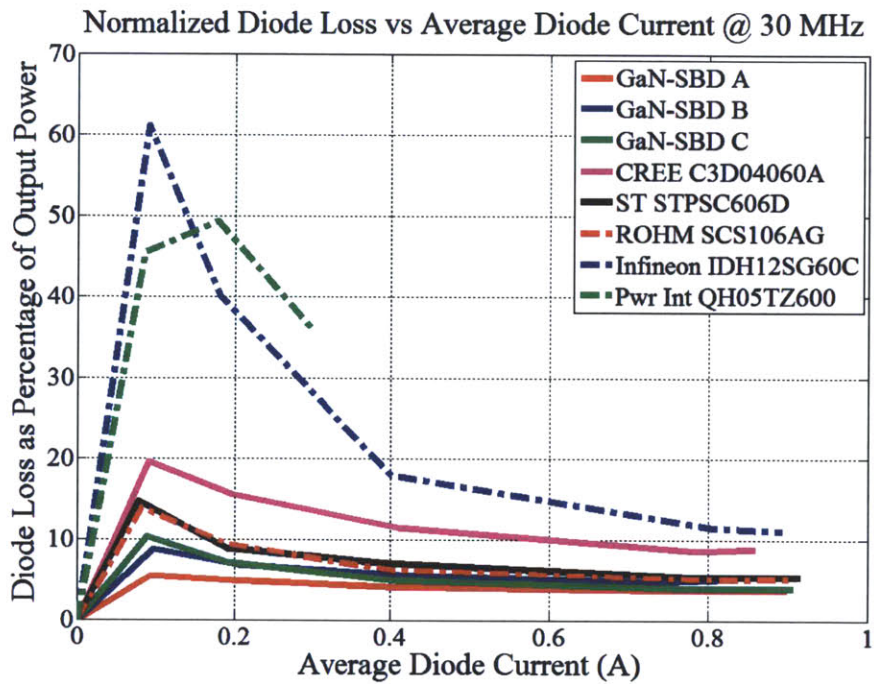


Fig. 5.13. Diode performance plot. Diode loss as a percentage of output power vs. average diode current.

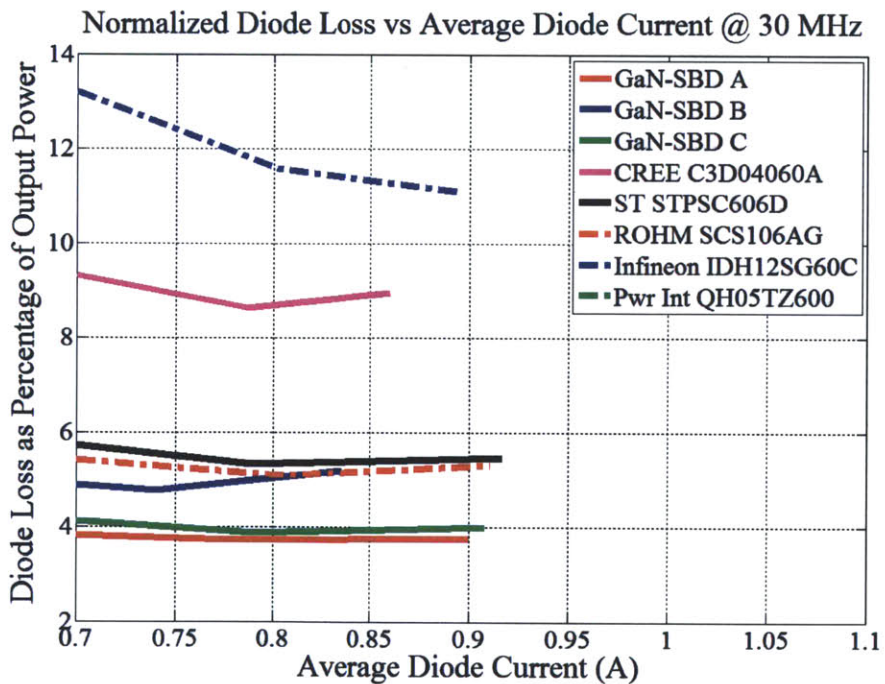


Fig. 5.14. Diode performance plot. Diode loss as a percentage of output power vs. average diode current. Zoom in on the tail end of the plot (0.7-1.1 A)

Table 5.3. Summary of Diode Performance Test

Diode	Pdiss/Pout % @ Max Power (57-64 W)	Peak Reverse Voltage
SEI GaN-SBD A	3.76 %	364 V
SEI GaN-SBD C	4.00%	299 V
SEI GaN-SBD B	5.20%	362 V
ROHM SCS106AG	5.32%	321 V
ST Micro STPSC606D	5.46%	323 V
CREE C3D04060A	8.97%	354 V
Infineon IDH12SG60C	11.11%	267 V
Power Integrations QH05TZ600	35.84%	273 V

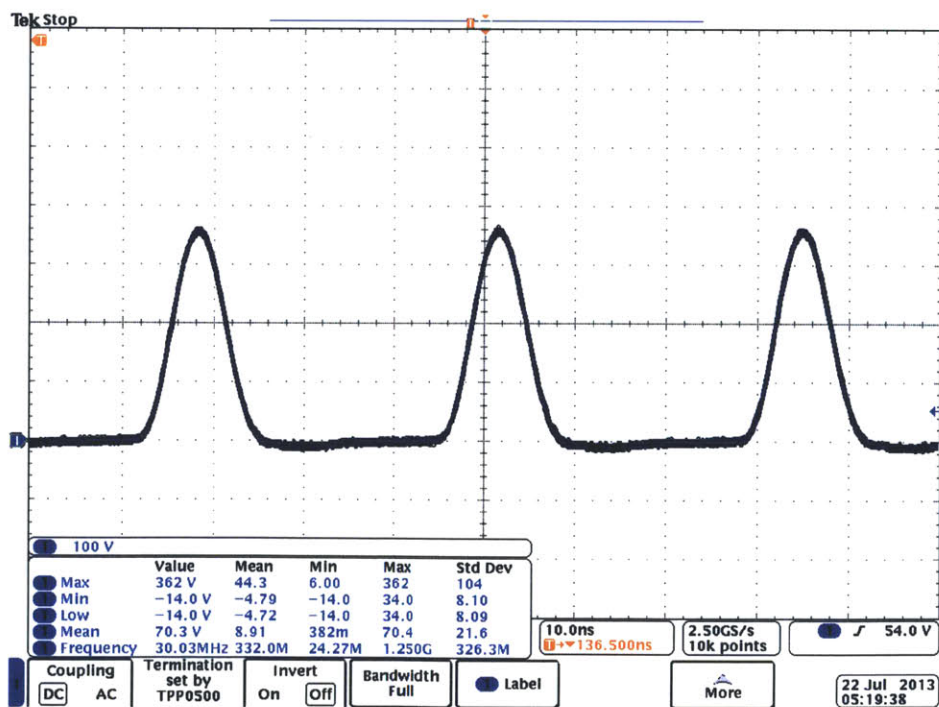


Fig. 5.15. GaN-SBD B. Diode voltage waveform at 57.65 W output power at 100V/div.

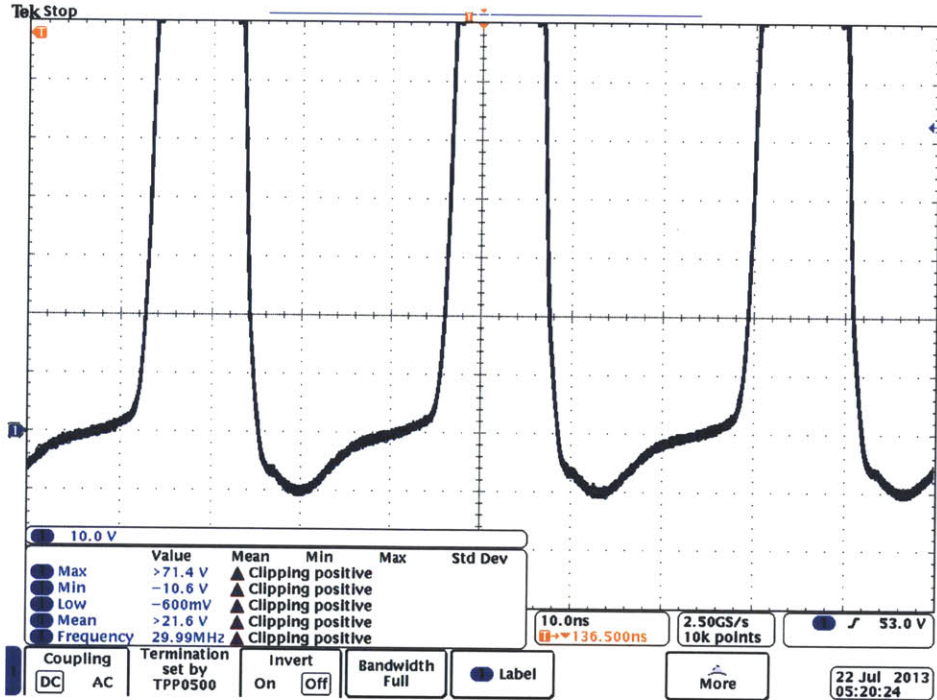


Fig. 5.16. GaN-SBD B. Diode voltage waveform at 57.65 W output power at 10V/div. Zoom in on diode conduction time.

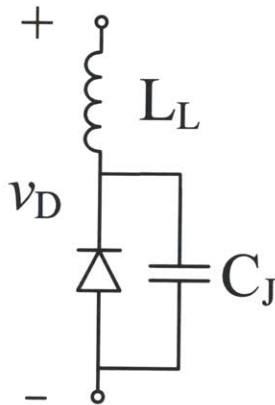


Fig. 5.17. Spice model of the GaN-SBD B diode. Includes  $L_L$ , lead inductance ( $\sim 10$  nH),  $C_J$ , junction capacitance of the diode (33 pF), and an ideal diode. Similar to Fig. 4.19.

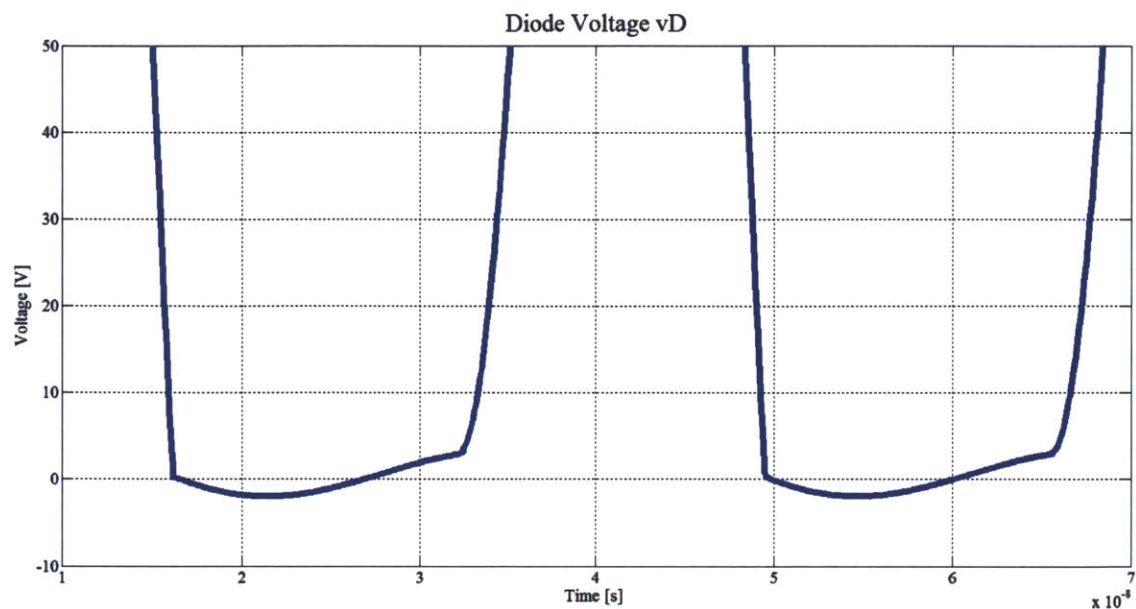


Fig. 5.18. Spice simulation of diode voltage including junction capacitance and lead and bondwire inductance.

Results of the diode test show that the conventional Si PiN diodes are not useful at VHF. On the other hand, SiC Schottky diodes can work well at VHF. This is consistent with circuits that have used them (e.g., [5]). Several of the commercial devices tested worked well, with ROHM SCS106AG being the best. GaN Schottky diodes also work well at VHF. In the devices tested, the experimental GaN Schottky diodes performed the best of all tested devices from an efficiency perspective. It should be noted that the devices were tested to well below their nominal rated voltages, and also probably below their achievable current levels. This was due to limitations in the test setup. Future tests should seek to explore both higher voltages and higher currents at VHF.

## **Chapter 6: Conclusion**

This thesis explores the design of class E rectifiers for variable power operation. The first portion of the work shows how to select the appropriate components to realize a rectifier achieving desired input resistive characteristics. The second half of this work focuses on evaluating the performance of diodes in VHF rectification. A variety of diodes are tested for their suitability for use at VHF, and a number of diodes are characterized for use in VHF rectifiers.

### **6.1. Thesis Summary**

Chapter 1 provides an introduction on power conversion systems and describes how miniaturization can be achieved through increases in switching frequency. Background is also provided on the design and application of resonant rectifiers in many high frequency power conversion applications including VHF dc-dc converters and wireless power transfer systems.

Chapter 2 explains the operational principle of the class E rectifier and derives analytical expressions that model its behavior. The analytical model derivation follows techniques used in previous work, but the model presented in this thesis addresses the more general case of the output inductor being a resonant inductor with high ac current instead of being a choke inductor with dc current. By coding the model equations in Matlab, three design plots are generated that enable rapid design of resonant rectifiers having approximately resistive input impedance characteristics. The design method is applied in an example design which is verified in simulation. The simulation proves the accuracy and usefulness of the design method at least for the case of ideal diodes.

Chapter 3 provides the experimental validation of the class E rectifier design method presented in chapter 2. The experimental setup, including measurement equipment, is described in detail. Two rectifiers are built: one with high external capacitance in parallel with the diode and another in which shunt capacitance is dominated by the nonlinear diode capacitance. The high external capacitance decreases the effect of the voltage dependence of the diode junction capacitance. These experimental results are in very good agreement with the theoretically expected values. The experimental results with the low external capacitance show a deviation

from the theoretically designed values. This is attributed to the voltage dependence of the diode capacitance.

Chapter 4 investigates diode performance for low voltage devices (60-100 V) in VHF resonant rectifiers. Seven Si Schottky diodes are tested. The experimental setup and design specifications are explained, as is the procedure for diode testing. The losses in the diodes are measured by a thermal characterization technique. The diodes are tested at four frequencies: 30 MHz, 50 MHz, 75 MHz and 100 MHz. The diode with the best overall performance was the PMEG6020EPA (a 60 V Si Schottky diode).

Chapter 5 investigates diode performance for high voltage devices (600 V) in VHF resonant rectifiers. Twelve diodes are tested: 4 GaN-SBD, 4 SiC-SBD and 4 Si-FRD. The GaN devices are experimental and are characterized for their device capacitance-voltage dependence. The diode capacitance measurement circuit and experiment are explained in detail. The other devices are well-characterized commercial devices. The diodes are tested at 30 MHz. The losses in the diode are also measured using thermal characterization. The GaN-SBD diodes had the best performance overall, with some of the SiC-SBD devices also performing well.

## **6.2. Thesis Conclusions**

This thesis provides a design methodology for selecting the components of a class E resonant rectifier (shunt loaded resonant rectifier) to achieve nearly resistive input impedance over a range of power levels. The design methodology presented here provides a way to select the resonant inductance and capacitance for a given maximum input impedance phase over a given power range. We develop analytical expressions to model the rectifier, and provide a graphical approach for the design. The design method is validated in simulation and experiment. Also guidance is given in selecting a diode for VHF resonant rectifiers. Various tests were conducted on diodes from different manufacturers and made from different materials. The best diode for a given voltage rating can also be selected. We can also easily measure power dissipated and characterize the capacitance-voltage dependence. It is hoped that the work presented here will prove to be useful in designing resonant rectifiers in applications that require resistive rectifier loads.

### 6.3. Future Work

There is still much that can be done in the in the field of VHF rectifiers. This thesis develops a model and design method for one specific kind of rectifier but the same principles can be applied to other types of rectifiers useful in different applications. Many other types of rectifiers exist that can be designed for resistive input impedance by careful selection of passive components. Some of these rectifiers may be less sensitive to device capacitance nonlinearity, which may be advantageous.

The diode testing experiments presented here serves as a foundation for testing at a larger scale and for different types of diodes. The characterization and testing carried out in this thesis covered some operating ranges of interest (e.g., including 12 V output at up to a few Amps). However, there needs to be substantially more work to identify the best devices for other voltage and power levels. Diodes should be tested at different power levels, and each circuit should be tuned for a specific family of diodes and operating range. Testing of high voltage devices showed that GaN and SiC devices are promising for VHF rectification, and broader testing is needed there as well. The GaN diodes had especially promising results with our circuits. Further study and application of GaN devices at VHF frequencies is definitely warranted as the technology develops.

The design method developed here could be used in conjunction with a class E inverter in order to complete a dc-dc converter. Other techniques could be applied, such as a resistance compression network, to design what could be a promising new topology of a high frequency, high efficiency dc-dc converter.

## Appendix A Matlab Code

### A.1 Class E rectifier parameter sweep Matlab code

```
% Class E Rectifier parameter sweep. Code solves for the rectifier input
% impedance at the fundamental frequency over a given power range for a given
% L-C pair. The code extracts the maximum phase and peak diode voltage over
% the power range and saves it. This process is repeated for a different L-C
% pair. The code stops after reaching the desired boundaries on L-C. Self
% contained code, no need for external custom functions.

% Written by Juan Santiago on March 2013

clc
clear all
close all
format long e
%% Design parameters, generic values for simulation. In the end, the data
% is going to be normalized.

Vo=12;           %rectifier output dc voltage in V
Po_max=54;       %rectifier maximum output power in W
f=30e6;          %frequency of input in Hz

%% Start of script

w=2*pi*f;        %frequency in radians/sec
rLmin=Vo^2/Po_max; %minimum dc output resistance in ohms
co=1/(w*rLmin);  %capacitance for normalization in F
lo=rLmin/w;      %inductance for normalization in H

pratio=10;       %power range ratio of the current power sweep in x:1

j=1;

clist=linspace(300e-12,2500e-12,2500); %capacitance range to be swept over;
%2500 is the current number of
%capacitance values to be tested

l1list=linspace(0.5e-9,140e-9,40); %inductance range to be swept over;
%40 is the current number of
%inductance values to be tested

% Begin loop

while j<=length(pratio)

plist=linspace(Po_max/pratio(j),Po_max,30); %power range to be swept over;
%30 is the current number of
%power values to be tested

k=1;
ki=length(l1list);
```

```

while k<=length(llist)
    L=llist(ki);
    m=1;
    mi=length(clist);
    D=0.5; %initial values of duty cycle D, current
    phi=0.5; %phase phi and current amplitude Im for
    Im=max(plist)/Vo; %the first iteration
    while m<=length(clist)
        C=clist(mi);
        mi=mi-1;
        r=1;
        while r<=length(plist)
            % Begin power sweep
            Po=plist(r);
            wr=1/sqrt(L*C); %resonant frequency for given LC pair
            zr=sqrt(L/C); %characteristic impedance for given LC
pair

            % Solve for D, phi and Im

            xo=[D,phi,Im]; %initial guess on solution of variables in each
                %iteration is the solution of the previous iteration

            % Solving the three non-linear equations for D, phi and Im using
            % fsolve

            [sol,fval,exitflag]=fsolve(@(x) [x(3)*w*L/((w/wr)^2-1)*(sin(2*pi*(1-
x(1)))*sin(x(2))-zr/(w*L)*sin(wr/w*2*pi*(1-x(1)))*sin(x(2))+cos(wr/w*2*pi*(1-
x(1)))*cos(x(2))-cos(2*pi*(1-x(1)))*cos(x(2)))+Vo-Vo*cos(wr/w*2*pi*(1-x(1)))-
x(3)*zr*sin(x(2))*sin(wr/w*2*pi*(1-x(1)))
            f*(x(3)*w*L/((w/wr)^2-1)*(-sin(x(2)))/w*cos(2*pi*(1-
x(1)))+zr/(w*wr*L)*cos(wr/w*2*pi*(1-
x(1)))*sin(x(2))+cos(x(2))/wr*sin(wr/w*2*pi*(1-x(1)))-
cos(x(2))/w*sin(2*pi*(1-x(1)))+Vo*(2*pi*(1-x(1))/w)-Vo/wr*sin(wr/w*2*pi*(1-
x(1)))+x(3)/wr*zr*sin(x(2))*cos(wr/w*2*pi*(1-x(1)))-(x(3)*w*L/((w/wr)^2-1)*(-
sin(x(2)))/w+zr/(w*wr*L)*sin(x(2)))+x(3)*zr/wr*sin(x(2)))-Vo
            f*(x(3)/((w/wr)^2-1)*(sin(x(2)))/wr*sin(wr/w*2*pi*(1-x(1)))-
sin(x(2))/w*sin(2*pi*(1-x(1)))-w*L/zr/wr*cos(x(2))*cos(wr/w*2*pi*(1-
x(1)))+cos(x(2))/w*cos(2*pi*(1-x(1)))+Vo/zr/wr*cos(wr/w*2*pi*(1-
x(1)))+x(3)*sin(x(2))/wr*sin(wr/w*2*pi*(1-x(1)))-(x(3)/((w/wr)^2-1)*(-
w*L/zr/wr*cos(x(2))+cos(x(2))/w)+Vo/zr/wr)+
Vo/(2*L)*(2*pi*x(1)/w)^2+(x(3)/((w/wr)^2-1)*(sin(x(2))*cos(wr/w*2*pi*(1-
x(1)))-sin(x(2))*cos(2*pi*(1-x(1)))+w*L/zr*cos(x(2))*sin(wr/w*2*pi*(1-x(1)))-
cos(x(2))*sin(2*pi*(1-x(1)))-Vo/zr*sin(wr/w*2*pi*(1-
x(1)))+x(3)*sin(x(2))*cos(wr/w*2*pi*(1-x(1))))*(2*pi*x(1)/w))-Po/Vo

            ],xo);

        aphil=0; %counter variable

        D=sol(1);

        phi=sol(2);

```

```

Im=sol(3);

maxiter=50; % max number of iterations for solving one L-C pair

n=0;

while D<0 | D>1 | phi<-2*pi | phi>2*pi | Im<0 | exitflag==0

    if aph1==100 % This loop changes the values of the
        xo(1)=xo(1)+0.01; % initial guess if one of the following
        xo(2)=xo(2)+0.01; % conditions are met: D greater than 1
        xo(3)=xo(3)+0.01; % or less than 0, or phi greater than
    else % 2pi or less than -2 pi, or Im less
than
        xo(1)=xo(1)-0.01; % zero. If a change is made, it will
        xo(2)=xo(2)-0.01; % solve the equation again until finding
        xo(3)=xo(3)-0.01; % the solution with physical meaning.
        aph1=aph1+1;
    end

    [sol,fval,exitflag]=fsolve(@(x) [x(3)*w*L/((w/wr)^2-1)*(sin(2*pi*(1-
x(1)))*sin(x(2))-zr/(w*L)*sin(wr/w*2*pi*(1-x(1)))*sin(x(2))+cos(wr/w*2*pi*(1-
x(1)))*cos(x(2))-cos(2*pi*(1-x(1)))*cos(x(2)))+Vo-Vo*cos(wr/w*2*pi*(1-x(1)))-
x(3)*zr*sin(x(2))*sin(wr/w*2*pi*(1-x(1)))
        f*(x(3)*w*L/((w/wr)^2-1)*(-sin(x(2)))/w*cos(2*pi*(1-
x(1)))+zr/(w*wr*L)*cos(wr/w*2*pi*(1-
x(1)))*sin(x(2))+cos(x(2))/wr*sin(wr/w*2*pi*(1-x(1)))-
cos(x(2))/w*sin(2*pi*(1-x(1)))+Vo*(2*pi*(1-x(1))/w)-Vo/wr*sin(wr/w*2*pi*(1-
x(1)))+x(3)/wr*zr*sin(x(2))*cos(wr/w*2*pi*(1-x(1)))-(x(3)*w*L/((w/wr)^2-1)*(-
sin(x(2)))/w+zr/(w*wr*L)*sin(x(2)))+x(3)*zr/wr*sin(x(2)))-Vo
        f*(x(3)/((w/wr)^2-1)*(sin(x(2)))/wr*sin(wr/w*2*pi*(1-x(1)))-
sin(x(2))/w*sin(2*pi*(1-x(1)))-w*L/zr/wr*cos(x(2))*cos(wr/w*2*pi*(1-
x(1)))+cos(x(2))/w*cos(2*pi*(1-x(1)))+Vo/zr/wr*cos(wr/w*2*pi*(1-
x(1)))+x(3)*sin(x(2))/wr*sin(wr/w*2*pi*(1-x(1)))-(x(3)/((w/wr)^2-1)*(-
w*L/zr/wr*cos(x(2))+cos(x(2))/w)+Vo/zr/wr)+-
Vo/(2*L)*(2*pi*x(1)/w)^2+(x(3)/((w/wr)^2-1)*(sin(x(2))*cos(wr/w*2*pi*(1-
x(1)))-sin(x(2))*cos(2*pi*(1-x(1)))+w*L/zr*cos(x(2))*sin(wr/w*2*pi*(1-x(1)))-
cos(x(2))*sin(2*pi*(1-x(1)))-Vo/zr*sin(wr/w*2*pi*(1-
x(1)))+x(3)*sin(x(2))*cos(wr/w*2*pi*(1-x(1)))]*(2*pi*x(1)/w))-Po/Vo

    ],xo);

D=sol(1);

phi=sol(2);

Im=sol(3);

n=n+1;
if n>maxiter,
disp('error solving function')
break
end
end
end

```

```

D=sol(1); %duty cycle

if D>0.999 %duty cycle, sim ends if too close to 1

    D=0.99;

end

phi=sol(2); %input current phase shift

Im=sol(3); %input current amplitude

%% Input Impedance Phase Calculation
% Extracts fundamental frequency component of the form
%  $f_1(t) = a_1 \cos(\omega t) + b_1 \sin(\omega t)$ 

t=0:0.01e-9:(1-D)/f; %time that diode is off, so  $v_D \neq 0$ 

vD= Im*w*L/((w/wr)^2-1)*(sin(w*t)*sin(phi)-
zr/(w*L)*sin(wr*t)*sin(phi)+cos(wr*t)*cos(phi)-cos(w*t)*cos(phi))+Vo-
Vo*cos(wr*t)-Im*sin(phi)*zr*sin(wr*t);

vd=vD.*cos(w*t);

a1=trapz(t,vd).*2.*f; %a1 fourier series coefficient

vd=vD.*sin(w*t);

b1=trapz(t,vd).*2.*f; %b1 fourier series coefficient

vD_fund=sqrt(a1.*a1+b1.*b1); %amplitude of fundamental input voltage

zinlmag(r)=vD_fund/Im;

zinlphase_mag(r)=abs(atan2(a1,b1)-phi)*180/pi; %magnitude of phase of
%the input impedance

zinlphase_true(r)=(atan2(a1,b1)-phi)*180/pi; %real phase of the input
%impedance

vDpklist(r)=max(vD); %max diode peak reverse voltage

r=r+1; %r is the power counter

%finish power sweep
end

%variables storing necessary values after a power sweep

[maxphasemag, ind1]=max(zinlphase_mag(:));

```

```

zin1clist_phasemag(m)=maxphasemag;
zin1clist_mag(m)=zin1mag(ind1);
zin1clist_truephase(m)=zin1phase_true(ind1);
vDpkclist(m)=vDpklist(ind1);
dutyclist(m)=D;
cvalue(m)=C;
m=m+1; % m is the capacitance counter

end

%variables storing necessary values after a capacitance sweep
lvalue(k)=L;
[minphasemag, ind2]=min(zin1clist_phasemag(:));
zin1llist_phasemag(k)=minphasemag;
zin1llist_mag(k)=zin1clist_mag(ind2);
zin1llist_truephase(k)=zin1clist_truephase(ind2);
vDpkllist(k)=vDpkclist(ind2);
dutyllisy(k)=dutyclist(ind2);
cvaluelist(k)=cvalue(ind2);

%figure
semilogx(cvalue./co, zin1clist_phasemag, '.')
title('Phase magnitude vs Capacitance for fixed Inductance');
grid on
hold on

k=k+1; % k is the inductance counter

ki=ki-1;

end

hold off

%variables storing necessary values after an inductance sweep

```

```

    zin1_phasemagplot(j,:)=zinl1list_phasemag;

    zin1_magplot(j,:)=zinl1list_mag;

    zin1_truephaseplot(j,:)=zinl1list_truephase;

    vDpkplot(j,:)= vDpk1list;

    dutyplot(j,:)=duty1list;

    cvalueplot(j,:)=cvalue1list;

    lvalueplot(j,:)=lvalue;

    j=j+1; % j is the power ratio counter

end

%plot L vs C
figure
loglog(cvalueplot./co,lvalueplot./lo,'r*')
hold on
grid on
xlabel('Capacitance')
ylabel('Inductance')
title('Inductance vs Capacitance')
hold off

%plot input phase mag vs C
figure
semilogx(cvalueplot./co,zin1_phasemagplot,'r*')
hold on
grid on
xlabel('Capacitance')
ylabel('Phase Magnitude')
title('Input Impedance Phase magnitude vs Capacitance')
hold off

%plot peak diode voltage vs C
figure
semilogx(cvalueplot./co,vDpkplot./Vo,'r*')
hold on
grid on
xlabel('Capacitance')
ylabel('Diode Peak Voltage')
title('Diode Peak Reverse Voltage vs Capacitance')
hold off

return

```

## A.2 Input impedance calculation from oscilloscope data Matlab code

```
% Calculates input impedance by extracting the fundamental components of the
% measurements provided by the oscilloscope.
% Written by Juan Santiago on June 2013.

format long e
close all
clear all
clc

f=30e6; %input frequency
r=0;

pwr=[1.44 2.9 5.9 10.1 12.75 15.53]; %list of output power in
                                     %experimental data.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

point
text=csvread('tek0107.csv'); %reads from CSV files. One operating
point
r=r+1;
k=1;

[a,ind1]=min(abs(text(:,1))) %for csv files starting in negative time

while text(k,1)-text(ind1,1)< 1/f %searches for one full period of
                                     %the waveform
    k=k+1;
end

ind2=k;

t=text(ind1:ind2,1)-text(1,1); %selects one full period of the waveform

vin=text(ind1:ind2,2); %selects one full period of the waveform

iin=text(ind1:ind2,3); %selects one full period of the waveform

% Extracts fundamental frequency component of the form
%  $f_1(t) = a_1 \cos(\omega t) + b_1 \sin(\omega t)$ 

w=2*pi*f;

vd=vin.*cos(w*t);

a1=trapz(t,vd).*2.*f; %a1 fourier series coefficient

vd=vin.*sin(w*t);

b1=trapz(t,vd).*2.*f; %b1 fourier series coefficient
```

```

vin_fund=sqrt(a1.*a1+b1.*b1); %amplitude of fundamental input voltage

id=iin.*cos(w*t);

a2=trapz(t,id).*2.*f; %a1 fourier series coefficient

id=iin.*sin(w*t);

b2=trapz(t,id).*2.*f; %b1 fourier series coefficient

iin_fund=sqrt(a2.*a2+b2.*b2); %amplitude of fundamental input current

zinlmag(r)=vin_fund/iin_fund; %magnitude of input impedance

zinlphase_true(r)=(atan2(a1,b1)-atan2(a2,b2))*180/pi; %phase of
%input impedance

pin(r)= vin_fund*iin_fund/2*cos(zinlphase_true(r)*pi/180);

[axisy,y1,y2]=plotyy(t,vin,t,iin)

%Repeat for every operating point by repeating code above and changing
the csv fileread command

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

text=csvread('zin_diodesim2.csv'); %reads from simulation results exported
%from SPICE

figure %plots impedance magnitude vs. power for experimental and SPICE data

[y1]=plot(pwr,zinlmag,'rs','LineWidth',6)
hold on
[y2]=plot(text(:,1),text(:,2),'bv','LineWidth',6)
plot(pwr,zinlmag,'r','LineWidth',6)
plot(text(:,1),text(:,2),'b','LineWidth',6)
grid on
set(y1,'LineWidth',3)
ylabel('Magnitude (Ohms)','FontSize',30,'Fontname','Times New Roman')
title('Input Impedance Magnitude vs. Power','FontSize', 30, 'Fontname','Times
New Roman')
xlabel('Power (Watts)','FontSize',30,'Fontname','Times New Roman')
hold off
legend('Experimental','Simulation')

figure %plots impedance phase vs. power for experimental and SPICE data

plot(pwr,zinlphase_true,'rs','LineWidth',3)
grid on

```

```
hold on
plot(text(:,1),text(:,3),'bv','LineWidth',3)
plot(pwr,zinlphase_true,'r','LineWidth',3)
plot(text(:,1),text(:,3),'b','LineWidth',3)
ylabel('Phase (Degrees)','FontSize',30,'Fontname','Times New Roman')
title('Input Impedance Phase vs. Power','FontSize', 30, 'Fontname','Times New
Roman')
xlabel('Power (Watts)','FontSize',30,'Fontname','Times New Roman')
hold off
legend('Experimental','Simulation')
```

## Appendix B Board Schematic and Layout Files

Schematics shown here are made with EAGLE software from CadSoft.

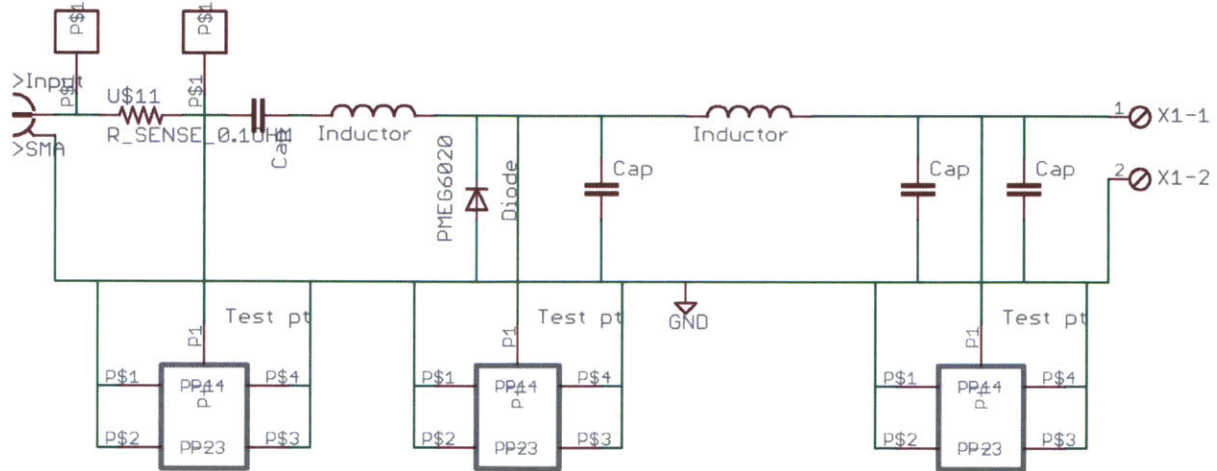


Fig. B.1. Schematic of class E rectifier circuit board. Input series resistor  $R_{sense}$  was replaced in the final design with a loop wire for current measurement with a clip-on current probe. Referenced in chapter 3.

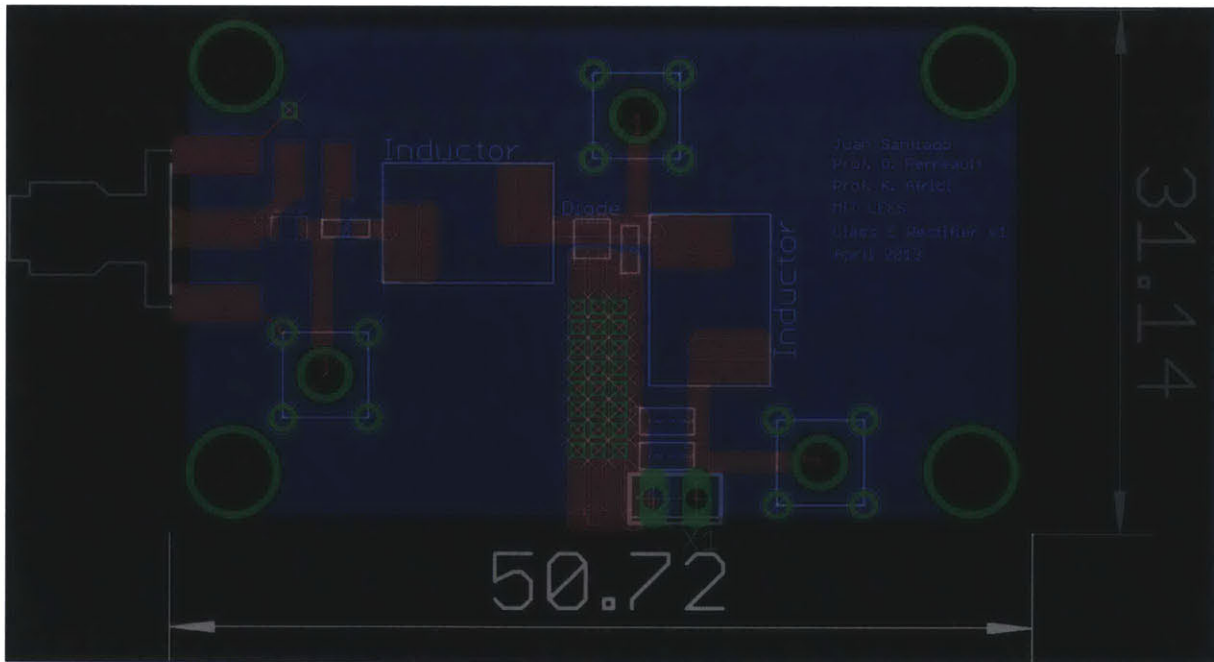


Fig. B.2. Layout of class E rectifier circuit board. The dimensions are in mm. Referenced in chapter 3.

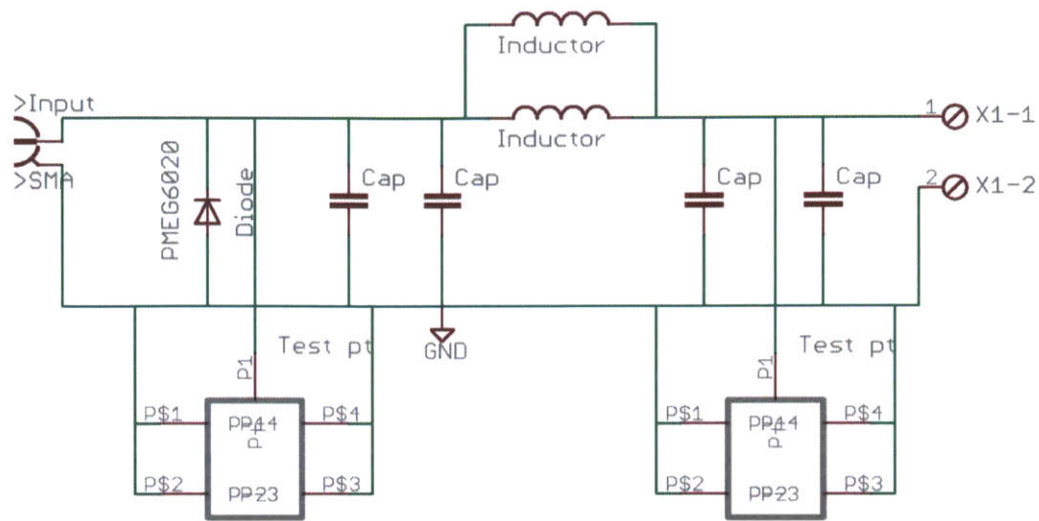


Fig. B.3. Schematic of SMD diode testing circuit board. The two inductors in parallel provide space and versatility on the board for using multiple inductors. Only one inductor is used at a time. Referenced in chapter 4.

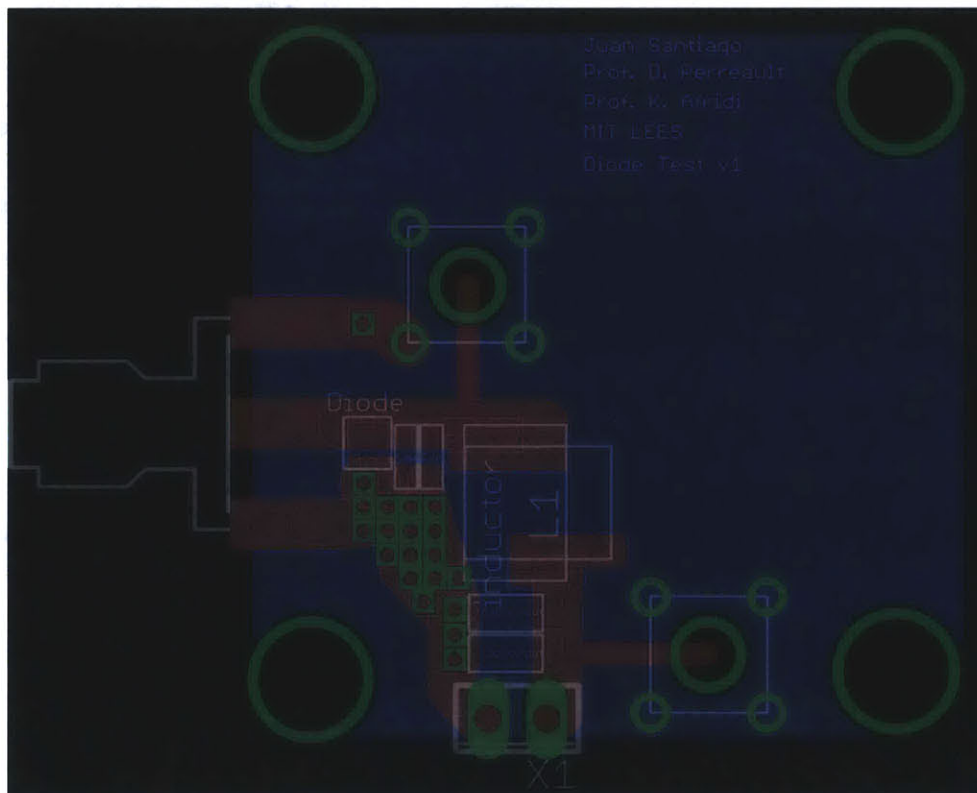


Fig. B.4. Layout of SMD diode testing circuit board. Referenced in chapter 4.

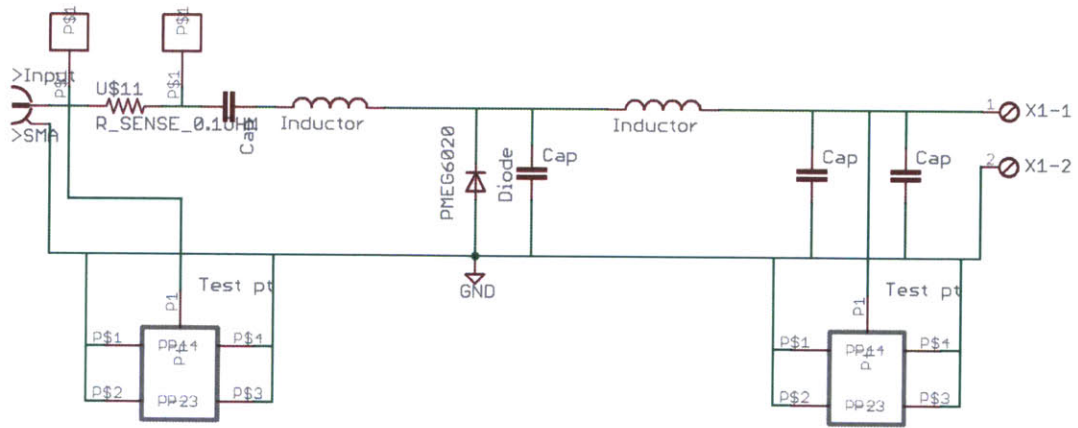


Fig. B.5. Schematic of class E rectifier circuit board. Input series resistor R\_sense was not needed in the final design and was replaced with a wire. Referenced in chapter 5.

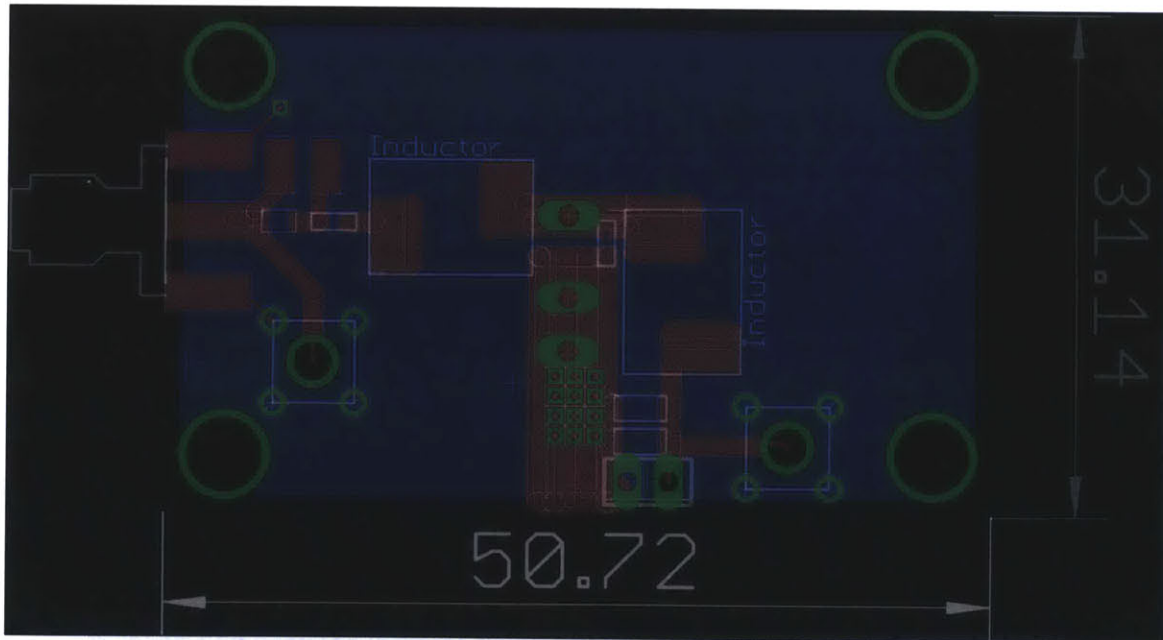


Fig. B.6. Layout of class E rectifier circuit board for through hole diodes. Referenced in chapter 5.

## Appendix C Diode Testing Data

### C.1. Low voltage diode performance test experimental data

#### Power dissipation-diode case temperature characterization

##### 1. NXP PMEG6020EPA

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	23.3
0.1	0.2984	23.6
0.2	0.3198	24.4
0.4	0.3426	27
0.6	0.3586	29.6
0.8	0.371	33.2
1	0.3829	36.5
1.2	0.3947	40.1
1.4	0.4067	42.5
1.6	0.4195	46
1.8	0.4325	49.5
2	0.4465	51.8

##### 2. Vishay 10MQ100

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	23
0.2	0.518	26.1
0.4	0.612	30
0.6	0.661	34.7
0.8	0.684	39.7
1	0.696	43.8
1.2	0.703	48.2
1.4	0.706	53.4
1.6	0.707	58.1
1.8	0.708	63.2
2	0.708	67.5

##### 3. Fairchild S100

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	20.6
0.1	0.489	21.2
0.2	0.54	23.1
0.4	0.616	27.2
0.5	0.636	30.3
0.6	0.65	32.9
0.8	0.666	37.3
1	0.672	41.4
1.2	0.675	45.5

##### 4. Vishay SS16

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	24.9
0.2	0.411	27.6
0.4	0.439	32
0.6	0.461	36
0.8	0.48	41.3
1	0.498	47.3
1.2	0.517	51.2

5. ST STPS1H100A

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25
0.2	0.539	27.3
0.4	0.611	31.1
0.6	0.648	36.1
0.8	0.663	41.1
1	0.672	45.6
1.2	0.676	50.3

6. NXP PMEG6030EP

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	27.4
0.2	0.3	27.7
0.4	0.323	28.8
0.8	0.347	32.7
1	0.355	35.2
1.4	0.37	39.6
1.8	0.384	44.8
2	0.39	45.9

7. Vishay MSS1P6

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25.7
0.2	0.372	27.6
0.4	0.422	31.1
0.6	0.467	35.1
0.8	0.514	40.8
1	0.561	46.7
1.2	0.597	53.9

### 30 MHz Diode Performance Test

#### 1. NXP PMEG6020EPA

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	23.1	0
12.12	0.178	29.4	41.2
12.38	0.386	33.7	46.5
12.7	0.588	38.4	50
13.02	0.788	44.7	53.4
13.36	1.017	51.6	56.7
13.67	1.192	58.8	59.1
13.99	1.395	66.6	62.2

#### 2. Vishay 10MQ100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	20.1	0
12.17	0.148	29	44.8
12.29	0.178	36.4	46.1
12.68	0.365	106	53.8

#### 3. Fairchild S100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	19	0
12.28	0.145	28.4	43.7
12.48	0.262	56.1	51
12.53	0.303	112.2	54.7

#### 4. Vishay SS16

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25	0
12.24	0.162	31.6	42.5
12.518	0.373	37.5	46.5
12.873	0.581	45.5	49.6
13.36	0.783	53.2	51.9
13.65	0.989	61.8	53.8
13.97	1.185	72.5	55.7

#### 5. ST STPS1H100A

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	24.5	0
12.011	0.131	32.3	41.1
12.319	0.381	57.4	51.9
12.541	0.543	121.6	56.9

#### 6. NXP PMEG6030EP

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	26.3	0
12.077	0.169	30.5	40.9
12.357	0.4	33.8	46.2
12.61	0.584	37	49.8
12.992	0.887	42.4	54.4
13.408	1.2	49.5	58.1
13.833	1.508	57.1	62.5
14.21	1.805	65.6	66.5

## 7. Vishay MSS1P6

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.7	0
12.03	0.139	30.8	40.7
12.31	0.365	37.5	47.6
12.576	0.574	45.4	51.7
12.85	0.776	55.7	55.2
13.14	0.995	69.7	59.3

## 50 MHz Diode Performance Test

### 1. NXP PMEG6020EPA

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	26	0
12.24	0.202	31.6	35.1
12.43	0.397	36.6	39.2
12.66	0.599	42.5	41.4
12.91	0.796	47.6	43.3
13.17	1	53.8	45.4
13.47	1.209	61.7	47.4
13.7	1.397	73	49.7

### 2. Vishay 10MQ100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	20.4	0
12.01	0.172	33.2	35.5
12.16	0.283	55.3	38.5
12.26	0.364	115.3	42.3

### 3. Fairchild S100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	20.6	0
12.07	0.187	37	36.6
12.18	0.273	85.5	42.6

### 4. Vishay SS16

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	24.2	0
12.061	0.171	32.6	34.8
12.326	0.385	40.2	37.4
12.588	0.582	49	40
12.886	0.786	62.1	43.6
13.215	1.023	74.5	48
13.463	1.188	87.1	51.7

### 5. ST STPS1H100A

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	26	0
12.135	0.189	44	37
12.363	0.362	105.7	42.7

### 6. NXP PMEG6030EP

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.7	0
12.186	0.281	34.6	36.4
12.551	0.587	44.5	41.3
12.936	0.888	54.6	44.3
13.334	1.189	66.6	47
13.741	1.488	81.6	49.6

## 7. Vishay MSS1P6

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	28.5	0
12.21	0.197	35.1	40.7
12.413	0.393	42.7	47.6
12.646	0.599	53.3	51.7
12.886	0.795	67.8	55.2

## 75 MHz Diode Performance Test

### 1. NXP PMEG6020EPA

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.1	0
12.18	0.189	34	35.1
12.38	0.398	42.2	39.2
12.62	0.595	49.8	41.4
12.87	0.795	58.4	43.3
13.15	0.996	68.8	45.4
13.43	1.193	83	47.4

### 2. Vishay 10MQ100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	23.5	0
12.006	0.139	34.8	26.8
12.21	0.281	64.8	30.9
12.28	0.365	105.7	34.1

### 3. Fairchild S100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	21	0
12	0.14	36.7	28
12.15	0.266	119.6	36.9

### 4. Vishay SS16

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	27	0
12.219	0.188	38.1	34.8
12.43	0.399	47.4	37.4
12.658	0.599	57.7	40
12.87	0.789	74	43.6
13.07	0.934	100.5	48

### 5. ST STPS1H100A

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	26.9	0
12.089	0.161	44.3	37
12.333	0.368	114.5	42.7

### 6. NXP PMEG6030EP

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	28.4	0
12.323	0.285	41	36.4
12.64	0.596	56.3	41.3
12.985	0.888	70.5	44.3
13.343	1.187	86.5	47

### 7. Vishay MSS1P6

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	27.1	0
12.12	0.175	35.3	40.7
13.365	0.391	46.6	47.6
12.608	0.595	61.1	51.7
12.87	0.804	85.5	55.2

## 100 MHz Diode Performance Test

### 1. NXP PMEG6020EPA

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	22.9	0
12.04	0.185	34.7	29.1
12.2	0.394	44.3	32.4
12.48	0.598	55	34
12.73	0.793	71.2	35.3

### 2. Vishay 10MQ100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	22.7	0
12.07	0.185	38.2	24.9
12.17	0.292	61.1	26.2
12.23	0.35	125	28.2

### 3. Fairchild S100

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	22.7	0
11.95	0.113	31.3	25
12.09	0.217	130.3	30.2

### 4. Vishay SS16

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	24.4	0
12.05	0.166	35.3	24.8
12.3	0.393	44.3	26.2
12.57	0.593	56.4	27.3
12.802	0.752	87.1	30

### 5. ST STPS1H100A

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	24.2	0
12.053	0.171	51.3	29.2
12.185	0.28	114.2	36.2

### 6. NXP PMEG6030EP

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	28.5	0
12.298	0.294	48.3	26.8
12.633	0.601	62	28.8
12.984	0.896	79.5	30.9

### 7. Vishay MSS1P6

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	27.5	0
12.125	0.193	39.2	25.1
12.367	0.403	55.7	27.4
12.586	0.601	81.1	30.1

## C.2. Capacitance Measurement

### 1. GaN SBD A

Bias Voltage (V)	Capacitance (pF)
0	210
1	153
2	126
3	110
4	99
5	92
6	85
7	80
8	76
9	72
10	69
16	58
24	49
32	45
40	40
56	35
72	32
105	29
153	25
200	23
306	20.5
400	20.2

### 2. GaN SBD B

Bias Voltage (V)	Capacitance (pF)
0	190
1	138
2	114
3	102
4	91
5	84
8	71
10	65
16	54
24	46
32	41
56	33.1
72	30.1
105	26.4
153	23.4
201	21.6
306	20.2
400	20.1

### 3. GaN SBD C

Bias Voltage (V)	Capacitance (pF)
0	400
1	275
2	229
3	202
4	183
5	168
7	147
9	133
10	127
16	105
24	89
32	79
48.4	67
64.5	60
88	53
105	50
153	43.6
201	39.8
250	37.2
300	35.6
400	34.9

### 4. GaN SBD D

Bias Voltage (V)	Capacitance (pF)
0	416
1	286
2	237.3
3	206.7
4	187.7
5	172.5
6	160.5
8	143.5
10	131
16	110
24	91.5
32	81.2
48.4	69
64.5	61.46
80.7	56.5
104.7	51.1
153	44.6
201.3	40.8
250	38
300	36.3
400	34.73

### C.3. High voltage diode performance test experimental data

#### Power dissipation-diode case temperature characterization

##### 1. GaN-SBD A

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	26.4
0.201	0.793	29.6
0.405	0.834	32
0.805	0.897	36.8
1.202	0.954	41.3
1.6053	1.015	46
2.01	1.0804	53.8

##### 2. GaN-SBD B

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25.6
0.201	0.992	28.5
0.403	1.075	31.3
0.805	1.196	38.1
1.203	1.282	46
1.604	1.364	53.4
2.012	1.449	61.1

##### 3. GaN-SBD C

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	26.6
0.203	0.765	29.7
0.403	0.801	31.4
0.804	0.853	34.9
1.211	0.897	39.7
1.611	0.939	44.2
2.004	0.98	49.8

##### 4. CREE C3D04060A

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	26.3
0.202	0.909	29.5
0.403	0.951	30.6
0.801	1.013	33.7
1.2046	1.072	37.6
1.613	1.134	43.2
2.014	1.201	45.5

5. ST Microelectronics STPSC606D

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25.8
0.202	0.875	27.7
0.402	0.912	29.1
0.806	0.965	31.2
1.21	1.014	34.3
1.603	1.06	37.3
2.018	1.114	40.5

6. ROHM SCS106AG

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25.5
0.209	0.979	27.1
0.405	1.005	29.1
0.804	1.041	32.3
1.204	1.071	36.1
1.605	1.101	38.3
2.008	1.131	43.7

7. INFINEON IDH12SG60C

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25.7
0.198	0.943	27.2
0.404	0.972	28.5
0.805	1.01	30.5
1.204	1.04	34.6
1.607	1.071	36.2
2.01	1.103	39.5

8. Power Integrations QH05TZ600

$I_D$ (A)	$V_D$ (V)	$T_D$ (°C)
0	0	25.6
0.21	1.36	28.2
0.505	1.547	31.7
1.006	1.705	38.4
1.5007	1.788	45.5
2.0077	1.824	52.7

### 30 MHz Diode Performance Test

#### 1. GaN-SBD A

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.8	0
60.1	0.0936	30.5	208
61.51	0.197	34	244
63.81	0.395	39.6	286
67.85	0.778	50.5	348
69.44	0.9	55.1	364

#### 2. GaN-SBD B

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.8	0
60.29	0.0961	32.6	205
61.69	0.205	37.1	239
64.15	0.413	44.8	291
67.8	0.74	55.8	345
69.04	0.835	63.2	362

#### 3. GaN-SBD C

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.8	0
60.1	0.0886	32.8	197
61.49	0.191	36.1	215
63.95	0.407	41.2	241
67.94	0.79	50.2	285
69.35	0.908	55.2	299

#### 4. CREE C3D04060A

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	26.6	0
60.22	0.0908	36.2	221
61.6	0.196	42.7	243
64.15	0.4105	52	285
68.3	0.787	65	345
69.2	0.86	70.5	354

#### 5. ST Microelectronics STPSC606D

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	25.2	0
59.85	0.0771	30.1	203
61.42	0.19	32.4	229
63.82	0.397	37.2	261
67.89	0.789	44	307
69.41	0.917	48	323

#### 6. ROHM SCS106AG

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	24.8	0
59.97	0.081	30.2	213
61.44	0.191	33.5	233
63.89	0.401	37.6	261
68.25	0.803	46.7	313
69.68	0.911	51.2	321

7. INFINEON IDH12SG60C

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	28.9	0
60.2	0.0904	49.8	179
61.4	0.181	56.8	191
63.97	0.401	57.8	217
68.2	0.802	68.5	255
69.47	0.894	72	267

8. Power Integrations QH05TZ600

Vo (V)	Io (A)	Td (°C)	Vrev,pk (V)
0	0	24.9	0
60.1	0.085	42.2	223
61.36	0.1785	64.8	273
62	0.3	74	---

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