A High Aspect-Ratio Silicon Substrate-Via Technology and Applications

by

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B.S.E. Electrical Engineering
University of Michigan-Ann Arbor, 1996

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of

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Abstract

Substrate vias are widely used in GaAs microwave and millimeter-wave ICs to provide low-impedance ground connections. As silicon RFICs strive for high-frequency operation, it becomes increasingly important to reduce all extrinsic parasitics. Of particular concern is the MOSFET source or BJT emitter impedance, which greatly affects the gain of RF amplifiers. To address this, we have developed a through-wafer via technology for silicon, which allows the implementation of high-aspect ratio, low-impedance ground connections. The fabrication of these vias involves three main steps: (1) anisotropic DRIE to etch the vias, (2) PECVD silicon nitride deposition to form an insulating, barrier liner, and (3) copper electroplating to fill the via. Since our vias incorporate an insulating liner, this through-wafer via technology could also be used to distribute power and ground in logic circuits and MEMS. We have demonstrated vias with an aspect ratio as high as 14:1 and an inductance that approaches the theoretically expected value.

Our via technology can also be exploited to reduce crosstalk and improve subsystem isolation in RF System-on-a-Chip applications. High crosstalk immunity is critical to enable one-chip systems integrating noisy logic with sensitive low-noise amplifier and analog circuitry. Using our substrate-via technology, we have implemented a novel Faraday cage isolation scheme that is successful in suppressing crosstalk by over 20 dB at 1 GHz at a distance of 100 μm.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

Acknowledgements

Completing this thesis has been one of the greatest and rewarding accomplishments of my academic career, and I have many people to thank for getting me this far. First, I would like to thank Professor Jesús del Alamo for his guidance through this project and for his patience through many processing mishaps, practice presentations, and red-inked revisions. I also sincerely thank the del Alamo group members, Jim Fiorenza, Samuel Mertens, Tassanee Payakapan, and Jörg Scholvin, for their invaluable assistance with this project and their camaraderie.

Other students and faculty who were instrumental in the success of this research are Arturo Ayón, Joel Voldman, and Andy Fan for their fabrication expertise and Don Hitko for his help with the measurement setup.

Also, I would like to thank all the staff of the Microsystems Technology Laboratories, especially Kurt Broderick and Denis Sullivan for their assistance in setting up the copper electroplating system in MTL.

I also must thank my friends I have made at MIT. You have made my experience here the best, and I will bring with me many happy and entertaining memories from this otherwise intimidating place.

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I also extend my thanks to my adopted SRC industrial mentor, Keith Jenkins, for his help in designing the test structures for the impedance measurements and Faraday cages.

Finally, I would like to thank my friends across the country who have supported me from afar and especially my parents, Chun-teh and Madeline, and my little sister, Emily, for their support and for their advice that led me to MIT.

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Chapter 1

Introduction

1.1 Motivation

The primary motivation for this thesis was to develop a low-impedance, through-wafer interconnect of high aspect ratio (height:width) to route power and ground in silicon ICs. Through-wafer interconnects or substrate vias are widely used in GaAs millimeter wave integrated circuits (MMICs) and radio frequency integrated circuits (RFICs) to reduce the inductance of ground connections [1-3]. As an economical alternative to GaAs, silicon is gradually replacing GaAs in low-end and high-volume RF applications [4]. As silicon RFICs attain higher frequencies of operation, it is crucial to reduce extrinsic parasitics, especially the MOSFET source or BJT emitter inductance because they negatively affect the gain of RF amplifiers [1-3, 5]. The effect of source inductance on gain can be seen from the equation for maximum available gain (MAG) of a FET [5]:

$$MAG = \left(\frac{f_T}{f}\right)^2 \frac{1}{4g_d\left(R_i + R_S + \pi f_T L_S\right) + 4\pi f_T C_{dg}\left(R_i + R_S + 2\pi f_T L_S\right)} \qquad \textit{Equation 1-1}$$

where f_T is the cutoff frequency, f is the operating frequency, g_d is the drain conductance, R_i is the channel resistance between source and gate, R_S is the source series resistance, L_S is the common source lead inductance, and C_{dg} is the Miller feedback capacitance. Equation 1-1 shows that L_S must be minimized along with the input resistance R_i and R_S between the source and gate to increase gain [5]. Using substrate vias reduces this inductance better over other methods such as sheet grounding [5] and metal bridging [1, 6].

By incorporating an insulating liner to electrically isolate the via from the substrate, we can use a single kind of via to route power and ground through the backside on the same chip.

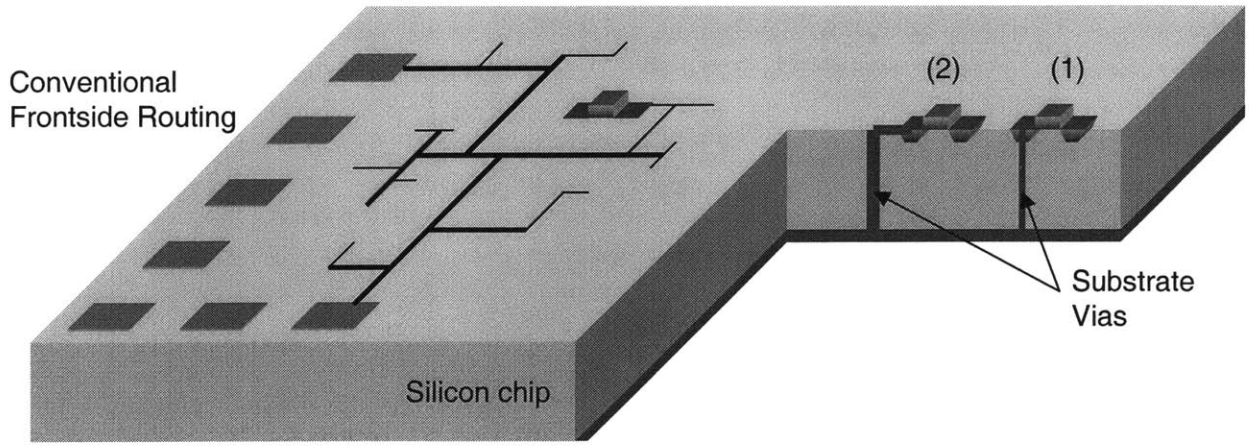

Figure 1-1. Silicon chip with conventional frontside metal routing of power/ground on the left. On the right, the cutaway shows an alternate way of routing by using substrate vias tapping individual transistors. (1) shows a substrate via connected to the source or drain of the transistor directly. (2) shows a larger substrate via to the side of the transistor and tapping the source or drain with a short metal line on the surface.

Conventional routing of power and ground is accomplished on the frontside of a chip using long metal lines (Fig. 1-1). These winding pathways of frontside interconnects have an increased resistance and inductance that is detrimental to circuit operation. By using a substrate via to tap an individual transistor, the impedance can be greatly reduced. Two possible ways of connecting to an individual transistor are also shown in Fig. 1-1: (1) tapping the source or drain of a transistor directly if the via footprint is small enough, or (2) etching a via to one side of the transistor and connecting the via to the source or drain through a short metal line on the surface.

Another important application for a substrate-via technology is as a Faraday cage to reduce crosstalk between devices and improve subsystem isolation in RF System-On-a-Chip (SOC) applications. Analog circuit failure due to noisy digital circuits on mixed-signal chips is a common problem facing SOC designs [7-9]. Fabricating a cage of substrate vias surrounding a sensitive or noisy circuit can attenuate undesired signals from propagating through the substrate.

1.2 Previous Substrate-Via Technology

Substrate-via technology in GaAs has been extensively researched and developed because of the serious impact the source impedance has on the gain of microwave circuits. GaAs substrate vias

are generally fabricated on the backside of thinned substrates using various dry etching techniques in a chlorine-based plasma [10-18]. For better step coverage for subsequent metallization steps, a conical or V-shaped profile is desired [11]. However, this greatly hinders the packing density of these vias. These conical vias have at best aspect ratios of about 1 [11, 17]. Vias with vertical sidewalls have better aspect ratios, as high as 3 (30-μm wide by 100-μm deep) etched from the backside [15]. One group was able to etch anisotropic vias from the frontside with an aspect ratio of 5 (20-μm wide by 100-μm deep) [19]. However, this is still too low for the applications we suggest for silicon substrate vias.

Diverse applications have stimulated the development of substrate vias in silicon. Most prominent are chip-to-chip connections in wafer stacks for 3-D integration [20-22], backside electrical connections for micro-electrical mechanical systems (MEMS) [23-27], on-chip inductors [28] and capacitors [29, 30], and, most importantly for this work, parasitic-inductance reduction in MMICs [4]. The previous work done for 3-D interconnections for chip stacks [20-23] and backside contacts for MEMS [24, 26, 27] developed substrate vias using a KOH etch which has a characteristic sloped sidewall because of its crystallographic etch selectivities (discussed in Section 2.1.2). These vias have the same packing density problem as the V-shaped GaAs vias. Pore arrays in silicon developed for capacitors could be used to fabricate substrate vias; however, this electrolytic etch is not easily controlled and limits the resistivities of wafers [30]. Both the MMIC and inductor applications use the same plasma-etch technology we used to etch anisotropic substrate vias. Their vias have aspect ratios of 2.5 (60-μm wide by 150-μm deep) [4] and 17 (30-μm wide by 525-μm deep) [28], respectively. However, these vias are only coated with metal (Cu or Au) and not filled. Although not a concern for inductors, Soh *et al.* [28] have used silicon dioxide as a liner material for Cu, which is not a barrier to migrating Cu ions that can be detrimental to transistors. Strohm *et al.* [4] report an inductance of 22 pH for their MMIC via hole, but their aspect ratio only reaches 2.5. Our via technology strives for significantly higher aspect ratios.

Thinning of GaAs substrates for RF applications is routine in industry. It is not uncommon for substrates to be thinned to 100 μm or less [2, 14, 15, 31]. In silicon this is not so typical. However, from Fig. 1-2, the trend in chip thickness for some applications is evolving in favor of

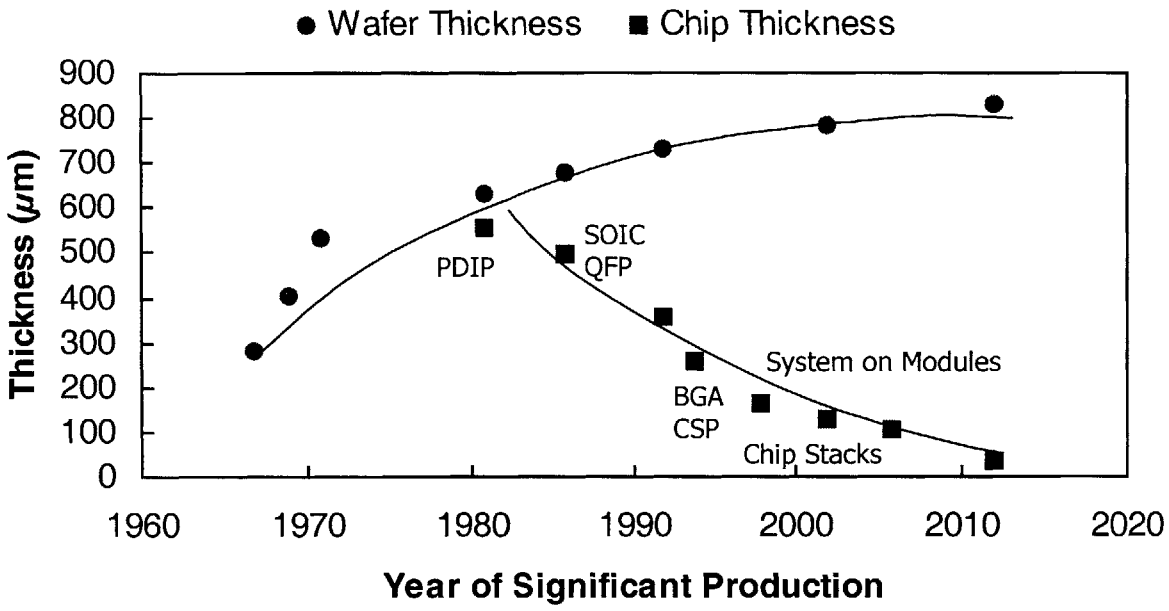

Figure 1-2. Chip and wafer thickness roadmap [32]. Chips thinner than 150 μm are expected in the next 10 years.

thinner chips [32]. For these reasons, we have chosen to use thin substrates of 75 to 170-μm thick for our work.

1.3 Thesis Goals and Outline

The ultimate goal of this thesis was to develop an isolated, substrate-via fabrication process and to characterize the via impedance at RF frequencies. We endeavored to obtain as high an aspect ratio as possible. The process required the development and integration of several major processing steps. Chapter 2 describes the fabrication of the substrate vias in detail. In order to measure the impedance using scattering or *S*-parameters at frequencies up to 6 GHz, we designed the test structures described in Chapter 3. Chapter 3 also discusses the measurement setup used to obtain the impedance data and results of this data.

The design and fabrication of Faraday cages using these substrate vias is explained in Chapter 4. We discuss the need for isolation in SOC applications and the impact of our Faraday cages on the reduction of crosstalk.

Finally, Chapter 5 summarizes the conclusions of this work and suggests future work to improve the fabrication and characterization of the substrate vias, and to integrate the vias in an actual transistor.

Chapter 2

Fabrication Technology

Development of a successful fabrication process to produce these substrate vias was the heart of this research. The availability of the Deep Reactive Ion Etch (DRIE) tool was imperative because of its ability to etch vias from the frontside with near-vertical sidewalls that achieved the high aspect ratios to which we aspired. We also needed a metal that could fill a high-aspect ratio via without voids. This lead to the choice of electroplated copper because of its low-resistance, high electromigration immunity, and its proven ability to fill high aspect ratio structures. Cu will also be widely used in Si in the future. Because copper diffuses readily into silicon, which can alter the threshold voltages of transistors, a conformal diffusion barrier liner was necessary. Also, in order to route different signals using these substrate vias, an insulating liner was desirable. For these two reasons, we chose silicon nitride as the liner material. An illustration of our substrate-via concept is depicted in Fig. 2-1. To keep this a back-end process, no step surpassed 400°C. All fabrication steps were developed and executed at the Microsystems Technology Laboratories (MTL) at MIT.

2.1 Test Vehicle

In order to fabricate substrate vias on thin substrates, 75 to 170-μm thick, without using such fragile starting material, we developed a test vehicle on silicon-on-insulator (SOI) wafers. The device layer was intended as the substrate for via fabrication, while the handle wafer strengthened wafer integrity. Holes etched in the handle wafer from the backside using KOH gave access to the buried oxide (BOX) and the underside of the device layer (when the BOX is etched) while still maintaining wafer integrity. The manufacture of SOI wafers for this process and the backside KOH etch are described in sections 2.1.1 and 2.1.2.

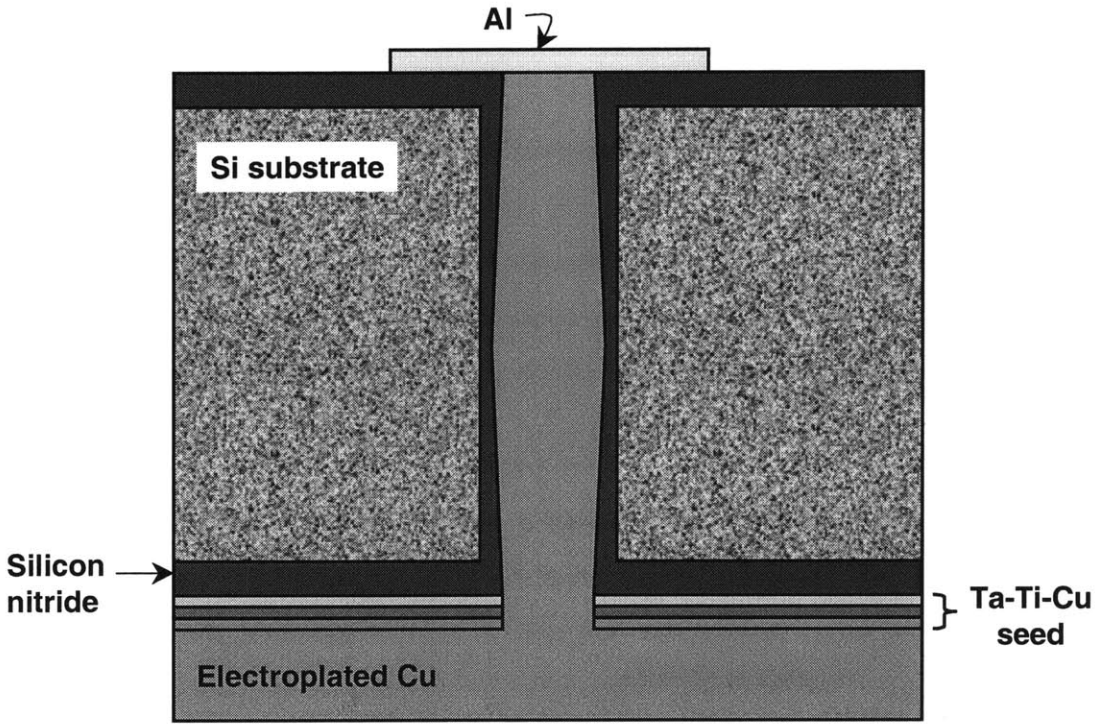

Figure 2-1. Conceptual drawing of a substrate via conformally lined with silicon nitride and filled with Cu with an Al pad connected to the top of the via.

The via fabrication process contains three main steps: (1) via etch from the front of the wafer using an anisotropic deep reactive-ion etcher (DRIE) in a time-multiplexed inductively-coupled plasma, (2) deposition of conformal silicon nitride liner from the front and the back of the wafer by PECVD, and (3) via filling with copper by electroplating. Each of these three steps was developed independently. For ease of imaging, our via technology was first characterized by fabricating trenches. Once fully developed, the steps were integrated into one process to fabricate vias.

A pictorial representation of the integrated process flow for substrate-via fabrication is depicted in Fig. 2-2. Appendix B contains the detailed process steps and recipes. The process began with a 100-mm diameter SOI wafer with a device layer or substrate thickness between 75 and 170 μm, <100> orientation, and varying resistivity. First, 2500 Å of silicon nitride was deposited

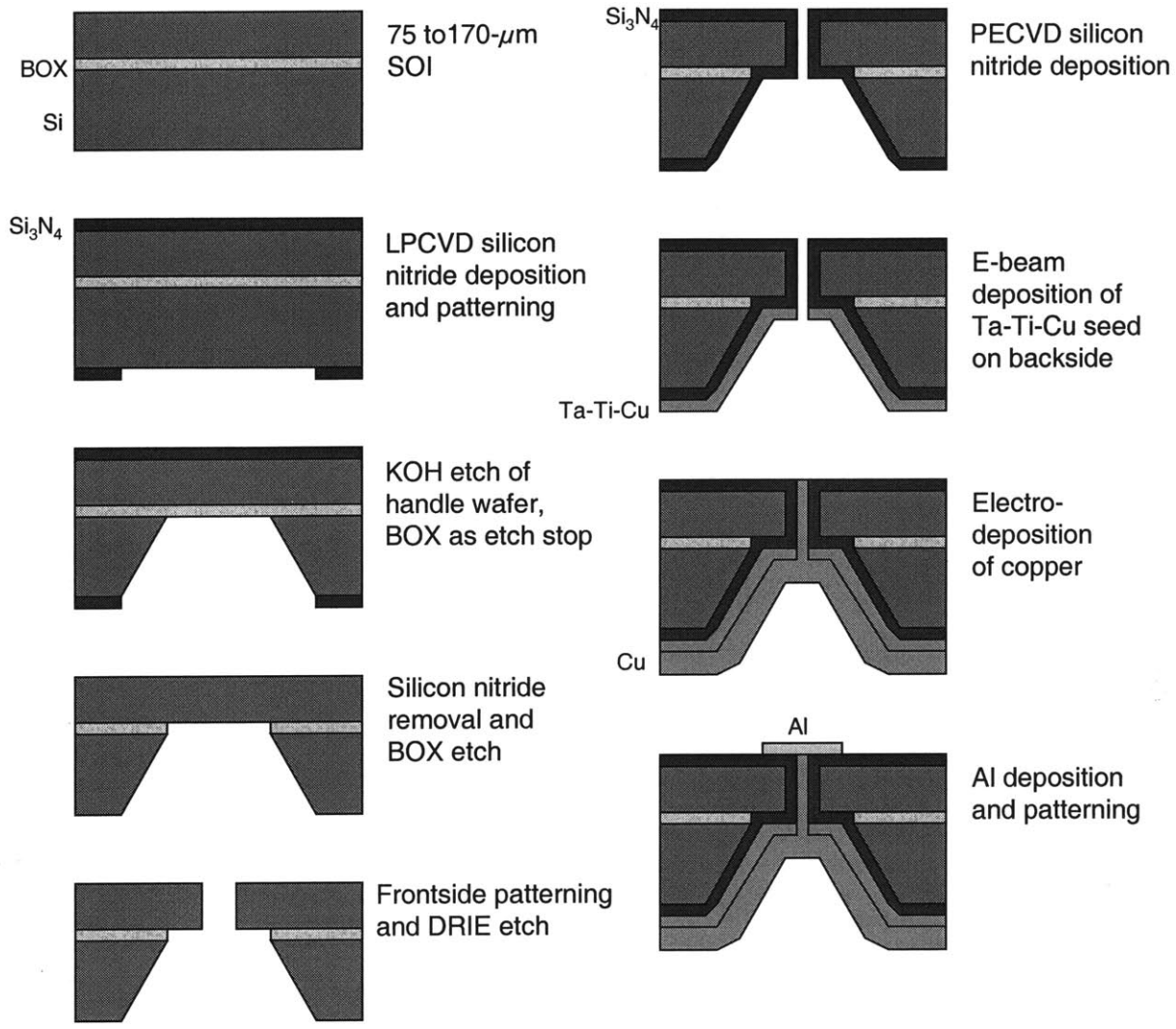

Figure 2-2. Cross-sectional view of the isolated substrate-via process flow.

over the entire wafer, front and back using low-pressure chemical vapor deposition (LPCVD). The nitride was patterned on the backside of the wafer using standard photolithography techniques, and the patterned nitride was etched using CF_4. The silicon nitride acted as a mask for the subsequent KOH etch step. The wafer was etched in a solution of KOH:H_2O (20 wt% KOH) with surfactant at 80°C. The buried oxide of the SOI wafer acted as an etchstop for the KOH etch. After the etch and post-KOH clean, the silicon nitride was removed in 85% hot phosphoric at 175°C, and the exposed BOX was removed in BOE (7:1). Next, the frontside was coated with photoresist and patterned. The exposed silicon was etched in the DRIE to create the

through-wafer vias. Once the vias were etched all the way through the substrate, silicon nitride was deposited using plasma-enhanced chemical vapor deposition (PECVD) on the front and back of the wafer. Before electroplating, a seed of 250 Å of Ta, 250 Å of Ti, and 2000 Å of Cu was e-beam evaporated on the backside of the wafer, so that the via would fill from the bottom to the top in the Cu electroplating step. This method produced no seams or voids when electroplating. The last step was to deposit Al by e-beam and pattern it to form the test structures. An SEM cross-section of a finished via is shown in Fig. 2-3. Fig. 2-4 depicts detailed cross-sections of a through-wafer trench and via to show the conformal silicon nitride liner between the Si substrate and the Cu trench or via.

2.1.1 SOI Wafer Bonding

Because of the thick device layer required for this test vehicle, bonded-SOI wafers were necessary as the starting material. Several bonded-SOI wafers were acquired from Virginia Semiconductor and BCO Technologies. However, for quicker turn-around time, SOI wafers were fabricated at MIT and polished at Lincoln Laboratories by Skip Hoyt.

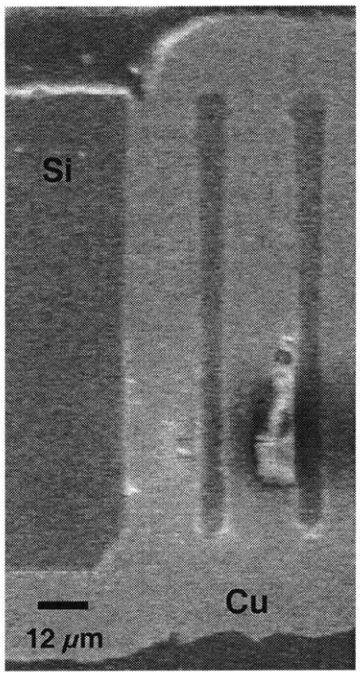

Figure 2-3. SEM cross-section of a substrate via with an aspect ratio of 7. The substrate is 103-μm thick. The via is 14-μm wide.

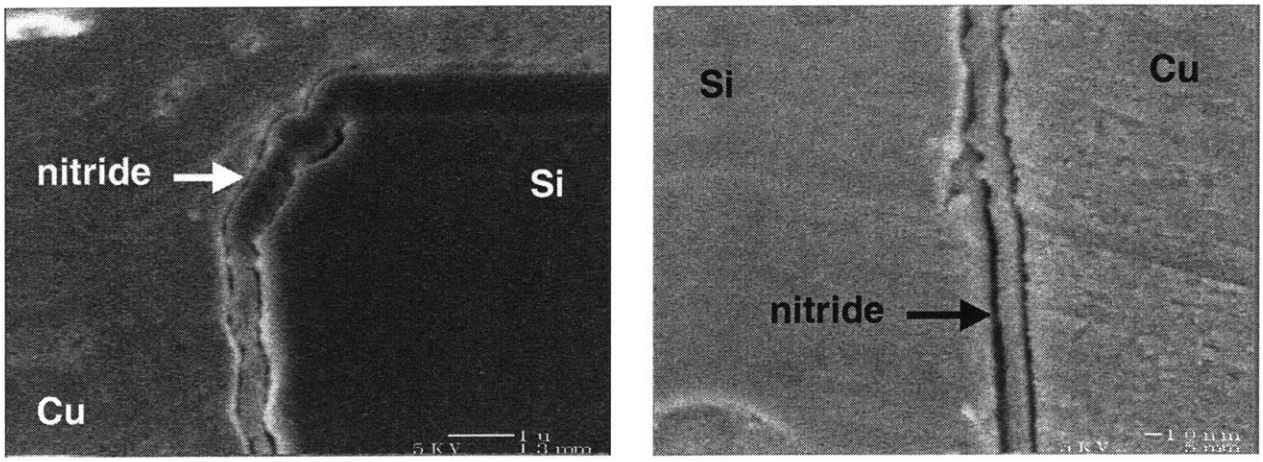

Figure 2-4. Left: SEM cross-section of top-sidewall of a 14-μm wide by 103-μm deep via . The nitride liner is 550-nm thick at the surface and 500-nm thick 1 μm down from the surface. Right: cross-section of the mid-sidewall of a 38-μm wide by 106-μm deep trench. The nitride is 120-nm thick. Both are conformally lined with nitride and filled with Cu.

A simple approach called direct bonding uses the contact attractive forces between smooth, flat surfaces to bond wafers together [33]. For a 100-mm wafer, a roughness of less than 10 Å, and a bow of less than 5 μm is necessary for a good quality bond. This applies to Si-Si bonds as well as to Si-SiO_2 bonds. Surface preparation of the surfaces requires a clean procedure to hydrate the surface. Then the two wafers are contacted at a single central point, which creates a contact wave to prevent trapping particulates or air. Lastly, an anneal at greater than 1000°C strengthens the bond to near silicon single-crystalline strength.

In our case, we require two wafers, one with 1 μm of SiO_2 thermally grown on the polished side, and one double-side polished (DSP), <100> wafer 400 to 450-μm thick. The polished frontside of the DSP wafer was bonded to the SiO_2 film grown on the polished frontside of the other wafer. The SiO_2 film became the buried oxide (BOX). The bonded wafers were annealed at 1000°C in nitrogen for 70 minutes. If the surfaces were not perfectly clean or if there were protrusions at the surface, voids would form after bonding that could be easily seen with an infrared camera (Fig. 2-5). After the anneal, the unpolished side of SiO_2 wafer was polished back so that the device layer was between 75 to 170-μm thick. See Appendix A for the detailed process flow for SOI wafer bonding.

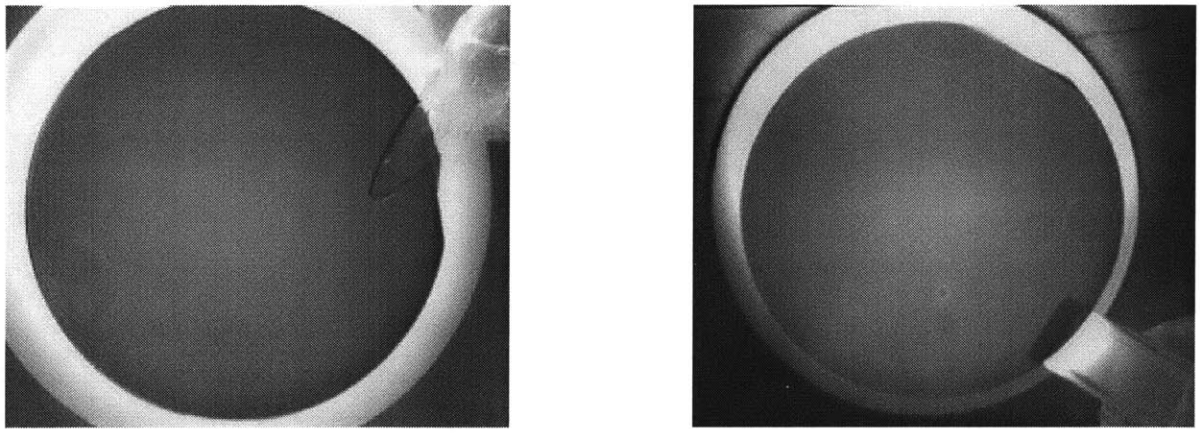

Figure 2-5. Left: infrared image of a good quality SOI bond with no voids. Right: SOI bond with defective voids.

2.1.2 KOH Etching

The KOH etch allows access to the backside of the device layer without sacrificing the integrity of the wafer. It also provides a slanted sidewall of 54.7° from the Si surface so that the Cu seed will deposit conformally on the sidewall. This characteristic slanted sidewall of the KOH etch on a <100> wafer is due to the high etch selectivity of the <100> plane to <111>. The <100>:<111> etch rate ratio varies from 100:1 at room temperature to 30:1 at 100°C [34]. The etch rate of <100> Si is approximately 80-90 μm/hr at 80°C. Fig 2-6 contains an illustration of the backside and cross-section of a KOH-etched hole in the handle wafer of an SOI wafer and a photograph of a KOH-etched wafer.

Silicon nitride is considered the perfect masking material for KOH since no etch rate can be measured [34]. However, pinholes in the nitride can cause pitting in the silicon surface. Increasing the thickness of the nitride decreases the number of pinholes. Silicon dioxide, in comparison, has a finite etch rate of approximately 0.2 μm/hr in 20% KOH at 80°C, or an etch rate ratio for SiO_2:<100> Si of approximately 300:1 [34]. The high selectivity renders SiO_2 suitable as an etchstop, which is the function of the BOX.

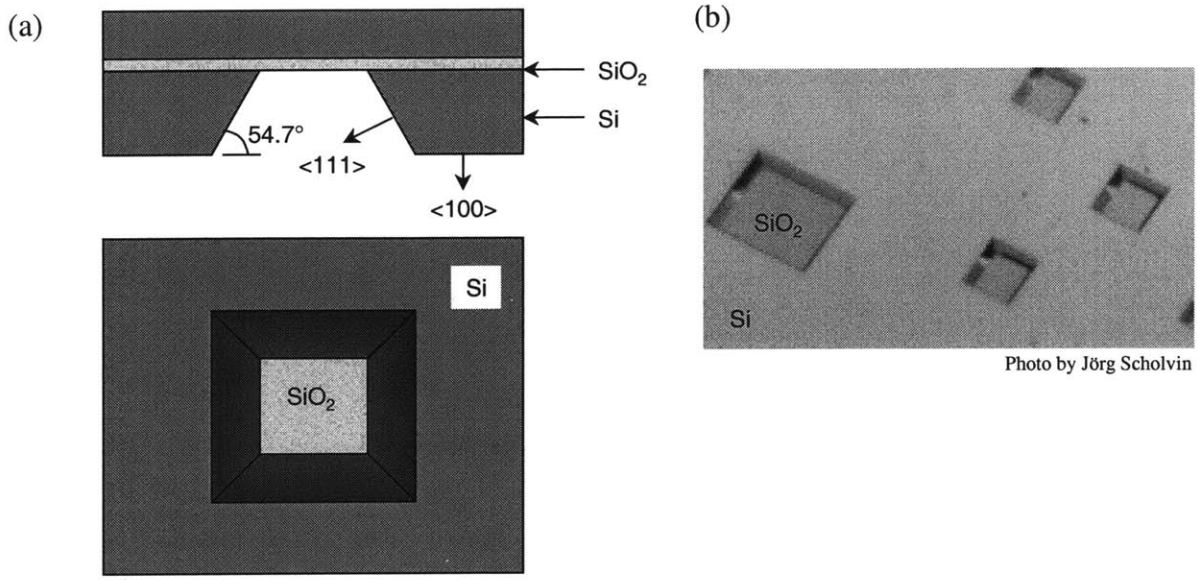

Figure 2-6. (a) Cross-sectional and backside sketch of a KOH-etched hole in Si handle wafer with an BOX etchstop. The preferential etching of <100> Si to <111> gives the 54.7° angle of the sidewall. (b) Photograph of a wafer with KOH-etched holes and BOX exposed.

The surfactant added to the KOH solution acts to lower the surface tension of the solution so that bubbles that form will not stick to the Si surface and reduce etching at that point. This gives a smoother sidewall.

A post-KOH clean is necessary in order to re-enter the CMOS-compatible laboratory. The clean consists of a double pirahna clean, first in KOH-contaminated glassware, and a second in CMOS-compatible glassware. This is followed by a 1-minute dip in HF (50:1).

2.2 Deep Reactive Ion Etch (DRIE)

2.1.1 DRIE Tool Specifications

The DRIE tool used in this process is a Surface Technology Systems time-multiplexed inductively coupled plasma (ICP) etcher. This tool is readily used by the microelectro-mechanical systems (MEMS) community to create silicon-based micromachines with high-aspect ratio structures. The DRIE uses a time-multiplexed deep etching technique developed by Robert Bosch GmbH that is able to etch structures with near-vertical sidewalls [35]. As shown

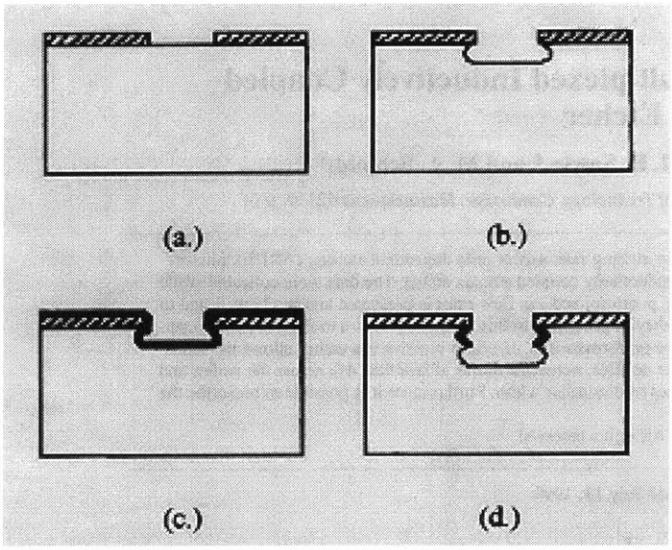

Figure 2-7. DRIE time-multiplexed etch: (a) patterned photoresist on a wafer, (b) etch cycle, the isotropic etch is noticeable, (c) passivation cycle, a Teflon-like film is deposited on all surfaces, and (d) next etch cycle, passivation film is removed from all surfaces exposed to ion bombardment and then the etch proceeds. Illustration courtesy of A. Ayón [35].

in Fig. 2-7, this technique uses a sequence of alternating etch and passivation cycles to produce an aggressive anisotropic etch. During the etch cycle, SF_6 etches silicon isotropically. Then in the passivation cycle, C_4F_8 flows to form a Teflon-like polymer film on all surfaces, including the sidewalls and bottom of the via. During the next etch cycle, polymer at the bottom of the via is removed by ion bombardment, leaving the polymer on the sidewalls intact. Protection of the sidewalls during subsequent etch steps gives the via its vertical sidewalls with a characteristic scalloping (Fig. 2-8).

Both photoresist and SiO_2 are used as masking material for DRIE. Photoresist is the traditional choice because of the fewer fabrication steps required. However, for longer etches or definitions of smaller features, SiO_2 is preferred because of its greater etch selectivity. Selectivity for photoresist can vary from 60 to 75:1. SiO_2 selectivity can be as high as 150:1.

Several parameters of the DRIE can be varied to produce desired etch rates and selectivities [35]. Length of etch and passivation cycles, cycle overlap time, gas flow rate, and applied electrode and coil power can be controlled independently. Also, pressure can be controlled indirectly by

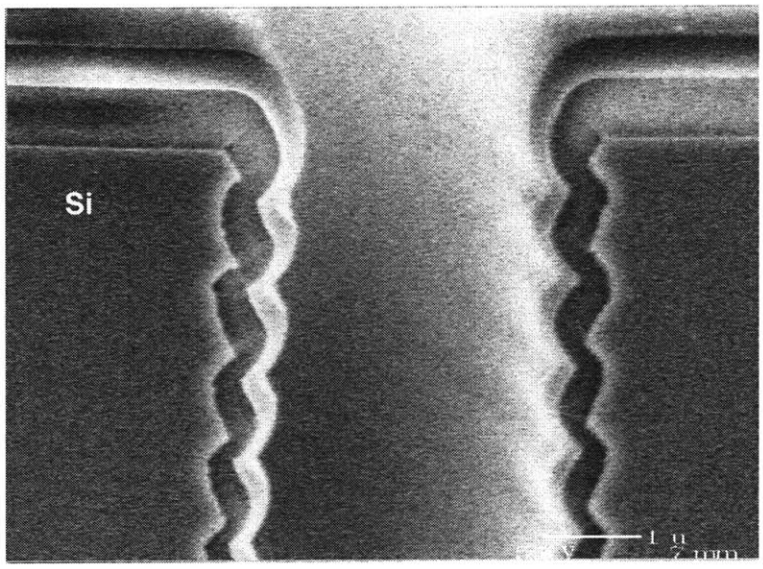

Figure 2-8. SEM cross-section of a trench etched in the DRIE. The scalloping of the walls is clearly evident. This trench has a film of silicon nitride and TEOS deposited after etching.

adjusting either the automatic pressure control (APC) valve or gas flow. The effects of varying these parameters are explored in papers [35-38].

2.1.2 DRIE Results

To first characterize the etch and ease imaging of cross-sections, we etched trenches in bulk Si. The trench opening widths varied from 2 to 64 μm. We have achieved aspect ratios of 49 for trenches (Fig. 2-9). Several interesting observations of the DRIE have been previously reported in [35-37]. The most significant aspects for this research were the dependence of aspect ratio on etch rate and the "footing" effect seen on SOI substrates. Also, we will discuss another undesirable effect from the DRIE that caused "pockets" to etch into the sidewalls, which made the sidewalls difficult to line conformally.

In [35] and in our own experiments, we found that the etch rate decreased with increasing aspect ratio. Our results, depicted in Fig. 2-10, show that the dependence was noticeable but small, and that for aspect ratios as high as 20, the decrease in etch rate was less than 15%. This dependence is due to reactive ion etch lag (RIE-lag) common in fluorinated plasmas [35, 39]. A high SF_6 flow rate minimizes aspect ratio dependence of etch rate, with a maximum SF_6 flow rate of 140

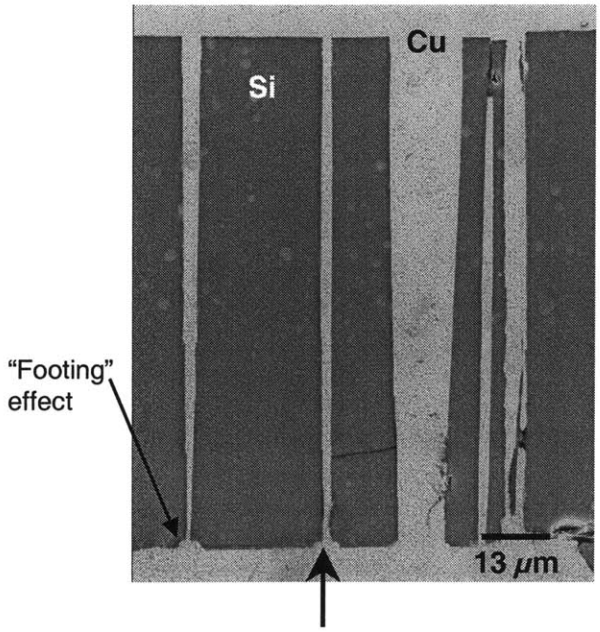

Figure 2-9. Best DRIE and Cu electroplating result: a trench of aspect ratio 49 (2-μm wide by 97-μm deep) filled with Cu without seams or voids. The footing is present due to an earlier process which had an oxide etchstop for the DRIE.

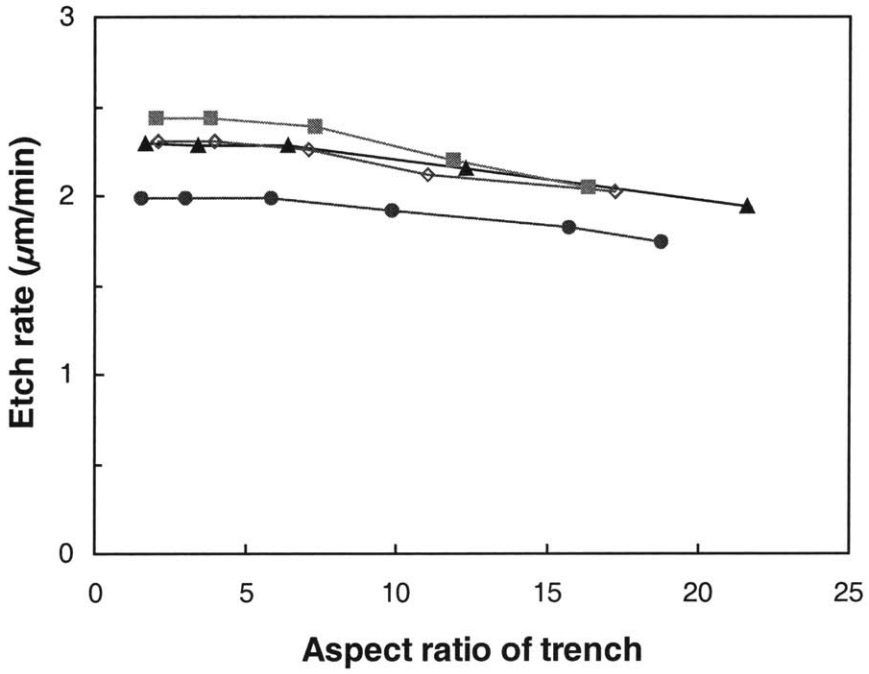

Figure 2-10. DRIE etch rate vs. aspect ratio for trenches in different wafers. For aspect ratios as high as 20, the decrease in the etch rate is less than 15%.

sccm reported in [35], which we used. Another observation was the lateral etching of trenches and vias due to the anisotropic photoresist profile [35]. The sloping of the profile (Fig. 2-11) gave a wider final opening of the trench and via. For every 100 μm etched in depth, the opening widened by 1 to 2 μm. This gives the via a slight narrowing towards the bottom and a lower aspect ratio than printed on the mask. Moreover, it limits the attainable aspect ratio to 50 on a 100-μm wafer.

"Pockets" etched into the sidewalls of trenches and vias were observed as another by-product of the DRIE. This feature originated from a discontinuous coating of the sidewalls by the polymer during the passivation cycle [40]. Any holes in the polymer became pockets in the next etch cycle and increased in depth in subsequent etch cycles until etch species could no longer reach the bottom of the pocket (Fig 2-12). This undesirable characteristic is detrimental for conformal lining with nitride. We conducted preliminary experiments to reduce or eliminate the pockets by increasing the C_4F_8 flow rate, C_4F_8 active time, and APC angle independently. However, the pockets persisted. Further work needs to be performed to understand and eliminate this effect.

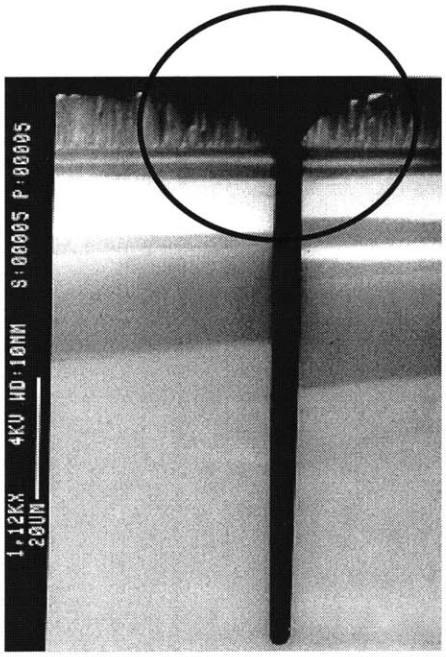

Figure 2-11. SEM cross-section of the sloping photoresist profile that widens the patterned opening during DRIE, but narrows the trench in the bottom half.

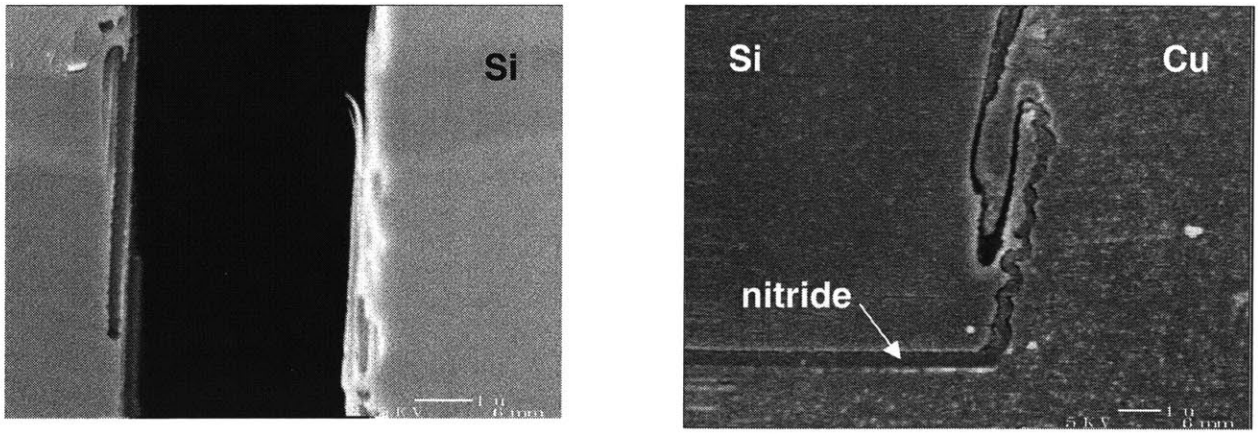

Figure 2-12. Left: "pockets" etched by the DRIE in the sidewall of a trench 5-μm wide by 128-μm deep. Right: bottom of a trench 65-μm wide by 65-μm deep lined with nitride and filled with Cu. A pocket was etched into the sidewall during DRIE and could not be corformally lined by nitride.

Our initial fabrication process used the BOX as an etchstop for the DRIE. Overetching of the silicon on top of the BOX caused a notching or "footing" at the bottom interface as seen in Fig. 2-13 [37, 41]. This feature arises from the negative charging of the sidewalls near the opening and positive charging of the bottom SiO_2 from the anisotropic ion flux of the plasma (Fig. 2-14). The negative charge at the surface narrows the view factor of the plasma and limits the flux of electrons to the bottom sidewalls and BOX. The positive charging of the BOX causes the deflection of the ions to the bottom sidewall creating the notching. The non-uniformity in the sidewalls that the footing produced made conformal lining of the via at the bottom impossible as shown in Fig. 2-15. We therefore chose to remove the BOX before DRIE to eliminate the footing. Without the BOX, the DRIE proceeded to etch all the way through the substrate. Any overetch allowed ions to bombard and etch the backside of the wafer but on a much smaller scale than the footing. The roughness caused by this bombardment is easily lined by silicon nitride as shown in the SEM in Fig. 2-16.

2.3 Silicon Nitride Insulating Barrier Liner

Our expectations for the via lining were twofold. First, the liner must be a barrier to the Cu used to fill the via because migrating Cu ions can alter the threshold voltage of transistors. Second, in order to be able to route power and ground on the same chip, the substrate vias must be insulated

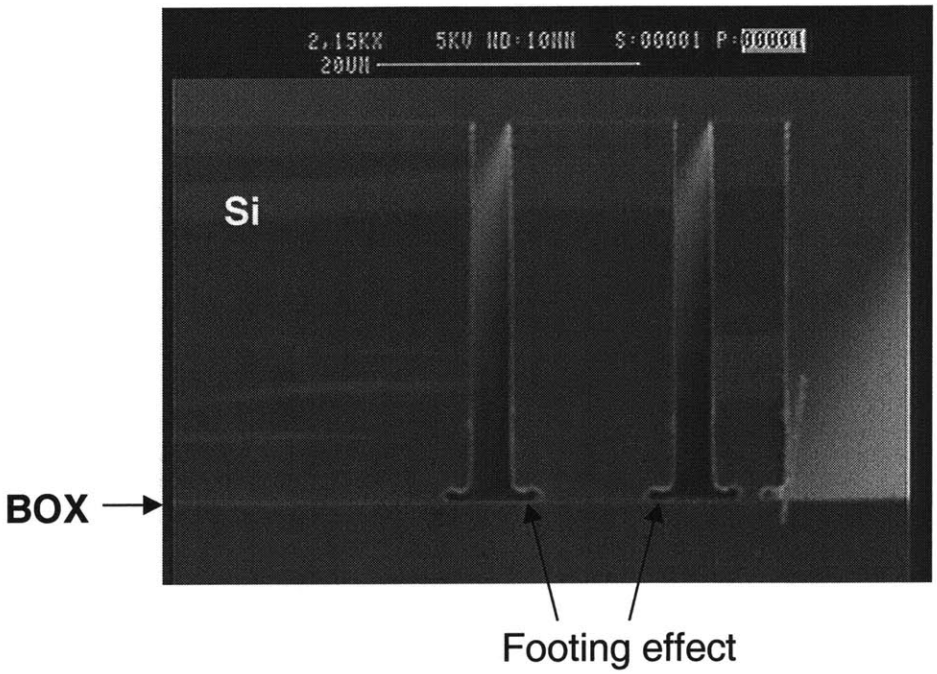

Figure 2-13. DRIE on a 35-μm SOI substrate with a silicon dioxide etchstop. The footing effect is noticeable.

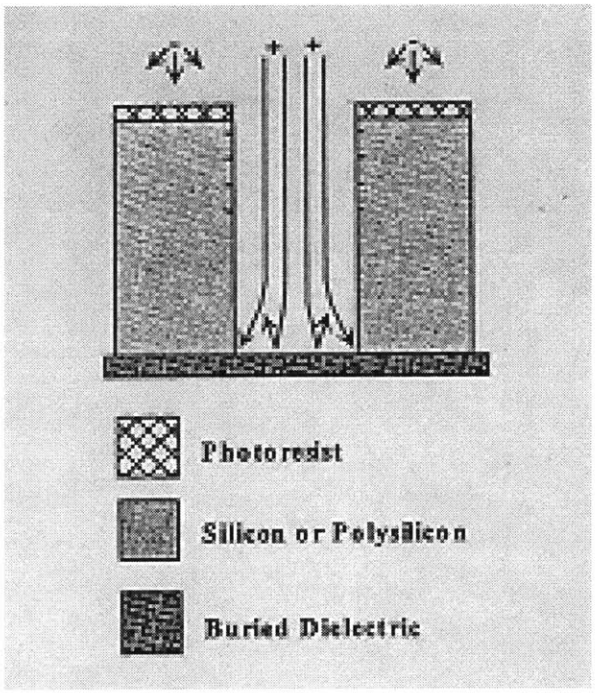

Figure 2-14. Footing originates from the isotropic flux of electrons on the sidewalls of the feature that creates a negative charge near the opening. The flux of electrons to the lower sidewalls and bottom of the feature is limited by the reduced view factor to the plasma and the repulsive negative charging near the opening. The bottom regions of narrow spaces charge positively due to the greater monodirectional ion flux. Illustration courtesy of A. A. Ayón [37].

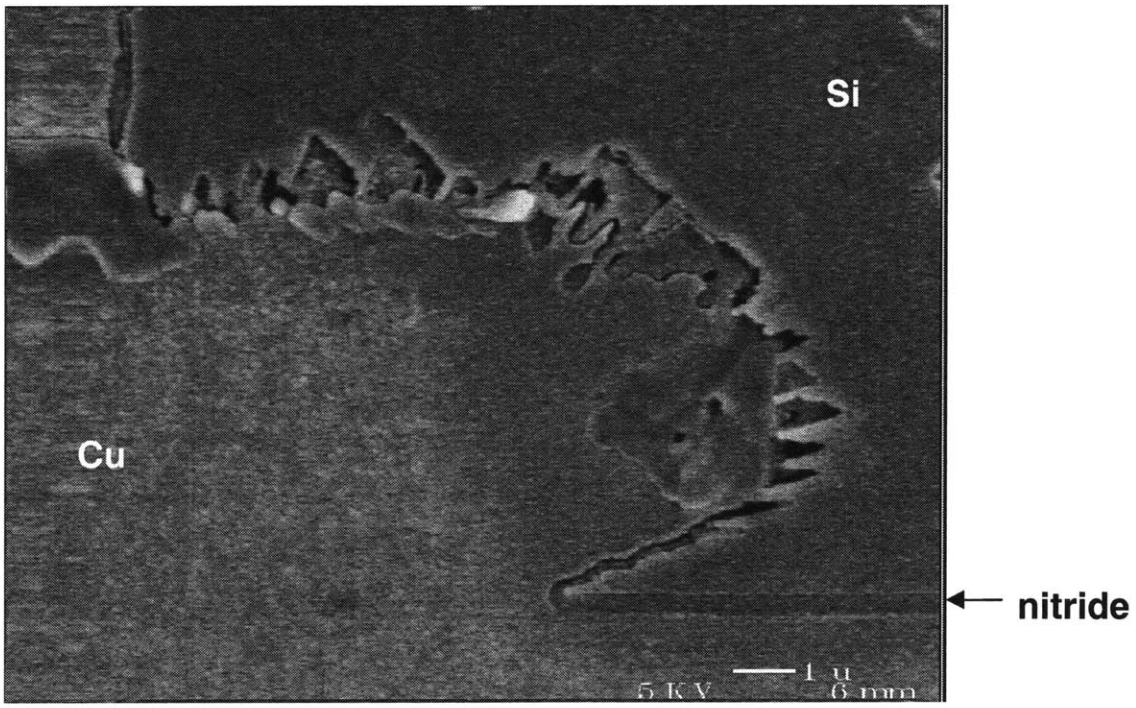

Figure 2-15. Closeup of a foot at the bottom of a DRIE-etched trench. The trench is lined with silicon nitride and filled with Cu. It was impossible for the nitride to conformally line the foot due to the surface irregularities.

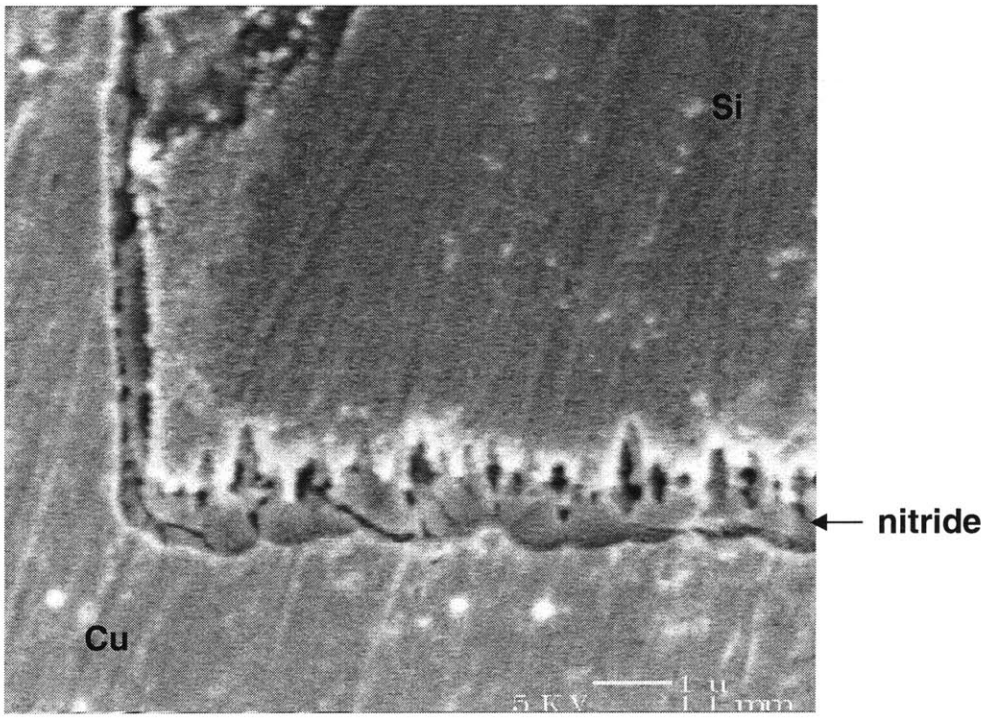

Figure 2-16. SEM cross-section of the bottom of a via lined with nitride and filled with Cu. The backside surface of the wafer is irregular due to ion bombardment in the DRIE when the via is overetched. However, the nitride can still conformally line this surface.

from the Si substrate and each other. Thus, we needed an insulating, diffusion barrier liner. Silicon nitride is a proven insulator in VLSI technology [42] including Cu interconnects [43], so we have focused on its abilities as a barrier to Cu diffusion in the next section.

2.3.1 Silicon Nitride as a Barrier Liner

Because Cu has become the desired interconnect metal for VLSI circuits, considerable research has been published characterizing suitable dielectrics and barrier materials to prevent Cu diffusion into Si. Many conducting barrier materials have been developed, such as TiN, TaN_x, and WN_x; Ta_xSi_y and W_xSi_y; and combinations of these [44-51]. The basic premise of a metal diffusion barrier is to create an amorphous form of the metal because grain boundaries act as fast pathways for Cu diffusion. For example, using just Ta as a liner allows Cu to diffuse through grain boundaries and defects at temperatures of 450°C [44, 52]. However, these amorphous barriers fail when temperatures reach above the crystallization temperature of the metal. Adding impurities like nitrogen to stuff the grain boundaries further prevents diffusion of Cu [44].

An important drawback of metal barrier liners is their higher resistivity and permeability than Cu. When operating at RF frequencies, most of the current flows near the perimeter of the via due to the skin effect. Having a high-resistivity liner only degrades the performance of the via [53, 54]. This gave us another compelling reason besides isolation to use an insulating liner.

Amorphous dielectric films like SiO_2, Si_3N_4, and SiO_xN_y were logical choices for Si. Even though SiO_2 is more conformal than Si_3N_4, unfortunately, SiO_2 has been proven to be a poor barrier to Cu diffusion [50, 54-57]. However, Si_3N_4 and SiO_xN_y are both effective in preventing Cu diffusion with similar results [50, 54, 57]. In Pai *et al.* [57], 2000 Å of SiO_2, 2000 Å of PECVD SiO_xN_y and 1500 Å of LPCVD Si_3N_4 were deposited on Si, and Cu was evaporated on top of the dielectric to form an MOS capacitor. After heating the samples to 300°C and biasing at 20 V, Pai *et al.* found a 2-V shift in C-V measurements for the SiO_2 sample, but no shift for SiO_xN_y or Si_3N_4. Li *et al.* [50], measured flatband voltages of similar MOS capacitors and also found a 2-V shift for SiO_2, and a less than 0.1-V shift for SiO_xN_y and Si_3N_4. The results in Adema, *et al.* [54] also confirm the effectiveness of SiO_xN_y and Si_3N_4 as barrier materials. Due to our greater familiarity with Si_3N_4, we chose Si_3N_4 over SiO_xN_y. We chose to keep the

substrate-via process a back-end process, so LPCVD Si_3N_4 was not a viable option due to its high temperature of deposition. Therefore, we deposited Si_3N_4 by PECVD at 400°C. Because of the presence of pinholes in the Si_3N_4 film, a minimum thickness of 500 Å is necessary to be an effective barrier to Cu [54].

2.3.2 Silicon Nitride Conformality

To take advantage of the insulating and barrier properties of silicon nitride, the liner had to be conformal to the sidewalls of the via. Using the Novellus Concept-1, we characterized the conformality of PECVD silicon nitride by examining cross-sections of silicon nitride deposited in trenches etched in bulk Si. The Concept-1 is a multi-station, dual-frequency, plasma deposition tool. The five stations allow for concurrent processing of more than one wafer and give better uniformity. The dual-frequency provides increased low-frequency ion bombardment for better sidewall density and integrity. At high frequency (13.56 MHz), ions are immobile in the RF field due to their mass, but at lower frequencies (< 1 MHz), ion bombardment increases significantly. This low-energy ion flux enhances the surface mobility of precursors by reducing their sticking coefficients, which improves sidewall coverage [58-60]. By combining high and low frequencies, we gain the stable discharge and substrate coupling of high frequency and the ion bombardment of low frequency [58].

Nitride deposition into trenches etched in bulk Si followed the general shape illustrated in Fig. 2-17. The thickness of the nitride was greatest at the surface of the wafer and decreased further down the trench. For increasing aspect ratios, the drop in nitride thickness became more pronounced until there was no nitride present at the bottom sidewall of the trench. This indicated that the bottom sidewall was the most critical dimension for silicon nitride conformality. To quantify the conformality, we took measurements of nitride thickness at four places on the trench: the surface, the sidewall 1 μm from the surface, the bottom, and the sidewall nearest the bottom. These measurements are plotted in Fig. 2-18 against aspect ratio, with the top, bottom, and bottom sidewall measurements normalized to the surface thickness. The aspect ratio was the dominant variable for sidewall coverage. The nitride thickness at the top sidewall remained relatively constant with aspect ratio. The thickness decreased dramatically at the bottom of the trench, thinning rapidly with aspect ratio. The bottom sidewall thickness followed this same

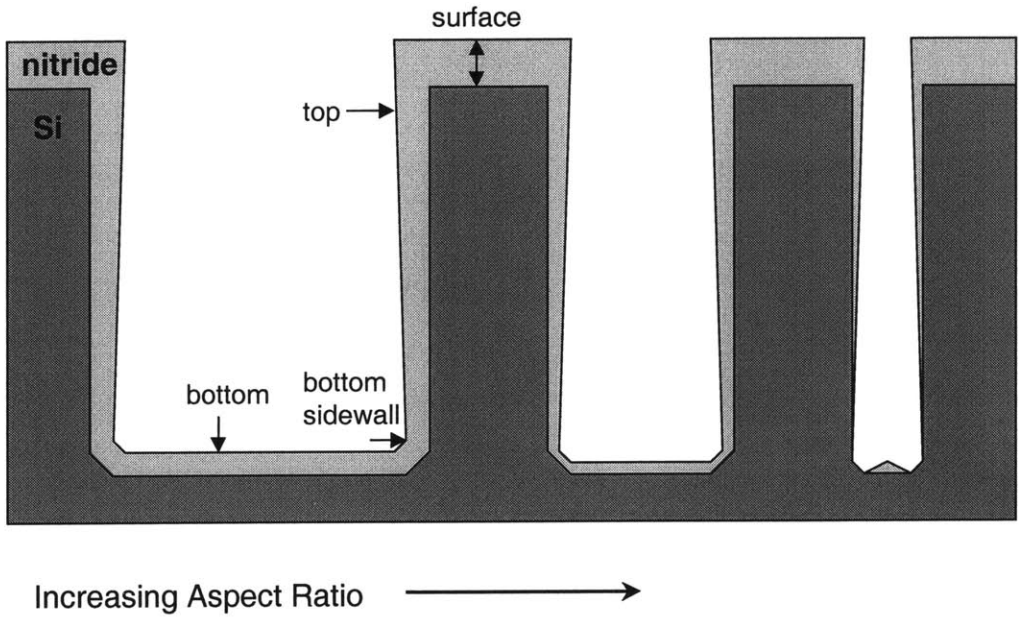

Figure 2-17. Illustration of silicon nitride deposition in trenches or vias for different aspect ratios.

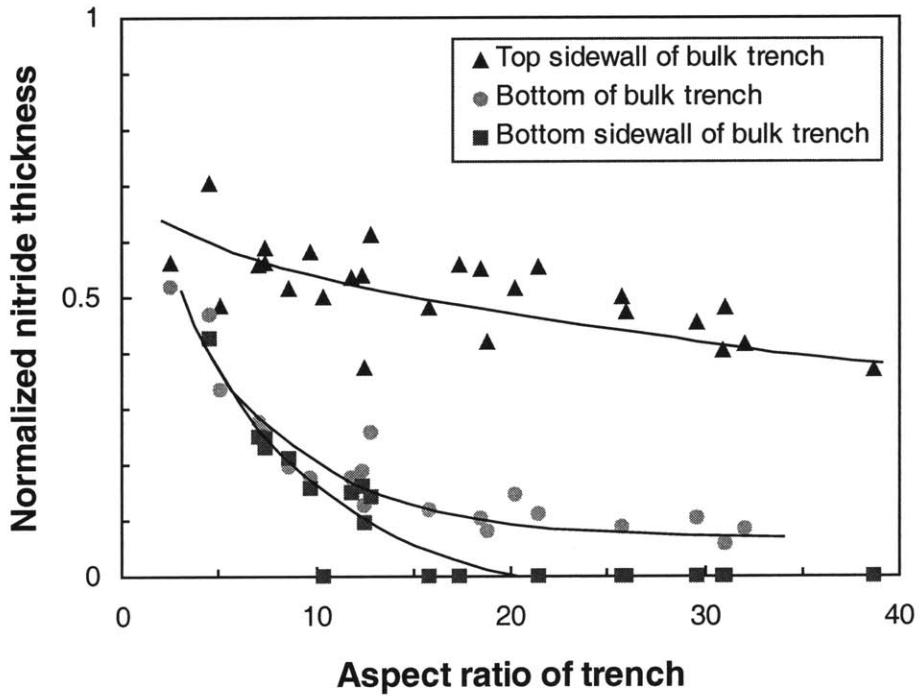

Figure 2-18. Normalized PECVD silicon nitride thickness vs. aspect ratio of a trench etched in *bulk*. The liner thickness was normalized to the surface thickness. Top sidewall measurements were taken 1 μm down from the surface. The top sidewall thickness is relatively independent of aspect ratio. However, the bottom and bottom sidewall thicknesses decrease dramatically with aspect ratio. At an aspect ratio of about 15, the liner is nonconformal in the trench.

trend but drops off at a lower aspect ratio. These results show that the nitride is thinnest at the bottom sidewall, and for aspect ratios greater than about 15, the nitride is not present at the bottom sidewall and therefore, is not conformal. Fig. 2-19 shows SEM cross-sections of silicon nitride deposited in bulk trenches with conformal and non-conformal nitride liners. To measure the nitride thickness accurately, a tetraethyl orthosilicate (TEOS) film was deposited on top of the nitride to define the edge of the nitride. After cross-sectioning, the nitride was etched back a few hundred Å in 85% phosphoric acid at 150°C to delineate the materials. TEOS is more conformal than nitride, so it gave a continuous interface that allowed us to define the nitride in the trench.

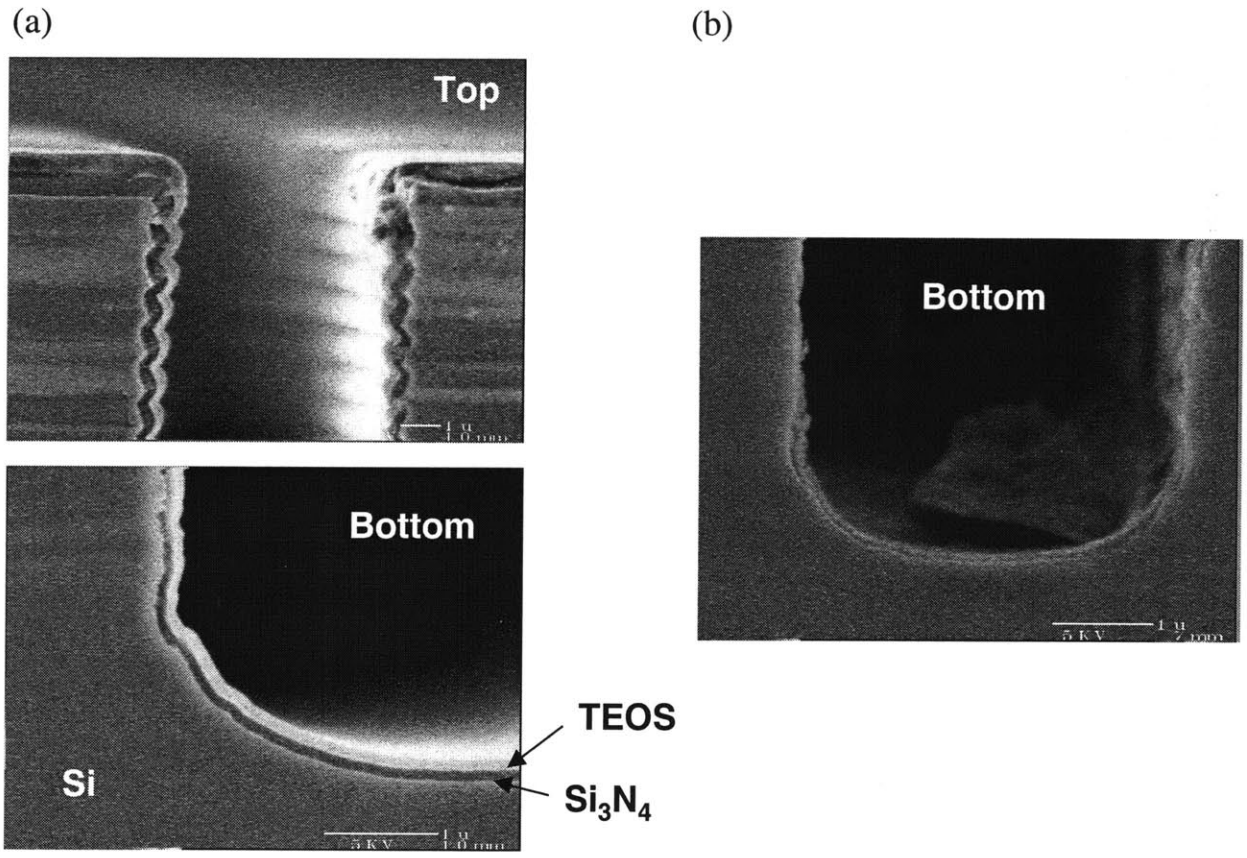

Figure 2-19. (a) Trench etched in bulk conformally lined with silicon nitride. This trench is 7-μm wide by 68-μm deep (aspect ratio, A=10). (b) Bottom of a trench with non-conformal nitride. Nitride is present at the bottom but not on the sidewalls. This trench is 5-μm wide by 129-μm deep (A=26).

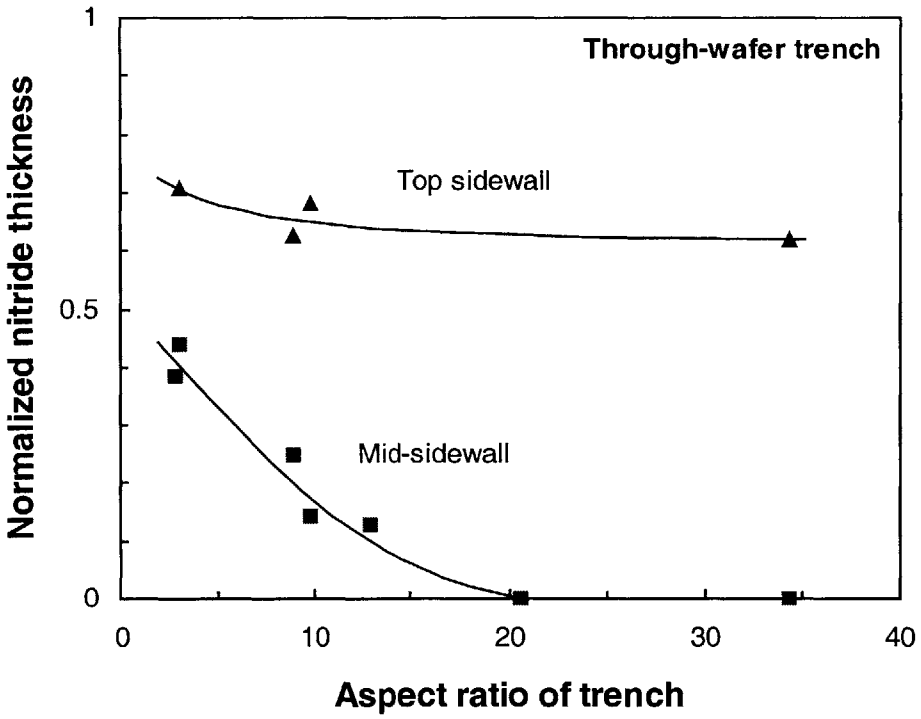

Figure 2-20. Normalized PECVD silicon nitride liner thickness vs. aspect ratio of a *through-wafer* trench. The nitride has been deposited as a double deposition, one on the front and one on the backside at 60% low-frequency power. The liner thickness is normalized to the surface thickness. Mid-sidewall measurements were taken halfway down the trench and top sidewall measurements 1 μm down from the surface. The top sidewall is relatively independent of aspect ratio. However, the mid-sidewall thickness decreases drastically with aspect ratio similarly to the bulk trenches.

Using through-wafer trenches on SOI gave us the opportunity to perform a double deposition of nitride, on the front and backside. Because nitride in bulk wafers was thinnest at the bottom sidewall, this double deposition would have improved the conformality. Fig. 2-20 plots the normalized nitride thickness of a through-wafer trench at the top sidewall 1 μm from the surface and at the mid-sidewall, since the thinnest nitride would be at the middle of the trench in a double deposition. From these results, the double deposition in through-wafer trenches followed the same dependence as the bottom sidewall in bulk trenches with no apparent improvement in conformality. This could be due to the narrowing of the trench during the DRIE, which shrinks the opening at the bottom of the trench to limit the view factor of the plasma from the backside.

To improve the sidewall coverage, van de Ven *et al.* [58] suggests increasing the low frequency power (LFP), stating that step coverage only improves with low-energy ions. They report a peak

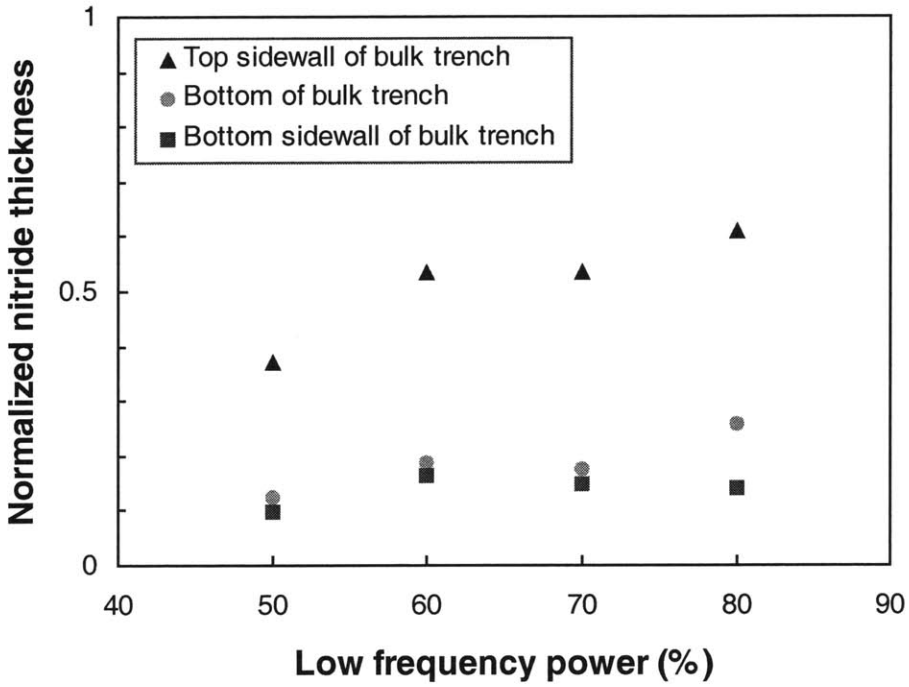

Figure 2-21. Normalized silicon nitride thickness in bulk trenches vs. low frequency power (LFP) of the PECVD tool. From the bottom sidewall measurements, which is the most critical dimension, the best conformality is obtained between 60 and 70% LFP.

improvement in step coverage of 10-12% when the LFP was between 60-70%. In our own experiments on trenches etched in bulk, we confirmed this trend. In Fig. 2-21, we have plotted the normalized nitride thickness versus LFP. Looking at the bottom sidewall, the most critical parameter, we see a peak in thickness between 60 and 70% LFP. In our final processing, we have used 65% LFP. A larger electrode spacing has also been reported to increase conformality [59, 61]. However, we could not pursue this variable with the equipment at MIT. The highest aspect ratio trench lined with conformal nitride was 13 (Fig. 2-22). For vias, it was 7 (Fig. 2-23).

2.4 Copper Electroplating

The semiconductor industry is transitioning from Al to Cu interconnects. Since line dimensions on chip are continuously scaling down, and faster operation calls for higher current densities to flow through these smaller interconnects, reliable and low-resistive wiring is imperative [43, 62].

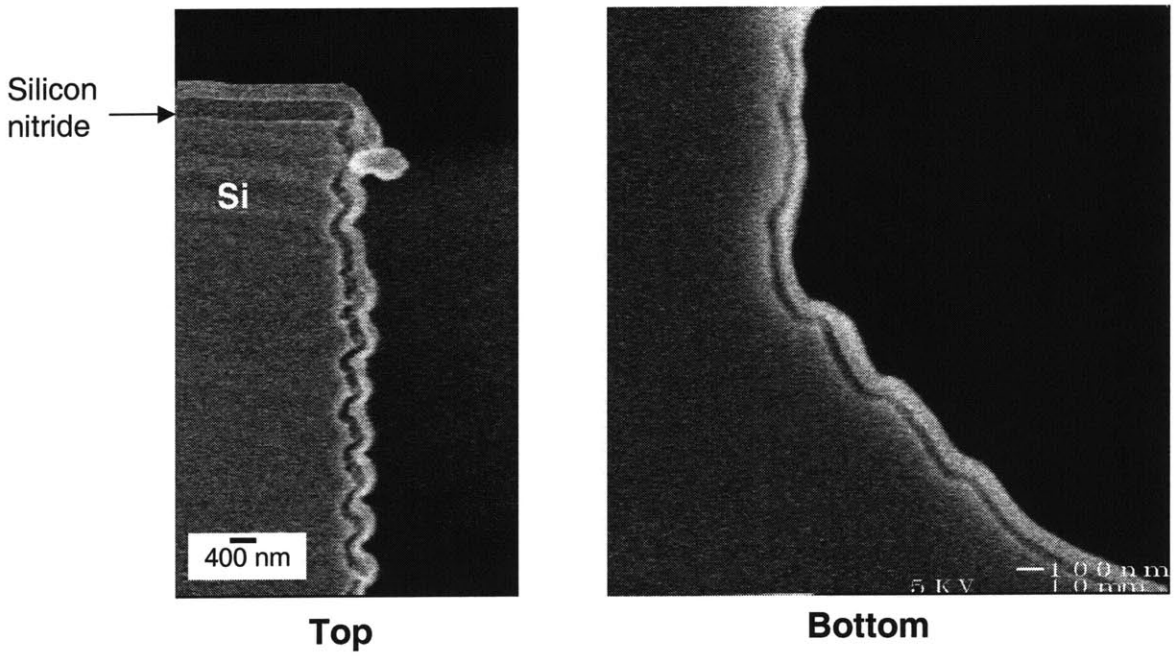

Figure 2-22. SEM cross-section of a trench etched in bulk and conformally lined with silicon nitride. This trench is 10-μm wide by 125-μm deep (aspect ratio, A=13), which is the best conformality confirmed.

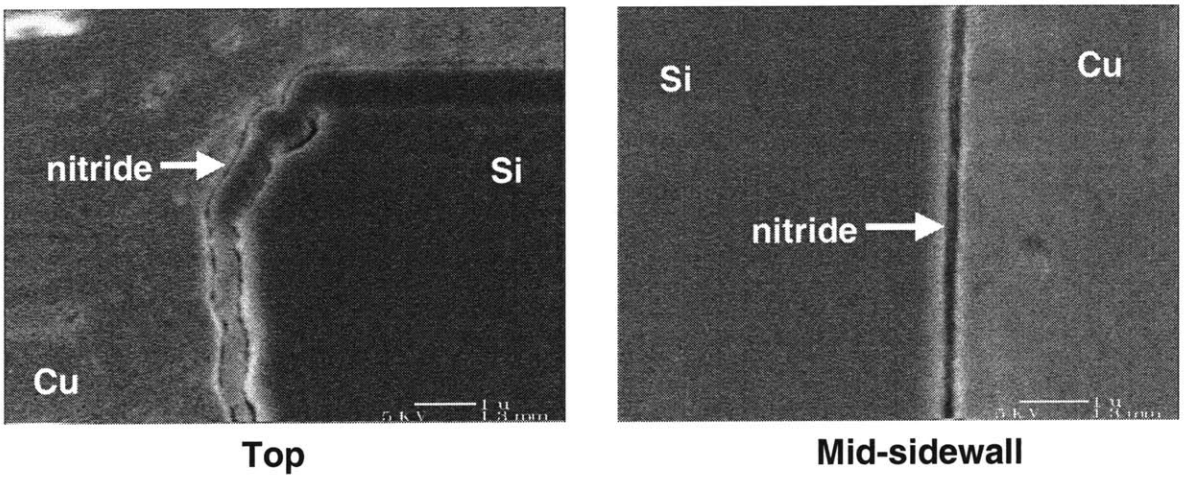

Figure 2-23. SEM cross-section of a through-wafer via conformally lined with silicon nitride. This via is 14-μm wide by 103-μm deep (A=7). This is the best conformality result for vias.

The chief advantage of Cu is its low resistivity, 1.7 μΩ-cm at 22°C for pure Cu. More attainable resistivities for Cu are about 3.5 μΩ-cm [43]. Also, Cu can form clean interfaces which reduces contact resistance between metal layers [43]. Cu allows higher current density, increased scalability, and better electromigration reliability than Al interconnects [62-65]. Some disadvantages of Cu are its poor adhesion to dielectrics and the need for barrier and/or adhesion layers [62].

For our work, Cu has the advantage of being able to fill high aspect ratio holes by electroplating. Using our perforated seed discussed in Section 2.4.3, the Cu via had no seams or voids. Evaporation and conventional magnetron sputtering are unable to fill high aspect ratio vias because deposition on the top sidewalls plug the opening forming voids [66]. Other methods for depositing Cu such as collimated sputtering [67], electron cyclotron resonance (ECR) [68, 69] or vacuum arc plasma sources [70] have produced aspect ratios no better than 3. Better filling by chemical vapor deposition (CVD) [71] and cathodic arc plasma deposition [66] have achieved aspect ratios of 8. However, by electroplating, we have been able to achieve significantly higher aspect ratios of up to 49 for trenches and 14 for vias.

2.4.1 Cu Electrochemistry

Cu electroplating involves an oxidation reaction at the anode and a reduction reaction at the cathode (sample). The reaction at each electrode is:

$$Cu \rightarrow Cu^{2+} + 2\,e^{-} \qquad \text{(oxidation at anode)}$$
$$Cu^{2+} + 2\,e^{-} \rightarrow Cu \qquad \text{(reduction at cathode)}$$

The reduction reaction at the cathode actually takes two one-electron transfers to reduce the cupric ion (Cu^{2+}) to the cuprous ion (Cu^{+}), and then to atomic Cu [72].

There are various types of Cu electroplating solutions available that provide advantages for different applications. The two types of baths are alkaline plating baths, which include cyanide baths, and acid plating baths, which include Cu sulfate and Cu fluoborate baths. Cyanide baths give better deposition uniformity and throwing power (a measurement of the uniformity of the deposit over a range of current densities), but have greater health hazards and waste management problems [73]. Acid baths are more immune to ionic impurities and most importantly have

better micro throwing power, giving it the ability to fill and smooth fine scratches and holes [73]. However, plated substrates must be able to withstand high acidity. Cu sulfate baths are regularly used in plating printed circuit boards and semiconductor applications and have the advantage of producing strong, ductile Cu [73]. They also have cathode efficiencies approaching 100%, and are easy to maintain and control [73]. For these reasons, we chose to use Cu sulfate as the plating solution.

Chemicals in the Cu sulfate bath include copper sulfate, sulfuric acid, chloride, and organic additives such as levelers, brighteners, and carriers (wetting agents). Copper sulfate and the Cu anode provide the metal ions, sulfuric acid controls the conductivity of the solution, and chloride the quality of the deposit [73]. The organic compounds act to enhance uniformity and grain size of the deposition. Levelers are polymers that migrate to high-current density areas to shield from overplating [74]. This reduces surface irregularities and allows for more even plating [72, 74]. Brighteners and carriers influence the grain structure of the deposit by controlling the reduction reaction rate at the cathode [72, 74]. This gives a smoother Cu surface [74]. Carriers also improve the throwing power of the solution [72].

2.4.2 Electroplating System Specifications

We have designed and implemented a Cu electroplating station for the Microsystems Technology Laboratories at MIT. Fig. 2-24 is a drawing of the setup, and Fig. 2-25 is a picture of the actual system that was built in MTL. The Cu electroplating system contains three essential components: the Cu sulfate solution, Cu anodes, and current supply. We used a commercial Cu sulfate solution acquired from Enthone-OMI. This solution is commonly used for semiconductor applications and especially for high aspect ratio plating. The solution operating conditions are noted in Table 2-1. The solution contains less than 80% water, less than 20% sulfuric acid, and less than 10% copper sulfate. Organic additives in the solution were proprietary. The solution was agitated with a Teflon-coated stirrer. Agitation distributes ions more uniformly throughout the solution and promotes more uniform corrosion of the anode [73].

For Cu sulfate solutions, a phosphorized Cu anode (0.04 to 0.06% P) is required. Larger anode-to-cathode spacing gives better uniformity [75]. Our spacing was approximately 20 cm since

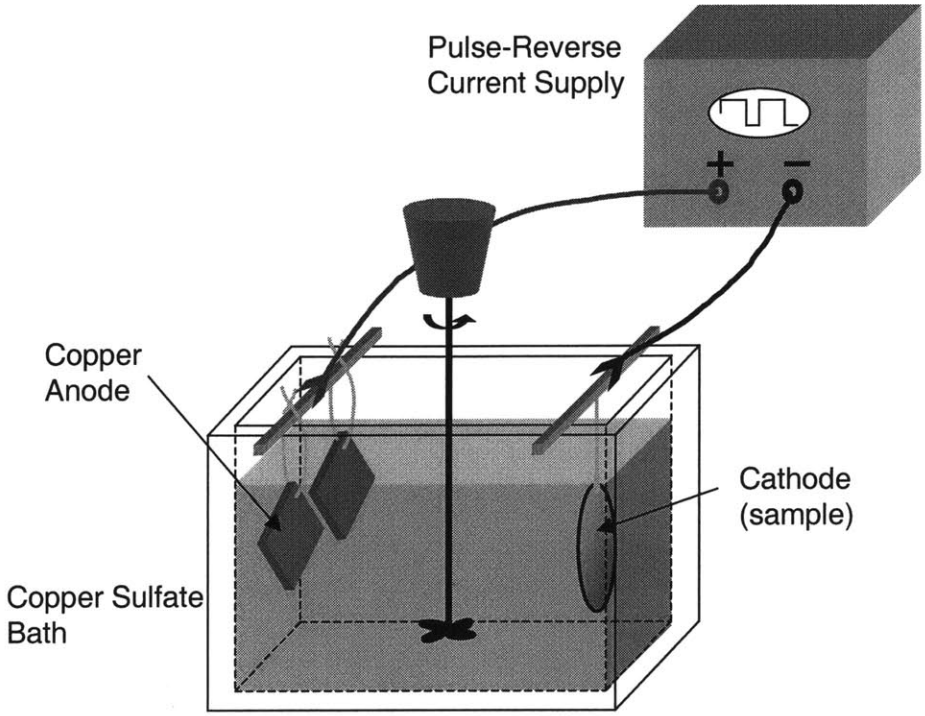

Figure 2-24. Illustration of the copper sulfate electroplating system at MTL. The bath contains a copper sulfate solution, which is agitated with the stirrer. The pulse-reverse current supply is connected to the copper anodes and the cathode, which is the sample to be plated.

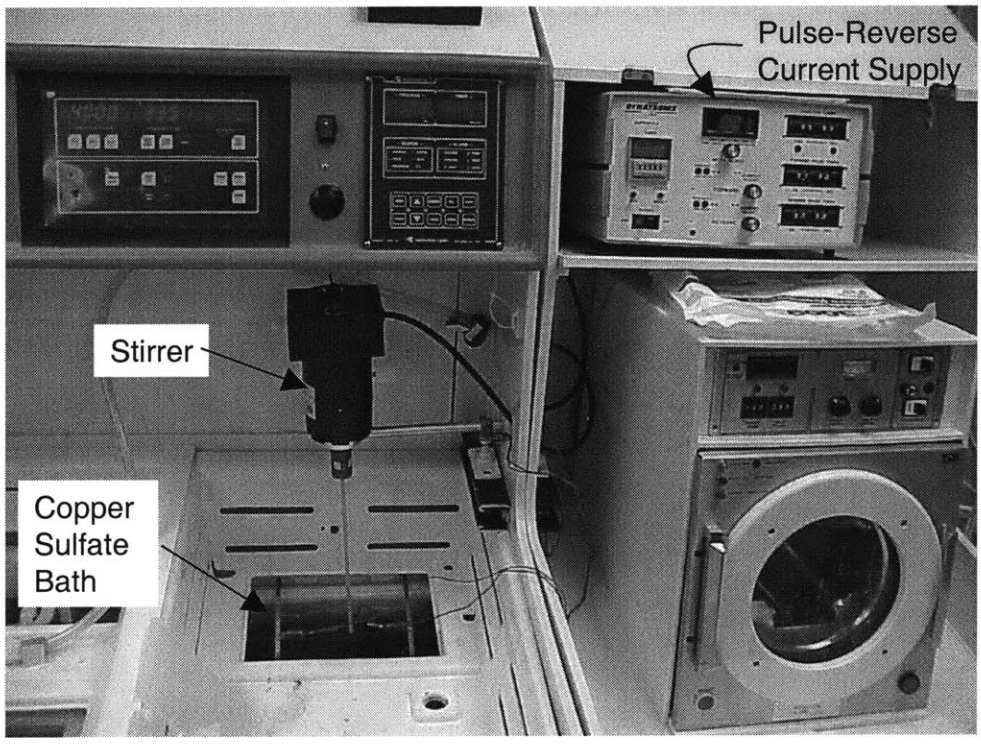

Figure 2-25. Photograph of the Cu electroplating system in MTL.

Table 2-1. Operating conditions for Cu electroplating solution [75]

Parameter	Nominal	Range
Cu concentration	17 g/L	15 – 19 g/L
Cu sulfate	67 g/L	59 – 75 g/L
Sulfuric acid	170 g/L	150 – 225 g/L
Chloride ions	70 mg/L	50 – 90 mg/L
Temperature	24°C	21 – 27°C
Anode to cathode ratio	2:1	1.5:1 – 2.0:1

this was the furthest distance possible for our tank. The anodes were placed in woven polypropylene anode bags in order to prevent Cu chips and particles from the anode from contaminating the bath [76].

For the power supply, a pulse-reverse current source has been known to fill high aspect ratio structures better than dc [77, 78]. This is due to the dissolution during the negative pulse because it provides greater concentration of cupric ions at the bottom of the trench. This concentration gradient at the beginning of the subsequent deposition step preferentially deposits Cu at the bottom of a trench [78]. The current supply used in the electroplating system was purchased from Dynatronix Inc. This source can supply up to 1 A average current for forward and reverse and a maximum of 3 A peak current. The timing specifications allowed up to 9.9 ms positive and negative pulses, and a forward or reverse period of up to 99 ms. The waveform used to electroplate was a pulse of positive current for 5 ms, and then a pulse of negative current for 1 ms [79]. The actual current for each sample varies according to the area in order to keep the current density constant. We chose to plate at an average current density of 10.8 mA/cm^2, which is relatively low to obtain better uniformity. The peak positive current density was 1.2 times the average current density, and the peak negative current density was 0.2 times the average current density. The current-density waveform and calculations are explained in Appendix C.

2.4.3 Seed for Electroplating

When electroplating a metal, a seed or plating base is required to distribute the current from the electrode contact point to the areas to be plated. For our seed, we used a stack of 250 Å of Ta, 250 Å of Ti, and 2000 Å of Cu that was e-beam evaporated. The Ta and Ti improve the adhesion of Cu to the silicon nitride.

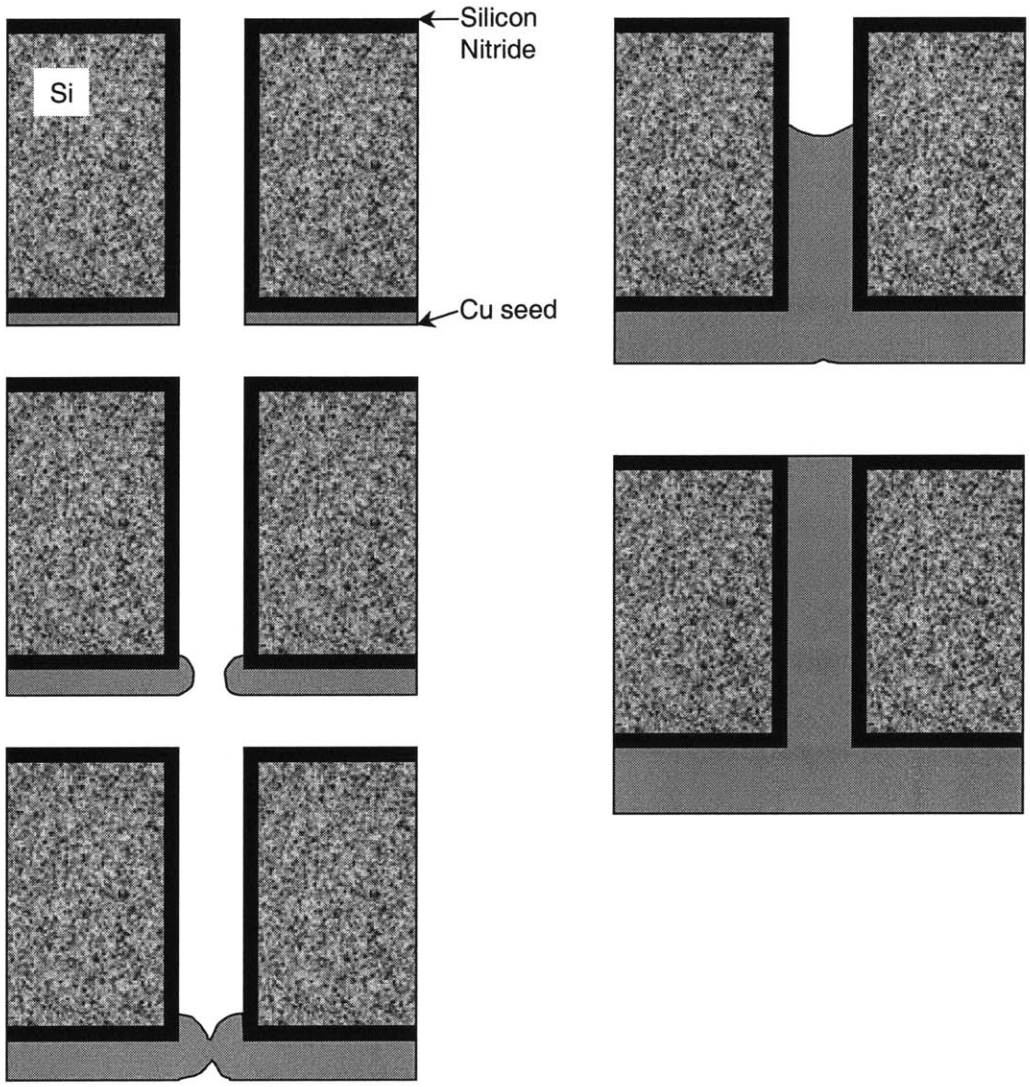

Figure 2-26. Evolution of the electro-deposition of Cu with perforated seed. Starting from the seed evaporated on the backside, the electroplated Cu deposits isotropically on the seed. The Cu deposit grows horizontally until the Cu on the two sides of the via meet, sealing the via opening at the bottom. Then the Cu deposits inside the via filling it and on the backside.

The seed in our process is perforated due to the via openings on the backside. During copper electroplating, Cu deposits onto the seed, increasing in thickness in all possible directions. At the opening of the bottom of the via, the growth of Cu increases until both sides of the Cu layer join to close the opening as depicted in Fig. 2-26. Once the via bottom is sealed, the inside of the via fills with Cu from bottom to top with no seams or voids.

2.4.4 Cu Electroplating Characterization and Results

Using the electroplating system and pulse-reverse current waveform described in Section 2.4.2, we characterized the bath using unpatterned wafers and substrate-via samples. Fig. 2-27 shows the deposition rate on unpatterned samples using pulse-reverse and dc plating. Both are above the published deposition rate for this Cu sulfate solution. However, these results were used only as a benchmark for deposition rates since the plating bath variables were not necessarily the same as that used to obtain the published data. We also experimented with the orientation of an unpatterned wafer with respect to the anode. In Fig. 2-28, the deposition rate shows no significant dependence on orientation. However, along the length of the wafer, the deposition rate increases with depth in the bath.

In substrate vias, we found that the rate of filling has a slight inverse dependence on aspect ratio or in actuality the opening width (Fig. 2-29). This is most likely due to the perforated seed since

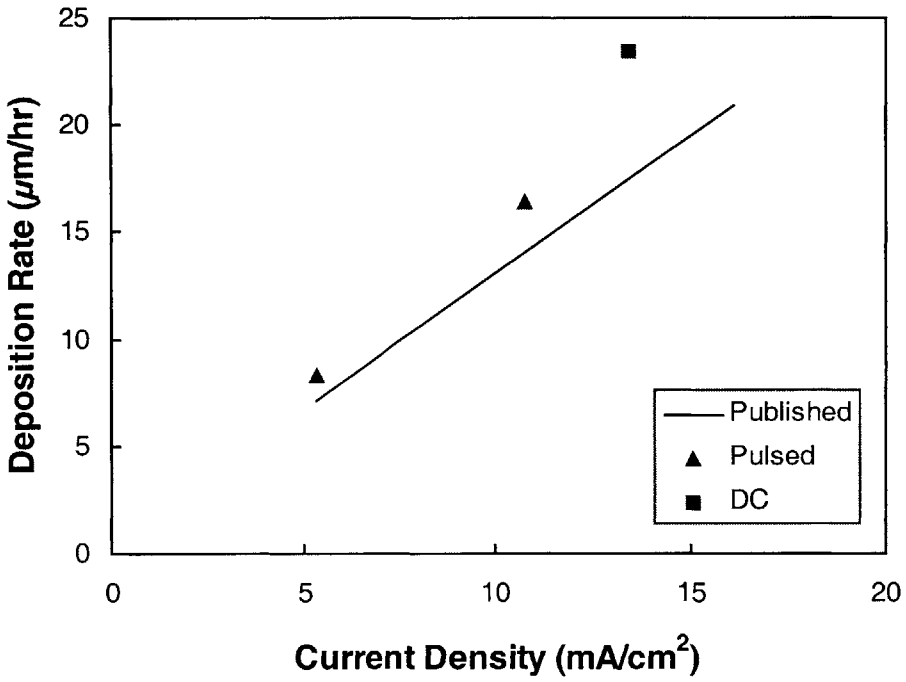

Figure 2-27. Deposition rate on unpatterned wafer vs. current density for pulsed and dc plating compared to the published deposition rate by Enthone-OMI for their Cu sulfate solution.

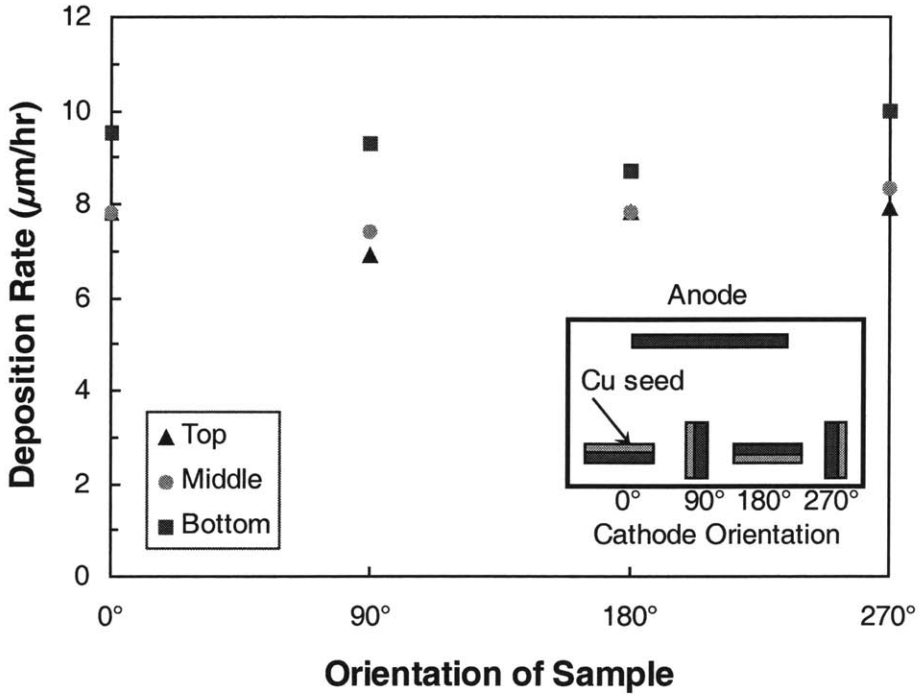

Figure 2-28. Deposition rate on unpatterned wafers vs. the orientation of the Cu seed on the wafer. The current density is 5.4 mA/cm^2. Deposition rate has no significant dependence on orientation, but the deposition rate increases with depth in the bath.

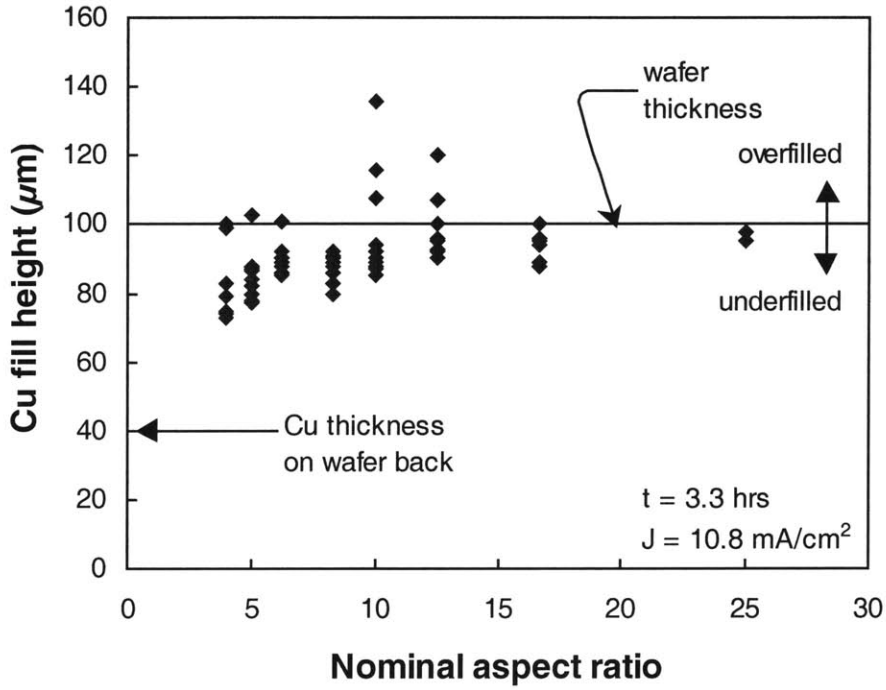

Figure 2-29. Height of the Cu filled inside the via vs. nominal aspect ratio on a 100-μm thick wafer after 3.3 hours of electroplating at a current density of 10.8 mA/cm^2. Most vias on this wafer were underfilled, while a few were overfilled. The Cu thickness on the backside of the wafer was 40 μm, significantly less than inside the vias.

the bottom of the via must close first before it can be filled. For larger openings, plugging the bottom would take longer, increasing the fill time. Another observation from Fig. 2-29 is that on the same sample the vias range from being underfilled to overfilled. This non-uniformity in deposition has caused problems with subsequent processing steps and in measurements. The highest aspect ratio trench filled with Cu was 49 (Fig. 2-9), and 14 for vias.

2.5 Process Integration

The integration of these process steps was not a trivial endeavor. Several unforeseen issues emerged when integrating these steps for the first time. The KOH holes etched in the backside posed several problems. They hindered subsequent processing steps since wafers could no longer hold vacuum on the photoresist coater chuck. Also, there were problems due to the KOH holes in the DRIE because of the wafer cooling mechanism of the tool. For the final metallization steps, we had to change the process to its current arrangement because of metal etch/deposition incompatibilities.

In order the solve the vacuum chuck problem, we placed the KOH-etched wafer on a specially-designed jig that holds the wafer to a round Al plate using three pegs. The coater vacuum chuck holds vacuum to the Al plate. Because the DRIE uses He to cool the backside of the wafer during the etch, through-wafer etches are not possible since He would then flow into the plasma chamber. The common remedy is to mount the wafer to a quartz handle wafer using photoresist. The problem with the handle wafer mount is that the photoresist seals the KOH cavities etched in the backside, and then during the pump down in the DRIE load lock, the cavities explode destroying the wafer. To combat this, we used a target mount of photoresist depicted in Appendix B, Fig. B-1. This target mount prevented photoresist from entering areas of the wafer with KOH cavities so they would not seal and still provided enough heat dissipation for the DRIE.

Because of the corrosive nature of the Cu sulfate bath, the process required Cu electroplating to be performed first before the frontside metal could be deposited and patterned. Cu structures that were not electrically connected to the current supply or protected were etched away in the plating solution. Al regularly etches in sulfuric acid. We were limited to Al in our choice for the test

structure metal because of the etch chemistries required us to etch the frontside metal but leave the backside electroplated Cu undamaged. The basic solution of developer was able to selectively etch Al while not disturbing the Cu on the backside of the wafer. There was approximately 4 μm of undercutting for the etch.

2.6 Imaging of Cross-sections

Cross-sections of the substrate-vias give true representations of the dimensions of the via and the appearance of the nitride and Cu and were essential to this research. However, due to the ductility of copper, obtaining cross-sections of the substrate-vias by simple cleaving was unfeasible. Cleaving in liquid nitrogen was also unsuccessful because of the difference in coefficient of thermal expansion between Si and Cu. As seen in Fig. 2-30, the Cu in the trenches cracks resembling bamboo. We attempted to die saw the wafers, but this smeared the Cu so that

Figure 2-30. SEM cross-section of a Si wafer with trenches filled with Cu after cleaving in liquid nitrogen. The Cu has cracked in the trenches because of the thermal expansion mismatch.

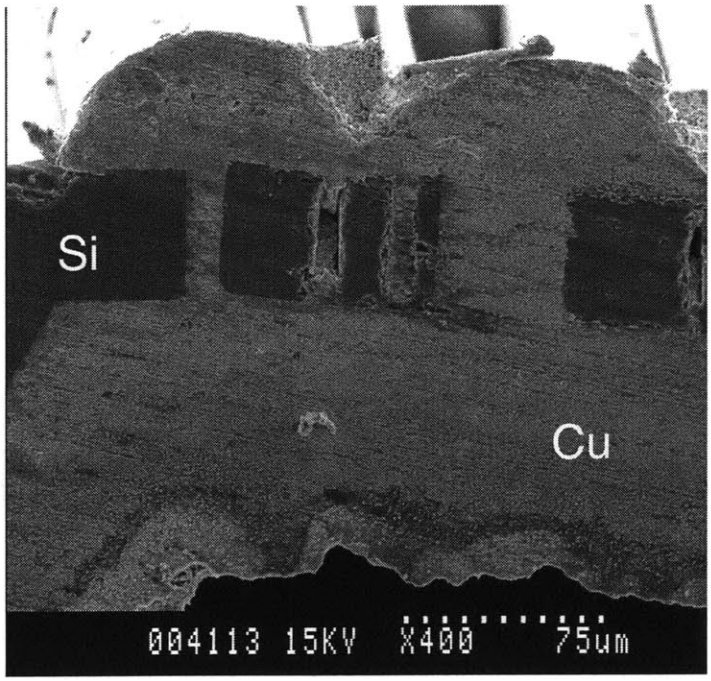

Figure 2-31. SEM cross-section of through-wafer trenches filled with Cu after die saw. The Cu has smeared to obscure the true dimensions of the trench and Cu filling.

the actual dimensions of the Cu filling were obscured (Fig. 2-31). By combining die saw with subsequent polishing, we were able to achieve clean, accurate cross-sections (Fig. 2-32). In order to polish a cross-section, samples were sandwiched between pieces of Si with epoxy for adhesion as depicted in Fig. 2-33. Then the samples were polished on silicon carbide pads of decreasing grit size (300-4000) followed by an alumina polish and ultrasound clean. All cross-section pictures in this thesis were obtained using this method.

Delineation of the materials was necessary to distinguish between the Si, nitride, and Cu interfaces and to measure the thickness of the nitride. A 1-minute dip in BOE (7:1) accomplished this by etching a few hundred Å of nitride, while leaving the Si and Cu intact.

2.7 Summary

This chapter has detailed the fabrication process to produce isolated substrate vias. Once the test vehicle was determined, we developed and characterized the three major process steps, DRIE,

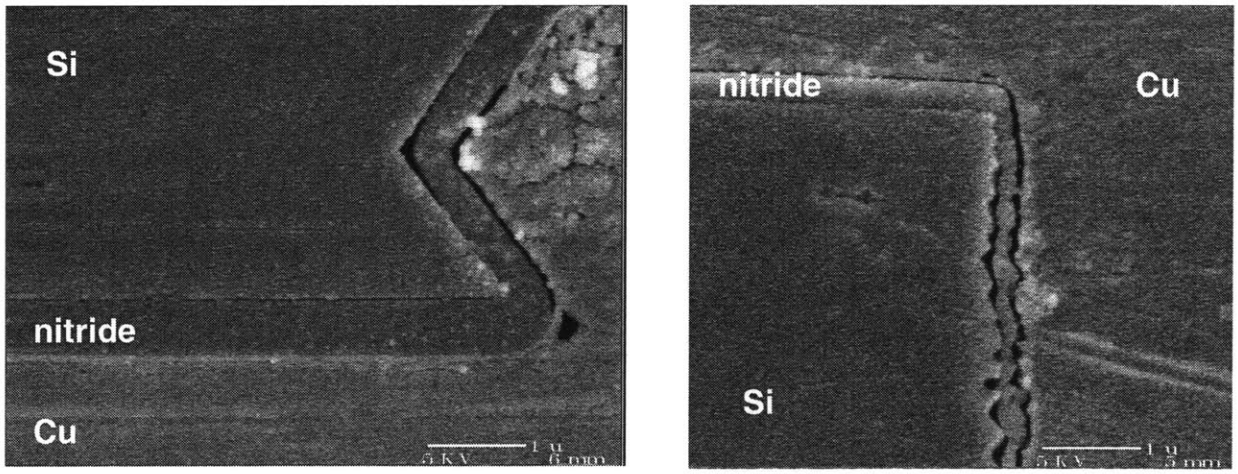

Figure 2-32. Left: SEM cross-section of the opening to a KOH hole on the backside of a wafer. Right: cross-section of the top of a trench 11-μm wide by 98-μm deep lined with nitride and filled with Cu. The nitride is 240 nm at the surface. The Si, nitride, and Cu are clearly defined by the cross-sectioning procedure.

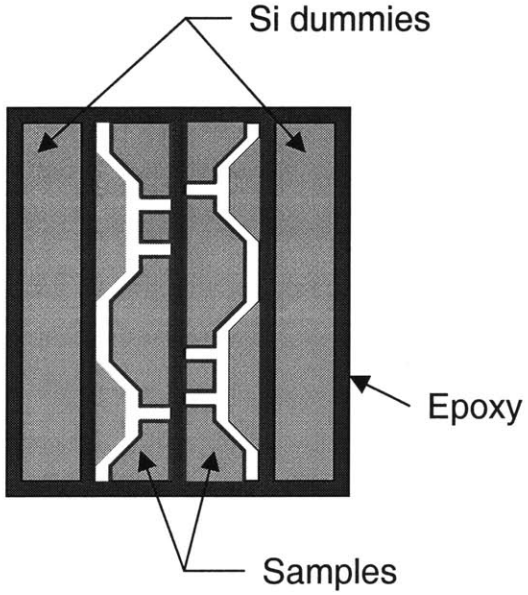

Figure 2-33. Samples are sandwiched between dummy Si pieces and set with epoxy. Then the cross-section is polished on silicon carbide pads and alumina.

silicon nitride conformal deposition, and Cu electroplating, and many minor steps. We have etched and electroplated Cu in trenches with aspect ratios of 49 and vias with aspect ratio of 14. The conformality of the nitride is limited to 15. We have confirmed nitride conformality in trenches of aspect ratio 13 and vias of aspect ratio 7. The next chapters will discuss the impedance measurements and an application for SOC isolation using these substrate vias.

Chapter 3

Test Structure Design and Measurement of Impedance

Once the substrate-via process was fully developed, we needed to evaluate the electrical performance of these vias. We designed and fabricated microwave test structures that allowed the measurement of a single via. These impedance measurements revealed a simple via model, so we could easily extract the inductance and impedance. These results were compared to theory and models discussed in literature.

3.1 Test Structure Design

We designed the microwave test structures with much guidance from Keith Jenkins at IBM T. J. Watson Research Center in Yorktown Heights, NY. These are one-port test structures with a 50-Ω coplanar ground-signal-ground configuration. Fig. 3-1 shows the layout of the test structure with dimensions and a 3-D illustration of its cross-section. Fig. 3-2 depicts the top view of the test structure fabricated on a wafer. The test structure pads on the surface of the wafer are Al, and silicon nitride insulates the Al test structures from the substrate. The via under test is on the signal line. The ground lines are shorted to the Cu ground plane on the back of the substrate through a large number of vias (30). Measured vias ranged from 3 to 25 μm in nominal opening width. However, the actual width is larger due to the DRIE. The test-structure dimensions as shown in Fig. 3-1 are 200 μm wide and 342 μm high. These short dimensions allow us to ignore transmission line effects.

3.2 Measurement Setup

The substrate vias were measured using the measurement setup depicted in Fig. 3-3. The one-port test structures were probed on a Cascade Microtech Summit 9600 thermal probe station

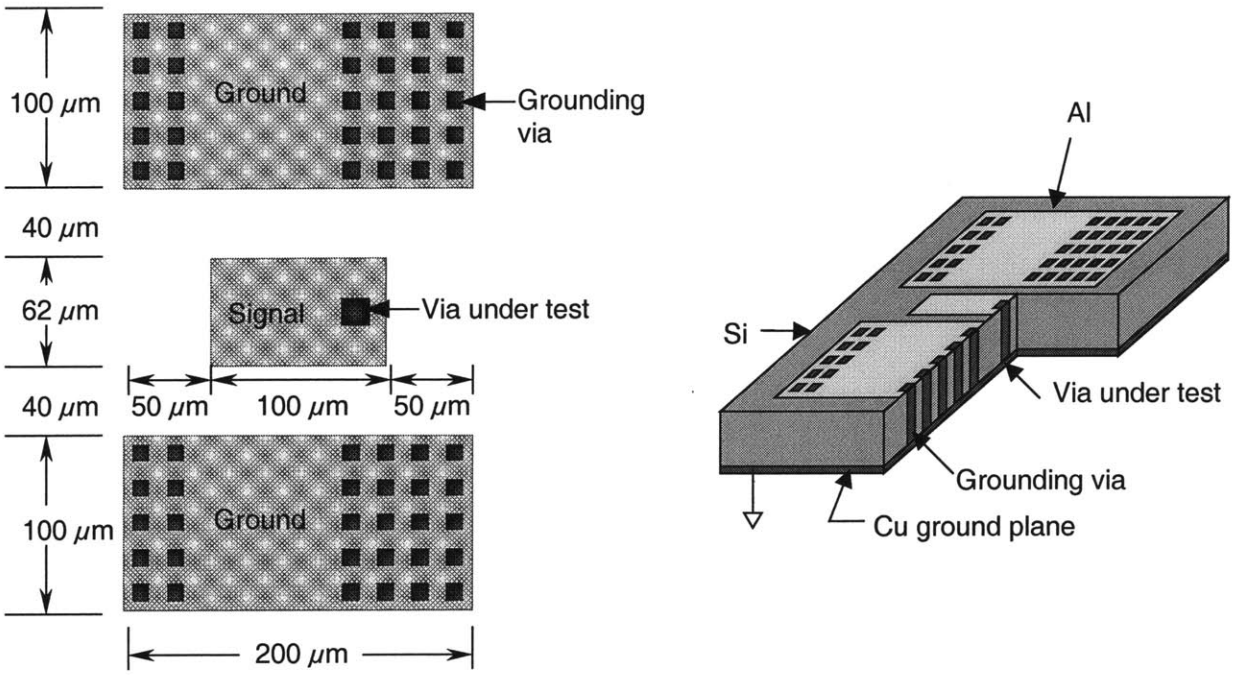

Figure 3-1. Left: layout drawing with dimensions of the one-port test structure used to measure the impedance of a single via. Right: 3-D schematic of the test structure. The multiple grounding vias are introduced to reduce the impedance of the ground pads.

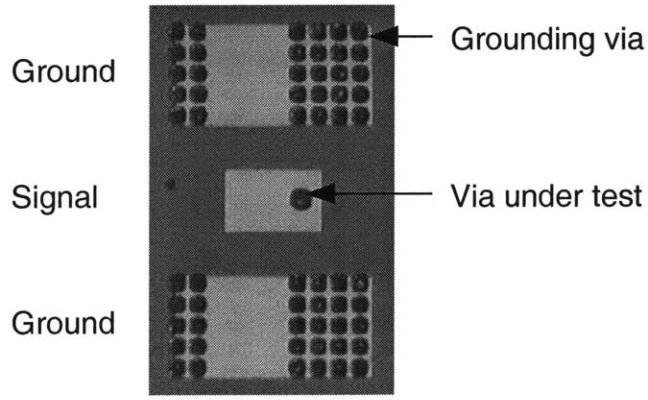

Figure 3-2. Picture of a one-port test structure fabricated on a wafer.

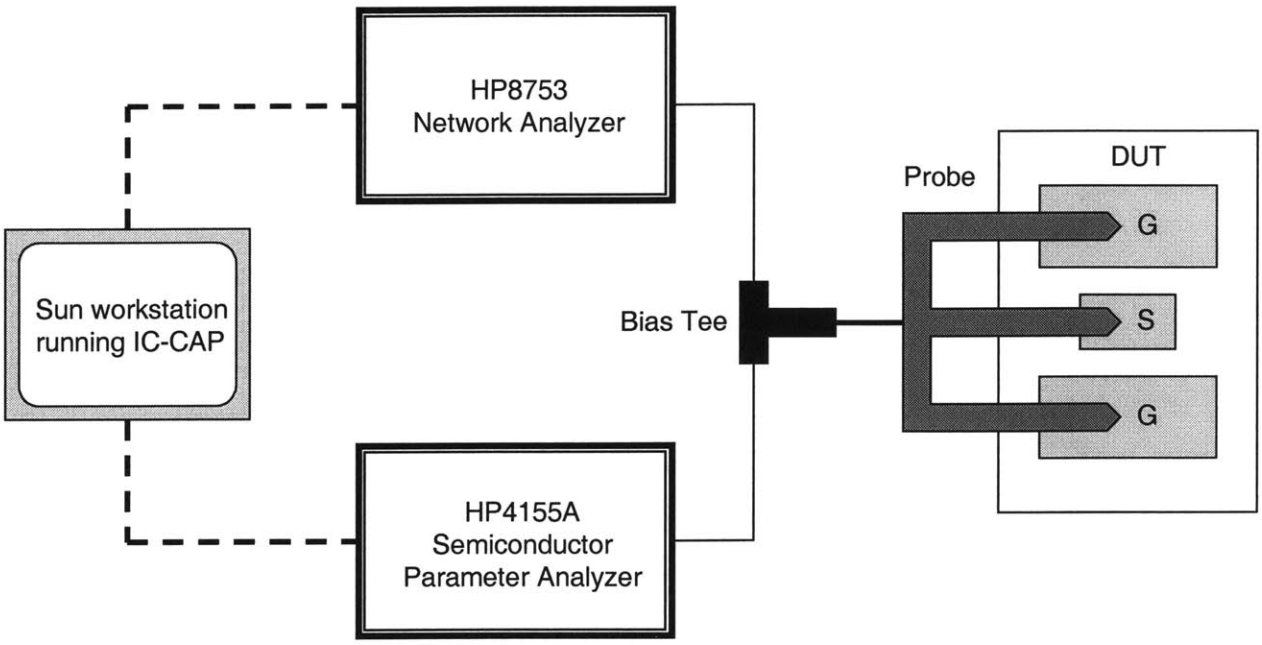

Figure 3-3. Illustration of the measurement setup for dc biasing and S-parameter measurement of a substrate via.

using a 150-μm pitch, GGB Industries Inc. microwave probe. The probe was connected to an HP4155A Semiconductor Parametric Analyzer for dc biasing and a HP8753 network analyzer for *S*-parameter measurement. Both analyzers were controlled by IC-CAP software running on a Sun Ultra 5 workstation. The prober stage on which the samples were placed was grounded to the HP8753. The HP8753 was calibrated using a calibration standard substrate from GGB Industries, Inc.

The S_{11} scattering parameter was measured at a bias point of zero from 10 MHz to 6 GHz. S_{11} is defined as the reflection coefficient seen at port 1 (Fig. 3-4):

$$S_{11} = \frac{P_1^-}{P_1^+} \qquad \textit{Equation 3-1}$$

where P_1^- is the output power from port 1 and P_1^+ is the input power to port 1. Once the S_{11} data was acquired from the HP8753, IC-CAP converted them to impedance, Z_{11}, using the following formula [80]:

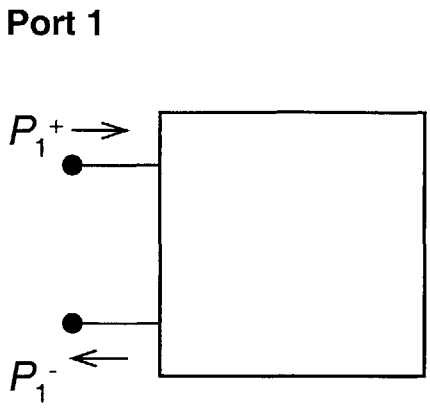

Figure 3-4. Pictorial representation of S_{11}, the reflection coefficient at Port 1.

$$Z_{11} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \qquad \textit{Equation 3-2}$$

The Z_{11} data was plotted against frequency, and its analysis is discussed in the next section.

3.3 Results and Discussion

From the Z_{11} impedance data collected, we have been able to obtain a simple circuit model for a substrate via. From this via model, we easily extracted the inductance and resistance of the via. We then compare these results to theoretical models of inductance and resistance.

3.3.1 Via Model

The Z_{11} impedance data of one via is plotted against frequency in Fig. 3-5 in its real and imaginary parts. For all vias, we found that the real part of Z_{11} is largely independent of frequency, while the imaginary part is positive and increases linearly with frequency. These results suggest a simple via model that consists of a resistor and an inductor in series. This impedance is defined as:

$$Z = R + j\omega L \qquad [\Omega] \qquad \textit{Equation 3-3}$$

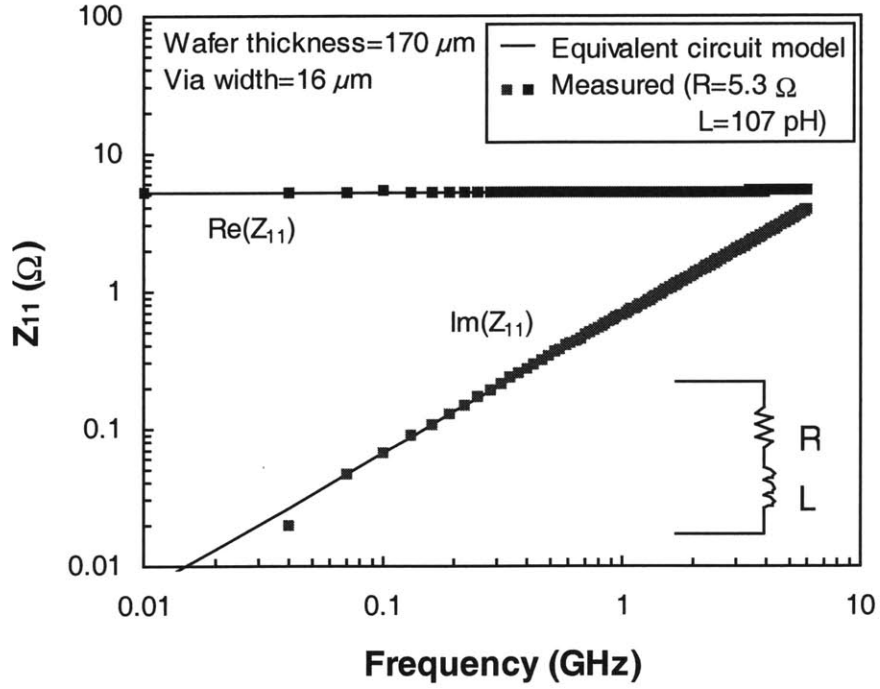

Figure 3-5. Z_{11} vs. frequency of a one-port test structure with a via 16-μm wide and 170-μm deep. The real part of Z_{11} is independent of frequency, while the imaginary part has a linear dependence. This is the ideal behavior of a simple resistor and inductor in series.

where the real part, R, is the resistance, and the imaginary part, ωL, is the frequency times the inductance. From this, the inductance can be easily extracted.

For vias with low resistance, typically less than 1 Ω, the skin effect causes a noticeable dependence of via resistance and, to a lesser extent, inductance on frequency (Fig. 3-6). The skin depth is defined as:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad [\text{m}] \qquad \textit{Equation 3-4}$$

where f is the frequency of operation, μ is the permeability, and σ is the conductivity. For Cu,

$$\sigma = 5.80 \times 10^{7} \quad [\text{S/m}]$$
$$\mu = 4\pi \times 10^{-7} \quad [\text{H/m}]$$

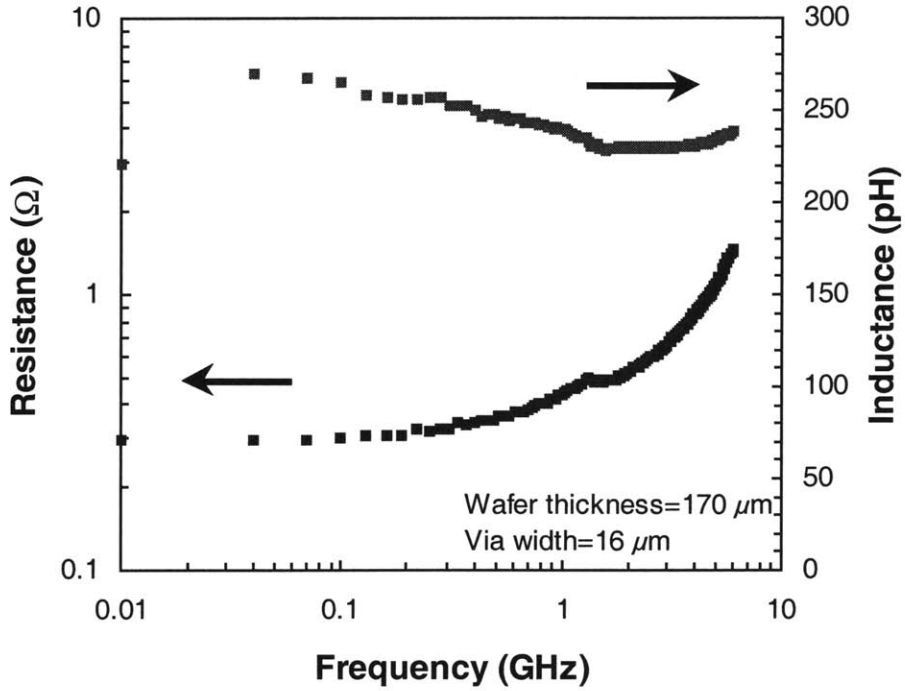

Figure 3-6. Resistance and inductance vs. frequency for a via 16-μm wide and 170-μm deep. For vias with resistance less than 1 Ω, the skin effect is noticeable, producing a dependence of resistance and inductance on frequency.

The skin depth for Cu at 1 GHz is 2.1 μm and 0.85 μm at 6 GHz. At these frequencies, the current is pushed to the skin depth of the via perimeter, which increases the resistance and lowers the inductance. Since our vias have a diameter on order of 25 μm and less, the skin effect can be noticeable at frequencies as low as 100 MHz.

3.3.2 Inductance Results

All measurements are plotted in Figs. 3-7 and 3-8. The measured data includes the series resistance and inductance of the test structure pads, so the actual impedance of a via is lower than that measured. A true de-embedding structure for these test structures is difficult to design. Fig. 3-7 shows the extracted inductance of several vias on a 170-μm thick substrate as a function of the via aspect ratio. The scatter in the data is believed to result from slight underfilling or overfilling of some vias and the difficulty of the top pads in contacting them. Also, the measured

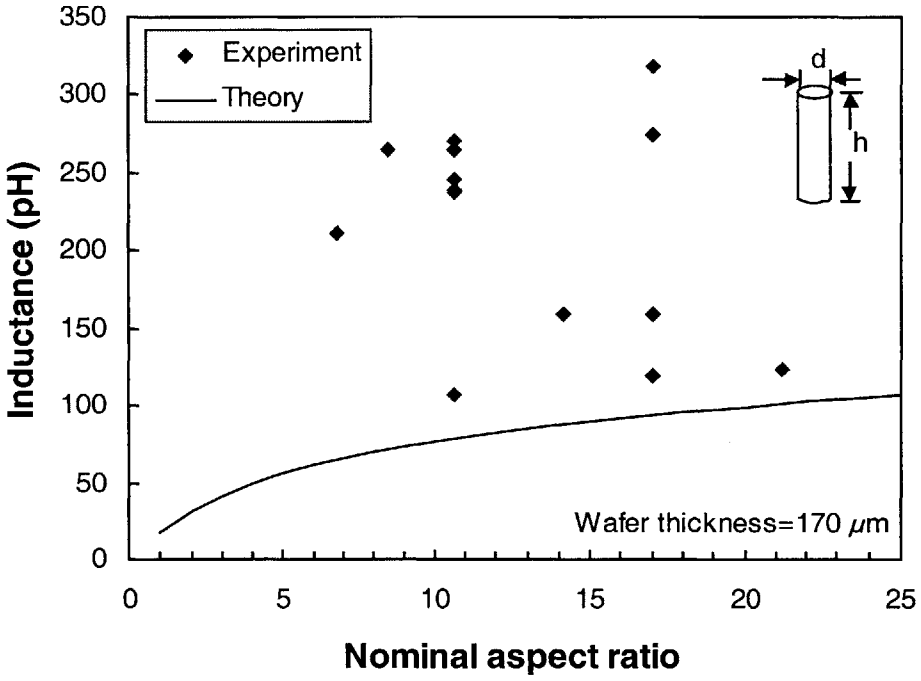

Figure 3-7. Extracted inductance vs. nominal aspect ratio of vias on a substrate thickness of 170 μm. Also plotted in a solid line is the theoretical inductance model from Goldfarb and Pucel [82].

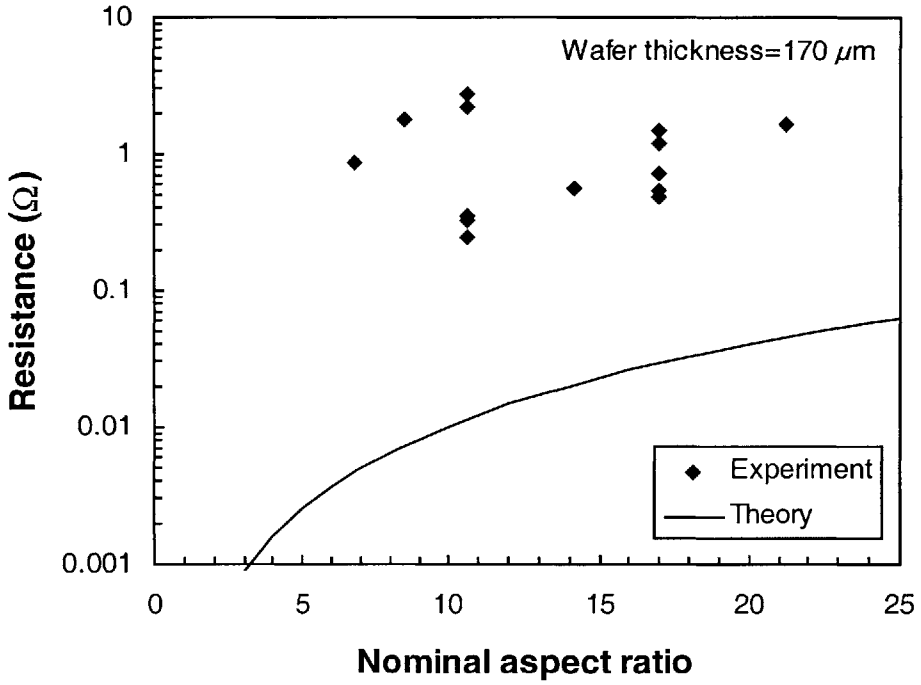

Figure 3-8. Resistance vs. nominal aspect ratio of vias on a substrate thickness of 170 μm.

inductance has a significant dependence on the placement of the probes on the test structure. Placing the probes closer to the via under test decreases the inductance by as much as 10%. This may be due to the decrease in the inductance loop area when moving the probes closer to the via.

3.3.3 Inductance Model

The theoretical self-inductance of a cylindrical wire in free space is derived as:

$$L = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h+\sqrt{h^2+r^2}}{r} \right) + r - \sqrt{h^2+r^2} \right] \quad \text{[H]} \qquad \textit{Equation 3-5}$$

where $\mu_0 = 4\pi \times 10^{-7}$ [H/m], h is the height, and r is the radius of the cross-section. This formula is based on equations from [81, 82]. Goldfarb and Pucel [83] modified this equation in order to match the inductance of a via in a microstrip to their measurements and numerical simulation data. The empirical equation that they proposed is:

$$L_{via} = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h+\sqrt{h^2+r^2}}{r} \right) + \frac{3}{2}\left(r - \sqrt{h^2+r^2} \right) \right] \quad \text{[H]} \qquad \textit{Equation 3-6}$$

This equation can be rearranged in terms of aspect ratio, $A = h/2r$:

$$\frac{L_{via}}{h} = \frac{\mu_0}{2\pi}\left[\ln\left(2A + \sqrt{1+(2A)^2} \right) + \frac{3}{2}\left(\frac{1-\sqrt{1+(2A)^2}}{2A} \right) \right] \quad \text{[H/mm]} \qquad \textit{Equation 3-7}$$

where h is in mm. The inductance per unit length of a via depends only on the aspect ratio. For a via height of 100 μm and diameter of 10 μm, the theoretical inductance is 45 pH. For a via height of 170 μm and diameter of 10 μm, the theoretical inductance is 94 pH.

Along with the measured data Fig. 3-7 also includes a theoretical calculation of an inductance model by Goldfarb and Pucel [83] for a substrate via. The lower lying experimental data points agree well with this theoretical model. This gives us confidence that without overfilling/underfilling, this technology can produce vias with theoretically minimum inductance.

3.3.4 Resistance Results and Model

The theoretical resistance of a Cu wire is:

$$R = \frac{l}{\sigma S} \qquad [\Omega] \qquad \textit{Equation 3-8}$$

where l is the length, σ is the conductivity, and S is the cross-sectional area of the wire. For a wire 100-μm long with a square cross-section of width 10 μm, the resistance is 0.017 Ω; for 170-μm length, the resistance is 0.029 Ω. The measured resistance of the substrate vias includes the Al test structure pads, so that the via resistance is actually smaller than measured. From Fig. 3-8, the resistances are drastically higher than theory, and are rather random in value. There are possibly many contributors to this discrepancy such as contact resistance from processing defects due to under/overfilling of vias.

Chapter 4

Faraday Cages for SOC Isolation

Of the numerous possible applications for silicon substrate vias, we chose to explore its effectiveness at subsystem isolation for mixed-signal circuits for SOC applications. The high aspect ratio of our substrate vias allows them to be packed in high density. We have exploited this to demonstrate a novel Faraday cage isolation scheme to suppress crosstalk in ICs.

4.1 Introduction

Designers of mixed-signal circuits have raised much concern about the problem of crosstalk between sensitive analog circuits and noisy digital components to motivate substantial work in this area [7-9, 84-90]. Crosstalk can be diminished by either reducing the signal at its source or preventing the signal from interfering with other circuits. The former is impractical for designers; hence, various implementations to reduce noise coupling have been examined. Crosstalk can occur through metal lines and pads, bond wires, and the substrate [85]. However, most work has concentrated on substrate coupling as a contributor to crosstalk.

Previous technology to reduce the crosstalk in the substrate include guard rings, bonded-SOI substrates [84, 85], high-resistivity SIMOX (Separation by IMplanted OXygen) substrates [86, 90], and junction-isolated wells [84, 88, 91]. Guard rings are not deep enough to effectively reduce crosstalk [84]. Because of the insulating BOX, bonded- and SIMOX-SOI have better immunity to crosstalk than bulk Si wafers. Up to 10 dB of improvement over bulk has been reported [85, 90], but their effectiveness diminishes at high frequency. However, both Joardar [88] and Merrill *et al.* [84] report that junction isolated wells perform better (6 to 11 dB) than SOI for suppressing crosstalk.

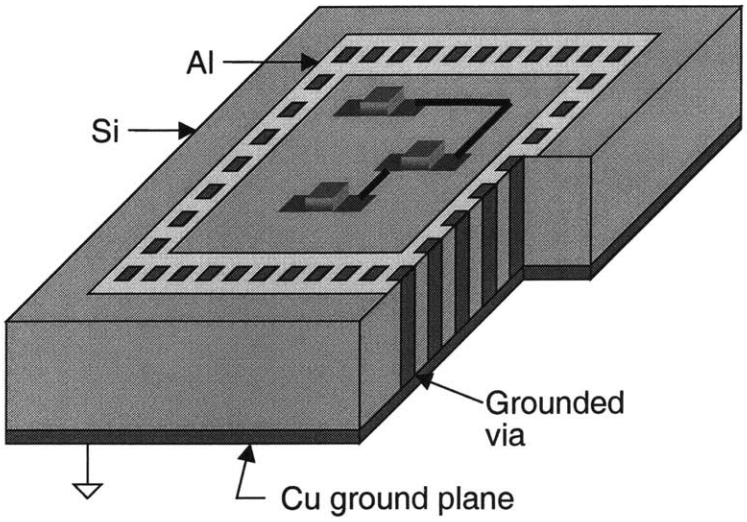

Figure 4-1. Illustration of a Faraday cage surrounding a noisy or sensitive circuit as a novel isolation scheme.

These previous technologies use buried oxide or doped silicon to isolate devices. We propose a new method of isolation by using our substrate vias to form a cage of grounded Cu vias with a Cu backplane that surrounds a noisy or sensitive circuit. This concept is illustrated in Fig. 4-1.

4.2 Test Structure Design

A Faraday cage consists of a simple ring of grounded vias that circle a noisy or sensitive subsystem in a chip. To test this isolation concept, we designed test structures in which a Faraday cage was created around a transmitter pad in a coplanar 50-Ω ground-signal-ground configuration. Isolation was measured at a receiver pad placed at varying distances of 100, 200, 400, and 800 μm. An identical reference structure was fabricated without the Faraday cage. Fig. 4-2 is a photograph of a fabricated test structure and a reference with a transmitter-receiver separation or transmission distance of 100 μm. Fig. 4-2 also includes additional test structures, one with a double Faraday cage of staggered vias and another with a metal strip and no Faraday cage. The vias of the Faraday cage are nominally 10-μm wide and are separated by varying distances. The variable via spacing of the Faraday was evaluated on test structures of a transmission distance of 200 μm. The nominal via spacings tested were 10, 15, 20, 30, 40, and 70 μm.

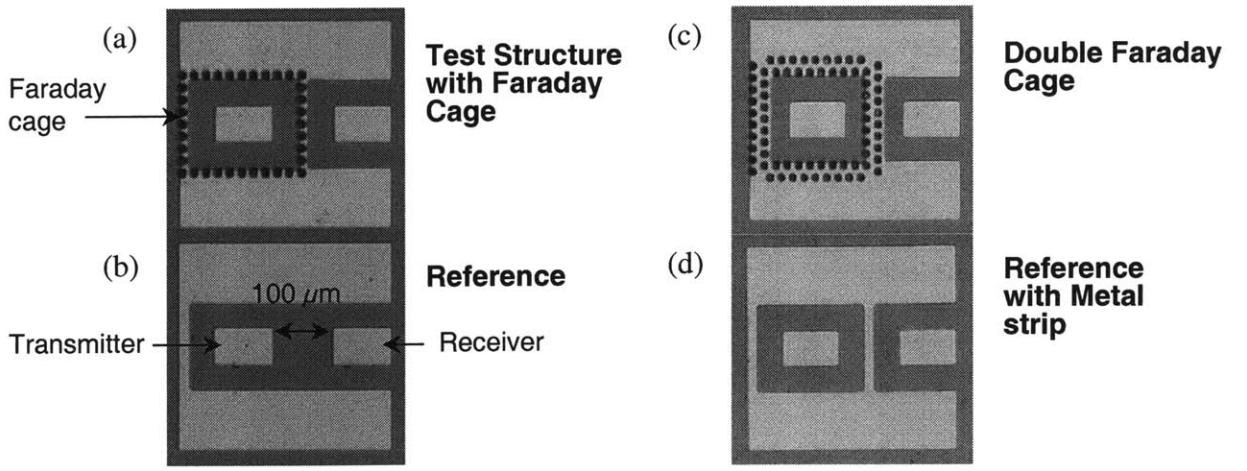

Figure 4-2. (a) Top view of the Faraday cage test structure, (b) a reference with no Faraday cage, (c) a double Faraday cage, and (d) a reference with a metal strip and no Faraday cage at a transmitter-receiver separation or transmission distance of 100 μm. Each via of the cage is 10-μm wide and separated by 10 μm.

4.3 Measurement Setup

The measurement setup used to characterize the isolation effectiveness of the Faraday cages is of a two-port nature. Calibration uses the same standard substrate from GGB Industries Inc. as the impedance measurements. As the isolation figure of merit, the magnitude of S_{21} was measured up to 6 GHz. S_{21} is a two-port measurement defined as the transmission coefficient from port 1 to port 2 when port 2 is terminated by a matched load of 50 Ω (Fig. 4-3):

$$S_{21} = \left.\frac{P_2^-}{P_1^+}\right|_{P_2^+=0} \qquad \textit{Equation 5-1}$$

where P_2^- is the output power from port 2, P_1^+ is the input power to port 1, and P_2^+ is the input power to port 2. S_{21} gives a quantitative measure of the degree of crosstalk between structures. The lower S_{21} is, the better the isolation.

4.4 Results and Discussion

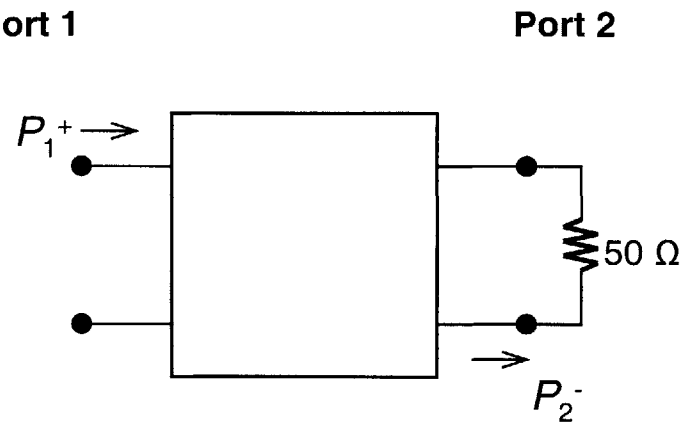

Figure 4-3. Pictorial representation of S_{21}, the transmission coefficient.

Compared to the reference structure, at a transmission distance of 100 μm, the Faraday cage with via separation of 10 μm improves isolation by 21 dB at 1 GHz and 15 dB at 6 GHz (Fig. 4-4). Over the entire frequency range, the signal measured with the probes in the air is similar to the caged-structure signal, indicating that the Faraday cage suppresses crosstalk down to the noise floor of our experimental technique. The crosstalk suppression improves as the distance away from the transmission pad increases (Fig. 4-5). Also, inserting a double cage of staggered vias appears to have the same effect as a single cage. In the range of via spacings that we have examined (10-70 μm), the via density of the cage does not affect the isolation effectiveness substantially (Fig. 4-6). These two results are consistent with an isolation effectiveness for the Faraday cage that exceeds the resolution of our experiments.

A test structure that had a grounded metal strip between the transmitter and receiver and no Faraday cage had crosstalk suppression nearly identical to the reference structure at a transmission distance of 100 μm (Fig. 4-7). This result was true for all the transmission distances tested in this work. This shows that inserting a metal line between pads has a negligible effect on isolation effectiveness.

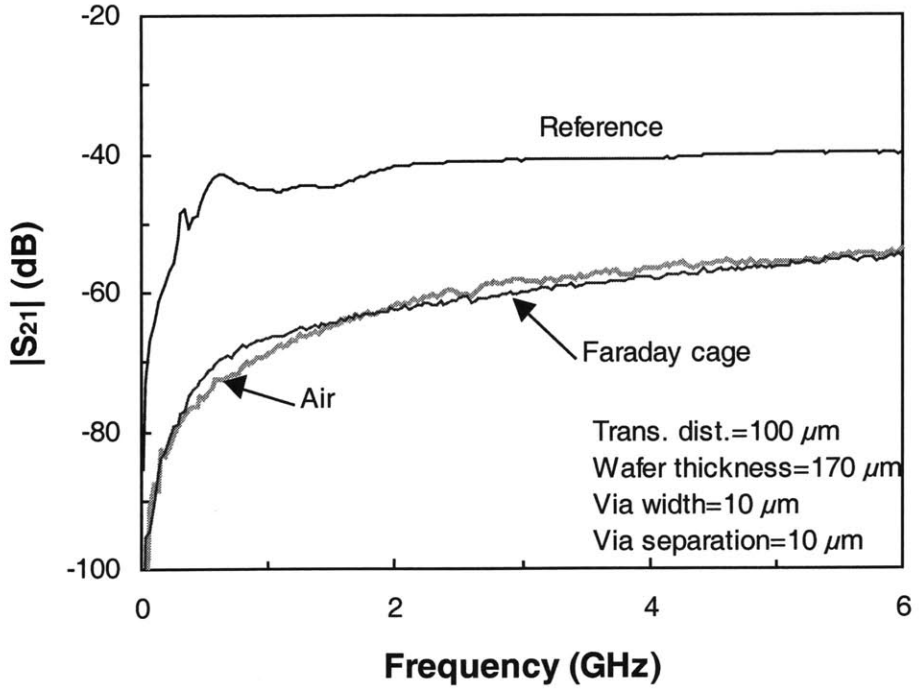

Figure 4-4. Magnitude of S_{21} vs. frequency for a reference and caged structure at a transmission distance of 100 μm. The Faraday cage gives at least 15 dB of isolation improvement at 6 GHz and over 20 dB of improvement at 1 GHz. Measurement of the signal taken with the probes in the air is similar to the caged-structure signal, indicating that the Faraday cage suppresses substrate crosstalk down to the resolution limit of our experimental technique.

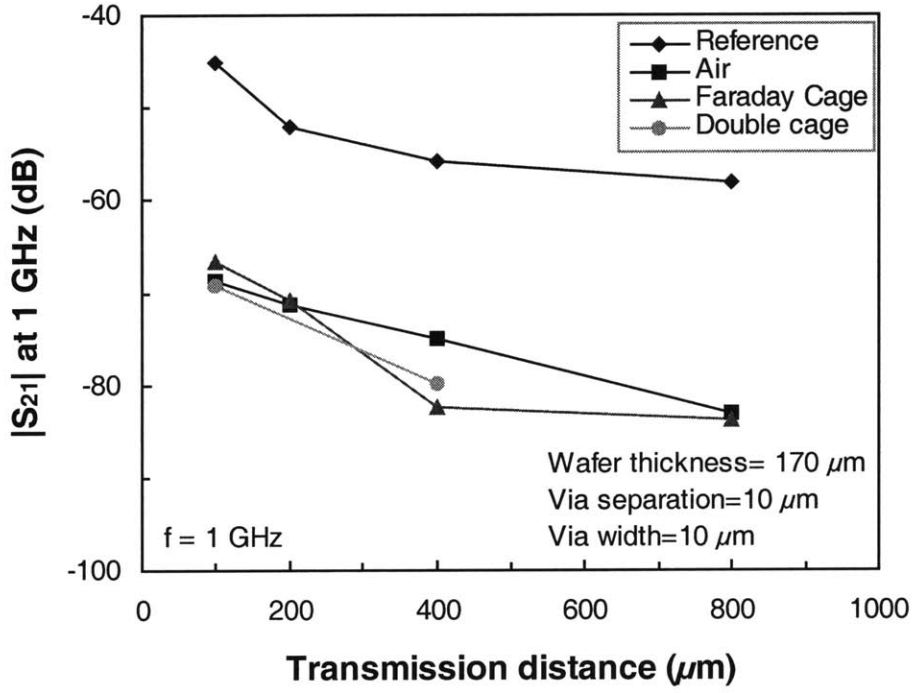

Figure 4-5. Magnitude of S_{21} at 1 GHz vs. the transmission distance for a reference and caged structure. The effectiveness of the Faraday cage appears to increase with increasing transmission distance. A single or double cage seems to have the same effect. Measurements with the probes in the air suggest that the Faraday cage effectiveness is higher than can be resolved.

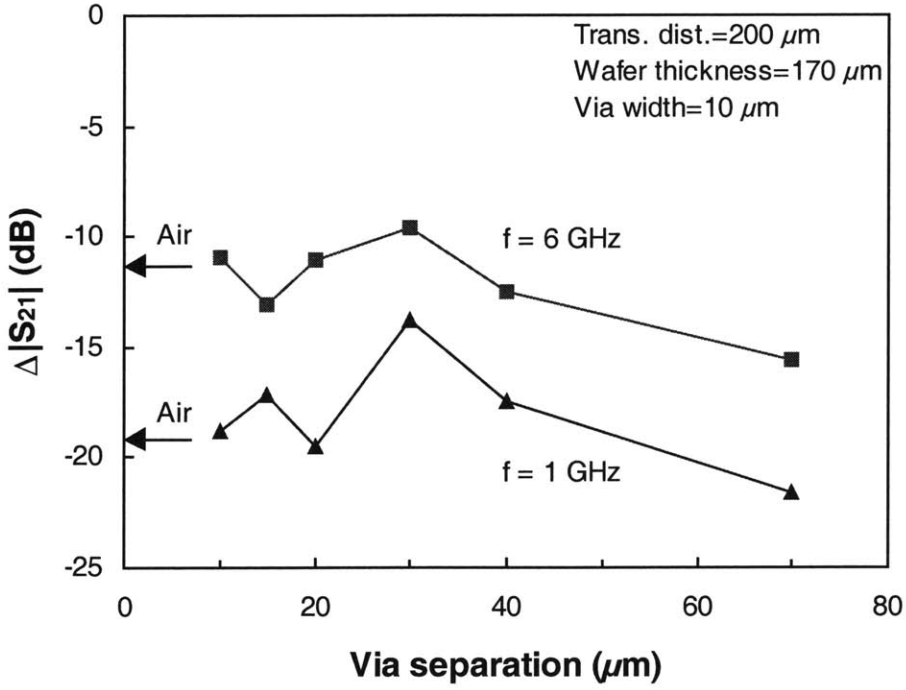

Figure 4-6. Difference in the magnitude of S_{21} between the reference and caged structure vs. the separation between vias of the Faraday cage at 1 and 6 GHz. There is no apparent difference on via separation for isolation effectiveness. This suggests that crosstalk suppression exceeds the air noise floor.

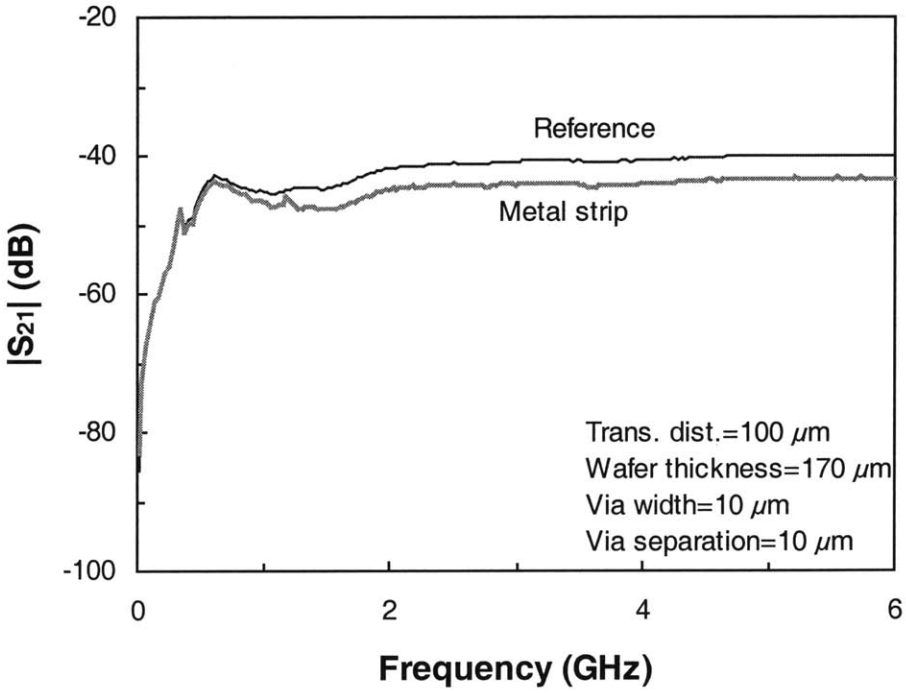

Figure 4-7. Magnitude of S_{21} vs. frequency for a reference and metal-strip test structure with no Faraday cage at a transmission distance of 100 μm. Both structures have nearly identical crosstalk suppression.

Chapter 5

Conclusions

5.1 Summary of Conclusions

We have successfully developed a high-aspect ratio, insulated substrate-via technology for low-inductance power and ground distribution in ICs. We have integrated an anisotropic reactive ion etch with a conformal silicon nitride deposition and Cu electro-deposition. We have been able to etch and electroplated Cu in trenches with aspect ratios of 49 and vias with aspect ratio of 14. From experiment, the conformality of the nitride is limited to 15 in trenches and vias. We have visually confirmed the nitride conformality in trenches of an aspect ratio of 13 and vias of an aspect ratio of 7.

We have extracted a simple via model of a resistor and an inductor in series and have obtained measured inductance values approaching theoretical expectations from this model. The resistance values obtained have issues because of process variations that could be corrected with suggestions made in the next section.

We have also used this technology to demonstrate Faraday cages as a novel isolation scheme for SOC applications. We have measured an improvement in isolation of over 20 dB at 1 GHz at a transmission distance of 100 μm.

5.2 Suggestions for Future Work

5.2.1 Fabrication Improvements

As mentioned in Chapter 2, Section 2.1.2, the DRIE has the problem of etching pockets into the sidewall of the via or trench, which makes conformal lining of the sidewalls difficult. Several

cursory experiments on adjusting the DRIE parameters of C_4F_8 flow, C_4F_8 active time, and APC angle have been performed without positive results. A detailed examination of these DRIE parameters and the cycle overlap time is suggested to improve the quality of the via sidewall for the subsequent liner deposition. Another suggestion is to deposit a film of TEOS first before nitride in order to smooth out the sidewall because TEOS is more conformal than nitride.

From Fig. 2-29, the apparent difference in deposition rate in filling vias with electroplated Cu caused problems in subsequent processing steps. The Al patterning on most overfilled vias was defective because of the non-uniform Al deposition due to shadowing by the Cu overfill cap. Because of the thinner Al around the cap and also because of uneven photoresist coating that results from surface non-uniformity, the Al would etch around the cap, creating an incomplete test structure. A way to increase the uniformity of the electroplated Cu is to incorporate a Cu chemical-mechanical polish (CMP) step into the process. By first overplating all the vias, we could use the CMP to polish back the Cu caps so that vias would be flush with the silicon nitride surface. Cu CMP is used in industry today for Cu interconnects for dual damascene processes [43, 63, 64], and a Cu CMP tool has recently come on-line in MTL.

5.2.2 Test Structures and Measurements

Since we found that a change in probe position along the test structure pad could significantly change the measured inductance of a via, a new two-port test structure that would be insensitive to this effect would be ideal. Also, the design of a true de-embedding structure to subtract out the test structure pad impedance is needed.

5.2.3 Integration of Substrate Vias on a Transistor

To quantify the true benefits of substrate vias to reduce source parasitic inductance of a FET, future work to integrate substrate vias on a power MOSFET is needed. In this way, a comparison of the gain between transistors with and without substrate vias could be accomplished.

5.2.4 Faraday Cages

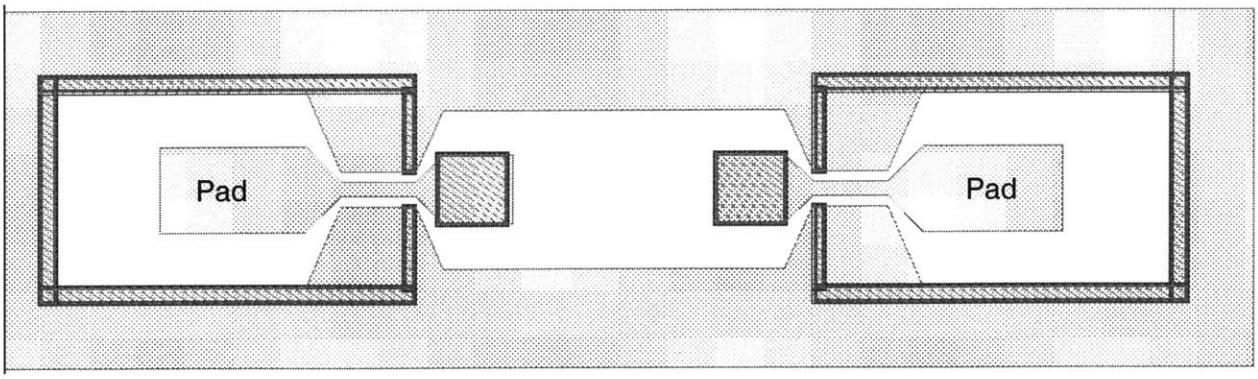

Figure 5-1. Layout picture of a superior test structure for isolation measurements. This structure allows pads to be de-embedded. Courtesy of Jim Fiorenza.

In our measurements, the data taken with the probes in the air and our Faraday cage test structures were similar, indicating we had reached the noise floor of our setup. The crosstalk suppression is beyond the resolution of our measurement setup. A less noisy test bench is needed to accurately determine the isolation improvement of the Faraday cages. Also, a better test structure design as seen in Fig. 5-1 that has a pad structure that can be de-embedded would also reduce the air leakage and noise in the measurements.

Appendix A

SOI Wafer Bonding Process Flow

Starting material: Prime 100-mm, p-type <100> Si wafers, single-side polished (SSP)

Prime 100-mm, p-type <100> Si wafers, double-side polished (DSP) to 400-450 μm thick

	Operation	Parameter	Machine	Lab
1	RCA clean (SSP wafers)		rca	ICL
2	SiO_2 growth (SSP)	Recipe #218: 1150°C, wet, 1 μm SiO_2	tubeB1	ICL
3	RCA clean (all wafers)	Wafers plus Teflon tweezers	rca	ICL
4	Bond wafers	Using Teflon tweezers, drop SSP wafer into same boat slot as DSP wafer with flats aligned, polished sides touching. Squeeze wafers together in center with tweezers.	bonding station	ICL
5	IR inspection	Check for voids under IR camera. Do not anneal wafers with voids greater than ~2 mm in diameter.	bonding station	ICL
6	Anneal (bonded pairs)	Recipe #225: N_2 ambient, 1100°C, 70 min.	tubeA3	ICL
7	Polish back frontside	Send to Skip Hoyt at Lincoln Labs for polish. Remove 410-415 μm.		LL
8	Pirahna clean	Double pirahna clean 3:1 H_2SO_4:H_2O_2, 10 min. (twice) 50:1 H_2O:HF, 1 min.	acidhood	TRL

ICL: Integrated Circuits Laboratory at the Microsystems Technology Laboratories at MIT
TRL: Technology Research Laboratory at the Microsystems Technology Laboratories at MIT
LL: MIT Lincoln Laboratories, Lexington, MA

Appendix B

Substrate-Via Process Flow

Starting material: Prime 100-mm, p-type <100> SOI wafers with 75-170 μm device layer, 400-450 μm handle wafer, 1 μm BOX

100-mm quartz wafer for handle wafer mount, step 12

	Operation	Parameter	Machine	Lab
	Backside:			
1	RCA clean		rca	ICL
2	Si_3N_4 deposition	Recipe #460, 765-785°C, 1:30 hr., 2500 Å	tubeA5	ICL
3	Photolithography			TRL
	3.1 HMDS	150°C, 18 min.	HMDS	
	3.2 Coat photoresist	Coat both sides, backside first then front, 5 min. soft bake (90°C) in between coats. Photoresist: OCG825 Coat: 500 rpm, 6 sec. Spread: 750 rpm, 6 sec. Spin: 3200 rpm, 30 sec. Thickness: 1 μm	coater	
	3.3 Soft bake	90°C, 30 min.	prebake	
	3.4 Exposure	Backside only Mask: KOH1FLIP Time: 45 sec. Contact: Hard	ksaligner2	
	3.5 Develop	Developer: OCG934 1:1 Time: 45-60 sec. with agitation or until photoresist (PR) cleared	photowet-1	
	3.6 DI H_2O rinse	2 min., cascade	photowet-1	
	3.7 Spin dry	2000 rpm, 200 sec.	photowet-1	

	3.8 Hard bake	120°C, 30 min.	postbake	
4	Si_3N_4 etch	Recipe: Nitride CF4 Time: Step 4, 150 sec.	AME5000	ICL
5	Photoresist strip	1 min. each side	asher	ICL
6	Native oxide strip	BOE (7:1), 1 min.	oxide	ICL
7	KOH etch	20% KOH = 250 g KOH:1 L H_2O 80-85°C, 4-5 hrs. Start inspection after 4 hrs.		Schmidt lab
8	Post-KOH clean	Double pirahna clean 3:1 H_2SO_4:H_2O_2, 10 min. (twice) 50:1 H_2O:HF, 1 min.	acidhood	TRL
9	Nitride strip	85% H_3PO_4, 175°C. * Do not spin dry *	nitride	ICL
10	BOX etch	BOE (7:1), 12 min. Air dry.	oxide	ICL
	Frontside:			
11	Photolithography			TRL
	11.1 HMDS	150°C, 18 min.	HMDS	
	11.2 Coat photoresist	Triple coat frontside with 5 min. soft bake (90°C) in between coats. Use jig. Photoresist: OCG825 Coat: 500 rpm, 10 sec. (1st coat), 11 sec. (2nd and 3rd coat) Spread: 770 rpm, 6 sec. Spin: 2000 rpm, 30 sec. Thickness: ~3 μm	coater	
	11.3 Soft bake	90°C, 25 min.	prebake	
	11.4 Exposure	IR alignment to KOH holes Mask: VIA1 Time: 120 sec. Contact: Hard	ksaligner2	
	11.5 Develop	Developer: OCG934 1:1 Time: 5:30-6 min. with agitation, until PR cleared	photowet-l	

	11.6 DI H_2O rinse	2 min.	photowet-l	
	11.7 Blow dry	N_2	photowet-l	
	11.8 Hard bake	120°C, 20 min.	postbake	
12	Handle wafer mount	100-mm quartz wafer Coat: 1600 rpm, variable time. Use acetone and PR to make ring and dot pattern shown in Fig. B-1. Spin: 4000 rpm, 10 sec.	coater	TRL
13	DRIE etch	Recipe: MIT37 (Table B-1)	sts1	TRL
14	Acetone dismount	Soak in acetone for 3-24 hrs. until handle wafer dismounts. Rinse with methanol then DI water. Air dry.	photowet-l	TRL
15	Photoresist strip	≥ 45 min.	asher	TRL
	Nitride Liner:			
16	Pirahna clean	3:1 H_2SO_4:H_2O_2, 10 min. 50:1 H_2O:HF, 1 min.	acidhood	TRL
17	Nitride liner deposition	Front and backside (double deposition) Recipe: joyce, 65% low-freq. power (Table B-2) Thickness: 7000Å on unpatterned surface	concept1	ICL
	Metallization:			
18	Ta/Ti/Cu seed deposition	Backside 250 Å Ta 250 Å Ti 2000 Å Cu	e-beam	TRL
19	Cu electroplating	Pulse-reverse current, J_{ave}=10.8 mA/cm^2 (Fig. C-1)	KOHhood	ICL
20	Solvent clean	Rinse with acetone, methanol, then isopropyl alcohol. Blow dry with N_2.	photowet-r	TRL
21	Al deposition	2 μm Al	e-beam	TRL
22	Photolithography			TRL
	22.1 Coat photoresist	Frontside. Use jig. Photoresist: AZ4620	coater	

		Coat: 1750 rpm, 10 sec. Spin: 2000 rpm, 70 sec. Thickness: ~10 μm		
	22.2 Soft bake	90°C, 1 hr.	prebake	
	22.3 Exposure	Mask: METAL1 Time: 600 sec. Contact: Hard	ksaligner2	
	22.4 Develop	Developer: AZ440MIF Time: 3-4 min. with agitation, until PR cleared	photowet-r	
	22.5 DI H_2O rinse	2 min.	photowet-l	
	22.6 Blow dry	N_2	photowet-r	
	22.7 Hard bake	90°C, 30 min.	prebake	
23	Al etch	Wet etchant: developer 1:1 ratio of OCG934 1:1 and AZ440MIF Time: ~30 min. or until features cleared	photowet-r	TRL

ICL: Integrated Circuits Laboratory at the Microsystems Technology Laboratories at MIT
TRL: Technology Research Laboratory at the Microsystems Technology Laboratories at MIT
Schmidt lab: Laboratory of Prof. Martin A. Schmidt at MIT

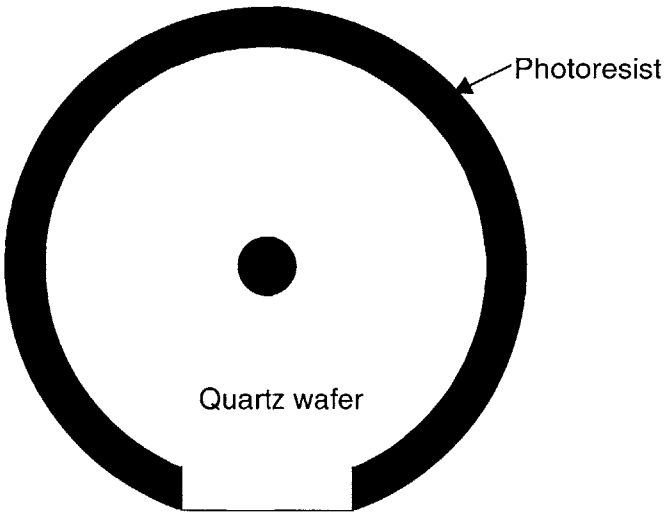

Figure B-1. Photoresist pattern for handle wafer mount in step 12 of the substrate-via process.

Table B-1. DRIE parameters for recipe MIT37.

Parameter	Passivation Cycle	Etch Cycle
SF_6 flow rate	0	140 sccm
SF_6 active time	0	15 sec
C_4F_8 flow rate	95 sccm	0
C_4F_8 active time	11 sec	0
Etch overlap	-	0.5 sec
Electrode power	0	12 W
APC angle	65	65

Table B-2. Novellus Concept-1 PECVD silicon nitride recipe parameters.

Parameter	Value
SiH_4 flow rate	500 sccm
NH_3 flow rate	4000 sccm
N_2 flow rate	1600 sccm
High-Frequency Power	350 W
Low-Frequency Power	650 W
Pressure	2.6 Torr
Temperature	400°C
Deposition Rate	1000-1100 Å/min

Appendix C

Cu Electroplating Current Density Calculations

Refer to Fig. C-1 for the current density waveform. First, choose a duty cycle, D, and average current density, J_{ave}.

$$J_{ave} = J_{ave}^{+} - J_{ave}^{-}$$
$$J_{ave}^{+} = 1.2 J_{ave}$$
$$J_{ave}^{-} = 0.2 J_{ave}$$

where J_{ave}^{+} is the average forward (positive) current density and J_{ave}^{-} is the average reverse (negative) current density. The peak current densities for forward and reverse are defined as follows:

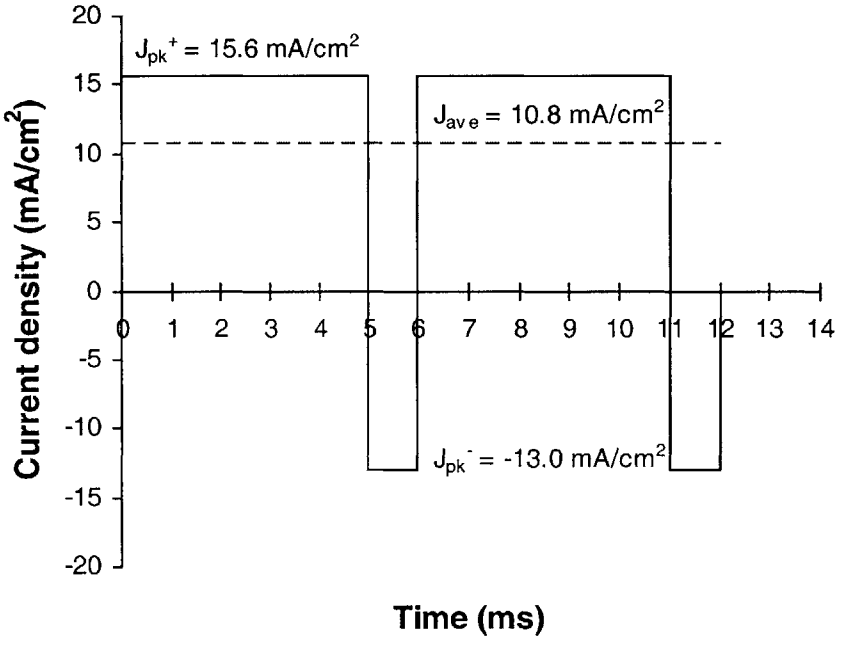

Figure C-1. Current density waveform used for Cu electroplating. The average current density is 10.8 mA/cm^2. The peak forward (positive) current density is 15.6 mA/cm^2, and the peak reverse (negative) current density is -13.0 mA/cm^2.

$$J_{pk}^{+} = \frac{J_{ave}}{D}$$

$$J_{pk}^{-} = \frac{J_{ave}}{1-D}$$

Our experiments use an average current density of 10.8 mA/cm^2 and a duty cycle of 0.83. For the positive pulse, the peak current density is 15.6 mA/cm^2, with an average forward current density of 13.0 mA/cm^2. For the negative pulse, the peak current density is -13.0 mA/cm^2, with an average reverse current density of -2.16 mA/cm^2 [79].

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