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Methodology for Analysis of TSV Stress Induced Transistor Variation and Circuit Performance

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Abstract—As continued scaling becomes increasingly difficult, 3D integration with through silicon vias (TSVs) has emerged as a viable solution to achieve higher bandwidth and power efficiency. Mechanical stress induced by thermal mismatch between TSVs and the silicon bulk arising during wafer fabrication and 3D integration, is a key constraint. In this work, we propose a complete flow to characterize the influence of TSV stress on transistor and circuit performance. First, we analyze the thermal stress contour near the silicon surface with single and multiple TSVs through both finite element analysis (FEA) and linear superposition methods. Then, the biaxial stress is converted to mobility and threshold voltage variations depending on transistor type and geometric relation between TSVs and transistors. Next, we propose an efficient algorithm to calculate circuit variation corresponding to TSV stress based on a grid partition approach. Finally, we discuss a TSV pattern optimization strategy, and employ a series of 17-stage ring oscillators using 40 nm CMOS technology as a test case for the proposed approach.

I. INTRODUCTION

Continual scaling of microelectronic devices has brought serious challenges to the materials and processes of on-chip interconnects beyond the 28 nm technology node. Stacking multiple processed wafers containing integrated circuits into a pseudo three-dimensional (3D) structure provides opportunities for improving performance, for enabling integration of devices with incompatible process flows, and for reducing form factors [1]. Through-silicon vias (TSVs), which directly connect stacked structures die-to-die, are an enabling technology for future 3D integrated systems. The process steps and physical presence of TSVs, however, may introduce mechanical stress and further perturb the performance of nearby transistors and associated circuits. The stress in the silicon is introduced by the processing thermal profile due to the mismatch in thermal expansion coefficient (CTE) between the copper TSV (17.7 ppm/°C) and the surrounding silicon (3.05 ppm/°C) [2]. This mechanical stress can be decomposed in two directions, radial tension and tangential compression, as illustrated in Fig. 1, and affects the carrier mobility and threshold voltage of the adjacent devices. These effects could cause timing violations for digital circuits or current mismatch for analog circuits.

A few papers have reported methods to address TSV stress induced thermo-mechanical reliability or device mobility variation [3], [4], [5], [6]. Ref. [3] provides an analytical formulation for stress distribution around a TSV, referred to as the 2D *Lamé* stress solution. This model was further extended

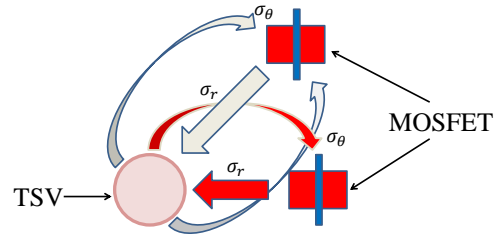


Fig. 1. Stress pattern from TSV to transistors, where σ_r represents radial tension and σ_θ represents tangential compression

to TSV stress effect on mobility to deal with timing issues in digital circuit [5]. Even though this model captures the ideal stress distribution in silicon bulk, it fails to consider an irregular shape of landing pad, liner and effect of stress concentration at silicon surface where the transistor channel is located. A semi-analytical solution was proposed to capture the near-surface stress distribution [4]. However, it is only valid for a TSV with a high aspect ratio and only applicable to a single TSV in isolation. Finite element method (FEM) based device simulations have also been used to numerically analyze the thermo-mechanical stresses and device variation in 3D integrated structures [6]. However, it is often hard to extend this analysis to circuit level due to large computing resources required. Recently, the principle of linear superposition of stress tensors against FEA simulations was validated to generate a reliability metric map on a full-chip scale [7]. However, the problem of how to accurately and efficiently characterize TSV stress impact on circuit performance, especially how to represent this influence for circuit simulation, is still an open question.

In this paper, a complete flow and methodology to analyze transistor characteristics and circuit performance under the influence of TSV stress is proposed. The major contributions of our work are as follows:

- A realistic finite element method simulation of single TSVs considering effects of landing pad, SiO₂ liner and stress concentration. The linear superposition method is then employed to analyze stress distribution under multiple TSVs on a full-chip scale.

- An accurate analytic model converting TSV stress into mobility and threshold voltage variation on nearby transistors which may easily feed into post extraction netlists. Compari-

TABLE I
SUMMARY OF TSV PROCESS STEP CONDITIONS.

	Process Step	Temperature($^{\circ}C$)
1	TEOS liner deposition	400
2	Ta barrier layer deposition	375
3	Cu electroplating	25
4	Annealing (temperature corresponds for effective thermal load)	145
5	Cooling	25

son is also made between measurement result, our model and prior work.

- An efficient algorithm for analyzing circuit variation under TSV stress. Different from prior full chip analyses which focus on digital circuit timing issues, this work is also valid for RF/analog circuits.

- Prediction of ring oscillator performance around TSVs at the 40nm node. The interaction between layout and circuit performance is predicted by the new stress models.

II. FEM BASED TSV STRESS MODELING

In this section, we calculate the single TSV induced stress distribution through FEM simulation and extend to multiple TSV stress analysis through linear superposition. An accurate stress contour is the basis for calculating mobility threshold voltage variation.

A. Baseline FEM model for isolated TSV

To study the thermal stress distribution of an isolated copper TSV with liner and landing pad, a finite element analysis is performed using the commercial package, COMSOL. An axial symmetric property is assumed in this simulation. The critical process step conditions that we assume for simulation of TSV stress are summarized in Table I [3], [6].

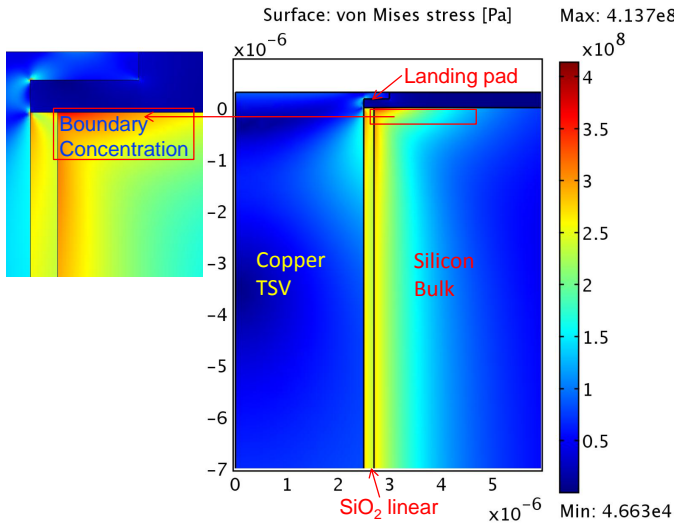


Fig. 2. Von Mises stress distribution around the TSV

Our baseline TSV process mimics the via middle technology in 3D IC manufacturing and the basic structure sizes are

summarized as followed [6]. Wafer direction is selected to be (100)/<110> and CMOS transistors are located at the silicon surface. TSVs are etched with a depth of $30\mu m$ and a $5\mu m$ diameter. A $200nm$ thick oxide liner is deposited using TEOS CVD and a $5nm$ Ta barrier is fabricated with PVD Ta. Then the copper TSV is electroplated and annealed subsequently. A CMP process is introduced after a $6\mu m$ landing pad is electroplated. In order to isolate stress contributed by the TSV, both shallow trench isolation (STI) and contact etch stop layer (CESL) structure are not included in this simulation. Material properties used for our experiments are as follows: thermal expansion coefficient ($ppm/^{\circ}C$): $\alpha_{Cu}=17.7$, $\alpha_{Si}=3.05$, $\alpha_{SiO_2}=0.5$; Young's modulus (GPa): $E_{Cu}=70$, $E_{Si}=130$ and $E_{SiO_2}=70$; Poisson ratio: $\nu_{Cu}=0.34$, $\nu_{Si}=0.28$ and $\nu_{SiO_2}=0.17$.

Fig. 2 shows the FEA results for von Mises stress distribution around the TSV. We find that the stress concentration can make the stress at the silicon surface larger than in the silicon bulk. Since the TSV structure is axial symmetric and silicon is assumed to be isotropic, we adopt a cylindrical coordinate system in the first step and then convert the tensor matrix into a Cartesian coordinate system. In our simulation, the normal stress σ_r and σ_ϕ are two major components in stress distribution, as shown in Fig. 1. We further compare normal stress distribution at silicon surface and silicon bulk, both of which are from FEM result, with 2D Lamé solution, as is shown Fig. 3. It shows that while the Lamé solution matches well with silicon bulk case, it does not capture the irregular characteristics of TSV surface stress distribution correctly, especially for near TSV region.

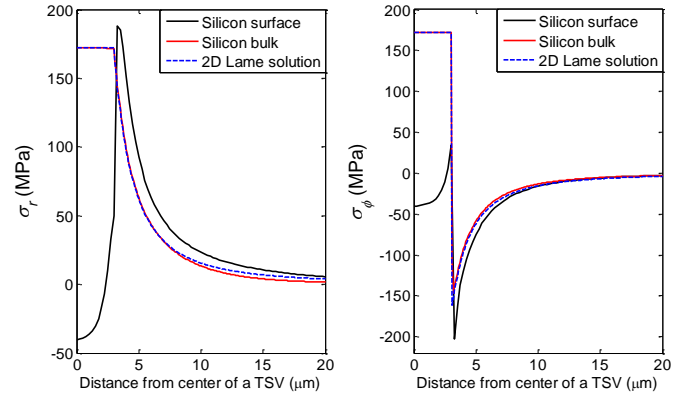


Fig. 3. TSV stress effect on σ_r and σ_ϕ .

B. Multiple TSV Stress Contour

While FEM gives a very accurate axial symmetric distribution of stress around a single TSV, we cannot perform this kind of “exact” simulation on a full chip scale since FEM is too computationally costly to apply to large areas with complex TSV layout pattern. However, we do have a solution to analyze stress distribution with multiple TSVs in full chip scale because the baseline TSV structure is highly repeatable and the stress tensor is linear superposable within

the stress scope generated by TSVs [7]. Before doing this, we need to convert the cylindrical coordinate tensor $T_{r\phi z}$ to a Cartesian coordinate system tensor $\hat{T}_{[110]}$ with three axes at $[110]$, $[1\bar{1}0]$, and $[001]$ respectively according to transistor channel direction. The method is discussed in Appendix A where ϕ is the angle between the x-axis and a line from the TSV center to the simulation point and $\theta = 0^\circ$. Fig. 4 shows a single TSV stress contour for σ_{xx} and σ_{yy} after the coordinate transformation. Then we can perform linear superposition method at any point needed by adding up stress tensor of different TSV within $25\mu\text{m}$.

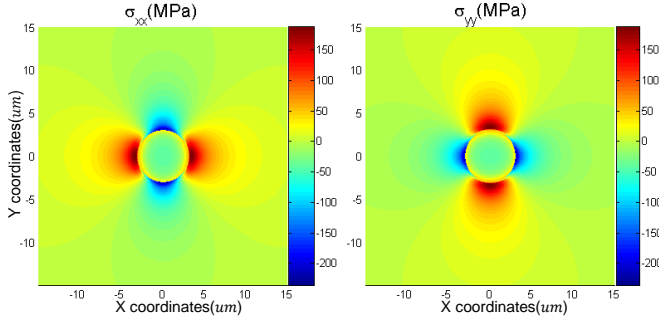


Fig. 4. σ_{xx} and σ_{yy} contours.

III. MOBILITY AND THRESHOLD VOLTAGE VARIATION RELATED TO TSV STRESS

With the FEM simulation result and superposition method, we obtain an accurate channel stress tensor for each transistor. To estimate $\Delta\mu/\mu$ and $\Delta V_{th}/V_{th}$ as a function of stress applied to a MOSFET with respect to its unstressed condition, we will further develop the corresponding variation model combining linear piezoresistance theory and energy calculation. This model is also verified using published device simulation results.

A. Mobility Variation Modeling

Mobility variation, which corresponds to drive current and transistor speed, is one of the most critical consequences induced by stress. For modern technologies, both intentional stress (such as CESL and Si-Ge stress) and unintentional stress (such as STI and TSV stress) are introduced and the transistor performance is affected accordingly. For elastic materials such as silicon, the superposition rule holds under small deformation conditions. In this situation, we may decouple the complex stress distribution by different stress sources. To better illustrate mobility and V_{th} variation induced by TSV stress, we assume that the neighboring environment of transistors is constant and only the TSV location is varying. Therefore we may deal with this problem as adding a small stress variation (TSV stress) on a large fixed stress operating point (the total stress contributed by other sources). Since TSV stress is small ($<200\text{MPa}$) compared with the total stress (normally several GPa), this approach has good linearity. A linear piezoresistance model is the most widely employed

model to depict this effect [8]. The validity of the model is verified with coefficients taken either from measurements or from calculations [9]. Since our coordinate system already corresponds with the transistor channels, we use the following well known equation to express mobility changes:

$$\Delta\mu/\mu = \Pi_L \cdot \sigma_{xx} + \Pi_T \cdot \sigma_{yy} \quad (1)$$

Here Π_L and Π_T represent longitudinal and transverse piezoresistance coefficients for $(100)/\langle 110 \rangle$. Note that these coefficients should take account of effects contributed by channel doping because this would cause quantization splitting and alters the conductivity mass [10].

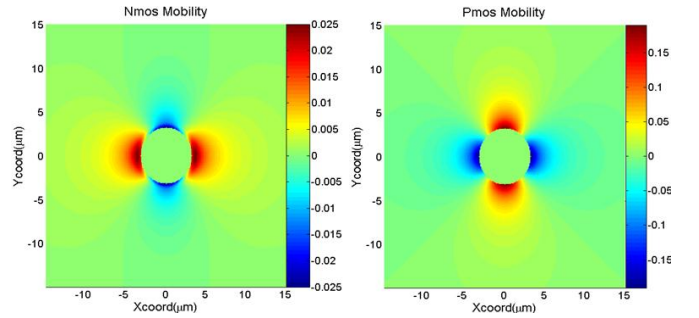


Fig. 5. Comparison between nMOS and pMOS mobility variation maps.

Simulated mobility contours for nMOS and pMOS transistors are compared in Fig. 5. We find that nMOS transistors are almost immune from TSV stress, which is different from result in Ref. [5] where nMOS is also strongly affected by TSV stress. This is because n-channel piezoresistance coefficient Π_L and Π_T have the same sign and the two items in equation (1) counteract each other. The pMOS transistors, on the other side, suffer more from the different sign of p-channel piezoresistance coefficient Π_L and Π_T and the two items reinforce. In addition, mobility is immune from TSV stress in diagonal direction because shear stress does not contribute to mobility change. This property can be further exploited to optimize TSV and transistor layout configurations, as discussed in Section IV.

The accuracy of FEM based stress and mobility model are validated by 3D FEM device simulation [11], as shown in Fig. 6. The mobility variation predicted by the 2D *Lamé* solution is also compared in the same figure. Although the *Lamé* solution captures the general trend of mobility variation, it could still cause a maximum error with 3% of the total mobility.

B. Threshold Voltage Variation Modeling

Threshold voltage is also significantly affected by TSV stress because strain can induce shifts and splits in both conduction and valence bands. However, there is no intuitive way in piezoresistance theory to depict this effect through coefficients from direct measurement. Therefore we introduce deformation potential theory to calculate the impact of TSV

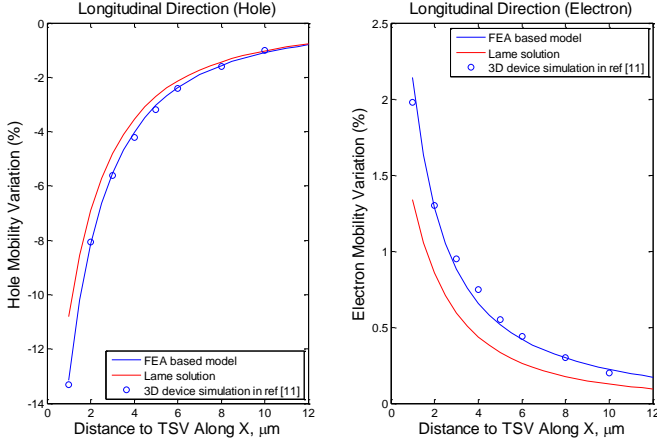


Fig. 6. Variation of the mobility versus distance to TSV from modeled data and 3D device simulation [11].

stress on threshold voltage. For the first time, the impact of TSV stress on threshold voltage is estimated.

Since strain is the direct cause of energy splitting, we need to convert stress tensor from current coordinates $\hat{T}_{[110]}$ into crystallographic coordinate tensor \hat{T} using the method discussed in Appendix A, where $\phi = 45^\circ$ and $\theta = 0^\circ$. Then stress is transformed into strain according to Appendix B.

After that, the hydrostatic shift and shear splitting of the valence band ΔE_V and conduction band ΔE_C edges can be calculated through the following equations [12]:

$$\Delta E_C^{(i)}(\sigma) = \Xi_d(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + \Xi_u \varepsilon_i \quad (2)$$

$$\Delta E_V(\sigma) = a(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + [b^2(\varepsilon_2 - \varepsilon_3)^2 + d^2 \varepsilon_6^2/4]^{1/2} \quad (3)$$

TABLE II
BAND EDGE DEFORMATION POTENTIAL CONSTANTS [12].

	Ξ_d	Ξ_u	a	b	d
Deformation potential constants (eV)	1.13	9.16	2.46	-2.35	-5.08

In equation 2 and 3, the hydrostatic term (with parameters Ξ_d and a) takes account of the band edge shift without change in degeneracy, and the shear term (including parameters Ξ_u , b and d) split the valence and conduction band states. The deformation potential constants are summarized in Table II.

With both ΔE_C and ΔE_V , the expression for the strain-induced threshold-voltage shifts becomes [13]:

$$\Delta V_{thn}(\sigma) = -m\Delta E_C + (m-1)\Delta E_V \quad (4)$$

$$\Delta V_{thp}(\sigma) = (m-1)\Delta E_C - m\Delta E_V \quad (5)$$

where m is the body-effect coefficient.

Simulated threshold voltage variation contours for nMOS and pMOS are shown in Fig. 7, where x and y axis represent $[110]$, $[1\bar{1}0]$, respectively. Because of the biaxial property of TSV stress, the threshold voltage shift is greatly reduced. Therefore the stress effect on threshold voltage is much less

than uniaxial stress reported elsewhere [12]. In addition, the ΔV_{th} contour is almost axisymmetric, but the axial direction is more affected because the shear term also contributes to ΔV_{th} . However, considering that the threshold voltage in advanced technology node is around 100 mV , the variation induced by TSV stress amounts to 8% of the total threshold voltage, which should not be neglected.

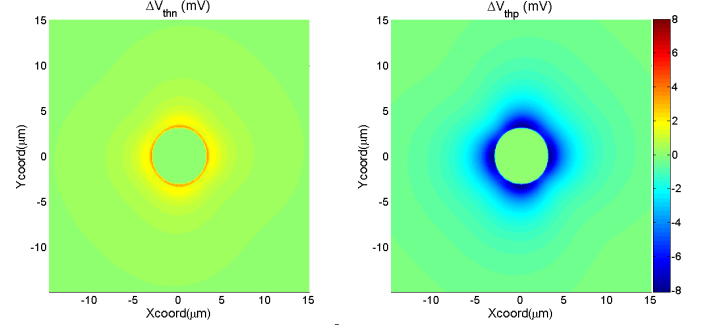


Fig. 7. Comparison between nMOS and pMOS V_{th} variation maps.

IV. ANALYSIS AND OPTIMIZATION OF CIRCUIT CONSIDERING TSV STRESS EFFECTS

The changes in transistor characteristics due to TSV stress alters circuit performance around TSVs. While the existing work has focused on timing analysis of digital circuits [5], we propose here a more comprehensive flow to characterize circuit variation in both analog and digital circuits.

A. Stress Aware Circuit Analysis

As noted above, TSV stress-induced transistor variation is determined by: (1) the separation between the TSV and the transistor, and (2) the angle between the x-axis and a line from the TSV center to the transistor. With LVS extraction result, both information can be obtained and a TSV stress aware circuit simulation is possible. Because our purpose is to analyze transistor performance under TSV stress, there is no need to generate stress tensor for each point in the full chip. In this work, an efficient algorithm based on a partition grid is proposed for analyzing circuit performance under TSV stress, as shown in algorithm 1.

This flow: (1) reads the geometrical and coordinate information of transistors and TSVs; (2) partitions the chip into $50\mu\text{m} \times 50\mu\text{m}$ grids and categorize each TSV into grids within its influence zone; (3) categorizes each transistor into a particular grid and generates its stress by superposition of TSV stress within the same grid; (4) calculates the amount of variation in transistor characteristics using out TSV stress variation models; and (5) outputs a SPICE netlist reflecting the calculation results. In the SPICE netlist, the characteristic variations are specified with MULU0 and DELVTO. Then the impact of these variations can be considered by performing a SPICE simulation using the SPICE netlist. The complexity of this variation extraction algorithm is $O(nk)$, where n is the number of transistors and k is the average number of TSVs

```

Input: chip,  $C$ ; set of TSV list,  $T$ ; set of transistor list,
 $Tr$ ; TSV stress tensor matrix map  $M$  and
influence distance  $r$  for single TSV
Output:  $umulu0, delvto$  for each  $tr \in Tr$ 
set of Grid,  $G \leftarrow \text{PartitionChipIntoGrid}(C)$ ;
for each TSV  $t \in T$  do
  for each  $g_i \in \text{FindTSVGrid}(t)$  do
     $g_i.t \leftarrow t$ 
  end
end
for each transistor  $tr \in Tr$  do
   $g \leftarrow \text{FindTransistorGrid}(tr)$ ;
  for each TSV  $t' \in g$  do
    if  $\text{Distance}(t', tr) < r$  then
       $tr.stress \ += \text{FindAvgStressTensor}(t', tr,$ 
       $M)$ ;
    end
  end
   $tr.umulu0 \ += \text{ComputeMuVar}(tr.stress)$ ;
   $tr.strain \leftarrow \text{CovertStressToStrain}(tr.stress)$ ;
   $tr.delvto \ += \text{ComputeVthVar}(tr.stress)$ ;
end

```

Algorithm 1: Stress aware circuit analysis.

per grid. The influence zone of a TSV is selected to be $25\mu m$. One TSV could belong to multiple grids if there is any overlap between its influence zone and those grids. The length of a grid side, $50\mu m$, is decided through an optimization process to minimize k .

B. TSV Placement Optimization

After a full chip analysis, we are able to further optimize TSV placement and reduce the impact of TSVs on transistors.

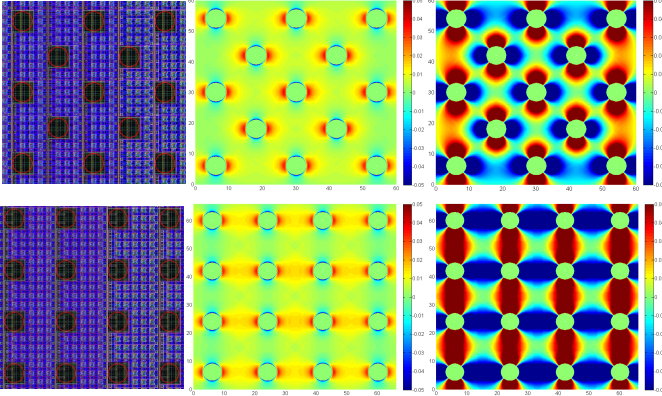


Fig. 8. Comparison between TSV “diamond” matrix and “square” matrix for realistic layout (left), electron (middle) and hole (right) mobility variation contours.

As an example, we first compare mobility variation between “diamond” and “square” TSV layout patterns with the same TSV density, as shown Fig. 8. The TSV pitch (minimum TSV distance) in both TSV configurations are selected to be $18\mu m$, which is a standard distance between TSV in 3D

IC chips. In square configuration, the interaction between neighboring TSV intensifies the mobility variation, while in diamond configuration the interaction between neighboring TSV cancels the mobility variation. Since TSVs have an almost opposite impact on x and y axis for pMOS transistors, the crossover area is less affected by TSV stress.

To further investigate effect of TSV layout pattern on nearby circuit, a Keep-Out-Zone (KOZ) is defined as an area where transistor mobility variation is larger than a certain limit. In this example, a criterion for KOZ is set as 0.5% and 5% variation of total mobilities for analog and digital MOSFETs, respectively. Fig 9 shows the comparison for analog KOZ and allowable layout area between different TSV patterns and pitches, where green area represents for allowable layout area and red area represents the KOZ.

TABLE III
ALLOWABLE LAYOUT AREA FOR DIGITAL CIRCUITS.

	Analog or Digital	TSV pitch (μm)	TSV pattern	nMOS area	pMOS area
1	Digital	18	Diamond	89.05%	65.61%
2	Digital	18	Square	90.67%	50.49%
3	Digital	12	Square	77.99%	28.38%
4	Digital	24	Square	94.41%	78.21%
5	Analog	18	Diamond	15.22%	17.87%
6	Analog	18	square	25.32%	10.31%
7	Analog	12	square	12.25%	5.99%
8	Analog	24	square	58.45%	15.13%

The percentage of allowable layout area for analog and digital circuits with different TSV pattern are summarized in Table III. As discussed earlier, pMOS transistors are significantly affected by TSV stress and nMOS digital transistors are almost immune from TSV stress. However, an interesting result appears that analog nMOS transistor are also strongly influenced by TSV arrays. This is mainly because TSV stress has more impact on longitudinal direction than transverse direction, and this effect is increased by parallel TSVs. We may also observe that “diamond” TSV pattern benefits pMOS transistor in both analog and digital with 7.56% and 15.12% more allowable layout area. However, this configuration also greatly reduces digital nMOSFET layout area to 15.22%, which is comparable to pMOS case. In summary, the “diamond” TSV pattern provides more balanced layout area for nMOSFET and pMOSFET compared with “square” pattern.

C. Circuit Performance Analysis: Ring Oscillator Around TSV

While the previous case study is about how multiple TSVs affect one transistor, in this part we analyze how a single TSV affects performance of a circuit that is an aggregate of many transistors. We use realistic 17-stage ring oscillators (ROs) designed in 40 nm CMOS technology to show TSV stress impact on RO frequency using the proposed model. Sixteen groups of RO devices under test (DUTs) around a TSV are designed to characterize the TSV’s influence in various locations, as shown in Fig. 10. The surrounding area around each group of ROs is carefully designed to cancel out other systematic variations.

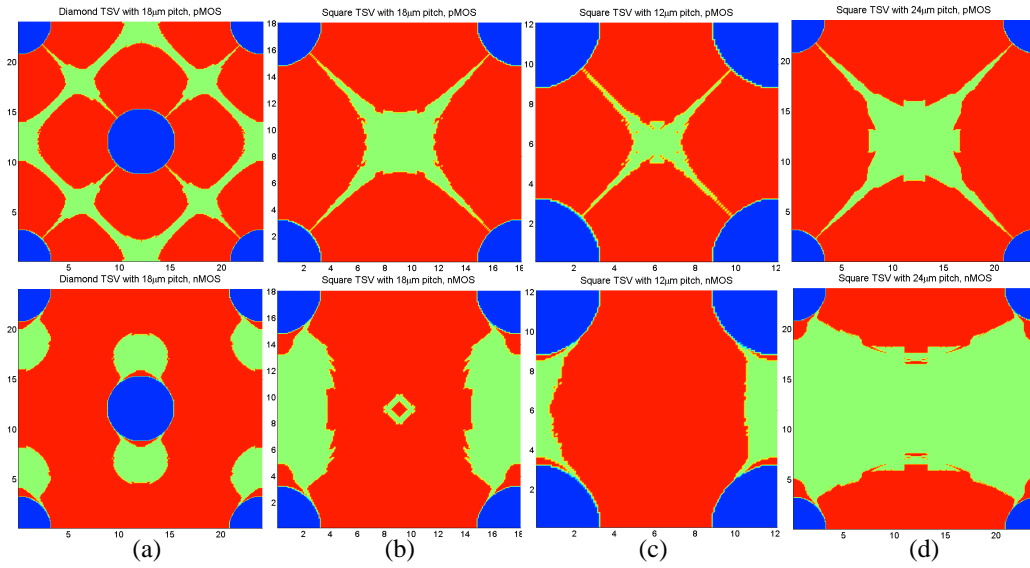


Fig. 9. nMOS and pMOS “unit cell” comparison for analog KOZ and allowable area between: (a) “diamond” TSV with $18\ \mu\text{m}$ pitch; (b) “square” TSV with $18\ \mu\text{m}$ pitch; (c) “square” TSV with $12\ \mu\text{m}$ pitch; and (d) “square” TSV with $24\ \mu\text{m}$ pitch

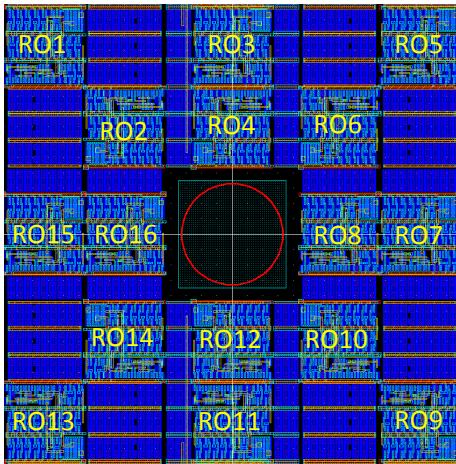


Fig. 10. Layout of TSV and the sixteen 17-stage ring oscillator groups.

We first generate transient waveforms of all 16 ROs, as shown in Fig. 11. Because ratio of carrier velocity change to mobility change $\Delta v/\Delta\mu$ tends to saturate in advance technologies, the TSV stress does not bring significant change to circuit delay ($\approx 2\%$).

Fig. 12 further shows how RO frequency changes according to their geometric relation with TSV. While we see that most RO groups in the diagonal direction are not affected, the 4th and 12th RO groups become slower, and the 8th and 16th RO groups become faster. This is because TSV stress on pMOS is more evident than that on nMOS.

D. Test Chip

A test chip has been implemented in a 40nm TSMC CMOS process. DUT arrays under the stress effect of single and multiple TSVs are built to validate the aforementioned

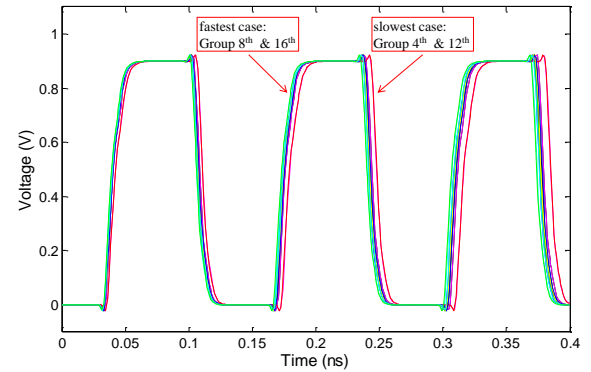


Fig. 11. RO waveforms for sixteen different 17-stage ring oscillators.

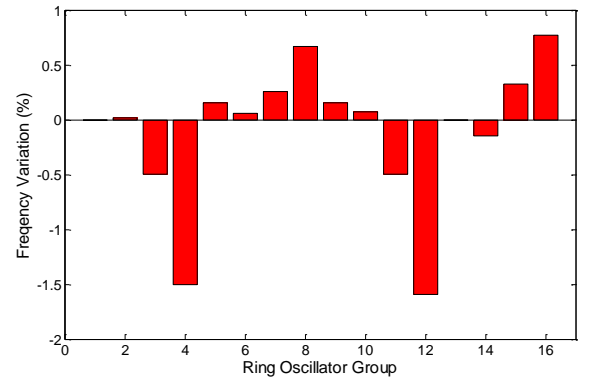


Fig. 12. Frequency variations of the sixteen ring oscillator groups.

mobility and V_t model. A series of ring oscillators are also designed to characterize and identify the influence of TSV on digital circuits. The layout of each block is shown in Fig. 13.

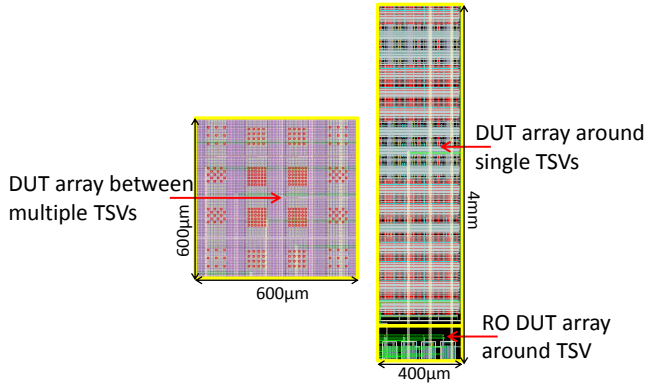


Fig. 13. Test circuit layout.

V. CONCLUSIONS

In this paper, a complete flow for analyzing circuit performance under the impact of TSV stress is proposed. At the stress characterization level, we show how realistic TSV process and structure affects stress distribution, and show how to convert the FEM stress model into stress tensor matrix. At the device modeling level, we propose a fast and accurate model to capture TSV stress induced variation on mobility and threshold voltage. At the circuit level, we propose a fast and efficient extraction flow to combine our model with commercial circuit simulation tools. Optimization of TSV layout pattern and a case study of ring oscillators around TSVs is also presented, to illustrate our proposed flow and methodology.

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APPENDIX

A. Stress Tensor Coordinate Transformation

we summarize how the stress tensor is transformed between different coordinate systems. Consider a generalized direction $[x', y', z']$ in which the stress is applied. The stress in the coordinate system $[x, y, z]$ can be calculated using the transformation matrix U

$$U(\theta, \phi) = \begin{bmatrix} \cos \theta \cos \phi & \cos \theta \sin \phi & -\sin \theta \\ -\sin \phi & \cos \phi & 0 \\ \sin \theta \cos \phi & \sin \theta \sin \phi & \cos \theta \end{bmatrix} \quad (\text{A.1})$$

Here θ denotes the polar and ϕ the azimuthal angle of the stress direction relative to the new coordinate system. The stress in the new coordinate system is then given by

$$\hat{T}^{new} = U \cdot \hat{T} \cdot U^T \quad (\text{A.2})$$

B. Stress-Strain Relationship

Here we summarize the transformation between stress and strain.

$$\begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{12} & 0 & 0 & 0 \\ s_{12} & s_{11} & s_{12} & 0 & 0 & 0 \\ s_{12} & s_{12} & s_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{44} \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} \quad (\text{B.1})$$

In equation B.1, the transformation matrix is the tensor of elastic stiffness for silicon.