A 3.4-pJ FeRAM-Enabled D Flip-Flop in 0.13-μm CMOS for Nonvolatile Processing in Digital Systems

A 3.4 pJ FeRAM-Enabled D Flip-Flop in 0.13 μm CMOS for Nonvolatile Processing in Digital Systems

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Abstract

In order to realize a digital system with no distinction between "on" and "off," computational state must be stored in non-volatile memory elements. If the energy cost and time cost of managing computational state in nonvolatile memory can be lowered to the microsecond and picojoule per bit level, such a system could operate from unreliable harvested energy, never requiring a reboot. This work presents a nonvolatile D flip-flop (NVDFF) designed in 0.13 μm CMOS that retains state in ferroelectric capacitors during sporadic power loss. The NVDFF is integrated into an ASIC design flow, and a test-case nonvolatile FIR filter with an accompanying power management unit automatically saves and restores state based on the status of a one-bit indicator of energy availability. Correct operation has been verified over power cycle intervals from 4.8 μs to 1 day. The round-trip save-restore energy is 3.4 pJ per NVDFF. Also presented are statistical measurements across 21,000 NVDFFs to validate the capability of the circuit to achieve the requisite 10 ppm failure rate for embedded system applications.

Index Terms

Digital electronics, embedded systems, low-power electronics, nonvolatile memory, registers, latches, ferroelectric random access memory, energy harvesting

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I. Introduction

Nonvolatile processing—continuously operating a digital circuit and retaining state through frequent power interruptions—creates new applications for portable electronics operating from harvested energy [1] and high-performance systems managing power by operating "normally off" [2,3]. To enable these scenarios, energy processing must happen in parallel with information processing.

The cartoon in Fig. 1 illustrates nonvolatile operation under energy harvesting. When sufficient energy exists in the system to establish a functional supply level, the circuit computes. When energy is lost and VDD cannot be maintained, the circuit stops processing and retains state in its registers. The transition from computing to retention and vice versa involves the automatic management of state in nonvolatile memory elements. The goal of this work is to minimize the cost of these transitions in terms of energy and time. Ferroelectric capacitors are a promising low-power nonvolatile technology for this application. Compared to other nonvolatile technologies, ferroelectric random access memory (FeRAM) has been shown to consume the least amount of energy per read or write operation compared to other nonvolatile memory technologies; although, it has a larger cell area [4]. Several developments in nonvolatile processing have been introduced [5]–[7], but practical challenges related to system integration prevent their widespread use while further improvement in save/restore energy and time can still expand the scope of this technology.

As a test-case for nonvolatile operation, the 3-tap FIR filter in Fig. 2 will be implemented. The following describes its input-output relation:

$$y[n] = w_3 \cdot x[n-7] + w_2 \cdot x[n-6] + w_1 \cdot x[n-5]. \tag{1}$$

The registers in this FIR filter will contain embedded nonvolatile memory elements, and the FIR filter's continued operation under power interruption will demonstrate the desired nonvolatile operation. First, a nonvolatile D flip-flop (NVDFF) with embedded ferroelectric capacitors (fecaps) that senses data robustly and avoids race conditions is presented. Next the NVDFF is integrated into the ASIC design flow with a power management unit (PMU) and a simple one-bit interface to brown-out detection circuitry . Finally the NVDFF statistical signal margin and the energy cost of retaining data is characterized.

II. The design of the NVDFF

Table I summarizes the properties of the technology used in this work. Embedded ferroelectric capacitors (fecaps) store data in a charge versus bias voltage hysteresis illustrated in Fig. 3. Writing data to an fecap requires applying either +VDD or -VDD across its two terminals. By engineering the fecap hysteresis coercive limits to be compatible with the CMOS transistor supply voltage, the write operation becomes simple. A register can quickly save its state to ferroelectric capacitors with simple static CMOS logic. A circuit-level description of the ferroelectric capacitor can be found in [4].

Reading the ferroelectric capacitors is more challenging because extracting the charge does not directly produce a full-rail static CMOS voltage output. The conventional approach shown in Fig. 4 is based on [5] and [6]. A master latch, slave latch, and pair of ferroelectric capacitor dividers comprise this NVDFF. Either four or two of the capacitors are written to opposite data states by passing the slave latch node voltages to nodes QT and QC while sequencing PL1 and PL2 appropriately. When sensing the fecaps[1], PL2 is held low while PL1 is pulsed from low to high. For a supply voltage of 1.5 V and writing all four capacitors to opposite data states, approximately $400mV$ of nominal differential signal, $V_{\mathrm{QT}} - V_{\mathrm{QC}}$, can be developed between QT and QC because the effective capacitance of an fecap depends on its state. The common mode voltage, $(V_{\mathrm{QT}} + V_{\mathrm{QC}})/2$, is near $\mathrm{VDD}/2$. This small signal is passed to the slave latch and amplified to full-rail CMOS levels by enabling the cross-coupled inverters in the slave latch.

The concept of a NVDFF—based on fecaps or other nonvolatile technologies—has been well established; however, several challenges to system integration have prevented its widespread adoption. These challenges are enumerated in Table. II. First, the voltage bias on the ferroelectric capacitors should be maximized to prevent very slow signal development. Fecap signal dynamics are exponentially sensitive to voltage bias, so it is important to avoid the performance penalty associated with sensing at low bias. The data in [8] suggests that the electric field from 0.6 V of bias in this work's technology will require over $10\mu s$ to develop 80% of the signal. On the other hand, [9] has shown 1.2 V or higher extracts most signal under $100ns$.

Secondly, when the system power supply is in an unreliable brown-out condition, glitches must

[1]In this paper, the words "sense" and "restore" have very similar meaning. The word "sense" emphasizes the process of *converting* the ferroelectric capacitor remnant charge into a logic-level voltage signal; whereas, the word "restore" signifies the abstract operation of an NVDFF recovering the data it held prior to power-loss.

be prevented from corrupting the fecap state. Tracing from the capacitor nodes through transistors in Fig. 4 shows that unreliable voltages on nodes WL and CK can cause unwanted voltage to develop across the ferroelectric capacitors. Third, to prevent damage and imprint in the sensitive dielectric of the fecap, zero bias must be maintained across the fecaps during active operation. Fourth, the sensing operation cannot rely on multiple timing edges that require careful control with respect to each other. The NVDFFs are interspersed in a sea of digital gates with automated routing, and must function in an environment just exiting brown-out. Fifth, the peak current from simultaneously toggling the fecaps in thousands of NVDFFs can far exceed the current specification during normal operation of the circuit. The peak current is especially constrained for this work's targeted microcontroller application. Therefore careful design must ensure that the peak current during save and restore remains compatible with the current consumption of normal operation. Sixth, analog circuit techniques to maximize the sensing margin have limited benefit if they require additional time for bias currents and voltages to settle. Seventh, the digital circuit should automatically start or stop computation and manage state based on the amount of available energy for operation. Such a behavior requires that multiple control signals are internally generated for writing and reading nonvolatile memory elements. Finally, the resulting solution should be compatible with the ASIC design flow so that the NVDFF can be adopted without increasing design complexity and cost. The final challenge, poses a significant barrier to local memory array approaches because the physical designer has to develop a circuit-dependent approach to integrating the nonvolatile memory elements.

With regards to these eight challenges to system integration, an alternative NVDFF is developed, based on integrating a nonvolatile latch (NVLATCH) into the slave stage of a conventional DFF. Shown in Fig. 5(a) is a simplified schematic of the proposed sensing scheme in the NVLATCH and Fig. 5(b) shows the associated waveforms. Prior to sensing, the fecaps have been programmed to opposite data states, corresponding to opposite points on the zero bias voltage points of the hysteresis curve. Identical charging currents integrate the difference in remnant charge between the two fecaps onto nodes FET and FEC. In other words, both capacitors experience an identical vertical displacement (charge axis) on the hysteresis of Fig. 3, but different horizontal displacements (voltage axis) depending on the starting point of "0" or "1."

The node to first cross the diode voltage drop plus a PMOS threshold will quickly pull the internal node of the sensing latch high. The incremental capacitance on the ferroelectric capacitor

nodes is large (roughly 200 fF) compared to the internal node of the sensing latch (roughly 10 fF), so a small voltage difference on the high capacitance nodes FET and FEC is converted to a large voltage difference on the latch nodes. In addition to being self-timed (solving challenge #4), this circuit topology ensures sufficient bias (1.1 V) across the fecap before its data is captured (solving challenge #1).

The schematic of the nonvolatile latch in Fig. 6 shows the additional transistors for saving data, isolating fecaps during active operation, and protecting fecaps during power loss. This latch is combined as the slave stage with a clocked CMOS master latch to form the NVDFF in Fig. 7. Also included, but not shown, are transistors in the master and slave stages to implement an asynchronous active-low reset. The waveforms in Fig. 8 show how the ports PG, LD, EQ, and VDDNV need to be sequenced during power interruption.

While active, PG=LD=0, and nodes FET and FEC act as a virtual supply for the slave latch. The opposite plate of the ferroelectric capacitors, node SN, is also at the same potential as VDDNV, resulting in 0 V across the fecaps during active operation (challenge #3). The save operation initiates when PG rises as CK is held low, cutting off VDDNV and enabling a weak pull-down path (M8-M10) to discharge one of the two fecaps (write “0”) depending on the data state of the slave latch. The subsequent rise of LD preserves the data in the other fecap, which has already been written to a “1” during the previous restore operation. Prior to power loss, the EQ signal assertion clears floating voltages inside the slave latch, and then the VDDNV rail is discharged to prevent unintentional conducting paths to nodes FET/FEC (solving challenge # 2). A complementary sequence is applied after VDD and VDDNV return high for restore. First, PG falls low, biasing M1 and M2 into their saturation region through the PMOS diodes M3 and M4. The sense operation completes and the correct value appears on the NVDFF Q output. When LD falls low, the voltages across the fecaps are cleared and the NVDFF can resume active operation. The four operating modes of the NVLATCH are summarized in Table. III.

It should be noted that the NVDFF itself has no fundamental disadvantage for active power consumption relative to a volatile DFF because the fecaps are isolated; however, the performance is degraded. Under typical process-voltage-temperature (PVT) conditions and small load with sharp edges, the clock-to-q delay for the falling output (4 x Fo4) is roughly twice the delay for the rising output transition (2 x Fo4) because the former transition has to first propagate through the slave stage jam latch before driving the output inverter buffer. The performance degradation

is tolerable because the microcontroller systems this technology targets operate at clock periods equal to 150 x Fo4 or larger (800 x Fo4 in this work).

Both the pull-up and pull-down paths for nodes FET/FEC are sized weak so that no more than 10 μA of peak current is drawn by each NVDFF (challenge #5). These issues related to avoiding race conditions, sensing fecaps at high voltage bias, and minimizing peak current prevent the adoption of the conventional ferroelectric DFF based on a pair of fecap dividers [5] (challenges #1, #4, #5). Additionally, Table. IV shows that the proposed NVDFF consumes 40% less energy (from simulation) because it contains 2 fecaps instead of 4. Finally, the NVDFF still satisfies challenge #6 because it requires only one low-accuracy bias voltage, generated dynamically through PMOS diodes within 10ns of the beginning of the microsecond-scale restore operation.

III. System-level nonvolatile state management

Figure. 9 shows the architecture of the nonvolatile state management. A test case FIR filter has all of its volatile DFFs replaced by NVDFFs of the type described in section II. Only one type of NVDFF—asynchronous active-low reset without scan chain—is employed. Also added are buffer trees for the PG, LD, and EQ signals and a global rail VDDNV that supplies current for the toggling of internal slave latch nodes and FET/FEC. This system works with the energy harvester interface in [10] which provides a VBAT_OK signal that rises only if a sufficient amount of energy exists in the system to restore and save state. Similarly VBAT_OK falls when the system is about to lose its minimum energy reserve. A free running clock that settles before VBAT_OK goes high is also required. An on-chip power management unit (PMU) takes the VBAT_OK signal and generates a control signal sequence (see FSM in Fig. 10) whose transitions align to the PMU's clock edges and satisfy the timing constraints in Fig. 8 (solving challenge #7).

To incorporate the NVDFF into the ASIC design flow (challenge #8), the following modifications are necessary:

1) Exclude volatile DFFs during synthesis.
2) Add PG, LD, EQ ports to NVDFF instances in the post-synthesis structural netlist.
3) Create nonvolatile related ports PG, LD, EQ in the top-level of the physical design.
4) Create a global power rail for VDDNV, which is a low-current rail without explicit decoupling capacitance.

5) Route NVDFFs to the VDDNV rail.
6) Synthesize buffer tree for PG, LD, EQ with a maximum skew constraint of 10ns (targeting a 200 ns clock period for the PMU).

The modifications above do not influence how the front-end designer writes the behavioral description of the circuit. In the physical design stage, the most critical timing is the skew constraint for the PG, LD, EQ signals which easily meets the chosen requirement of $10ns$. The self-timed nature of the sensing operation in the NVLATCH enables this relaxed timing constraint. Namely, the slave latch automatically senses the fecap state after PG falls low without the need for an additional control signal. In addition, the VDDNV rail does not require explicit decoupling capacitance because it supplies very little current. It supplies less than $10\mu A$ per NVDFF during save or restore, and during active operation the VDDNV rail supplies current for only the dynamic switching of the internal slave latch nodes. Post-layout simulation of the entire FIR and measurement validate the electrical integrity of the VDDNV rail.

The complete implementation of the nonvolatile FIR filter is shown in Fig. 11. The NVDFFs are placed and routed among the logic gates. Also, the PMU containing only volatile DFFs is separately constructed so that its connections to the FIR filter can be bypassed for testability. Table V estimates the overhead from replacing every volatile DFF with an NVDFF. Based on the fact that the NVDFF consumes 2.7x the area of a volatile DFF and the relative area of sequential elements versus logic gates, the current approach incurs a 49% area overhead in the FIR filter in exchange for nonvolatile processing capability. The significant area overhead motivates selective DFF replacement as employed with MTCMOS retention registers [11,12]. Also, more NVDFF library cell types can help reduce the area. The additional NVDFF types can share a common set of transistors to drive the nodes PBIAS and SN, while careful custom design can potentially eliminate the EQ signal and its associated transistors.

IV. NVDFF ENERGY AND SIGNAL MARGIN MEASUREMENT

Fig. 12 shows the die micrograph of the test chip. In addition to the nonvolatile FIR filter with PMU, the chip also contains a bank of 4096 NVDFFs arranged into 8 shift registers of 512 bits. The measurement of the nonvolatile FIR filter will demonstrate the timing of the save and restore operation, and the NVDFF shift register permits gathering the statistical signal margin

of the proposed technique. Both structures reveal the breakdown of the energy cost of saving and restoring state.

The waveform set in Fig. 13(a) shows the measured output of the test-chip during a power interruption during which all chip power supplies are actively driven to ground. The signals VBAT_OK, CLK, and the 1.5 V chip supply are emulated by a pattern generator during chip testing. After the power interruption, the FIR filter resumes operation with the correct state. The waveform set in Fig. 13(b) zooms in on the power-loss event. Prior to power loss, the FIR values are consistent with the relation in Eq. (1), the provided inputs, and the programmed coefficients (w_1, w_2, w_3) equal to $(87, -77, -98)$. Namely, the application of a periodic input sequence $\{120, -2, 90, -75, 60, 45, -111, 72, \ldots\}$ produces the expected output sequence $\{-13259, 2175, 6645, -19002, 10401, 15774, -16470, -3776, \ldots\}$. The fall of VBAT_OK indicates power loss, and this event passes through a two-register synchronizer before the PMU freezes the FIR filter—in this case, to the output value -3776—and then continues the save operation by internally generating the PG, LD, and EQ signals. In the eighth cycle after the fall of VBAT_OK, the save completes and the rise of EQ sets all outputs of the FIR filter to "1" (the NVLATCH node is buffered with an inverter). The PMU waits another 2 cycles to let the internal VDDNV rail completely discharge as in the timing diagram of Fig. 8. Then, it is safe to cut off all power to the chip. The waveform set in Fig. 13(c) zooms in on the power-restoration. In the sixth cycle after VBAT_OK rises, the correct data (-3776) has been restored to the FIR filter. In the tenth cycle after VBAT_OK rises, the FIR filter resumes computation with the previously programmed coefficients. Even in the toy example of the FIR filter, the parallel save and restore of the NVDFF takes only 10 cycles to resume; whereas, a volatile implementation would have required 24 cycles to reprogram the three filter coefficients.

The round trip energy cost of save and restore is measured by issuing repeated save and restore commands at the highest possible frequency (Fig. 14), which turns out to be $208kHz$. Under these conditions, the FIR filter computes for six cycles and captures six new input samples between power interruption. The average current into the chip (FIR, PMU, SR latches) is measured and the current drawn by the VDDNV rail is separately recorded. A similar power cycling pattern is applied to the NVDFF shift register and the average currents associated with the control signals and VDDNV terminal are separately measured. The average current times the power supply voltage (1.5 V) divided by the save-restore repetition period and divided once more by

the number of NVDFFs produces the round-trip energy per NVDFF values in Table VI.

As a result, the contributions from fecap switching, the NVDFF interface, and FIR glitches plus toggling plus PMU overhead can be determined. The pie chart in Fig. 15 describes this breakdown of the round-trip save and restore energy for the NVDFF. By measuring the energy in both the context of a shift register (no logic and little interconnect) and the context of an FIR filter, the additional energy cost from nodes glitching in the FIR filter, cycle overheads, and PMU energy can be quantified to 1.780 pJ out of 3.439 pJ. Interestingly, slightly more than half the energy is associated with the CMOS circuits, which is largely independent of choosing the ferroelectric capacitor as the nonvolatile memory technology. The measurements of energy, save time, restore time, and on-off cycling rate are summarized in Table VII and compared to related work [7]. The improvements in this work's energy per save/restore operation can come from a difference in fecap size and circuit topology. Also, the proposed NVDFF has no direct current paths from power supply to ground; whereas, [7] precharges the slave latch into a metastable state that can produce significant short circuit current through the cross-coupled inverter pair. The improved save/restore timing is suspected to come from (1) the larger voltage bias applied to the ferroelectric capacitors while sensing in the NVDFF and (2) the larger sensing time constant on the latch nodes in [7] because of loading by the fecaps.

Finally, the statistical signal margin is measured. The FIR filter has 96 NVDFFs and about 500 gates. For a target application of a microcontroller, approximately 5,000 DFFs need to be retained. The plot in Fig. 17 shows the number of failures induced in the eight shift registers of 512 NVDFFs (4096 total per chip) when a skew is applied. The test pattern first writes and saves $(0, 1, 0, 1, \ldots)$, then writes and saves the opposite data $(1, 0, 1, 0, \ldots)$, then restores the state under a given skew, and finally reads out the shift register to compare with previously written data. The NVDFF has a split supply rail (Fig. 16), so the sensing current ramps can be perturbed from their nominally identical values. In simulation, the relationship between the skew on VDDNVT/VDDNVC and percentage skew in current ramp rate is roughly linear:

$$\frac{I_T - I_C}{I_T} \propto V_{\mathrm{DDNVT}} - V_{\mathrm{DDNVC}}.$$

Furthermore, the voltage signal, defined as the voltage difference between nodes FET and FEC,

is approximated by:

$$V_{\text{sig}} \approx V_{\text{trip}} \left(\frac{I_T - I_C}{I_T} \right) + \frac{Q_r}{C_{\text{lin}}}.$$

The above relation comes from modeling transistors M1 and M2 in the NVLATCH of Fig. 6 as current sources and the slave latch trip point as an ideal detector of when FET or FEC first charge up to V_{trip}. The remnant charge, Q_r, is the charge signal stored in the fecap hysteresis—the vertical distance between the two remnant points on the charge versus voltage hysteresis under zero bias in Fig. 3. C_{lin} is dominated by the non-hysteretic component of the ferroelectric capacitor which determines how much voltage can be generated by a given amount of remnant charge.

In measurement, the reduction of skew between VDDNVT and VDDNVC results in a Gaussian-like quadratic decrease of the failure rate on a logarithmic vertical scale in Fig. 17. From zero skew up to VDDNVT=1.2 V, all NVDFFs in all five measured chips (about 21,000 NVDFFs total) operate without failure. A wide distribution of failure versus skew relative to the horizontal separation of the failure curves of individual chips shows that within die variation is dominant, though non-negligible die to die variation exists. Because several hundred millivolts of skew between VDDNVT and VDDNVC translates to several hundred millivolts of skew between the internal nodes FET and FEC, the transistor mismatch is also negligible compared to fecap signal variation. Conservative extrapolation of the failure distributions (individual chips and total) as a straight line on a logarithmic scale suggests that an unskewed NVDFF will meet the 10 ppm requirement for a microcontroller application.

In a production setting, skewing VDDNVT and VDDNVC can screen out marginal chips. In a digital circuit block with arbitrary DFF placement, a conventional scan chain (data multiplexer or clock multiplexer-based) can initialize the master stage with the test data during the active phase. A subsequent save operation would write the test data to the fecaps, after which the restore operation can take place with a desired skew to check if the correct data appears despite the signal stress.

V. Conclusion

A nonvolatile D flip-flop based on ferroelectric capacitors has been developed with regards to the key challenges of system integration. It enables an arbitrary digital circuit to save state

in $2.2\mu s$ and reboot in $2\mu s$. A microcontroller having a few thousand NVDFFs that cost 3.44 pJ per bit will be able to power its state management from the decoupling capacitance already available on its power pin. These scales of time and energy are comparable to the scales of time and energy during regular computation, and therefore energy processing and computation can happen in parallel. Finally, the energy breakdown of the round-trip save and restore operation has revealed that artifacts of the CMOS circuitry can limit further reduction in the energy cost of managing state, independently of improvements in the nonvolatile technology.

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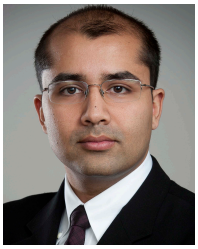

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He was a co-recipient of several awards including the 1993 IEEE Communications Society's Best Tutorial Paper Award, the IEEE Electron Devices Society's 1997 Paul Rappaport Award for the Best Paper in an EDS publication during 1997, the 1999 DAC Design Contest Award, the 2004 DAC/ISSCC Student Design Contest Award, the 2007 ISSCC Beatrice Winner Award for Editorial Excellence and the ISSCC Jack Kilby Award for Outstanding Student Paper (2007, 2008, 2009). He received the 2009 Semiconductor Industry Association (SIA) University Researcher Award. He is the recipient of the 2013 IEEE Donald O. Pederson Award in Solid-State Circuits.

His research interests include micro-power digital and mixed-signal integrated circuit design, wireless microsensor system design, portable multimedia devices, energy efficient radios and emerging technologies. He is a co-author of Low Power Digital CMOS Design (Kluwer Academic Publishers, 1995), Digital Integrated Circuits (Pearson Prentice-Hall, 2003, 2nd edition), and Sub-threshold Design for Ultra-Low Power Systems (Springer 2006). He is also a co-editor of Low Power CMOS Design (IEEE Press, 1998), Design of High-Performance Microprocessor Circuits (IEEE Press, 2000), and Leakage in Nanometer CMOS Technologies (Springer, 2005).

He has served as a technical program co-chair for the 1997 International Symposium on Low Power Electronics and Design (ISLPED), VLSI Design '98, and the 1998 IEEE Workshop on Signal Processing Systems. He was the Signal Processing Sub-committee Chair for ISSCC 1999-2001, the Program Vice-Chair for ISSCC 2002, the Program Chair for ISSCC 2003, the Technology Directions Sub-committee Chair for ISSCC 2004-2009, and the Conference Chair for ISSCC 2010-2012. He is the Conference Chair for ISSCC 2013. He was an Associate Editor for the IEEE Journal of Solid-State Circuits from 1998 to 2001. He served on SSCS AdCom from 2000 to 2007 and he was the meetings committee chair from 2004 to 2007. He was the Director of the MIT Microsystems Technology Laboratories from 2006 to 2011. Since July 2011, he is the Head of the MIT EECS Department.

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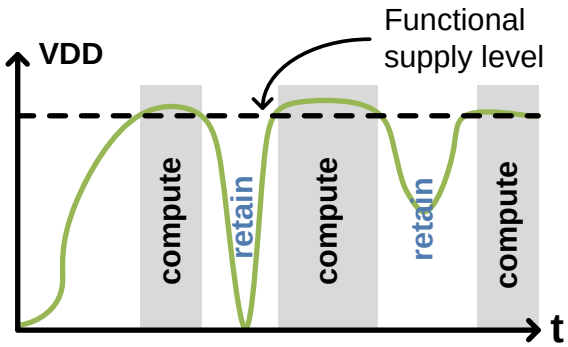


Fig. 1. A cartoon illustrating the desired operation of nonvolatile processing: the system performs useful computation in between unpredictable interruptions in the availability of harvested energy

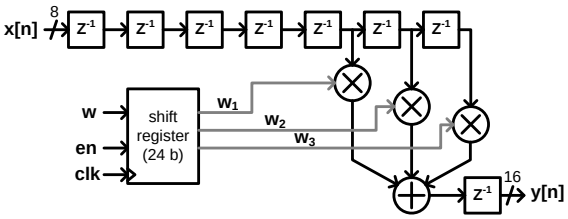


Fig. 2. The test case digital circuit in this work is a 3-tap FIR filter with configurable coefficients and a four-cycle input buffer. All 96 registers in this circuit will contain nonvolatile ferroelectric memory elements.

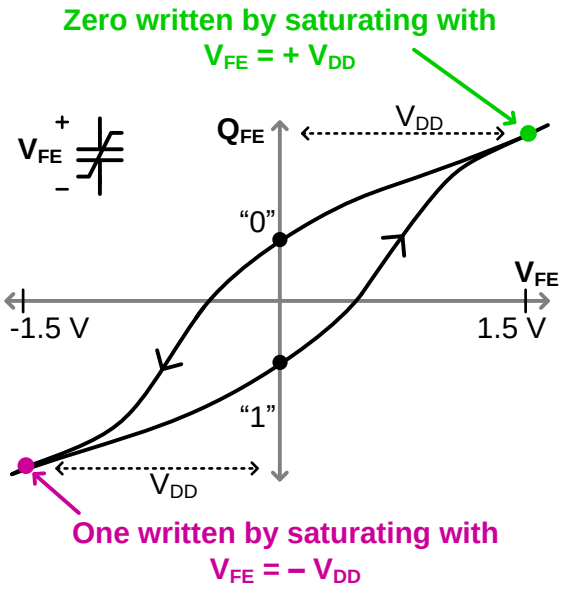


Fig. 3. Charge versus voltage hysteresis of the ferroelectric capacitor

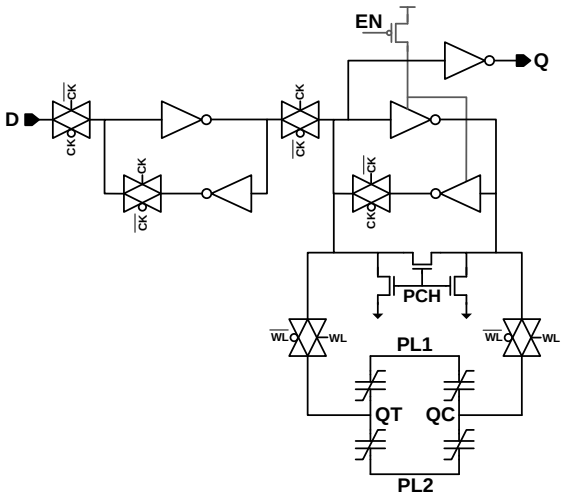
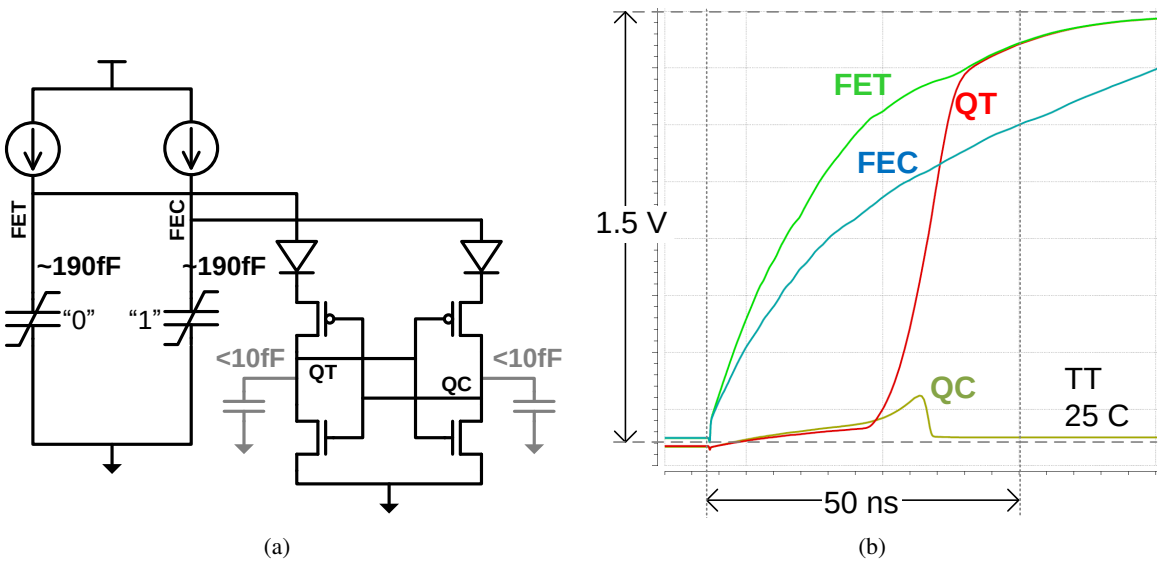


Fig. 4. The conventional approach to a nonvolatile DFF contains a differential pair of ferroelectric capacitor dividers.



(a) (b)

Fig. 5. Shown is (a) a simplified schematic of the nonvolatile latch during restore and (b) the associated waveforms from post-layout simulation

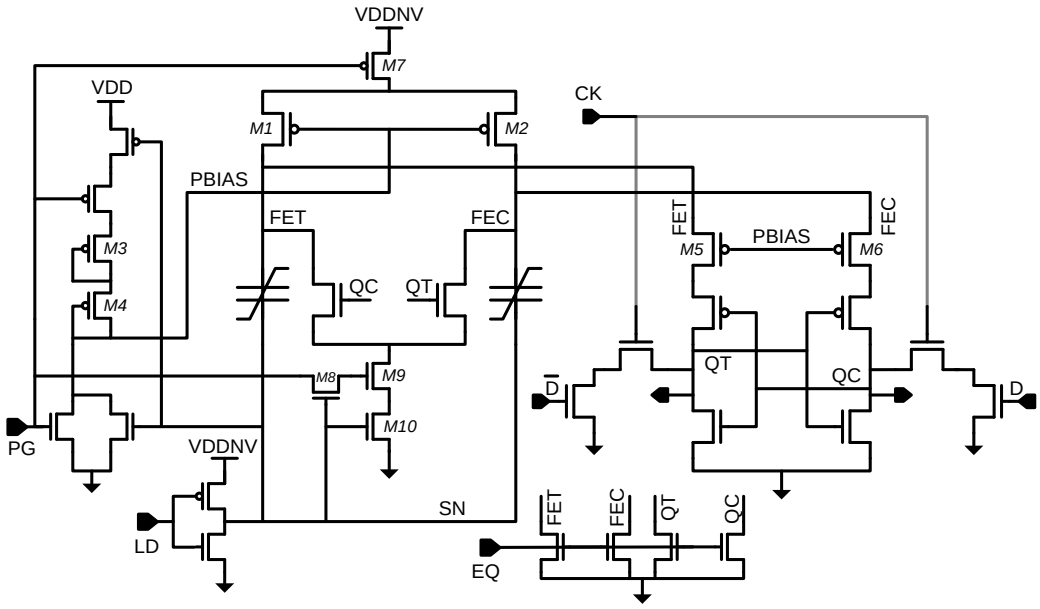


Fig. 6. Full transistor schematic of the NVLATCH

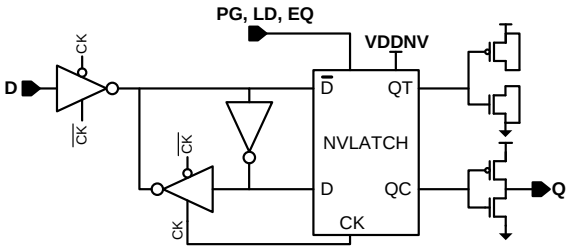


Fig. 7. The NVDFF is constructed by placing the NVLATCH in the slave stage

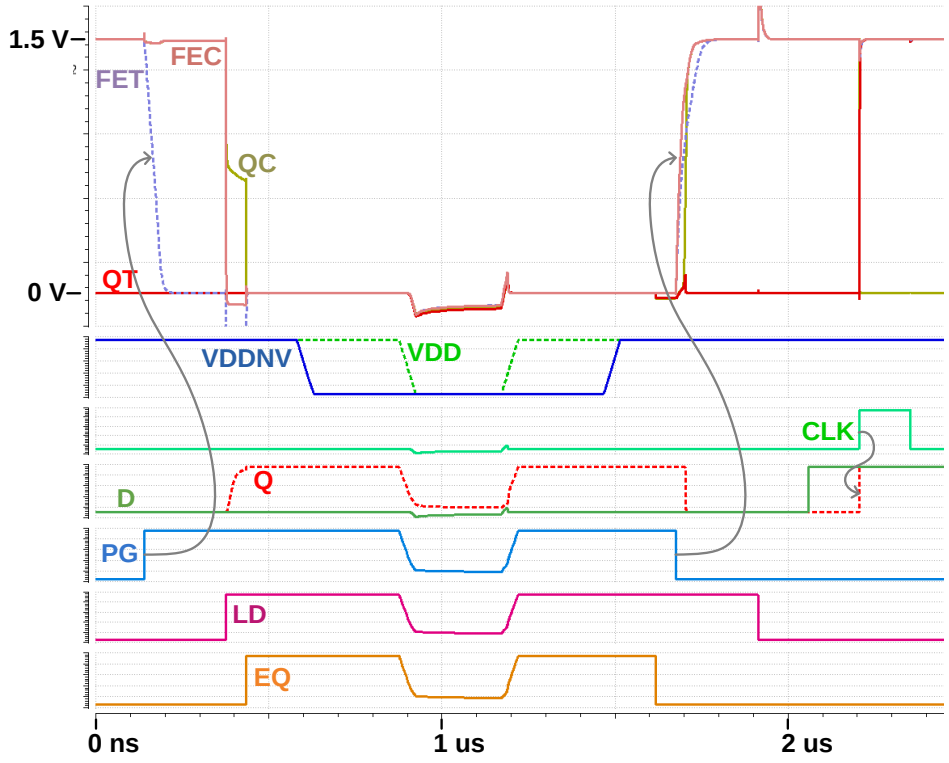


Fig. 8. Timing diagram for the NVLATCH control

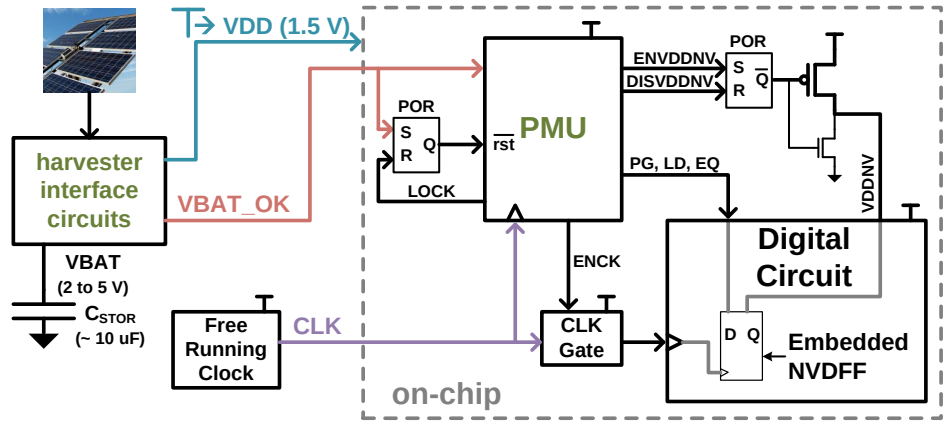


Fig. 9. System-level nonvolatile state management with energy harvesting circuits from [10]

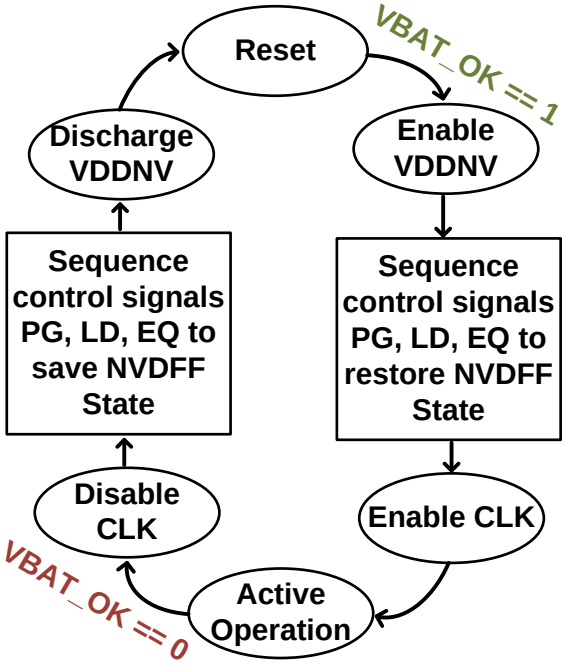


Fig. 10. Power management unit FSM designed to operate with a single flag (VBAT_OK) from the energy processing circuits in [10]

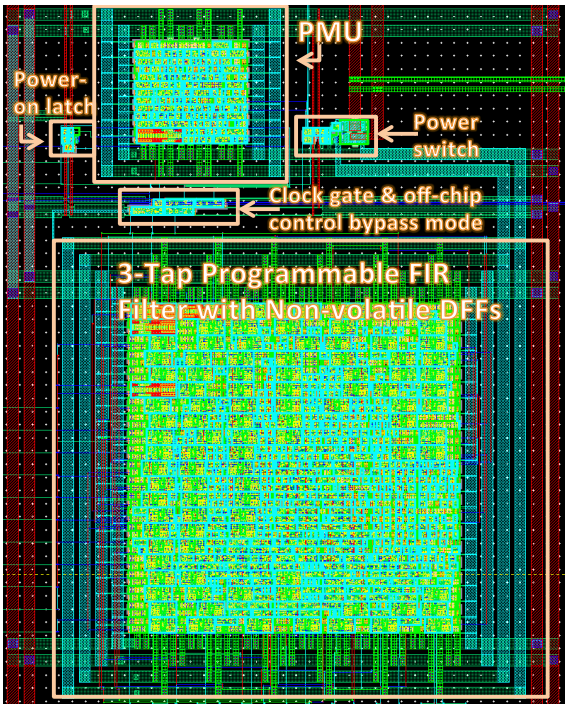


Fig. 11. Physical implementation of the test case FIR with embedded NVDFFs

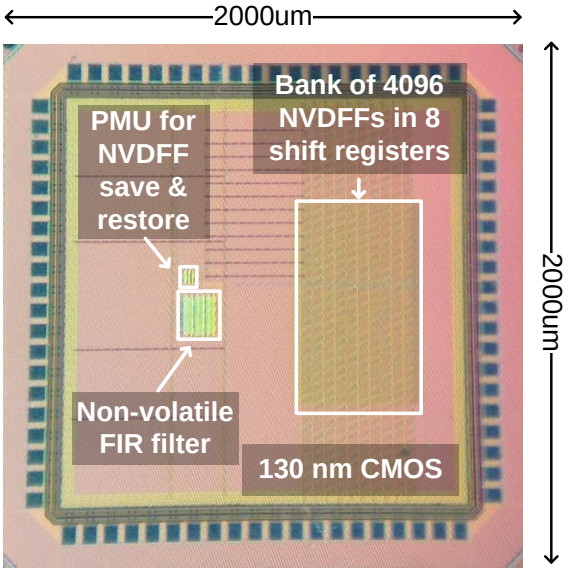


Fig. 12. Micrograph of the die containing the nonvolatile FIR and a 4096 NVDFF shift register test structure

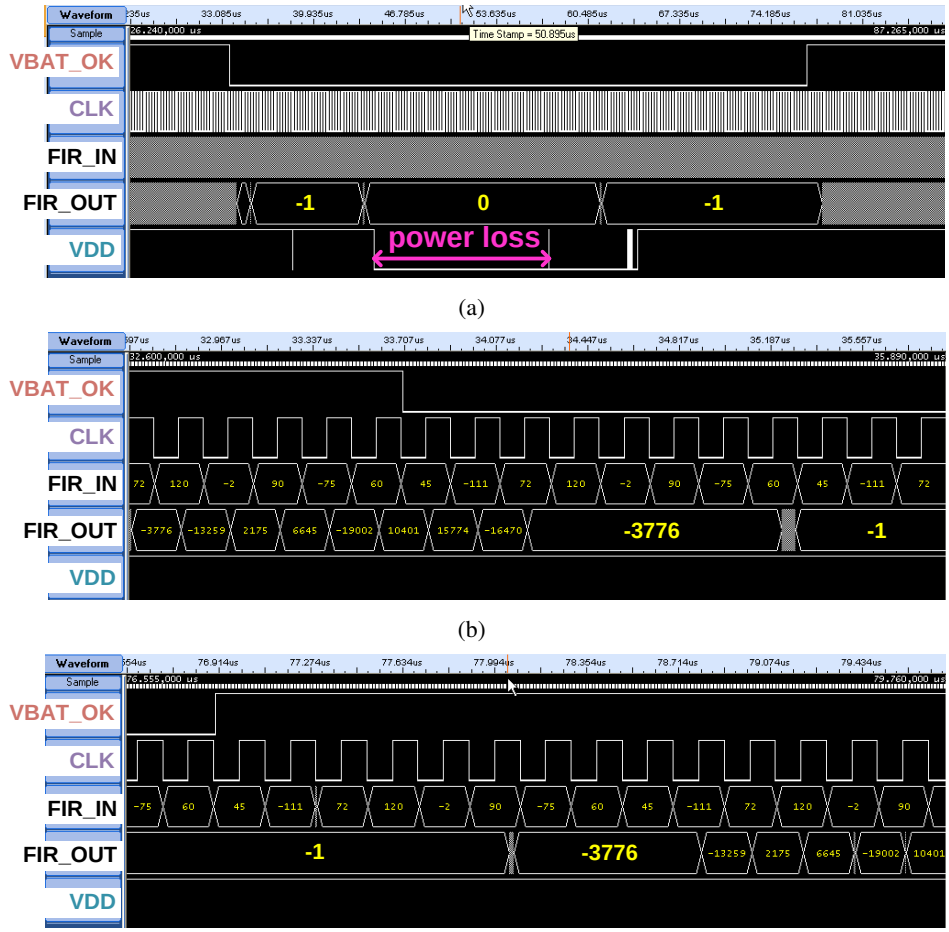


Fig. 13. Screenshot of measured logic analyzer waveforms of nonvolatile operation over the (a) full power interruption, (b) zoom-in of the save operation, and (c) zoom-in of the restore operation. A periodic input sequence $\{120, -2, 90, -75, 60, 45, -111, 72, \ldots\}$ is applied and the resulting output sequence is $\{-13259, 2175, 6645, -19002, 10401, 15774, -16470, -3776, \ldots\}$. Certain digital waveform values have been annotated for readability.

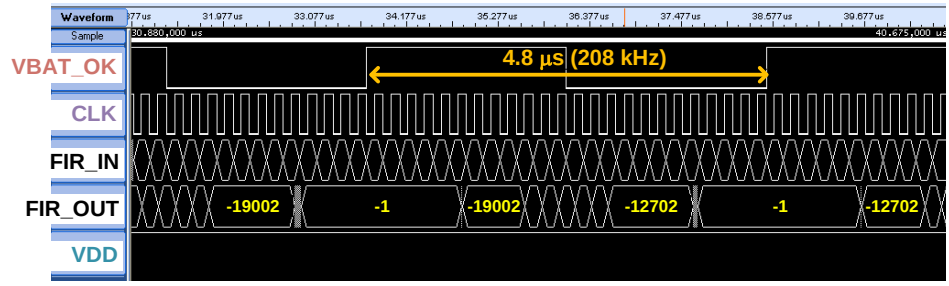


Fig. 14. Logic analyzer waveform during maximum on-off toggling rate during energy measurement, certain digital waveform values have been annotated for readability

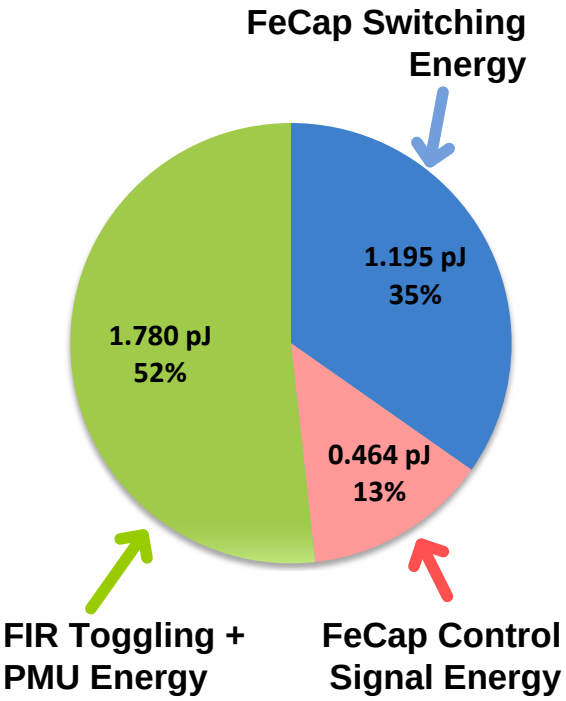


Fig. 15. Breakdown of the 3.44 pJ round-trip energy cost per NVDFF for save and restore

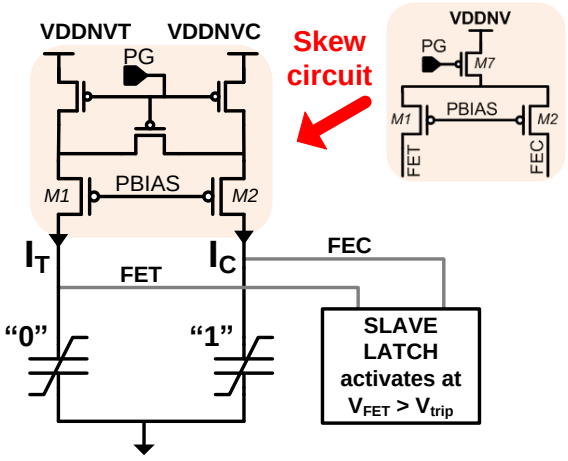


Fig. 16. Skewed PMOS header device for observing signal margin

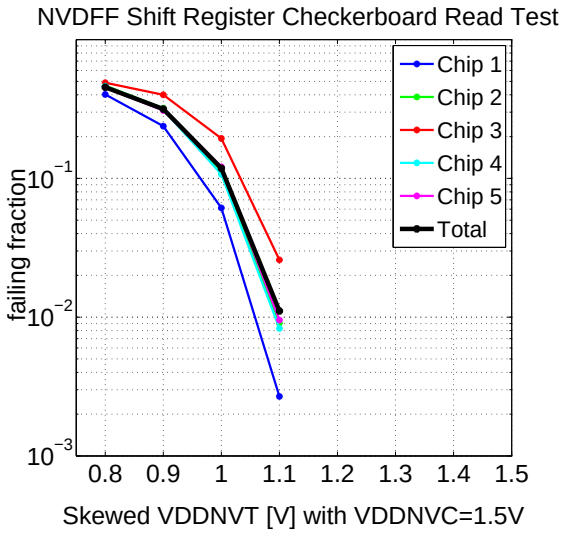


Fig. 17. Measurement of signal margin from NVDFF failure versus magnitude of skew (4096 NVDFFs per chip)

TABLE I
SUMMARY OF TECHNOLOGY PROPERTIES (REPORTED IN [13]–[15])

Technology	0.13 μm CMOS with embedded FeRAM
VDD	1.5 V
Ferroelectric Material	PZT
Dielectric Thickness	70 nm
Coercive Voltage	$\approx$ 0.5 V
Saturation Voltage	$\approx$ 1.5 V
Remnant Polarization	150 - 200 $fC/\mu m^2$

TABLE II
THE EIGHT CHALLENGES OF NVDFF SYSTEM INTEGRATION

1	Maximize voltage bias on FeCap during sensing
2	Prevent glitches on FeCap during brown-out
3	Apply zero bias on FeCap during active operation
4	Avoid race conditions and sensitive high impedance nodes during sensing
5	Limit peak current during save and restore
6	Avoid settling time for analog biases and references
7	Control state management with interface to system energy information
8	Develop a solution compatible with the ASIC design flow

TABLE III
THE FOUR MODES OF THE NVDFF DECODED BY PG & LD

PG	LD	Mode
1	1	Off
0	1	Restore
0	0	Active
1	0	Save

TABLE IV
SIMULATION-BASED COMPARISON WITH CONVENTIONAL APPROACH FOR NONVOLATILE LATCH OPERATION

	conventional	proposed
Restore energy (normalized)	0.16	0.38
Save energy (normalized)	0.84	0.20
Total energy (normalized)	1.00	0.58
Nominal differential signal (static model)	383 mV	309 mV
Voltage bias across switching capacitor	$0.59 \sim 0.62$ V	$1.10 \sim 1.30$ V

TABLE V
AREA OVERHEAD OF THE NVDFF

Total standard cell area of nonvolatile FIR	$11020\mu m^2$
Area of gates	$5194\mu m^2$
Area of NVDFFs	$5826\mu m^2$
Area of equivalent number of volatile DFFs	$2184\mu m^2$
Area of equivalent number of NVDFFs	$7378\mu m^2$
Overhead based on synthesis area report	49%

TABLE VI
PER-NVDFF ENERGY FOR FIR AND SHIFT REGISTER

Domain	Shift Reg.	FIR
VDDNV	1.09 pJ	1.20 pJ
VDD	0.46 pJ	2.24 pJ

TABLE VII
COMPARISON TO RELATED WORK

	[7]	This work
CMOS Technology	0.13 μm w/ FeRAM	0.13 μm w/ FeRAM
VDD	1.5 V	1.5 V
NVDFF area	—	$60.69\mu m^2$
Standard DFF area	—	$22.75\mu m^2$
NVDFF area overhead (from synthesis report)	—	49 %
Placed NVDFF save & restore energy	19.42 pJ/bit	3.44 pJ/bit
Save time	$7\mu s$	$2.2\mu s$
Restore time	$3\mu s$	$2\mu s$
Maximum reported on-off cycling rate	$20kHz$	$208kHz$