WIDE-BANDWIDTH DIGITAL CONTROLLER FOR MULTI-PHASE CONVERTERS

by

Lyne Petse Tchapmi

S.B. EECS, Massachusetts Institute of Technology, 2013

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of Master of Engineering in Electrical Engineering and Computer Science at the Massachusetts Institute of Technology

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Abstract

DC-DC converters with high bandwidth are essential for today's high efficiency and high-speed micro-processing applications. In order to satisfy the requirements of those systems, we propose the implementation of a practical wide bandwidth digital controller for multiphase buck converters. Traditional implementations of multiphase converters have a performance comparable to single-phase implementations, with a bandwidth limited to a fraction of the per-phase switching frequency F_{sw}. The goal of this project is to take advantage of multiphase to achieve a higher bandwidth for any given switching frequency. Specifically, we target a bandwidth that scales with $N \times F_{sw}$, rather than F_{sw}, with N being the number of phases in the system.
This work focuses on the evaluation of a previously proposed digital modulator that is able to react to duty cycle changes at a speed equal to $N \times F_{sw}$. Using this modulator, we design a few digital controllers and compare their performance to that of traditional digital controllers.

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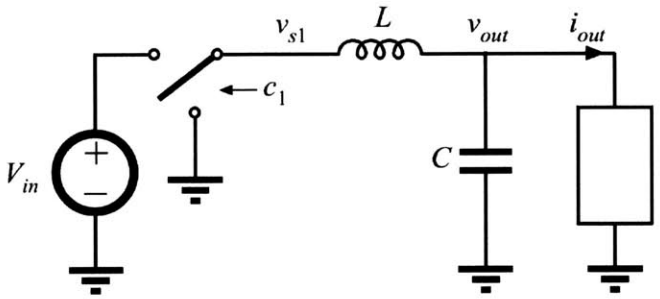
Chapter 1 Introduction and Background

1.1 The need for high bandwidth DC-DC converters for microprocessors

The need for higher processing speed in microprocessors calls for power converters that can keep up with fast varying loads. Through dynamic voltage scaling (DVS), the power consumption of modern processors is reduced by adjusting the supply voltage in real time [4]. This technique puts a requirement on the power converter supplying the processor to have a wide output voltage range and a fast reference-tracking response, while maintaining high efficiency. DC-DC converters with high bandwidth are therefore essential for today's high-speed micro-processing applications.

Synchronous buck converters are good candidates for such applications. A single-phase buck converter is shown in Figure 1.



Adapted from Maksimovic, PESC 2006

Figure 1: Single phase buck converter

In micro-processing applications using this type of converter, a controller is used to regulate the output voltage V_{out} to a reference voltage V_{ref}. When DVS is used, V_{ref} varies

depending on the processor's requirements, and the output voltage has to track the varying V_{ref} with high speed and accuracy [5]. The load current requirement of microprocessors also varies with operating conditions. This translates to a varying load current i_{out}. For large and fast i_{out} steps, the limited slew rate of the converter due to the magnitude of the inductance causes the load current to be sourced initially from the output capacitor C to the load. The resulting discharge of the output capacitor, and its non-zero ESR cause a voltage droop at the output.

Such voltage droop can significantly compromise the operation of the microprocessor [3]. In practical implementations, the output voltage droop is minimized by choosing a very large output capacitor with low-ESR. But the size requirement of the output capacitor can be significantly reduced with a fast controller that can quickly detect the output voltage droop and counteract it by increasing the inductor current. The speed of the controller is therefore essential for both the performance and the size of the power converter [6]. Typical DC-DC power converters address these challenges using PWM voltage- or current-mode controllers, and techniques such as interleaving in multiphase converters. But these techniques have limitations that can be improved upon.

1.2 Performance of typical DC-DC buck converters

In the operation of a traditional single phase buck converter, as shown in Figure 1, a single inductor is used to provide current to a load. The inductor therefore has to be rated for a current comparable to the maximum load current, and the higher the current, the larger the inductor. Going from a single phase to a multiphase converter allows reducing the current requirements on the inductors. In an N-phase converter (Figure 2), the load

current is shared amongst N inductors, allowing for the use of smaller inductors. Interleaving also presents an advantage for multiphase converters.

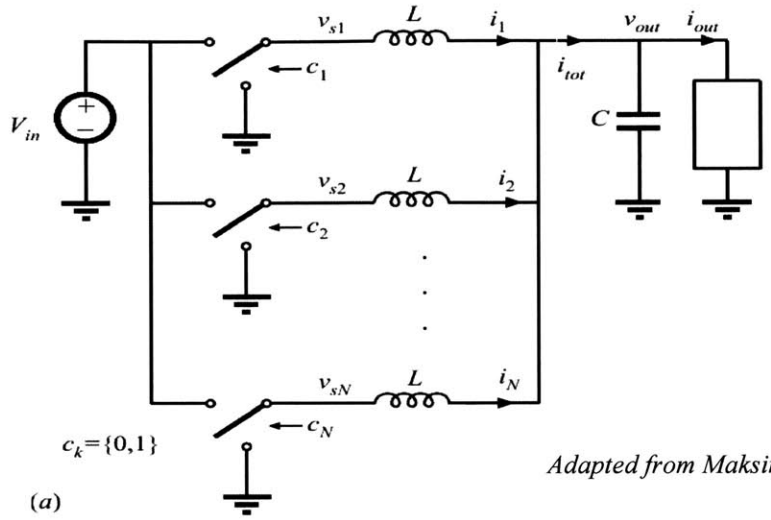
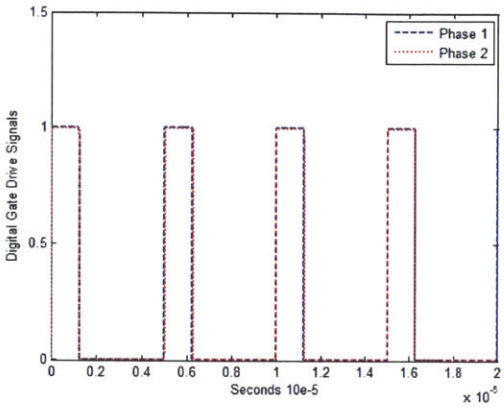


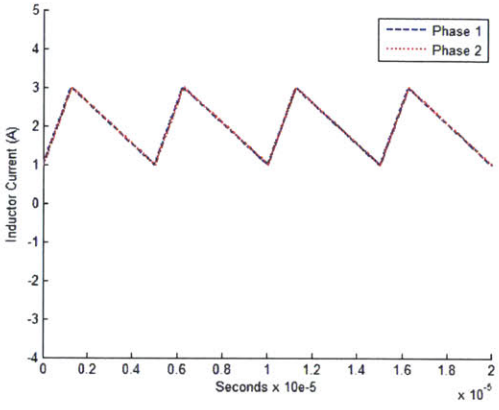
Figure 2: Multiphase Buck Converter

1.2.1 Interleaved multiphase converters

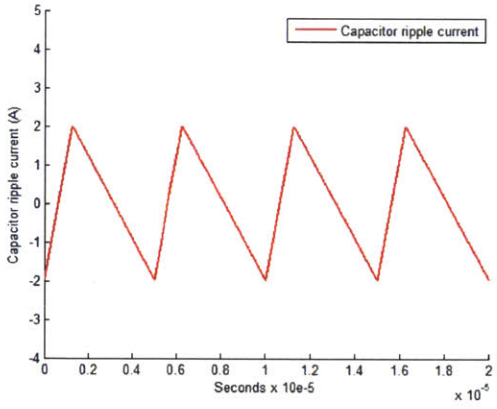
Interleaving in multiphase converters opens the possibility for further reduction in energy storage. The operation of a non-interleaved 2-phase buck converter is shown in Figure 3. Figure 3a shows the digital gate drive signals for each phase. The phase currents are shown in Figure 3b, and the resulting output capacitor current ripple is shown in Figure 3c. During operation, the gate drive signals are identical for both phases, and the ripple currents per-phase, ΔI_{phase}, add up at the output, resulting in an output ripple $\Delta I_{out} = N \times \Delta I_{phase} = 2 \times \Delta I_{phase}$.



a)Digital gate drive signals



b)Phase inductor currents

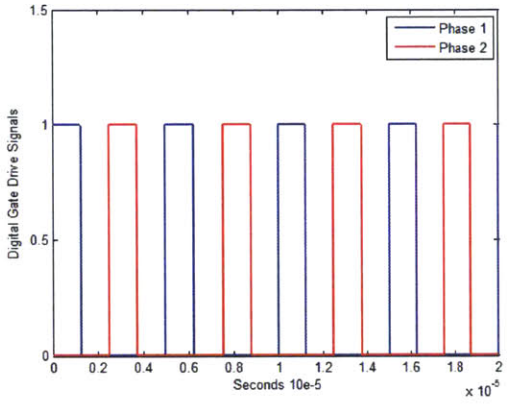


c) Output Capacitor ripple current

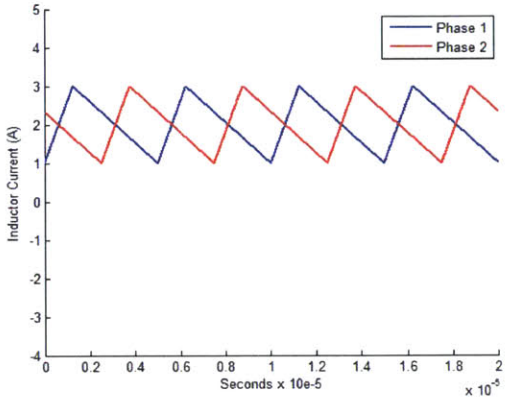
Figure 3: Operation of a non-interleaved 2-phase buck converter

In contrast, the operation of an interleaved 2-phase buck converter is shown in Figure 4. The gate drive signals, phase currents and output capacitor current ripple are also depicted. The gate drive signals and phase currents in this case are phase shifted by $\frac{360°}{N}$ = $\frac{360°}{2}$ = 180° relative to the next phase. This relative phase shift results in ripple cancellation at the output of the converter. The amount of ripple cancellation varies with duty cycle but

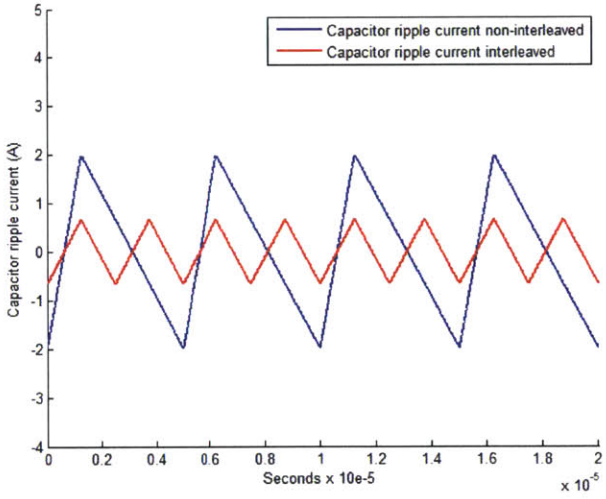
the resulting output capacitor current ripple is always less than or equal to the per-phase current ripple ($\Delta I_{out} \leq \Delta I_{phase}$). The ripple is therefore reduced at least by a factor of N with interleaving. The current capacitor current ripple for the non-interleaved converter above is also reproduced in Figure 4c for comparison.



a)Digital gate drive signals



b)Phase inductor currents



c) Output Capacitor ripple current

Figure 4: Operation of an interleaved 2-phase buck converter

This ripple reduction translates into opportunities for size reduction in power converters through reduction of the magnitude of inductance and capacitance in the converter. For a given current ripple per phase ΔI_{phase}, the minimum inductor value required is given to first order by,

$$L_{min} = Vin \times \frac{D}{F_{sw} \times \Delta I_{phase}} \quad (1)$$

With,

D = duty cycle

F_{sw} = per-phase switching frequency

V_{in} = input voltage

Given that the output ripple current ΔI_{out} is at least N times smaller with interleaving, for a given ΔI_{out}, ΔI_{phase} can be set to a value that is N times larger in an interleaved converter as compared to a non-interleaved converter. According to Equation (1), the inductor can therefore be N times smaller in the interleaved converter.

Similarly, the ripple-limited capacitance requirement for a buck converter is given to first order by

$$C_{min/phase} = \frac{\Delta I_{out} \times D \times T_{sw}}{\Delta V_{out}} \quad (2)$$

With,

$T_{sw} = \frac{1}{F_{sw}}$ = Switching period

ΔV_{out} = Output voltage ripple

Given that the output ripple current ΔI_{out} is at least N times smaller with interleaving, for a given ΔI_{phase}, ΔI_{out} is at least N times smaller in an interleaved converter as compared to a

non-interleaved converter. Keeping the same ΔV_{out}, according to Equation (2), but noting that for interleaved converters the capacitor ripple frequency is N*Fsw, the output capacitor can therefore be N times smaller in the interleaved converter.

In summary, interleaving offers the opportunity to decrease energy storage in buck converters, through a reduction of the inductor and capacitor sizes by a factor greater than or equal to N. Multiphase converters as a result can have lower per-phase inductance which allows for higher slew rates and opens the possibility of faster transient responses. Traditional controller designs for multiphase interleaved buck converters are often based of single phase PWM controller designs that are applied to the multiple phases of the converter. But these controllers do not take advantage of the higher slew-rate potential of multiphase converters that could allow achieving fast load transient response and superior reference tracking performance. As a result, the performance of multiphase converters in terms of bandwidth is often comparable to that of single phase converters operating at the same per-phase switching frequency, due to the limitations of traditional PWM controllers.

1.2.2 Traditional PWM controllers

Common control techniques for buck converters use voltage-mode control and current-mode control PWM-based controllers. For a single phase converter, these controllers are able to achieve bandwidths that are a fraction of the switching frequency F_{sw}. In multiphase buck converters, industry-standard PWM controllers have a similar performance resulting in a bandwidth to switching frequency ratio $\frac{BW}{F_{sw}}$ similar to that of single phase converters. This similarity suggests that common PWM controllers do not

take full advantage of the potential of multiphase converters which is their comparatively higher slew rates.

A limitation of common PWM-based controllers is the fact that the duty cycle command sent from the controller to the power stage is only updated at the end of a switching cycle. As an illustration of this issue, Figure 5 shows the diagram of an average-current mode control (ACMC) scheme for a buck converter.

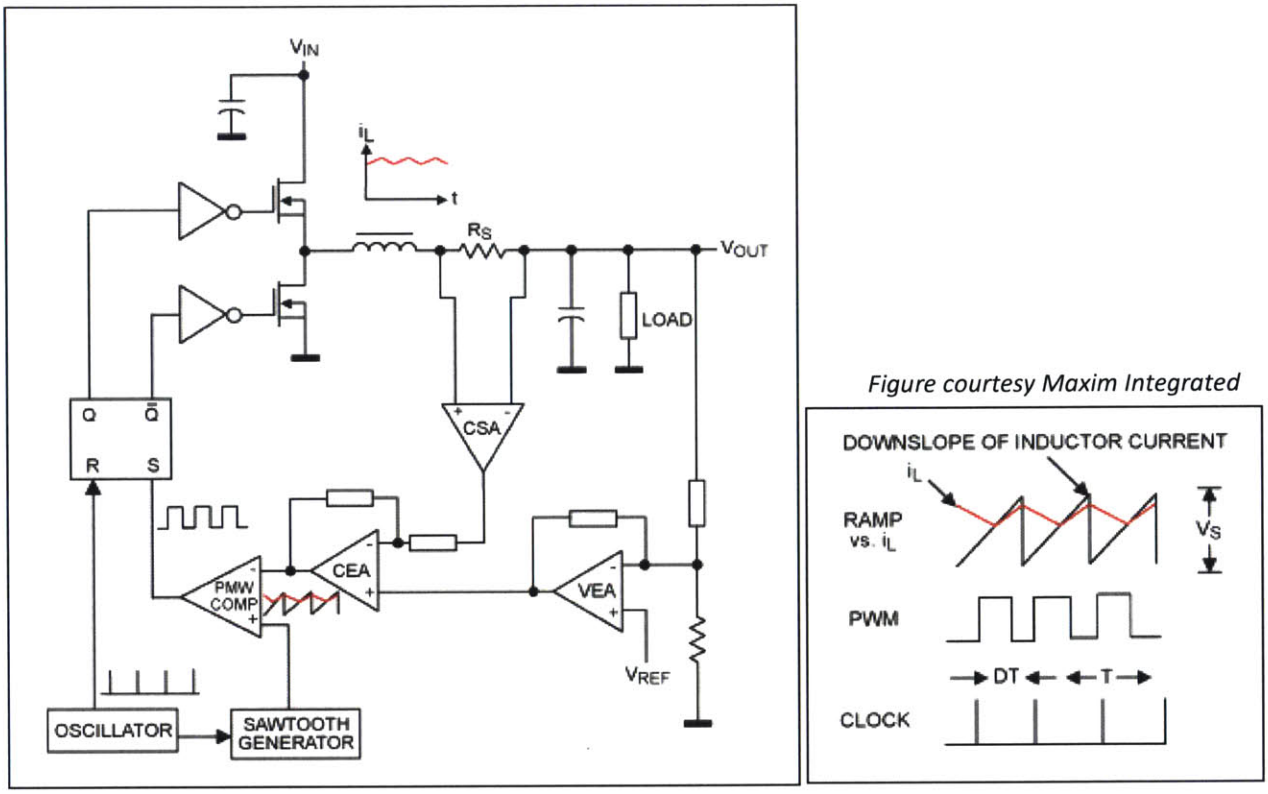


Figure courtesy Maxim Integrated

Figure 5: a) Functional block diagram of a buck converter operated in ACMC, b) Control waveforms for a.

In this control scheme, the oscillator resets the SR latch driving the FETs of the power stage and determines the frequency of the PWM signal. Together, the oscillator and the PWM signal determine the update frequency of the duty cycle which is equal to the switching

frequency F_{sw} in this case. A limitation of this technique becomes obvious when a voltage reference step happens soon after the edge of the oscillator signal. In such scenario, the controller has to wait until the end of the switching period before it is able to react to the disturbance. This mandatory delay limits the speed of the transient response of the system. In an ACMC controller implementation, increasing the bandwidth and thus the speed of the converter would require increasing the switching frequency F_{sw}, which would increase switching losses in the power stage and consequently reduce efficiency. To address this tradeoff and reduce the mandatory delays in PWM controllers, we implement a digital multiphase modulator with the ability to update duty cycle commands at a rate higher than the switching frequency F_{sw}, specifically at a rate of $N \times F_{sw}$. An illustration of this concept is shown in Figure 6 where the gate drive signals for a 4-phase converter are shown during a 25% to 75% duty cycle transition. Figure 6 shows the gate drive signals in a controller with a modulator that updates the duty cycle at a rate of $N \times F_{sw}$ while maintaining the same switching frequency F_{sw} Such a controller updates the duty cycle at a higher rate but does not require changing the per-phase switching frequency of the converter and therefore maintains the same efficiency. Using this fast modulator, we take advantage of the high slew rates in multiphase converters to achieve a bandwidth that scales with $N \times F_{sw}$.

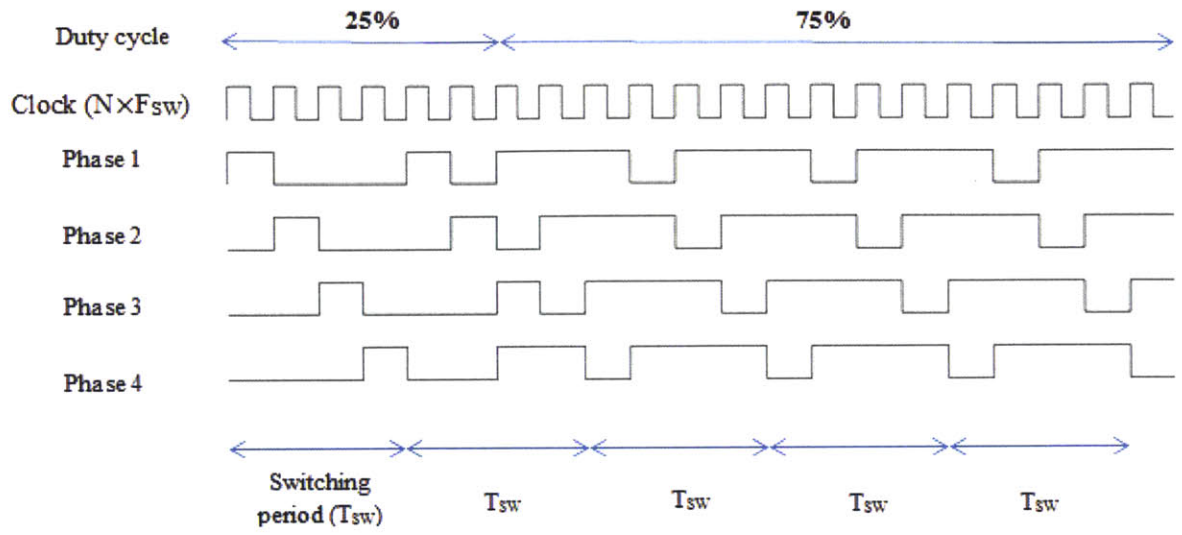


Figure 6: Gate drive signal for a 4-phase converter where the duty cycle is updated at a rate of $N \times F_{sw}$

1.3 Proposed analysis

The work presented is an analysis of the speed and performance improvement in systems that use a previously proposed fast modulator [1], with the ability to update the duty cycle at a rate of $N \times F_{sw}$ without changing the switching frequency. The performance of such systems is compared against the performance of systems that use traditional PWM modulators. Three types of compensator are used to compare the two systems. For each compensator type, an assessment of the performance improvement is made using metrics such as rise time, settling time, and output voltage droop. This analysis, presented in Chapter 3, reveals that the advantages of the fast modulator are indeed present and vary according to the type of compensator used.

Chapter 2 Controller system description

The multiphase controller solution described is based on a digital modulator that computes and updates duty cycle commands at a rate of N× F_{SW}. This modulator, initially described in [1] is implemented and modified for better phase current balance.

2.1 System model

The design of our system starts with the power D/A model of a multiphase converter presented in [1] and [2]. In this model, an N-phase converter, shown in Figure 7, is controlled by a modulator which sends duty cycle commands c_k to phase k of the converter, where $c_k = \{0, 1\}$.

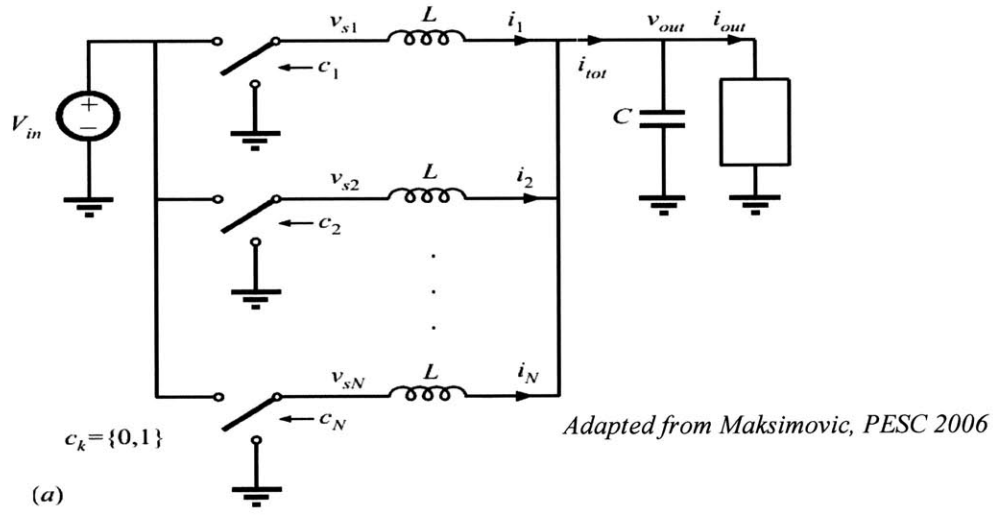


Figure 7: N-phase buck converter

When $c_k = 1$, the input to phase k is Vin, and when $c_k = 0$, the input is 0V. So at all times, the input to phase k is c_kVin. If we let i_{Lk} be the current through the k_{th} inductor and V_{Lk} the voltage across the same inductor, then

$$i_{Lk(s)} = \frac{V_{Lk(s)}}{sL} = \frac{c_k(s)V_{in} - V_{out}(s)}{sL} \qquad (3)$$

Summing all phase currents, we get:

$$i_{tot}(s) = {}_1^N\Sigma i_{Lk}(s) = \frac{({}_1^N\Sigma c_k(s))V_{in} - ({}_1^N\Sigma V_{out}(s))}{sL} = \frac{({}_1^N\Sigma c_k(s))V_{in} - NV_{out}(s)}{sL}$$

$$i_{tot} = \frac{\frac{({}_1^N\Sigma c_k(s))}{N}V_{in} - V_{out}(s)}{s\frac{L}{N}} \qquad (4)$$

Drawing an analogy between (3) and (4), the N-phase converter behaves as a single phase converter with duty cycle command equal to $\frac{({}_1^N\Sigma c_k)}{N}$ = d_c (and thus input equal to $\frac{({}_1^N\Sigma c_k)}{N}V_{in} = d_c Vin$), and inductance equal to $\frac{L}{N}$. From these observations we derive the power D/A model shown in Figure 8.

Adapted from Maksimovic, PESC 2006

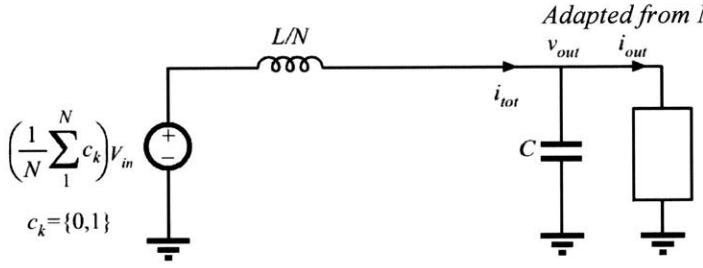
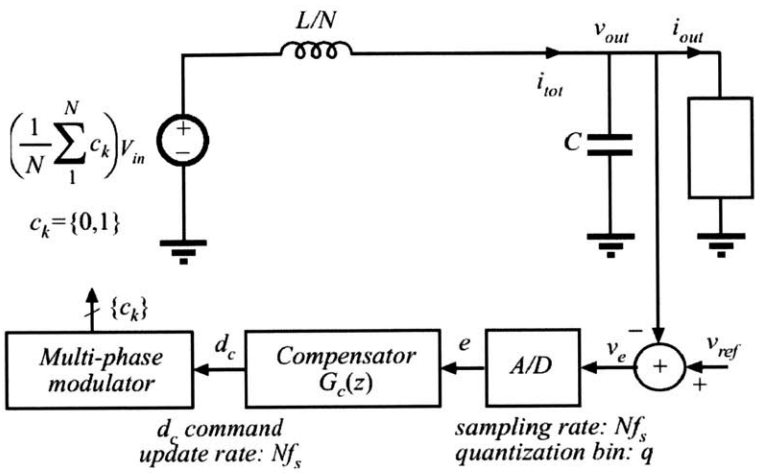


Figure 8: Power D/A model of N-phase buck converter

From this model, we design a control loop for the converter's power stage using an A/D, a digital compensator followed by the digital modulator above mentioned (Figure 9). The A/D samples the difference between the reference voltage and the output voltage and outputs a digital value for the error e[n] at a rate of N × Fs. The compensator uses the digital error e[n] to produce a duty-cycle command d_c[n] also at a rate equal to N × Fs. The duty-cycle command is then used by the modulator to produce the gate drive signals for the different phases of the converter.



Adapted from Maksimovic, PESC 2006

Figure 9: System block diagram of the wide-bandwidth digital controller

2.2 The advanced digital modulator

2.2.1 Modulator architecture and operation

2.2.1.1 Previous modulator design

The digital modulator we implement in our design takes in a duty cycle command from a compensator output and generates the gate drive signals for all N phases of the converter. The modulator design we use is based on the modulator architecture presented in [1]. This architecture is targeted towards digital controllers and solves the issue of slow duty cycle update that traditional PWM-controllers have.

The input to this modulator is an n-bit duty cycle command that is split into n_{MSB} low resolution most significant bits (MSB) and n_{LSB} high resolution least significant bits (LSB) with $n = n_{MSB} + n_{LSB}$. As was done by [1], we choose the partition such that $N = 2^{n_{MSB}}$, and

there are N distinct MSB commands, which correspond to having 0 to N-1 phases on. The architecture of this modulator is presented in Figure 10.

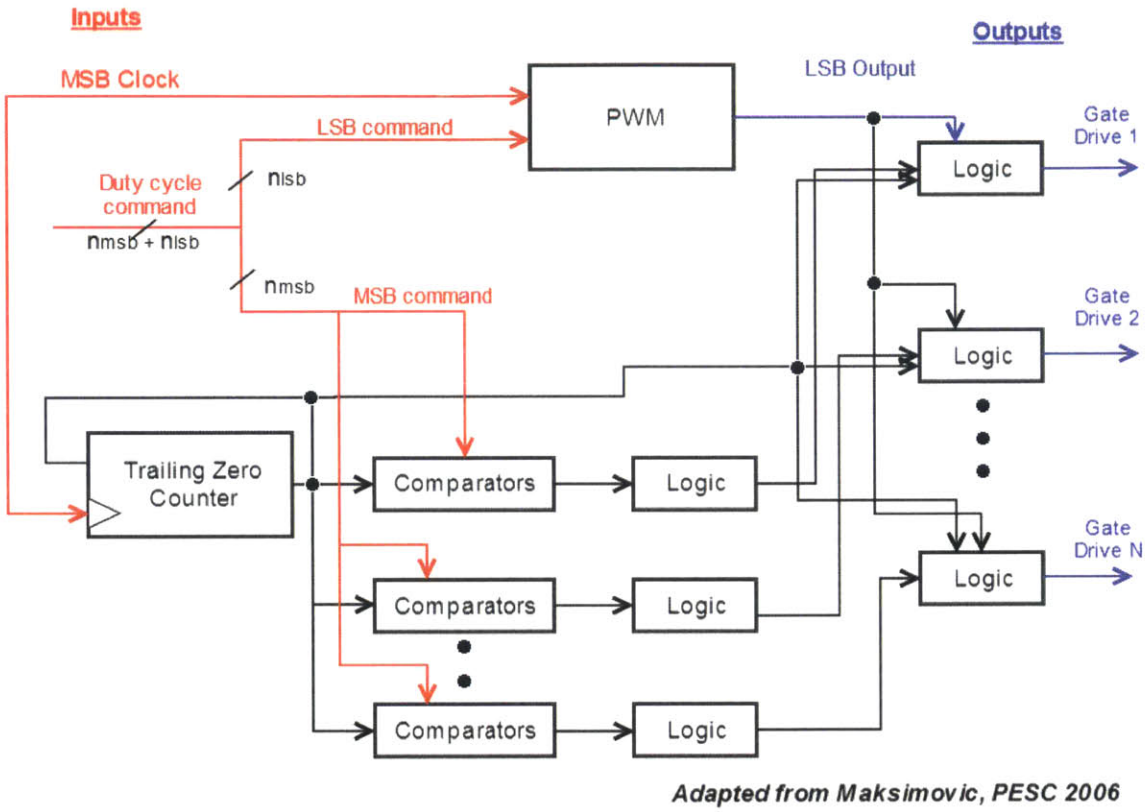


Figure 10: Hardware architecture of the initial multiphase modulator

This modulator takes as input a clock (MSB clock) with a frequency of $N \times F_{sw}$ and a duty cycle command which is split into an MSB command and an LSB command. The duty cycle command is updated at the rising edge of the MSB clock. The MSB command goes through comparators and a few logic blocks to determine the phases that are fully on and set their gate drive signals appropriately. At most N-1 phases can be fully on at a specific time step and the gate drive signal for the remaining phase is determined by the high resolution LSB command. Based on the MSB command, an n_{MSB}-bit counter is used to keep track of the

position of the phase whose gate drive signal is determined by the high resolution LSB command. The LSB command is then used by a PWM module which generates the gate drive signal for that phase.

This modulator has the advantage of implementing interleaving for multiphase converter as well as the ability to update duty cycle command at the MSB clock rate of $N \times F_{sw}$. The duty cycle update is performed instantaneously for the entire multiphase system. As a result, multiple phases in the converter can turn on/off simultaneously depending on duty cycle requirements. This behavior contrasts with the behavior of traditional multiphase converters in which phases are turned on in a regular order and each phase has to wait for its turn to go on/off.

These contrasting behaviors are illustrated in Figure 11 with a 16 phase converter where the duty cycle is slowly increasing. Figure 11a shows the operation of a traditional modulator in which the duty cycle is updated at a rate of F_{sw} (or period of T_{sw}). In this case, the phases are turned on/off in a predetermined order. During each switching interval of length T_{sw} all phases have the same duty cycle. Despite the continuous increase in duty cycle, each phase has to wait for an entire switching interval before updating to a new duty cycle. Figure 11b in contrast shows the operation of the advanced controller where the duty cycle is updated at a rate of $N \times F_{sw}$ (corresponding to a period of $\frac{T_{sw}}{N}$). In this case, as the duty cycle increases, the next phase scheduled to turn on updates its duty cycle within a $\frac{T_{sw}}{N}$ time interval without the need to wait for an entire switching period T_{sw}. As a result, the system can react more quickly to duty cycle changes and has a potential for faster transients.

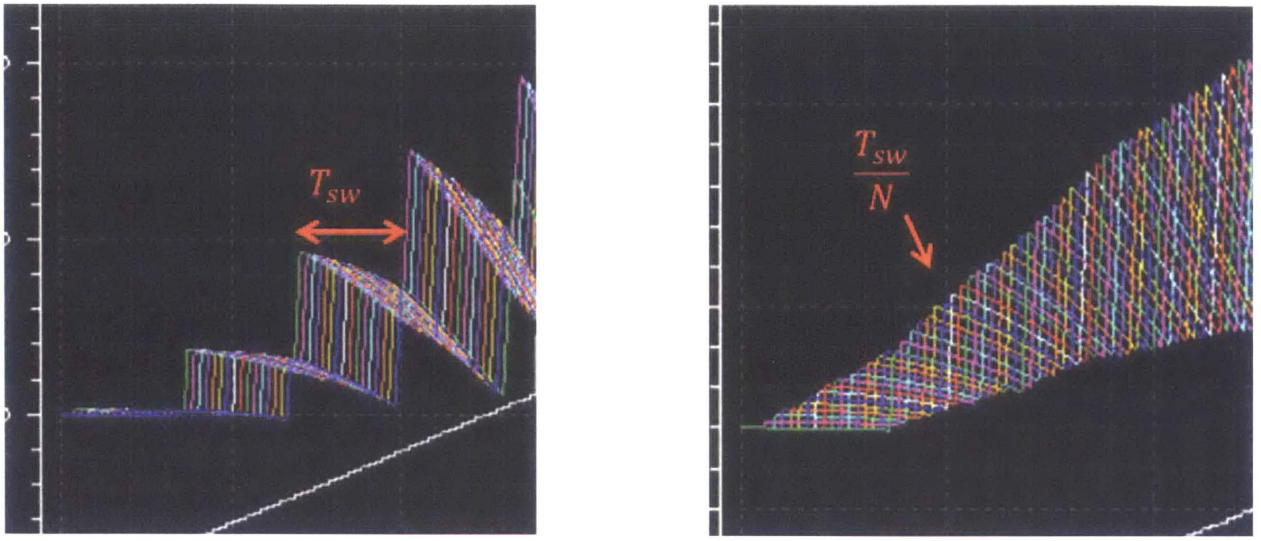


Figure 11: Inductor currents in a 16-phase converter when the duty cycle is slowly increasing a)case of a traditional modulator b)case of the advanced modulator

Another advantage of the advanced modulator, its ability to turn on/off multiple phases simultaneously, is illustrated in Figure 12 which shows the phase current for a 16-phase converter during a transition from a low to a high duty cycle. During that transition, almost all phases of the converter are turned on to keep up with the new duty cycle. This feature allows controllers to react quickly to large variations in duty cycle, a feature which is not present in traditional PWM controllers in which phases are always turned on consecutively in a predetermined order.

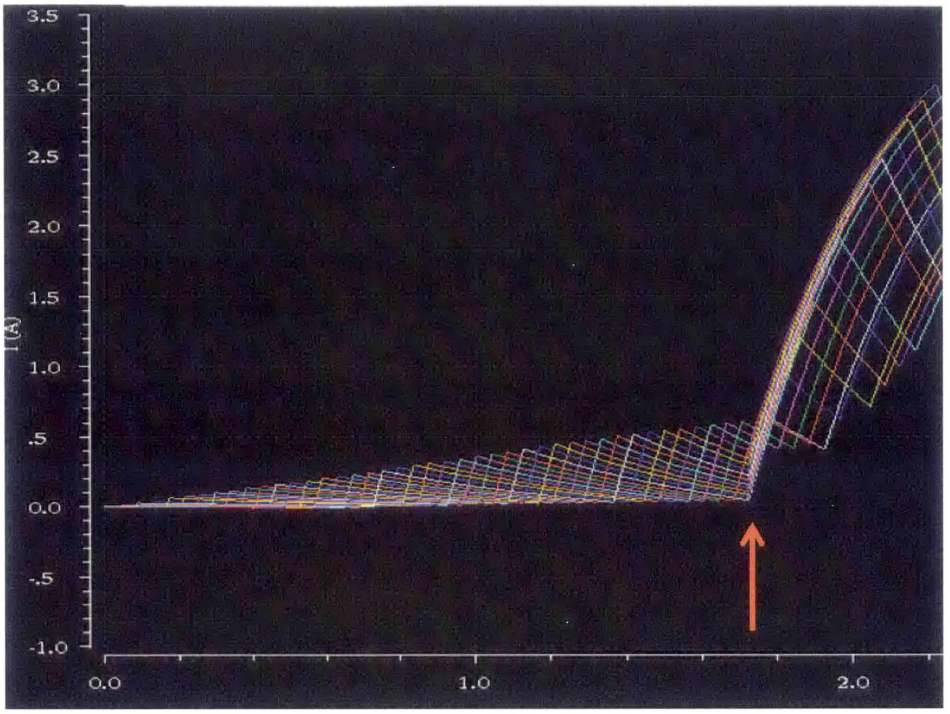


Figure 12: Inductor currents in a 16-phase converter for a low to high duty cycle transition

2.2.1.2 Modification to the advanced modulator

The modulator presented in [1] used a counter to determine which phase will receive the gate drive determined by the LSB portion of the duty cycle. In our implementation we also use a counter at steady state to maintain interleaving, but during transients, we implement a different algorithm that chooses which phase will receive the LSB portion of the duty cycle command, in order to avoid some undesirable current deviations during transients and improve the overall current balance in the system.
An illustration of the improvement resulting from this algorithm is illustrated in Figure 13 which shows the inductor currents in a 16-phase converter during 2 steps in the reference voltage. Figure 13a shows the currents with the initial counter based modulator presented [1]. With this modulator, there is visible mismatch between some of the phase currents

during both transients. Figure 13b shows the currents with the modified modulator which uses the current balancing algorithm. These waveforms do indeed show current balance improvement in Figure13b) with the new algorithm. By the end of both transients, all phase currents show significantly better matching.

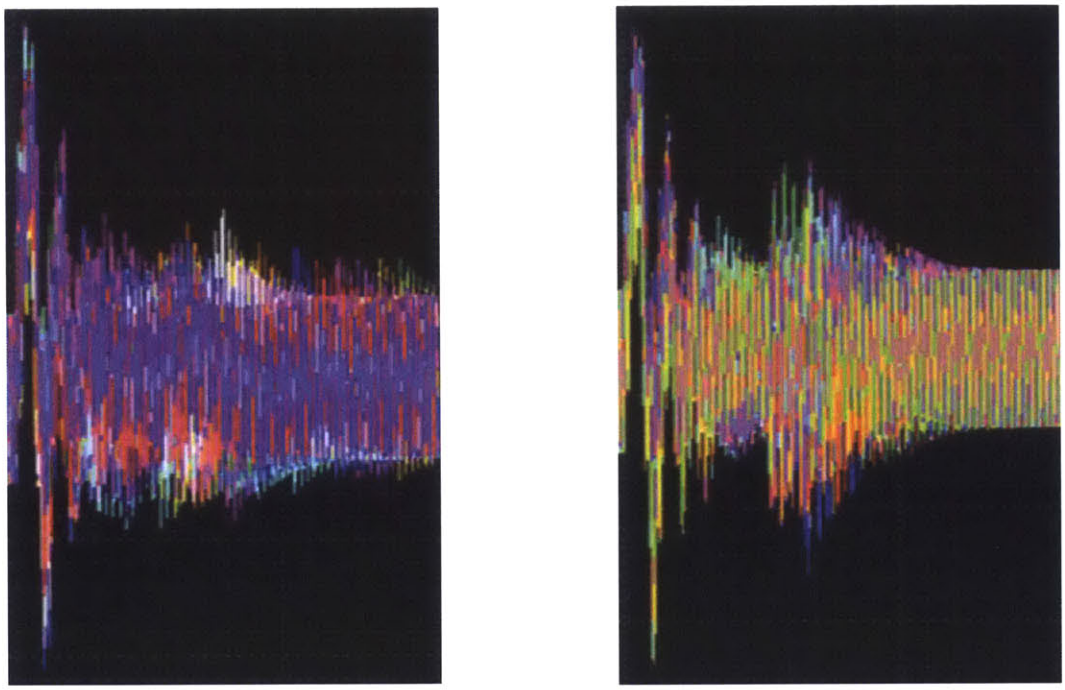


Figure 13: Comparison of inductor current balance in a 16-phase converter during reference voltage step a) Case of the counter-based advanced modulator b) Case of the advanced modulator with current balancing algorithm

Chapter 3 Controller studies of an 8-phase converter design

We analyze the speed and performance improvement in systems that use the advanced modulator with the new algorithm presented above. The performance of such systems is compared against the performance of systems that use traditional PWM modulators. To assess the performance of these systems, we implement a practical multiphase converter and design compensators for the power D/A model described in Chapter 2. Controllers of the form shown in Figure 9 are designed for each system. Three compensator types are used to compare the two systems. For each compensator type, an assessment of the performance of both the traditional and the advanced controllers is made and the results obtained are compared. .

3.1 Converter parameters

The parameters chosen for the practical converter system are as follows: the number of phases N =8, the nominal input voltage V_{in} = 3V, the per-phase switching frequency F_{SW} = 1MHz, the per-phase inductance is L = 300nH, the inductor series resistance is R_{dc} = 13.6mΩ, and the high-side and low-side switch resistances are each R_{on} = 54mΩ. The nominal output capacitance is 22μF per phase, so C = N×22μF = 8×22μF = 176μF. Each capacitor has an equivalent series resistance R_{esr} = 5mΩ. The sampling period $F_S = F_{SW}$ = 1MHz for controllers using the regular PWM modulator, and $F_S = N \times F_{SW}$ = 8MHz for controllers using the advanced modulator. For modeling purposes, we set $R_{Le} = R_{on} + R_{dc}$. Using these parameters, the model of our converter in Figure 9 is updated to include the resistances mentioned above, resulting in Figure 14.

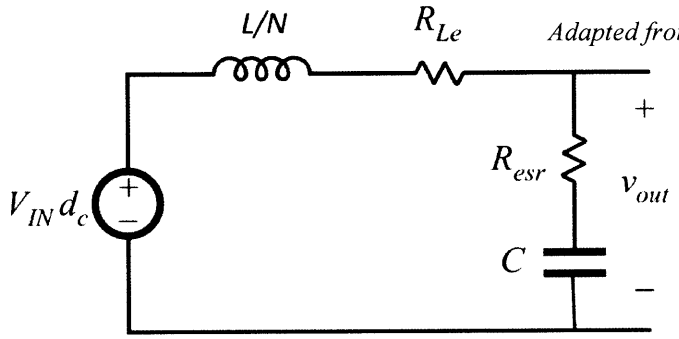


Figure 14: Equivalent circuit for compensator design

From the model in Figure 14, we derive the frequency response of the N-phase buck converter by replacing circuit elements with their respective impedances and finding the circuit's transfer function using a voltage divider equation as follows:

$$V_{out} = \frac{Z_{load}}{Z_{load} + s\frac{L}{N} + R_{Le}} \times \frac{(\sum_1^N c_k)}{N} V_{in} = \frac{Z_{load}}{Z_{load} + s\frac{L}{N} + R_{Le}} \times d_c \times V_{in} \qquad where\ Z_{load} = R_{esr} + \frac{1}{sC}$$

Then, $$G_{vds}(s) = \frac{V_{out}}{d_c}(s) = \frac{Z_{load}}{Z_{load}+s\frac{L}{N}+R_{Le}} V_{in} = \frac{5\times10^4\ s + 4.545\times10^{11}}{s^2+2.62\times10^5\ s+1.515\times10^{11}}$$

3.2 Compensator designs

Using MATLAB's ZOH mapping function we turn $G_{vds}(s)$ to the digital domain form $G_{vdz}(z)$. For the traditional controller, $F_s = F_{sw} = 1$ MHz and we obtain

$$G_{vdzt}(z) = \frac{(0.249\,z + 0.1459)}{z^2 - 1.638z + 0.7695} \times \frac{1}{z}.$$

For the advanced controller, $F_s = N \times F_{sw} = 8$ MHz and we obtain

$$G_{vdza}(z) = \frac{(9.658\times10^{-3}\,z - 2.672\times10^{-3})}{z^2 - 1.965z + 0.9678} \times \frac{1}{z}.$$

The additional factor $\frac{1}{z}$ models the delay of T_s from sampling the voltage error to updating the duty cycle command d_c. It is assumed that the total ADC conversion plus compensator calculation is completed in less than one sampling interval 1/Fs.

Three different compensator methods were considered. Each compensator was designed in the analog domain, and then converted to the digital domain. The three compensator design methods are presented below.

Method 1: Integrator

- Place a pole at s = 0 for integration (to ensure 0 steady state error)

Using this method in MATLAB, we obtain a compensator for the traditional controller $G_{ct1}(z) = 0.02107 \times \frac{z+1}{z-1}$. The magnitude and phase response of the system loop gain $G_{vdzt}(z) \times G_{ct1}(z)$ are shown in Figure 15a. A 22 KHz loop gain bandwidth was achieved with this compensator. For the advanced controller, this method yielded the compensator $G_{ca1}(z) = 0.002819 \times \frac{z+1}{z-1}$. The magnitude and phase response of the system loop gain $G_{vdza}(z) \times G_{ca1}(z)$ are shown in Figure 15b. A 24.5 KHz loop gain bandwidth was achieved with this compensator. The step responses for both the traditional and advanced controllers are shown in Figure 16.

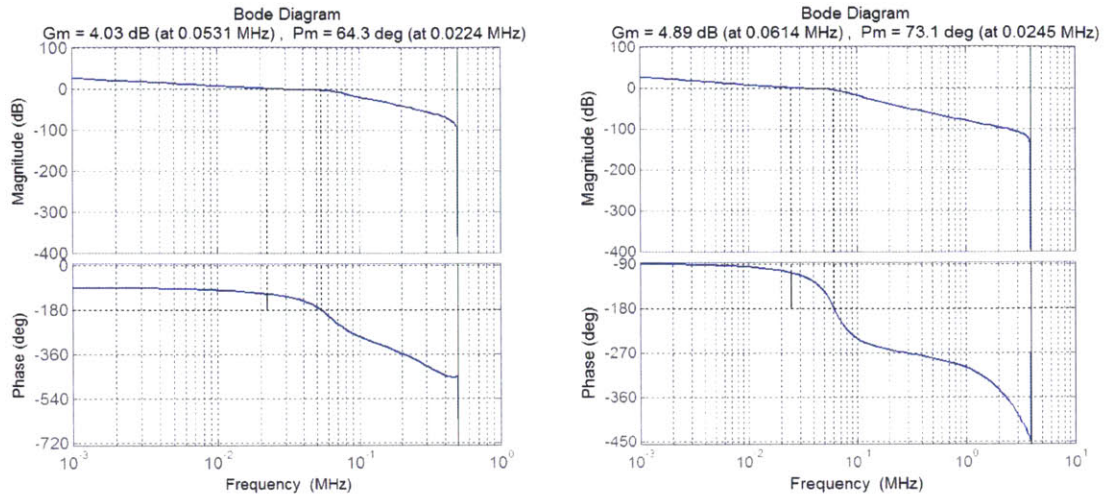


Figure 15: Magnitude and Phase response of the loop gain in the a) traditional controller system b) advanced controller system both using Method 1

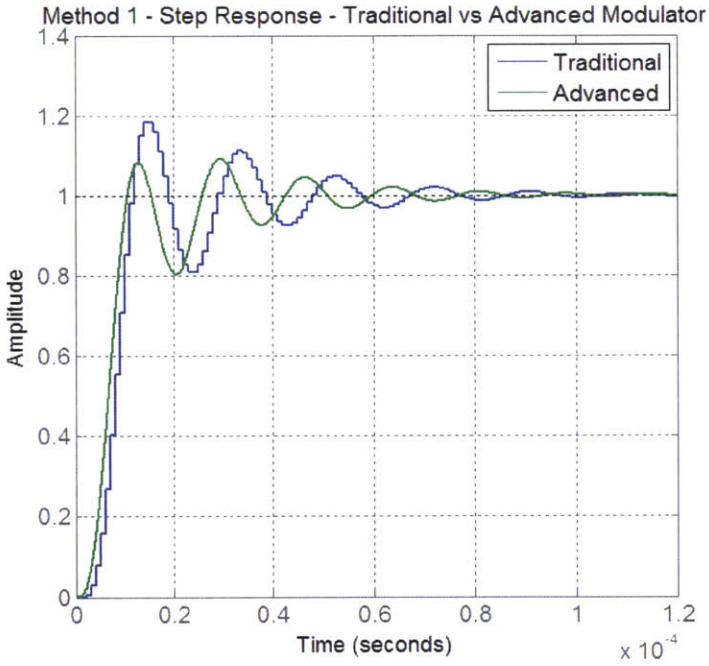


Figure 16: Step response comparison of Traditional and Advanced modulator based controllers designed using Method 1

Method 2: 1 pole, 1 zero compensator

- Place a pole at s = 0 for integration (to ensure 0 steady state error)
- Place 1 zero at the converter's double pole frequency to reduce phase drop
- Convert to digital form using Tustin mapping for best pole matching
- Adjust gain for a 40° minimum phase margin, less than 20% overshoot, and no oscillations in the first rising edge of the step response

Using this method in MATLAB, we obtain a compensator for the traditional controller $G_{ct2}(z) = \frac{0.04852\,z - 0.03287}{z-1}$. The magnitude and phase response of the system loop gain $G_{vdzt}(z) \times G_{ct2}(z)$ are shown in Figure 17a. A 7.62 KHz loop gain bandwidth was achieved with this compensator. For the advanced controller, this method yielded the compensator $G_{ca2}(z) = \frac{0.04913\,z - 0.04682}{z-1}$. The magnitude and phase response of the system loop gain $G_{vdza}(z) \times G_{ca2}(z)$ are shown in Figure 17b. A 9.06 KHz loop gain bandwidth was achieved with this compensator. The step responses for both the traditional and advanced controllers are shown in Figure 18.

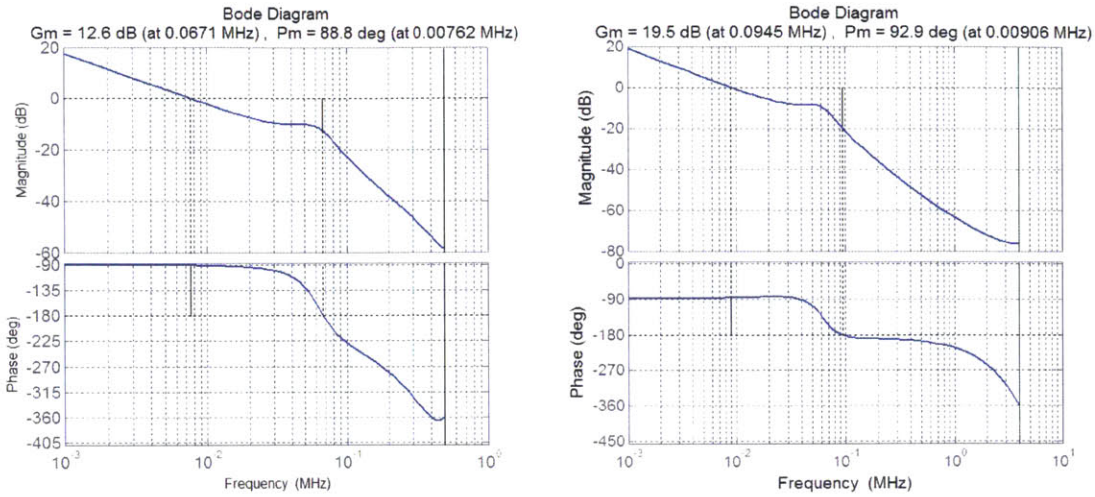


Figure 17: Magnitude and Phase response of the loop gain in the a) traditional controller system b) advanced controller system both using Method 2

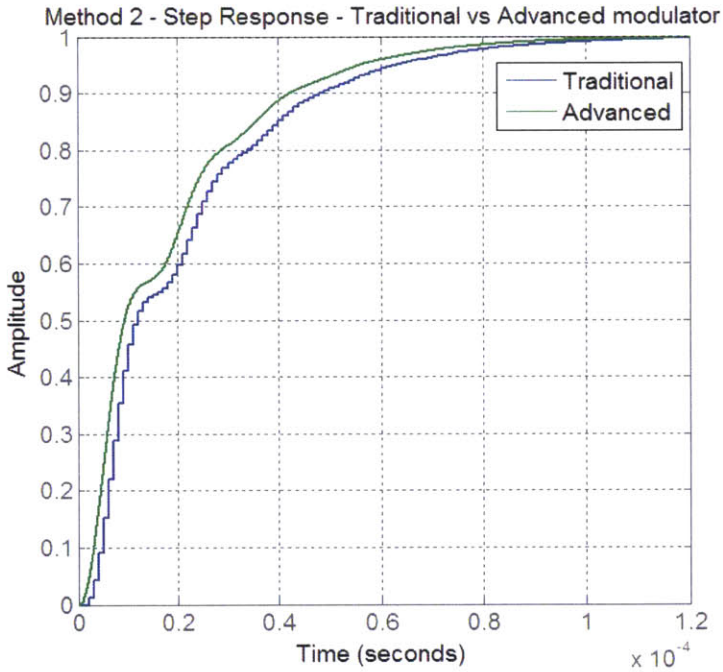


Figure 18: Step response comparison of Traditional and Advanced modulator based controllers designed using Method 2

Method 3: 2 poles, 2 zeroes compensator

- Place a pole at 0 for integrator (to ensure 0 steady state error)
- Place 2 zeroes at the converter's double pole frequency to reduce phase drop
- Place 1 high-frequency pole at $\frac{F_S}{2}$ (The lower this pole's frequency, the lower the high-frequency gain of the digital compensator, and the smaller the oscillations in the duty cycle. $\frac{F_S}{2}$ was experimentally found to be a pole location with acceptable/no duty cycle oscillations to an error impulse input)
- Convert to digital form using Tustin mapping for best pole matching
- Adjust gain for a 40° minimum phase margin, less than 20% overshoot, and no oscillations in the first rising edge of the step response

Using this method in MATLAB, we obtain a compensator for the traditional controller $G_{ct3}(z) = \frac{0.05922\,z^2 - 0.08023\,z + 0.02718}{z^2 - 1.606\,z + 0.6063}$. The magnitude and phase response of the system loop gain $G_{vdzt}(z) \times G_{ct3}(z)$ are shown in Figure 19a. A 7.65 KHz loop gain bandwidth was achieved with this compensator. For the advanced controller, this method yielded the compensator $G_{ca3}(z) = \frac{5.604\,z^2 - 10.67\,z + 5.08}{z^2 - 1.603\,z + 0.6025}$. The magnitude and phase response of the system loop gain $G_{vdza}(z) \times G_{ca2}(z)$ are shown in Figure 19b. A 157 KHz loop gain bandwidth was achieved with this compensator. The step responses for both the traditional and advanced controllers are shown in Figure 20.

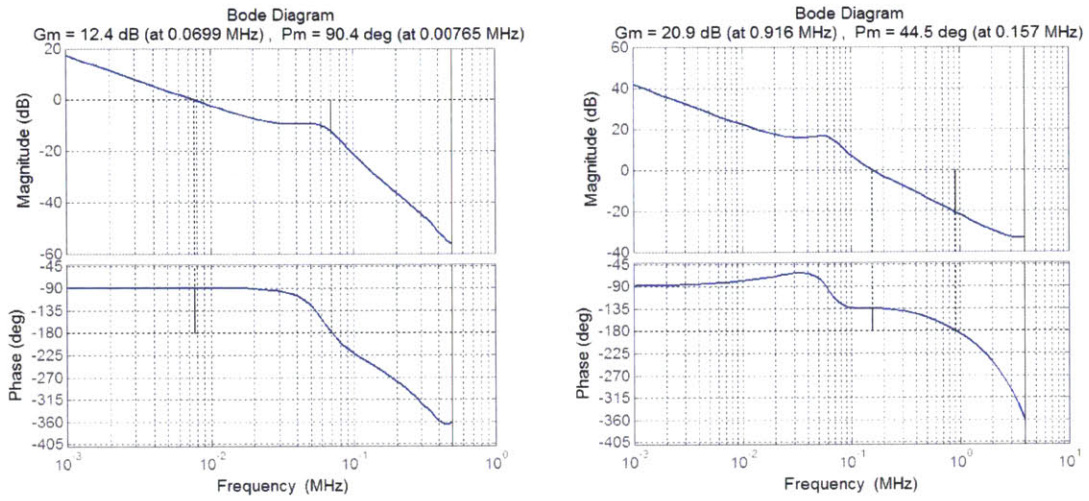


Figure 19: Magnitude and Phase response of the loop gain in the a) traditional controller system b) advanced controller system both using Method 3

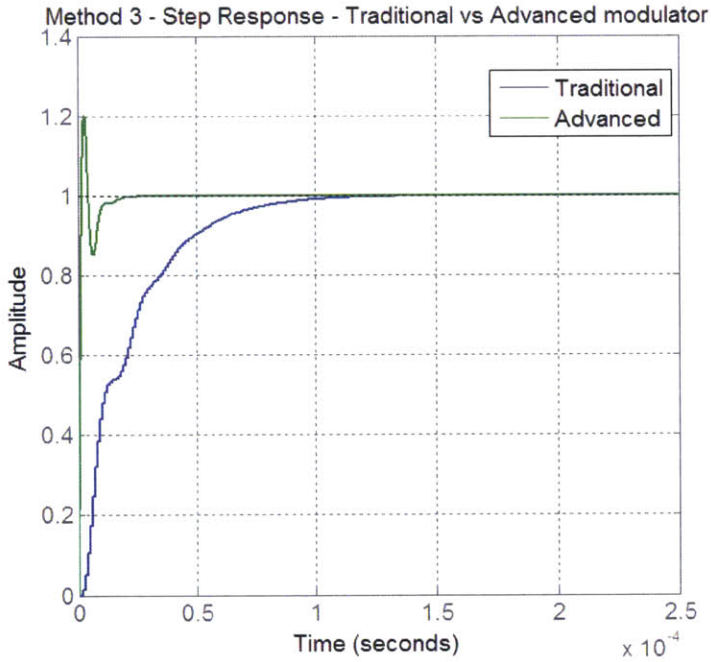


Figure 20: Step response comparison of Traditional and Advanced modulator based controllers designed using Method 3

3.3 Simulation performance results

The performance of the above presented compensators was evaluated using Cadence test benches. An illustration of which is presented in Figure 21. The power stage was implemented using passives and an ideal switch. The modulators and the ADC were both implemented as VerilogA blocks. We chose to use a 9-bit duty cycle command d_c, corresponding to 3-bit MSB commands and 6-bit LSB commands for the advanced modulator. The resolution of the PWM module therefore corresponds to an LSB of $\frac{Vin}{d_{c\_LSB}} = \frac{3V}{2^9} = 5.9mV$. In order to avoid limit cycles in the system, we need the ADC's resolution to be lower than the resolution of the PWM converter. From [7], we need: Resolution of PWM ≥ Resolution of ADC +1. We therefore chose the bin size of the ADC to be 20mV in order to meet this requirement. The compensators designed above were also implemented as verilogA modules.

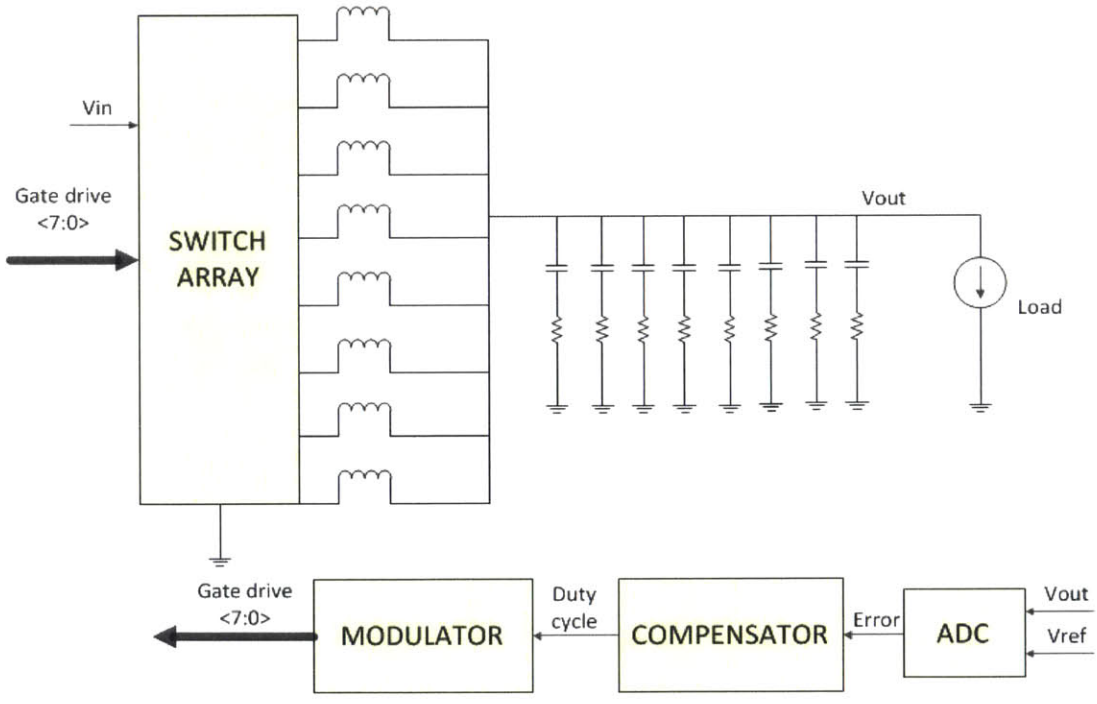


Figure 21: Illustration of a circuit test bench in Cadence

3.3.1 Simulation results for the traditional modulator

The benchmark we used in our test was the system implemented using the traditional modulator. Our system was tested both for reference tracking performance as well as load transient performance. We tested this system with the 3 compensators designed in section 3.2 for the traditional modulator $G_{ct1}(z), G_{ct2}(z), and\ G_{ct3}(z)$. The results of the tests are presented below and analyzed in Chapter 4.

3.3.1.1 Reference tracking simulations

- **Compensator $G_{ct1}(z)$**

Figure 22 demonstrates a 0.1V step in the system with compensator $G_{ct1}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The transition has a **6.25µs** rise time, a **21.4%** overshoot and a **44µs** settling time. After a couple of oscillations, the output voltage accurately tracks the reference within $\pm$10mV as expected from the size of the ADC's zero error bin. Both output voltage and duty cycle command settle to a constant value at steady state with no limit cycle, and the inductor currents are well matched both during transients and at steady state.

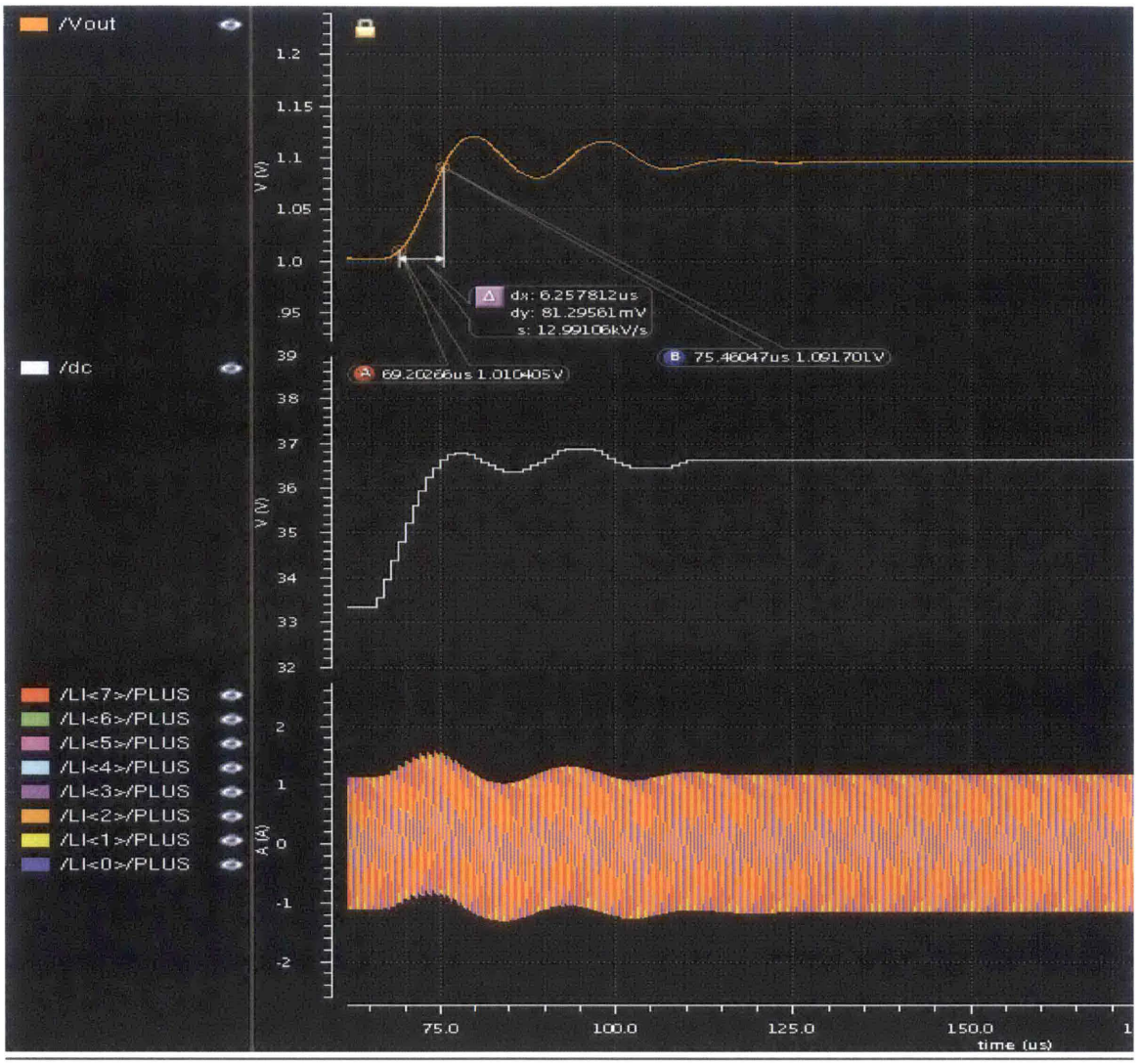


Figure 22: Reference tracking simulation with traditional modulator and $G_{ct1}(z)$ compensator a) Output voltage for 0.1V Vref step b) Duty cycle c) Inductor currents

- **Compensator $G_{ct2}(z)$**

Figure 23 demonstrates a 0.1V step in the system with compensator $G_{ct2}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. This transition has a **41.45µs** rise time, a **74.18µs** settling time and **no** overshoot.

The output voltage accurately tracks the reference within ± 10mV as expected from the size of the ADC's zero error bin. Both output voltage and duty cycle command settle to a constant value at steady state with no limit cycle, and the inductor currents are well matched both during transients and at steady state. The output voltage in this case has no overshoot and the rising edge resembles that of a second order system with slight oscillations.

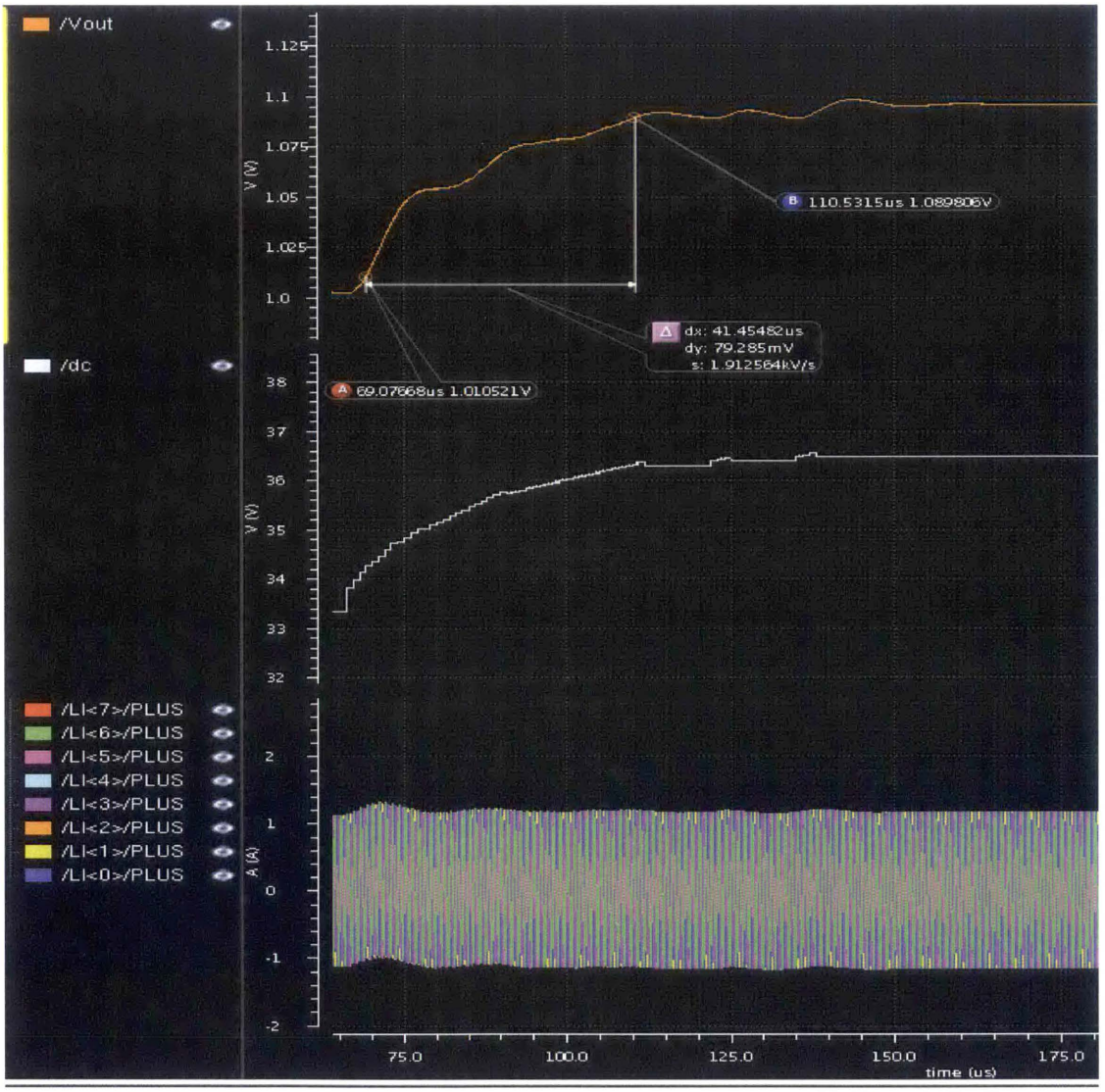


Figure 23: Reference tracking simulation with traditional modulator and $G_{ct2}(z)$ compensator a) Output voltage for 0.1V Vref step b) Duty cycle c) Inductor currents

- **Compensator $G_{ct3}(z)$**

Figure 24 demonstrates a 0.1V step in the system with compensator $G_{ct3}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The transition has a **42.16µs** rise time, and a **73.04µs** settling time. The output voltage accurately tracks the reference within $\pm$10mV as expected from the size of the ADC's zero error bin. Both output voltage and duty cycle command settle to a constant value at steady state with no limit cycle, and the inductor currents are well matched both during transients and at steady state.

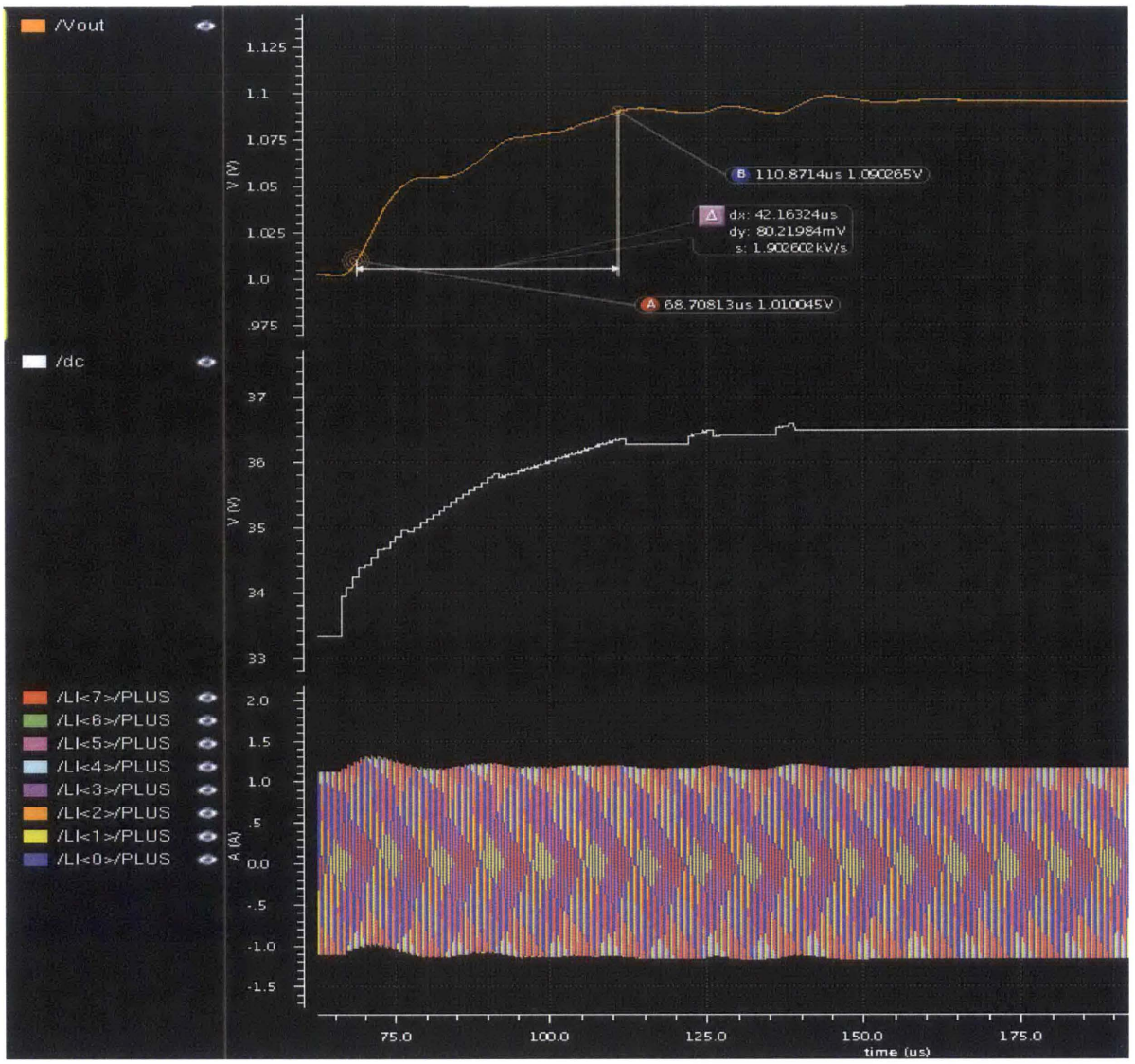


Figure 24: Reference tracking simulation with traditional modulator and $G_{ct3}(z)$ compensator a) Output voltage for 0.1V Vref step b) Duty cycle c) Inductor currents

As expected from the theoretical bandwidths reported in Section 3.2, the traditional modulator based controller with compensator $G_{ct1}(z)$ achieves the highest speed in rise time (**6.25µs**) compared to $G_{ct2}(z)$ (**41.45µs)** and $G_{ct3}(z)$ **(42.16µs).** $G_{ct1}(z)$ also

outperforms $G_{ct2}(z)$ and $G_{ct3}(z)$ in settling time with a **44µs** settling time for $G_{ct1}(z)$ compared to **74.18µs** for $G_{ct2}(z)$ and **73.04µs** for $G_{ct3}(z)$.

3.3.1.2 Load transient simulation results

Load transient simulations with the traditional controllers were also performed and the results are presented below.

- **Compensator $G_{ct1}(z)$**

Figure 25 demonstrates a 16A current load step at a rate of 8A/ps in the system with compensator $G_{ct1}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The output voltage droops by **250.6mV** during the transition and it takes **81.76µs** for it to settle back within the zero error bin of the ADC. A few oscillations are observed after the voltage droop before steady state is reached. The system does not exhibit any limit cycle and there is good matching between the phase currents.

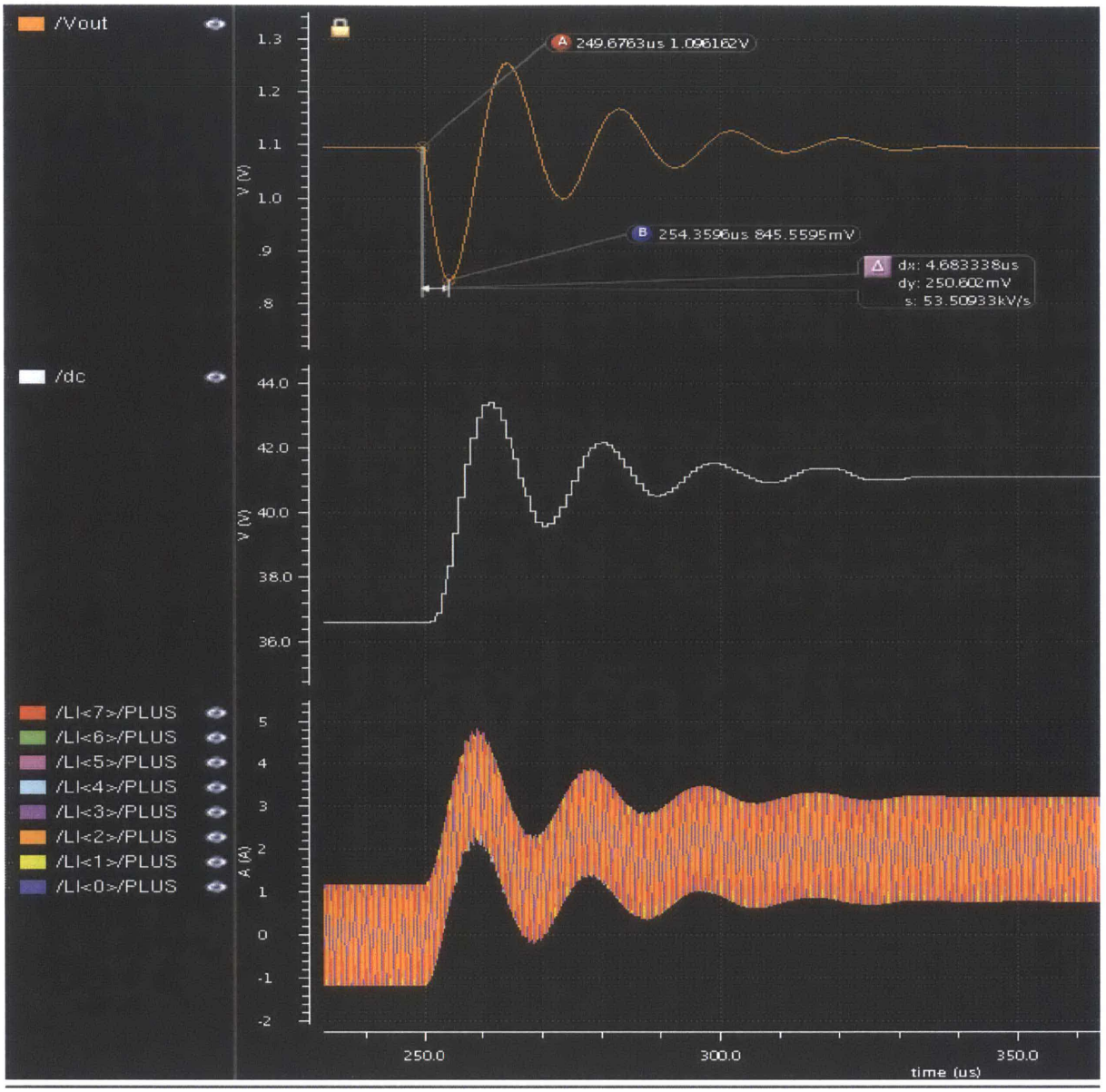


Figure 25: Load transient simulation with the traditional modulator and $G_{ct1}(z)$ a) Output voltage for 16A load step b) Duty cycle c) Inductor currents

- **Compensator $G_{ct2}(z)$**

Figure 26 demonstrates a 16A current load step at a rate of 8A/ps in the system with compensator $G_{ct2}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The output voltage droops by **252.4mV** during the transition and it takes **60µs** for it to settle back within the zero error bin of the ADC. The output voltage slightly oscillates after the voltage droop before steady state is reached. But the oscillations are less significant compared to the oscillations above with compensator $G_{ct1}(z)$. The system does not exhibit any limit cycles and there is good matching between the phase currents both during transients and at steady state.

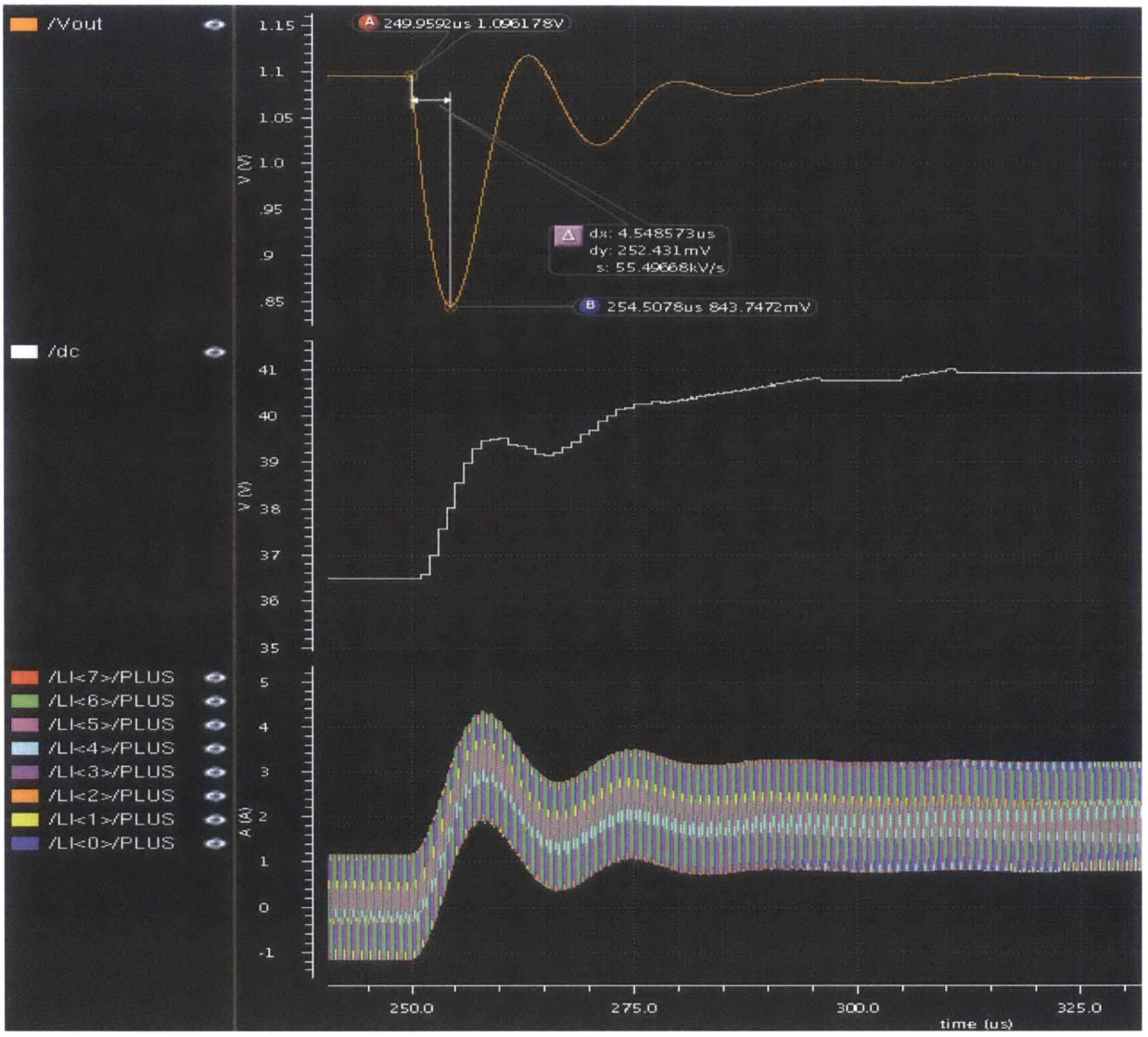


Figure 26: Load transient simulation with the traditional modulator and $G_{ct2}(z)$ a) Output voltage for 16A load step b) Duty cycle c) Inductor currents

- **Compensator $G_{ct3}(z)$**

Figure 27 demonstrates a 16A current load step at a rate of 8A/ps in the system with compensator $G_{ct3}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The output voltage droops by **250.1mV** during the transition and it takes **70.28µs** for it to settle back within the zero error bin of the ADC. . In this case

also, the output voltage slightly oscillates after the voltage droop before steady state is reached. These oscillations are comparable to the oscillations presented above with compensator $G_{ct2}(z)$. The system does not exhibit any limit cycles and there is good matching between the phase currents both during transients and at steady state.

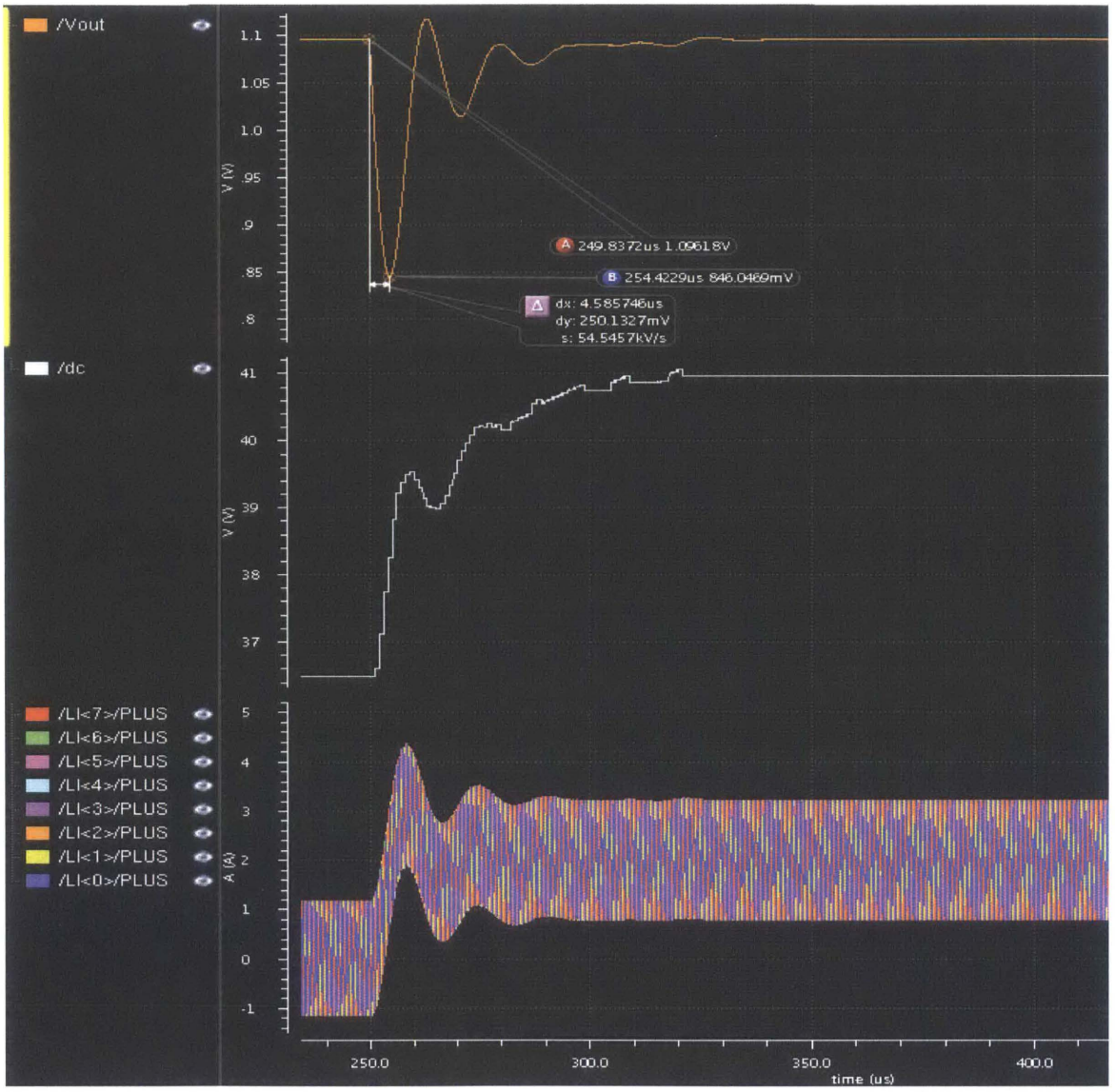


Figure 27: Load transient simulation with the traditional modulator and $G_{ct3}(z)$ a) Output voltage for 16A load step b) Duty cycle c) Inductor currents

With a 16A, 8A/ps load step, the voltage droop is similar across the 3 types of controller using the traditional modulator. The droop time is around 4.5-4.6μs and the voltage droop is around **250.1-252.4mV** which suggests that regardless of the 2.8X bandwidth difference from $G_{ct1}(z)$ to $G_{ct2}(z)$ and $G_{ct3}(z)$, the 3 controllers achieved with the traditional modulator are still too slow to keep up with the fast load transient. But the advanced controller improved these performances especially with the compensator design method 3.

3.3.2 Simulation results for the advanced modulator

A test bench was set up for our circuit using the advanced modulator. The resulting system was tested both for reference tracking performance as well as load transient performance. We tested this system with the 3 compensators designed in section 3.2 for the advanced modulator $G_{ca1}(z), G_{ca2}(z), and\ G_{ca3}(z)$.

3.3.2.1 Reference tracking simulations

- **Compensator $G_{ca1}(z)$**

Figure 28 demonstrates a 0.1V step in the system with compensator $G_{ca1}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The transition has a **6.2μs** rise time, a **9.74%** overshoot and a **24.04μs** settling time. After a couple of oscillations, the output voltage accurately tracks the reference within ±10mV as expected from the size of the ADC's zero error bin. Both output voltage and duty cycle command settle to a constant value at steady state with no limit cycle, and the inductor currents are well matched both during transients and at steady state.

This compensator shows a significant improvement in overshoot (**11.66%**) and Vref step settling time (**45.35%**) compared to the traditional compensator $G_{ct1}(z)$. But the rise times are essentially equal as expected from the comparable bandwidths.

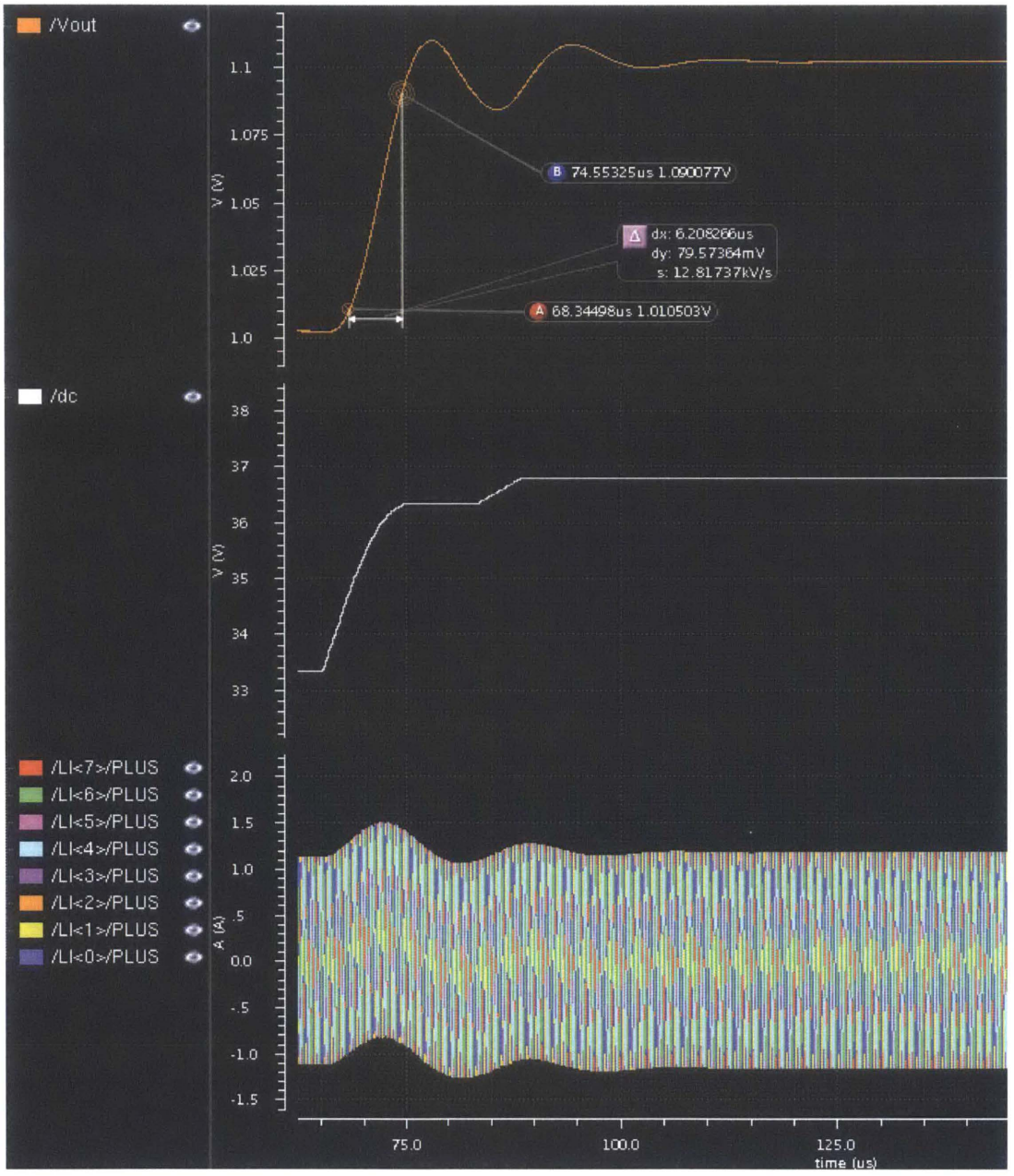


Figure 28: Reference tracking simulation with advanced modulator and $G_{ca1}(z)$ compensator a) Output voltage for 0.1V Vref step b) Duty cycle c) Inductor currents

- **Compensator $G_{ca2}(z)$**

Figure 29 demonstrates a 0.1V step in the system with compensator $G_{ca2}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The transition has a **36.54µs** rise time, and a **62.08µs** settling time with **no** overshoot. The output voltage accurately tracks the reference within $\pm$10mV as expected from the size of the ADC's zero error bin. Both output voltage and duty cycle command settle to a constant value at steady state with no limit cycle. The transient is close to a first order response and the inductor currents are well matched both during transients and at steady state. This compensator also shows improvement in rise time (**11.8%**), and Vref step settling time (**16.31%**) compared to the traditional compensator $G_{ct2}(z)$.

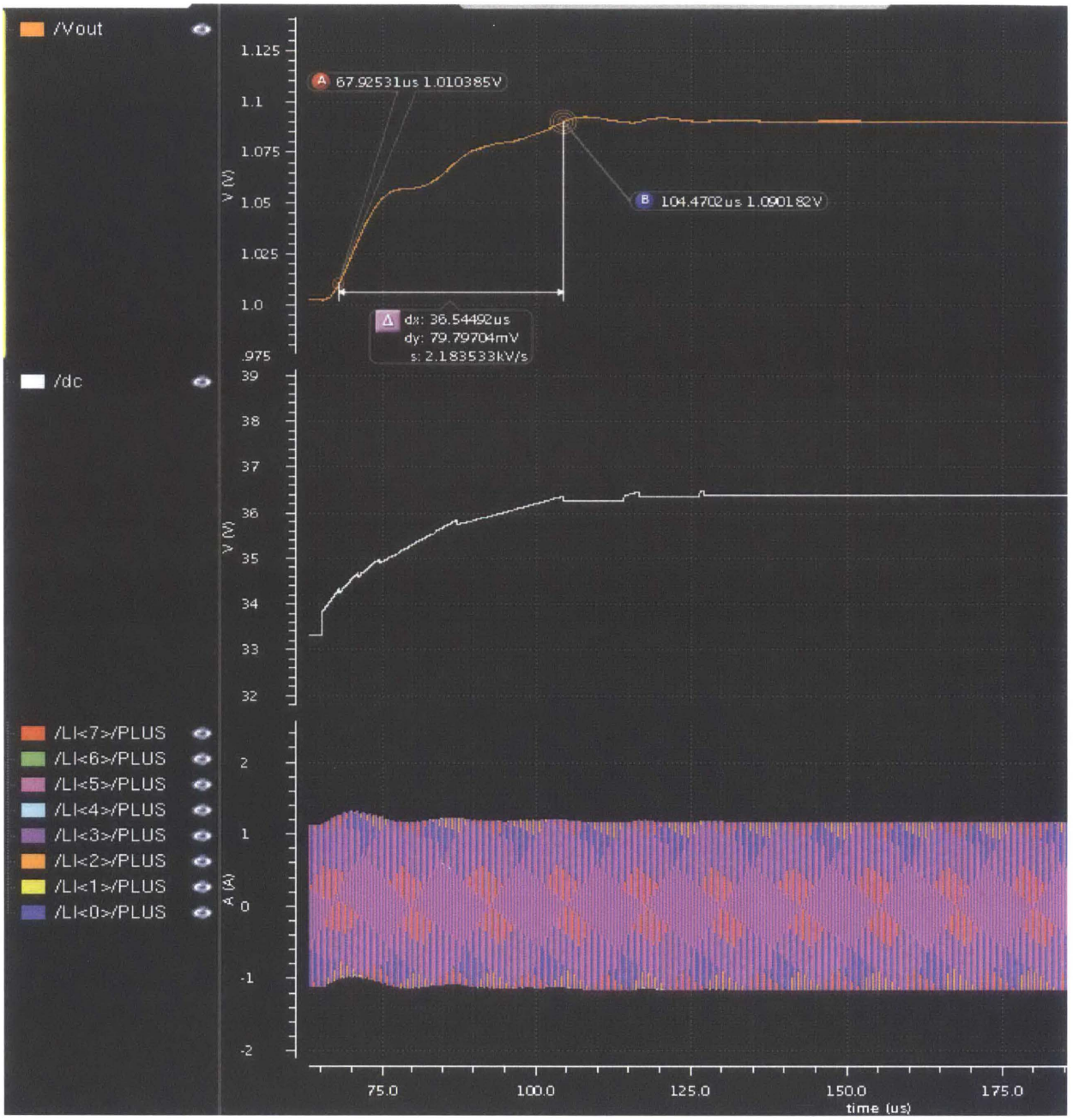


Figure 29: Reference tracking simulation with advanced modulator and $G_{ca2}(z)$ compensator a) Output voltage for 0.1V Vref step b) Duty cycle c) Inductor currents

- **Compensator $G_{ca3}(z)$**

Figure 30 demonstrates a 0.1V step in the system with compensator $G_{ca3}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The transition has a **1.24µs** rise time, a **20.75µs** settling time and an **18.05%** overshoot. The output voltage again settles within $\pm$10mV of the reference at steady state and the system has no limit cycles. Due to the larger bandwidth of this controller, the duty cycle changes more quickly during transients compared to the previous compensators $G_{ca1}(z)$ and $G_{ca2}(z)$. As a result, the matching between inductor currents degrades during transients compared to the previous systems. Although overshoot worsened by **18.05%** due to lower phase margin, this compensator allowed a **97.06%** improvement in rise time and a **71.59%** improvement in Vref step settling time compared to the traditional compensator $G_{ct3}(z)$.

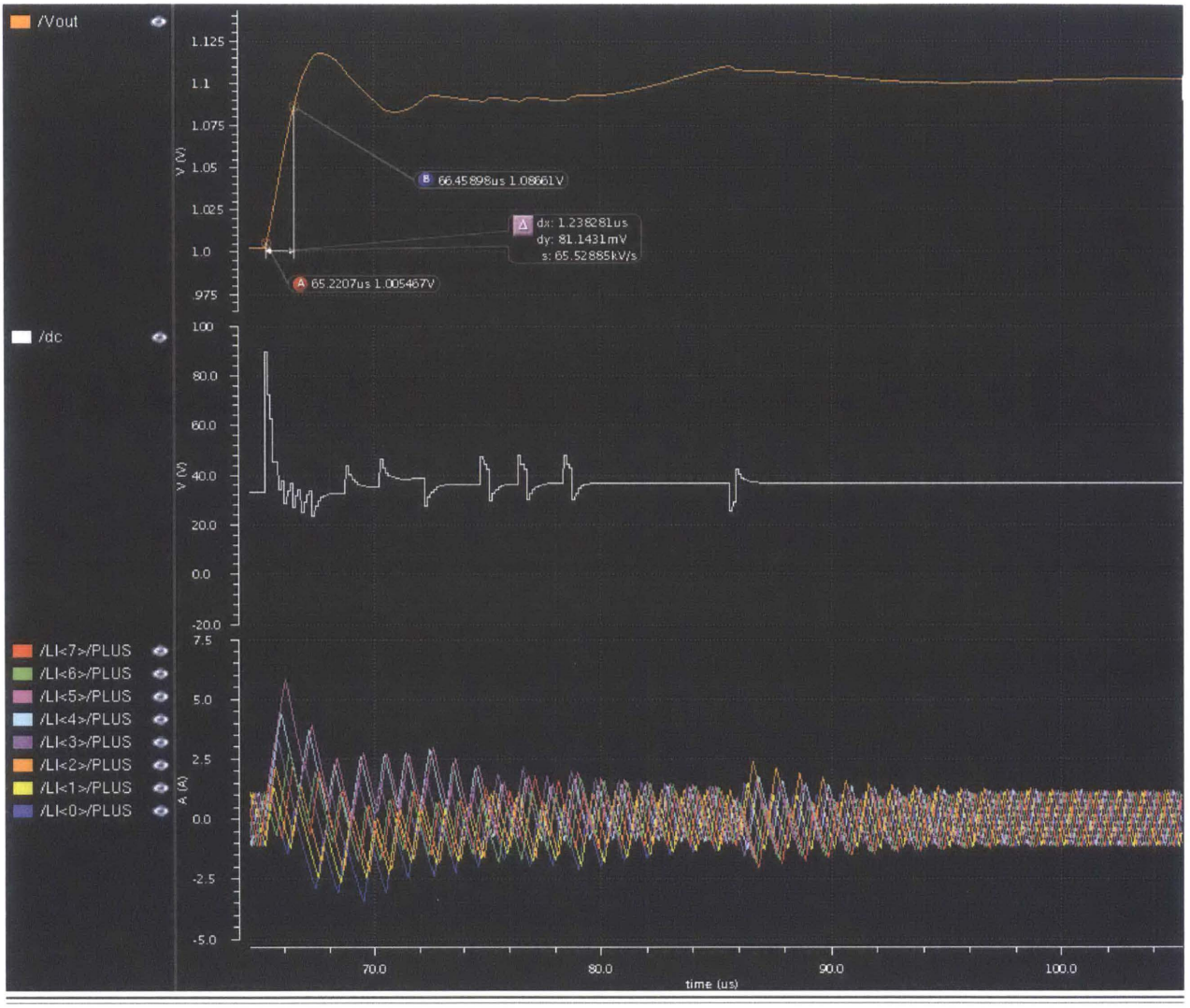


Figure 30: Reference tracking simulation with advanced modulator and $G_{ca3}(z)$ compensator a) Output voltage for 0.1V Vref step b) Duty cycle c) Inductor currents

3.3.2.2 Load transient simulation results

- **Compensator $G_{ca1}(z)$**

Figure 31 demonstrates a 16A current load step at a rate of 8A/ps in the system with compensator $G_{ca1}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The output voltage droops by **237.3mV** during the transition

and it takes **74.31µs** for it to settle back within the zero error bin of the ADC. These values represent a **5.42%** improvement in voltage droop and **9.11%** improvement in droop settling time from the traditional controller with compensator $G_{ct1}(z)$. Some oscillations are observed at the output voltage after the voltage droop. These oscillations disappear as we reach steady state and the system does not exhibit any limit cycles. There also is good matching between the phase currents both during transients and at steady state.

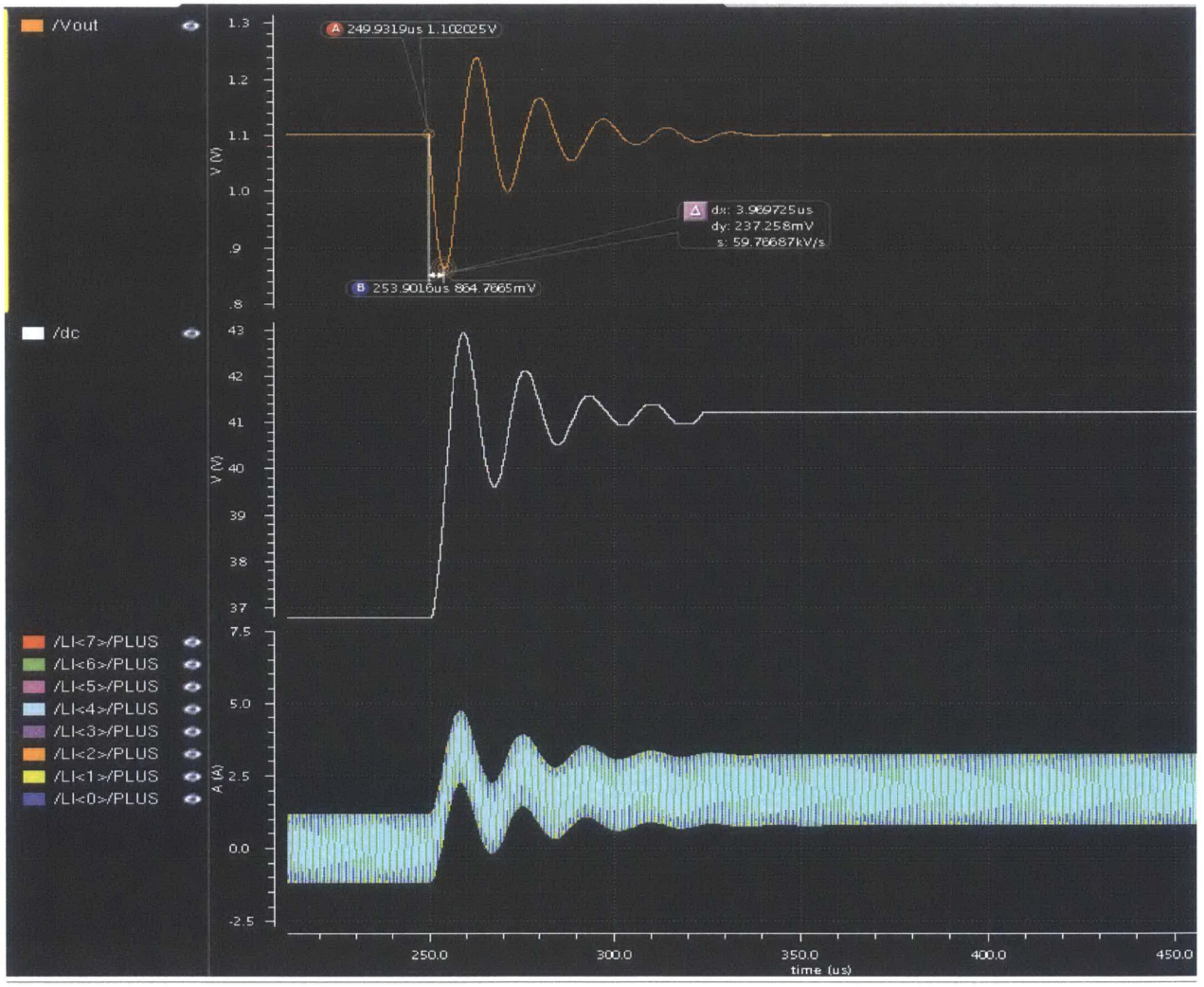


Figure 31: Load transient simulation with the advanced modulator and $G_{ca1}(z)$ a) Output voltage for 16A load step b) Duty cycle c) Inductor currents

- **Compensator $G_{ca2}(z)$**

Figure 32 demonstrates a 16A current load step at a rate of 8A/ps in the system with compensator $G_{ca2}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The output voltage droops by **232mV** during the transition and it takes **64.04µs** for it to settle back within the zero error bin of the ADC.These values represent an **8.08%** improvement in voltage droop but **6.3%** degradation in droop settling time from the traditional controller with compensator $G_{ct2}(z)$. The output voltage slightly oscillates after the voltage droop before steady state is reached. But the oscillations are less significant compared to the oscillations above with compensator $G_{ca1}(z)$. The system does not exhibit any limit cycles and there is good matching between the phase currents both during transients and at steady state.

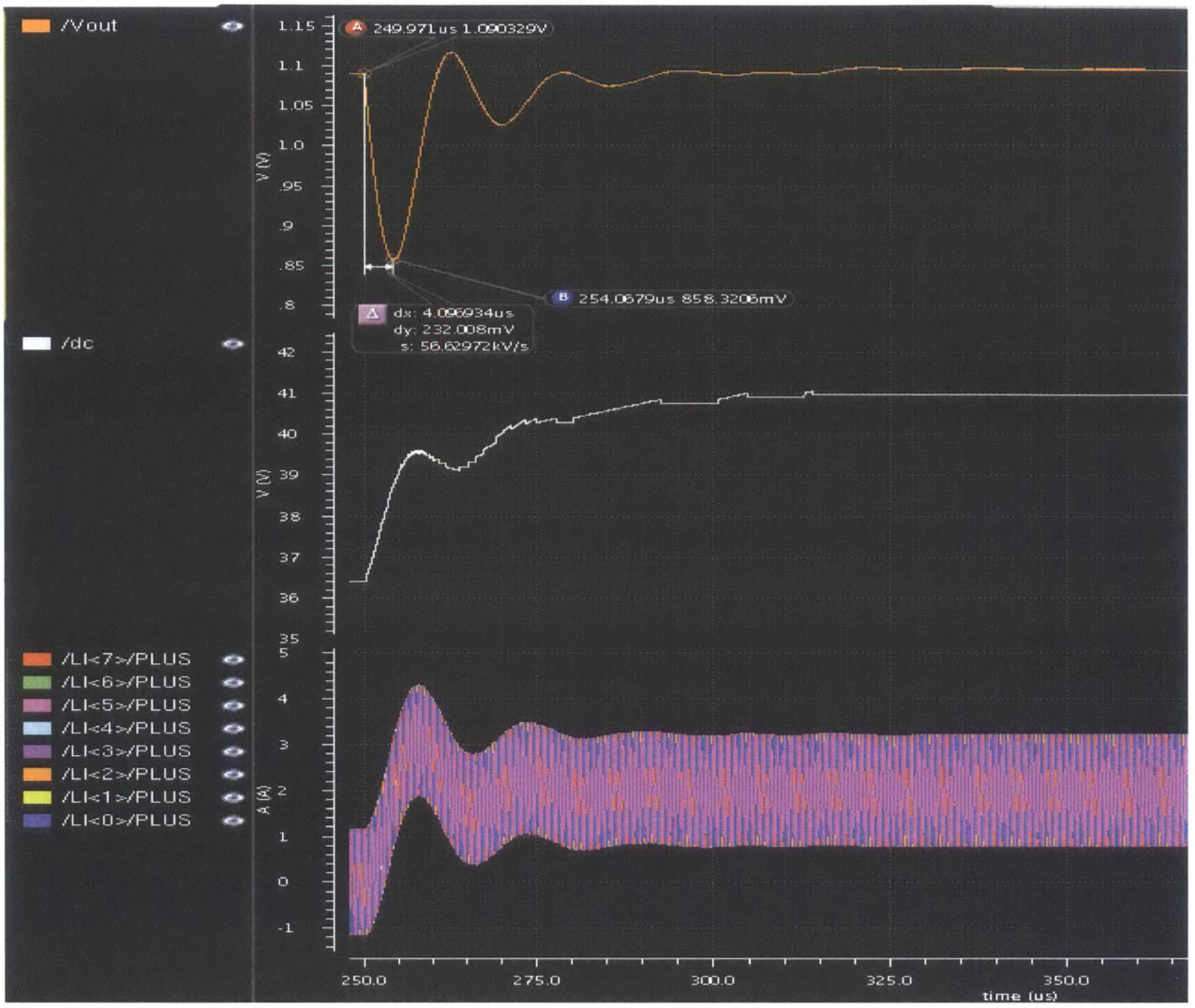


Figure 32: Load transient simulation with the advanced modulator and $G_{ca2}(z)$ a) Output voltage for 16A load step b) Duty cycle c) Inductor currents

- **Compensator $G_{ca3}(z)$**

Figure 33 demonstrates a 16A current load step at a rate of 8A/ps in the system with compensator $G_{ca3}(z)$. The output voltage of the system along with phase currents and duty cycle commands are plotted. The output voltage droops by **85.46mV** during the transition

and it takes **9.76μs** for it to settle back within the zero error bin of the ADC. These values represent a **65.83%** improvement in voltage droop and **86.11%** improvement in droop settling time from the traditional controller with compensator $G_{ct3}(z)$. The output voltage slightly oscillates after the voltage droop before steady state is reached. But the droop magnitude is significantly smaller compared to the droop obtained with compensators $G_{ca1}(z)$ and $G_{ca2}(z)$. Due to the larger bandwidth of this controller, the duty cycle changes more quickly during transients compared to the previous compensators $G_{ca1}(z)$ and $G_{ca2}(z)$. As a result, the matching between inductor currents degrades during transients compared to the previous systems.

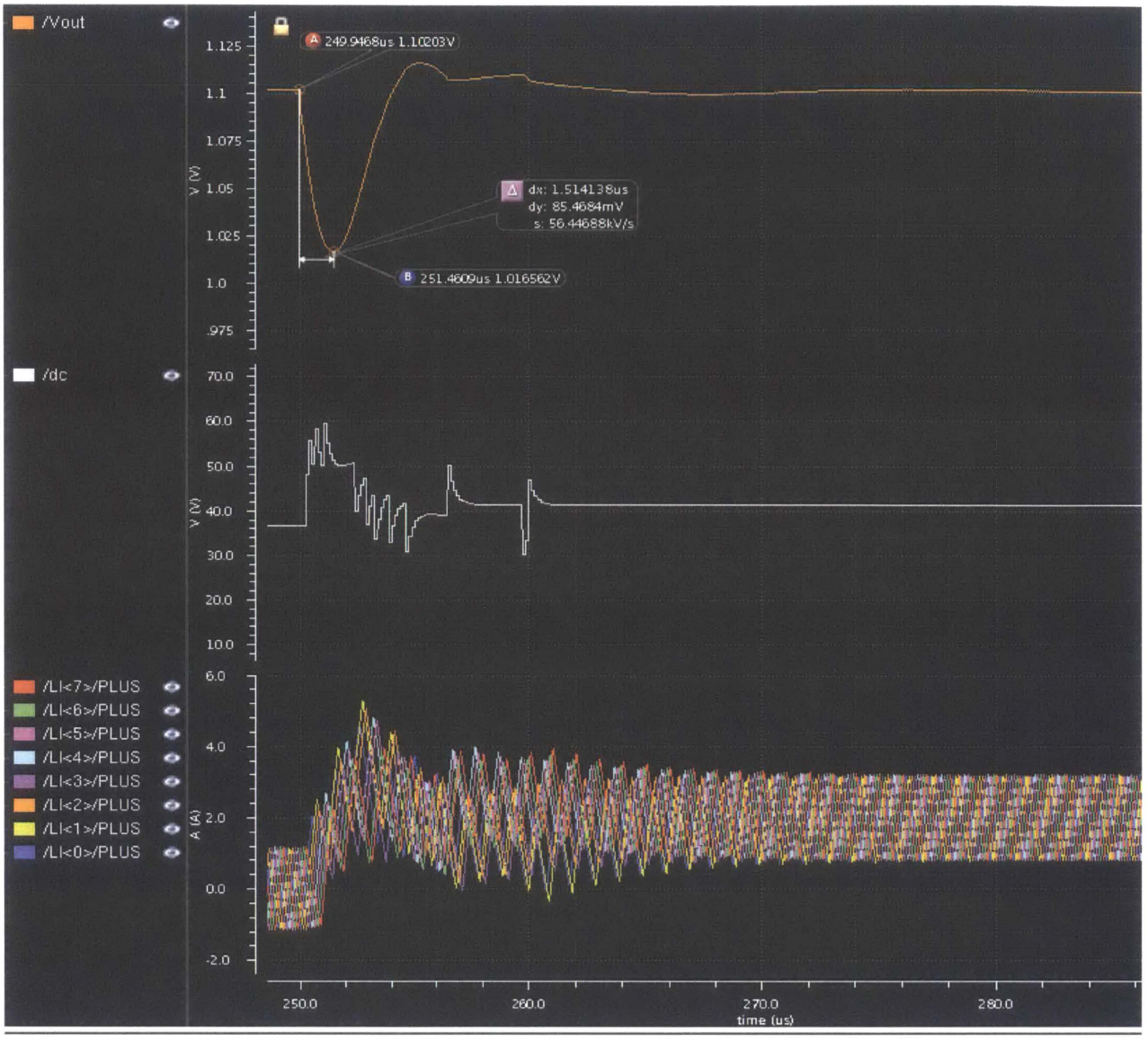


Figure 33: Load transient simulation with the advanced modulator and $G_{ca3}(z)$ a) Output voltage for 16A load step b) Duty cycle c) Inductor currents

Chapter 4 Performance Analysis and Comparison

The performance parameters obtained from simulations of the traditional and advanced modulator systems are summarized in Table 1.

ACHIEVED	Traditional			Advanced			Improvement*		
Compensator Design Method	**1**	**2**	**3**	**1**	**2**	**3**	**1**	**2**	**3**
Bandwidth	**22KHz**	**7.62KHz**	**7.65KHz**	**24.5KHz**	**9.06 KHz**	**157KHz**	1.11X	1.19X	20.52 X
Phase Margin	**64.3**	**88.8**	**90.4**	**73.1**	**92.9**	**44.5**	-	-	-
Rise time	**6.25µs**	**41.45µs**	**42.16µs**	**6.2µs**	**36.54µs**	**1.24µs**	1.008 X	1.134 X	34X
Vref step Vout Overshoot	**21.4%**	**0%**	**0%**	**9.74%**	**0%**	**18.05%**	-	-	-
Vref step Settling time (within zero error bin)	**44µs**	**74.18µs**	**73.04µs**	**24.04µs**	**62.08µs**	**20.75µs**	1.83X	1.19X	3.52X
Droop @16A step	**250.6 mV**	**252.4 mV**	**250.1 mV**	**237.3 mV**	**232mV**	**85.46 mV**	1.056 X	1.088 X	2.93X
Droop settling time (within zero error bin)	**81.76µs**	**60µs**	**70.28µs**	**74.31µs**	**64.04µs**	**9.76µs**	1.1X	0.94X	7.2X

*Improvement value is computed as a ratio of the traditional controller's result over the advanced controller's result

Table 1: Summary of simulations performance results for traditional and advanced controllers

Performance comparison within compensator types

The controller designed using Method 1 had a slightly better performance with the advanced modulator compared to the traditional modulator. Both controller systems had similar rise times around of 6.25µs and 6.2µs. The voltage droop was 237.3mV for the advanced controller but 250.6mV for the traditional controller which is a 1.056X improvement for the advanced controller. The settling times also improved from 44µs to 24.04µs which is a 1.83X improvement for the reference step, and from 81.76µs to 74.31µs

for the load step which is a 1.1X improvement. The speed and output droop improvements ratios obtained with this compensator type are around **1-1.83X** which is relatively small for a controller that takes advantage of interleaving in a multiphase converter with N = 8 phases through the advanced modulator.

The controller designed using Method 2 also had a slightly better performance with the advanced controller compared to the traditional controller. The rise time of 36.54μs was 1.134X faster than the 41.45μs rise time with the traditional controller. The voltage droop was 232mV for the advanced controller but 252.4mV for the traditional controller which is a 1.088X improvement for the advanced controller. The settling time also improved from 74.18μs to 62.08μs which is a 1.19X improvement for the reference step, but slightly degraded from 60μs to 64.04μs for the load step. The speed and output droop improvements obtained with this compensator type are around **0.94-1.19X** which is also small compared to the number of phases N =8. This controller therefore does not allow us to see the full benefits of the advanced modulator.

The improvement of the advanced controller is more visible with the compensator design Method 3. This design allows pushing the bandwidth much higher with the advanced modulator. The rise time of 1.24μs was 34X faster than the 42.16μs rise time with the traditional controller. The voltage droop was 85.46mV for the advanced controller but 250.1mV for the traditional controller which is a 2.93X improvement for the advanced controller. The settling times also improved from 73.04μs to 20.75μs which is a 3.52X improvement for the reference step, and from 70.28μs to 9.76μs for the load step which represents a 7.2X improvement. The speed and output droop improvements obtained with this compensator type are around **2.93-34X** which is significantly better compared to the

previous 2 designs. This compensator design allows us to see the benefits that the advanced modulator offers to increase the speed of transients in interleaved multiphase converters and reduce the size of the output capacitor in interleaved multiphase converters.

Performance comparison across all compensator types

The best compensator design method for the advanced modulator is Method 3, while the best design method for the traditional controller is Method 1. Comparing these two controllers, we still observe an improvement from the advanced modulator. The improvement is 5X in Vref step rise time, and 2.12X in step settling time, 2.93X in voltage droop, and 8.38X in droop settling time. These improvements range from **2.12-8.38X**, still demonstrating a significant benefit in using the advanced modulator. Overall, the advanced modulator does indeed improve the speed and performance of the transients, but the improvement is subject to the type of compensator used.

Chapter 5 Summary and Future works

In today's high-speed micro-processing applications, the voltage and load of micro-processors vary during operation. Such applications place a requirement on DC-DC converters to have a high-bandwidth that will allow excellent reference voltage tracking and load transient performance. Traditional single and multiphase converters have a speed limitation which is partly due to their slow update rate of duty cycle during transients. Given the potential multiphase converters present to reduce inductor and capacitor size requirements, and given their comparatively higher slew rates, we implemented an advanced modulator which takes advantage of the higher slew rates in multiphase converters buck converters by updating the duty cycle at the fast rate of $N \times F_{sw.}$ This advanced modulator operates without changing the per-phase switching frequency which helps maintain efficiency converters. Our goal was to assess the role of this advanced modulator in enabling the design controllers that achieve bandwidths that scale with $N \times F_{sw}$ rather than F_{sw} as is the case with traditional PWM-based controllers.

To assess the performance of the advanced modulator described in Chapter 2 we use a comparative approach in which the benchmark is a controller based on a traditional PWM modulator which updates duty cycle at the slower rate of F_{sw}. Three types of compensator are used to compare the two types of controller systems. For each compensator type, an assessment of the performance improvement due in the controller containing the advanced modulator is made using metrics such as rise time, settling time, and output voltage droop. This analysis, presented in Chapter 3, reveals that the advantages of the advanced modulator are indeed present and vary according to the type of

compensator used. All 3 compensator types showed an improvement in reference tracking speed and a reduction in voltage droop during load transients with the advanced modulator. The performance improvement with the advanced modulator was **1-1.83X** with Method 1, **0.94-1.19X** with Method 2 and **2.93-34X** with Method 3. Method 3 achieved the highest bandwidth and demonstrated the highest benefits in using the advanced modulator. Its compensator $G_{ca3}(z)$ helped achieve a **2.93-34X** improvement of transient parameters compared to compensator $G_{ct3}(z)$ for the traditional modulator. Method 3 also showed a **2.12-8.38X** overall improvement of transient parameters compared to the best design method for the traditional controller (Method 1). These results show that the magnitude of improvements in performance due to the advanced modulator has a magnitude that is subject to the type of compensator used but also the performance criteria under observation.

In future analyses exploring other compensator design methods could therefore enable to achieve higher bandwidths with the advanced modulator. More advanced linear and non-linear compensator design techniques could therefore make a greater use of the ability of the advanced modulator and achieve faster transients. As bandwidth increases, other challenges in the design of the controller will also need to be addressed. An observation of Figure 33c and Figure 30c also shows that with the highest bandwidth achieved with Method 3, the matching between the inductor phase currents degrades during transients. This issue arises at higher bandwidth as the duty cycle command changes more quickly. Solving this issue might require further modifying the algorithm used by the advanced modulator for better sharing of gate drive signals when the duty cycle changes rapidly. A more complex algorithm could be used to give turn-on priority to

phases that have been off for a longer period of time. Another possibility is to include current magnitude information in the controller and adjust gate drive signals using phase currents information. The phases with higher currents would therefore see their gate drive signal duration reduced. Finally, depending on the amount of mismatching or current imbalance present in the system, a current limiting algorithm could be sufficient simply to prevent inductor saturation. Implementing the modifications suggested would allow to achieve wide-bandwidths that scale with $N \times F_{sw}$ and obtain a more practical and robust converter.

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