Flat Panel Display Drivers With Printed Elements

by

Christopher T. Turner

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Electrical Engineering and Computer Science
at the Massachusetts Institute of Technology

July 23, 1997

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ABSTRACT

A new type of flat panel display is constructed using electrophoretic display material. A non linear backplane is used to implement matrix addressing of the display. Techniques for creating such a non linear backplane using electrically nonlinear ZnO varistors fabricated in a thick film, low temperature process are reported. Drive circuitry is combined with the printable varistor and electrophoretic display material to create a matrix addressed electrophoretic display. The resulting display has high contrast, consumes little power and can be manufactured in a low cost, additive process.

Thesis Supervisor: Joseph Jacobson
Title: Associate Professor, MIT Media Lab
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1 Introduction

1.1 Electronic Displays - Historical Perspective

The electronic display of information in a visually appealing manner has been the subject of much research in the past century. Although an incredible amount of progress has been made since the invention of the cathode ray tube in 1897 (Matsumoto, p. 3), there is still a need for significant improvement as we enter the next century. As applications demand that displays become thinner, lighter, higher resolution, and less expensive, the need for new technologies becomes apparent.

Fueled primarily by demand for portable computer displays, the class of electronic displays known as flat panel displays (FPDs) have become a multi billion dollar industry. Given the current demand for flat panel displays, the increasing popularization of computing, and the trend towards portable technologies, FPDs will become ever more important in years to come.

Table 1-1 (Matsumoto, p. 3) shows the history of electronic display technology and of important related inventions.

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1879</td>
<td>Invention of carbon filament incandescent lamp. (Edison, USA)</td>
</tr>
<tr>
<td>1888</td>
<td>Discovery of liquid crystals. (Reinitzer, Austria)</td>
</tr>
<tr>
<td>1897</td>
<td>Invention of cathode ray tube (CRT). (Braun, Germany)</td>
</tr>
<tr>
<td>1904</td>
<td>Invention of vacuum tube. (Fleming, Britain)</td>
</tr>
<tr>
<td>1935</td>
<td>World's first television broadcast. (Germany)</td>
</tr>
<tr>
<td>1936</td>
<td>Discovery of electroluminescent phenomenon in ZnS:Cu. (Destriaux, France)</td>
</tr>
<tr>
<td>1947</td>
<td>Development of transparent electrode glass. (Corning, USA)</td>
</tr>
<tr>
<td>1948</td>
<td>Invention of transistor. (Barden and others, USA)</td>
</tr>
<tr>
<td>1954</td>
<td>Publication of d.c. drive plasma display panel (PDP). (Skellet, USA)</td>
</tr>
<tr>
<td>1954</td>
<td>Announcement of GaP light emission phenomenon (Wolf and others, USA)</td>
</tr>
<tr>
<td>1958</td>
<td>Development of the NIXIE discharge display indicator. (Burroughs, USA)</td>
</tr>
<tr>
<td>1963</td>
<td>Publication of liquid crystal electrooptic effect (Williams, USA)</td>
</tr>
<tr>
<td>1963</td>
<td>Discovery of tungsten oxide electrochromic effect. (Jones, USA)</td>
</tr>
<tr>
<td>1967</td>
<td>Development of single digit vacuum fluorescent display (VFD). (Ike Denshi, Japan)</td>
</tr>
<tr>
<td>1968</td>
<td>Development of thin film a.c. drive electroluminescent display (ELD) (Bell Labs, USA)</td>
</tr>
<tr>
<td>1968</td>
<td>Implementation of GaAsP red light emitting diode (LED). (Monsanto, USA)</td>
</tr>
<tr>
<td>1972</td>
<td>Implementation of liquid crystal watch and calculator. (Muroma and Rockwell, USA)</td>
</tr>
<tr>
<td>1973</td>
<td>Publication of electrophoretic image display (EPID). (Matsushita Denki, Japan)</td>
</tr>
<tr>
<td>1978</td>
<td>Trial d.c. drive color PDP TV. (NHK, Japan)</td>
</tr>
<tr>
<td>1979</td>
<td>Trial VFD television. (Ike Denshi, Japan)</td>
</tr>
<tr>
<td>1979</td>
<td>Trial LED television. (Sanyo, Japan)</td>
</tr>
<tr>
<td>1982</td>
<td>Implementation of electrochromic display (ECD) clock. (Seiko, Japan)</td>
</tr>
<tr>
<td>1982</td>
<td>Development of low voltage, multicolor thin film ELDs (Osaka Univ., Japan)</td>
</tr>
<tr>
<td>1984</td>
<td>Implementation of color liquid crystal TV. (Seiko, Japan)</td>
</tr>
<tr>
<td>1995</td>
<td>Full color 12 inch active matrix LCD displays prevalent.</td>
</tr>
</tbody>
</table>

As the table illustrates, although many of the physical mechanisms underlying current display technologies were discovered early in the century, it is only recently that many of these technologies have appeared in commercial display products. The engineering of a display is a complex problem and there are many criteria that a technology must satisfy to make it an attractive candidate for a display. Similarly, while the electrophoretic display
is almost 25 years old, only recently has it become a viable technology for modern flat panel display applications.

This thesis presents developments related to current research in the area of electrophoretic image displays (EPID). Although EPIDs have been little more than a footnote in the annals of electronic display history, recent developments suggest that they may soon emerge as an important and widespread display technology.
1.2 Electrophoretic Displays

The display technology that this thesis deals with is the electrophoretic imaging display (EPID). The concept of the EPID was first introduced in 1973 by Ota (Ota, 1973, p.832). Original work done by Ota at Matsushita sparked significant research in the 1970s and early 1980s at companies such as Xerox, Exxon Enterprises and Philips. Although the technology failed to achieve commercial success, recent efforts have indicated that EPIDs may prove commercially feasible.

Electrophoresis is “the movement of suspended particles through a fluid under the action of an electromotive force applied to electrodes in contact with the suspension”. (Webster) A display unit which exploits this phenomenon is shown in cross section in Figure 1-1.

![Figure 1-1](image)

Small charged particles are placed in a dye of a contrasting color. This suspension is sandwiched between two conductive plates, one of which is transparent. As a field is applied across the two conductive plates, the charged particles are drawn to one plate and repelled from the other, depending on the polarity of the particles and the direction of the applied field. Thus, if negatively charged white particles are placed in a black liquid between two electrodes, the white particles will move to whichever plate is more positive. If this “pixel” is observed through the transparent plate, the display will appear white if the transparent electrode is more positive and black if it is more negative. By applying electric fields to specific areas of the suspension by means of patterned electrodes, a multi pixel electrophoretic matrix display can be created.

The resulting display offers many potential advantages in that it can be extremely thin, has good contrast, and consumes little power. In addition, the fact that the display is a reflective rather than emissive display is advantageous in terms of power and viewing angle. One of the key reasons that EPIDs may potentially consume little power is that the display material exhibits a bistability, or memory effect. Thus, power need not be applied continuously, but only to cause a pixel transition. In early research efforts, this memory effect was primarily attributed to attractive forces between the particles and electrodes. While this does create some bistability, it is not desirable to have the particles stick to the
electrodes. Current research suggest that bistability can be added to the display material by appropriately density matching the particles to the surrounding liquid.

Although EPIDs offer many advantages, there are some drawbacks. Our work has shown that EPIDs have little or no non linearity. The lack of a non linearity makes it difficult to address large matrices of pixels. Although it is possible that electrophoretic suspensions may be developed with a non linearity, there are few current prospects for this. Thus, a non linear element must be added to each pixel. While this is not desirable in terms of device complexity, it is a tractable problem. The focus of this thesis is largely on providing low cost materials and processes for constructing EPIDs with non linear elements. Approaches and results are detailed later in this document.

A second disadvantage of EPIDs is that relatively high voltages must be used to achieve fast switching times. Switching voltage can be reduced by increasing the charge of the particles, reducing the size of the particles, or by reducing the gap between the electrodes. While lower voltage EPIDs that switch quickly appear possible, the high switching voltage currently required must be regarded as a drawback.

In addition to the above, early research efforts unearthed some problems which led to the abandonment of research in EPIDs for some time. Primary failure modes observed in EPIDs were permanent sticking of particles to electrodes, aggregation of the particles, and particle migration. (Ota, 1977, p. 249). Current research efforts at the MIT Media Lab by Jacobson and Comiskey (Comiskey, p. 75) have been able to eliminate many of these problems by encapsulating an electrophoretic suspension in small, discrete microcapsules.

Thus, the display operates in essentially the same manner as described earlier. However, if the microcapsules can be made sufficiently small, the failure modes reported by Ota should be eliminated. That is, particles may not migrate, nor agglomerate if the capsules are chosen on a scale smaller than the scale of typical agglomerations. Sticking to the electrodes is also eliminated by encapsulation. While all problems have not been resolved, it seems likely that they will in the near future.

It should be noted that the development of encapsulated electrophoretic suspensions offers several new advantages not previously associated with EPIDs. Encapsulating the display material allows for the display to be manufactured entirely by a printing process. Standard techniques such as screen printing can be used to deposit microencapsulated electrophoretic display material which has been dispersed in a binder for printing (Comiskey, p. 75). In terms of lowering manufacturing costs, such a process offers great reward. Secondly, the printing of display material enables displays to fabricated on thin, flexible, arbitrary substrates (such as paper). This will enable entirely new applications of displays, such as electronic books and paper (Comiskey, p. 75).
Although the EPID has garnered little notice historically, the developments detailed above and later in this thesis indicate that the EPID is a viable flat panel display technology.
1.3 Advantages of Electrophoretic Displays

The flat panel display market is a hotly contested one. Thus far, liquid crystal displays (LCDs) have dominated. Despite this dominance, the LCD has several inherent shortcomings which will become more significant in the future. Thus there is an urgent need for new flat panel display technologies. Although there are many types of new flat panel technologies, most suffer from key drawbacks. The encapsulated EPID offers significant improvements over existing technologies in several areas:

• Power Consumption - Current 12.1” active matrix LCDs consume over 2.5 watts of power. This severely limits the battery life of modern portable computers. By eliminating the need for a backlight and active matrix backplane, it may be possible to reduce this power consumption to the milliwatt range in encapsulated EPIDs.

• Thickness and Flexibility - The display of a typical laptop computer is still nearly an inch thick. In addition, current technology does not address the need for flexible displays. Thin, flexible displays would enable the creation of entirely new products and technologies. For example, it would be possible to create electronic books and newspapers that maintain the traditional book/newspaper interface, but are able to dynamically display digital information.

• Emissivity vs. Reflectivity. - Almost all current FPDs are emissive displays. This property makes it difficult and tiresome to observe these displays for long periods of time (e.g. computer screens). This is one of the primary reasons that current FPDs consume large amounts of power. EPIDs offer good contrast at lower levels of power consumption.

• Viewing Angle - Current displays using liquid crystals also suffer from reduced contrast when they are not observed head on. There is a need for FPDs which are viewable over a wide range of angles, such as the EPID.

• Cost and Manufacturability - Although active matrix LCD displays are quite stunning in appearance, the cost for such technology has not yet dropped below the $500 level. (Werner, p.18) There is a need for high quality displays which can be manufactured at significantly lower costs. One especially large component of the current cost AMLCD manufacturing is the production of the thin film transistor (TFT) backplane required to drive the display. By eliminating the need for the TFT backplane and allowing for manufacture of displays by a printing process, the EPID offers significantly reduced cost.

It is clear that there is room for improvement in flat panel displays. This thesis will discuss the use of electrophoretic displays as a proposed solution to these problems. Specifically, the focus will be on low cost, printable structures which enable matrix addressing of an EPID.
2 Encapsulated Electrophoretic Display Material

2.1 Overview
Current research in my group has focused on two different types of electrophoretic display systems. The first is based upon the movement of negatively charged white particles in a black dye. This system is contained in a clear microcapsule. Figure 2-1b depicts a basic microcapsule of this type.

![Diagram of microcapsules with negatively charged white particles and positively charged black particles](image)

Figure 2-1

Depending upon the polarity of the applied field, the white particles migrate to cover one hemisphere of the capsule, thus changing the perceived color of the capsule.

The second system is based on negatively charged white particles and positively charged black particles in a clear microcapsule. Figure 2-1a depicts this system.

Because the particles are oppositely charged, they are drawn to opposite hemispheres when a field is applied. By reversing the polarity of the field, the particles can be made to migrate to the opposite electrode. In this manner the perceived color of the capsule can be changed from black to white.

Currently, microcapsule sizes are on the order of 200 µm. Particle sizes are approximately 10 µm. Electrode gaps have typically been 250-500 µm. In the near future it is likely that all of the above dimensions will be significantly reduced. This will increase switching times and decrease the voltage required to obtain reasonable response times. The display material as currently developed exhibits good bistability. This is largely due to surface interactions and density matching of the solutions.
2.2 Voltage requirements and Switching Time

For an electrophoretic solution with electrophoretic mobility $\mu$, the velocity of the particles is given by (Dalisa, p. 831).

\[ v = \mu E \]

Thus, the time required to complete a transition between colors is given by:

\[ t = \frac{L^2}{\mu V} \]

As will become apparent, the non linearity, or lack thereof, of these displays is critical to the construction of a large display. Figure 2-2 shows the theoretical time necessary for an electrophoretic pixel to switch from white to black as a function of applied voltage.

![Switching Time vs Voltage Graph](image)

**Figure 2-2**

The figure shows that the display material's switching time is essentially linear with voltage. This thesis presents methods that allow the material to be addressed in a large display despite this linear behavior.

In addition, relatively high voltages are required to achieve fast switching times. Voltage requirements can be lowered by decreasing capsule sizes and electrode spacing.
2.3 Electrical Model

A basic electrical model of an electrophoretic cell is shown in Figure 2-3.

![Diagram of electrical model with symbols C_{ep} and R_{ep}](image)

**Figure 2-3**

The cell is represented as a capacitance with an associated leakage resistance. This representation is adequate for modeling the behavior of electrophoretic elements in a matrix display. An important note is that optical switching does not correspond to the charging of the capacitance in the model. The optical response for a typical cell was given as a function of voltage in section 2-2.

Typical capacitances are on the order of 20-100 pf/in².

Typical leakage resistances are so large it is difficult to accurately measure them. In general they exceed 1 gigaohm.
3 Addressing Schemes

3.1 Direct Addressing

The most straightforward type of control for an electronic display is direct addressing. In this scheme the state of each display element is controlled directly via two electrodes. The simplest example is that of a single pixel. As has been previously stated, the optical characteristics of an electrophoretic pixel depend on the polarity of the voltage applied across the cell. Applying a positive voltage from the top electrode to the bottom electrode causes the electrophoretic pixel to appear to be a certain color. When the polarity of this voltage is flipped, the display cell changes color. Thus, a simple implementation of direct addressing corresponds to connecting addressing wires to the top and bottom electrodes of an electrophoretic pixel. These addressing wires can then be used to toggle the color of the display pixel. This is represented in Figure 3-1.

![Diagram of a single pixel with control wires, top electrode, and bottom electrode](image)

**Figure 3-1**

The display structure is effectively a capacitor. As the capacitor is charged to different polarities, the charged particles in the interior preferentially migrate to one plate or the other, changing the color of the display.

Although single pixel devices are often used to characterize the properties of the display material during the research stage, the end goal is usually to form some type of multi pixel display. Once again, direct addressing can be used in a simple extension of the single pixel addressing scheme. Here each pixel in the display has two electrodes (top and bottom) which are each connected to an addressing electrode. These addressing electrodes are in turn connected to voltage switching circuitry. The state of each pixel can be controlled independently via this switching circuitry by setting one electrode to 0 Volts and one to $V_{sw}$, or vice versa. This cause each pixel to see a net voltage across it of either $V_{sw}$ or $-V_{sw}$ volts, thus allowing the state of the pixel to be toggled.

This method of addressing is desirable in that each display element can be controlled independently, but it is a poor technique for large displays. A display of M rows and N columns has MxN pixels and 2xMxN addressing electrodes. As M and N increase, the
number of wires and switching transistors becomes prohibitively high. In addition, pixels that are in the interior of the display are difficult to wire to in such a system. Although direct addressing is not a suitable technique for large displays, there are some applications for which it is a good solution. Common examples include single pixel indicators (i.e. on/off indicators, fixed status messages) and seven segment displays. Seven segment displays, prevalent in digital clocks and watches, are easily implemented with direct addressing.

In using direct addressing there is a simple change that can be made that eases the requirements on the number of connections that must be made to each display element. Because the state of an electrophoretic pixel depends only on the polarity of the field applied across it, the elements of a multi pixel display can share one set of their electrodes in common.

For example, a conductive, transparent indium tin oxide (ITO) slide can be used as the common top electrode. This electrode is hard wired to a voltage of $V_{sw}$. Each of the seven bottom segments are constructed of silver ink, and serve as 7 distinct electrodes. These electrodes are connected via address wires to switching circuitry which allows them to be set at either 0 Volts or $2V_{sw}$ Volts. Thus, depending on the state of the rear electrodes, the electrophoretic display material sandwiched between the top and bottom electrodes sees a net voltage across it of either $V_{sw}$ or $-V_{sw}$. This means that the state of each of the seven pixels can be toggled.

The use of a common top electrode thus reduces the number of electrodes for a direct addressed matrix display to $(M \times N) + 1$. Although this is still unsuitable for large displays, it does help simplify the construction of those displays for which direct addressing is used. The key difference when using a common electrode is that 3 voltages (0, $V_{sw}$ and $2V_{sw}$) must be generated, as opposed to the 2 voltages (0 and $V_{sw}$) that must be generated when using two distinct electrodes per pixel. Note also that in such a system twice the voltage required to switch a pixel ($2V_{sw}$) must be generated, as opposed to $V_{sw}$. In most situations, these drawbacks are not significant enough to warrant not using a common top electrode.
3.2 Matrix Addressing

Because the feasibility of direct addressing does not scale well as the number of pixels increases, it is necessary to investigate the use of matrix addressing schemes. In general, matrix addressing refers to a scheme by which a display of M by N pixels can be addressed with M row electrodes and N column electrodes. A schematic of a display system using matrix addressing is shown in Figure 3-2. Such a system requires only M+N control electrodes, as opposed to (MxN)+1 electrodes for direct addressed display with common electrode.

![Figure 3-2](image)

Typically, such matrix addressed systems are addressed row at a time. This means that one row electrode is activated while the data for that row of the display is applied to the column electrodes. As the rows are cycled through, this process is repeated and the display thus reflects the image data. Such multiplexing does not typically hurt the visual characteristics of the display, if it performed on a fast enough timescale.

However, in order to implement a matrix addressing scheme, the display material must have a non linearity in its voltage transfer curve. Considering the case of a typical electrophoretic display will explain why. Assume first that the electrophoretic display material has a switching time that is linear with applied voltage, as was depicted in Figure 2-2.

Given such an electrophoretic material between two plates, row and column electrodes can be patterned onto the plates, orthogonal to each other. This display consists of 4 “pixels” in the areas where the row and column electrodes overlap each other - the areas in which the field will be applied. Also assume that the display assumes a color that is
either black or white; white corresponds to a positive field from row to column electrode and black to a negative field.

It is desired to write the following pattern on a display which is initially all black:

<table>
<thead>
<tr>
<th>Column 1</th>
<th>Column 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row 1</td>
<td>A-White</td>
</tr>
<tr>
<td>Row 2</td>
<td>C-Black</td>
</tr>
</tbody>
</table>

In a matrix addressed system the following steps would be taken to write this pattern:

1) Hold Row 1 electrode at a voltage of $V_o$
2) Hold Row 2 electrode at $V_o/2$
3) Hold Column 1 electrode at 0
4) Hold Column 2 electrode at $V_o/2$

Thus pixel A has a voltage of $V_o$ from row to column electrode. Pixels B and C have a net voltage of $V_o/2$ from row to column. Pixel D sees no net voltage. In an electrophoretic display this has the desired effect of changing pixel A to the white state. Since the electrophoretic display has no threshold characteristic, the $V_o/2$ voltage on pixels B and C will change the state of these pixels from black to white also. As can be seen from the linear transfer function shown in Figure 2-2, the only noticeable difference will be that these pixels will change less quickly due to the smaller field. This problem is commonly referred to as half-select. As explained earlier in this thesis, historically, there has been little observed threshold effect in electrophoretic displays. If it has existed it has occurred at low voltages. If a threshold effect is present at low voltages, a matrix addressing system works, however the response time of the cells is usually quite poor due to the small fields involved.

To illustrate how the non linearity enables matrix addressing to be used, consider the previous example, but assume that instead the display material possessed the transfer characteristic shown in Figure 3-3.

![Figure 3-3](image-url)
Note that the full select voltage $V_o$ lies in a portion of the transfer curve where the switching time is fast. The half select voltage $V_o/2$ lies on the portion of the curve such that the display material switches very slowly relative to the full select case.

Once again, it is desired to write the following pattern on a display which is initially all black:

<table>
<thead>
<tr>
<th>Column 1</th>
<th>Column 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row 1</td>
<td>A-White</td>
</tr>
<tr>
<td>Row 2</td>
<td>C-Black</td>
</tr>
</tbody>
</table>

The following steps would be taken to write this pattern:

1. Hold Row 1 electrode at a voltage of $V_o$  
2. Hold Row 2 electrode at $V_o/2$  
3. Hold Column 1 electrode at 0  
4. Hold Column 2 electrode at $V_o/2$

Once again pixel A has a voltage of $V_o$ from row to column electrode. Pixels B and C have a net voltage of $V_o/2$ from row to column. Pixel D sees no net voltage. Pixel A is changed to the white state. The $V_o/2$ voltage on pixels B and C will change the state of these pixels from black to white also. However, because of the nonlinearity of the transfer characteristic the pixels will take a much longer time to switch than pixel A. Thus as long as these pixels can be readdressed before they switch, there is no problem. It can be seen that such an addressing scheme scales easily to larger displays. This difference in switching time between fully selected pixels and half selected pixels essentially determines how many pixels can be addressed in the display without degraded optical characteristics.

As mentioned earlier, the current electrophoretic display material has an essentially linear voltage transfer characteristic. Although there are potential methods for creating an electrophoretic material with a non linearity, it has not been done to date.

Figure 3-4 shows two different schemes for addressing a material with a threshold. Figure 3-4a shows the 2V/1V scheme outlined above. Figure 3-4b shows a 3V/1V scheme. In this scheme, it is possible to ensure that no non selected pixels see a voltage greater than 1/3 of the full select voltage in magnitude.
This is done by holding unselected rows at 2/3 of the full select voltage and unselected 
columns at 1/3 of the full select voltage. (Tannas, p.108) This offers the benefits of being 
able to lower the full select voltage.

It should be noted that because electrophoretic cells require bipolar drive signals, only 
one set of image transitions can be made at a time. In addition, unlike liquid crystals, 
electrophoretic cells exhibit bistability and thus do not return to the "off" state after a 
certain period of time. In the example above, it was assumed that the display was initially 
all black. Thus only the pixels that are desired to be white were addressed. This issue can 
be dealt with in two ways in implementation. The first is a bulk erase of the material to 
one state before addressing begins. Thus, voltages can be applied such that the entire 
display is forced black or white, and then the necessary pixels are addressed. This has 
benefits when displaying images which do not change very often. However, it degrades 
the optical quality of the display when used with video or continuously scanned images.

A second method is to address the display row at a time, but to perform two passes, one 
for the black to white transitions, and one for the white to black transitions. The polarity 
of all voltages must be flipped in each phase. First, positive (column to row) voltages are 
alplied to cause the white transitions. Then polarities are flipped and negative (column to row) voltages are used to force the black transitions. The use of 1/2 and -1/2 voltages in 
respective phases ensures that unselected pixels do not change. This system could also be 
implemented using the 3V/1V scheme outlined earlier, with appropriately chosen 
polarities.

The schemes outlined above assumed that the display material had an intrinsic non 
linearity. An equivalent method for enabling a display to be matrix addressed is 
represented in Figure 3-5

![Figure 3-5](image-url)
In this system, a non linear element is placed in series with the display material. The non linear element is represented schematically as a pair of back to back diodes because the current voltage characteristic of two diodes in such a configuration has an appropriate non linearity.
A typical I-V curve for such an element is shown in Figure 3-6.

![Figure 3-6](image)

At voltages of small magnitude, the device essentially presents current from flowing. The electrodes of the display material are not charged, and the display will not change state. At large voltages above some threshold voltage the device begins to conduct and the display electrodes charge, thus changing the state of the display. The non linear element must be chosen such that the full select voltage lies in the conduction region, while the half select voltage lies in the cutoff region. It should be noted that it is important that the characteristic is symmetric. This is necessary because of the bipolar drive voltages required for electrophoretic devices.

Although the non linear element is represented here as a pair of diodes, it is not necessary that diodes be used in the actual device. Any element with a similar I-V characteristic is suitable.

A further improvement can be made to the system by adding an additional storage capacitor in parallel with the display cells of Figure 3-5. This is done to allow the use of a much shorter address time. (Chiang, p. 114). The optical response of the EP medium is fairly slow. The storage capacitor can be charged quickly and will hold the voltage long enough for the electrophoretic pixel to undergo the appropriate optical transition. Thus, the amount of time a pixel must be addressed for is determined by how long it takes to charge the storage capacitor, and is not limited by the slower optical response of the display material. In an early matrix addressed electrophoretic system address times were reduced to 20 us from 20ms by this mechanism. (Chiang, p.114).
It should also be noted that at voltages less than the threshold voltage, the non linear devices are not perfect insulators. A small leakage current flows. The magnitude of this leakage current must not be so large that the storage capacitors discharge via it before the display cell changes optically. In addition, the leakage current must be small enough that the storage capacitors of half selected pixels do not charge significantly during the address time of a pixel. Thus, ensuring that the leakage current is small guarantees good contrast. This is an important characteristic of the non linear element to be used.
4 Addressing Circuitry

4.1 Direct addressing circuitry

For display applications involving direct addressing, simple control circuitry can be developed. The basic scheme involves applying control voltages to each pixel individually as outlined in Figure 3-1 earlier.

As was mentioned in Section 3-1, all of the pixels of the display may share one of their two electrodes common electrode. This reduces the number of transistors required by N/2-1. However, this also cuts the voltage applied across each pixel in half. Consequently, switching speeds will decrease. Often this is an acceptable tradeoff. If it is not, the voltage can be increased to compensate.

A simple transistor switching circuit is shown in Figure 4-1.

![Figure 4-1](image)

This circuit has two drawbacks associated with the use of the pull-up resistors. The first consequence is that the resistors increase the time it takes to switch a display pixel. This occurs because the display material is modeled primarily as capacitor. Placing a resistor in series with it increase the charging time constant, thus reducing the response time. The second drawback of this circuit is that the resistors contribute a large amount of static power dissipation. When the transistors are on, unnecessary power is being dissipated in the resistors.
An alternative circuit is shown in Figure 4-2.

![Circuit Diagram](image)

**Figure 4-2**

This circuit again uses FETs. They are configured in a standard push pull configuration. If high voltage FETs are used, care must be taken to shift the levels of the control voltages appropriately. This ensures that the maximum allowed gate to source voltage is not exceeded. However, this requires additional transistors. The choice between the above two circuits involves a tradeoff between the circuit complexity and switching speed and voltage.

At the time of this writing, relatively high voltages are still required to quickly switch electrophoretic cells. Typical voltages are 200 to 300V. Although high voltage is required, very little current is drawn, and thus overall power consumption is still low. One circuit that was utilized to generate the high voltages required was a charge pump based design. This effectively converted a 5 VDC input to a 300 volt DC output. A full schematic is included in the appendix. While this is not directly related to this thesis, it is mentioned because of the widespread use it found in direct addressing of electrophoretic cells during the course of my research.
4.2 Matrix Addressing Circuitry

In order to implement the addressing schemes previously outlined, it is necessary to construct display driver circuitry. A block diagram of a typical display driver system is shown in Figure 4-3.

A microprocessor reads the image data from some input source. This image data is converted into appropriate control signals for the row and column switching circuitry. Control signals are shifted out through shift registers and applied to the row and column drivers.

The voltage levels and timing of the waveforms is dependent upon the switching time of the display material, display size, desired frame rate, and other display parameters.

The microprocessor and shift register circuitry are easily implemented using standard techniques.

The row and column drivers can take different forms. Matrix addressed electrophoretic displays require 3 level drivers. One level corresponds to the half select voltage, while the other 2 correspond to the 2 different polarities of the full select voltage.
A simple circuit which implements such a driver using FETs is shown in Figure 4-4 with the associated truth table.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Cell Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Low</td>
<td>+V</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
<td>0</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>+V/2</td>
</tr>
<tr>
<td>High</td>
<td>High</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 4-4

All devices shown are FETs which switch at logical levels. Because electrophoretic displays often require high drive voltages, the transistors should be chosen to have an appropriately high Vds breakdown voltage.

Once again, the use of resistors increases the switching time for a given voltage and increases static power dissipation.
An alternative circuit is shown in Figure 4-5.

![Figure 4-5]

This circuit again uses FETs in a push pull configuration. A third transistor is added at the output to provide the required third voltage level. Once again, when high voltage FETs are used, care must be taken to shift the levels of the control voltages appropriately. This ensures that the maximum allowed gate to source voltage is not exceeded. A simple level shifting circuit is shown in Figure 4-6.

![Figure 4-6]
The resistors in the level shifting circuit will increase the power consumption. More complex level shifting circuitry can be used if this is an issue. In general the push pull circuit is preferred over the simple circuit of Figure 4-4 because of the reduced power dissipation and faster charging time. Although transistor count is increased this is not usually a problem when integrated circuits are used.

As display sizes increase, it is necessary to achieve a high level of integration in the drive circuitry. Commercial parts available from vendors such as the Supertex incorporate the shift registers, 3 level push pull drivers, and low power level shifters in are relatively small IC package. Similar circuits can be custom developed to suit the exact requirements of the display.
5 Varistor Technology

5.1 Varistors - Background

Section 3.2 illustrated the need for a non linear element to permit the use of matrix addressing techniques for electrophoretic displays. This section presents methods used for previous electrophoretic displays and other display technologies.

Probably the most famous and widespread type of non linear element currently used in flat panel displays is the thin film transistor (TFT). The gate or controlling voltage is applied via the row electrode, while the power is provided by the column electrode. When both are active, the display material is selected. Thus the TFT serves as a switch which allows individual pixels to be selected by the row and column electrodes. Because the TFT essentially acts as a switch, it behaves as almost an ideal non linear element.

TFT research began in earnest in the 1960s and was pioneered by Brody. (Brody, p.114) Original TFT were based on a CdS material, although recently amorphous silicon has become the dominant TFT material. Polysilicon also has received some attention of late.

It should be noted that the TFT is a three terminal device, essentially behaving as an electrically controlled switch. The use of such a non linear element to address the display is known as active matrix addressing. Active matrix addressing has become the address method of choice for current color LCDs. Although it performs well, it has proven difficult to manufacture large substrates of TFTs with high yield. In addition, putting an active element on each pixel increases power consumption.

Another popular technology is metal insulator metal (MIM) devices. This consists of a thin layer of insulator sandwiched between two conductors. The insulator is usually Ta$_2$O$_5$ and is on the order of 1000-2000 angstroms thick. In such thicknesses, the device exhibits Poole-Frenkel conductivity. (Baraff, p. 200) Essentially, this corresponds to a highly non linear current-voltage characteristic. MIM devices were first used to multiplex LCDs by Baraff in 1980.

The MIM is a two terminal device that essentially behaves as a pair of back to back diodes. Thus it is a very good technique for enabling the matrix addressing of linear display materials. The main problem with MIM devices is yield. Because of the extremely thin insulator layer, pinhole defects are quite difficult to avoid. A single defect can render a display essentially unusable. Thus, the manufacturing process for MIM devices must be refined before the devices will see widespread use.

Various types of diode structures have also been used to address displays. Examples include PIN diodes, back to back amorphous Si diodes, and amorphous Si ring diodes. Although success has been reported, there have been problems with manufacturing uniform devices for large displays.
ZnO varistors have been used to successfully address both LCD (Castleberry, p.1123) and electrophoretic displays (Chiang, p.114). This thesis deals in part with the use of a new type of varistor process for electrophoretic addressing. Details of ZnO operation, results and problems will be explained later in this document.

All of the technologies listed above are suitable for addressing electrophoretic displays. However, one of the goals of this thesis is to provide a means for manufacturing an electrophoretic display with non linear backplane in a low cost, printable process. TFT and MIM devices are inherently thin film device, and are not suitable for a printing process. In addition, it is desirable to avoid the manufacturing yield problems that have been associated with these devices. The various diode technologies are applicable, however these are usually manufactured via a vacuum deposition process. This excludes them from consideration for a low cost printed non linear backplane. However, alternative thick film methods for diode construction are actively being researched. Finally, traditional ZnO varistors are traditionally not manufacturable via a printing process. Methods for achieving this are presented later in the document.
5.2 Varistors - Electrical Characteristics

A varistor is a two terminal passive electrical device which has a resistance that varies with voltage. In general a varistor has a highly nonlinear current-voltage characteristic. The I-V curve of a commercial varistor is shown in Figure 5-1.

![I-V Curve for Commercial Varistor](image)

Figure 5-1

It can be seen that the curve is exponential in nature. The varistor acts as a very good insulator before some breakdown voltage, $V_i$. At applied voltage above this breakdown voltage, the varistor becomes highly conductive. It should also be noted that the varistor I-V curve is basically symmetrical. Thus it is similar to the I-V curve obtained from two back to back diodes, as shown in Figure 5-2.

![Figure 5-2](image)
A simple electrical model for a varistor is shown in Figure 5-3. In display application the capacitance of the varistor becomes important and is thus shown. The resistance is a function of applied voltage.

\[ I = \frac{V^a}{k^b} \]

where \( k \) and \( a \) are constants.

The value of \( a \) essentially characterizes the steepness of the I-V curve in the nonlinear region. Si diodes typically have alpha values of approximately 35, while alphas between 35 and 100 have been reported for varistors. (Gupta, p. 1822).

The voltage at which the varistors begins to conduct is often referred to as the breakdown voltage. Typically this value is defined as the voltage at which the varistor passes 1 ma. A more suitable definition compensates for electrode area. As suggested by Gupta (Gupta, p. 1823), a good value is .5 ma/cm².

A final electrical characteristic of varistors which is important is the leakage current of the device. This is defined as the current which the device passes at voltages below breakdown voltage. For display applications the ratio of the current passed above breakdown and the leakage current will be an important parameter. It is desirable to have a very small leakage current.

Commercially varistors are used almost exclusively for overvoltage protection/transient suppression on line voltages. They are used to shunt power lines in case of large spikes. Thus most commercial varistors are able to absorb a great deal of energy. This specification is less important for display application because of the smaller currents involved.
5.3 Varistors - Physics

The true mechanism by which varistors work has been the subject of much research and debate. Varistors are traditionally fabricated by mixing a small amount of various dopants, such as Bi₂O₃, MnO, CoO, and Cr₂O₃ with a much larger percentage of ZnO (typically 98%+ by weight.). (Matsuoka, p.736-737) The resultant powder is then pressed and sintered at temperatures upwards of 1000 C. The sintering process cause a polycrystalline structure to form. Various studies have confirmed that the nonlinearity of a ZnO varistor is caused by interactions at the grain boundaries within the material (Gupta, p. 1819).

Various theories have been proposed for the actual mechanism. These included space charge effects, thin layer tunneling, and Schottky barrier effects. (Gupta, p. 1819)

Thin layer tunneling is an effect which is explained by a quantum mechanical argument. As an electron approaches a barrier there is a probability based on the thickness of the layer and the barrier energy that the electron will be able to tunnel through the barrier. As the barrier layer becomes very thin the probability increases and a tunneling current can be observed. Tunneling is the source of the electrical non linearity in MIM diodes. (Lerner, p. 1307).

Matsuoka (Matsuoka, p.744) theorized that a space charge limited current flows through the segregation layer of the varistor boundary because the segregation layer in ZnO varistors is essentially an insulator with many traps. The basis of this was that space charge limited current flows in other insulators with traps at a field strength of 10,000 V/cm which roughly matched what was found in his varistors.

Schottky barrier effects relate to an energy barrier which is setup at the interface of two different materials. The height of this energy barrier depends on the work function of the two materials. Electrons crossing the interface must overcome this potential barrier in order for current to flow. (Trigg, p. 575)

It is still not clear exactly which theory best describes the mechanism, but a Schottky barrier effect is regarded as the most likely candidate.

Internally varistors are comprised of small grains (typically 15-20 um). Because the nonlinearity of the bulk varistor comes from interactions at these grain structures, the grains can be thought of as the smallest useful unit of varistor material. A breakdown voltage can be associated with each grain in a device. The value of this voltage depends on dopants, dopant levels, sintering time and grain size. Typical values are less than 5 volts per grain boundary. Thus, the breakdown voltage for the bulk varistor can be controlled by controlling the thickness of the device. Thicker device have more grains through which the current must pass, and thus have higher breakdown voltages.
5.4 Varistors - Standard Fabrication and Results

Although the eventual goal was to produce varistors in a low temperature process, traditional methods of fabricating varistors were first attempted. The basic process used to create the varistors from was:

1) Press powder into disc at pressures of > 3kN.
2) Sinter at 1200 C for 1 hour.
3) Cool to 600 C in oven.
4) Quench to air.

Various powder compositions were tested:

A) .5 mole% MnO
   .5 mole% Bi₂O₃,  
   99 mole% ZnO

B) .5 mole% MnO
   .5 mole% Bi₂O₃,  
   .5 mole% CoO  
   98.5 mole% ZnO

C) .5 mole% MnO
   .5 mole% Bi₂O₃,  
   .5 mole% CoO  
   .5 mole% Cr₂O₃  
   98 mole% ZnO

D) .5 mole% MnO
   .5 mole% Bi₂O₃,  
   .5 mole% CoO  
   .5 mole% Cr₂O₃  
   .5 mole% Sb₂O₃  
   97.5 mole% ZnO

Results from these experiments were mixed. The measure of device quality that was used in these experiments was to measure the device current at one voltage and then measure the current at twice the first voltage. The size of this ratio gives an indication for how nonlinear the device is and also indicates its usefulness for matrix addressing systems (because of the half select nature of the addressing scheme). This ratio was computed for various voltages and the best ratio obtained was used as the final measure of device quality.
<table>
<thead>
<tr>
<th>Powder</th>
<th>Best Current Ratio at V and .5V</th>
<th>V used (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.51</td>
<td>180</td>
</tr>
<tr>
<td>B</td>
<td>4.02</td>
<td>240</td>
</tr>
<tr>
<td>C</td>
<td>2.67</td>
<td>160</td>
</tr>
<tr>
<td>D</td>
<td>3.45</td>
<td>190</td>
</tr>
</tbody>
</table>

As the table shows, while nonlinear devices with varistor like characteristics were fabricated, the results were not ideal. Although devices which passed greater than 4 times the amount of current were produced, this effort falls well short of commercially available products which are similar in nature. In addition, it would probably not be wise to give too much weight to the numbers above because control of process parameters was not strict enough to obtain very repeatable results.

Breakdown voltage and degree of nonlinearity varied significantly between devices. This is most likely due to the fact that the various process parameters were not controlled strictly enough. Pressed thickness and heating and cooling rates (which control grain size) were not precise enough. Because suitable devices were available commercially which gave the desired results, this series of experiments was not pursued further.
5.5 Low Temperature Printable Varistors - Methods

Because the goal is to make a non linear printable material, traditional methods of varistor fabrication are not suitable. The high temperatures involved (> 1000 C) eliminate the possibility of constructing a display on a wide variety of thin flexible substrates. In order to overcome this problem, the following process was attempted:

1) Obtain varistor wafers by traditional means (as outlined previously).
2) Pulverize varistor wafers into particulate matter.
3) Sieve particulate matter to obtain particles of the appropriate size.
4) Disperse particulate varistor material in a suitable binder for a printing process.
5) Print the varistor ink and cure at a low temperature.

First, commercial varistor wafers were obtained from the Maida corporation. These varistors have a grain size of 15 um on average and a breakdown voltage of 6.2 volts per grain boundary. These varistors were ground using a small grinder outfitted with a stainless steel blade. Standard sieves were used to separate the resulting material into various sized powders. The belief is that the ground varistor particles must be greater in size than the average grain size, since the nonlinearity is a result of grain boundary interaction.

The particles were then dispersed in one of two binders, a vinyl from Acheson and a polyester from Acheson. The vinyl binder is traditionally used in silver inks and has some conductive properties of its own. The polyester is a very good insulator when cured. Both binders cure at approximately 107 C for 15 minutes. The particles were mixed into the binder to form a printable paste. The ink was then drawn down on top of a bottom copper tape electrode using a straightedge and a 4 mil thick piece of Mylar with a cutout. After curing, a top copper tape electrode was applied.

The current voltage characteristics of the resulting printed varistors were then analyzed.
5.6 Low Temperature Printable Varistors - Results

The results of the printed varistor work is summarized below. Once again, the device quality is measured by calculating the ratio of the currents through the device at some voltage \( V \) and .5V for the \( V \) which yields the highest ratio.

<table>
<thead>
<tr>
<th>Particle Size</th>
<th>Binder</th>
<th>Best Current Ratio (at ( V ) and .5V)</th>
<th>( V ) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;25 um</td>
<td>Vinyl</td>
<td>1.00</td>
<td>300</td>
</tr>
<tr>
<td>25-106um</td>
<td>Vinyl</td>
<td>6.81</td>
<td>280</td>
</tr>
<tr>
<td>106-150um</td>
<td>Vinyl</td>
<td>33.92</td>
<td>320</td>
</tr>
<tr>
<td>&lt;25 um</td>
<td>Polyester</td>
<td>1.00</td>
<td>300</td>
</tr>
<tr>
<td>25-106um</td>
<td>Polyester</td>
<td>57.47</td>
<td>340</td>
</tr>
<tr>
<td>106-150um</td>
<td>Polyester</td>
<td>1051.23</td>
<td>300</td>
</tr>
</tbody>
</table>

An I-V curve from one of the best devices is shown in Figure 5-4.

![I-V Curve for Printed Varistor](image)

Figure 5-4

The polyester binder varistors had better results in general. As predicted, varistors formed with powders less than 25 um had little non linearity. In addition, varistor between 25 and 106 um performed poorer in general than larger particles. It is likely that these particles had fewer grain boundaries intact after the grinding process. Adequate results were obtained by using particles greater than 106 um in size.

The devices fabricated with the larger (> 106 um) particles worked well and showed very good stability over time. Device thickness must be controlled very carefully to ensure uniformity of breakdown voltage between devices. This proved to be the most difficult problem to control, but better printing technologies would allow for greater control over
the thickness of the resulting device.
5.7 Low Temperature Printable Varistors - Future Work

Although these initial results are promising, there is much characterization that needs to still be done. The resulting particles structure should be analyzed in terms of packing density. A different binder may produce a tighter packing of particles, thus helping improve threshold uniformity across devices.

Particle size effects should be further analyzed to determine if there is any way in which smaller particles can be used. Related to this is the idea of using varistors with smaller grains.

Finally, various grinding techniques and their effect on device performance (contamination) should be analyzed.
6 Display System with Printed Varistors

6.1 System Overview

The aforementioned technologies can be combined to produce an all printed display system. The display system is basically described by the block diagram of Figure 4-3. The various layers of the display are shown in Figure 6-1.

The heart of the system is a layer of microencapsulated electrophoretic display material (Figure 6-1e). This layer has been printed on a glass substrate (Figure 6-1a) on which silver ink row electrodes (Figure 6-1b) and particulate varistor material (Figure 6-1c) have been printed. The varistor material consists of commercial varistor wafer which has been ground by the aforementioned method and sieved to obtain particle sizes between 106 and 150 um. The resulting powder is dispersed in a polyester binder. Figure 6.1d depicts squares of printed silver ink. These are placed on top of the varistor layer. They are intended to make the capacitance of the varistor smaller than the capacitance of the display by altering the area of each. Top column electrodes (Figure 6-1f) are then applied using strips of ITO coated polyester. Alternatively these could be printed using an indium tin oxide ink. The display is shown in cross section in Figure 6-2.
To simplify the switching circuitry a basic 3 level driver of the type as was shown in Figure 4-4 is used to drive each row and column electrode. Data is presented to the switching transistors via shift registers. A full schematic is given in Appendix A.
6.2 Electrical Model of the System and Simulation

The electrical model for the system comprised of the driving circuitry, varistor and display cell is shown in Figure 6-3.

```
\begin{figure}
\centering
\includegraphics[width=\textwidth]{figure6_3}
\caption{Figure 6-3}
\end{figure}
```

It should be noted that this model is the model for the circuit when the varistor is its relatively non conducting region. For the purpose of circuit analysis, the varistor is modeled piecewise linearly, as shown in Figure 6-4.

```
\begin{figure}
\centering
\includegraphics[width=\textwidth]{figure6_4}
\caption{Figure 6-4}
\end{figure}
```
Thus the varistor is modeled as one of two resistances, depending on the region we are in. While this is not a perfect model, it is sufficient for the purpose of circuit analysis. Ideally, the resistance in the conducting region, $R_{vb}$ will be much greater than the resistance in the nonconducting region, $R_{va}$. Given this model for the varistor, a model for the complete circuit when the varistor is conducting is shown in Figure 6-5.

![Figure 6-5](image)

The model of Figure 6-3 will be analyzed first. After the analysis is complete it is fairly easy to understand the model of Figure 6-5.

We are interested in seeing how the voltage across the display cell, $V_d$ changes with time for various input levels, $V_b$. In practice the input $V_b$ will look somewhat like a square wave; there are 3 levels that $V_b$ can assume and transitions between levels are made instantaneously. This is modeled by a voltage source in series with a switch. Given initial conditions on $V_d$ and $V_v$ we can completely describe the response of $V_d$ to various input stimuli.

The first step is to determine the differential equation that describes the relationship between $V_d$ and $V_b$. This is done using impedance methods. The transfer function from $V_b$ to $V_d$ is given by:

42
\[
\frac{V_d}{V_b} = \frac{\frac{1}{s C_d} R_d}{\frac{1}{s C_d} + R_d + \frac{1}{s C_v} R_v + \frac{1}{s C_v} R_v a + R_n}
\]

This simplifies to:

\[
\frac{V_d}{V_b} = \frac{D s + E}{s^2 + B s + C}
\]

with:

\[
B = \frac{1}{R_v a C_v R_n} + \frac{1}{R_d C_d R_n} + \frac{1}{R_n C_d} + \frac{1}{R_n C_v}
\]

\[
C = \frac{1}{R_n C_d R_d C_v R_v a} + \frac{1}{R_n C_d C_v R_v a} + \frac{1}{R_n C_d R_d C_v}
\]

\[
D = \frac{1}{C_d R_n}
\]

\[
E = \frac{1}{R_v a R_n C_v C_d}
\]

This describes the following differential equation:

\[
\frac{d^2 V_d}{dt^2} + B \frac{dV_d}{dt} + C V_d = E \frac{dV_b}{dt} + F V_b
\]

The solution to this differential equation for a DC input level \( V_b \) after the switch is closed is given by:
\[ V_d = K_1 e^{s_1 t} + K_2 e^{s_2 t} + (E/C)V_b \]

where

\[ K_1 = \frac{1}{R_n C_2} \left( V_b - V_{init1} - (1 + \frac{R_{n}}{R_2})V_{init2} \right) - s_2 V_{init2} + s_2 \frac{E}{C} V_b \]

\[ K_2 = V_{init2} - K_1 - \frac{E}{C} V_b \]

\[ s_1 = \frac{-b + \sqrt{b^2 - 4ac}}{2} \]

\[ s_2 = \frac{-b - \sqrt{b^2 - 4ac}}{2} \]

with \( V_{init1} \) and \( V_{init2} \) being the initial conditions of the two state variables.

\( V_v \) is thus given by

\[ V_v = V_b - V_d(1+(1/R_d)) - C_d s_1 K_1 e^{s_1 t} + C_d s_2 K_2 e^{s_2 t} \]

While these expressions appear complex, the behavior of the system is easily described. Assuming that both capacitors initially have no voltage across them, when the switch is closed, a current equal to \( V_b/R_n \) flows. Thus the two capacitors charge up very quickly to a level determined by the ratio of their capacitances. The voltage on \( C_q \) is \( V_b/(C_q/(C_v+C_d)) \) while the voltage on \( C_v \) is \( V_b/(C_q/(C_v+C_d)) \). The capacitors are charged to this voltage with a time constant approximately equal to \( R_n(C_q||C_d) \). This assumes that \( R_n \) and \( R_d \) are much larger than \( R_m \), which is almost always the case. Typical capacitances are on the order of tens of pf. \( R_n \) is determined by the type of switching circuitry used and is usually very small. Thus the time constant is usually much smaller than 1 us and the capacitors essentially charge instantaneously to their values.

After these initial values have been reached, a second charging/discharging takes place. Whichever capacitor has a smaller shunt resistance will eventually have no voltage across it. Consequently, the capacitor with the larger shunt resistance will have all of the voltage across of it. Because the leakage resistance of the display cell is huge, it will almost always be larger than the off resistance of the varistor. Thus, given enough time the display cell will have all of the voltage across of it. While this result is not desirable it can be dealt with by ensuring that the capacitors reach these voltages very slowly. The time constant with which these capacitors charge to these voltages is determined by the
smaller resistance, which in this case is $R_{va}$. By ensuring that this resistance is large enough, charging to these steady state levels can be made extremely slow.

This analysis leads to several design rules. Keep in mind that this analysis is for when a half select voltage is applied to a pixel and it is desired to prevent the pixel from changing.

1) $C_v$ must be much smaller than $C_d$. This ensures that during the initial fast charging, most of the voltage appears across the varistor. Thus the display does not see any significant initial voltage and no optical transition ensues.

2) $R_{va}$, the off resistance of the varistor, should be very large. Thus, while the display cell will eventually end up with all of the voltage across it, the charging will occur on a slow enough timescale that the pixel in question will be readdressed before it has time to change.

3) $V_b < V_r$. $V_b$, the half select voltage, must be chosen to ensure that the varistor is in a regime such that rule 2 is obeyed - the varistor resistance at this value must be very large.

Now consider the case where the varistor has enough voltage across it to be in its conducting regime. This corresponds to the scenario where the full select voltage $V_a$ is applied to the system with the intention of switching a certain pixel. In this case the key difference is that the varistor has a constant drop across it of $V_r$. Also the resistance $R_{vb}$ is typically very small here (<10 kilohms). The result on the display is similar to before. There is a near instantaneous charging of the capacitors, during which the varistor enters its conducting region. After, there is a secondary charging. After a charging time the varistor will have only its threshold voltage $V_r$ across it. The display cell will have the total voltage $V_a - V_r$ across it. In this scenario, this is a desirable result. While this is similar to what happened in the half select case, it happens on a much faster timescale. This is because the charging time is dominated by the resistance, $R_{vb} + R_{a}$. Typically this time constant be several orders of magnitude smaller than in the half select case where the charging occurred through the off resistance $R_{va}$. Thus the display pixel will charge orders of magnitude more quickly to its final voltage ($V_a - V_r$) than it did in the prior case to the half select voltage $V_b$. This illustrates how the nonlinear change in the resistance of the varistor allows the charging of a pixel to be controlled. Several more design rules arise from this situation. (the scenario where the full select voltage is applied with the intention of switching a pixel)

4) $V_a$ must be greater than the threshold of the varistor device, $V_r$.

5) $V_a - V_r$, the resultant display voltage, must be large enough to cause an optical transition in the desired amount of time.
6) $R_v + R_n$, the on resistance of the varistor plus the source resistance, should be much smaller than $R_v$, the off resistance. This ratio essentially determines how many rows a display can have.

Thus for a display, the time spent addressing a particular row, $T_{row}$, is determined by the capacitance of the display elements and the source resistance plus the varistor on resistance. If $T_{full}$ is $(R_v + R_v)C_d$, the $T_{row}$ should be $\geq 5T_{full}$. The number of rows in the display is in turn determined by the charging time given by the display capacitance and the off resistance of the varistor. These values determine the $T_{half} = C_d * R_v$ time constant. A pixel in a given row may be charged to the half-select voltage $V_b$ for a total time of $(M-1)T_{row}$. Thus, it must be ensured that during the time $(M-1)T_{row}$, the half selected pixels do not charge to a voltage significant enough (essentially determined by the $T_{half}$ time constant) to cause an optical transition. Thus the size of the resultant display (number of rows) is essentially determined by the ratio of the varistor off resistance to the varistor on resistance. This results in a final design rule, which is closely related to rule 6.

7) $(M-1)T_{row} \ll T_{half}$, with $T_{row} = 5(R_v + R_v)C_d; T_{half} = R_v C_d$

An example will illustrate the use of these design rules. Assume a varistor with a capacitance of 1 pf and a display cell with a capacitance of 100 pf. Next, assume a half select voltage of 150 V and full select voltage of 300 V with corresponding varistor resistances of 100 kilohms and 1 gigaohm, respectively. Thus to fully charge a full selected pixel requires $5*100pf*100kilohms = 50$ us. The time constant which charges the half selected pixels cells is given by $100pf*1 gigaohm = 100 ms$. This means that half selected pixels will be fully charged in approximately 500 ms. In this case half selected pixels change 10,000 times more slowly than full selected pixels, yielding a theoretical display size of 10,000 rows. This number is not achievable due to the slower optical transition of the display material. If the material switched in 10 ms, 50 rows would be possible. This number could be increased by using storage capacitors. It should be noted that it was assumed that the capacitance of the varistor was much smaller than the capacitance of the display cell. This must be true for any display constructed. Otherwise half selected pixels will charge almost instantaneously. (see figures on next page)

This example shows the general rules for designing a display of this type

1) Ensure that the varistor capacitance is much smaller than display capacitance.

2) Given #1, theoretical display size is essentially determined by the ratio of the current passed by the varistor at the full and half selected voltages.

3) Response time of display material will probably limit display size, although storage capacitors can be used to improve this.
A MATLAB simulation of the system was created. Full code is in appendix C. This simulation enables one to design a display based on the specifications of a given varistor and display material. The simulation was compared to actual results by using standard resistors and capacitors and was found to be quite accurate.

The results of the simulation are shown for two different cases on the next page. These plots illustrate the effects of the relative capacitances of the varistor and display cell. In the first plot the varistor has a capacitance which is 1000 times smaller than the display cell. In the second plot the two elements have equal capacitances. The voltage applied to the system switches between -100 and 100 every 50 ms.

The simulation shows that when the capacitances are equal, the voltage is divided evenly between the two elements. Because this is meant to simulate the non conducting state of the varistor (the half select case), this is not desirable. It means that even though the varistor is not passing much current, the display cell is still seeing a large voltage because of the ratio of the capacitances. This is undesirable because the pixel is supposed to be half selected and a transition should not occur.

The first plot shows the effect of reducing the varistor capacitance relative to the display cell. In this case the display cell sees a very small voltage when the input waveform makes a transition. The display cell will eventually end up with all of the input voltage across it (given enough time) because it has a smaller leakage current, but this can be dealt with by appropriate choice of addressing times. The simulation is intended to analyze what happens at the input voltage transition. It shows that the varistor capacitance must be made smaller to ensure that half selected pixels do not change.
Figure 6-6: Varistor Capacitance = 1/1000 of Display Capacitance

Figure 6-7: Varistor Capacitance = Display Capacitance
6.3 Display Testing and Results

A display was constructed as outlined in section 6.1. The display consisted of two printed silver row electrodes on glass. On top of this a UV curable dielectric layer was printed. Holes were left in this layer for four varistor pads, each approximately .5 cm on a side. These holes were filled with a varistor mixture consisting of a polyester binder and ground commercial varistor wafer which was sieved to obtain 106-150 um particles. Large (2 cm on a side) silver pads were printed on piece of flexible polyester. This piece was inverted with the silver down, on top of the varistor. The goal was to create an intermediary electrode that would reduce the varistor capacitance relative to the display capacitance. Electrophoretic display material, sandwiched between two pieces of polyester, was the next layer. Finally, two thin indium tin oxide coated glass slides were used as top column electrodes. The resulting structure was intended to be 2x2 matrix addressed electrophoretic display.

Using driving techniques described earlier, the display was tested. Unfortunately the display exhibited a relatively high degree of cross coupling. The result was that half selected pixels changed state, although the varistor was intended to prevent this effect. Although this was discouraging, further inspection of the system revealed that the effect was due to improperly ratioed capacitances. Although an intermediary layer was used to attempt to reduce the capacitance, the fabrication of the structure resulted in capacitances that were close in magnitude. This was caused by undesired coupling between the row electrodes and the large silver pads (through both the varistor and dielectric layer). This issue should be eliminated by more careful design of the printed structure. It was encouraging to note that the varistor material acted as an electrode for the display material. With the silver pads removed, the display changed state only where the varistor material was present. This showed that the varistors were conducting when they were supposed to. The varistor were tested for non linearity and all devices showed good non linearity. Thus it was not the varistors that were at fault. It was improper design of the layout which led to cross coupling.

To demonstrate that the varistors did introduce a non linearity which enabled matrix addressing, a second system was created. This time 4 discrete varistors were created on glass slides, using copper tape as the electrode material. In addition, 4 discrete electrophoretic test cells were used. Capacitances were measured and were found to average 18 pf for the varistors and 200 pf for the display cells. This ratio was achievable because the area of the varistors was made significantly smaller than the area of the display cells. The cells and varistor were wired in a standard matrix addressing configuration. The system was driven with appropriately scaled and timed waveforms and the display was successfully matrix addressed. Each of the 4 pixels could be individually controlled without any significant cross coupling in the other pixels.

This experiment demonstrates the feasibility of low temperature thick film methods for creating devices which enable electrophoretic displays to be matrix addressed. In the
current setup, the achievable display size is limited primarily by the optical transition time of the display material. Based on the design rules presented earlier and the characteristics of the varistors I created, displays with up to 15 rows could most likely be created. The use of storage capacitors and more careful design of the varistor/display cell layout could result in displays with greater than 100 rows.

This system presents several key advantages over traditional displays. While the advantages of the electrophoretic display material itself have already been presented earlier in this document, the method of manufacture of the display has advantages as well. All components of the display could potentially be the result of an additive printing process: electrodes, non linear backplane and display material. This reduces cost and complexity dramatically. Significantly, a viable, low cost, high yield, low temperature type of non linear backplane has been presented. Further it has been shown that this backplane allows electrophoretic display to be matrix addressed.
References


Appendix A: Drive Circuitry Schematic

The schematic for the matrix addressing driver is shown below. The microprocessor is a PIC16C84. 74HC595 shift registers are used to apply the data to the Supertex AN0132 high voltage transistor arrays. The high voltage is generated by a Durel D353. All unmarked resistors are 10 megaohms.
#include "c:\pic\examples\16c84.h"
#fuses xt,nowdt,noproduct,par

#define RCK PIN_A4
#define SCK PIN_A3
#define SER PIN_B2
#define G PIN_B3 //active low

#define ONT 300
#define WAIT 500
#define OFFT 500

#define LOW 0
#define HIGH 1
#define HALF 2

#define ROWS 2
#define COLS 2

//first ROWS electrodes (0 to ROWS-1) go to the rows, next COLS to columns

//each shift reg of form :abdefgh
//pairs control output lines
//truth table for pair ab:
//   a  b  out
//   -  -  ----
//   0  0  V
//   0  1  V/2
//   1  0  0
//   1  1  0

void shift(int b);
void shift4 (int b1, int b2, int b3, int b4);

void map(int line, int state);
void clr_display (int sel);
//void disp_image (void);
//void hsel(void);

int d1, d2, d3, d4;
int pic[ROWS][COLS];

void main() {
    int i;

    output_low(RCK);
    output_low(SCK);
    output_low(SER);
    output_low(G);
}
// image:
// 0
// 0 1

// clr_display(1);
// delay_ms(2000);

while (1) {

    // clr_display(1);
    // delay_ms(1000);
    // clr_display(0);
    // delay_ms(1000);

    for (i=0; i<5; i++) {
        clr_display(0);
        delay_ms(OFFT);

        // 0 white
        // 1 red
        // 2 black
        // 3 green

        map(0,HIGH);
        map(1,HALF);
        map(2,LOW);
        map(3,HIGH);

        shift4(d1,d2,d3,d4);
        delay_ms(ONT);

        // map(0,LOW);
        // map(1,LOW);
        // map(2,LOW);
        // map(3,LOW);
        // shift4(d1,d2,d3,d4);
        // delay_ms(WAIT);
    }

    for (i=0; i<5; i++) {
        clr_display(0);
        delay_ms(OFFT);
        map(0,HIGH);
        map(1,HALF);
        map(3,LOW);
        map(2,HIGH);
        shift4(d1,d2,d3,d4);
        delay_ms(ONT);
    }
}

for (i=0; i<5; i++) {
    clr_display(0);
}
delay_ms(OFFT);
map(1,HIGH);
map(0,HALF);
map(2,LOW);
map(3,HIGH);
shift4(d1,d2,d3,d4);
delay_ms(ONT);
}

for (i=0; i<5; i++) {
clr_display(0);
delay_ms(OFFT);
map(1,HIGH);
map(0,HALF);
map(3,LOW);
map(2,HIGH);
shift4(d1,d2,d3,d4);
delay_ms(ONT);
}

//void hsel (void) {
// int m, n;

//for (m=0; m<ROWS; m++)
//map (m, HALF);

//for (n=0; n<COLS; n++)
//map(n+ROWS,HALF);
//
//shift4 (d1,d2,d3,d4);
//}

void clr_display (int sel) {
int m, n;

//clear display
for (m=0; m<ROWS; m++) {
    if (sel==1)
        map (m,HIGH);
    else
        map(m,LOW);
}
for (n=0; n<COLS; n++) {
    if (sel==1)
        map (n+ROWS, LOW);
    else
        map(n+ROWS,HIGH);
}

shift4(d1,d2,d3,d4);
}
/*void disp_image() {
    int m, n, k;

    //display image
    for (m=0; m<ROWS; m++) {
        //half select unselected rows
        for (k=0; k<ROWS; k++)
            if (k!=m) map (k, HALF);

        //low select active row
        map (m,LOW);

        //apply data to columns (opposite image sense form beginning erase)
        for (n=0; n<COLS; n++) {
            if (pic[m][n]==1)
                map (n+ROWS,HIGH);
            else if (pic[m][n]==0)
                map (n+ROWS,LOW);
        }

    //apply data
    shift4(d1,d2,d3,d4);

    //delay_ms (500);
    map(0,HALF);
    map(1,HALF);
    map(2,HALF);
    map(3,HALF);
    shift4(d1,d2,d3,d4);
}
*/
void map(int line, int state) {

    //lines are labeled 0 thru 15 starting from left side of board

    if (line==0 || line==1 || line==2 || line==3) {
        if (state==LOW) {
            bit_set (d1,7-(line*2));
            bit_set (d1,6-(line*2));
        } else if (state==HIGH) {
            bit_clear (d1,7-(line*2));
            bit_clear (d1,6-(line*2));
        } else if (state==HALF) {
            bit_clear (d1,7-(line*2));
            bit_set (d1,6-(line*2));
        }
    }
}
/* if (line==4 || line==5 || line==6 || line==7) {
    bit_clear (line,7);
    bit_clear (line,6);
    bit_clear (line,5);
    bit_clear (line,4);
    bit_clear (line,3);
    bit_clear (line,2);
}

if (state==LOW) {
    bit_set (d2,7-(line*2));
    bit_set (d2,6-(line*2));
} else if (state==HIGH) {
    bit_clear (d2,7-(line*2));
    bit_clear (d2,6-(line*2));
} else if (state==HALF) {
    bit_clear (d2,7-(line*2));
    bit_set (d2,6-(line*2));
}

if (line==8 || line==9 || line==10 || line==11) {
    bit_clear (line,7);
    bit_clear (line,6);
    bit_clear (line,5);
    bit_clear (line,4);
    bit_clear (line,3);
    bit_clear (line,2);
    if (state==LOW) {
        bit_set (d3,7-(line*2));
        bit_set (d3,6-(line*2));
    } else if (state==HIGH) {
        bit_clear (d3,7-(line*2));
        bit_clear (d3,6-(line*2));
    } else if (state==HALF) {
        bit_clear (d3,7-(line*2));
        bit_set (d3,6-(line*2));
    }
}

if (line==12 || line==13 || line==14 || line==15) {
    bit_clear (line,7);
    bit_clear (line,6);
    bit_clear (line,5);
    bit_clear (line,4);
    bit_clear (line,3);
    bit_clear (line,2);
    if (state==LOW) {
        bit_set (d4,7-(line*2));
        bit_set (d4,6-(line*2));
    } else if (state==HIGH) {
        bit_clear (d4,7-(line*2));
        bit_clear (d4,6-(line*2));
    } else if (state==HALF) {
        bit_clear (d4,7-(line*2));
        bit_clear (d4,6-(line*2));
    }
bit_set(d4,6-(line*2));
}

*/

void shift (int b) {
  int i;

  output_low(SCK);
  for (i=0; i<8; i++) {
    output_bit(SER, shift_right(&b, 1, 0));
    output_high(SCK);
    output_low(SCK);
  }
}

void shift4 (int b1, b2, b3, b4) {
  shift (b4);
  shift (b3);
  shift (b2);
  shift (b1);

  output_low(RCK);
  output_high(RCK);
  output_low(RCK);
}

Appendix C: Matlab Code

The following is a MATLAB function which models the varistor/electrophoretic cell system. This is intended to be used to model the system when the varistor is below threshold. For values above threshold the forward voltage drop of the varistor must be added in. As input it takes \( R_m \), the source resistance; \( R_1 \), the varistor resistance; \( C_1 \), the varistor capacitance; \( R_2 \), the display resistance; \( C_2 \), the display capacitance; \( V_b \), the voltage which is applied to the system; \( \text{init1} \) and \( \text{init2} \), the initial voltages of the varistor and display capacitors, respectively; and \( t_{\text{max}} \) which is the length of time that the solution is computed for. The algorithm produces the and plots the varistor and display cell voltages for \( 0 \leq t < t_{\text{max}} \) with 1000 points. It returns the two voltage waveforms as well as the values of these voltages at \( t_{\text{max}} \).

```matlab
function [vo1,vo2,last1,last2,temp] = var2(m,r1,c1,r2,c2,vb,init1,init2,tmax)

b = (1/(r*2^2*r*m)) + (1/(r*1+c*r*m)) + (1/(c2*r*m));
c = (1/(r*1+c2*r2*m)) + (1/(c1+c2*r2*m)) + (1/(r*1+r2*c2*m));
d = 1/(c2*r*m);
e = 1/(r1*r*m*c1*c2);
ec = e/c;
s1 = (-1*b) + sqrt((b*b)-(4*c))/2;
s2 = (-1*b) - sqrt((b*b)-(4*c))/2;

tau1 = 1/s1
tau2 = 1/s2
tmp1 = vb - init1 - (init2*(1+(m/r2)));
tmp2 = tmp1 / (m*c2);
tmp3 = tmp2 - (s2*init2) + (s2*ec*vb);
k1 = tmp3/(s1-s2);
k2 = init2 - k1 - (ec*vb);

t=0:(tmax/1000):tmax;

v2 = k1*exp(s1*t) + k2*exp(s2*t) + (ec*vb);
dv2 = s1*k1*exp(s1*t) + s2*k2*exp(s2*t);
v1 = vb - v2*(1+(1/r2)) - (c2*dv2);

subplot(211)
plot(v2);
title('V display cell');
subplot(212)
plot(v1);
title('V Varistor');

thresh = .1 * vb;

ind=9999999999999;
flag = 0;
for i=1:length(v2)
    if (flag==0) & (v2(i)>thresh)
        ind=i;
        flag=1;
    end
end

temp = ind * (tmax/1001)
vo1 = v1;
vo2 = v2;
```

60
last1 = v1(length(v1))
last2 = v2(length(v2))

The following function calls the previous function to simulate the response of the system to various square wave like patterns. It too takes the 5 resistor/capacitor values specified above. In addition, it takes a vector vb, which contains the sequence of voltage levels to be applied to the system. In this case, tmax is the length of time for which each level is applied. The function assumes zero as the initial conditions for the first waveform. Subsequent to that it takes the final values supplied by the last function call and uses them as the initial conditions for the next level. Thus it simulates realistically the behavior of the system. For example, with vb = [-100 100 -100 100] and tmax = 1, the function would simulate the response of the system to a -100 to 100 V square wave with period = 2 seconds for 2 periods of the square wave. The function plots the resulting varistor and display voltages and returns these vectors as output.

function [v1, v2, t] = vstim (rn, r1, c1, r2, c2, vb, tmax)

n = length(vb);
t=0;
v1=0;
v2=0;
i1=0;
i2=0;
b = 0;

for j = 1:n
    [vm, vn, i1, i2, foo] = var2 (rn, r1, c1, r2, c2, vb(j), i1, i2, tmax);
    v1 = [v1 vn];
    v2 = [v2 vn];
    bvec = ones(1,length(vn))*vb(j);
    b = [b bvec];
end

subplot(311)
plot(b)
tmp = axis;
axis ([tmp(1) tmp(2) (1.1*tmp(3)) (1.1*tmp(4))]);
title ('In')

subplot(312)
plot(v1)
tmp = axis;
axis ([tmp(1) tmp(2) (1.1*tmp(3)) (1.1*tmp(4))]);
title ('Varistor')

subplot(313)
plot(v2)
tmp = axis;
axis ([tmp(1) tmp(2) (1.1*tmp(3)) (1.1*tmp(4))]);
title ('Cell');