A Differential Passive Pixel Image Sensor

by

Iliana L. Fujimori

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degrees of Master of Engineering and Bachelor of Science at the MASSACHUSETTS INSTITUTE OF TECHNOLOGY February 1997

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Author
Department of Electrical Engineering and Computer Science
January, 1997

Certified by
Charles G. Sodini
Professor of Electrical Engineering
Thesis Supervisor

Accepted by
Arthur C. Smith
Chairman, Departmental Committee on Graduate Students

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Abstract

A differential passive-pixel image sensor was designed for a wireless camera application. One of the restrictions that the system places on the imager is that it have a power savings mode when no motion is detected in the camera's range of vision. The architecture chosen for the imager was thus a CMOS random access array. Compared to its CCD counterpart, a CMOS imager allows separate and independent access of each pixel. During the power savings mode, the sensor exhibits significant power savings by only turning on the required circuitry to send out images at reduced resolutions.

An n-well photodiode is a promising implementation for the conversion of light into a measurable electrical quantity. The n-well diode, with its deeper junction and lower doping concentration, offers a potential for higher quantum efficiency and lower noise than the conventional n-diffusion photodiode. Furthermore, the n-well photodiode has a much higher transmission rate than its silicided n-diffusion counterpart.

The strict layout design rules of the n-well, however, prevent reasonably-sized active pixels with high fill factors. It is therefore necessary to use a passive pixel. A passive pixel, which consists of only a photodiode and a row select transistor and whose output is in the form of charge, also has lower fixed pattern noise.

A differential architecture allows the pixel being sensed to be compared with a dummy cell that is kept in the dark. The differential output voltage corresponds to the sensed charge. This differential scheme reduces the column-to-column variation in large arrays by rejecting substrate bounce and effects due to temperature changes.

Thesis Supervisor: Charles G. Sodini
Title: Professor of Electrical Engineering
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Dedication

To my parents, Pedro and Elizabeth, and to our American Dream.
Contents

1 Introduction .......................................................... 12
  1.1 Motivation ..................................................... 12
  1.2 Objective ..................................................... 12
  1.3 Thesis Organization .......................................... 13

2 Pixel Design ......................................................... 15
  2.1 Imaging ......................................................... 15
    2.1.1 Generation of an electron-hole pair .................. 15
    2.1.2 Collection of Generated Charge Carriers ............ 17
    2.1.3 Transfer of Signal to Output ......................... 21
  2.2 Construction of Photodiode ................................ 21
    2.2.1 N-Diffusion .............................................. 21
    2.2.2 N-Well .................................................. 22
    2.2.3 P-Diffusion and P-Well ................................ 25
  2.3 Types of Pixels .............................................. 25
    2.3.1 Interline Transfer CCD .................................. 26
    2.3.2 CMOS Current Output Pixel ............................ 27
    2.3.3 CMOS Voltage Output Pixel ............................. 27
    2.3.4 CMOS Charge Output Pixel ............................. 28
  2.4 Pixel Capacitance - Charge Output Pixel ................. 29
  2.5 Noise Analysis - Charge Output Pixel ..................... 31
## 3 Architecture

3.1 Random Access ........................................... 34
3.2 Differential Mode of Imaging .............................. 35
3.3 Output Circuit ............................................. 38
   3.3.1 Schematic Diagram .................................. 38
   3.3.2 Clocking Scheme .................................... 41
   3.3.3 Reset Phase ......................................... 42
   3.3.4 Sample Phase ....................................... 42
   3.3.5 Offset Cancellation ................................ 43
3.4 Architecture Summary .................................... 44

## 4 Op Amp Design .............................................. 45

4.1 Topology ................................................... 45
   4.1.1 Folded Cascode ...................................... 45
   4.1.2 Biasing ............................................... 47
   4.1.3 Common Mode Feedback Circuit ...................... 48

4.2 Opamp Characteristics ................................... 49
   4.2.1 Specifications ....................................... 49
   4.2.2 Gain and Bandwidth ................................ 50
   4.2.3 Phase Margin ....................................... 51
   4.2.4 Swing ................................................ 51
   4.2.5 Power ............................................... 52

4.3 Noise Analysis ............................................. 52

4.4 Output Buffer ............................................. 55

## 5 Layout ..................................................... 56

5.1 Process Information ..................................... 56
5.2 Pixel Cell ................................................ 56
5.3 Dummy Cells .................................................. 57
5.4 Pixel Array ...................................................... 58
5.5 Opamp .......................................................... 58
5.6 Electrostatic Discharge Protection (ESD) ...................... 59
5.7 Complete Layout ............................................... 59

6 Results and Discussion ......................................... 63
  6.1 Test Setup ..................................................... 63
    6.1.1 Chip Structure ........................................... 63
    6.1.2 PC Board ................................................ 63
    6.1.3 Illumination .............................................. 64
  6.2 Results ........................................................ 65
    6.2.1 Output Waveforms ....................................... 65
    6.2.2 Optic Response .......................................... 68
  6.3 Discussion .................................................... 71
    6.3.1 Origin of Parasitic Current ............................ 71
    6.3.2 Second Order Effects .................................. 73
  6.4 Recommendations ............................................ 74
  6.5 Results Summary ............................................. 75

7 Conclusions ..................................................... 76

A Differential Passive Pixel Image Sensor
List of Figures

1-1 Overall architecture of wireless camera proposed by the Wireless Sensor Project at MIT .............................................. 13
2-1 Photodiode ........................................................................ 16
2-2 Absorption coefficient vs wavelength in Silicon ..................... 17
2-3 Dependence of minority carrier diffusion length on the doping levels .... 18
2-4 Spectral response as a function of the wavelength with the diffusion length as a parameter ........................................... 19
2-5 N-Diffusion pixel ............................................................... 22
2-6 N-Well pixel ...................................................................... 23
2-7 Device architecture of interline transfer CCD ....................... 27
2-8 Schematic diagram of a CMOS current output pixel ................ 28
2-9 Schematic diagram of a CMOS voltage output pixel ................. 29
2-10 Schematic diagram of a CMOS charge output pixel ................. 30
2-11 Capacitance seen from the row select switch ....................... 31
3-1 Architecture of a random access photodiode array introduced by Yadid-Pecht et al. .................................................. 35
3-2 Implementation of random access array with dummy cells .......... 36
3-3 Imager Architecture .......................................................... 37
3-4 Opamp in Feedback configuration ........................................ 39
3-5 Clocking Scheme ............................................................. 41
LIST OF FIGURES

3-6 Opamp in Feedback Configuration - Reset Phase ..................................... 42
3-7 Opamp in Feedback configuration - Sample Phase ................................. 43
3-8 Offset Cancellation Scheme ................................................................. 43

4-1 Folded Cascode OpAmp Schematic Diagram ....................................... 46
4-2 Opamp Biasing Circuit ................................................................. 47
4-3 Common Mode Feedback Circuit ...................................................... 49
4-4 Folded Cascode Open-Loop Gain ....................................................... 51
4-5 Folded Cascode Phase ................................................................. 52
4-6 Output swing for positive and negative output nodes ....................... 53
4-7 Noise Analysis ................................................................................. 54
4-8 Output Buffer for Opamp ............................................................... 55

5-1 Pixel Layout ......................................................................................... 57
5-2 Input/Output Pads ............................................................................. 59
5-3 Power and Ground Pads ..................................................................... 60
5-4 Pads for voltages greater than 5V ..................................................... 60
5-5 Implementation of a pn diode ............................................................. 60
5-6 Implementation of Metal2 Field Transistor ...................................... 61
5-7 Implementation of Resistor ............................................................... 61
5-8 Complete Layout ................................................................................. 62

6-1 Schematic Diagram of Imager ............................................................. 64
6-2 Clocking Scheme Used for Testing Imager ......................................... 65
6-3 Relationship between illumination power and input voltage with an attenuation filter of 100:1 .......................................................... 66
6-4 Output Waveform with no pixels selected for readout indicates the presence of a parasitic current ......................................................... 67
6-5 Output Waveform with one pixel selected for readout ..................... 67
6-6 Output Waveform with two pixels selected for readout .................. 68

A Differential Passive Pixel Image Sensor ........................................... 9
6-7 Behavior of output waveform at various illumination levels ............... 69
6-8 Optic response of imager with one (o) and two pixels (+) selected for readout 69
6-9 Comparison of individual optic responses to pixel in the top of the array (o) and pixel in the middle of the array (*) ........................................ 70
6-10 Optic response of two pixels being selected together (+) compared with the sum of the individual responses (x) ........................................ 71
6-11 Layout of the pixel array ................................................................. 72
6-12 Output Voltage effect of selecting one pixel in second column on parasitic current ................................................................. 73
6-13 Output Voltage effect of selecting two pixels in second column on parasitic current ................................................................. 74
6-14 Subthreshold characteristics of row select device .......................... 75
List of Tables

4.1 Folded Cascode Transistor Sizes in $\mu$m .......................... 46
4.2 Bias Circuit Transistor Sizes in um ............................... 48
4.3 Common Mode Feedback Circuit Parameters ....................... 48
Chapter 1

Introduction

1.1 Motivation

The importance of low power electronics is evident from the increasing demand for portable electronics that can realize high levels of functionality. One dominant example is the laptop computer which attempts to achieve the same functionality of a desktop computer by operating on a battery. While some progress in battery technology is being made, circuit designers must also work to reduce the power dissipation in electrical circuits [1].

The Wireless Sensor Project at MIT is currently developing low power techniques to build a wireless camera. The overall architecture of the camera is shown in figure 1-1. It consists of a sensor, data conversion, digital signal processing, RF transceiver and a power supply system. The compressed, encrypted digital data will be transmitted in a range of data rates over a wide range of average transmission output power levels to a base station.

1.2 Objective

The objective of this thesis is to investigate the issues involved in the implementation of an imager for the system shown in figure 1-1. While the projected array size for this system is 256 $\times$ 256, this thesis examines a 256 $\times$ 4 array.
Figure 1-1: Overall architecture of wireless camera proposed by the Wireless Sensor Project at MIT

One of the proposed methods to save power in the wireless camera consists of transmitting an image at full resolution only when motion is detected. If there is no motion detected in the camera’s range of vision, the imager will transmit images at a reduced resolution. The imager presented in this thesis uses a CMOS random access architecture to enable this “sleep” (or reduced resolution) mode. In addition, a differential readout scheme is used to reduce the column-to-column mismatch due to substrate bounce or temperature variations.

The imaging element presented in this thesis, an n-well photodiode, is a promising implementation for high performance imagers in sophisticated device technologies. Furthermore, a passive pixel readout scheme was selected in hopes of achieving a high fill factor.

1.3 Thesis Organization

Chapter 2 explains the advantages of the n-well photodiode over the n-diffusion photodiode. The different types of pixel readout schemes are also explained in this chapter.

The CMOS random access architecture is described in chapter 3. The architecture also
features a differential mode in which the output of a sensed pixel is compared with that of a dummy pixel. The output circuit of the system is also described in this chapter.

Chapter 4 describes the characteristics of the folded cascode opamp, bias circuit and switched capacitor common mode feedback scheme.

The layout of the pixel cell, opamp and pixel array is shown in chapter 5. The electrostatic discharge circuits used for the input/output pins are also described in this chapter.

Chapter 6 shows test results and chapter 7 concludes the thesis.
Chapter 2

Pixel Design

2.1 Imaging

The most common method used for solid-state imaging consists of converting light into a measurable electrical quantity (voltage, current or charge). The process includes the conversion of photons into electron-hole pairs, integration of electrons or holes, and transfer of the signal to the output [2]. There exist several alternatives to achieve image sensing, but this chapter focuses on the photodiode, a reverse-biased p-n junction (see figure 2-1).

2.1.1 Generation of an electron-hole pair

The generation of an electron-hole pair occurs when a photon carrying an energy greater than the silicon bandgap energy (1.1 eV) is absorbed by a substrate. The amount of generated charge depends on the photon flux and wavelength of the incoming light and the absorption coefficient of the semiconducting substrate [3].

The energy of the photon can be described by:

\[ E = h\nu \tag{2.1} \]

where \( h \) is Planck’s constant and \( \nu \) can be represented by \( \frac{c}{\lambda} \), the speed of light, \( c \), divided...
by the wavelength of the photon, $\lambda$. We can now get energy in terms of wavelength:

$$E = \frac{hc}{\lambda} \quad (2.2)$$

Plugging in the values for constants $h$ and $c$, the maximum wavelength for a photon to generate an electron-hole pair in silicon is 1.13$\mu$m, making silicon a suitable material for imaging in the visible wavelength range (400nm to 800nm).

The photon flux as a function of the depth of the substrate $x$, $\phi(x)$, can be represented by an exponential function:

$$\phi(x) = \phi_0 e^{-\alpha x} \quad (2.3)$$

where $\phi_0$ is the photon flux at the surface and $\alpha$ is the absorption coefficient of the substrate material.

Another useful parameter is the inverse of the absorption coefficient or penetration depth. Figure 2-2 shows the relationship between absorption coefficient and wavelength and the corresponding curve for the penetration depth. For short wavelengths, the absorption coefficient is large and the penetration depth is consequently small. Most of the carriers
at this wavelength are generated at the surface of the semiconductor where the rate of recombination is very high and electron hole pairs recombine almost instantly. It should now be clear that appreciable photocurrent is only generated for a certain range of wavelengths that includes the visible range.

2.1.2 Collection of Generated Charge Carriers

Once the photon has been absorbed and the electron-hole pair has been generated, the electrons must be separated from the holes. In addition, since the charge of a single electron is much too small to be converted into a measurable electrical quantity, it is necessary to collect the generated charge carriers over a period of time.

In the photodiode shown in figure 2-1, the separation is achieved with the help of the electric field in the depletion region. The collection efficiency is highly dependent on the wavelength of the incoming light through the penetration depth. The collection in the depletion region is highly efficient because the charge is collected where it is generated. The carriers generated outside of the depletion region, however, must diffuse their way to the depletion region. If the diffusion length of the minority carrier is larger than the distance
Figure 2-3: Dependance of minority carrier diffusion length on the doping levels

it must travel to the depletion region, the carrier has a very strong chance of contributing to the photocurrent. On the other hand, if its journey to the depletion region is longer than the diffusion length, then the carrier will most likely recombine before reaching the depletion region. The collection outside of the depletion region then depends highly on the diffusion length of the minority carriers.

The minority carrier diffusion length, $L_{e,h}$, formally defined as the average length a carrier travels by diffusion before it recombines, can be expressed by $\sqrt{D_{e,h} \tau}$ where $D_{e,h}$ is the diffusion constant of electrons and holes respectively and $\tau$ is the minority carrier lifetime. Since both $D_{e,h}$ and $\tau$ depend on the majority carrier doping, $L_{e,h}$ is a strong function of the doping concentrations. Figure 2-3 shows the strong dependance of minority carrier diffusion length on the doping levels [4].

Lower doping concentrations lead to larger depletion regions which means a larger area for the separation of electrons and holes and a shorter distance for the minority carriers to travel. However, this is a second order effect. Lower doping concentrations are therefore advantageous in two ways: longer diffusion lengths and wider depletion regions.
Figure 2-4: Spectral response as a function of the wavelength with the diffusion length as a parameter

Although the circuit designer does not typically have much control over where the edge of the depletion region will be, it should be noted that the location of the latter will also affect the performance of the imager. Since the collection efficiency is close to 100% in the depletion region, the location of the depletion region will determine which wavelength gets the highest response.

Spectral Response

A measure of the response of an imager is the spectral response, R, which is defined as the output voltage or current as a function of incoming light energy or power. The spectral response of an imager sensor is dependent on the wavelength of the incoming light and the diffusion length of the substrate material. Figure 2-4 shows a typical spectral response as a function of the wavelength with the diffusion length as a parameter.

The bottom curve with a diffusion length of zero has a spectral response that corresponds purely to the charge collected in the depletion region. As the diffusion length increases, the response for higher wavelengths increases since the charge generated outside the depletion
region has a greater chance of diffusing and becoming collected.

**Quantum Efficiency**

Another parameter used to compare different image sensors is the quantum efficiency, \( \eta \), defined as the number of collected electrons divided by the number of photons impinging on the device. The number of collected electrons per unit of time, \( N \), can be expressed as follows:

\[
N = \frac{Q_n}{qT_{int}} \tag{2.4}
\]

where \( Q_n \) is the collected charge, \( T_{int} \) is the integration time and \( q \) is the charge of a single electron. We can describe the number of photons incident to the surface of the substrate, \( P \), as follows:

\[
P = \frac{\phi_o}{E} \tag{2.5}
\]

Combining equations 2.2, 2.4 and 2.5, we can now define the quantum efficiency as:

\[
\eta = \frac{Q_nhc}{qT_{int}\phi_o\lambda} \tag{2.6}
\]

The quantum efficiency can also be written in terms of the spectral response, \( R \), as follows:

\[
\eta = \frac{Rhc}{q\lambda} \tag{2.7}
\]

The value of the quantum efficiency, like the spectral response, is dependent on the diffusion length and depletion width through the collection efficiency and the wavelength of the incoming light through the absorption coefficient. Other factors that might affect the quantum efficiency include any material that is deposited on top of the photodiode area. For example, the use of silicide to lower the resistance in source/drain diffusion in some
recent processes can severely hurt the performance of the imager due to its opacity.

2.1.3 Transfer of Signal to Output

After a certain integration time, the signal is sent to the output for read-out. The output signal can be in the form of charge, current or voltage. Different output circuits exist for the different forms of output signals. Section 2.3 elaborates on the different output circuits utilized in CCD and CMOS imaging.

2.2 Construction of Photodiode

A photodiode can be constructed in many different ways. One possibility is an n-diffusion in a p-type substrate where electrons are the carriers integrated. Alternatively, the n-diffusion can be replaced by an n-well where the electrons would be integrated. This section delves into the advantages and disadvantages of these possibilities and describes the photodiode chosen for this thesis project. The last section also offers some reasoning for rejecting p-diffusion and p-well pixels.

2.2.1 N-Diffusion

The n-diffusion photodiode shown in figure 2-5 is a common form of light conversion in the field of imagers. The diffusion used to construct the photodiode is the same heavily doped n-type material used as the source and drain for a typical MOSFET. The junction depth is approximately 0.25μm and the n+ region is degenerately doped to approximately $10^{20} cm^{-3}$. The doping of the substrate is on the order of $5 \times 10^{16} cm^{-3}$. Rowsel selects the row for readout and Col represents the column line.

The inevitable trend to bring about more sophisticated technologies to the world of IC design, however, seems to be hurting the performance of imagers. As device sizes scale down, source/drain junction depths are getting smaller and doping concentrations are getting higher. Furthermore, most of the current standard processes are depositing a silicide on the source/drain diffusions in order to reduce junction resistances.
Figure 2-5: N-Diffusion pixel

We can qualitatively analyze the impact that these changes will have on the n-diffusion photodiode in terms of the quantum efficiency. The increase in doping concentration in the substrate leads to smaller depletion regions and shorter diffusion lengths in the bulk. As mentioned in section 2.1.2, smaller depletion regions and shorter diffusion lengths lead to lower collection efficiency and consequently lower quantum efficiency.

As source/drain junction depths become shallower, the edge of the depletion region becomes too shallow for optimal spectral sensitivity. The quantum efficiency of the n-diffusion photodiode is also affected by the presence of silicide in current technologies. The transmission rate for silicide can be as low as 10% in the visible light spectrum [5].

The next section explores an alternative pixel that might not require a tradeoff of sophisticated device technologies for imager performance.

2.2.2 N-Well

The n-well photodiode illustrated in figure 2-6 is a promising implementation for high performance imagers in sophisticated device technologies. Compared with the n-diffusion photodiode, the n-well implementation has a lower doping concentration ($5 \times 10^{16} \text{cm}^{-3}$) and its junction goes deeper into the p-type substrate ($\sim 3 \mu \text{m}$). The n+ region overlapping
with the well is used as a contact for the well during the sample phase.

The first improvement over the n-diffusion photodiode is on the size of the depletion region. Eq. 2.8 describes the depletion region in a pn diode:

\[
X_d = \sqrt{\frac{2\epsilon\phi_{bi} N_A + N_D}{q N_A N_D}}
\]  

(2.8)

In the n+ diffusion diode, the doping of the n+ region is so much higher than the doping in the p region that most of the depletion region is located in the p region and is only dependent on the doping of the substrate as shown in Eq. 2.9. The size of the depletion region can only be expected to decrease as the doping levels of the substrate increase with more modern technologies.

\[
X_d = \sqrt{\frac{2\epsilon\phi_{bi}}{N_A q}}
\]  

(2.9)

For an n-well diode, the doping in the n-well is comparable with the doping in the p substrate and the size of the depletion region then depends on the doping of the well as well as the substrate, as shown in Eq. 2.8. The depletion width on the substrate remains the same, but we now see a depletion region also forming on the n-well, consequently doubling
the size of the depletion region for equally doped p and n regions.

It is essential to note that a larger depletion region also leads to a decrease in the capacitance of the pixel. The advantage of having a lower capacitance is lower thermal noise which is characterized by $\sqrt{kT/C}$ in the charge domain. Chapter 3 explains the improvement in the conversion gain for a lower pixel capacitance. The design tradeoff for a lower pixel capacitance is a decrease in the amount of charge that the pixel can hold for a certain voltage.

The second advantage of using a lower-doped material for charge integration is on the minority carrier diffusion length. The graph shown in figure 2-3 shows the hole and electron diffusion length of 0.5 $\mu$m for a doping concentration of $10^{20} cm^{-3}$ and approximately 100 $\mu$m for a doping concentration of $10^{17}$. These figures show a difference of two orders of magnitude in the hole and electron diffusion length for n+ diffusion and n-well photodiodes.

Another difference between the n-well and n-diffusion photodiodes is the depth of the junction. Figures 2-5 and 2-6 show that the depth of an n-well is approximately ten times larger than that of the n-diffusion photodiode. The deeper junction of the n-well is advantageous for the performance of the photodiode because the edge of the depletion region is closer to the range of visible photon absorption, thereby decreasing the distance that generated carriers need to travel and improving the quantum efficiency of the pixel.

In contrast with the n-diffusion photodiode, the n-well implementation is not affected by the silicide used in modern technologies. Due to the field oxide that is placed on top of the n-well, the n-well does not get silicided unless there is an n+ or p+ diffusion or poly inside it. The transmission rate is thus not altered by the silicide in an n-well photodiode.

It is also important to analyze the disadvantages of the n-well photodiode. As shown in figure 2-6, an n+ diffusion is necessary to access the charge collected in the n-well. This n+ diffusion must make contact with the n-well but it must also serve as the drain of the rowselect transistor. The n+ diffusion must extend outside long enough so that the n-well does not accidentally expand during fabrication and short out the rowselect transistor. This irregular extension of an n+ diffusion beyond the n-well is not permitted under the
standard design rules for this process. There is therefore a certain amount of risk involved in attempting this layout since the current fabrication processes have not been designed for it.

The design rules for an n-well are much more strict than they are for n+ diffusion. For instance, the minimum width for n-diffusion is $3\lambda$ compared with $10\lambda$ for an n-well. In addition, the spacing of n-diff to n-diff ($3\lambda$) is also more flexible than the n-well to n-well ($9\lambda$). As a result, the layout of an n-well photodiode turns out to be almost 3 times bigger than that of an n-diffusion for similar fill factors. However, this negative effect can be tolerated for an increase in the diffusion lengths.

Compared with the n-diffusion photodiode, the n-well photodiode is the big winner in terms of quantum efficiency. Even in the absence of the opaque silicide, the n-well photodiode has a much larger diffusion length and a larger and deeper depletion region. After weighing the advantages and disadvantages, the n-well photodiode was chosen for this project since it seems to be a worthwhile effort to improve imager performance for sophisticated CMOS technologies.

### 2.2.3 P-Diffusion and P-Well

It is also physically possible to integrate holes rather than electrons by placing a p-diffusion or p-well in an n-type substrate. Since a p-well process was not available to us, the p-well pixel was not an option. A p-diffusion pixel requires n-wells for each pixel and leads to a significantly lower fill factor due to the strict design rules for n-wells. A p-diffusion pixel in an n-well process would only integrate carriers generated in the n-well and not in the p-substrate, severely deteriorating the quantum efficiency for high wavelengths.

### 2.3 Types of Pixels

Since their conception, charge-coupled devices (CCDs) have dominated the field of imaging. It was not until a few years ago that the scaling and improvements in CMOS technology
made the integration of imaging arrays practical. CMOS imagers are becoming more common and in many cases more appealing than CCDs [6, 7, 8].

There are three main advantages of CMOS imagers. First, CMOS operates at lower power supplies (3.3 V operation vs 5-15V). Second, CMOS imagers can be easily integrated with other CMOS circuitry on the same chip. Finally, CMOS imagers allow random access of each pixel giving it an extra pan and zoom feature. These will become evident in the following paragraphs.

This section illustrates one example of a CCD imager (Interline Transfer CCD) and three types of CMOS pixels (charge output, current output and voltage output).

### 2.3.1 Interline Transfer CCD

A typical construction of an interline transfer device is shown in figure 2-7 [2]. It consists of an m x n photodiode array, n vertical CCD shift registers and one horizontal CCD register. After a certain integration period, the collected charge in each photodiode is transferred to the CCD shift registers and read out sequentially. The main reason why CCD imagers use more power than CMOS imagers is because all the pixels in a CCD array must be clocked individually. As soon as the photodiode has completed the integration, $\phi_1$ goes high and the electrons collected in the photodiode gather under the register driven by $\phi_1$. Consequently, when $\phi_2$ goes high and $\phi_1$ goes low, the electrons cluster under the gate driven by $\phi_2$. The process continues until the electrons reach the output. The readout is performed serially and all the bottom row pixels must be read out before the adjacent row above can be read.

Since the output of the photodiodes are read serially on a CCD imager, there is no power savings when the resolution is reduced. In other words, if the resolution of the imager is reduced and only certain pixels are selected for readout, all the pixels in subsequent rows must be read out before the desired pixel can be accessed.
2.3.2 CMOS Current Output Pixel

Figure 2-8 is a schematic diagram of a CMOS current output pixel [9]. The pixel is shown inside the dotted lines. Prior to the integration of the photodiode, node A is reset to Vdd (if $V_{gg} > V_{dd} + V_t$). It is advantageous to bootstrap the gate of the reset pixel in order to reduce any mismatch in the threshold voltage between devices. During the integration period, the electrons collected in the photodiode reduce the voltage of node A to $V_{pix}$. This new voltage then determines the current flow through M1. When this row is selected for readout, M1 pulls current through the resistor and converts the current to a voltage at the output, $V_{out}$. If linearity is desired in the pixel, the positive input of the opamp can be set to some voltage, $V_{small}$, so that when the rowsel transistor is selected, the drain of M1 charges up to $V_{small}$. If $V_{small} < V_{pix} - V_t$, then we can be assured that M1 will stay in the triode region.

2.3.3 CMOS Voltage Output Pixel

A diagram of the CMOS voltage output pixel is shown in figure 2-9 [10]. The reset method here resembles that of the current output pixel: node A is reset to Vdd if $V_{gg} > V_{dd} + V_t$. 

A Differential Passive Pixel Image Sensor  

27
Figure 2-8: Schematic diagram of a CMOS current output pixel

During the integration period, the electrons collected in the photodiode reduce the voltage of node A to \( V_{pix} \). When this row is selected for readout, the rowsel gate goes high and a current \( I_{out} \) is pulled through M1. The value of \( V_{out} \) is described by Eq. 2.10:

\[
V_{out} = V_{pix} - V_T - \sqrt{\frac{2I_{out}}{\mu C_{ox} \frac{W}{L}}} \tag{2.10}
\]

The error due to the mismatch in the threshold voltage across devices can be eliminated by correlated double sampling. In correlated double sampling, the pixel is sampled twice, once with the integrated charge and then immediately after reset. The difference is then taken between the two values and \( \Delta V_{out} \) should now equal \( \frac{Q_s}{C_{pix}} \) where \( Q_s \) is the pixel charge and \( C_{pix} \) is the pixel capacitance.

### 2.3.4 CMOS Charge Output Pixel

A schematic diagram of a CMOS charge output pixel is illustrated in figure 2-10 [11]. The pixel itself appears inside of the dotted line. The rest of the diagram represents the output circuit. During the reset phase, the voltage across the feedback capacitor is set to zero and the photodiode voltage, \( V_{pix} \), is set to \( V_{cm} \). When the charge collected by the photodiode
is dumped onto the line capacitance, the integrated charge is transferred to the feedback capacitor in order to maintain charge conservation. The charge-to-voltage conversion is achieved by this feedback capacitor and the output voltage is proportional to the integrated charge.

The CMOS charge output pixel was chosen for this imager sensor. Due to the strict design rules for the n-well photodiode, the voltage output or current output pixels would not provide an adequate fill factor for a given area. In comparison, the charge readout pixel yields high fill factors even for n-well pixels.

2.4 Pixel Capacitance - Charge Output Pixel

The capacitance of a CMOS charge output pixel can be determined from the capacitance of a reverse-biased pn junction. The capacitance per unit area of a pn junction is described as follows:

\[
C = \sqrt{\frac{q\epsilon}{2(\phi_{bi} - V) \frac{N_A+N_D}{N_A N_D}}} \quad (2.11)
\]
Figure 2-10: Schematic diagram of a CMOS charge output pixel

where \( N_A \) and \( N_D \) are doping concentrations, \( V \) is the reverse bias voltage and \( \phi_{bi} \) is the built-in potential described as:

\[
\phi_{bi} = \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2} \tag{2.12}
\]

A useful parameter to calculate is the maximum charge that can be collected in the photodiode, \( Q_{max} \). Since the capacitance of the junction depends on the reverse bias, \( Q_{max} \) must be integrated over the voltage swing of the pixel:

\[
Q_{max} = A \int_0^5 \sqrt{\frac{q\epsilon}{2(\phi_{bi} - V) N_A N_D} \frac{N_A + N_D}{N_A N_D}} dV \tag{2.13}
\]

After integrating and evaluating Eq. 2.13, we have

\[
Q_{max} = -A \sqrt{\frac{2q\epsilon N_A N_D}{N_A + N_D} \left[ \sqrt{\phi_{bi} - 5} - \sqrt{\phi_{bi}} \right]} \tag{2.14}
\]

where \( A \) is the area of the junction plus the area of the sidewalls. For simplicity reasons, we will assume that the sidewall capacitance is equal to the junction capacitance. In order to get a rough estimate of the maximum charge, we further assume that the depth of the
n-well is $4\mu m$ and the doping concentrations of the n-well and the p-type substrate are $10^{16} \text{cm}^{-3}$. These approximations lead to an area of $\approx 260\mu m^2$ (see chapter 5 for a layout of the pixel) and a built-in potential of 0.718 V. Consequently, the maximum charge that a pixel cell can hold is approximately 160 fC.

2.5 Noise Analysis - Charge Output Pixel

The mean square noise voltage introduced by a switch is proportional to $kT/C$, where $k$ is Boltzmann’s constant, $T$ is the absolute temperature and $C$ is the effective sampling capacitance seen by the switch [12]. Using the expression $Q = CV$, we can express the thermal noise in the charge domain as follows:

$$\overline{Q^2} = C^2 \frac{kT}{C} = kTC$$  \hspace{1cm} (2.15)

Figure 2-11 shows the capacitance seen by the row select switch. $C_{pix}$ is the pixel capacitance, $C_{line}$ is the line capacitance, $C_{in}$ is the blocking capacitance and $C_p$ is the parasitic capacitance seen looking into the opamp.

The capacitance to the right of the switch can be combined to give:

$$C_{net} = C_{line} + \frac{C_{in}C_p}{C_{in} + C_p}$$  \hspace{1cm} (2.16)
This expression can be reduced to $C_{\text{line}}$ if we assume that $C_{\text{in}} \gg C_p$ and $C_{\text{line}} \gg C_p$. The mean square noise charge introduced by the switch is then:

$$\overline{Q^2} = kT \frac{C_{\text{pix}} C_{\text{net}}}{C_{\text{pix}} + C_{\text{net}}}$$  \hspace{1cm} (2.17)

If we replace $C_{\text{net}}$ with $C_{\text{line}}$ and assume that $C_{\text{line}} \gg C_{\text{pix}}$, then $\overline{Q^2}$ can be reduced to $kTC_{\text{pix}}$.

The voltage seen at the output due to this noise charge must be equal to the voltage seen for a charge $Q$ generated at the photodiode:

$$V_{\text{out}} = \frac{Q \times 0.7}{C_{fb}}$$  \hspace{1cm} (2.18)

where 0.7 is the ratio of the charge that gets through the blocking capacitor to the feedback capacitor $C_{fb}$. The total noise voltage seen at the output is then:

$$V_{\text{noise}} = \frac{\sqrt{kTC_{\text{pix}}(0.7)}}{C_{fb}}$$  \hspace{1cm} (2.19)

In order to determine the signal to noise ratio, we must compare it to the signal voltage and find their ratio:

$$V_{\text{signal}} = \frac{Q_{\text{pix}}(0.7)}{C_{fb}}$$  \hspace{1cm} (2.20)

giving a signal to noise ratio of:

$$SNR = \frac{Q_{\text{pix}}}{\sqrt{kTC_{\text{pix}}}}$$  \hspace{1cm} (2.21)

The signal to noise ratio is then inversely proportional to the pixel capacitance for a certain amount of charge. If we now make a noise comparison between the n-diffusion and the n-well pixels, we can see that the n-well pixel wins due to its smaller capacitance. Furthermore, we would expect the n-well pixel to yield a larger amount of charge for a certain number of photons due to issues discussed in section 2.2.2 giving the n-well pixel a
double advantage in terms of signal to noise ratio.

2.6 Pixel Design Summary

This chapter described the advantages and disadvantages of using an n-well photodiode for this project. The advantages include a longer diffusion length, a larger depletion region, lower noise and consequently a better spectral response in silicided processes. On the other hand, the n-well photodiode takes a larger area due to the strict design rules and presents some risks since the required layout does not pass the standard design rules. The pixel readout methods were also explained in this chapter. The passive (or charge readout) pixel was mainly chosen for this project mainly because it allows high fill factors in reasonable areas for the n-well photodiode.
Chapter 3

Architecture

3.1 Random Access

A random access array is a promising implementation that allows one to vary the spatial resolution of the imager and save power for lower resolutions. The array in figure 3-1 shows the random access architecture introduced by Yadid-Pecht et al in 1991 [10]. It operates in a fashion similar to the architecture used in random access memories (RAM). A pixel is selected for readout by addressing the row and column. The outputs of all pixels in the selected row appear simultaneously at their column lines, and the column decoder sequentially selects column lines to access the line outputs, buffer and send the signal to the chip output.

The main advantage of this architecture is the ability to access pixels independently. We can easily read out one pixel of interest without looking at irrelevant data. This architecture also allows us to reduce the resolution by decreasing the number of rows or columns accessed. A zoom/pan option is also available with this implementation.

Though this architecture may be implemented using charge-coupled devices (CCD's) or CMOS pixels, the random access advantage only applies to a CMOS implementation. A CCD array would not be a true random access architecture since the output of each pixel is read out sequentially and does not lead to power savings for reduced resolutions. In contrast
to CCD arrays, the CMOS random access array represents power savings during the sample mode as well as the sleep mode. CCD arrays require driving multiple high capacitive lines for each pixel, whereas CMOS arrays only require driving one high capacitive line per row. During the sleep mode, large power savings can be expected if some of the rows or columns are not accessed.

3.2 Differential Mode of Imaging

The array and output circuitry shown in the previous section can be implemented with a fully-differential scheme. Figure 3-2 illustrates an example of this implementation which is specific for a charge readout pixel. The integrated charge of a particular pixel is dumped on the feedback capacitor and converted to a voltage when its row is selected for readout. The sense amplifier then compares the output of this opamp with the output of the adjacent opamp (which contains the output of a dummy pixel) and outputs only the voltage equivalent to the integrated charge. In essence, this implementation first accomplishes a charge
to voltage conversion and then senses the difference between a sensed and a dummy signal.

This differential mode of imaging is helpful in eliminating effects due to substrate bounce and other common mode disturbances that eventually lead to column-to-column variations. It is important to place the dummy cell as close to the sensing pixel as possible since the substrate bounce can vary from column to column.

The major drawback of the architecture shown in figure 3-2 is that it employs two amplifiers to achieve the charge-to-voltage conversion and the sensing between imaging and dummy pixels. Figure 3-3 illustrates the architecture designed for this thesis, which is a variation of the implementation shown in figure 3-2. The fully-differential opamp at the output performs the charge to voltage conversion and differentiation simultaneously. This architecture requires that the array be staggered since pixels on adjacent columns now need to be addressed separately. If the pixels were not placed in a staggered configuration, the word lines of adjacent rows would cross and lead to capacitive coupling.

Although this figure shows one opamp for every two columns, the number of opamps
Figure 3-3: Imager Architecture
in the array depends on various factors. The first factor consists of the power savings that can be extracted from having many slow opamps rather than one fast one. During the sleep mode when only certain columns are being read out, power is saved by turning off the opamps not being used. If there was only one fast opamp for the entire array, there would be no power savings during the sleep mode. Another factor to consider is the layout of the opamp. If the pitch of the opamp is larger than the pitch of one column of pixels, one opamp will have to be shared among the number of columns it takes to match the pitch of the opamp. This issue is discussed in more detail in chapter 5.

### 3.3 Output Circuit

The output circuit of the imager is described in this section. It consists of an opamp, a buffer, capacitors and switches. The opamp design and characteristics as well as the source follower are described in more detail in chapter 4.

#### 3.3.1 Schematic Diagram

Figure 3-4 illustrates the opamp in the closed-loop configuration. All the transistors in this figure act as switches. The W/L ratios for all switches were set to 2.5u/1.0u. Cfb1 and Cfb2 are the feedback capacitors. Cin1 and Cin2 are blocking capacitors that allow the column line to be reset to 5 V while the common mode of the opamp is at 2.5 V. Cline1 and Cline2 are the parasitic capacitances of the bit line, which were calculated to be 3 pF. The photodiodes are represented in this figure by their respective capacitances, Cpix1 and Cpix2. The pixel capacitance varies with the reverse bias voltage, but in this section we are only interested in the maximum capacitance that the pixel can have. This maximum capacitance, calculated in the absence of a reverse bias when the depletion region is at a minimum, is 65 fF. The role of all switches and clocks will become more apparent in sections 3.3.3 and 3.3.4.

The value of the blocking capacitors needs to be maximized in order to maximize the amount of charge that gets transferred to the feedback capacitors. The amount of charge
that is transferred to the feedback capacitor is defined by the ratio of $\frac{C_{in}}{C_{in} + C_{line}}$. The ideal case would consist of a $C_{in}$ that is much greater than $C_{line}$. The value of $C_{in}$, however, is limited by the area that it takes up. The final value was chosen to be 7 pF and the ratio of the charge that gets across to the pixel charge is $7/10$.

In order to prevent the opamp from saturating, it is important to choose a reasonable value for the feedback capacitors. In other words, the amount of charge that the feedback capacitor can hold should be greater than the maximum amount of charge that the pixel can hold. The lower limit for $C_{fb}$ is then defined by

$$\frac{7}{10} \frac{Q_{pix}}{V_{sw}} = 18.8 \mu F$$ (3.1)

where $Q_{pix}$ is the maximum amount of charge that the pixel can hold and $V_{sw}$ is the output swing of the opamp ($\approx 6$ V for a differential output). It is important to prevent the feedback capacitor from saturating before the pixel capacitance, but it is also essential
to maintain the feedback capacitor close to the lower limit for a high conversion gain. If the feedback capacitor is too large, the voltage seen at the output for a certain amount of charge will be insignificant.

The feedback capacitors on opposite sides of an opamp must be closely matched for the differential mode to function properly. The smaller the capacitors, the more apparent the mismatches become. We must then find a middle point where the conversion gain is high and the matching of the capacitors is reasonable. The value chosen for \( C_{\text{fb}} \), based on the latter constraint, was \( \approx 60 \, \text{fF} \).

As mentioned in section 4.2.4, the output swing of the opamp can be doubled with a slight alteration in the configuration. The switches enabled by clocks \( \phi_a \) and \( \phi_b \) are the swing enhancement transistors. If the output of the imaging pixel is connected to the positive input and the output of the dummy cell is connected to the negative input of the opamp, the negative output will move up and the positive output will move down. For this case, we can connect the negative output to a low voltage and the positive output to a high voltage so that they can swing to the respective rail. If they had both been reset to the common mode voltage (2.5 V), each output would be limited to 2.5 V of swing before the opamp saturated. In this implementation, the switches are connected to 1 V and 4 V supplies. These values were chosen to ensure that the cascoded transistors remain in the saturation region. The output swing of this enhanced implementation is the full 6 V since each output can swing 3 V.

The switches allow more flexibility since there is a dummy cell in every column, but only one opamp for every two columns. In other words, when the output of the sensing cell is attached to the positive input, the negative output needs to be attached to a low voltage since we expect it to increase. Alternatively, if the sensing cell is connected to the negative input, the positive output needs to be connected to a high voltage since it is expected to decrease. The phase of \( \phi_a \) is identical to \( \phi_1d \) when we want to initialize the negative output to a high voltage and the positive output to a low voltage. In this case, \( \phi_b \) is set to zero.
3.3.2 Clocking Scheme

Figure 3-5 illustrates the clocking scheme used for the reset circuitry. $\phi_1$ represents the reset phase and lasts 25 $\mu$s. The sample phase, which also lasts 25 $\mu$s is described by $\phi_2$. $\phi_1$ and $\phi_2$ are non-overlapping clocks and there is a 7 $\mu$s delay between the two. The rowselect clock which is used to sample an individual pixel shares the rising clock edge with $\phi_2$ but only lasts 1 $\mu$s. This short pulse is intended to read out only the integrated charge and not the charge that is being integrated during the sampling phase. The amplitude of the rowsel pulse was chosen to be 7 V to enable the pixel to charge up to the full 5 V. $\phi_{1d}$ is a delayed version of the reset phase $\phi_1$. The delay in $\phi_{1d}$ eliminates the signal dependence of the charge injection on the input nodes of the opamp.

The duration of each phase was chosen based on the frame rate. A frame rate of 30 frames/second gives us 33.3 ms to read each frame. Since we have one opamp for every two columns, we need to read $256 \times 2$ rows for each frame. The clock period must be 65 $\mu$s. If we add up the durations of $\phi_1$, $\phi_2$ and the rest time in between, we get 65 $\mu$s.
3.3.3 Reset Phase

During the reset phase, shown in figure 3-6, the opamp is in unity gain. The inputs of the opamp are reset to the value of the outputs, 2.5 V. One feedback capacitor is reset to 4 V while the other is reset to 1 V. When the ends of these capacitors are connected to the outputs, they initialize the value of the outputs to enhance the output swing. The capacitance of both lines is reset to 5 V. This figure shows the need for the blocking capacitors.

3.3.4 Sample Phase

Figure 3-7 shows the schematic diagram during the sample phase. The feedback capacitors are now placed in feedback in anticipation for the readout of the pixel. When rowsel goes high, 3/10 of the charge from the photodiode is dumped onto Cline and 7/10 onto Cin. The charge that is present on Cin quickly appears across Cfb. The photodiode is reset at the same time that it is being read. When the rowsel switch is closed, the voltage at Cline (5 V from the reset phase) forces the node of Cpix to charge to 5V since Cline $\gg$ Cpix.

The closed loop gain can be calculated by looking at figure 3-7. The capacitance seen at the input of the opamp is $(Cline + Cpix) || Cin$ or $Cline || Cin$ since $Cpix \ll Cline$. The
closed loop gain, \( \frac{V_a}{V_i} \), is then equal to \( \frac{C_{line}||C_{in}}{C_{fb}} \). Plugging in all the values of Cline, Cin and Cfb, the closed loop gain equals 35.6.

3.3.5 Offset Cancellation

The reset scheme described in the previous sections is also advantageous in cancelling the input-referred offset of the opamp. Figure 3-8 illustrates the reset and sample phases for a single-ended opamp with the offset voltage remaining constant in both cases. The ratio of
the offset voltage seen at the output can be derived by setting the charge at node $V_x$ and $V_x'$ to be equal. The charge at node $V_x$ is then equal to:

$$Q_1 = (V_x - 5V)C_{in} + V_xC_{fb}$$

(3.2)

where $V_x$ equals $\frac{AV_x}{1+A}$. In the second case, the charge at node $V_x'$ is described by:

$$Q_2 = (V_x' - 5)C_{in} + (V_x' - V_{out})C_{fb}$$

(3.3)

where $V_x'$ equals $\frac{-V_{out}}{A} + V_{os}$. The output voltage can now be described in terms of the offset voltage, the open loop gain and the ratio of the feedback and input capacitors:

$$V_{out} = V_{os}(\frac{1}{1+A})(\frac{C_{in} + C_{fb}}{C_{fb}})$$

(3.4)

For the opamp described in this chapter, the open-loop gain is 45,000 and the ratio of $\frac{C_{in}}{C_{fb}}$ is 119. The amount of offset voltage seen at the output has been reduced to $2.6 \times 10^{-3}$ of its original value.

### 3.4 Architecture Summary

This chapter described the architecture used for the imager. The architecture consists of a random access array implemented with CMOS technology. The architecture also features a differential mode in which the output of a sensed pixel is compared with that of a dummy pixel. This differential scheme attempts to reduce the column-to-column variations introduced by substrate bounce and temperature changes. The output circuit of the system was also described.
Chapter 4

Op Amp Design

4.1 Topology

4.1.1 Folded Cascode

The folded cascode topology was chosen for the output stage of the imager. This implementation provides moderate gain and bandwidth and high phase margin and output swing. The capacitance at the load serves as the compensation network. This topology also provides high power supply rejection ratios from both sources since the compensation capacitors are attached between the output of the opamp and analog ground. A schematic diagram of the folded cascode is given in figure 4-1. Table 4.1 lists the corresponding device geometries.

M1 and M2 form an input differential pair. The difference in the voltage at the input sets the difference in the current at the second stage. The differential output voltage is set by the difference in the current and the transconductance of the amplifier. The cascode in the second stage helps improve the gain by increasing the output resistance. M21 and M22 provide the current for the input differential pair. The bias voltages Vbias1, Vbias2 and Vbias3 are generated by the bias circuit described in the following section. A common mode feedback circuit provides the voltage Vbias4 as described in section 4.1.3.

Although it is not specified in the figures, the backs of all p-channel transistors are
Figure 4-1: Folded Cascode OpAmp Schematic Diagram

<table>
<thead>
<tr>
<th>Device</th>
<th>W/L ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>250/1</td>
</tr>
<tr>
<td>M3, M4</td>
<td>60/2.5</td>
</tr>
<tr>
<td>M5, M6</td>
<td>60/2.5</td>
</tr>
<tr>
<td>M7, M8</td>
<td>60/2.5</td>
</tr>
<tr>
<td>M9, M10</td>
<td>30/2.5</td>
</tr>
<tr>
<td>M21</td>
<td>72/1.5</td>
</tr>
<tr>
<td>M22</td>
<td>180/1.5</td>
</tr>
</tbody>
</table>

Table 4.1: Folded Cascode Transistor Sizes in μm
connected to their respective sources and the backs of all n-channel transistors are connected to the substrate.

4.1.2 Biasing

Figure 4-2 shows the circuit used to provide the bias currents and voltages to the folded cascode. The p-channel transistors (M12, M13, M15 and M16) set the bias voltages, Vbias1 and Vbias2, while the n-channel transistors (M17-M20) set Vbias3. M12, M15 and M16 are sized equal to M5-M8. M13 is sized much smaller to ensure that M12, M15 and M16 stay in saturation [13]. A similar approach is used for the n-channel bias circuit. M18 and M20 are sized equal to M3 and M4 while M19 is sized equal to M9 and M10. These devices stay in the saturation regime due to the small geometry of M17. The final device geometries are shown in table 4.2. In order to maintain a current of approximately 1.5μA through each of the legs of the folded cascode, Iref was set to 100μA and the W/L ratio of M11 to M14 was set to 100:1. In retrospect, the value of Iref does not need to be this high. It is actually a better design technique to set the current of all legs of the opamp to be of the same order.
<table>
<thead>
<tr>
<th>Device</th>
<th>W/L ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>M11</td>
<td>1800/1.5</td>
</tr>
<tr>
<td>M14</td>
<td>18/1.5</td>
</tr>
<tr>
<td>M12, M15, M16</td>
<td>60/2.5</td>
</tr>
<tr>
<td>M13</td>
<td>10/5</td>
</tr>
<tr>
<td>M18, M20</td>
<td>60/2.5</td>
</tr>
<tr>
<td>M17</td>
<td>7.5/15</td>
</tr>
<tr>
<td>M19</td>
<td>30/2.5</td>
</tr>
</tbody>
</table>

Table 4.2: Bias Circuit Transistor Sizes in um

<table>
<thead>
<tr>
<th>Device</th>
<th>W/L ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>M23, M24</td>
<td>30/2.5</td>
</tr>
<tr>
<td>M25, M26</td>
<td>60/2.5</td>
</tr>
<tr>
<td>M27</td>
<td>144/1.5</td>
</tr>
<tr>
<td>M28</td>
<td>180/1.5</td>
</tr>
</tbody>
</table>

Table 4.3: Common Mode Feedback Circuit Parameters

4.1.3 Common Mode Feedback Circuit

Due to the differential mode configuration of the opamp, a common mode feedback scheme is needed to maintain the output voltages at the common mode. Without a common mode feedback circuit, the output voltages will move to either rail. Figure 4-3 shows the switch capacitor circuit used for this design and table 4.3 lists the transistor sizes. The $\frac{W}{L}$ ratios of all nmos and pmos transistor switches for this circuit were $\frac{7.5\mu}{1\mu}$. The value of the capacitors was chosen to be 150 fF. The upper limit for this capacitance was the RC time constant for the settling time and the lower limit was imposed by the charge injection of the transistor switches.

The switch capacitor circuit is used as a detector of the common mode level. Let us say that the common mode voltage is higher than its normal value. This change in the common mode will increase the gate voltage of M24 and decrease the current through that leg. In order to maintain a constant current through M27 and M28, there is an increase in the
current through M23 and M25 which increases Vbias4. When Vbias4 increases, the current through both M3 and M4 increases and consequently the voltage through the active loads increases and pulls down the common mode of the output.

The phase diagrams of φ1 and φ2 are described in section 3.3.2.

4.2 Opamp Characteristics

4.2.1 Specifications

The opamp design at the output stage must provide a reasonably high gain (> 10,000) in order to minimize the error. It would be ideal to have an opamp with infinite gain, but since there are other specifications that must be met, a gain greater than 10K should be sufficient.

The specification of the bandwidth can be derived from the sampling rate of the imager and the closed-loop gain of the amplifier. The sample rate of 30 frames/sec is one of the specifications provided by the system. The time allotted to sample each row is then:
\[ T = \frac{1}{(30 \text{ frames/sec})(256 \text{ rows/frame})} \approx 130 \mu s \quad (4.1) \]

Since we have two rows for every opamp, we have approximately 65 \( \mu s \) to sample each row. For a 10-bit resolution (also provided by the system specifications), we need to settle to approximately 8 time constants, leading to a time constant, \( \tau \), of 8.13 \( \mu s \).

The closed-loop gain, which is explained in more detail in section 3.3, was calculated to be around 36 based on the ratio of the feedback and input capacitance of the opamp. The unity-gain frequency can then be expressed as:

\[ UGF = \frac{G_{cl}}{2\pi \tau} = 697k\text{Hz} \approx 1MHz \quad (4.2) \]

where \( G_{cl} \) is the closed-loop gain and \( \tau \) is the time constant. 1 MHz is then the lower limit of the unity-gain bandwidth. The upper limit is set by the amount of noise that can be tolerated since noise is integrated over frequency.

**4.2.2 Gain and Bandwidth**

The open-loop gain of the folded cascode is described by 4.3:

\[ A_o = g_m(9r_0r_o)(9r_0)(9r_0)(9r_0)(9r_0) \]

where \( g_m \) is the transconductance and \( r_o \) is the output resistance of the respective transistors. Note that the parameters of transistors M1 and M2, M5 and M6, M7 and M8, M9 and M10 and M3 and M4 are interchangeable. Figure 4-4 shows the open loop gain of the opamp around 45,000, which is more than the specifications required.

The dominant pole is due to the capacitors at the load. The values of these capacitors were chosen to provide the bandwidth required. The frequency of the first pole is determined by: \( \frac{1}{R_oC_l} \) where \( R_o \) is the output resistance of the opamp and \( C_l \) is the load capacitance. The unity gain bandwidth is then the open-loop gain times the frequency of the first pole or \( \frac{g_m}{C_l} \). For a \( C_l \) of 3.9 pF, the unity gain frequency (shown in figure 4-4) is at 5 MHz.
Although this value is slightly higher than the specified value and it will introduce extra noise, it provides a safe margin to work with.

### 4.2.3 Phase Margin

Figure 4-5 shows the phase of the opamp. Due to the low specification for the bandwidth, the gain of the opamp reaches unity at a much lower frequency than the second pole. This large split between the two poles provides a phase margin of $89^\circ$. It can be noted from the figure that the second pole (caused by parasitic capacitances on the nodes between M3 and M9 and M4 and M10) appears at a frequency of approximately 100 MHz.

### 4.2.4 Swing

As figure 4-6 illustrates, the output swing of the opamp was high. The high gain region was measured wherever the slope of the curves was greater than 10,000, the initial gain specification. The output nodes can swing down to 177 mV and up to 4.80 V. Due to the differential nature of this opamp, the output swing can be doubled from that shown in the figure if the output voltages are properly set. Since the positive output node moves up when
Figure 4-5: Folded Cascode Phase

the negative output node moves down, the output swing can be greater than the supply voltage. Section 3.3 shows the configuration that allows the output swing to improve.

4.2.5 Power

The total power dissipation of a single opamp was calculated to be 94.3 $\mu$W. This figure includes the power dissipation in the folded cascode itself, the bias circuit and the common mode feedback circuit. In the folded cascode, a current of 3.52 $\mu$A through transistors M3 and M4, leads to a power dissipation of 35.2 $\mu$W. In the bias circuit, the total current of 4.5 $\mu$A dissipation 22.1 $\mu$W. Finally, in the common mode feedback circuit, the power dissipation of 37 $\mu$W is due to two legs of current of 3.7 $\mu$A each.

4.3 Noise Analysis

The noise in the operational amplifier can be calculated from the noise of the individual devices referred back to the input. The noise for a MOSFET in saturation can be described by:
Figure 4-6: Output swing for positive and negative output nodes

\[ \overline{v_{eq}^2} = 4kT \frac{2}{3} g_m \Delta f \]  \hspace{1cm} (4.4)

where \( g_m \) is the transconductance of the transistor. Since we want to refer the noise from each transistor back to the input, the noise from devices M3-M10 must be multiplied by a transconductance ratio. For instance, the noise seen at the input due to transistor M3 is:

\[ \overline{v_{eq}^2} = \left( \frac{g_{m3}}{g_{m1}} \right)^2 \left( 4kT \frac{2}{3} \frac{1}{g_{m3}} \Delta f \right) \]  \hspace{1cm} (4.5)

The ratio of the transconductances must be squared since we are dealing with noise spectrum density. The overall noise seen at the input due to all devices in the folded cascode is:
Figure 4-7: Noise Analysis

$$v_{eq}^2 = 4kT \frac{2}{3} \left( \frac{2}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}} \right)^2 4 \frac{2}{g_{m9,10}} \frac{2}{g_{m9,10}} + \frac{g_{m5,6,7,8}}{g_{m1,2}} \frac{4}{g_{m5,6,7,8}} \right) f$$  (4.6)

Plugging in all the value of the transconductances, the numerical value for the total noise spectrum density is $1.16 \times 10^{-15} \Delta f$.

The total value of the noise must be calculated in the opamp's closed-loop configuration (shown in figure 4-7) since our concern is the noise during the sampling phase. In this configuration, the frequency range is:

$$\Delta f = \frac{5 MHz \pi}{36} \frac{\pi}{2}$$  (4.7)

where $\frac{5 MHz}{36}$ is the cutoff frequency when the opamp has a closed-loop gain of 36. The factor of $\frac{\pi}{2}$ is added to account for the fact that the 3dB point does not end abruptly.

Recalling that the total noise spectrum density was $1.16 \times 10^{-15} \Delta f$, if we incorporate Eq. 4.7 into the latter equation, we get an input-referred noise spectrum density of:

$$\overline{v_{eq}^2} = 1.16 \times 10^{-15} \frac{\pi 5 MHz}{2} \frac{5 MHz}{36}$$  (4.8)

The noise we see at the output is then the quantity in Eq. 4.8 combined with the square
of the closed-loop gain, $36^2$:

$$\overline{v_{eq}^2} = 1.16 \times 10^{-15} \frac{\pi 5MHz}{2} \frac{36}{36^2}$$  \hspace{1cm} (4.9)$$

giving a final value of 573 $\mu$V at the output.

4.4 Output Buffer

A source follower was used as a buffer at the output of the opamp to enable it to drive the output pin without affecting the performance of the opamp. Figure 4-8 illustrates the connection between the opamp and the source follower. Transistors M101 and M102 were used as the source followers. Their W/L ratios were set to 200u/.8u and I_in was set to 400 $\mu$A to give a small-signal gain of 0.98. The opamp is shown in its sample phase with the imaging and dummy capacitances connected to the inputs.
Chapter 5

Layout

5.1 Process Information

The imager was laid out using the HP 0.8 $\mu$m process design rules. This silicided process consists of one layer of poly and three layers of metal. Two layers of metal were used for routing and the third layer of metal was used as a light shield for the opamp and the ESD protection circuit. Although the final minimum gate length is expected to be 0.8 $\mu$m, the actual drawn value is 1.0 $\mu$m and the minimum geometry size is 0.5 $\mu$m.

5.2 Pixel Cell

The final layout of the passive pixel cell is shown in figure 5-1. The most challenging part of laying out the pixel was in maximizing the fill factor and minimizing the overall pixel area at the same time. The row select transistor was kept at minimum size (2.5u/1u) to increase fill factor. The size of the overlap between n+ diffusion and n-well was set at the minimum geometry size, 0.5 $\mu$m, since only a small area of diffusion is required to make contact with the well. The distance between the n-well and the poly gate of 1.75 $\mu$m, or the extension of diffusion beyond the n-well was chosen to be similar to the minimum distance between n+ diffusion and n-well.
The overlap between the n+ diffusion and the n-well is 0.5 um and the extension of the n+ diffusion beyond the n-well is 1.75 um. The active area of the rowselect transistor is light shielded with metal2.

The large spaces from n-well to n-well were used to run metal lines. Metal1 was oriented vertically to run the column lines and metal2 was oriented horizontally to carry the rowselect lines.

The pixel layout shown in figure 5-1 has an area of $15.5\mu m \times 15.5\mu m$ and a 40% fill factor.

5.3 Dummy Cells

Two variations of the dummy cells were laid out. Both were based on the pixel layout discussed above. The photodiode area of the first one was light-shielded with metal3. The light-shield of the second dummy cell was made out of silicide. The entire n-well region of this pixel was covered with n+ diffusion to ensure that silicide would be placed on top of it.
5.4 Pixel Array

The pixel array for this test chip consists of 256 rows by 4 columns. All four columns have connections to output pins, but only certain rows were selected to be read out. Three rows were chosen from the top of the array, three from the middle and three from the bottom. All four dummy cells can be selected for readout.

The pixel array was surrounded by a protective guard rail. This guard rail, which consists of an n-well tied to Vdd, prevents any carriers generated outside the array from being collected by the pixels in the array.

5.5 Opamp

There were two opamps in the imager chip. It was mentioned in chapter 3 that the number of columns per opamp depends on the relative widths of the column and the opamp. If we place one opamp above the array and one below it, we have four column widths per opamp, or 62μm. Since this width was still not sufficiently large enough to make a reasonably sized opamp, the number of columns per opamp was increased to four. The width of the opamp is now constrained to 124μm.

In order to reduce the systematic offset of the opamp, the opamp was laid out symmetrically wherever it was possible. The common mode feedback circuit used common centroid techniques to improve the matching of the capacitors [14]. The smaller capacitors (less than 300 fF) were made out of polysilicon and metal. The larger capacitors were implemented with pmos transistors with the source, drain and back tied together to form the negative plate and the poly was the positive plate of the capacitor.

The opamp was light-shielded with metal3 and a guard rail was placed around its boundaries.
5.6 Electrostatic Discharge Protection (ESD)

The protection circuits used for input/output pads are shown in figures 5-2, 5-3 and 5-4. Most input/output pins were connected to the ESD protection circuit shown in figure 5-2. This protection circuit consists of a high threshold field transistor, a pn diode and a resistor. When a voltage higher than 5 V is connected to the pad, the pn diode turns on and the current flows to the high rail. When the input voltage is higher than the threshold voltage of the field transistor, the current is discharged to ground through this device.

The protection circuit for power and ground pins shown in figure 5-3 is similar to the previous circuit with the exception of the resistor at the output.

The protection circuit for the row select pins must allow voltages as high as 7 V. Figure 5-4 shows the implementation used for these pads. There is thus a slight variation where the pn diode is replace by another diode-connected high-threshold field transistor.

Figures 5-5, 5-6 and 5-7 show the implementation of the pn diode, high-threshold metal 2 field transistor and the resistor respectively.

5.7 Complete Layout

The complete layout of the chip is shown in figure 5-8. The final die size was 1171 \( \mu \text{m} \times 7922 \ \mu\text{m} \).
Figure 5-3: Power and Ground Pads

Figure 5-4: Pads for voltages greater than 5V

Figure 5-5: Implementation of a pn diode
Figure 5-6: Implementation of Metal2 Field Transistor

Figure 5-7: Implementation of Resistor
Figure 5-8: Complete Layout
Chapter 6

Results and Discussion

6.1 Test Setup

6.1.1 Chip Structure

As chapter 5 indicates, the test chip designed for this thesis consists of an array of $256 \times 4$. There are two fully-differential opamps, one for every two columns. A source follower is used to buffer each one of the opamp outputs. The chip lacks a row decoder and only four pixels can be accessed per column. The gates of the non-accessible row select devices are connected to ground. Figure 6-1 shows a schematic diagram of the imager chip.

6.1.2 PC Board

A PC board was implemented to generate the currents, voltages and clocks for the chip. The voltage references consist of a series of resistive divider circuits while the current sources for the opamp and output buffers use bipolar components and resistors. The different phases of the clocks were generated using two synchronous counters and a programmable array logic (PAL) chip. The rowsel phase was buffered through a 7407 buffer and level shifted to 7 V with a series of resistive networks.

Figure 6-2 shows the clock phases used for testing. Note that the clock period is ten times slower than required for the 30 frames/s sample rate. Subsequent figures show the presence
of a light-dependent parasitic current in one of the column lines. At high illumination levels, the opamp saturates quickly due to the parasitic current and does not leave enough swing for the pixel charge to be measured. It was thus necessary to lower the illumination levels to reduce the negative effects of this parasitic current. The clock frequency consequently had to be lowered to provide the pixel with enough time to accumulate charge in the n-well. The purpose of a long reset phase ($\phi_1$) and a short sample phase ($\phi_2$) is to extend the integration period for a pixel and decrease the effects of the parasitic current during the sample phase.

6.1.3 Illumination

A lamp attached to an integrating sphere was used as the source of illumination. The purpose of the integrating sphere is to yield uniform illumination to a specific area. Filters were used to eliminate all IR light and to attenuate the light intensity by 100 times. The light intensity was adjusted with the power supply of the lamp. Figure 6-3 shows the relationship between the illumination power and the input voltage of the lamp's power.
supply.

The system was placed in a dark compartment and the outputs of the source followers were observed in an analog oscilloscope for varying light intensities.

6.2 Results

6.2.1 Output Waveforms

Figures 6-4, 6-5 and 6-6 show the output waveform in response to an illumination of 4 μW/cm². The only difference in the conditions is the number of pixels selected: none in figure 6-4, one in figure 6-5 and two in figure 6-6. The middle waveform shows the sample phase and the bottom one is the row select clock.

Contrary to expectations, the first waveform shows a ramp indicating the presence of a parasitic current in one of the inputs of the opamp. The slope of this ramp increases with light intensity. Since no pixels are selected, it is not surprising that the rising edge of the row select clock has no effect on the output waveform.
Figure 6-3: Relationship between illumination power and input voltage with an attenuation filter of 100:1

The response of the imager when one pixel in the first column is selected for readout shows a jump in the output immediately after the rising edge of the row select. This voltage difference corresponds to the charge that is being dumped on the first column line. The parasitic current from the previous case is still present.

This trend is repeated in figure 6-6 which shows the output waveform when two pixels from column 1 are selected for readout. As expected, there is an increase in the jump at the rising edge of the row select since the charge from two pixels is being dumped on the first column line.

The slope of the ramp in the case when no pixels are selected for readout was found to be approximately the same as the initial and final slopes in the other two figures. Even in the presence of the parasitic current, it is possible to measure the change in voltage due to the charge collected in a single pixel. Figure 6-7 shows the procedure used to measure the size of the signal. The offset voltage is subtracted from the output voltage leading to a voltage that corresponds solely to the pixel charge.

The limitations of these measurements arise for high illuminations when the parasitic
Figure 6-4: Output Waveform with no pixels selected for readout indicates the presence of a parasitic current.

Figure 6-5: Output Waveform with one pixel selected for readout.
current is so large that the opamp saturates before the pixel charge is dumped onto the column line. At low illumination levels, the slope of the ramp is low and the voltage corresponding to the pixel charge is also low. As the light intensity is increased, the slope of the ramp as well as the pixel response continue to increase until the opamp saturates and an accurate response can no longer be taken.

6.2.2 Optic Response

The differential voltage in response to pixel charge was measured at different illumination levels. The optic response of the imager is shown in figure 6-8. The bottom curve shows the output when one pixel is selected for readout and the top curve shows the output when two pixels are selected for readout. The slopes of the lines are 94.1 mV cm$^2/\mu W$ and 61.7 mV cm$^2/\mu W$ for the top and bottom curves respectively giving a ratio of 1.5:1. This linear dependance on illumination shows that the system is functional and well-behaved for low illumination levels.

Assuming that the illumination through the entire pixel array is uniform, the pixel
6.2. RESULTS

Figure 6-7: Behavior of output waveform at various illumination levels

Figure 6-8: Optic response of imager with one (o) and two pixels (+) selected for readout
Figure 6-9: Comparison of individual optic responses to pixel in the top cf the array (o) and pixel in the middle of the array (*)

charge from two pixels should be twice as much as the pixel charge from one pixel. The slopes of the curves shown in figure 6-8, however, show that this ratio is only 1.5:1. The optic response of the second pixel alone was observed and compared with the response of the first pixel (figure 6-9). There is a difference of 22 mV cm²/μW between the two slopes, indicating that there is a variation in the illumination of the two pixels and making the initial assumption invalid.

It is not surprising to find this type of illumination difference since the pixel with a higher slope is located at the top of the array while the second pixel is in the middle of the array. This mismatch in illumination arises from an inadequacy in the setup where the pixel array could not be placed directly in the mouth of the integrating sphere.

Figure 6-10 shows the response due to the pixel at the top of the array (o), the pixel in the middle of the array (*) and the two pixels selected together (+). The fourth curve (x) displays the sum of the two individual responses. There is only a slight difference, probably due to experimental error, between the actual output with the two pixels selected and the sum of the individual responses demonstrating that the system is also well-behaved when
Figure 6-10: Optic response of two pixels being selected together (+) compared with the sum of the individual responses (x)

two pixels are selected for readout.

6.3 Discussion

6.3.1 Origin of Parasitic Current

A possible explanation for the parasitic current present in the previous figures is a mismatch in the layout of the pixel array. Figure 6-11 illustrates the mismatch in the layout of the first and second columns. The lack of a light shield between the guard rail and the first column leads to a significant amount of photogeneration. Most of this charge goes onto the first column line and behaves as a constant current source. As shown in figures 6-4 through 6-6, the output voltage increases when pixels on this column are selected for readout, providing further evidence that the parasitic current is connected to the first column.

Figures 6-12 and 6-13 show the output waveform when one and two pixels are selected on the second column respectively. The waveform begins as usual with a ramp, but is severely disturbed at the rising clock edge of the row select. The charge dumped on the
Figure 6-11: Layout of the pixel array
Figure 6.12: Output Voltage effect of selecting one pixel in second column on parasitic current

second column works against the parasitic current on the first column and the outputs of the amplifier consequently shift directions. Once the opamp has settled to the value corresponding to the pixel charge, the outputs continue to ramp up in the original direction.

6.3.2 Second Order Effects

Although not as blatant as the effects of the parasitic current, there are some second order effects, namely blooming and subthreshold conduction, that could affect the behavior of the system at high illumination levels. Since these two effects are common to both columns, the differential nature of the output circuit rejects them and their consequences are not visible at the output.

Blooming occurs with excessive light input when the potential wells become full of electrons even before the end of the integration period. The excess carriers spill over into the substrate and might find their way into neighboring pixels. In this design, the danger exists for the pixels that are never selected for readout and therefore are never reset. One of the possible fates of the spilled charge is simply to get collected in the column lines during
the sample phase and get interpreted as pixel charge.

The second problem that could arise from the lack of a reset scheme for non-accessed pixels is subthreshold conduction. Since the gates of these row select devices are tied to ground, subthreshold conduction is possible if the n-well potential drops below zero. Figure 6-14 shows the subthreshold characteristics of a row select device.

6.4 Recommendations

In light of the problems experienced in this design, some recommendations can be made to improve the quality of this passive pixel imager. First, a metal light shield should be used over the entire pixel array with windows over the photodiode area. This type of light shield will help prevent the parasitic current problem faced in this project.

If no decoder is present, a reset scheme should be included in the design so that all pixels are reset during every cycle. The gates of the row select devices of the non-accessible pixels should be tied together and made accessible from off-chip. In this way, subthreshold
conduction can be avoided by setting these gates to a voltage lower than 0 V.

6.5 Results Summary

The optic response of the imager was presented in this chapter. Even in the presence of a parasitic current, the voltage corresponding to the pixel charge was visible. The experimental data presented showed that the imager is functional and well-behaved for low illumination levels. A possible source of the parasitic current was hypothesized and proven with scope photographs. Although not blatant in the scope photographs, blooming and subthreshold conduction were also described as possible problems due to the lack of a reset scheme for non-accessible devices. Some recommendations were made to improve the quality of the passive pixel imager.
Chapter 7

Conclusions

A differential passive-pixel image sensor has been designed and implemented with an N-well photodiode in the Hewlett-Packard CMOS26B 0.8 μm process, available through MOSIS [15].

The n-well photodiode has many advantages over the conventional n-diffusion photodiode. A higher quantum efficiency can be achieved due to much longer diffusion lengths and larger depletion widths. The lack of silicide on the n-well photodiode also leads to a higher quantum efficiency. The larger depletion width of the n-well photodiode yields a lower pixel capacitance and consequently a higher signal to noise ratio than the n-diffusion photodiode.

One of the few disadvantages of the n-well photodiode is the minimum size and minimum spacing required by the layout design rules. A passive pixel implementation, consisting of only a row select transistor and a photodiode, permits the use of an n-well photodiode and yields a pixel with a high fill factor in a reasonable area.

A CMOS random access architecture is ideal for power savings. In contrast to a CCD array, a CMOS architecture allows separate and independent access of each pixel and saves power by doing so.

A differential architecture allows a sensing pixel to be compared with a dummy cell that is kept in the dark. The output voltage then purely corresponds to the sensed charge. This differential scheme reduces the column-to-column variation in large arrays by rejecting
substrate bounce or effects due to temperature changes.

Experimental results show that the imager is functional and well-behaved at low illumination levels.
Bibliography


