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Abstract—**We present an optimized fabrication process for superconducting nanowire single-photon detectors (SNSPDs) that allowed us to obtain a yield of ~ 70 % for detectors based on 80-nm-wide niobium nitride nanowires. We fabricated detectors that showed 24-ps timing jitter and saturated detection efficiency without the need for cryogenic amplifiers, allowing for operation in a low-bias low-dark-count-rate regime while operating at maximum detection efficiency.**

Index Terms— **Single-Photon Detectors, Infrared Photon Detectors, SNSPDs, SSPDs, Niobium Nitride**

I. INTRODUCTION

SUPERCONDUCTING nanowire single-photon detectors (SNSPDs [1]) offer high detection efficiency [2-4], sub-50-ps timing jitter [5, 6] and sub-50-ns-dead time [7] for near-infrared photons. The unique combination of these characteristics has led to rising interest and development towards SNSPD arrays for high-speed free-space telecommunication [8-10], imaging applications with single-photon sensitivity [11-13] and on-chip photonic quantum processors [14]. One of the core challenges in scaling up the number of detectors has been the nanofabrication yield, which can be small for low-jitter SNSPDs due to non-uniformities in the superconducting film and defects introduced during fabrication [15].

In the course of this paper we will discuss the steps we took to increase the yield and switching current of our detectors:

(1) We optimized the niobium nitride (NbN) growth and detector fabrication processes to reduce defects

(2) Given the optimized film and fabrication parameters in (1), we investigated the nanowire geometry required for saturated detection efficiency

(3) We investigated the dependence of timing jitter on nanowire width and bias current and found the main limit to be the signal-to-noise ratio (SNR). Based on this result we selected the widest nanowire investigated in step (2) that could reach saturation.

(4) In order to further increase the signal-to-noise ratio, we used a parallel-nanowire architecture, superconducting nanowire avalanche photodetectors (2-SNAP [16-18])

Using the improved process we fabricated detectors that, measured with 3-GHz-bandwidth room-temperature amplifiers, exhibit 24 ps timing jitter in single-photon regime [19], current-independent detection efficiency and high count rates simultaneously over an active area of 22 μm^2 for 1550-nm-wavelength light.

Current-independent detection efficiency (DE), commonly referred to as saturated DE, is sign of high internal efficiency [2, 3, 20], low sensitivity to electrical noise [18] and high yield. However, to date the timing jitter of saturated detectors has been limited to 35 ps [6] in niobium nitrode (NbN) and 60 ps [21] in tungsten silicide (WSi). Our sub-30-ps timing-jitter detectors were saturated over a bias current range of up to 3.5 μA, the largest current range reported to date, allowing for operation in a low-bias-current low-dark-count-rate regime while operating at maximum detection efficiency. Furthermore, these detectors were based on ~ 80-nm-wide nanowires, thus relaxing the nano-fabrication requirements in terms of resolution compared to ultra-narrow nanowires in NbN [18]. Once internal efficiency is optimized, the detection efficiency can, as demonstrated by various groups, be increased with additional optical structures such as cavities [2, 3, 22] or plasmonic structures [23].

II. OPTIMIZED FABRICATION PROCESS

Film quality is crucial for detector performance. We used the metrics sheet resistance (Rs) and critical temperature (T_C) to characterize our films. High T_C is associated with high sheet

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current density and possibly low timing jitter, while high R_S could be associated with higher sensitivity due to larger Joule heating [25]. In accordance with previous work [18] we targeted R_S = 450-550 $\Omega/\square$ and a T_C as close as possible to the bulk T_C .

We deposited NbN by Reactive DC Magnetron Sputtering onto double-polished Si substrates covered with ~300-nm-thick chemical-vapor-deposited silicon nitride (SiN_x). During the NbN deposition the substrate holder was heated to a nominal temperature of 800°C. In addition to heating the holder the substrate itself was heated directly from halogen heat lamps via a hole in the substrate holder. Using this method we obtained films that at a given T_C had comparable or higher R_S than our previous films. Table 1 contains a list of R_S and T_C values of films used for data shown in this paper. Our reference film (film #1) had R_S = 515.5 $\Omega/\square$ and T_C = 10.9 K. The thickness of this film, estimated by optical transmission measurements, was ~ 4.3 nm. Compared with our previous films on sapphire in Ref. [18] (R_S = 480 $\Omega/\square$ and T_C = 10.8) these films had higher R_S and higher T_C.

film ID	old film	1	2	3	4	5	6
R_S ($\Omega/\square$)	480	516	504	533	586	525	444
T_C (K)	10.8	10.9	10.5	10.5	10.1	10.6	11
used in	Ref. [18]	Fig. 8	Fig. 4	Fig. 4	Fig. 7	Fig. 10(b)	Fig. 10(a)

Table 1. List of films used for data shown in this paper.

We modified our previous fabrication process [18] as follows: (1) We replaced the single-layer liftoff process, used for the initial fabrication of gold contact pads, with a bilayer liftoff process; (2) we reduced the exposure time of bare NbN to tetra-methyl-ammonium hydroxide (TMAH), used for adhesion promotion of the detector resist layer; (3) we performed post-reactive ion etch (RIE) imaging to minimize damage to the nanowires during pattern transfer from the detector resist layer into the NbN.

Figure 1 shows the resist mask for two detectors on top of gold pads fabricated with the old (a) and the new liftoff process (b). The Au pads in Fig. 1(a) were fabricated using a single layer of photoresist (Shipley S1813) as evaporation mask for gold liftoff. Due to the small size of our samples (1cm × 1cm square), the photoresist thickness on the edges was significantly larger than in the center of the sample (detector region), preventing tight contact between the photomask and the photoresist during exposure. The lack of reliable contact often resulted in rough edges of gold pads after liftoff, as outlined in red in Fig. 1(a), and defects at the interface between detector resist mask and gold pad. These defects, often localized in certain regions on

the detector chip, resulted in severed detector-to-Au-pad connections (open circuit) or large electrical resistance at the interface, which caused detectors to latch [25] and decreased the overall detector yield of the chip which typically included a matrix of ~ 50 - 200 detectors. In order to address this problem we transitioned to a bilayer liftoff process (see appendix). As shown in Fig. 1(b) the new process resulted in smooth gold pad edges and reduced the number of detectors that suffered defects at the gold pad-NbN interface.
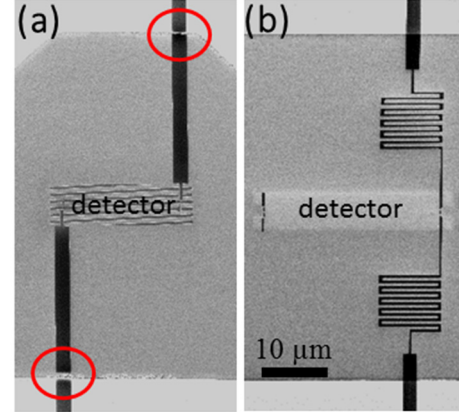

Fig. 1. (a) Patterned e-beam resist on top of gold pads defined via single-layer liftoff process. The red circles highlight the interface between detector resist mask and the electrical contact pads (Au pads). (b) Patterned e-beam resist on top of gold pads defined via bilayer liftoff process.

We reduced the exposure of our films to TMAH in order to minimize damage to the film. The detectors were patterned via electron-beam lithography using hydrogen silsesquioxane (HSQ) as a resist (see appendix). Our previous fabrication process [26] included a 4-minute long TMAH dip as adhesion promotion step before the HSQ was spun on to the sample. However, we found that this step decreased the T_C by up to 0.3 K while increasing the R_S, as shown in Fig. 2, possibly associated with a thinning of the film. Our new process included a TMAH dip of at most 15 seconds, which we found sufficient in promoting HSQ adhesion.
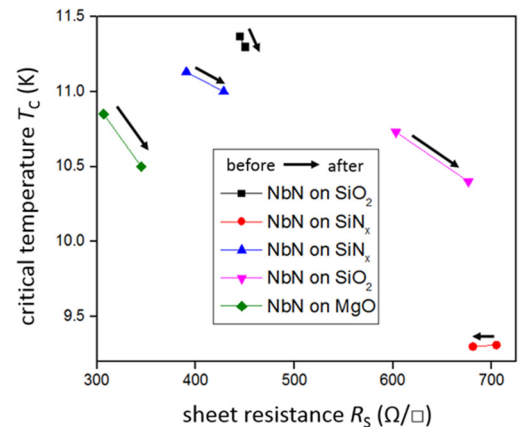

Fig. 2. Sheet resistance vs. critical temperature of NbN samples on a variety of substrates before (bottom of arrow) and after a 4-minute-
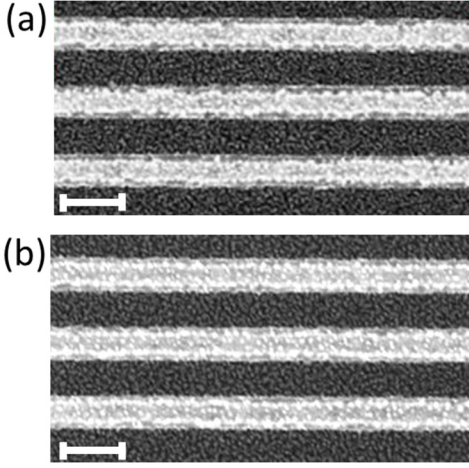
Fig. 3. (a) Top-down SEM of slightly over-etched NbN nanowires on SiN_x. (b) SEM of NbN nanowires on SiN_x with optimized etch time. The equivalent length of the white scale bar is 200 nm.

long dip in TMAH (tip of arrow).

After electron-beam exposure and development the detector resist pattern was transferred into the underlying NbN via RIE (see appendix). In contrast to sapphire, which we used as substrate in previous work [18, 27], our current SiN_x-on-Si substrate did not exhibit significant charging during scanning-electron microscopy (SEM), and enabled high-contrast post-RIE imaging of NbN nanowires, which allowed us to optimize our RIE process. Figure 3 (a) shows a detector without optimized RIE: while the HSQ mask was exposed with the correct dose (obtained from recent dose matrix), the detectors appeared over-etched. The red circles mark regions with severe constrictions. Interestingly, the over-etched features on the edges of the nanowires would not be visible for nanowires fabricated on Sapphire due to charging and low contrast. We found that a fixed RIE time (2 minutes 40 seconds, see appendix) and power (50 W) did not always yield the same effective etch rate. Over time the plasma voltage changes,

presumably due to contamination in the etch chamber. This resulted in a change in etch rate. We found that over-etch can be avoided by decreasing the etch time (~ 2 minutes 10 seconds), imaging the detectors, and etching further in 10- to 15-second steps if needed. Using this modified etch scheme we obtained better nanowire uniformity, shown in Fig. 3(b).

III. DETECTOR DESIGN

Our main objective was to design a detector that showed both saturation and sub-30-ps timing jitter without the need for cryogenic amplifiers. In order to achieve this goal we examined the saturation behavior and timing jitter as a function of nanowire width and bias current.

Figure 4(a) shows the normalized photon count rate (PCR) for 1550-nm-wavelength photons as a function of the detector bias current I_B normalized by switching current I_{SW}. We quantify saturation by introducing a saturation metric S, defined as

$$S = \frac{I_{SW} - I_B(0.9\,PCR(I_{SW}))}{I_{SW}}$$

, where $I_B(0.9\,PCR(I_{SW}))$ is the bias current at which the PCR has reached 90 % of its maximum value. Using this metric, $S = 0$ represents an unsaturated detector while $S = 1$ describes a detector that is saturated over its entire bias current range. Figure 4(b) shows S as a function of I_{SW} for the detectors in Fig. 4(a). As we had found earlier [18] decreasing width results in a smaller I_B/I_{SW}-dependence of the PCR at high bias currents.
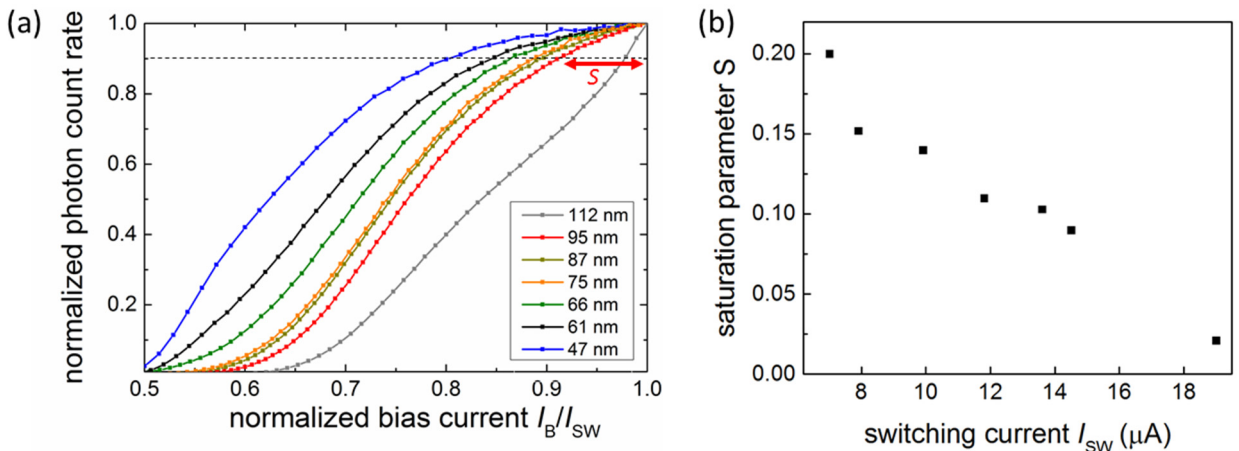

Fig. 4. (a) Normalized photon count rate vs bias current I_B normalized by switching current I_{SW} for nanowire widths ranging from 47 nm to 112 nm. The red arrow denotes the saturation parameter S for the 95-nm-wide nanowire. (b) Saturation parameter S vs switching current for the detectors shown in (a).
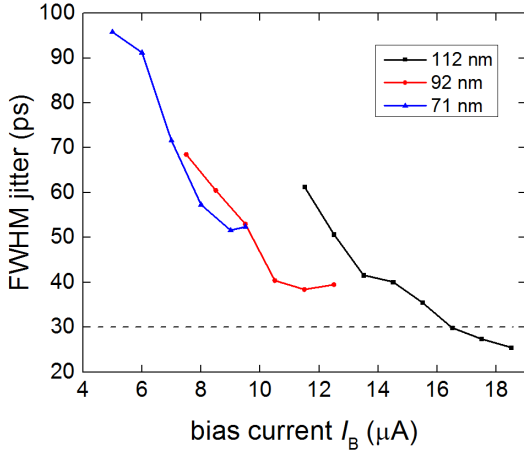
Fig. 5. Timing jitter vs. bias current for SNSPDs based on 71-, 92- and 110-nm-wide nanowires.

Figure 5 shows the timing jitter, defined as the full-width-at-half-maximum (FWHM) of the photodetection delay histogram (instrument response function IRF) as a function of nanowire width and bias current. The measurement setup was identical to [6]. At high I_B/I_{SW} the FWHM jitter seems to be mainly limited by the signal-to-noise ratio [6], although at low bias currents wider nanowires appear to have larger timing jitter.

While narrower nanowires resulted in a more saturated *PCR* vs. I_B curve, indicated by increasing S, they had smaller I_{SW} and hence larger jitter. In order to achieve sub-30-ps timing jitter a detector would need to have $I_{SW} > 16.5$ µA (see dashed line in Fig. 5). A 2-SNAP based on 60-nm-wide nanowires appears to fulfill both requirements of high S and low timing jitter. An SEM of an exemplary detector is shown in Fig. 6. The detectors consisted of 4 2-SNAP units in series [17, 28] as discussed in Ref. [14], each unit comprising two ~ 60- to 80-nm-wide nanowires (200 nm pitch) in parallel. We refer to this design as a series-2-SNAP. This detector had a long rectangular shape for subsequent integration with waveguides [14].

IV. DETECTOR PERFORMANCE AND YIELD

Based on the experiments on SNSPDs described in the previous section we designed SNAPs that could meet our requirement of large-bias-current-range saturation and low timing jitter.

The detection efficiency was measured at 2.4 K in a cryogenic probe station using a polarized incoherent CW source. The detectors were back-illuminated (through the Si substrate) and the polarization adjusted to achieve maximum efficiency. Fig. 7(a) shows the device detection efficiency vs bias current for a series-2-SNAP based on ~ 60-nm-wide nanowires. In this paper we will not discuss the unstable regime below the avalanche current I_{AV}, as this regime is discussed in detail in Ref. [24]. When biased above I_{AV} the detector showed a characteristic 'saturation plateau' with a detection efficiency value close to the calculated optical absorption of ~ 14.5 % (see appendix). The absorption values on our substrate were lower than typical absorption values on sapphire [29] due to the higher refractive index of silicon, which results in significant back-reflection at the substrate-vacuum interface. This is a common problem with Silicon that has been solved elsewhere [2-4].

When biased well within the saturation regime, at $I_B = 15.9$ µA, this detector had a timing jitter of ~ 35 ps, as shown in Fig. 7(b). Fig. 7 implies that in order to achieve sub-30-ps timing jitter for detectors biased well within the saturation regime higher I_{SW} is required. The revised detectors were based on wider ~ 80-nm-wide nanowires. The results are shown in Fig. 8. The revised 2-SNAPs enabled a high signal-to-noise ratio (~ 8 - 9, as defined in Ref. [2]), resulting in a timing jitter of 24 ps when biased well within the avalanche regime (I_B ~ 22 µA). Furthermore, this detector showed saturated DE over a bias current range of 3.5 µA, the largest range reported to date. As a result we could bias the detector at > 3 µA below I_{SW}, which reduced the dark count rate by more than one order of
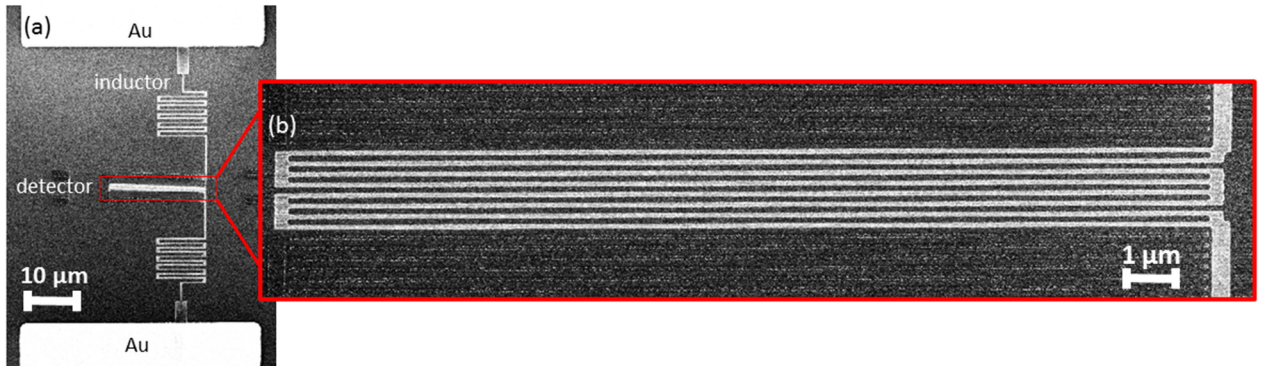

Fig. 6. SEM of waveguide-detector. (a) The detector is shown with the series inductor consisting of 300-nm-wide nanowires. (b) Magnified SEM of detector region encircled with red lines in (a). The detector consists of four 2-SNAPs in series with each 2-SNAP comprising two ~ 60- to 80-nm-wide nanowires in parallel.
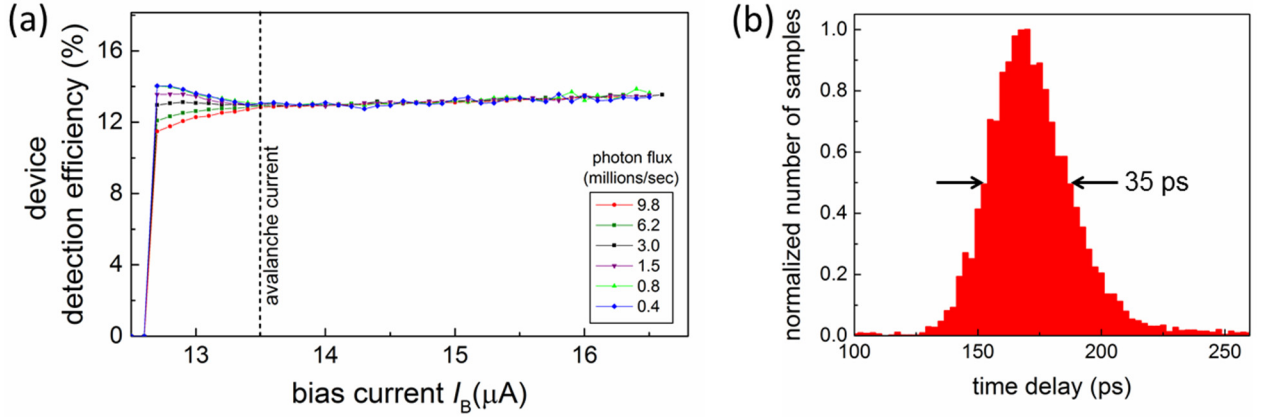
Fig. 7. (a) Back-illuminated device detection efficiency vs bias current for a series-2-SNAP based on ~ 60-nm-wide nanowires. The incident photon flux was varied between 0.4 million photons/second (blue) and 9.8 million photons/second (red). The trigger level was set to 310 mV. (b) Instrument response function (IRF) of the same detector as in (a) biased at 15.9 μA. The IRF was measured using the setup described in Ref. [6].

magnitude, while maintaining maximum internal efficiency. The optical absorption of this detector was calculated as ~ 18.4 % (see appendix).

A single-shot pulse trace of this detector, biased at 22 μA, is shown in Fig. 9. The room-temperature amplifiers had a bandwidth of 20 - 3000 MHz. When biased in this regime, the detector reached a photon count rate of 17 million counts per second (Mcps) at maximum efficiency.

The modified fabrication process resulted in higher detector yield. Figure 10 shows the switching current histogram of two samples for which SEMs of exemplary detectors were shown in Fig. 3. Fig. 10(a) shows that the switching current distribution of the sample without optimized etch process (Fig. 3(a)) is fairly broad for detectors with the same design. If we define the detector yield as the ratio of the detectors for which $I_{SW} > I_{AV}$, we obtain a yield of 30-50% for samples fabricated with the old process. In contrast, samples fabricated with the new process

(Fig. 3(b)) showed a significantly improved detector yield of ~ 70 %, as shown for an exemplary sample in Fig. 10(b).

V. SUMMARY

We optimized a fabrication process that allowed us to increase the detector yield to ~ 70 %. Based on the optimized process we fabricated detectors that, operated at 2.4 K and with room-temperature 3-GHz-bandwidth amplifiers, exhibit 24 ps timing jitter in single-photon regime, saturated detection efficiency and ~ 17-Mcps count rate simultaneously. The detectors were saturated over a bias current range up to 3.5 μA allowing for operation in a low-bias low-dark-count-rate regime while operating at maximum detection efficiency. Such detectors could be attractive for use in applications where low-jitter single-photon detectors are required in environments with high dark count rates, such as free-space coupled detectors. The high yield could additionally be attractive for implementation of SNSPD arrays [30].
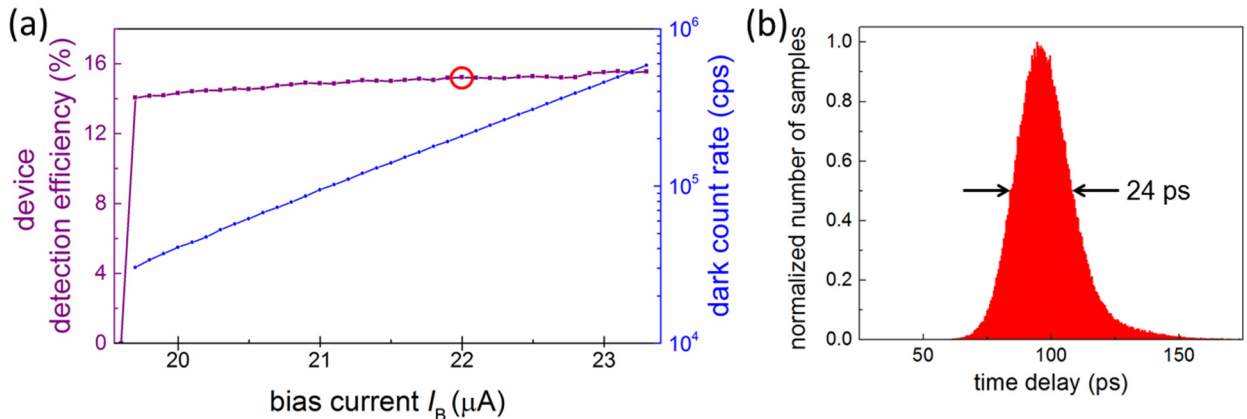

Fig. 8. (a) Back-illuminated device detection efficiency vs bias current for a series-2-SNAP based on ~ 80-nm-wide nanowires (see Fig. 6). The incident photon flux was 2.3 million photons/sec. The trigger level was set to 380 mV to show only the saturated avalanche regime ($I_B > 19.5$ μA, see Ref. [24]). The red circle denotes the operation point at which the timing jitter measurements were performed. (b) IRF of the same detector as in (a) biased at 22 μA. The IRF was measured using the setup described in Ref. [6].
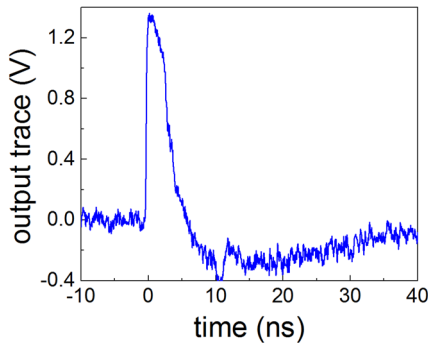
Fig. 9. Single-shot pulse trace of an exemplary 2-SNAP based on 80-nm-wide nanowires. The detector was biased at $I_B = 22$ μA.

850 μC/cm^2) and developed in TMAH at 27 °C for 3 minutes. The HSQ pattern was transferred into NbN via a ~ 2- to 2.5-minute CF_4 RIE at 50W.

Optical absorption calculation: According to an analytical model of the device based on the transfer matrix method, a 4-nm-thick layer of NbN nanowires with a fill factor of 30 % (60-nm-wide nanowires with a 200-nm pitch) has an absorptance of 14.5 % at a wavelength of 1550 nm. A similar layer of NbN with 80-nm-wide nanowires and a 40 % fill factor has an absorptance of 18.4 %. The calculation assumes illumination through the silicon substrate with a plane wave and that both sides of the silicon (n = 3.47772) have 300 nm of SiN_x (n = 2.217). The NbN layer is modeled using an effective index of refraction, which depends on the indexes of refraction of NbN (n = 5.23-5.82 i) and air and the fill factor. The coherence length of the incident light is assumed to be less than the thickness of the silicon substrate.

APPENDIX

Substrate cleaning: Substrates were prepared by dicing from a 100mm diameter wafer, cleaned with solvents, and lastly exposed to an oxygen plasma at 100W for 3min.

Definition of T_C: For both new NbN films and older films in Ref. [18] we defined T_C as the temperature at which the film resistance has fallen to 50 % of its value at 20 K.

Liftoff process: We exposed a 700-nm-thick PMGI-SF9 layer covered with ~ 1.5 μm-thick S1813 with UV for 13 seconds at 2300 μW/cm^2 and developing the bilayer for 24 seconds in CD-26. 10 nm Ti and 15 nm Au were evaporated and the liftoff was performed in Acetone under sonication for 2 minutes followed by a 1-minute-long dip in CD-26 and a 1-minute-long DI dip.

Electron-beam lithography: A ~ 60-nm-thick HSQ layer (4%) was spun immediately after the adhesion promotion step. The HSQ was exposed in a Raith 250 tool at 30 keV (dose 700-
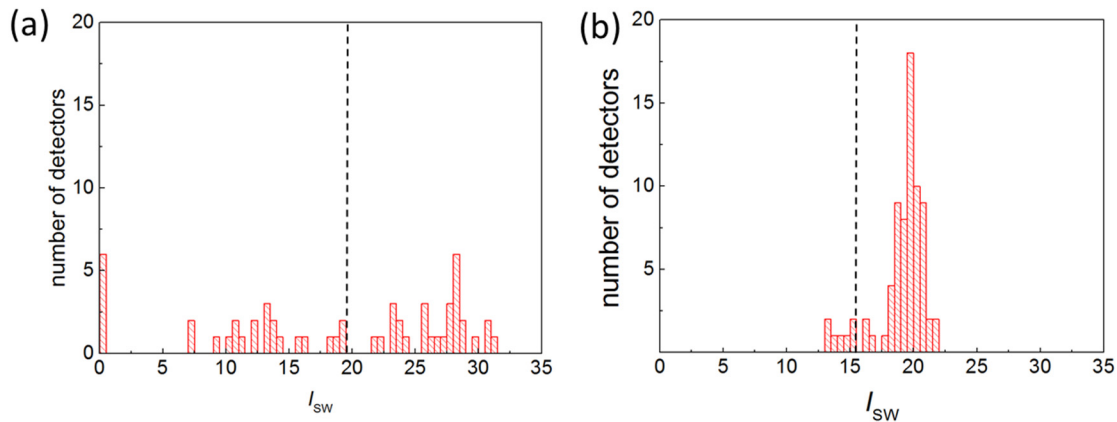
Fig. 10. (a) Switching current histogram of detectors on a sample prepared with the old RIE process. The dashed line represents the avalanche current. (b) Switching current histogram of detectors on a sample prepared with optimized etch process. The dashed line represents the avalanche current.

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