Fabrication of Extremely Smooth Nanostructures Using Anisotropic Etching

by

Andrea Elke Franke

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Abstract

Anisotropic etching has the potential to produce structures in silicon with extremely smooth surfaces, possibly even atomically smooth. Anisotropic etchants etch in <111> directions orders of magnitude more slowly than in other directions. Hence, etching virtually ceases when the etch front encounters a {111} plane. Any surface protrusion that exposes a plane other than a {111} is quickly etched. Structures defined by extremely smooth {111} planes result. An application of this etching technique is the fabrication of 200 nm period arrays of inverted pyramids in (100) silicon substrates. These substrates promise to reduce defect density in lattice mismatched epilayers. Also, anisotropic etching can be used to improve efficiency of grazing incidence, blazed, X-ray diffraction gratings.

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Chapter 1
Anisotropic Etching

Anisotropic etching has the potential to produce structures in silicon with extremely smooth surfaces, possibly even atomically smooth. Applications of anisotropically etched structures exist in crystal growth, optics, biology, micromachined sensors, and possibly other fields. In this chapter the behavior of anisotropic etching, basic crystallography, and alignment issues will be discussed.

High quality silicon crystal is easily available due to its importance in integrated circuits. Anisotropic etching takes advantage of this high quality crystallinity by etching in <111> crystal directions orders of magnitude more slowly than others. This means that any step or protrusion above a {111} crystal plane will quickly be etched, leaving behind a smooth surface bounded by a {111} plane.

This difference in etch rates can be explained in part by studying the silicon crystal structure. Silicon is of the diamond cubic crystal structure (Figure 1.1). Silicon atoms are at each corner of the cube (black), at the center of each cube face (white), and four silicon atoms (gray) are 1/4 of a lattice constant, 'a', in each direction from a corner atom. Each silicon atom has four nearest neighbors to which it is most strongly bonded. In the front upper right-hand corner of Figure 1.1, the four bonds are indicated with thick black lines. The diamond cubic structure can be thought of as two interpenetrating face centered cubic (fcc) sublattices. The first sublattice is the black and white atoms and the second is the gray atoms in Figure 1.1.

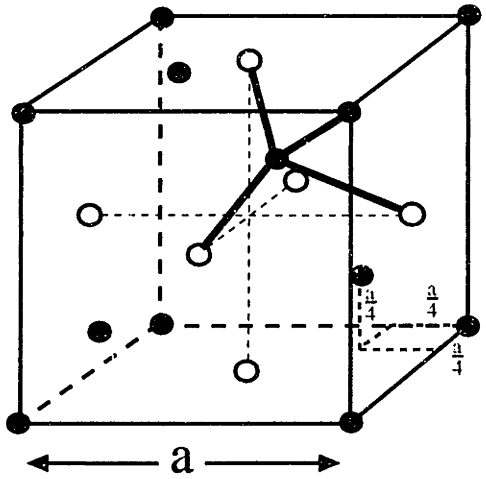

Figure 1.1 The diamond cubic unit cell with lattice constant, 'a'.

As with all crystals, silicon consists of the unit cell repeated through three dimensional space. This results in considerable symmetry. For example, consider rotating the silicon unit cell, or a crystal containing many unit cells, 180° about a unit cell edge. There will be no noticeable difference. Hence, the origin can be the corner of any unit cell, and axes can be chosen along any three edges of a unit cell which intersect the origin.

Crystal planes are defined with three coordinates, called Miller indices. Planes are described by first locating the intercepts of the plane along the **x**, **y**, and **z** axes in a unit cell. The Miller indices are obtained by taking the reciprocals of the intercepts, and if necessary multiplying each by the same integer to give integer indices (Figure 1.2). Using this method, planes which do not have an intercept with an axis will have a zero for the Miller index corresponding to that axis. Consider the (1 0 2) plane. It intercepts the **x**, **y**, and **z** axes at 1, infinity, and 1/2, respectively. Taking the reciprocals gives (1 0 2).

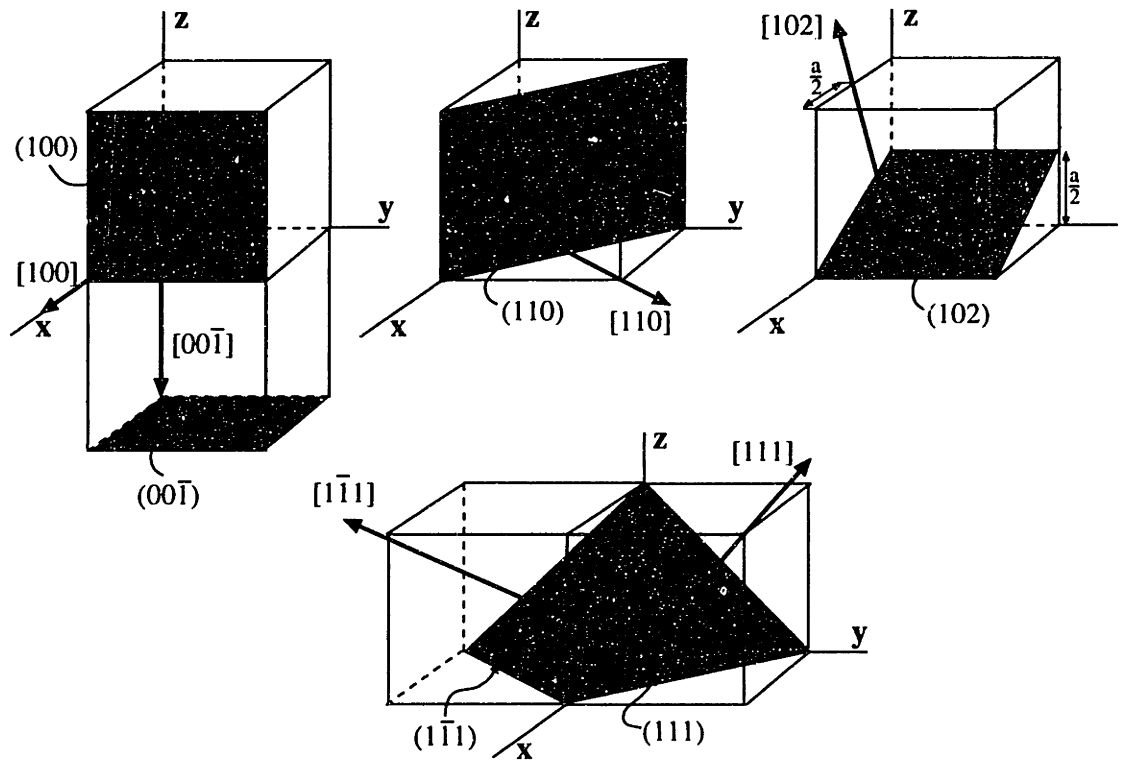

Figure 1.2 Examples of crystal planes and directions.

Similarly, to determine the indices for a direction, projections of the direction in a unit cell on the axes are located, and if necessary are multiplied by an integer to give integer indices. The projections of the [1 0 2] direction in

the unit cell on the **x**, **y**, and **z** axes are 1/2, 0, and 1, respectively. Multiplying by two gives [1 0 2].

Specific planes are labeled (h k l), and families of planes are {h k l}. Specific directions are labeled [h k l], and families of directions are <h k l>. For example, the planes (1 0 0) and (0 0 $\bar{1}$) are in the {1 0 0} family which means that they are equivalent planes whose labelling depends only on the choice of origin and axes. A bar over an index indicates a plane which intercepts a negative portion of an axis, or a direction whose projection is on a negative portion of an axis. In cubic crystals such as silicon the direction [a b c] is always perpendicular to the plane with the same indices, (a b c).

The {111} planes in silicon have the highest atomic lattice packing density, or number of atoms per area. The spacing between adjacent, parallel {111} planes is the greatest, and there is the least number of bonds between adjacent, parallel {111} planes. The bond densities are 1:0.71:0.58 between adjacent, parallel planes for the {100}:{110}:{111}. The lower the density of bonds between adjacent, parallel planes, the more bonds there are between atoms in the plane, and so the more difficult to remove atoms. However, etch rates as selective as 300:600:1 for the <100>:<110>:<111> directions have been found[4]. The differences in etch rates can not be explained solely by the differences in bond densities. It has been proposed that the high selectivity is a result of selective passivation of the {111} planes. The {111} planes of silicon are known to oxidize more quickly than other planes. This oxide could be protecting the {111} planes during etching. The fact that the etch rates of {111} silicon planes and silicon dioxide have been found to be nearly equal supports this theory.

Anisotropic etching proceeds as depicted in Figure 1.3. In this example a (100) wafer is used. Etching proceeds quickly until the {111} planes are encountered (Figure 1.3a). The etch rate in the <111> directions is small yet does allow for undercutting of the mask (Figure 1.3b). If the etching is allowed to proceed for a long enough period of time, parts of the mask can be completely undercut (Figure 1.3c).

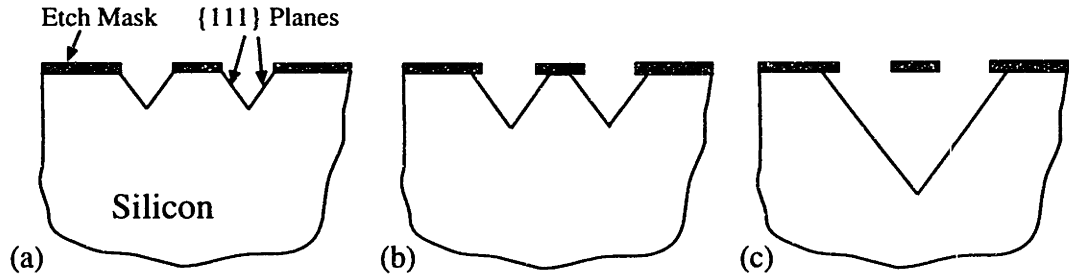

Figure 1.3 As anisotropic etching proceeds, the etch mask is slowing undercut. This figure was adapted from a figure by Peterson[5].

For most anisotropic etching applications careful alignment of the etch mask to the crystallographic planes is required. As discussed by Kendall[4], misalignment results in altered etch rates, and surface steps on etch facets (Figure 1.4). As the misalignment angle, Θ, increases, the density of surface steps on the etched facets increases. Edge roughness of the etch mask produces similar surface steps on etch facets and is discussed further in Chapter 5.

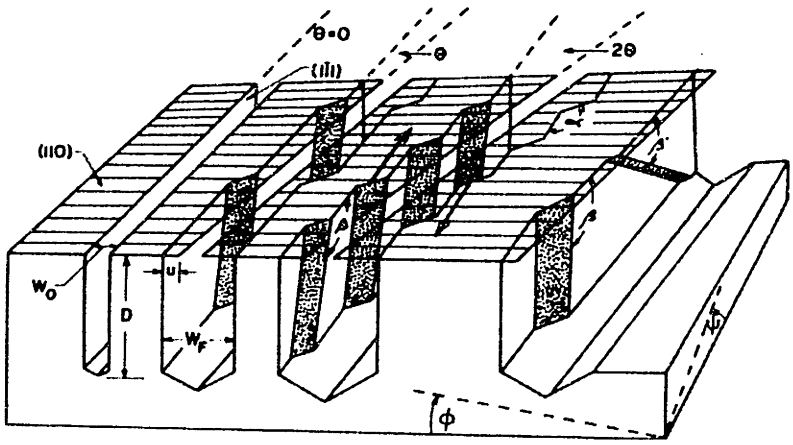

Figure 1.4 Misalignment of the etch mask results in surface steps on the etched facets. This figure is from Kendall[4].

There are several solutions which can be used as anisotropic etchants[6-10]. Potassium hydroxide, KOH, was chosen for the following work because the etch rate selectivity is the highest. This results in extremely smooth facets. Two applications of anisotropic etching were investigated: arrays of inverted pyramids and grazing incidence, blazed, X-ray diffraction gratings. The arrays of inverted pyramids promise to improve the crystal quality of epitaxial layers of other semiconductors. The X-ray diffraction gratings are shown to provide enhanced efficiency by a factor of two in comparison to currently available gratings, and are more reliably fabricated.

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Chapter 2

Epitaxy of Lattice Mismatched Semiconductors on Silicon

2.0 Introduction

There is great interest in SiGe alloys[1-5], GaAs[6-9], and InP[10-12] because of their higher mobilities and/or higher bandgaps compared to silicon. These properties indicate the possibility of higher speed electronic devices and smaller wavelength optical devices. Epitaxially growing these materials on silicon would provide larger wafer areas and would be less expensive than using bulk grown wafers. High density silicon circuitry could be combined with high speed and optical devices on the same substrate, thereby eliminating interchip capacitances and increasing speed.

However, the lattice mismatch of $Si_{1-x}Ge_x$ on silicon varies from 0 to 4.2% as x varies from 0 to 1. GaAs and InP on silicon have lattice mismatches of 4.1% and 8.1% respectively. This leads to dislocations, stacking faults, twin boundaries, and surface roughness in the epitaxial films. Thermal expansion coefficients for Si, Ge, GaAs, and InP are 2.6×10^{-6} K^{-1}, 5.8×10^{-6} K^{-1}, 6.86×10^{-6} K^{-1}, and 4.75×10^{-6} K^{-1} respectively[13]. Thermal cycling introduces defects since the thermal expansion coefficients of the epitaxial films are different than that of silicon. Finally, epitaxy of polar semiconductors, GaAs and InP, on Si, a nonpolar semiconductor, leads to anti-phase domains.

2.1 Epitaxy on (100) Silicon: Dislocations and Antiphase Domains

In order to combine high speed electronic devices or optical devices with conventional silicon circuitry on the same substrate, (100) silicon wafers must be used for epitaxy. Epilayers on (100) silicon tend to have high dislocation densities which negatively affect the epitaxial film quality in three ways. First, they form nonradiative recombination centers. Second, impurities diffuse more easily along dislocations than in perfect crystal, and this can allow silicon to diffuse into the epilayer and cause unintentional doping[8]. Third, the dislocations greatly decrease carrier mobility[3]. The dislocations are due to lattice mismatch, and the strain that the mismatch causes in the epilayer. Strain is accommodated by elastic deformation, if the epilayer is

below a critical thickness or if the growth area is small enough. Requiring that the film is thinner than the critical thickness or that the growth areas are small is too limiting for most applications. However, dislocations that do not thread to the surface of the epilayer do not have deleterious effects.

There are two different kinds of dislocations. Type I dislocations have a Burgers vector of 1/2<011>, in the (100) plane, and a dislocation line in the (100) plane. Type II dislocations have a Burgers vector of 1/2<110>, 45° to the (100) plane, and a dislocation line 60° to the (100) plane. Dislocations tend to slip along planes that contain both their Burgers vector and their dislocation line, so only type II dislocations thread to the epilayer surface. Type I dislocations tend to be generated at atomic scale steps on the silicon surface. Misorienting the crystallographic planes by a few degrees, so that the wafer surface is not exactly the (100) plane, results in more steps. This leads to more type I dislocations, and dislocation densities at the epitaxial surface that are 2-3 orders of magnitude less than epilayers grown on exactly oriented (100) wafers[8]. However, misorienting the silicon wafer degrades devices.

Another approach to reduce defect density is to anneal the epilayer at high temperature for a long period of time or to use rapid thermal annealing (RTA). Type I dislocations are energetically favorable to type II, and so annealing leads to the reduction of type II dislocations. Long anneal times tend to increase interdiffusion and unintentional doping. RTA does not have noticeable diffusion problems[8], but annealing at high temperatures is damaging to silicon devices that may have previously been fabricated on other parts of the wafer. Annealing relaxes strain which can not be tolerated when attempting to grow strained layers for mobility enhancement and bandgap engineering. Also, large temperature gradients can introduce more defects due to thermal expansion mismatches[14].

Another problem with epitaxy on (100) silicon is antiphase boundaries (APB) which reduce mobility[6]. APBs are charged structural defects made of cation-cation and anion-anion bonds which act as acceptors and donors. There tends to be an equal number of these bonds, and so the epilayer acts like a highly compensated semiconductor. Silicon is a nonpolar semiconductor because both fcc sub-lattices of the diamond structure are occupied by silicon atoms. GaAs and InP are polar because each fcc sublattice is exclusively occupied by one kind of atom. Antiphase boundaries occur between domains where atoms switch sublattices. Growth of polar semiconductors on (100)

silicon substrates consists of alternating monolayers of cation and anion atoms. Nonuniform surface coverage of the first epitaxial monolayer and monoatomic steps on the silicon surface lead to antiphase domains in the polar epilayer. Beginning growth by exposing the substrate to only one species can provide uniform surface coverage of the first monolayer. Misorienting the silicon substrate and high temperature annealing tend to increase the formation of double atomic steps on the silicon surface because these are energetically favorable to single atomic steps[8]. Double atomic steps do not lead to APBs, but neither substrate misorientation nor high temperature annealing are desirable for integrated circuit fabrication.

2.2 Epitaxy on (111) Silicon: Stacking Faults and Twin Boundaries

Although epitaxy on (111) silicon is not compatible with VLSI technology, it provides some interesting insights. The easy slip and twinning planes are {111} planes, because the spacing between adjacent, parallel {111} planes is greatest and the Peierls barrier to dislocation motion is the lowest. With (100) wafers there are no {111} planes parallel to the epilayer interface, and there are four {111} planes that intersect the epilayer surface at 54.7°. (111) wafers have one {111} plane parallel to the epilayer interface, and three planes that intersect the epilayer surface at 70.5°.

The dislocation density in InP epilayers on (100) silicon is about 10^8 cm^{-2}, and is an order of magnitude less when grown on (111) silicon[12]. High resolution TEM of InP epilayers on (111) silicon performed by Krost et al.[12] shows that the lattice mismatch is accommodated by twinning and dislocations near the interface. Twins appear to nucleate close to steps on the (111) silicon surface. At the steps, growth of a twinned or perfect (111) monolayer is equally likely. Above the twinned region the defect density is reduced, and the (111) planes inclined to the surface have the same orientation as in the silicon. Twins and stacking faults were still observed due to the three other {111} planes. However, the density was smaller than that in InP grown on (100) silicon. Stacking faults at the interface accommodated for the lattice mismatch of GaAs grown on (111) silicon[14]. Another advantage of epitaxy on (111) silicon is that APBs do not form as long as nucleation is uniform and islands of growth do not form, because the growth surface has both cations and anions exposed.

2.3 Epitaxy on Sawtooth Patterned Silicon

Several groups have tried to improve the crystal quality of epilayers by growing on sawtooth patterned silicon[16-25]. Unfortunately, there is a lot of variation between studies in wafer cleaning methods, growth parameters, patterning of the sawtooth structure, and techniques used to analyze the resulting epilayers (Table 2.1). This makes it difficult to compare nucleation, growth, and defect generation mechanisms and to conclude which is a repeatable process with optimal crystallinity. However, very promising improvements in epilayer defect density have been made in epilayers grown on sawtooth patterned silicon.

	Hashimoto et al., Refs. 16-18	**Sprung et al., Ref. 19**	**Karam et al., Refs. 20-22**	**Krost et al., Refs. 14, 23-25**
Off cut from (100)	3° towards <0$\bar{1}$1>	exactly (100)	2° towards [110]	exactly (100)
Wafer Clean	HF solution, 1 min.	none mentioned	trichoroethane, acetone, methanol, NH_4OH:H_2O_2:H_2O, HF	propanol, DI, H_2SO_4: H_2O:H_2O_2, HF
Wafer Anneal	930°C, 5 min.	850°C, 5 min	900°C, 5 min, (MBE); 1000° C, (MOCVD)	none
Buffer Growth Temp, Thickness	450°C, 20 nm	380°C, 50 nm	350°C, 40 nm, (MBE); 400°C, 5-20 nm, (MOCVD)	425°C (GaAs); 400°C (InP), 50nm
Layer Growth	750°C, MOCVD, 100 Torr	580°C, MBE	640°C, MBE; 600-700° C, MOCVD	700°C, 500 mbar (GaAs); 640°C, 20 mbar (InP), MOCVD
Groove Width, Width btw. Grooves	2 μm, 3 μm and larger	~350 nm, ~50 nm	~170 nm, 30 nm	320 nm, 80 nm (GaAs); 200 nm, 200 nm (InP)

Table 2.1 Comparison of epitaxy parameters on sawtooth patterned silicon

Hashimoto et. al.[16-18] studied the epitaxy of $Al_xGa_{1-x}As$ by MOCVD on silicon patterned with V grooves 2 μm wide etched at 3, 5, 8, and 350 μm intervals. SEM and scanning Auger electron spectroscopic (AES) measurements revealed that no epitaxy occurred on the {111} facets. It was proposed that the migration velocities of Ga and/or Al species were too high for nucleation to occur on {111} planes. Microscopic photoluminescence and Raman scattering measurements indicated that silicon originating from the

{111} facets contaminated the epilayers and that the epilayers were more stressed near the edge between the (100) and {111} planes, which implied a reduction of dislocation density near the edge. No more direct measurements of dislocation or other defect densities were made. The other research groups did not replicate this selective growth phenomenon[18-25], possibly because the growth temperatures in the other studies were lower which decreased the surface mobilities of the reactants.

Sprung et al.[19] grew GaAs by MBE on exactly oriented (100) silicon patterned with sawtooth grooves of 400 nm period. Unlike the Chong and Fonstad[9] study, reflected high-energy electron diffraction (RHEED) did not exhibit (2X2) reconstruction which indicates that surface oxide was desorbed after the sample was cleaned with a high temperature anneal. Yet both studies found (2X2) reconstruction after exposure to As. During the GaAs buffer growth the RHEED pattern was spotty, indicating that three-dimensional GaAs islands were being grown. The epilayer grown on the buffer exhibited streaky RHEED patterns indicating (2X4) surface reconstruction which is characteristic of single domain GaAs. However, epilayers of GaAs grown on unpatterned (100) silicon had blurred RHEED patterns thought to be due to APBs and large defect densities. Nomarski phase contrast micrographs confirmed the absence of APBs in the epilayers grown on the patterned silicon and the presence of APBs in epilayers grown on the unpatterned silicon. The crystal structure was further examined by x-ray diffraction. The full width at half maximum (FWHM) of the rocking curve was 220" for the epilayer grown on patterned silicon, and 390" for the epilayer on the exactly oriented, unpatterned silicon. The 220" measurement is higher than measurements of epilayers homoepitaxially grown, yet is comparable to measurements of epilayers grown on off-cut (100) silicon substrates. An estimate of dislocation density can be made using the FWHM measurement[26]: $D \simeq \beta^2/9b^2$, where D is the dislocation density, β is the FWHM, and b is the Burgers vector of the dislocations. Using this estimate, $D \simeq 1 \times 10^7$ cm^{-2} for the epilayer grown on the sawtooth patterned silicon, and $D \simeq 6 \times 10^7$ cm^{-2} for the epilayer grown on unpatterned silicon. These are promising results for integrating high speed electrical or optical GaAs devices with conventional silicon VLSI on the same substrate. However, little can be concluded about the nucleation and defect generation mechanisms from this study.

Karam et al.[20-22] grew GaAs by MBE and MOCVD on (100) silicon tilted 2° toward [110] and with 200 nm period sawtooth patterning. In earlier studies[20-21], RHEED patterns during MBE growth indicated that the buffer layer was amorphous, and that heating to 600°C or above caused (2X4) surface reconstruction, which indicated crystallization of the buffer layer. For MOCVD growth, RTA or thermal cycle growth was used to eliminate the high density of twins and stacking faults that were observed in initial epilayers. Shallow (~0.8 μm above the GaAs/Si interface) and deep (~0.1 μm above the GaAs/Si interface) KOH etches of the MOCVD epilayers resulted in 10^4 cm^{-2} and 10^5 cm^{-2} etch pit densities respectively. These etch pit densities give a lower bound on the dislocation density. Plan view TEM produced an upper bound on the dislocation density of 10^5 cm^{-2}. A thin interfacial amorphous SiO_x layer between the silicon and the epilayer was believed to be the cause of the low dislocation densities. It was proposed that the initial GaAs growth senses the symmetry but not the precise positions of the silicon beneath the SiO_x, and so the epilayer crystallizes without the mismatch induced defects. Another possibility mentioned was that growth was seeded through pinholes in the SiO_x. More detailed TEM work was performed in Ref. 22, and no SiO_x layer was seen in the micrographs. Most dislocations were confined to the first micron of epilayer and were observed to loop back to the GaAs/Si interface or to terminate without threading out of the V-grooves. No APBs were observed. Twinning was believed to be more prevalent when initial growth was on {111}. The extremely low dislocation densities measured in the earlier studies make this procedure for substrate preparation and epilayer growth very promising. However, high resolution TEM might be useful to more fully understand the SiO_x film and how it affects epitaxy.

The earlier studies of Krost et al.[23, 24] investigated MOCVD epitaxy of InP on exactly oriented (100) silicon patterned with grooves 6 μm and 4.5 μm wide separated by (100) facets 3.5 μm and 0.6 μm wide, respectively. The width of the grooves and the spacing between grooves were too large for planarization of the epilayer. However, some interesting insights were obtained. Nucleation took place on both (100) and {111} facets. Growth on the structures with smaller (100) facets between the grooves resulted in no APB formation. APBs are caused by monoatomic steps on the (100). Reducing the width of the (100) facets reduced the probability of monoatomic steps and APBs. In a later study[14], epilayers of GaAs and InP were grown on substrates

with 320 nm and 200 nm grooves, and 80 nm and 200 nm wide (100) facets, respectively. Planarization did occur, and no APBs were formed. TEM images revealed that there were voids above the (100) facets, and it was concluded that growth initiated on the {111} facets of the grooves. Recent research[25] investigated in more detail the growth process of InP on sawtooth patterned (100) silicon. SEM micrographs were taken during each stage of growth. The nucleation layer homogeneously covered both the {111} and the (100) facets. After heating up the same sample to 640° C, InP migrated along the surface from the (100) facets to the {111} facets. By examining the planar area next to the grooves, it could be seen that InP up to 0.5 μm from the grooves had migrated into the grooves. This indicates that the epilayers in previous studies[23, 24] did not planarize in part because the distance between the grooves was too large for the nucleated material to migrate to the grooves. Growth in the grooves continued at 640° C and coalesced above the (100) facets leaving voids. The FWHM of double crystal x-ray diffraction rocking curves indicated that the defect density was almost as low as that of epilayers grown on off-cut (111) silicon. An etch pit density of $7x10^4$ cm^{-2} was found for the epilayer on the patterned (100) silicon. However unlike growth on (111) silicon, a large number of twins and stacking faults aligned to the {111} groove facets did propagate to the epilayer.

2.4 Epitaxy on Inverted Pyramid Patterned Silicon

Twins and stacking faults were observed in GaAs[22] and InP[25] epilayers grown on sawtooth patterned (100) silicon. Growth was found to initiate on the {111} facets, and twins have been found to nucleate on surface steps of {111}. In papers that have shown SEMs of the sawtooth structure before growth[19, 21] the {111} have large surface steps. This is to be expected because it is not possible to align masks perfectly with the silicon crystal planes for the anisotropic etch of the sawtooth structure. Any misalignment will result in surface steps (Chapter 1). Also, the edges of the etch mask are quite rough, and this transfers into steps on the etched {111} groove facets (Chapter 5).

Anisotropic etching of inverted pyramids on (100) silicon is not sensitive to mask alignment. Regardless of where a circular hole in the mask is placed, a square inverted pyramid defined by {111} will be etched. Roughness of the edges of the mask is also not critical. As long as the hole in

the mask is symmetric, a square indentation will form. Epitaxy on arrays of inverted pyramids could take advantage of the growth mechanisms on sawtooth patterned silicon which result in low dislocation densities and no APBs, while reducing twins and stacking faults by eliminating surface steps on the inverted pyramid {111} facets. High temperature anneals would not be necessary to reduce the density of the twins and stacking faults, and epitaxy would be more compatible with standard silicon circuitry.

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Chapter 3
Design of Inverted Pyramid Process

3.0 Introduction

The inverted pyramid process steps are shown in Figure 3.1, and the process conditions for each step are described in detail in Appendix A. The process began with a (100) silicon wafer coated with silicon nitride, anti-reflection coating (ARC), and Shipley 1813 resist. The resist was patterned using interferometric lithography. Titanium was shadow evaporated on the resist posts to act as a hard mask for the reactive ion etch (RIE) of the ARC. Chromium lift-off reversed the tone of the pattern, and the holes were transferred into the silicon nitride layer using RIE. The patterned nitride layer was then an etch mask for the anisotropic etch of the silicon that produced inverted pyramids.

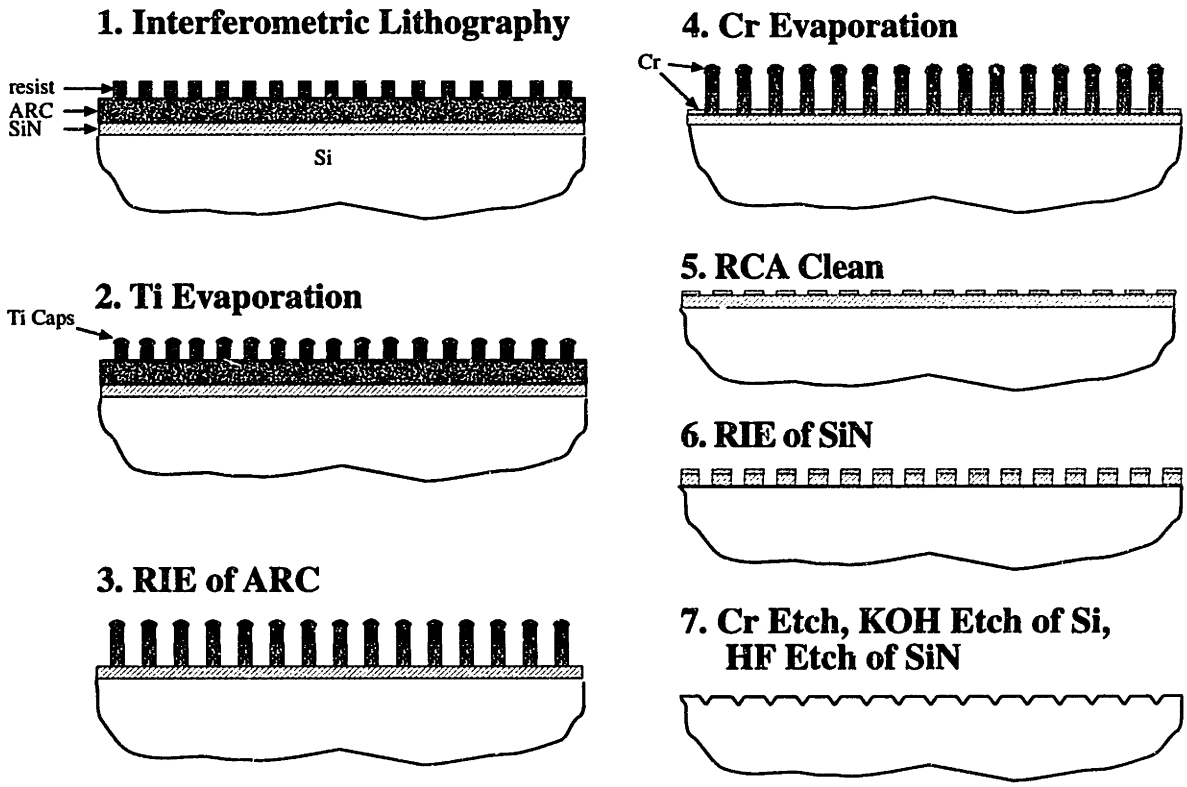


Figure 3.1 Schematic of inverted pyramid process steps.

3.1 Interferometric Lithography

Positive resist was exposed using interferometric lithography at 351.1 nm wavelength and for a 200 nm period pattern[1]. The wafer was exposed twice, with the wafer rotated 90° for the second exposure. After development, the posts of resist remained where the light destructively interfered in both exposures. The exposure dose was chosen to be high enough that shoulders between the posts were small compared to the posts and low enough that the posts were not thinner at the base than at the top (Figure 3.2). The dose was chosen for each exposure session by examining developed resist profiles from wafers exposed with several doses.

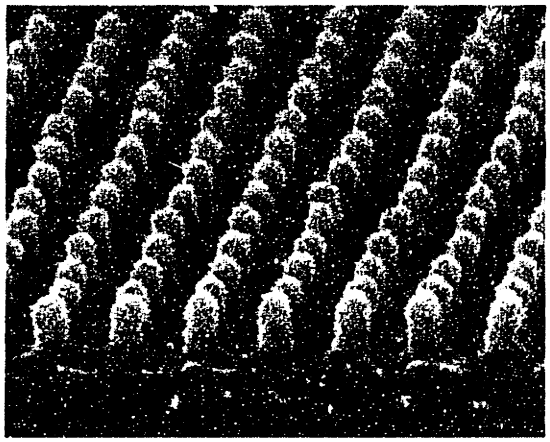


Figure 3.2 SEM micrograph of resist posts with appropriate interferometric dose.

The wafer must be aligned such that the lines of constructive interference run perpendicular and parallel to the wafer flat which is a {110} plane (Figure 3.3). The larger the misalignment angle with the crystallographic planes, the larger the spacing between inverted pyramids. As discussed in Chapter 2, the spacing between the V grooves in sawtooth structures must be small in order to reduce defects and have the epilayer planarize. Similarly, the spacing between inverted pyramids should be minimized.

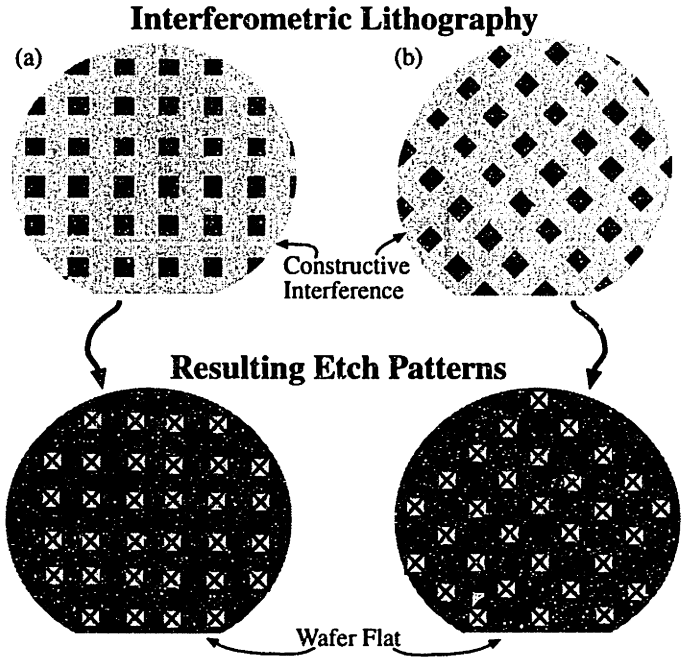


Figure 3.3 The correct interferometric lithography pattern is depicted in (a). Not aligning the lines of constructive interference parallel and perpendicular to the wafer flat results in larger spacing between inverted pyramids after KOH etching which is not desirable (b).

3.2 Titanium Evaporation

One of the main goals of the remaining steps was to produce small, round holes in the silicon nitride layer. If the holes in the silicon nitride were oval, more silicon area was exposed to the KOH along the larger axis of the oval, and rectangular trough-like indentations were etched (Figure 3.4). Hence, the titanium caps evaporated on the resist posts had to be as circular as possible. Originally, the caps were shadow evaporated from two directions, and this produced oval patterns. Four shadow evaporations each 90° apart resulted in circular patterns (Figure 3.5). A program written by another student[2] calculated that aligning the wafer flat at 30° and 120° with the evaporation plate edge allowed adequate shadowing, so titanium was not evaporated between the posts or on the bases of the posts (Figure 3.6).

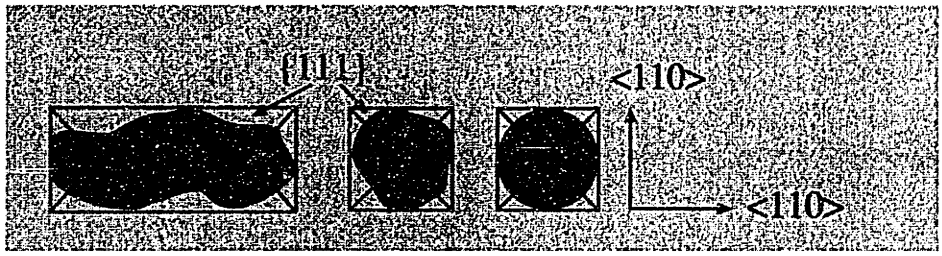
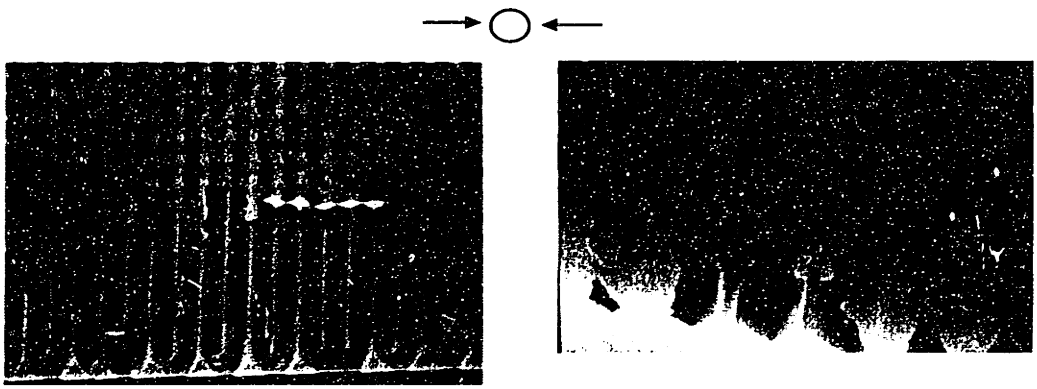


Figure 3.4 Top view of anisotropically etched indentations seen beneath the etch mask. An irregular oval hole in the silicon nitride etch mask resulted in a rectangular trough-like indentation. Irregular, yet not oval, and perfectly circular holes in the silicon nitride etch mask both resulted in inverted pyramids.

Two Shadow Evaporations:



Four Shadow Evaporations:

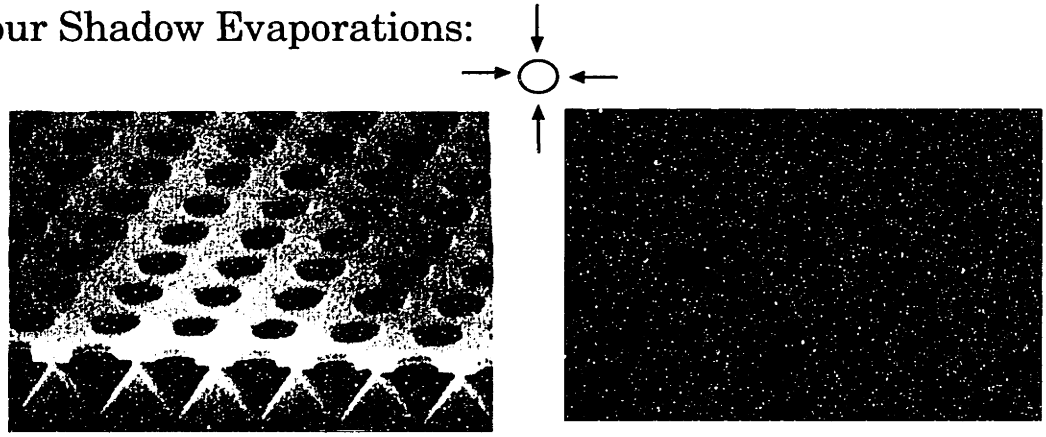


Figure 3.5 Four shadow evaporations resulted in more circular titanium caps, and hence more circular holes in the silicon nitride. In the above case, the nitride holes were so oval that during KOH etching the pyramids coalesced along the larger axis of the oval nitride holes.

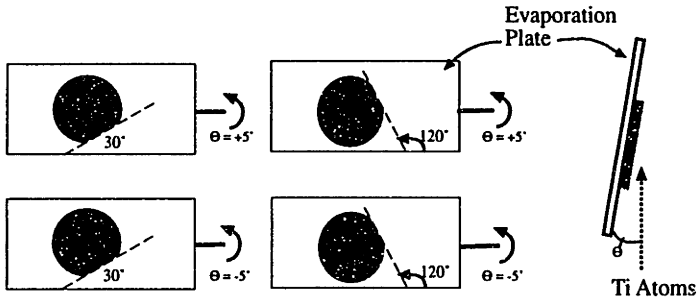


Figure 3.6 Configurations for shadow evaporations. Θ is the angle the plane of the wafer made with the titanium flux.

The evaporation plate tilt angle, Θ, was calculated by first realizing that in aligning the wafer to the evaporation plate above, the resist post A casts a shadow towards post B in Figure 3.7. The period of the interferometric lithography was 200 nm, so d ≅ 450 nm. The width of the holes in the silicon nitride were approximately the same as the width of the titanium caps. The smaller the holes in the silicon nitride were, the easier it was to control the anisotropic etching. However, the titanium caps had to be wide enough that the ARC posts did not fall together during RIE. The width of a titanium cap, w, was chosen to be ≅ 80 nm. The height, x, of the desired titanium cap was then approximated with an SEM micrograph of the resist profile after titanium evaporation and was on the order of 60 nm. This resulted in Θ = 7.6° or less. An angle of 5° was used.

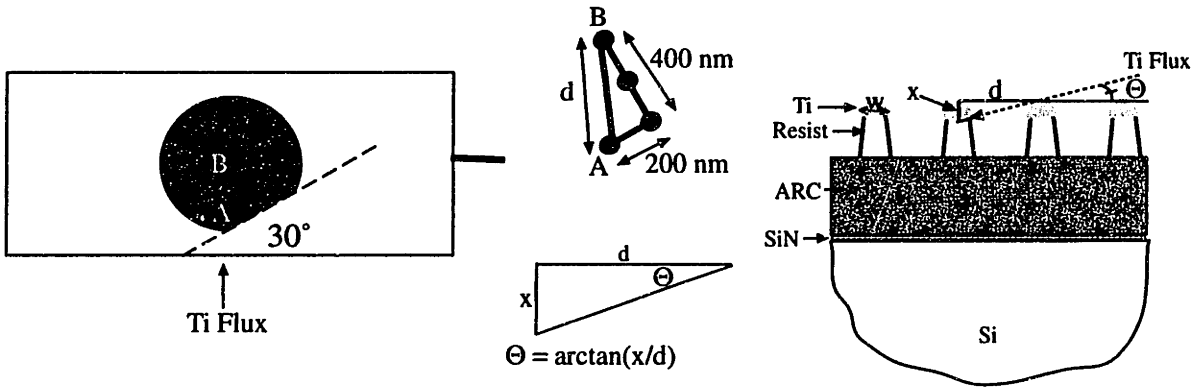


Figure 3.7 Determination of evaporation plate angle, Θ.

3.3 RIE of ARC

Oxygen RIE was used to transfer the pattern of the array of titanium circles into the ARC layer. The purpose of the ARC was to suppress standing waves in the resist due to reflection from the underlying silicon nitride and silicon layers in the interferometric lithography step. Without the ARC the standing wave would have created a vertical rippling in the resist profile or even prevented complete resist development. Initially, the ARC was spun to be 350 nm thick. This thickness gave a reflectivity of less than 1% at the resist/ARC interface (Figure 3.8). However, the process latitude of the RIE step was quite small with this thickness of ARC. If the ARC was not etched long enough, the chromium used for liftoff was evaporated onto ARC which dissolved away in the RCA step, and no pattern remained (Figure 3.9). If the ARC was over-etched the posts began to fall over because the RIE laterally etched the posts to the point where they could no longer support the titanium caps. As can be seen in Figure 3.10, after 6 minutes of RIE 33.4 nm of ARC remained. After 7 minutes of RIE the ARC cleared, yet an additional minute of RIE caused the posts to fall over. Because there is some variation in etch rate due to deposition of etched materials on the RIE chamber and other factors[3], the process latitude with 350 nm of ARC was too small. Decreasing the ARC thickness to 220 nm gave adequate standing wave suppression while greatly increasing the RIE process latitude (Figure 3.11). Using 220 nm of ARC the RIE etching was complete within 5 minutes. Although the posts became thinner with additional etching, they did not fall over, even after 9 minutes of etching. With this increased process latitude it was possible to over etch to ensure that the ARC had been etched through without the posts falling over.

Another way to check that the ARC had been etched through was to visually note the color of the wafer when the etch was thought to be complete based on the results of previous runs, and etch the wafer for an additional period, say 30 seconds. If the color did not change, the etch was complete. This method relies on interference from the ARC film being etched (Figure 3.12). As the thickness of the ARC changes, different wavelengths of light reflecting from the air/ARC and ARC/silicon nitride interfaces constructively interfere. Diffraction of light by the posts does not occur except possibly at grazing

angles because the period of the posts, 200 nm, is smaller than half the wavelength of visible light.

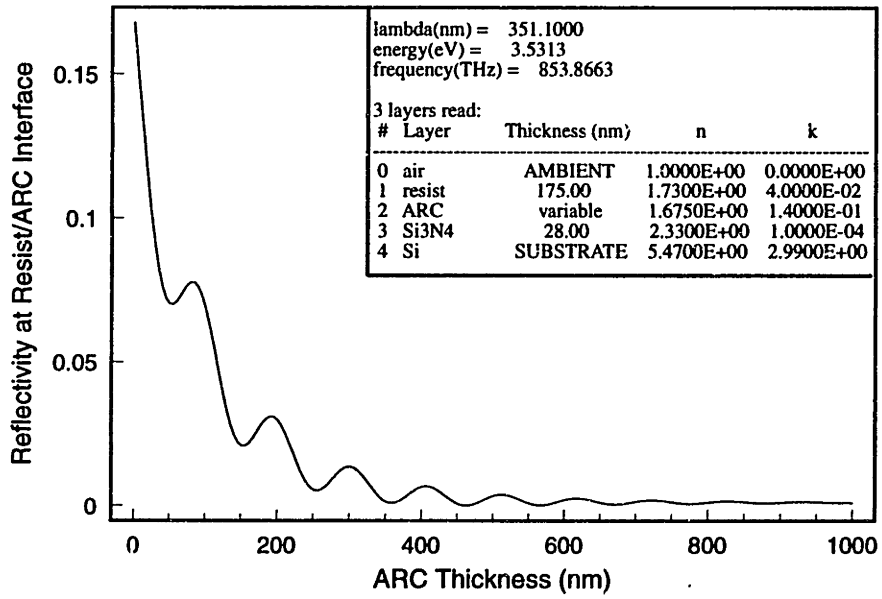


Figure 3.8 Calculated reflectivity at resist/ARC interface vs. ARC thickness.

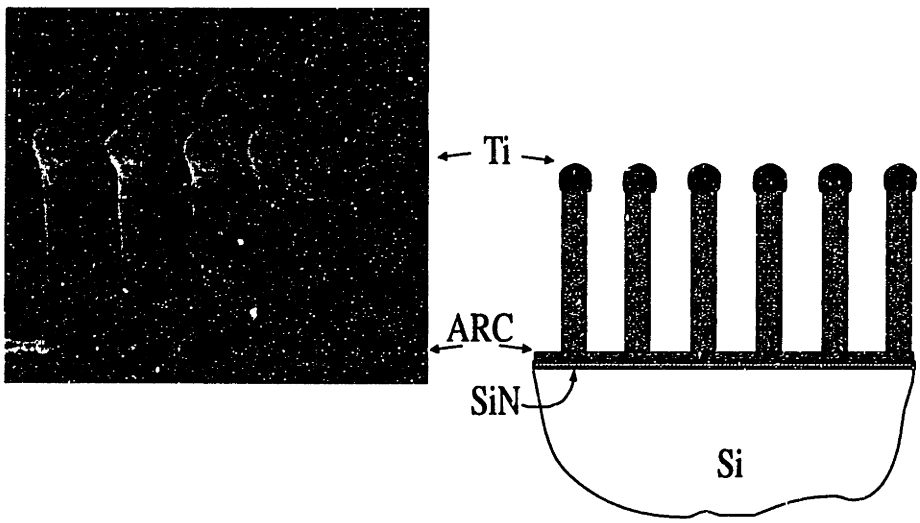


Figure 3.9 Insufficient RIE of the ARC. The ARC will dissolve in the RCA cleaning step, preventing chromium from adhering to the substrate around the bases of the posts.

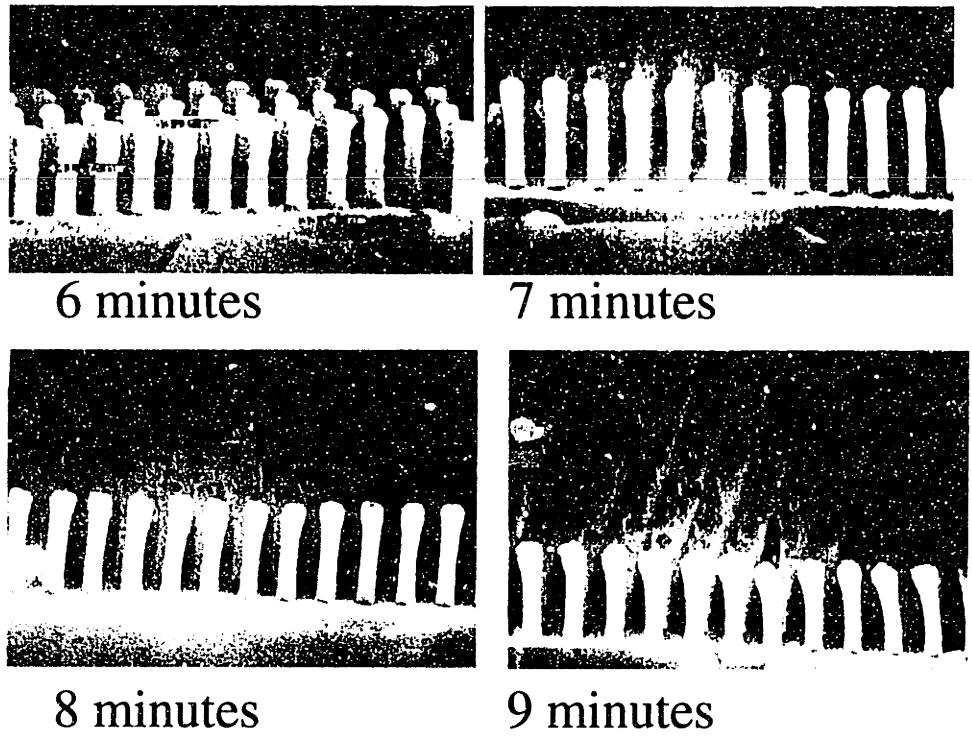


Figure 3.10 Thick ARC, 350 nm. After 7 minutes of etching all of the ARC had been etched through. However, with only one more minute of etching the posts began to fall together. The posts fell together more noticably after 9 minutes of etching.

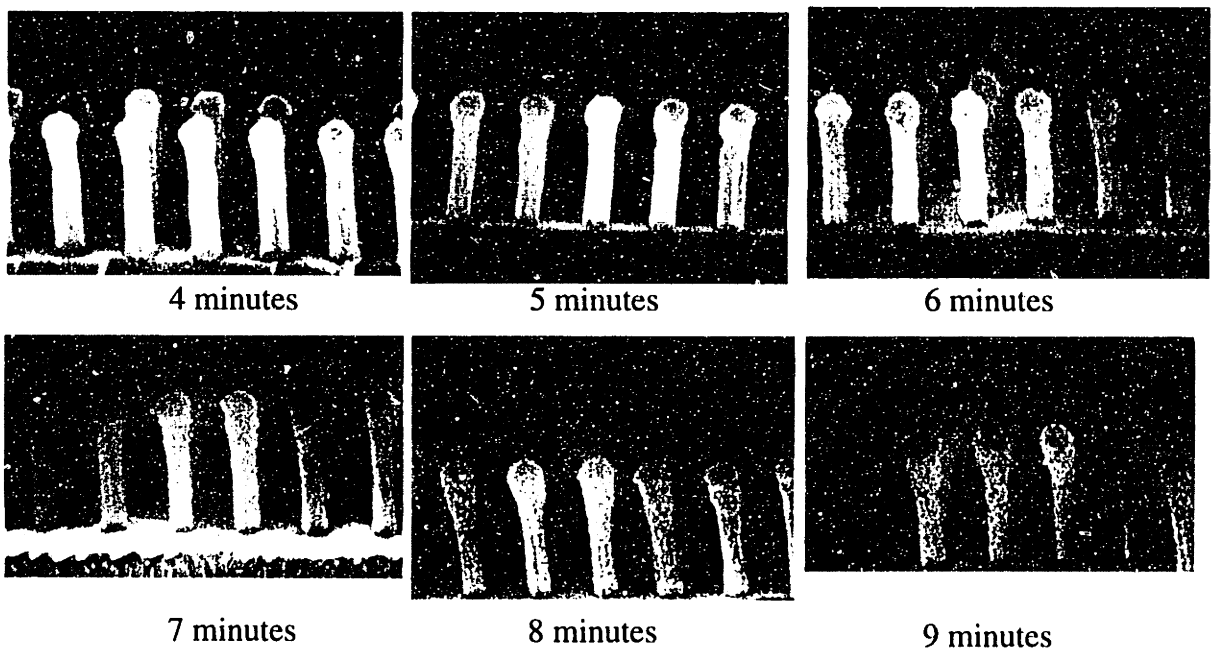


Figure 3.11 Thin ARC, 220 nm. The ARC has been completely etched through in 5 minutes. With further etching the posts became thinner but did not fall together.

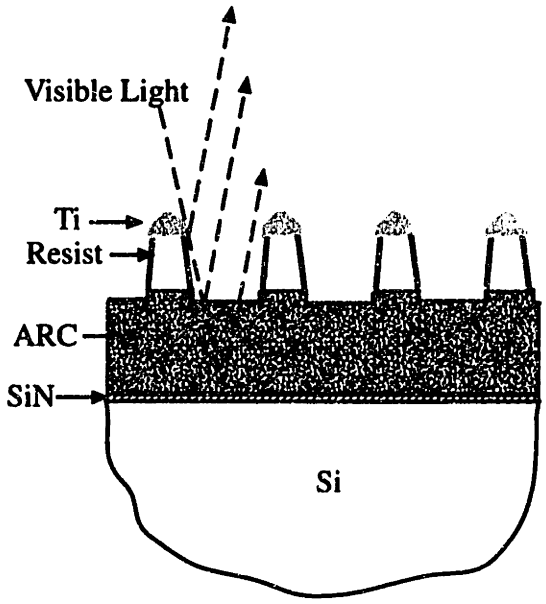


Figure 3.12 As the thickness of the ARC changes, different wavelengths of light reflecting from the air/ARC and ARC/silicon nitride interfaces constructively interfere. Diffraction of light by the posts does not affect the observed color because the period of the posts is smaller than the wavelength of visible light.

3.4 Cr Evaporation

The crucial consideration for the chromium evaporation step was to make sure the sample was centered on the evaporation plate and that the evaporation plate was exactly normal to the incident chromium atom flux. Any deviation from this configuration resulted in chromium deposition on the sides of the posts and shadowing. (Figure 3.13) The end result was oval holes in the silicon nitride. Also, it was important to use the second shutter in the evaporation chamber to block 'spitting' of the chromium at the beginning of the evaporation. Spitting refers to the ejection of chromium chunks from the evaporation target which can knock over posts on the sample.

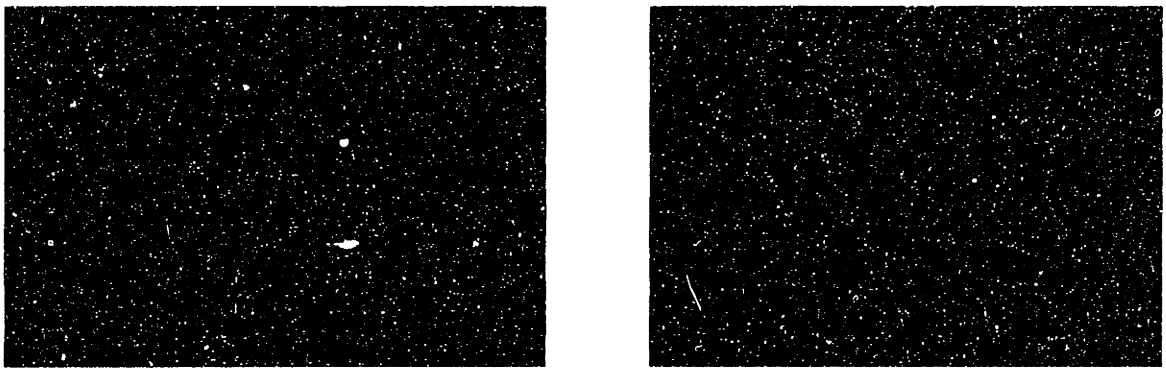


Figure 3.13 SEM micrographs of the centers of two wafers. The wafer shown in (a) was not placed in the center of the evaporation plate, and the holes in the silicon nitride are oval. The wafer shown in (b) was placed in the center of the evaporation plate, and the holes are smaller and more round.

3.5 RCA Clean

Considerable chromium redeposition occurred during the RCA clean used to remove the posts (i. e. the lift-off step). Chromium does not dissolve in RCA. If the chromium caps which were depcsited on the tops of the posts came in contact with the chromium that was deposited around the posts, the caps stuck. (Figure 3.14) If these chromium caps obscured holes which were to be transferred into the silicon nitride layer via RIE, the holes were not transferred. Several approaches were tried to alleviate this problem. The solution was to use two baths of RCA. In the first solution the posts dissolved. The wafer was then rinsed, removing some caps. The wafer was not allowed to dry because drying caused any caps which had redeposited to permanently adhere to the wafer. The second RCA bath was put in an ultrasound vessel. The ultrasound vibration shook free caps which had redeposited, and since the concentration of caps in the new clean bath was low, the chance or redeposition again was low.

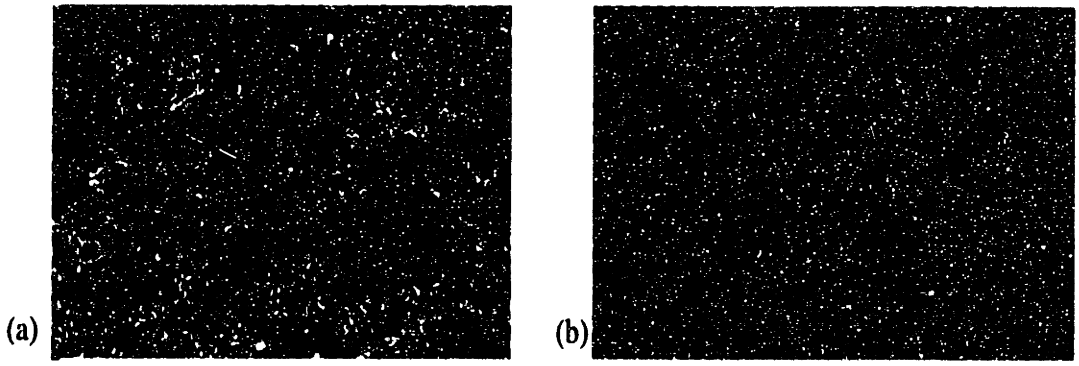


Figure 3.14 After RCA cleaning (a), chromium caps redeposited and obscured holes in the chromium mask. The obscured holes were not transferred into the silicon nitride layer (b), and inverted pyramids were not KOH etched where a chromium cap obscured a hole.

3.6 RIE of SiN

To transfer the pattern from the chromium into the silicon nitride CF_4 or CHF_3 RIE was used. Originally, CF_4 was used. However, CF_4 plasma etches silicon faster than silicon nitride.[3] Hence, it was difficult not to etch the silicon under the silicon nitride. If the underlying silicon was etched, another set of {111} planes defined the etched structure (Figure 3.15). CHF_3 prevents etching of silicon because a teflon-like polymer is deposited on silicon surfaces[4,5](Figure 3.16). This polymer must be removed to allow potassium hydroxide (KOH) anisotropic etching. The polymer can be removed either by piranha cleaning or oxygen RIE. (Piranha is a 3 parts sulfuric acid:1 part hydrogen peroxide mixture which dissolves organic compounds.)

Figure 3.15 The schematic labeled (a) depicts a CF_4 RIE etch that did not stop at the silicon nitride/silicon interface. After KOH etching, {111} planes facing downward resulted (b). The SEM micrograph (c) is a sample after KOH etching, and after the silicon nitride had been removed.

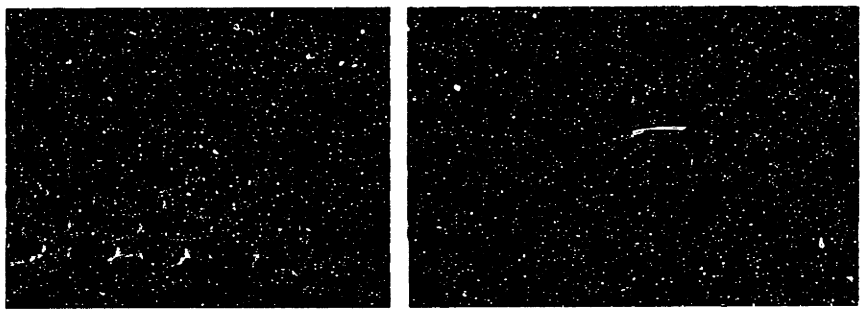


Figure 3.16 A teflon-like polymer film prevented uniform KOH etching. Etching occurred at the edges of the holes in the silicon nitride where the polymer film was thinner. As the silicon was etched out from beneath the polymer, some of the polymer film flaked off.

3.7 Cr Etch, KOH Etch of Si, HF Etch of SiN

KOH etching is slowed by silicon dioxide. To remove native silicon dioxide or silicon dioxide that resulted from oxygen RIE, a buffered HF or concentrated HF dip was used. It was found that concentrated HF and buffered oxide etch (BOE) fairly quickly dissolved the silicon nitride, and only buffered HF removed the oxide without damaging the nitride (Figure 3.17). If the silicon nitride was left in BOE or concentrated HF for too long, the nitride completely dissolved away, and there was no mask for the KOH etch.

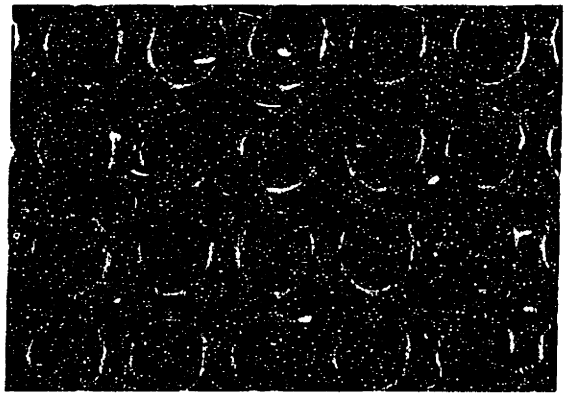


Figure 3.17 A dip in buffered oxide etch (BOE) partially dissolved the silicon nitride.

KOH etching of silicon produces gaseous products[6]. Bubbles form on the silicon surface which prevent the KOH from reaching the silicon, and etching is inhibited (Figure 3.18). Gently agitating the wafer with tweezers dislodges the bubbles.

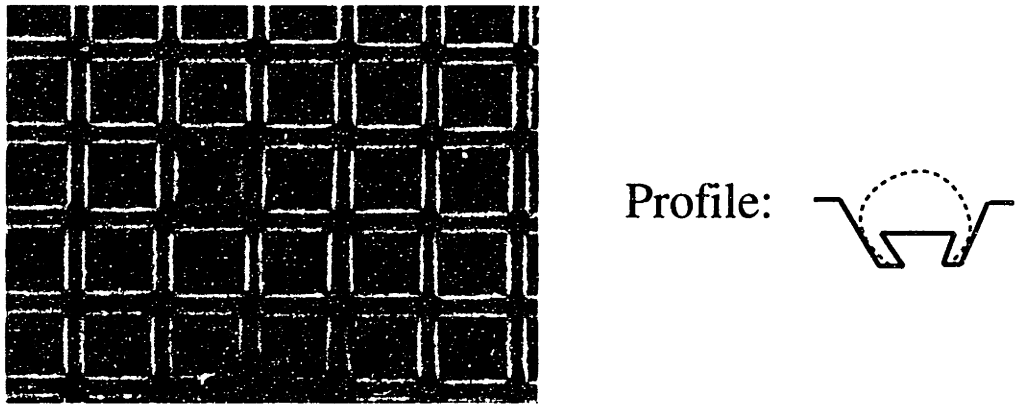


Figure 3.18 Unwanted Si in the bottom of the pyramids resulted from inadequate agitation during the KOH etching. The diagram shows a bubble protecting the silicon from the etchant.

With small, round holes in the silicon nitride, it was easy to control the width of the ridges separating the pyramids. As described in Chapter 2, this is an important factor in epitaxial growth on these substrates. An SEM can image both the edges of the silicon nitride holes and the edges of the pyramids (Figure 3.19). So, the width of the ridges can be monitored during the KOH

etch process, and etching can proceed until the desired ridge width is achieved. Although the etch rate in the <111> directions is small, it does allow for increased pyramid size with further etching. Also, there is some variation in the size of the holes in the silicon nitride across the wafer. This originates from the interferometric lithography step. The intensity of the radiation is greatest in the center of the wafer. This causes the resist posts to be thinner in the center of the wafer, and the silicon nitride holes to be smaller. So, the width of the ridges between the pyramids will decrease towards the edge of the wafer. As can be seen in Figure 3.19, 2 cm from the center of the wafer the ridges between the pyramids became so thin that in some places they were completely etched away, and in these places rectangular troughs formed.

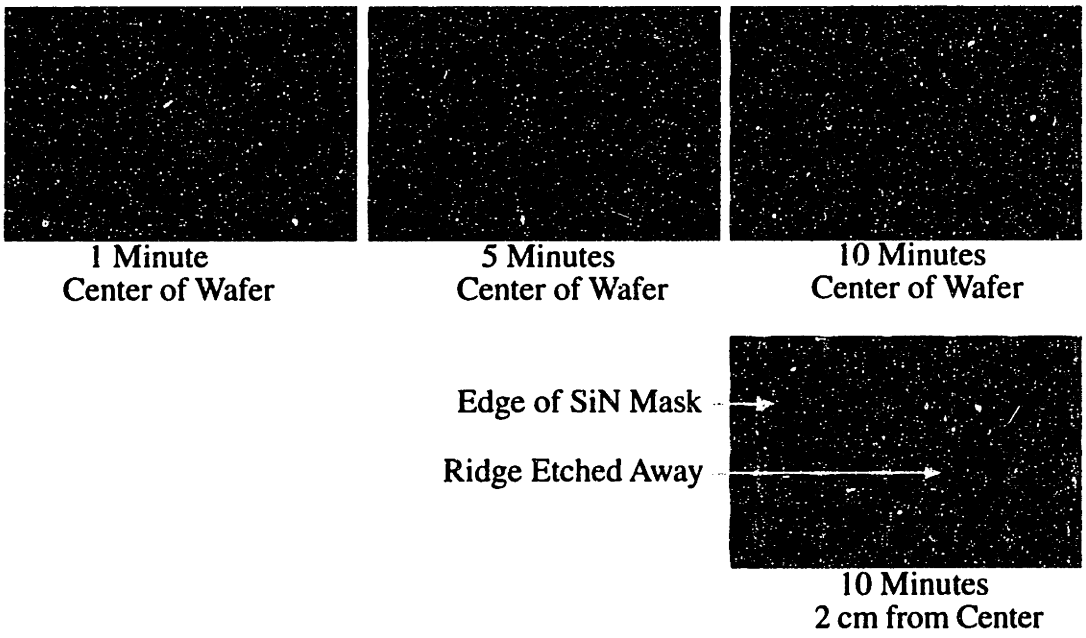


Figure 3.19 SEM micrographs at 19kV, illustrating that as KOH etching proceeds the size of the pyramids increases, and the ridges between the pyramids become smaller. The holes in the silicon nitride are larger away from the center of the wafer. This can cause the ridges to be etched away and pyramids to coalesce after long KOH etches.

In conclusion, large areas can be reliably patterned with arrays of 200 nm period inverted pyramid arrays (Figure 3.20). This is a promising structure for improving crystal quality in lattice mismatched epilayers grown on (100) silicon.

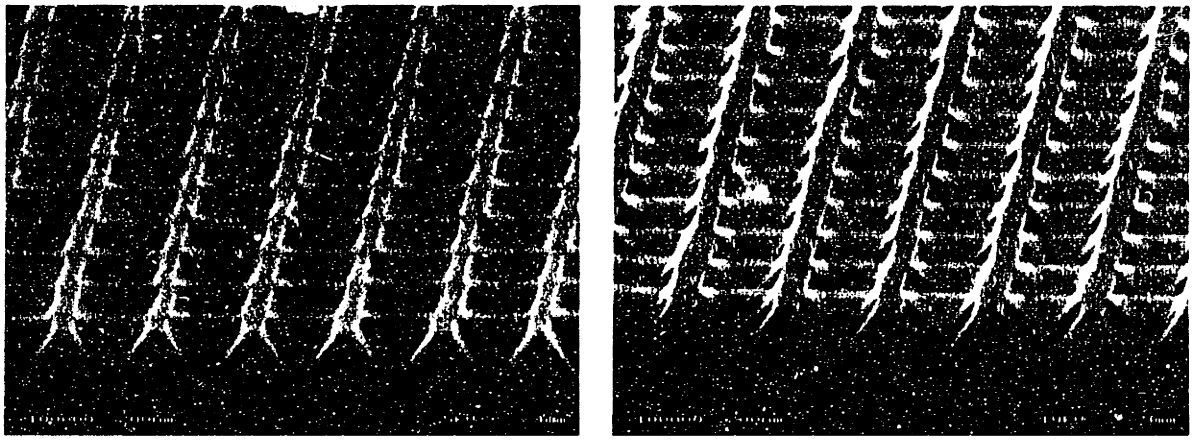


Figure 3.20 Inverted pyramid array. In SEM micrograph (b) the accelerating voltage is 19kV which is high enough to make the walls between inverted pyramids transparent.

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2 NSL/ Procedures/Holography/Gridshadow, by Ken Yee.

3 S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era Volume 1 - Process Technology*, Lattice Press, 1986, p. 556.

4 P. J. Astell-Burt, J. A. Cairns, A. K. Cheetham, and R. M. Haze. A study of the deposition of polymeric material onto surfaces from fluorocarbon RF plasmas. *Plasma Chemistry and Plasma Processing*, vol. 6, no. 4, pp. 417-427, 1986.

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Chapter 4

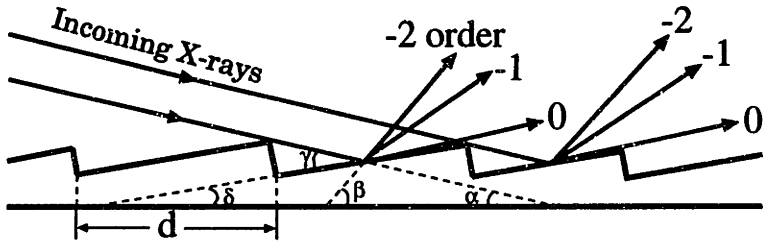
Grazing Incidence, Blazed, X-ray Diffraction Gratings

4.0 Introduction

There are a great number of astrophysical sources which emit in the 5 Å to 300 Å band. K-shell transitions of C, N, and O, and the L-shell transition of Fe are in the 6 Å to 60 Å range[1]. High spectral resolving power is required to identify these lines, which can be provided by grazing incidence, blazed, diffraction gratings. Similarly these gratings are used in spectrometers to image radiation from hot coronas of stars and to detect Doppler shifts and spectral features of intervening material[2]. In this chapter the basic operation of these diffraction gratings, traditional fabrication processes, and a new, more reliable process with higher diffraction efficiency will be discussed.

4.1 Diffraction Gratings

A groove profile with incident and diffracted rays, and the grating equation are depicted in Figure 4.1. The grating consists of triangular grooves of period, d. X-rays of wavelength, λ, at an incident angle, α, are diffracted. The mth order diffracts at an angle of β_m. The maximum diffraction efficiency occurs when the incident and exit angles on the facets are equal, or $\gamma = \alpha + \delta = \beta_m - \delta$. Determining grating parameters is a trade-off between short wavelength cut-off, diffraction efficiency, and spectral resolution[3]. It is desirable to be able to alter grating parameters easily in the design of spectrometers.



$$m\lambda = d(\cos\beta_m - \cos\alpha)$$

Figure 4.1 Diffraction of X-rays on a blazed, grazing incidence grating, and the grating equation.

4.2 Ruled Gratings

There are three methods to fabricate diffraction gratings: 1) ruling, 2) interferometric lithography with ion etching, and 3) interferometric lithography with anisotropic etching. The ruled gratings have traditionally had the highest efficiencies and are the most widely used. They are made by scribing grooves with a diamond tip[4]. The position of the diamond tip with respect to the beginning of the ruling is measured interferometrically by having a mirror attached to the diamond carriage and a mirror and beam splitter at the beginning of the ruling. The carriage progresses at a rate defined by the turning of a ruling screw and an electromechanical gear system. Errors in this system can be detected with the interferometric fringe signal and can be corrected.

Yet, there are errors in the ruling engine system which can not be totally corrected. Temperature, pressure, and humidity changes degrade the accuracy of the interferometric system. Wear on the diamond in the course of the ruling leads to changes in the groove profile[5]. Periodic errors in the ruling screw cause periodic errors in groove placement which give rise to ghosts, images of the parent line at a different angle and with less intensity. Another serious ruling error is nonparallelism of the grooves which degrades resolution. Ruling is typically done in aluminum or gold which has been evaporated on a glass substrate. The properties of evaporated metals which effect the ruling process are not well understood. Hence, two coatings of the same metal with the same evaporation parameters may not rule in the same manner. Optimal optical properties of the metals and success in ruling depend on the evaporation, and do not necessarily both result from the same evaporation parameters. Evaporations with high deposition rates have better optical properties, but are also known to have voids and small metal globules in the films. Finally, the metal thickness must be one half to several microns depending on the groove density, and this results in fairly rough surfaces, which are only partially smoothed by the ruling process.

Ruling gratings is a time intensive process. A grating 148.8 cm^2 in area with a groove density of 3600 grooves per mm required four weeks of ruling[5]. Hence, it is quite costly to produce a high quality ruled grating over a large area, and replicas of the master gratings are made. Replicas are made of these master gratings by coating the master with a parting agent followed by the

metal which is to be the replica's surface. Epoxy is poured onto the coated master, and the glass replica substrate is placed on top of the epoxy. Pressure is applied to the replica substrate so that the epoxy is as uniform and thin as possible. This is done to reduce distortion due to shrinkage as the epoxy cures. Once the epoxy has hardened, the replica and master are separated.

As can be seen in Figure 4.2, a master grating from Bixler et al.[6], the blaze facets are quite rough and have considerable curvature. The fraction of scattered X-rays depends on the square of surface roughness:

$$S = (2\pi\sigma[\sin(\alpha)+ \sin(\beta)]/\lambda)^2$$

where σ is the rms surface roughness, and S is the fraction of scattered radiation[6]. The curvature of the facets also decreases diffraction efficiency. Replicas have even less smooth and less flat profiles, and they are made with materials which degrade with heat cycling and use.

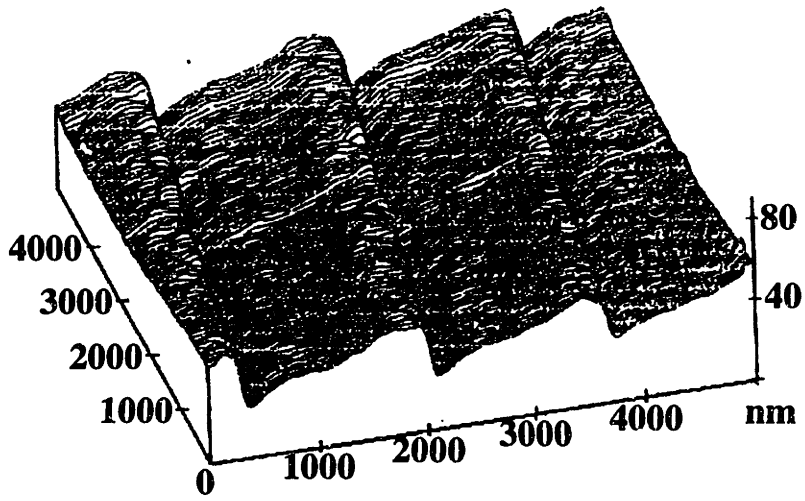


Figure 4.2 A scanning tunneling micrograph of a master ruled grating from Bixler et al.[6]

4.3 Interferometric Lithography and Ion Etching

Defining the grating with interferometric lithography greatly reduces errors in the grating pattern[7], and patterning can be completed within minutes. However, a pattern in photoresist in not very durable, and it is difficult to make a particular groove pattern in the resist, such as a blazed groove. To

make the blazed groove, ion etching is used with the resist as the mask and with the ions impinging on the substrate at the blaze angle[5, 8, 9]. Again, the resist is not very durable and etches faster than the substrate, so that only shallow etch grooves are attainable[5]. Reactive ion etching the resist pattern into a hard mask and then ion etching to make the grooves may alleviate this problem, but has not been attempted. A problem with this process that is more difficult to solve is that any edge roughness of the resist profile will be transferred into the facets, reducing flatness and resulting in the apex of a groove not being a straight line.

4.4 Interferometric Lithography and Anisotropic Etching

Another approach is to define the grating with interferometric lithography, or another lithographic technique, and to anisotropically etch the blaze facets[5, 10, 11, 12]. This has the potential of producing atomically smooth blaze facets. A silicon wafer is used as the substrate which has been cut and polished so that the (111) crystal planes intersect the surface of the wafer at the desired blaze angle. The process consists of patterning the grating in resist, transferring the pattern into silicon dioxide or silicon nitride, anisotropically etching, and then removing the silicon dioxide or nitride. The silicon dioxide or silicon nitride acts as the anisotropic etch mask. The etch rate in <111> directions is quite small compared to other directions and so the anisotropic etching defines facets that are bounded by the {111} planes. However, in previous work a good solution was not found to the problem of removing the silicon from beneath the etch mask (Figure 4.3). These silicon 'nubs' or (100) facets that are parallel to the initial wafer surface will decrease diffraction into the -1 order and will increase scatter. Roszhart[5] used thin lines for the etch mask to reduce the width of the nubs. Fujii et al. [10] did not address this issue. Philippe et al.[11] used an isotropic etch after removing the anisotropic etch mask. However, this rounds the apex of the groove, and introduces roughness on the blaze facets. Ciarlo and Miller[12] suggest continuing with an anisotropic etch after removal of the mask, which would quickly round the apex, and would be very difficult to control.

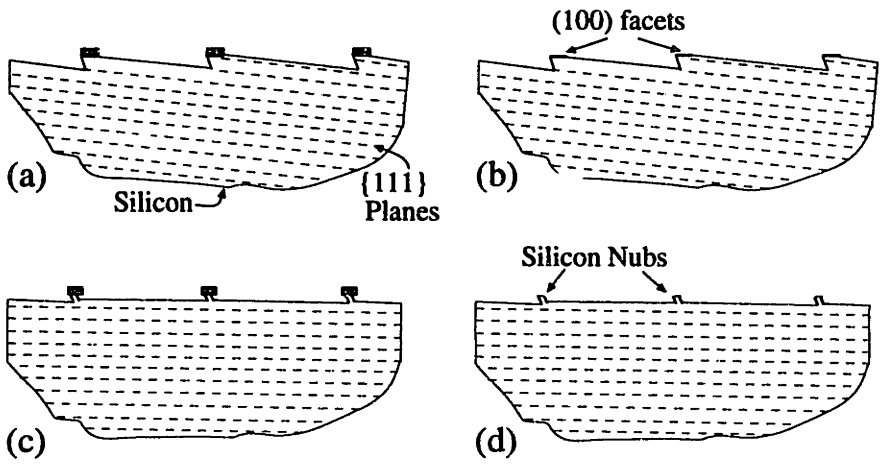


Figure 4.3 If anisotropic etching is stopped when {111} planes are reached (a), (100) facets result which reduce diffraction into the -1 order and increase scatter (b). If anisotropic etching continues (c), nubs are formed underneath the etch mask. These nubs can completely block grazing incident radiation.

In the following chapter a process is described which eliminates the nubs with a lift-off technique. Atomic force microscopy was performed to determine the smoothness of the facets, and rms roughness of less than 4 Å was achieved. Even more importantly, the gratings made with this process had peak X-ray diffraction efficiencies up 100% more than ruled gratings.

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2 John F. Meekins, Michael P. Kowalski, and Raymond G. Cruddace. Efficiency measurements of reflection gratings in the 100-300-Å band. *Applied Optics*, vol. 28, no. 7, pp. 1369-1377, 1989.

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5 W. R. Hunter. *Spectrometric Techniques, Volume IV*, Academic Press, New York, pp. 63-182, 1985.

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11 P. Philippe, S. Valette, O. Mata Mendex, and D. Maystre. Wavelength demultiplexer: using echelette gratings on silicon substrate. *Applied Optics*, vol. 24, no. 7, pp. 1006-1011, 1985.

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Chapter 5

Design of Anisotropically Etched Grating Process

5.1 Introduction

The anisotropically etched X-ray diffraction grating process steps are shown in Figure 5.1, and a detailed description of the steps can be found in Appendix B. The process began with a (111) silicon wafer off-cut so that the (111) planes were at a blaze angle to the surface of the wafer of 0.7 degrees (Figure 5.2). The wafer was coated with silicon nitride, anti-reflection coating (ARC), silicon dioxide, and Sumitomo PFI-34 resist[1]. The resist was patterned using interferometric lithography. The pattern was transferred into underlying layers by reactive ion etching (RIE). RCA removed all but the silicon nitride on the silicon. Anisotropic etching with KOH terminated on the {111} planes. Chromium evaporation and an HF etch removed the silicon nitride and protected the (111) facets desired for the blaze facets. RIE removed the silicon nubs and resulted in trenches. The incident X-rays do not 'see' these trenches, because the incident angle is so small that the trenches are shadowed (Figure 5.3).

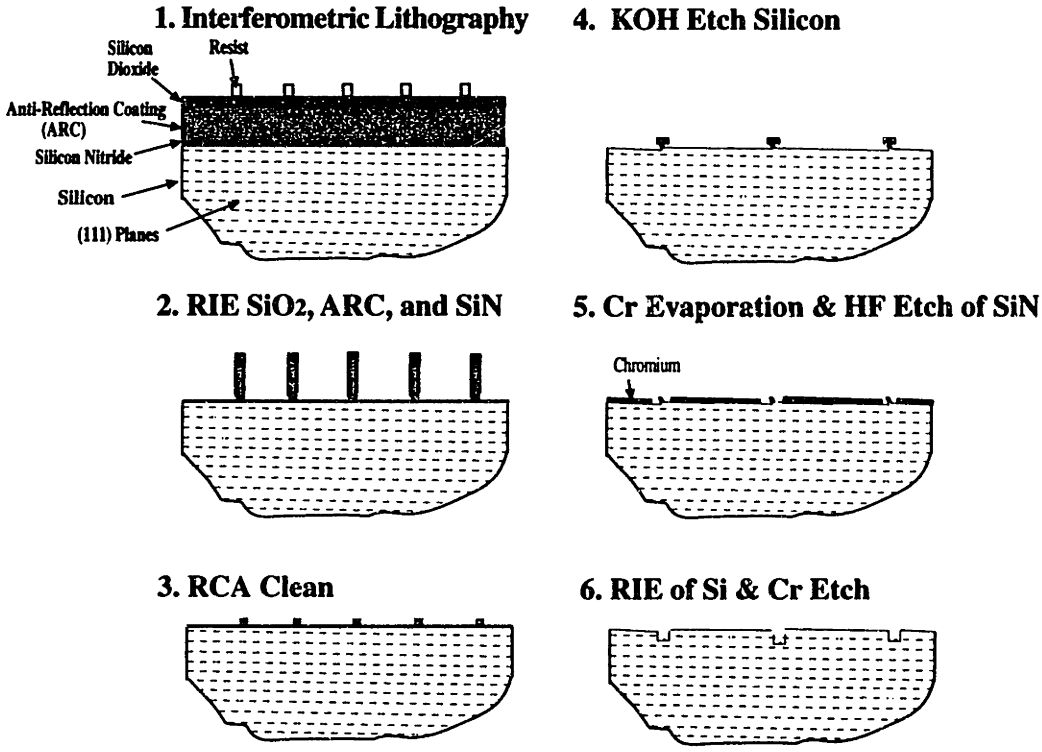


Figure 5.1 Schematic of X-ray diffraction grating process steps.

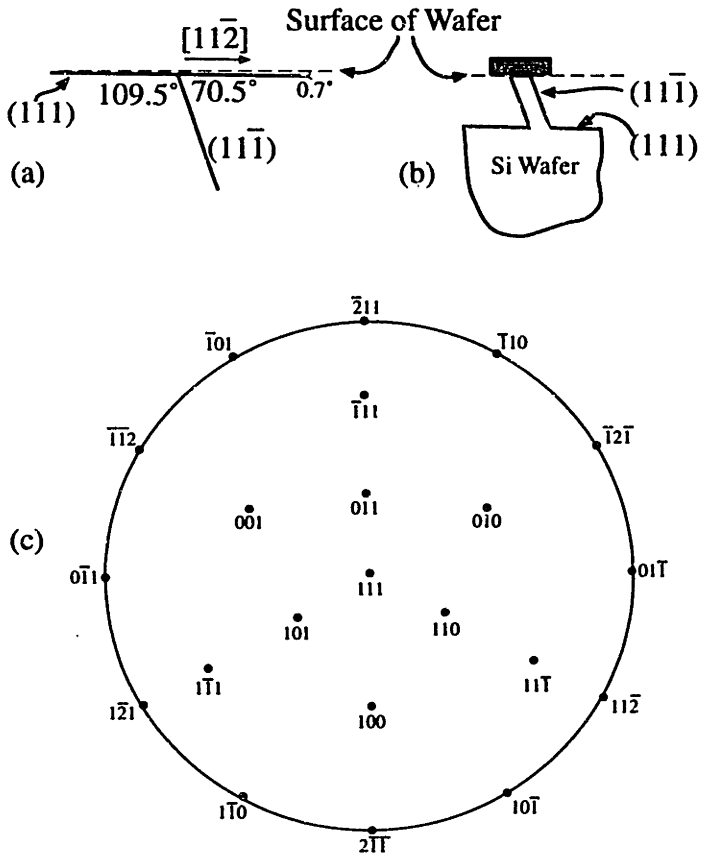


Figure 5.2 Important crystal planes and directions (a) are shown in a cross-section parallel to the ($\bar{1}$10) plane. The (111) plane can be seen to be at the blaze angle, 0.7°, to the surface of the wafer. After KOH etching (b) the (111) and (11$\bar{1}$) planes are exposed. The stereographic projection (c) indicates where the normal to plane (h l k) intersects a semisphere above a (111) wafer.

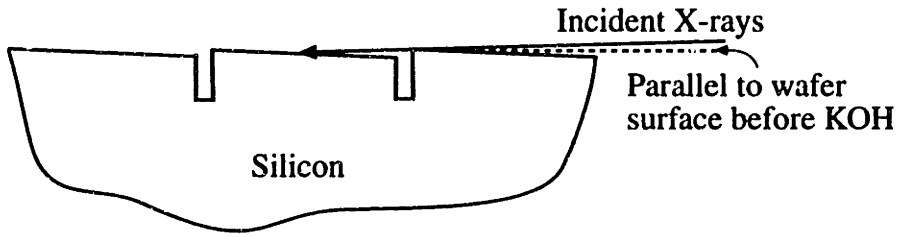


Figure 5.3 X-rays are incident on the grating at such a small grazing angle that the troughs between facets are completely shadowed.

The silicon wafers are cut from a boule which can be aligned to the desired angle to within 0.2 degrees. However, chemical mechanical polishing (CMP) may add some error to the angle the crystallographic planes make with the surface of the wafer. This may be a critical concern if large quantities of the diffraction gratings with a more precise and accurate blaze angle are desired. To ensure the correct crystallographic orientation, X-ray diffraction can be performed on each wafer after CMP to determine the crystallographic orientation to within 0.01 degrees.

The wafers must have no boron dopants. Boron greatly reduces etch rates in KOH solutions. It is also desirable to have minimal phosphorous, antimony, or contaminants as these alter the silicon lattice near the dopant atom, and may introduce roughness on etched facets.

5.1 Interferometric Lithography

Positive resist was exposed using interferometric lithography with 351.1 nm wavelength and 1.0 μm or 1.7 μm period[2]. Unlike in the pyramid process, the wafer was exposed only once so as to make a grating, instead of a grid. The dose used was 250 mJ, which is unusually high. A line to space ratio of approximately 1:10 resulted. This was desired in order to have only a small distance between blaze facets.

Correct alignment to the wafer flat was important. The lines of constructive interference had to be perpendicular to the flat, the $(1\bar{1}0)$ plane. This was because the wafers had been cut from the boule with the (111) plane tilted 0.7° towards the $[11\bar{2}]$ direction (Figure 5.2).

5.2, 5.3 RIE of SiO_2, ARC, and SiN, RCA Clean

The RIE step to etch through the silicon dioxide, ARC, and silicon nitride layers was much less critical than the RIE steps in the pyramid process. This was because the feature sizes were considerably larger and because stopping the etch at the silicon nitride/silicon interface was not necessary. However, etching of the silicon dioxide for too long resulted in unacceptably rough edges of the lines (Figure 5.4).

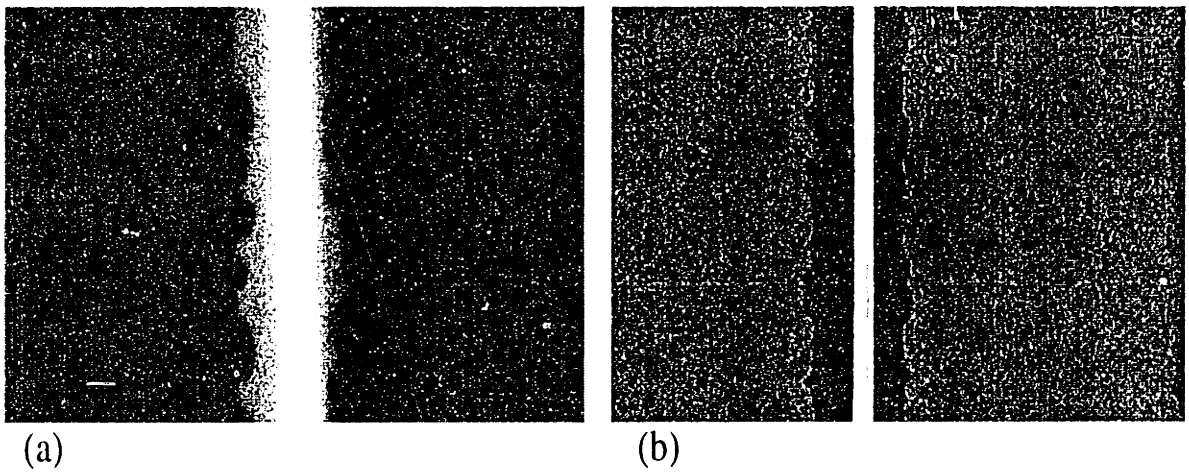


Figure 5.4 The silicon dioxide was over-etched. The edge roughness of the silicon dioxide lines transferred to the ARC and silicon nitride. In Figure 5.4(a) the rough-edged silicon nitride and the silicon ridge supporting the nitride can be seen after KOH etching. After chromium evaporation and lift-off, the edge roughness can be seen to have transferred to the chromium edge. This will also transfer into the edge of the blaze facets, causing scatter.

A polymer deposited during the CF_4 RIE of the silicon nitride was found to interfere with the KOH etch process (Figure 5.5). This was similar to the polymer that was encountered in the pyramid process, and it was also easily removed with oxygen RIE and/or piranha. The ARC present during the RIE of the silicon nitride was a probable source of hydrogen which produced similar results as RIE etching the silicon nitride with CHF_3. It was difficult to understand, however, why in some cases polymer was found on top of the silicon nitride lines. Possibly, the polymer can migrate along the surface or redeposit during the RCA clean.

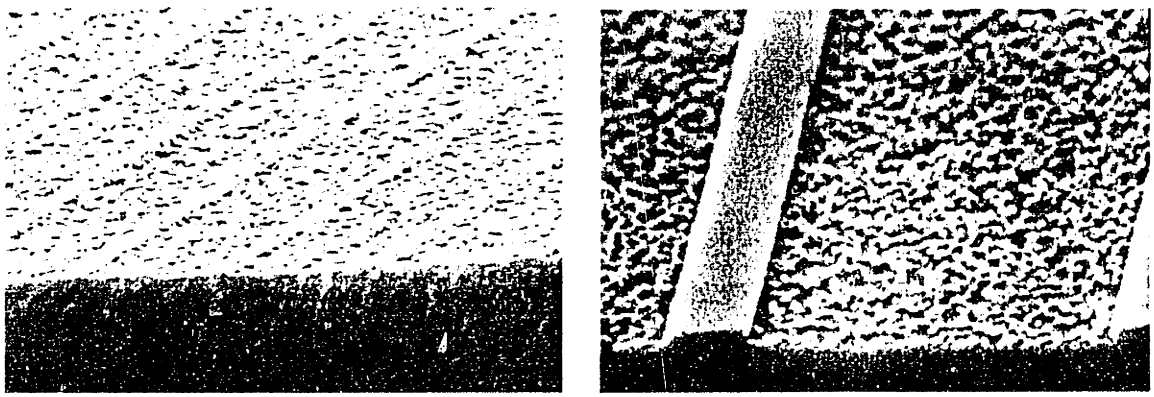


Figure 5.5 A polymer was found to impede KOH etching, and in some cases it covered the silicon nitride.

5.4 KOH Etch Silicon

The purpose of the grating process is to produce extremely smooth blaze facets. As can be seen in the SEM of Figure 5.6 (a), the $(11\bar{1})$ planes have numerous surface steps, while the blaze facets, the (111) planes, have no surface steps that are noticeable in the SEM. Surface steps can also be seen in the SEM of the (100) wafer of Figure 5.7 (a) which are similar to steps in the sawtooth structure discussed in Chapter 2.

The surface steps on the $(11\bar{1})$ planes in Figure 5.6 (a) can be explained by studying the schematics in Figures 5.6 (b) and (c). Etching in <111> directions occurs, since this etch rate is small yet not negligible. The surface steps are due to misalignment of the silicon nitride strips to the crystallographic planes (Chapter 1), and the edges of the silicon nitride strips not being perfectly straight. In Figure 5.6 (b), roughness of the silicon nitride edge is depicted. The $(11\bar{1})$ planes are pinned by the silicon nitride, and so there are surface steps in the $(11\bar{1})$ planes. The surface steps expose non-{111} planes at the convex corners, and so are etched quickly. The steps must be etched to the edge of the wafer unless there is a step being etched in the opposite direction (Figure 5.6 (c)). In this case, once the two convex corners come together, the step can be etched away. A detailed study is needed to understand more fully how these steps are etched, and whether they are nearly eliminated given enough etching.

In contrast, there is no etch mask to pin the etch front in the downward direction and no surface steps are noticable on the (111) planes (Figure 5.6(a)). However, the (111) blaze facets are most likely not atomically smooth. Surface curvature of standard wafers is less than 40 μm from peak to valley for a standard 4" wafer[3]. As depicted in Figure 5.6 (d), if the crystallographic planes do not conform with the curvature of the wafer, etching will leave surface steps. The atomic spacing of (111) planes is 1.81 Å. So in this worst case, there would be atomic steps approximately every 0.25 μm, assuming also that none of these steps are etched away. Surface steps also nucleate at crystalline defects. Given enough time, an equilibrium density of surface steps is reached on the (111) blaze facets. However, these steps are of such small height and/or density that they were not detected with a AFM and may not be a significant factor in reducing X-ray diffraction efficiency.

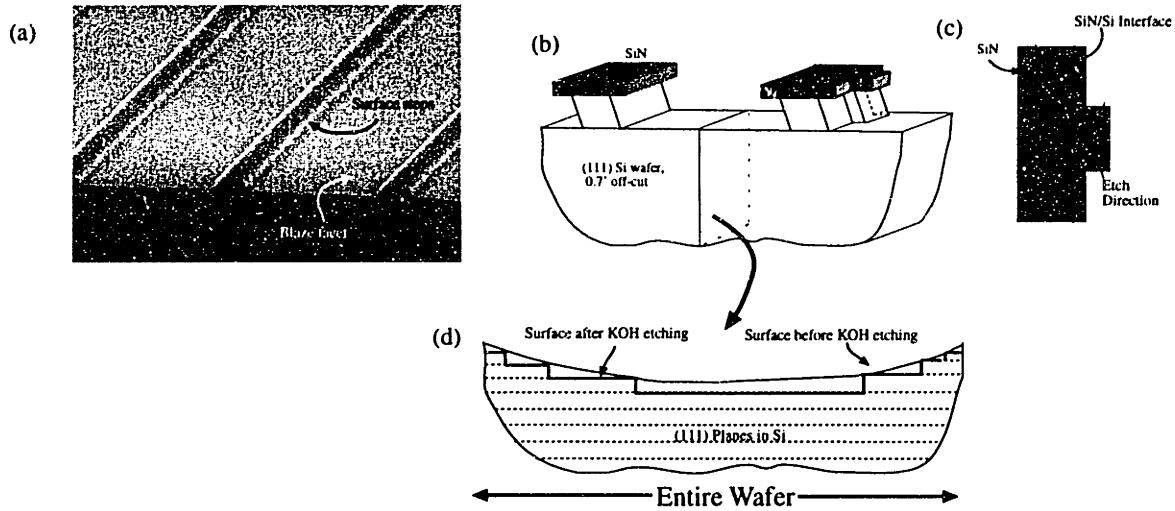


Figure 5.6 (a) is an SEM micrograph after KOH etching. Note the roughness of the $(11\bar{1})$ planes which intersect the silicon nitride. The blaze facets, though, do not have any noticeable steps. Roughness of the silicon nitride is depicted (b). A top view of the silicon nitride and the silicon nitride/silicon interface is depicted (c). Once etching proceeds to the point where the two convex corners come together, the step can be etched away. The entire wafer is depicted (d) with an exagerated surface bowing. (d) is the cross-section of (b) indicated. Surface steps on the blaze surface may result from the wafer bowing or not being polished parallel to the (111) plane.

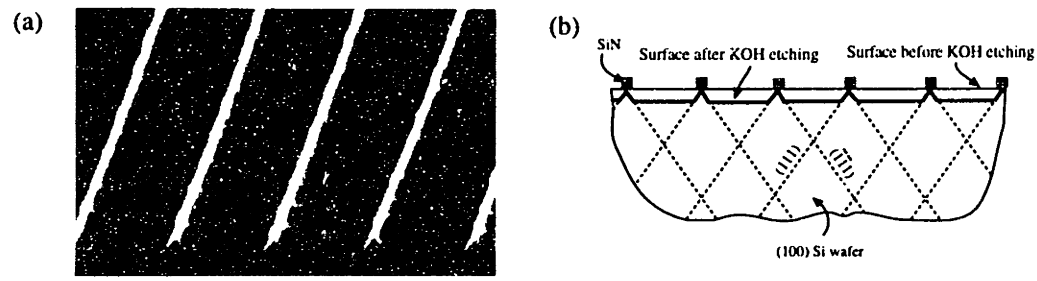


Figure 5.7 KOH etching of a (100) wafer can also lead to surface steps on the planes that intersect the mask. (a) is the SEM after partial etching of a sawtooth pattern. (b) depicts the positions of the {111} and how etching will proceed.

5.5 Cr Evaporation and HF Etch of SiN

For sucessful lift-off a material must protect the silicon blaze facets from the HF, and allow the silicon nitride to dissolve so the underlying silicon is exposed. In Figure 5.8(b), a top view after chromium evaporation and HF,

etching has occurred at the chromium grain boundaries, yet has not completely etched through the layer. However, the chromium on top of the silicon nitride has not been removed. In Figures 5.8(c) and (d), SEMs taken near a cleaved edge, this can be explained by noticing that there is not a large height difference from the regions with silicon nitride and the blaze facets. Hence, the chromium film was continuous.

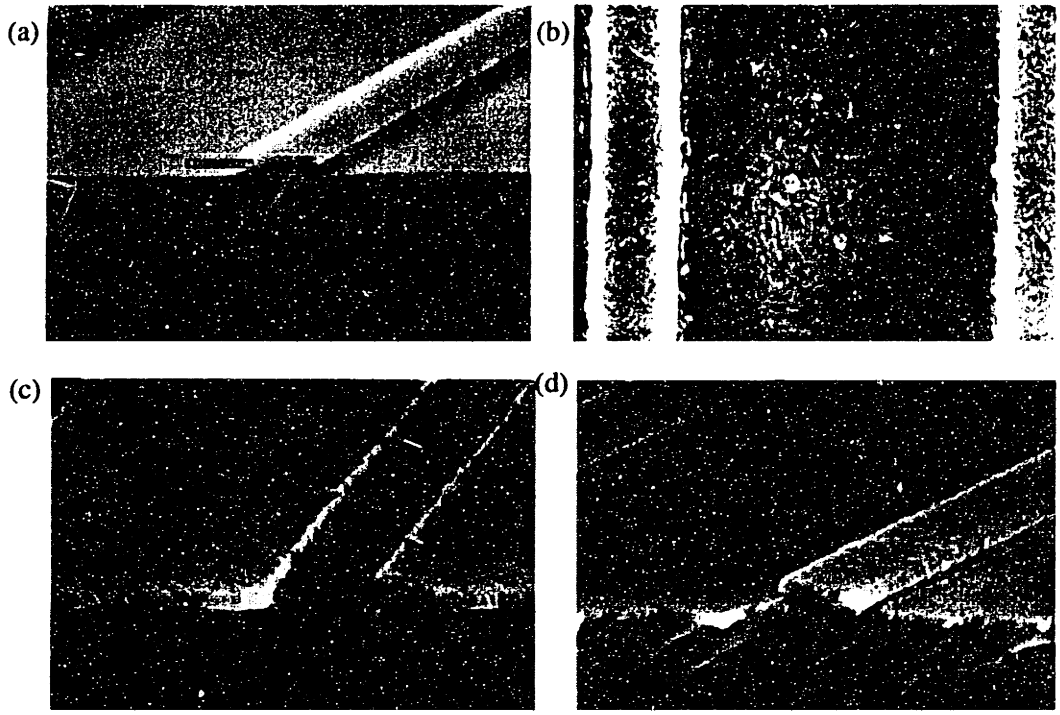


Figure 5.8 (a) is a sample after KOH etching. (b) shows the etching of the chromium grain boundaries after chromium evaporation and HF. (c) and (d) are along a cleave, where some of the chromium peeled off.

In Figure 5.9, another sample is shown where lift-off was not successful. High pressure CO_2 was used to remove some of the chromium, exposing silicon nitride which had not been etched with HF long enough to completely dissolve. The longer the sample is exposed to the concentrated HF, the longer the chromium protecting the blaze facets is etched. Depositing a thicker chromium film, would allow longer HF etch times. However, if the film is continuous, the silicon nitride will not be exposed to the HF. Clearly, another approach is necessary.

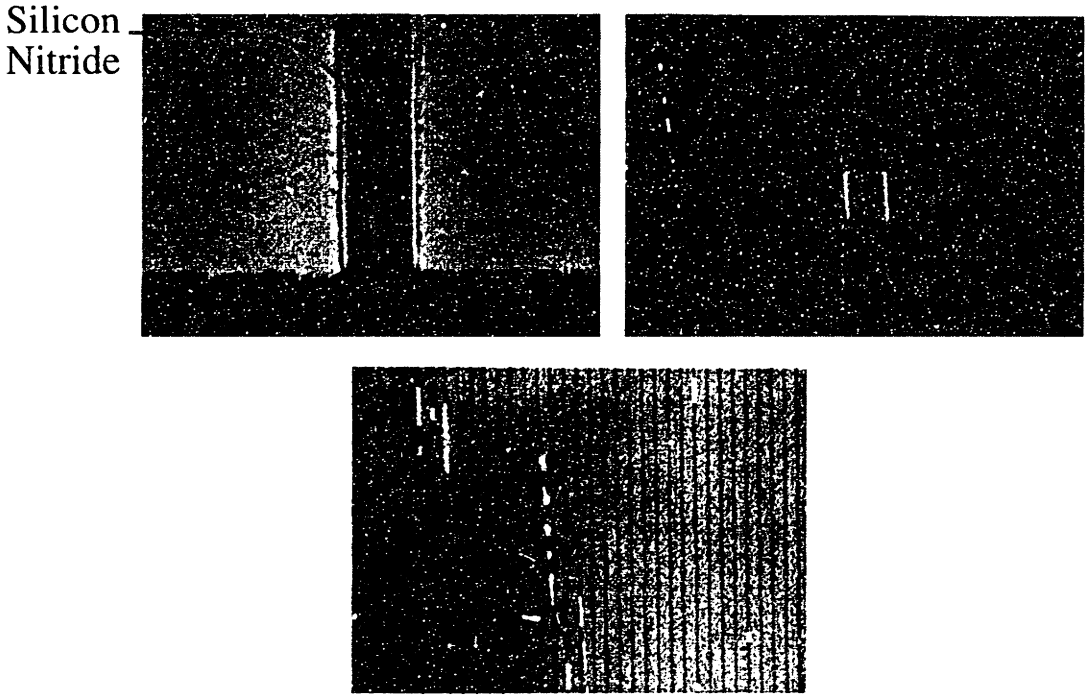


Figure 5.9 Another sample with unsuccessful lift-off. High pressure CO_2 was used to blow off the chromium strips revealing that the silicon nitride was not completely removed.

KOH etching until the silicon nitride was greatly undercut was found to give more successful lift-off (Figure 5.10). Etching in the <111> directions, the slowest etching directions was necessary. To increase the etch rate, the KOH concentration was increased to 20% KOH by weight. Etch times were on the order of 15 minutes at room temperature. Adding KOH to water is exothermic. The solution was allowed to cool to room temperature in order to have consistent etch rates.

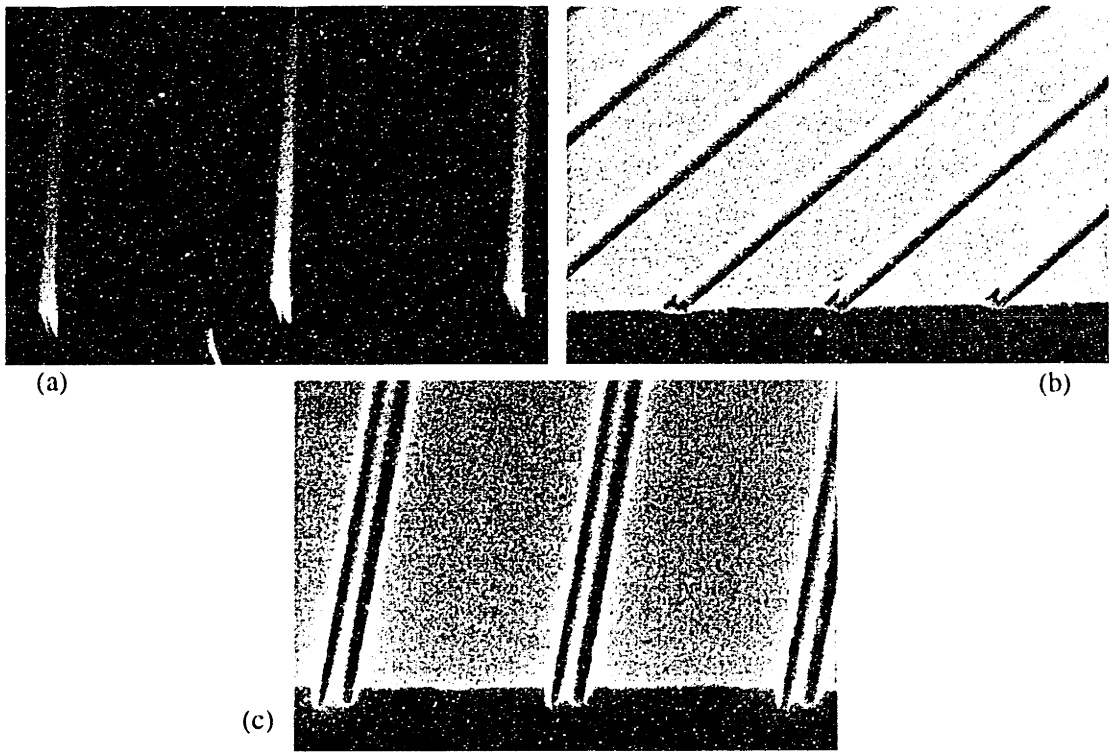


Figure 5.10 SEMs showing a sample after a long etch in 20% KOH by weight (a), after chromium evaporation and HF etch (b), and after the silicon nubs have been RIE etched down into troughs (c).

5.6 AFM Analysis of Gratings

If the KOH solution is not allowed to cool to room temperature, KOH can crystallize out of solution and deposit on the sample in rinsing (Figure 5.11). The crystals are not easily removed in piranha, RCA, or solvents. A similar result has been found to occur when etching silicon to expose silicon nitride membranes for X-ray lithography masks. Rinsing in water heated to the KOH solution temperature or higher, or allowing the KOH solution to cool to room temperature before etching are solutions to this problem.

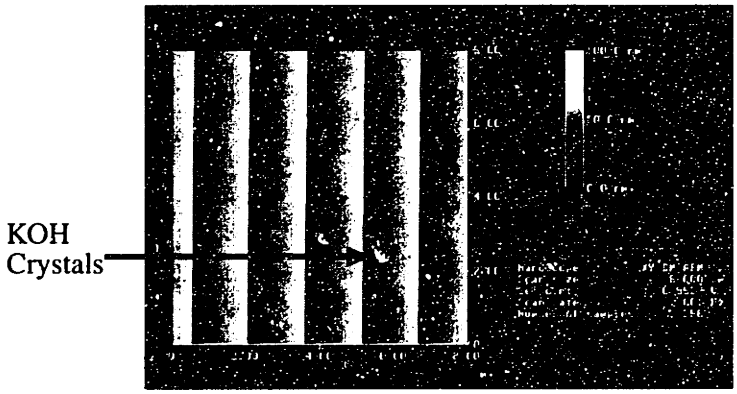


Figure 5.11 AFM micrograph showing KOH crystals remaining from rinsing the sample in water cooler than the KOH solution. The crystals are not removed with piranha, RCA, or solvents.

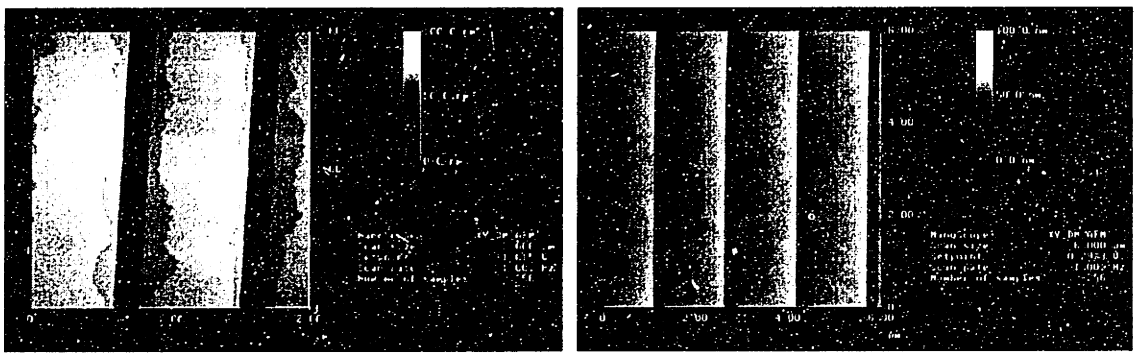


Figure 5.12 AFM micrographs showing how the silicon ledge is reduced (b) by careful RIE of the silicon nubs.

After etching the chromium away to complete the gratings, ~5 Å steps were found on the silicon blaze facets (Figure 5.12(a)). The cause of this problem was thought to be removal of silicon by lateral etching beneath the chromium in the CF_4 RIE trough etching step. A thin layer of native oxide can form on the silicon before evaporation of chromium. This oxide will dissolve quickly in the subsequent concentrated HF etch. This results in the chromium film not being supported where the oxide has dissolved away. The RIE plasma could laterally etch the silicon underneath the chromium film. This phenomenon was reduced by doing a buffered HF dip before chromium evaporation to remove any native oxide, and by reducing the RIE etch time (Figure 5.12(b)). The CF_4 RIE trough etching step can be carefully monitored with the AFM. The RIE is stopped after half the etch time that is known from past runs to be

sufficient. Short RIE etches are continued until the AFM confirms that the silicon nubs are completely concealed in the troughs. The ledge is wider on the lower edge of the blaze facet, which is shadowed, and therefore less likely to scatter X-rays. Further study is required to completely eliminate the ledge on the upper edge of the blaze facet.

The anisotropically etched gratings are much smoother and have less curvature than mechanically ruled gratings (Figure 5.13). As discussed in Chapter 4, these features are believed to increase diffraction efficiency.

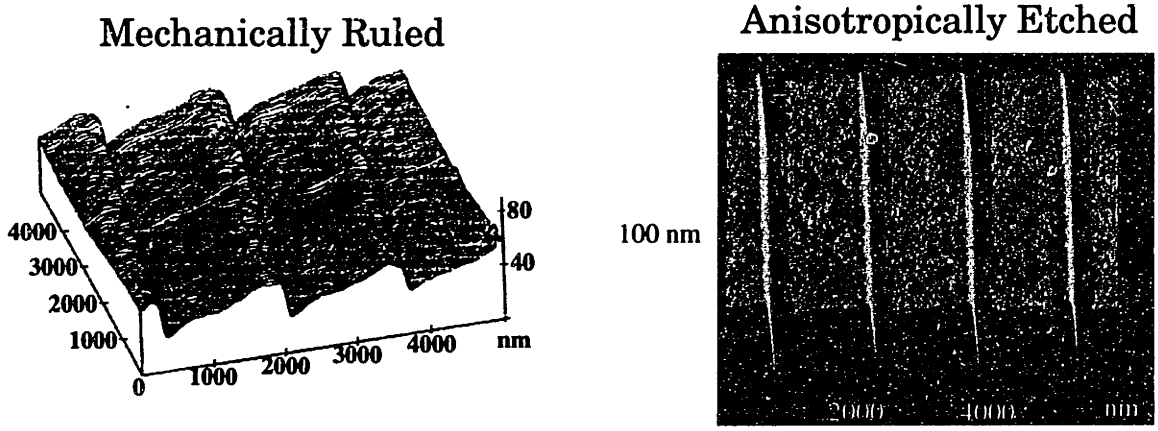
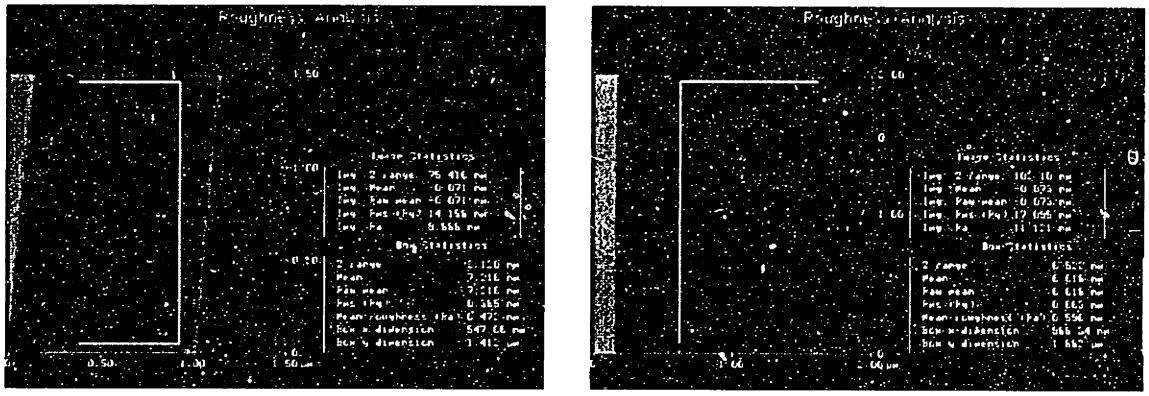


Figure 5.13 AFMs of a mechanically ruled master and an anisotropically etched grating.

Roughness analyses of the anisotropically etched gratings before and after coating with 50 Å of chromium and 200 Å of gold are shown in Figure 5.14. Without chromium and gold, the rms roughness of the blaze facet is less than 4 Å. With the chromium and gold the rms roughness is less than 7 Å. The roughness of the facets without chromium and gold is comparable to measurements of polished silicon wafers and cleaved edges of silicon wafers.



(a) (b)

Figure 5.14 Roughness analyses of blaze facets before (a) and after (b) evaporation of chromium and gold on the sample.

The definitive test, though, is to compare X-ray diffraction efficiencies. As described in greater detail in Appendix C, researchers at Columbia University and Lawrence Berkeley Laboratories tested the diffraction efficiency. The peak efficiency in the first order for the cases tested was ~24% for the anisotropically etched grating. The peak efficiency in the first order for the ruled replica grating was ~13%.

Another advantage of anisotropically etched gratings over ruled gratings is the flexibility and reliability of the process. It is difficult to get gratings of a precise blaze angle and period from the ruling process due to the problems discussed in Chapter 4. However, simply by ordering a different cut of the silicon boule, the blaze angle can be specified to within +/- 0.2°. The period is chosen by exposing that period in the resist, and can be 200 nm or greater.

1 M. L. Schattenburg, R. J. Aucoin, and R. C. Fleming. Optically matched trilevel resist process for nanostructure fabrication. *J. Vac. Sci. Technol. B.*, vol. 13, no. 6, pp. 3007-3011, 1995.

2 M. L. Schattenburg, E.H. Anderson, and H. I. Smith, X-ray/VUV Transmission Gratings for Astrophysical and Laboratory Applications, *Physica Scripta*, vol. 41, 13-20 (1990).

3 Semiconductor Equipment and Materials Institute, *Book of SEMI Standards*, 1995.

Chapter 6

Future Work, Other Applications

The inverted pyramid process is quite well understood. Clearly, the next step with this research will be to grow InP, GaAs, or SiGe on the inverted pyramid structure, and carefully analyze the epilayers. RHEED and SEM studies are necessary during the growth process to determine how the epilayer materials nucleate, how material crystallizes during the temperature ramp up to growth temperature, and how growth proceeds. Double crystal x-ray diffraction and more importantly high resolution TEM are needed to study any crystal defects, and to determine their cause.

A couple of other applications for the arrays of inverted pyramids were explored. First, they can be used as substrates for the crystallization of biological samples. Professor Carl Pabo of the MIT Biology department is researching the structure of DNA-binding proteins and protein-DNA complexes[1,2]. To understand the structure of these proteins they are crystallized and examined with X-ray diffraction. However, it is often difficult to get the complicated proteins to crystallize. In speaking with Professor Pabo, it became clear that the inverted pyramids might be a solution. The protein crystals have been found to nucleate on scratches in glass slides. The inverted pyramid structure is an array of 'scratches', and the bottom points of the pyramids may be an ideal place for protein nucleation. By changing the interferometric lithography setup to produce grids with different periods, several crystallization substrates could be attempted to find the geometry most useful for the nucleation of a particular protein.

Another potential application for the arrays of inverted pyramids is as surfaces with increased absorption for solar cells and night vision optics. High absorption of light is desired for solar cells, and low reflectivity is desired at infrared wavelengths for night vision optics. Patterning a silicon wafer with an array of inverted pyramids of 200 nm period is a promising method for decreasing reflectivity of silicon surfaces at visible and infrared wavelengths. The period of the pattern is less than the wavelength of light, and so will not cause diffraction, while the index of refraction gradually varies from that of air to that of silicon.

Initial tests were performed to investigate this idea. A laser of 633 nm wavelength was set up on an optical table, and the beam was reflected from a

polished wafer and a wafer patterned with inverted pyramids (Figure 6.1(a)). Initially, the detector was placed directly in front of the laser as a reference, and 2.3 mW was detected. To test whether there was simply more scatter, or if more radiation was actually being absorbed, the experiment depicted in Figure 6.1(b) was carried out. Scatter from the substrate was collected by the integrating sphere and was detected with the optical power meter at the side port. For a reference, the sample port was closed, and 138 μW was detected. As can be seen in Figure 6.2, for both experiments, approximately half the power was detected with the patterned wafer in comparison to the polished wafer. Although, these were not rigorous experiments, they indicate that there is promise in patterning wafers with inverted pyramids to decrease reflectivity. Experiments with a spectrum of wavelengths and carefully scanning incidence and reflectance angles would provide more insight.

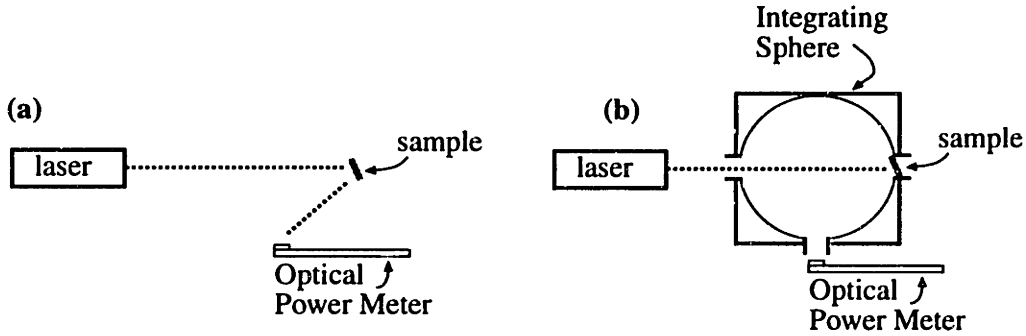


Figure 6.1 Experimental set-ups to test absorption of inverted pyramid patterned silicon versus polished silicon.

ReflectivityTest

Polished Silicon	Pyramid Patterned
795	363
761	346
792	368

Scatter Test

Polished Silicon	Pyramid Patterned
33	17
35	17
37	18

Figure 6.2 The units for the data in the tables is μW. Measurements were repeated three times. Both reflectivity and scatter intensity were approximately half as large with the patterned sample.

The grazing incidence, blazed, X-ray diffraction grating process is somewhat less mature. There is still work to be done to confirm the idea that the ledge in the silicon blaze facet is due to the silicon being exposed to the CF_4 RIE trench etch. To do this, the chromium used for the lift-off step could be evaporated at angles so that chromium partially covers the silicon nubs (Figure 6.3). This has been attempted, yet lift-off was not successful, probably because the evaporation angles were too shallow and a continuous coating resulted. Cleaving and examining the sample with SEM to determine the exact nub height would give information on what appropriate evaporation angles would be. If lift-off was successful, the intersection of the (111) plane with the $(11\bar{1})$ plane would define the edge of the blaze facet, which would be much less jagged than the silicon nitride edge. Also it would be more difficult for the concentrated HF to dissolve material at the chromium/silicon interface of the blaze facet since the HF would have to etch material at the chromium/ silicon interface of the nubs first.

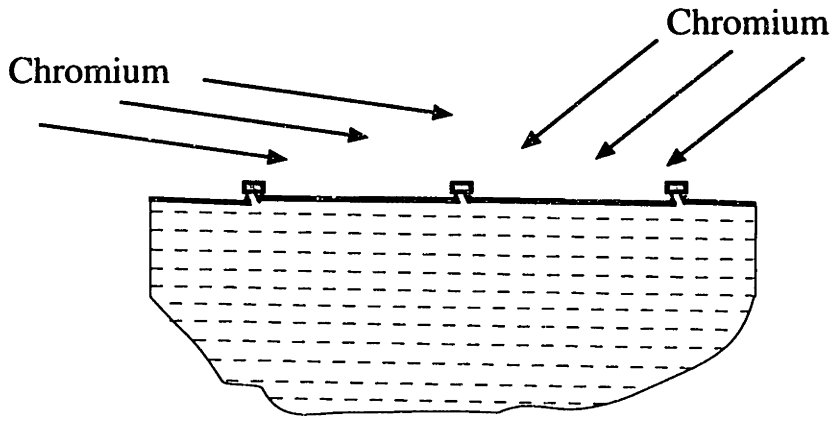


Figure 6.3 Proposed chromium evaporation for lift-off in the X-ray diffraction pattern to improve groove straightness and eliminate the ledge believed to be caused by RIE etching of the silicon nubs. Note that the two evaporation angles would be different because of the asymmetry of the nubs.

Another possible application of this process would be for use as line narrowing optics in eximer lasers at either 248 nm or 193 nm wavelength. Currently, ruled replica gratings are being used, which degrade quickly, and have to be replaced. The grating facets which are 78° from the substrate normal are used in Littrow to choose a high order diffraction and amplify it. By slightly altering the process described in Chapter 5, a grating could be

made with higher efficiency and which would not appreciably degrade with use.

The process changes needed would be to decrease the interferometric lithography dose, so that the line to space ratio would be smaller. This would produce wider silicon nitride lines, permitting more etching in the <111> directions so that the silicon nubs would be taller. The nubs have to be high enough to shadow the substrate to the foot of the next nub. (See Figure 6.4)

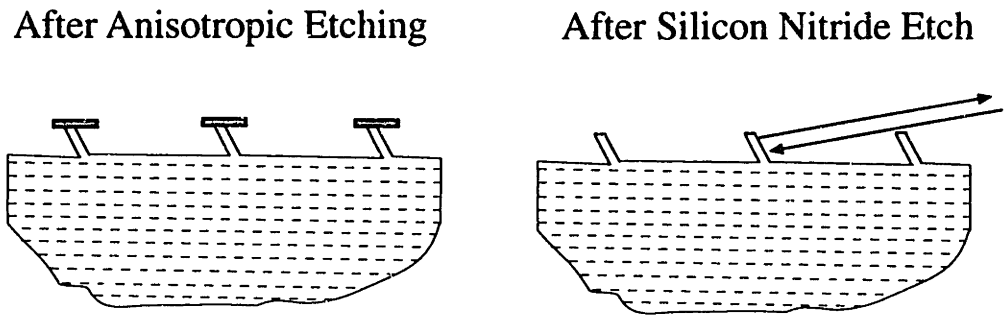


Figure 6.4 Having wider silicon strips for the anisotropic etch would allow longer etching, and would result in taller nubs, ideal for gratings needed in eximer lasers.

1 Steven R. Jordan, Timothy V. Whitcombe, Jeremy M. Berg, and Carl O. Pabo. Systematic variation in DNA length yields highly ordered repressor-operator cocrystals. *Science*, vol. 230, pp. 1383-1385, 1985.

2 Steven R. Jordan and Carl O. Pabo. Structure of the lambda complex at 2.5 Å resolution: details of the repressor-operator interactions. *Science*, vol. 242, pp. 893-899, 1988.

Appendix A.

Recipe for Inverted Pyramid Process

1. In ICL, have 300 Å of silicon nitride (SiN) deposited on (100) Si wafers. Either stoichiometric or Si-rich SiN is acceptable.

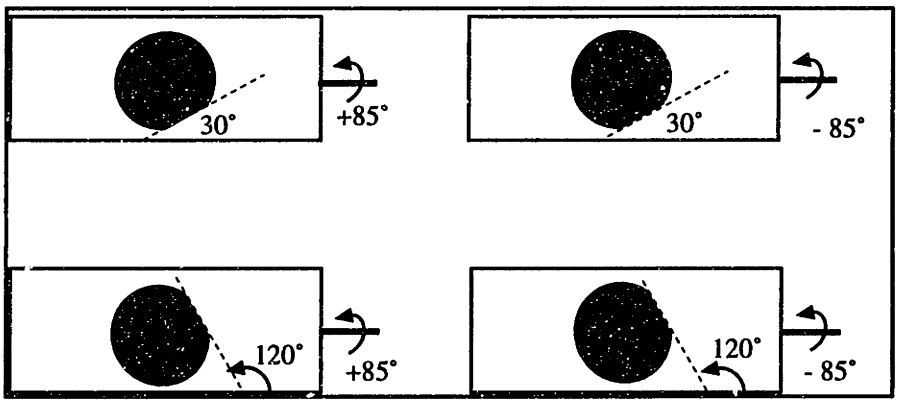
2. Spin 2200 Å of Brewer XL2200 ARC.
   - It is recommended that five monitor wafers (without SiN) are processed from this point on, to determine the appropriate interferometric dose, and to determine the cause of processing problems.
   - Spin at 5 krpm.
   - Bake at 180°C for 30 min.

3. Spin 1750Å of 1813 Shipley resist.
   - Spin at 4.5 krpm.
   - Bake at 90°C for 30 min.

4. Expose 200 nm period grids with interferometric lithography.
   - Align the wafer so that the lines of constructive interference will go parallel to the flat in one exposure, and perpendicular to the flat in the other exposure.
   - Shoot 3 monitors at 6, 8, 10 mJ/cm^2 doses.
   - Develop for 15 seconds in MF 352 at room temperature, and SEM.

5. Calculate appropriate Ti cap shadowing angles.
   - NSL/Procedures/Holography/Gridshadow.
   - Cap height calculation (Chapter 3).

6. Evaporate Ti caps.
   - Typical results of Step 5 are +/- 85° plate tilt with respect to horizontal, wafer flats aligned to 30 and 120° with respect to the plate edge,and 75Å of Ti at each of the four angle configurations.



7. Reactive Ion Etch (RIE) the ARC.
   - He 10 sccm.
   - O2 5 sccm.
   - Set DC to 250 V.
   - Set Reflected Power to 0 W.
   - Power should be between 150 and 180 W.
   - Ignition Pressure 35 mTorr.
   - Ignition run time 5 sec.
   - Chamber Pressure 7 mTorr.
   - It is recommended that a 10 minute cleanup run is done before actual samples, allowing the power to stabilize and cleaning the chamber of previous gases.
   - Do an 8 minute run. To ensure that the etch is complete, vent the chamber, look at the wafer, and do another 30 second run. If the color hasn't changed and is uniform across the wafer, the etch is complete. If the etch is not complete, everything will lift off in Step 11.

8. Evaporate Cr for liftoff.
   - Evaporate 300 Å of Cr with the plate at 0°, horizontal.
   - The sample must be in the middle of the plate. Do NOT use the mount that allows the plate to rotate. Small errors in the tilt angle result in oval holes after liftoff.

9. RCA (liftoff).
   - Prepare two large RCA beakers with RCA (ammonium hydroxide: hydrogen peroxide:DI water, 1:1:5). Set the first hotplate to high. Set the hotplate for the second beaker to ~6, so it will come up to 70°C in ~20 minutes.
   - With a q-tip and acetone remove ARC and Cr from the outer-most ring of the wafer (~1 cm wide). This outer-most ring was not exposed to the plasma in Step 7. If this material is not removed, it will liftoff in the RCA, and could redeposit.
   - Once the first solution is at 70°C, with tweezers put the wafer in the first solution face up for 20 minutes. If the ARC was completely etched in Step 7, the Cr will not peel off the center of the wafer.
   - Slowly pour off the RCA of the first solution, rinse the wafer, and put it in the second solution. Don't let the wafer dry. Put wafer in second RCA bath.
   - Put the second solution in ~3" of water, in vessel 3. Turn on the ultrasound at 65 W for 5 minutes.
   - Rinse with water, and dry with a N2 gun.
   - Inspection of the wafer with SEM is recommended at this point. There should be small, round holes in the Cr.

10. RIE the SiN.
    - CHF3 15 sccm.
    - Set DC to 300 V.
    - Set Reflected Power to 0 W.
    - Power should be ~300 W.
    - Ignition Pressure 35 mTorr.
    - Ignition run time 5 sec.
    - Chamber Pressure 10 mTorr.
    - It is recommended that a cleanup run is done before actual samples, allowing the power to stabilize near 300 W and cleaning the chamber of previous gases.
    - A 1 minute run is adequate. However, if the power is low, ie. 100 W, do a proportionally longer run, 3 minutes.

11. RIE of polymer.
    - The previous step leaves a teflon-like polymer which gives good SiN:Si selectivity, but must be removed for further processing.
    - Use the same process parameters as with Step 9, the RIE of the ARC, except do the run for 5 minutes.
    - A longer than 5 minute RIE step etches into the silicon, so piranha is used to complete the removal of the polymer.

12. Piranha
    - 3 parts sulfuric acid:1 part hydrogen peroxide.
    - Use a glass bowl and metal tweezers.
    - Gets very hot and steams; be careful and put near a vent in the hood.
    - Place sample in bowl before adding chemicals.
    - Remove with care and rinse with water.

13. Etch Cr.
    - Dip sample in Cr Photomask Etchant (Cyanotek Corp.) for 1 minute.
    - Rinse in DI water.

14. KOH etch of silicon.
    - With a scale, measure 10 gm of KOH chips (Mallinckrodt). Add 190 ml of DI water to the KOH chips in a glass bowl. (5% KOH by weight) Put in magnetic bar, and stir.
    - Pour buffered HF (Transene) into a teflon bowl.
    - Fill a large glass bowl with DI water in sink for rinsing.
    - Dip sample in buffered HF.
    - Rinse in DI water bath.
    - Put sample in KOH solution for 1 minute. Agitate sample with teflon tweezers to shake bubbles from the sample. If the sample doesn't emit small bubbles, the polymer was not completely removed in Steps 11 and 12.
    - Rinse in DI water bath.
    - SEM sample to ensure that some etching has taken place and to calculate how much longer to KOH etch. Repeat Step 14 to complete the etching of the Si.

15. Etch SiN. (May not be desired.)
    - Dip in concentrated HF for 2 minutes, rinse in DI water.

    -OR-

    - Heat Trans Etch N (Hot Phosphoric) to 180?C.
    - Dip sample for 5 minutes.
    - Rinse in DI water.

Appendix B.

Recipe for X-ray Diffraction Gratings

1. In ICL, after an RCA, deposit 300 Å of either stoichiometric or Si-rich silicon nitride (SiN) deposited on silicon wafers. The silicon wafers must be cut so that the (111) plane is at the desired blaze angle with the wafer surface, in this case 0.7° (Chapter 5)

2. In TRL, spin 4900 Å of Brewer XL ARC.
   - Spin at 6 krpm.
   - Bake at 180°C for 30 min.

3. In TRL, evaporate 400 Å of silicon dioxide in the planetary evaporator.

4. In TRL, clean wafers with UV/ozone, deposit HMDS, and spin 2000 Å of PFI-34 Sumitomo resist.
   - Consult spin curve to determine spin speed.
   - Bake at 90°C for 30 min.

5. In SML, Expose 1.7μm period gratings with interferometric lithography.
   - Align so that lines of constructive interference are perpendicular to the flat (Chapter 5).
   - Greatly overexpose to achieve a 1:10 line:space ratio.
   - 250 mJ has been an appropriate dose.
   - Track develop.
   - Several wafers with doses near 250 mJ should be exposed, developed, and SEM'ed to determine the correct dose.

6. In SML, reactive ion etch (RIE) the silicon dioxide.
   - CF4 15 sccm.
   - Chamber 2.
   - Set DC to 300 V.
   - Chamber Pressure 10 mTorr.
   - Temperature 20°C.
   - A run time of 2 minutes is sufficient.

7. In SML, RIE the ARC.
   - O2 45 sccm.
   - Chamber 1.
   - Set Power to 110 W.
   - Chamber Pressure 1.4 mTorr.
   - Temperature 20°C.
   - Over 10 minutes typical; use end point detection.

8. In SML, RIE the silicon nitride.
   - CF4 15 sccm.
   - Chamber 2.
   - Set DC to 300 V.
   - Chamber Pressure 10 mTorr.
   - Temperature 20°C.
   - A run time of 2 minutes is sufficient.

9. In NSL, RCA clean.

10. In NSL, RIE the polymer.
   - O2 5 sccm.
   - He 10 sccm.
   - Set DC to 250 V.
   - Set Reflected Power to 0 W.
   - Chamber Pressure 7 mTorr.
   - Temperature 20°C.
   - Ignition Pressure 35 mTorr.
   - Ignition run time 5 s.
   - A run time of 15 minutes is sufficient.

11. KOH etch of silicon.
   - With a scale, measure 80 gm of KOH chips (Mallinckrodt). Add 420 ml of DI water to the KOH chips in a glass bowl. (20% KOH by weight) Put in magnetic bar, and stir.
   - Pour buffered HF (Transene) into a teflon bowl.
   - Fill a large glass bowl with DI water in sink for rinsing.
   - Dip sample in buffered HF.
   - Rinse in DI water bath.
   - Put sample in KOH solution for ~10 minutes. Agitate sample with teflon tweezers to shake bubbles from the sample. The width of the silicon nub beneath the nitride can be viewed in the SEM to ensure that the etch is complete.
   - Rinse in DI water bath.

12. Evaporate 300Å of chromium.
   - 300 Å, with atom beam normally incident to wafer.

13. HF etch (liftoff).
   - The chromium can be seen to liftoff with the naked eye.

14. In NSL, RIE silicon.
    - CF4 15 sccm.
    - Set Power to 180W.
    - Set Reflected Power to 0 W.
    - Chamber Pressure 10 mTorr.
    - Temperature 20°C.
    - Ignition Pressure 35 mTorr.
    - Ignition run time 5 s.
    - A run time of 10 minutes is sufficient.

15. Chromium Etch.
    - Dip sample in Cr Photomask Etchant (Cyanotek Corp.) for 1 minute. Rinse in DI water.

16. Evaporate chromium and gold.
    - 50 Å of Cr.
    - 200 Å of Au.

Appendix C.

Measurement of Anisotropically Etched Grating Efficiency

Professor Kahn's group from Columbia University and Dr. Gullikson from Lawrence Berkeley Laboratories made measurements of the efficiencies of the anisotropically etched X-ray diffraction gratings (Chapter 4 and 5).

Professor Kahn's group measured the efficiency of the 0, -1, and -2 orders, varying incident angle, and with Al K (8.34 Å), and Cu L (13.34 Å) radiation (Figure C.1 and Figure C.2). For Al K (8.34 Å), the maximum efficiency in the -1 order was ~20%. In ruled gratings this figure is 14.7% and 10% for masters and replicas, respectively. For Cu L (13.34 Å), the maximum efficiency in the -1 order was ~24%. In ruled gratings the maximum efficiency is 20% and 13% for master and replica gratings, respectively.

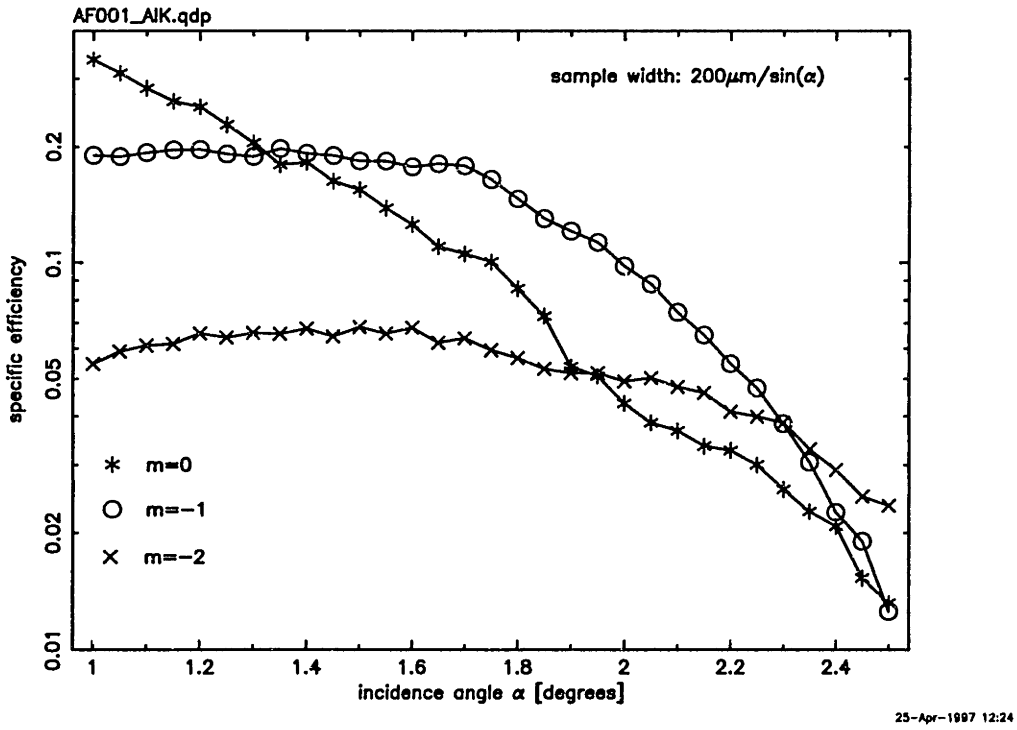


Figure C.1 Diffraction efficiency vs. incident angle from anisotropically etched grating at Al K (8.34 Å).

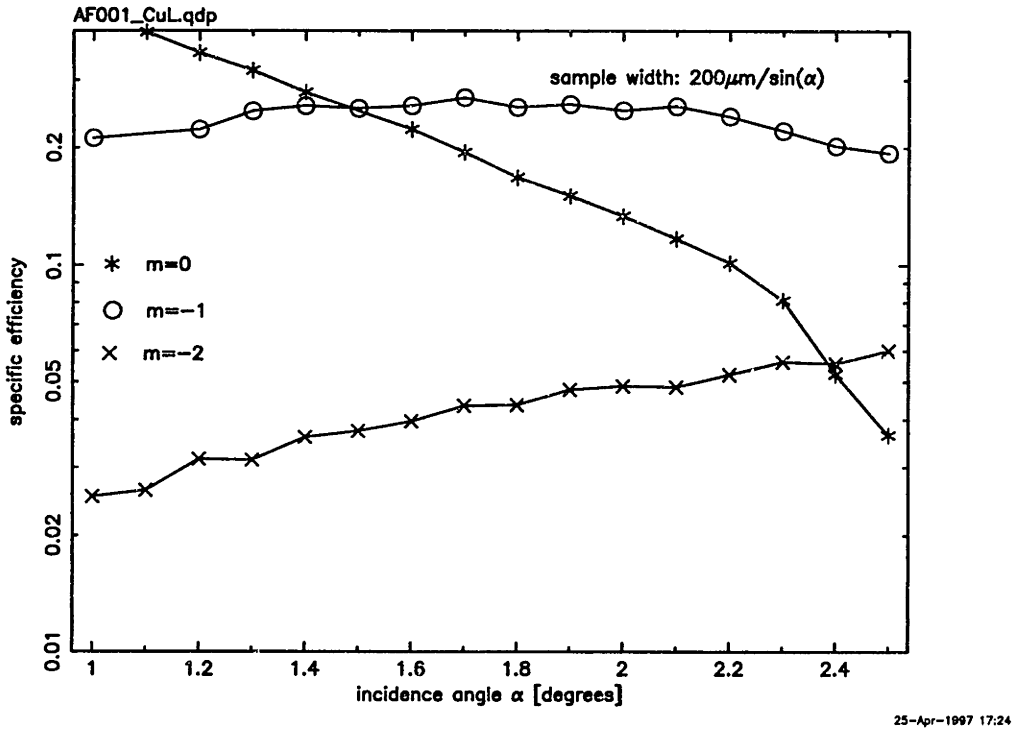


Figure C.2 Diffraction efficiency vs. incident angle from anisotropically etched grating at Cu L (13.34 Å).

Dr. Gullikson rotated the sample keeping the detector position and incident beam fixed. Figure C.3 shows a representative plot of measurements of the anisotropically etched (MIT) and a ruled (Hitachi) gratings. Also, the first order efficiency for fixed diffraction angles of 6° and 8°, with varying photon energies was measured (Figure C.4).

Further analysis of the data collected by these to groups will be presented in a future paper by Kahn and Gullikson.

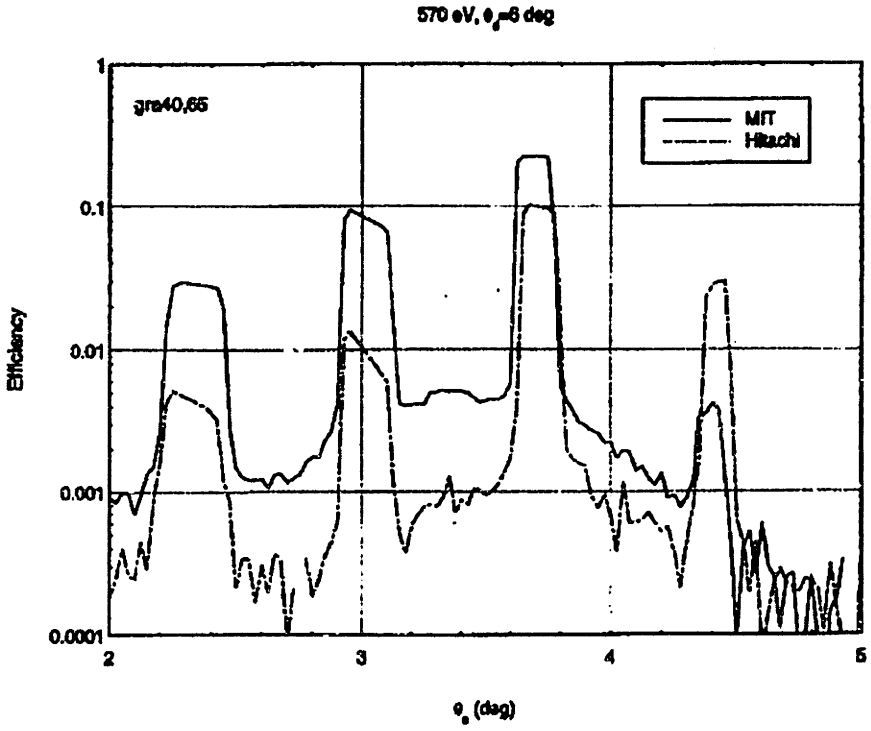


Figure C.3 Diffraction efficiency vs. incident angle for a fixed diffraction angle and photon energy. Several orders can be seen. The Hitachi grating was ruled.

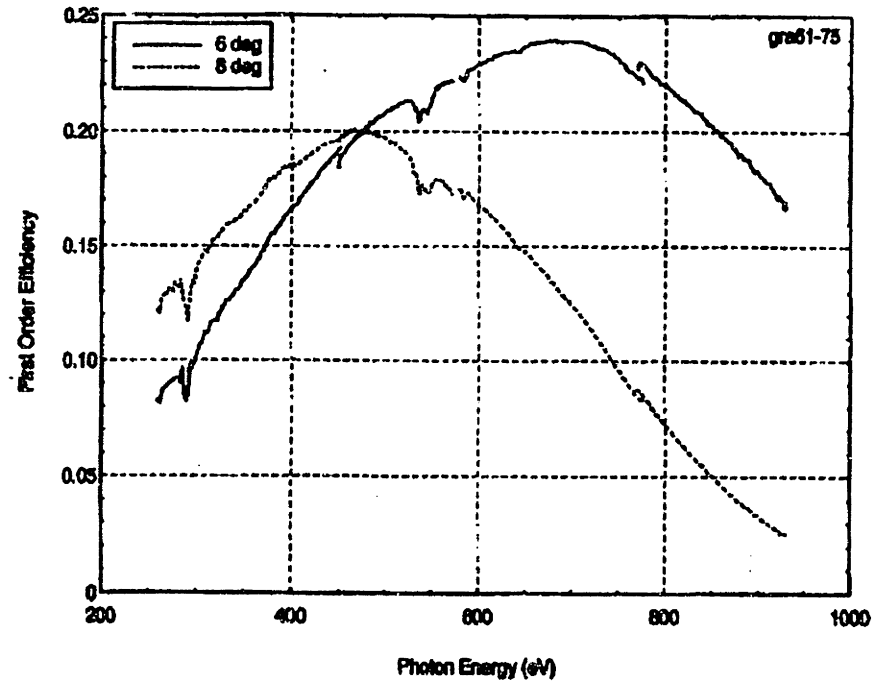


Figure C.4 First order efficiency of anisotropically etched grating vs. photon energy for fixed diffraction angles of 6° and 8°.