A Switching Ripple Based Current Sharing Control System for Cellular Converters

by

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Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 1997

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Abstract

Power conversion systems sometimes comprise a large number of parallel converters, or cells. Due to mass production of cellular converters and parallel operation, the cellular converter system is expected to offer high reliability and performance at low cost. However, severe current imbalances can occur among converters connected in parallel. Such imbalances can increase converter stresses and losses, and dramatically reduce the reliability of a parallel converter system. To overcome the imbalance problem, current-sharing techniques are often employed to force the converter cells to share the load current equally. This thesis develops a new current-sharing method for paralleled converters. Unlike conventional current-sharing methods, the new approach does not require additional interconnections for communicating current-sharing information. Instead, information for current-sharing control is communicated via the output voltage ripple. The advantage of this method is that the systems can be made more reliable and can be more easily implemented than in conventional methods due to the lack of interconnections for control. In this research, we implement and experimentally evaluate the current-sharing approach.

Thesis Supervisor: John G. Kassakian
Title: Professor of Electrical Engineering and Computer Science

Acknowledgments

I have many people to thank for their help in the completion of this thesis. First of all, I would like to sincerely thank Professor Kassakian for his guidance, enthusiasm, and encouragement during my two years at MIT. I appreciate not only his academic comments and suggestions throughout the development of my thesis but also his leadership on the 150-mile bike tour to Cape Cod, which was one of my most impressive experiences in the Laboratory for Electromagnetic and Electric Systems (LEES).

I also express my gratitude to David Perreault for working with me. He spent much time giving me his continued assistance through my work on my thesis research. His patience and willingness to answer my questions and explain things more than once have been greatly appreciated, but I have learned even more from his enthusiastic attitude towards our research.

I extend appreciation to everyone for sharing time in LEES. Philip, Yanqing, Mary and Julio, thanks for your friendship and support. I also thank Vahe and Khurram for their suggestions and discussions. Tim, Daline and Scott, thank you for encouraging me. I also would like to express my gratitude to Ms. Mizuno, secretary, who helped and advised me kindly.

I wish to thank all the friends that I have made here at MIT, who have helped to make the past two years such a pleasant experience. Special thanks for three wonderful roommates, Rava, Arturo and Leoneid.

Profound thanks to Ms. Baty, coordinator of the International Student Office, who introduced me to my great host family, Mr. and Mrs. Forbes. Their support made my life more fulfilling .

Additionally, I acknowledge Central Japan Railway Company for affording me the opportunity to study at MIT for two years.

Finally and most importantly, I am very thankful to my parents and brother for their unwavering love and support.

To my parents and brother

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Chapter 1

Introduction

1.1 Background

Recently, due to the development of high power devices, power conversion systems have been integrated into society. The wide use of such systems requires reliable, stable performance at low cost. The cellular converter architecture is expected to meet these demands by utilizing the parallel operation of many converter cells [1]. A cellular converter is comprised of a large number of quasi-autonomous converter cells operating in parallel as shown in Fig. 1-1. Each cell is itself a complete power converter including some level of control. Compared to conventionally designed and constructed converters, advantages of the cellular approach include improvements in performance and reliability, and reductions in cost.

A necessary characteristic of a cellular converter system is that the individual converter cells share the load current equally. Unfortunately, without control, severe current imbalances can occur among cells connected in parallel. Such imbalances can increase system stresses and losses, and dramatically reduce the reliability of the system. To overcome the imbalances of output current among cells, current-sharing methodologies have been developed. They can be categorized as follows:

Centralized control method [2-4] This system has a supervisory processing unit that ensures current balance among cells. This method allows large capacity to

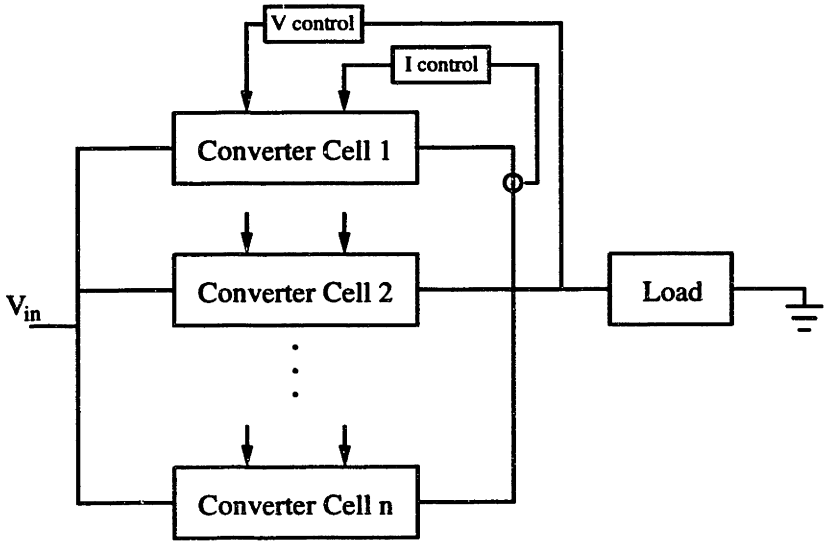

Figure 1-1: A Cellular Converter Architecture Supplying a Single Load.

be achieved by paralleling cell operation; however, the system reliability fully depends on the robustness of the supervisory processing unit. In other words, if the supervisory processing unit fails, the whole system will break down.

Output droop current-sharing method This method is simple to implement, and it does not require any interconnections among the paralleled cells. However, the major deficiency of the droop method is a poor regulation characteristic. Therefore, the droop method is not suitable for applications that require tight regulation [5-7]. Variations of this approach exist for ac supply systems, in which droops in output voltage and frequency are used to control real and active power balance [8, 9].

Active current-sharing method with a single interconnection wire To ensure acceptable current sharing among paralleled converter cells, active current-sharing techniques are often employed. In single-wire current-sharing methods, the cells exchange information about their output currents over a single-wire interconnection [10-14]. Typically, the current-sharing circuit is designed such that each cell generates a voltage proportional to its output current, and the

voltage on the single wire is proportional to the average [10, 11, 13], maximum [12], or other function of the individual voltages. This information can then be used by individual cells to achieve current sharing, by adjusting either the local converter reference voltage [10, 12] or output current [13, 14].

While the single-wire interconnection approach to current sharing is simple and effective, the direct interconnection among the cell control circuits in conventional schemes is a potential source of single-point failure mechanisms, which can limit the reliability of the system. To overcome the interconnection problem, a current-sharing approach that does not require interconnections among cells was proposed in [15].

In the *output perturbation* method of current-sharing control, each cell adds a small perturbation, with a frequency related to the output current, onto its output current. The aggregate perturbation in the output voltage is accessible to all of the cells. Each cell then uses the information contained in the common output voltage perturbation to adjust its own output and achieve current sharing. This method was proposed in [15] and developed in [15-17].

The *switching ripple* method of current-sharing control operates in a similar manner, but instead of injecting additional perturbations, the switching ripple method uses the cell-switching ripple as the perturbation source. The converter cells are controlled such that their switching frequency varies with output current. The output voltage ripple, therefore, contains information about the output currents of the individual cells. This information can be used by the cells to enforce current-sharing. The advantage of this approach over the perturbation method is that it does not require additional output perturbations to achieve current-sharing. Furthermore, the current-sharing information is communicated with high bandwidth (i.e., at the switching frequency).

The switching ripple method was originally proposed in [15], but not developed. Implementation of this method was explored in [16]. However, that implementation approach required the use of a complex frequency estimator circuit that was extremely noise sensitive. Due to the limitations of the estimator, the implementation was deemed impractical.

In this thesis, I propose to develop an implementation of the switching ripple current-sharing method that is both simple and robust. This new implementation method operates by having each cell detect the ripple voltage due to other cell(s) operating at a lower switching frequency than its own. If the switching frequency of each cell varies inversely with its output current, this is equivalent to detecting the existence of cells operating at a higher current level. To achieve current sharing, each cell adjusts itself such that no other cell is operating at a significantly lower switching frequency (or higher current). Because this approach relies only on a cell detecting the existence of switching frequencies lower than its own, it is simple to implement and insensitive to the harmonic content of the switching ripple. Through simulation, analysis and experimentation, we investigate this novel method and confirm its practicality.

1.2 Organization of Thesis

This thesis develops a novel current-sharing method for cellular converters, termed *switching ripple based current sharing.* First, we demonstrate the concept of this current-sharing method via simulation. Then, based on the analytical investigation, a prototype system is developed. Finally, we discuss the experimental results and evaluate this method.

In Chapter 2, we explain the concept of this current-sharing method. A Simulink simulation model is developed for a two-cell buck converter system using this current-sharing control method. Simulations using this method are used to demonstrate the control structure.

Chapter 3 focuses on the implementation of this method. A three-cell buck converter implementing this current-sharing control method is developed. The circuitry used to implement the system is presented and explained.

The experimental evaluation of this current-sharing control method follows in Chapter 4. This chapter discusses the static current-sharing test, the load regulation test, the transient current-sharing test and the load step test. Finally, Chapter 5

presents conclusions and recommendations for future work.

Chapter 2

The Switching Ripple Based Method of Current-Sharing Control

When power converter cells operate in parallel, severe current imbalances and circulating currents can occur among them. These effects increase system stresses and losses, and can dramatically reduce the reliability of the system. To eliminate these effects, active current-sharing control is often employed [2]. The implementation of active current-sharing control requires that the converters exchange information about their output currents. Current-sharing information is most commonly communicated across a single-wire interconnection from cell to cell [3, 10, 12] . However, the single-wire interconnection can be the source of single-point failures, a problem that limits the reliability of the system. Thus, methods that do not require additional interconnections among cells have been developed to overcome the interconnection problem [15-17].

This chapter proposes the *switching ripple based method of current-sharing control*, which does not require additional interconnections among cells. First, we discuss the concept of this approach in Section 2.1. Then, to illustrate the method, Section 2.2 presents the simulation of a two cell buck converter system using this method of current-sharing control.

2.1 Concept of the Switching Ripple Based Method

The switching ripple method proposed in this thesis is based on the use of information contained in the switching ripple on the output voltage to implement current-sharing control. It can be applied to any type of converter in which the switching frequency varies monotonically with output current, as illustrated in Fig. 2-1.

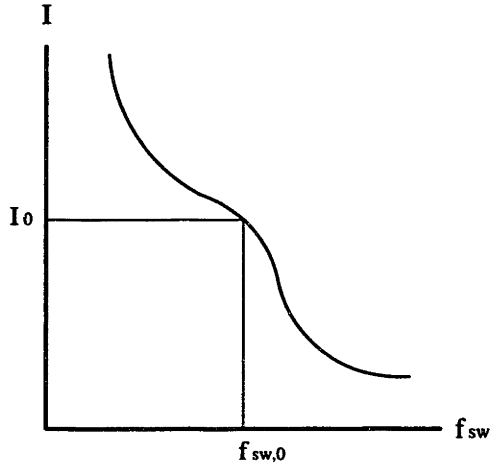

Figure 2-1: An example of a monotonic relation between switching frequency and output current.

In the figure, the line corresponding to some average output current I_0 intersects with the characteristic curve at one point, $f_{sw,0}$. This relation between output current and frequency ensures that the cell's current can be determined from its switching frequency. Since the switching frequency content of all the cells appears as an aggregate switching ripple on the output voltage, each cell can pick up information about other cell currents from the output voltage ripple without using an additional interconnection wire. Using information about cell switching frequencies determined from the switching ripple, each cell controls its own output current such that no other converter operates at a lower switching frequency than its own. As a result, all the cells' switching frequencies and output currents converge to a single value, and current sharing is achieved.

This approach has several advantages. First, because it relies only on each cell detecting the existence of switching frequencies lower than its own, the approach is

simple to implement and is unaffected by the harmonic content of the switching ripple. Second, since the current-sharing controllers operate independently, the system is robust against breakdown. Even if some cells in the system fail, the remaining cells still share current. Third, this approach can be applied to any kind of converter with a monotonic relation between switching frequency and average output current. Even converters that do not normally exhibit such a relation can often be caused to do so. For instance, this can be achieved in the case of clocked PWM converters by adjusting the clock frequency and PWM ramp slope as a function of output current.

2.2 A Simulation Example

To illustrate the concept of the switching-ripple-based method, this section presents the simulation of a two-cell buck converter system using this current-sharing approach.

2.2.1 Example System Power Stage

As an example, we adopt two parallel buck converters working at the edge of discontinuous conduction. Figure 2-2 shows the circuit schematic of the system.

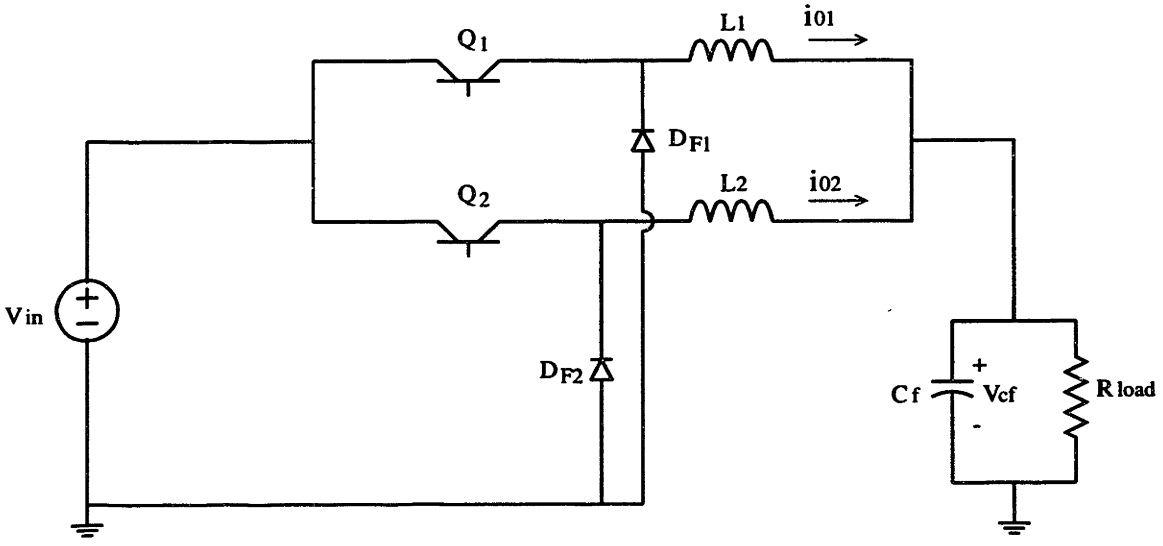

Figure 2-2: Circuit schematic of basic buck converter.

Figure 2-3 illustrates the waveform of output current for a cell. In this circuit, the

transistors, Q_1 and Q_2, are turned on until their output current, i_{01} and i_{02}, reach two times output current reference, $2i_{\text{ref}}$, and then they are turned off until i_{01} and i_{02} return to zero. This operation yields triangular output current wave form, in which its average current is equal to i_{ref}. Therefore, for convenience, we can regard i_{ref} as the average output current. The switching period of the k^{th} cell, T_{k}, can be expressed in terms of the circuit parameters as:

$$T_{\text{k}} = \frac{V_{\text{in}} L(2i_{\text{ref,k}})}{V_{\text{cf}}(V_{\text{in}} - V_{\text{cf}})}. \tag{2.1}$$

Thus, each converter cell operates at a switching frequency that is inversely proportional to its output current:

$$f_{\text{sw,k}} = \frac{C}{i_{\text{ref,k}}} \tag{2.2}$$

where C is a constant.

Equation 2.2 expresses the fact that the higher the output current of a cell, the lower the switching frequency of the cell. Moreover, because each triangular current waveform produces a switching ripple in the output voltage, the output voltage ripple contains the switching frequencies of both cells. Consequently, we can get information about the individual cell currents from the aggregate voltage ripple frequency content.

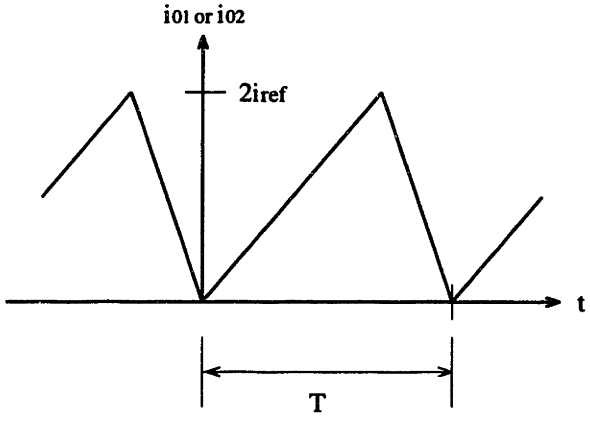

Figure 2-3: Waveform of output current i_{01} or i_{02} for the circuit of Fig. 2-2.

2.2.2 Example System Control Structure

The structure of the control system for the two-cell buck converters shown in Fig. 2-4.

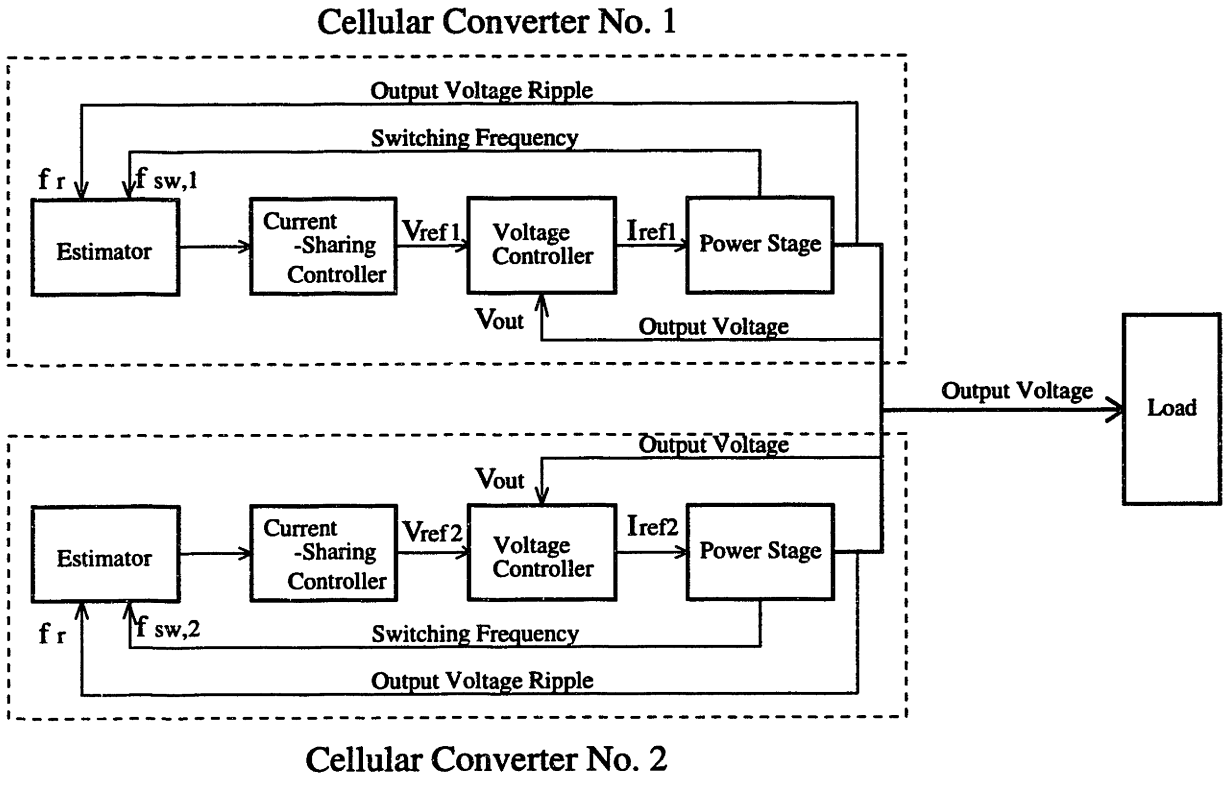

Figure 2-4: Control system for the two-cell buck converter of Fig. 2-2.

Each cell has an inner current control loop and a voltage control loop. The current control loop maintains an average output current of $i_{\text{ref,k}}$, as described in the previous section. The reference current is generated by a middle voltage control loop, which compares the output voltage, V_{out}, to the local cell reference voltage, $V_{\text{ref,k}}$. To maintain current balance, each cell has a slow outer current-sharing control loop, which adjusts the local cell reference voltage about a base value. The current-sharing control loop is composed of a frequency estimator and current-sharing controller. The frequency estimator compares the switching frequency in the local cell to the aggregate frequency of voltage ripple, which is the superposition of the two cells' switching frequencies. The estimator detects the existence of other cells operating at

a lower frequency (or equivalently a higher output current). Using this information, the current-sharing controller modifies the local voltage reference of the cell for the purpose of equalizing the cell's current. If a cell detects that other cells are operating at a higher current (lower frequency), it can increase its own reference voltage (within bounds) and thereby increase its own current. The procedure for adjusting the voltage reference can be expressed by the following equation:

$$\frac{dV_{\mathrm{ref,j}}}{dt} = \begin{cases} K_{\mathrm{j}}[i_{\max} - \Delta I - i_{\mathrm{j}}] & \text{for } V_{\mathrm{ref,j,base}} < V_{\mathrm{ref,f}} < V_{\mathrm{ref,j,max}} \\ 0 & \text{Otherwise} \end{cases} \tag{2.3}$$

where K_{j} and i_{j} are the integral control gain and output current of the j^{th} cell, $i_{\max}$ is the maximum output current of all of the cells, and ΔI is a small offset. In other words, utilizing the aggregate output voltage ripple on the common output voltage line, each cell shifts its reference voltage and output current towards the maximum one to make all cell output currents balance.

2.2.3 Simulink Simulation Model

Figure 2-5 shows the Simulink diagram simulating the converter of Fig. 2-2 with the control system of Fig. 2-4. As discussed in the previous section, the system consists of estimators, current-sharing controllers, voltage controllers and power stages for two cells. Figures 2-6 through 2-9 show the internal structure of some of these subsystems.

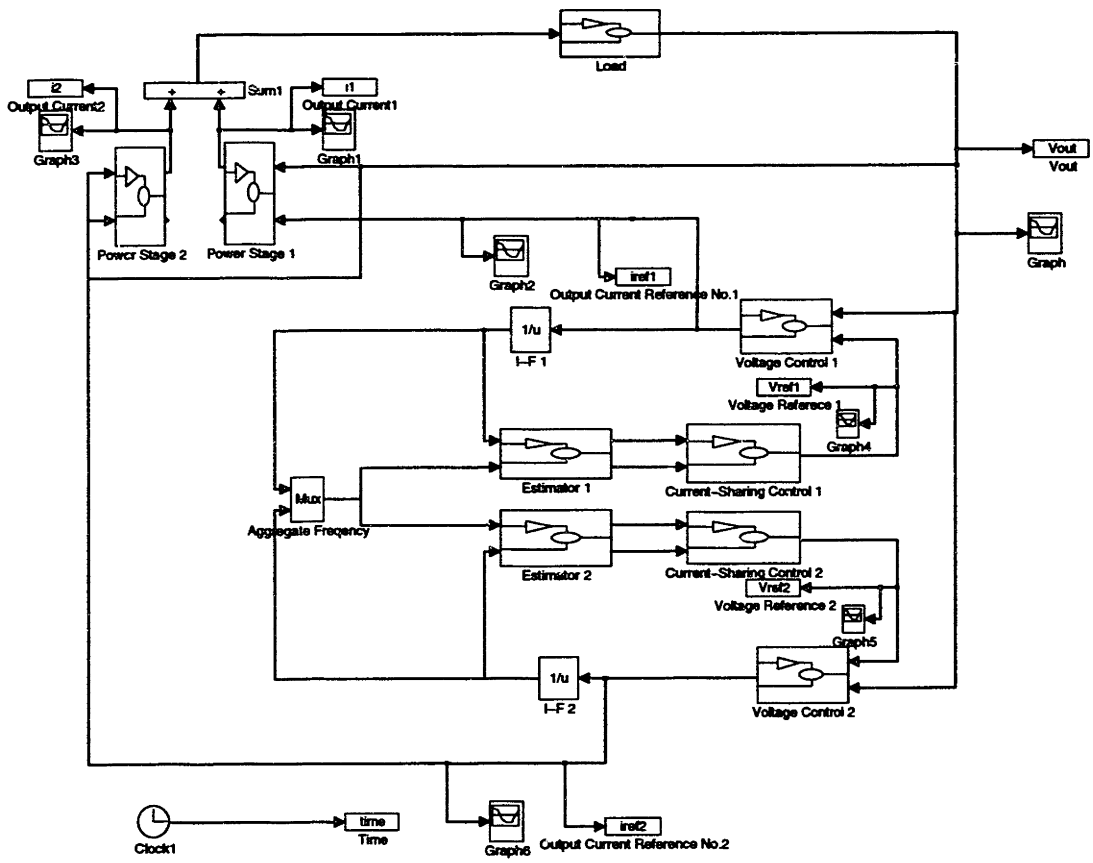

Figure 2-5: Simulation diagram of the two-cell buck converters with switching ripple based current sharing control.

In the simulation, the switching frequency of the cell is associated with its output current reference, which is equal to its average output current. To model aggregation of the switching ripple on the common output voltage that occurs in a practical circuit, the simulation combines the two converters' switching frequencies to form a vector. The estimator extracts the lowest frequency component from the aggregated switching ripple, effectively identifying the highest cell current as shown in Fig 2-6.

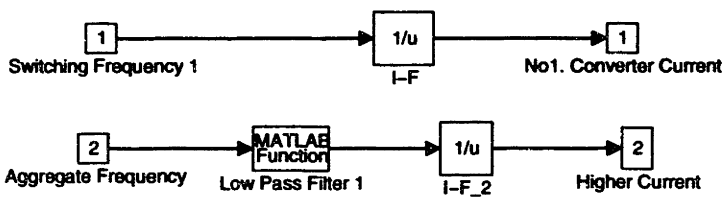

Figure 2-6: Internal structure of the the estimator of Fig. 2-5

Using the lowest switching frequency derived by the estimator and its own switching frequency, the current-sharing controller adjusts the voltage reference of the cell. The current-sharing controller of this simulation is shown in Fig 2-7. If the cell's own switching frequency is higher than the other's, the current-sharing controller increases the cell's voltage reference (within limits) to drop its switching frequency so that its output current increases to meet that of the other cell. The current-sharing control is achieved by integral control on a slower time scale than the voltage loop control.

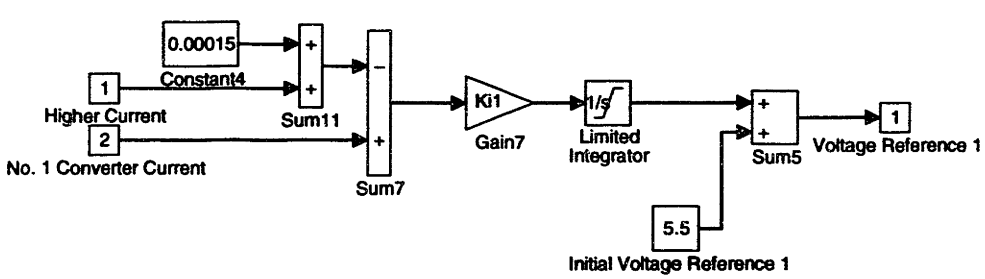

Figure 2-7: Internal structure of the current-sharing controller of Fig. 2-5.

Based on the adjusted output voltage reference, the voltage controller derives an output current reference from the output voltage and the voltage reference. To obtain fast response and low steady-state error, we adopt a lag compensation for the voltage loop. Figure 2-8 shows the internal structure of the voltage controller.

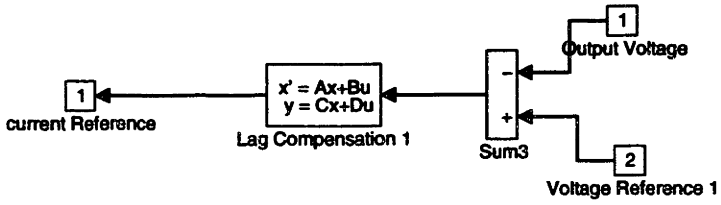

Figure 2-8: Internal structure of the voltage controller of Fig. 2-5.

The cell output current reference is fed to the power stage shown in Fig. 2-9. The power stage operates as previously described – the switch is turned on until the output current reaches twice the output current reference and is turned off until the current reaches zero.

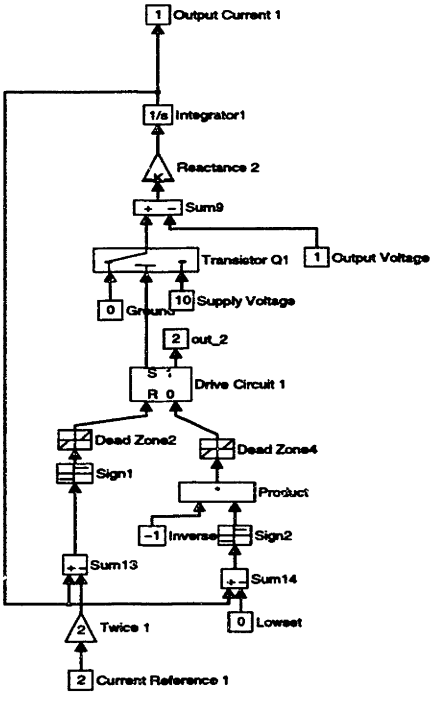

Figure 2-9: Internal structure of the power stage of Fig. 2-5.

2.3 Simulation Results

Figure 2-10 shows output voltage and voltage references of both converters, under current-sharing control, with initial condition I_{ref1}, I_{ref2}, V_{out}, V_{ref1}, V_{ref2} set as 3.08 mA, 7.88 mA, 5.48 V, 5.50 V and 5.53 V, respectively. The output voltage contains the aggregate switching ripple, whose frequency content is related to the cell output currents. We can also see that the ripple is beating at the beginning because the switching frequencies of the two cells are different.

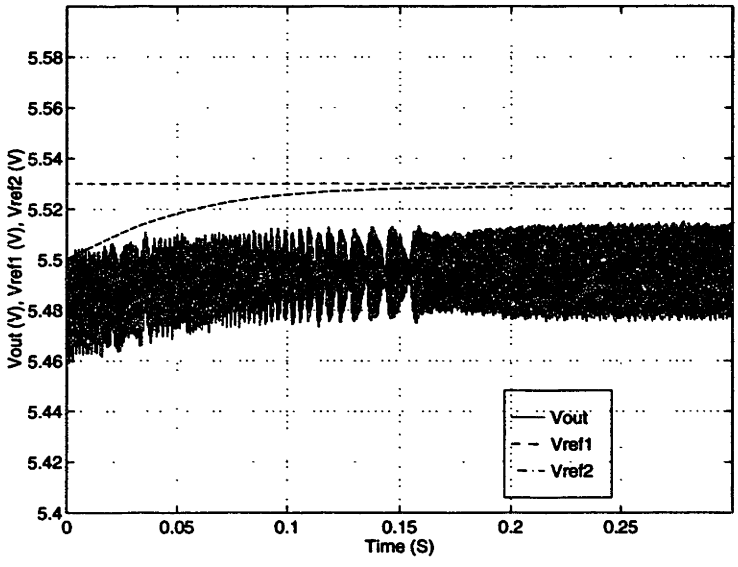

Figure 2-10: Output voltage and voltage references of the converters under current-sharing control.

Figure 2-11 illustrates current references of converters number one and two under current-sharing control. At first, two converters had different voltage references, $V_{ref1} = 5.50V$ and $V_{ref2} = 5.53V$, resulting in unbalanced output current and switching frequencies.

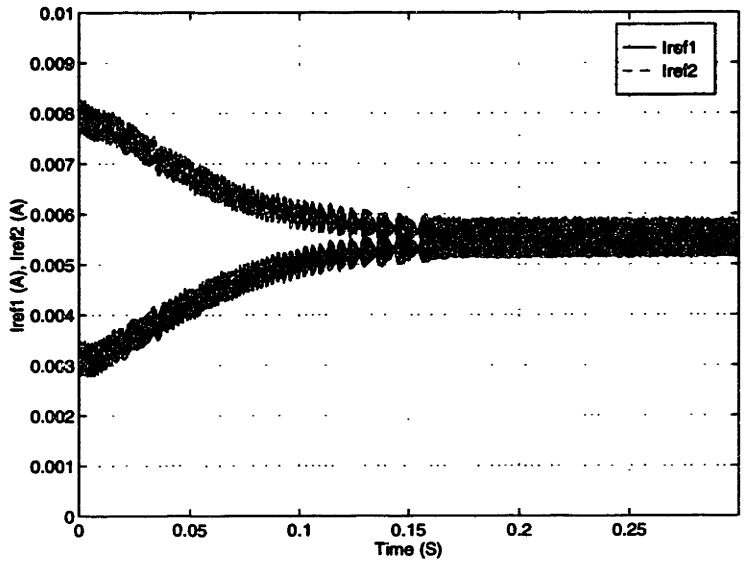

Figure 2-11: Current references of the converters under current-sharing control.

Converter #1's estimator recognized that its own switching frequency was higher than the other cell's and its current-sharing controller started to raise its voltage reference via integral control in response. As converter #1's voltage reference increased, its output current increased and converter #2's current decreased. As a result, the two converters' switching frequencies approached each other as illustrated in Fig. 2-12. Finally, the two output currents and switching frequencies converge on a single value.

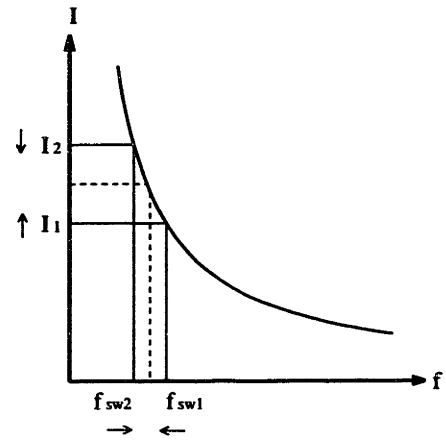

Figure 2-12: Image of output current and switching frequency shifting

Figures 2-13 and 2-14 show the steady-state output currents of both converters with and without current-sharing control.

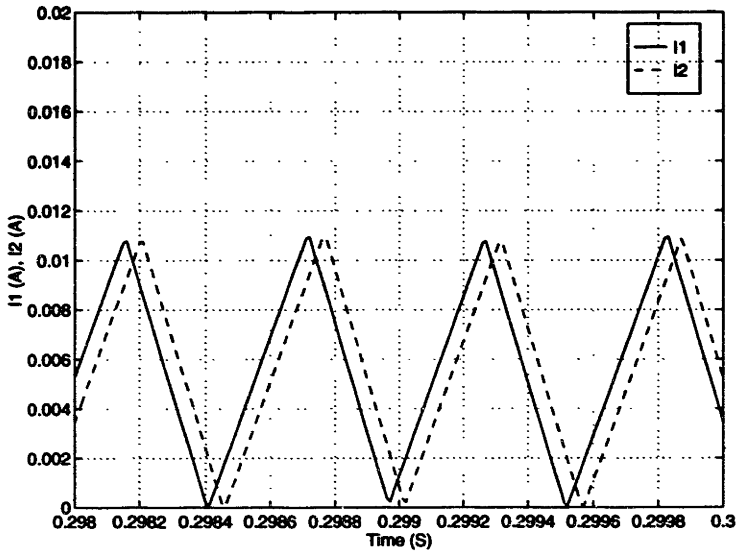

Figure 2-13: Output current of the converters with current-sharing control.

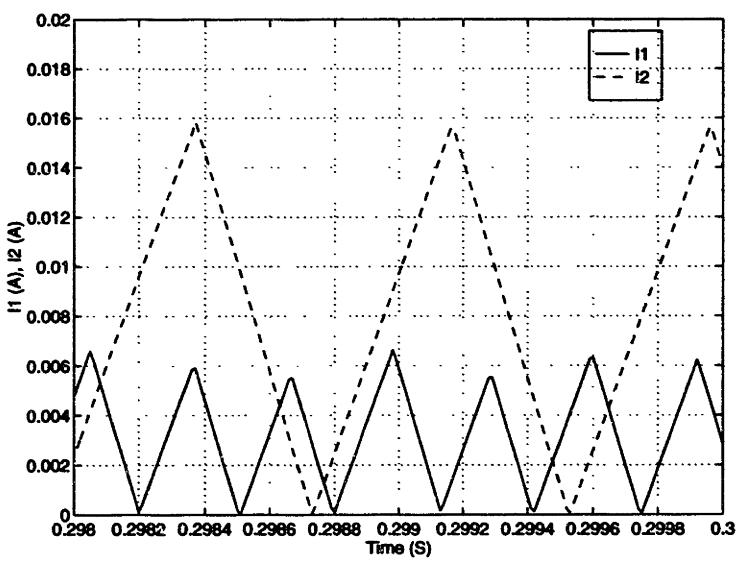

Figure 2-14: Output current of the converters without current-sharing control.

Without current-sharing control, converter #1's current was smaller, and its frequency was higher, than that of converter #2 due to the slight imbalance of the volt-

age reference. In contrast, with current-sharing control, both output currents and switching frequencies are well matched, owing to the current-sharing control action just described. From the simulation results, it can be said that the current-sharing control proposed in this chapter, which is based on encoding the current-sharing information in the switching ripple on the output voltage, eliminates the use of additional current-sharing interconnection among cells.

In this chapter, we proposed the switching ripple based method of current-sharing control. Then, by using Simulink simulation, we also demonstrated the operation of this current-sharing approach in the two paralleled buck converters. As a next step, based on the theoretical investigation conducted in this chapter, we will focus on the implementation of a prototype circuit realizing this current-sharing approach.

Chapter 3

Implementation of the Switching Ripple Based Method

In Chapter 2, we proposed the switching ripple based method of current-sharing control and demonstrated it through simulation. This chapter describes the design of a prototype converter system that implements the switching ripple based method. Section 3.1 introduces the structure of a cell implementing this control method. The following sections describe the cell subsystems one by one. Section 3.2 presents the estimator, which extracts current-sharing information from the output voltage ripple. The current-sharing controller is discussed in Section 3.3, and a description of the voltage controller follows in Section 3.4. Finally, Section 3.5 describes the power stage circuit.

3.1 Structure of the Prototype System

Figure 3-1 shows a diagram of the three-cell buck converter system. Each cell comprises a current-controlled power stage, a voltage controller, a current-sharing controller and a frequency estimator. The individual buck converter cells are designed to convert from 10 V to 5 V over a 1-10 mA load range.

The function of each subsystem is the same as previously discussed in Chapter 2. The estimator uses information in the output voltage ripple to detect the existence of

other cell(s) operating at a higher current. Using the information from the estimator, the current-sharing circuit adjusts the voltage reference such that there are no other cells supplying higher current than its own.

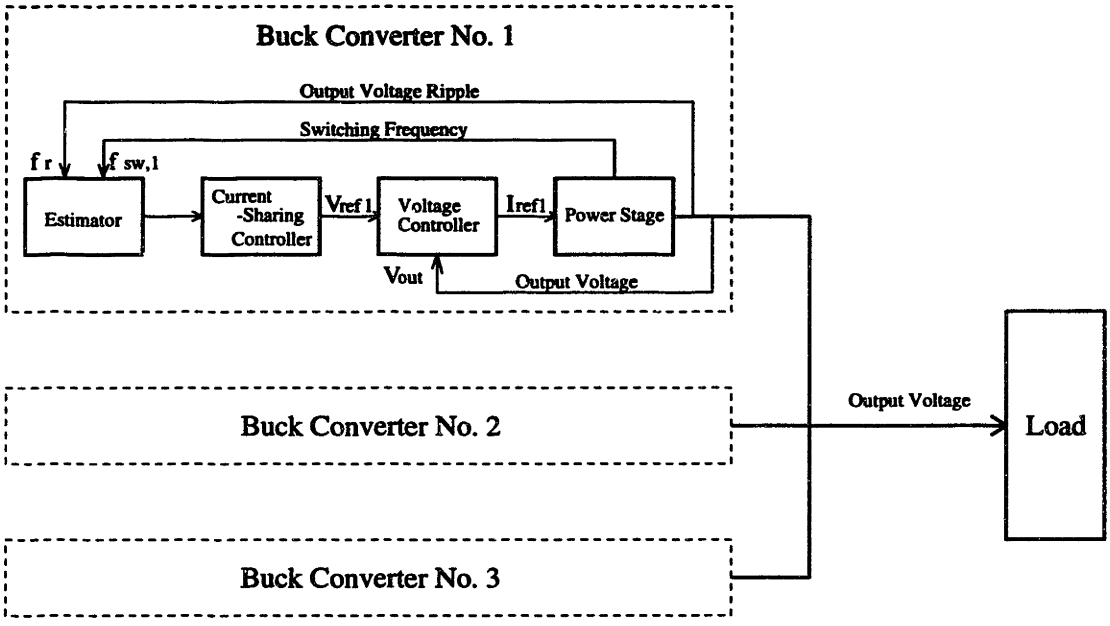

Figure 3-1: System diagram of the three-cell buck converter system.

Based on the voltage reference from the current-sharing circuit, the voltage controller generates the output current reference. The power stage circuit supplies an output current to the load that follows the output current reference.

3.2 Frequency Estimator

The estimator, shown in Fig. 3-2, consists of three parts, a pre-filter stage, a tracking filter stage and an rms-to-dc converter stage. The pre-filter is a bandpass filter, which extracts the aggregate switching ripple components from the output voltage. The tracking filter is a high-pass filter, whose cutoff frequency tracks to 0.8 times local switching frequency. Thus, the tracking filter passes only those ripple components at frequencies of the local cell and above. Then, the rms-to-dc converter stage computes the rms of the signals before and after the tracking filter. The function of the estimator is to detect the existence of other cell(s) operating at a higher current. The estimator operates in the following manner. First, the pre-filter separates out the aggregate switching ripple components from the output voltage. The ripple signal is fed to the tracking filter, which attenuates ripple components with frequencies lower than the cell's own switching frequency. The aggregate switching frequency ripples before and after the tracking filter are converted into dc signals by the rms-to-dc converters. Any deviation of the two dc signal values indicates the existence of one or more cells operating at a lower frequency (higher current) than the local cell.

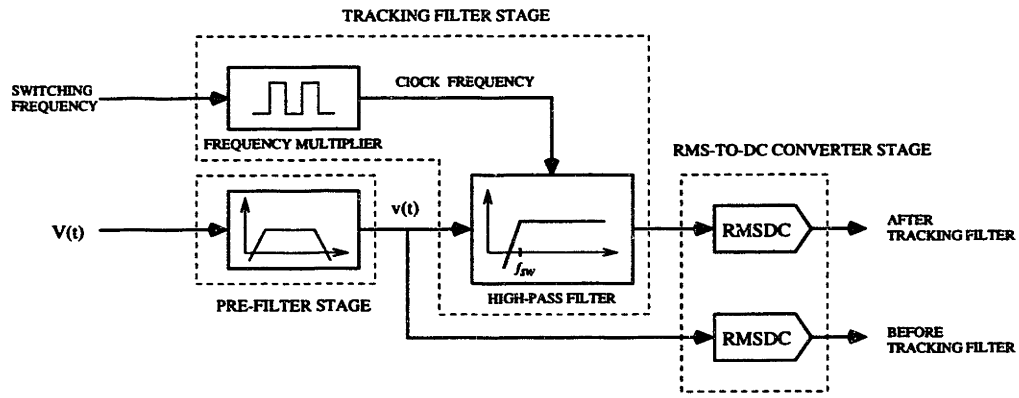

Figure 3-2: Block diagram of the frequency estimator.

3.2.1 Pre-filter Stage

Figure 3-3 shows the schematic of the pre-filter. To isolate the desired ripple frequency components, a band-pass filter is used. The band-pass filter consists of a 2nd order high-pass Butterworth filter ($f_c = 40$ kHz) cascaded with a 2nd order low-pass Butterworth filter ($f_c = 500$ Hz). Because the aggregate voltage ripple is small and its magnitude decreases as an inverse square with frequency components (see Appendix B.1), a frequency-dependent amplifier is implemented after the band-pass filter. The maximum magnitude of aggregate voltage ripple is approximately 75 mV at a switching frequency of 1 kHz in the prototype circuit, while the tracking filter allows a maximum continuous input of 3.8 V. Thus, the frequency-dependent amplifier is designed to implement a gain of 34 at 1 kHz, linearly increasing to 470 at 20 kHz.

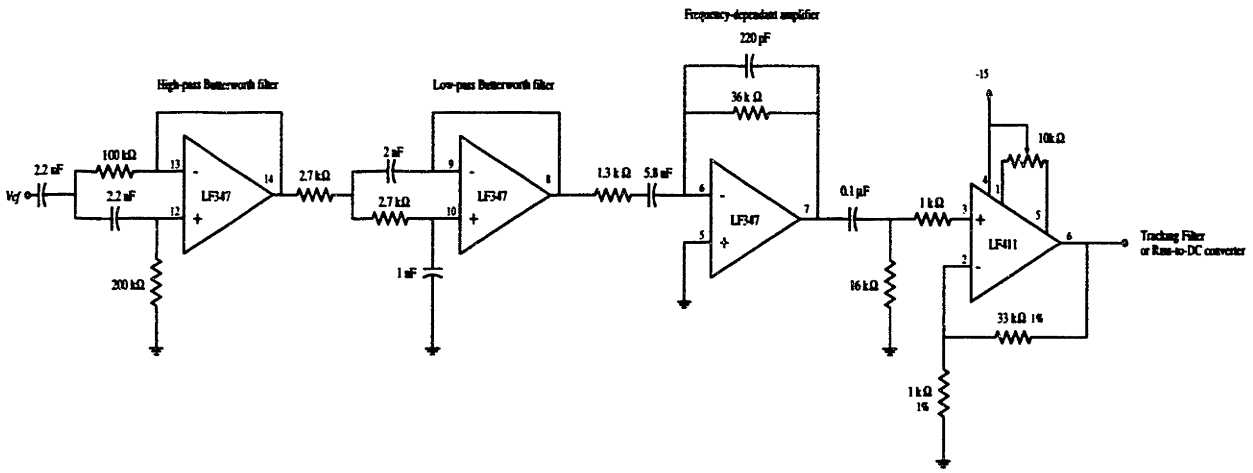

Figure 3-3: Schematic representation pre-filter stage in the frequency estimator.

As illustrated in Fig 3-3, the frequency-dependent amplifier is implemented as the cascade of a band-limited differentiator and a fixed gain of 34. The output of the pre-filter stage is a highly amplified and frequency compensated version of the output voltage ripple.

3.2.2 Tracking Filter Stage

In the tracking filter stage, the aggregate switching ripple from the pre-filter stage is filtered by a high-pass filter whose cutoff frequency tracks 0.8 times the local switching frequency. The tracking filter stage consists of a high-pass filter and a frequency multiplier. The high-pass filter, shown in Fig 3-4, is a fourth-order Butterworth switched-capacitor filter whose cutoff frequency can be controlled by a clock signal. The function of the frequency multiplier is to generate the clock signal for the switched-capacitor filter from the local gate drive signal.

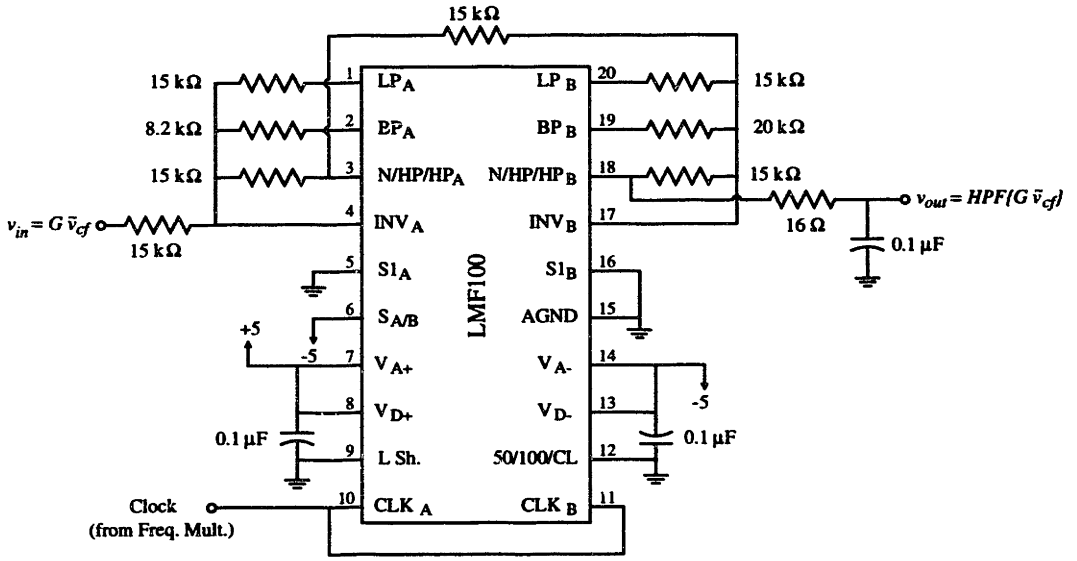

Figure 3-4: Switched-capacitor filter used in the tracking filter.

To implement a variable cutoff frequency, we used the switched-capacitor filter IC, National Semiconductor LMF100, whose cutoff frequency, f_c, is 1/100th of its clock frequency, f_{clk}. The fourth order Butterworth filter is adopted because it does not exhibit peaking in its frequency response near the cutoff frequency and cuts off sufficiently fast for our purposes.

Because a switched capacitor filter is a sampled-data system (operating at the clocking frequency), one must ensure that aliasing does not cause undesired consequences. The clock frequency of the switched capacitor filter is in the range of 80-1600

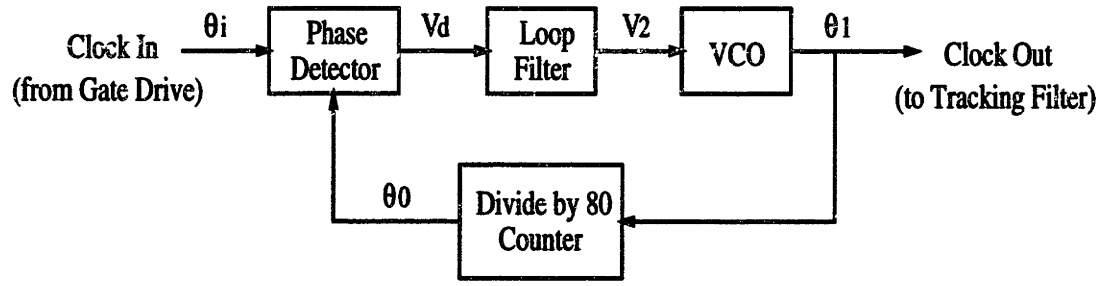

Figure 3-5: Structure of the frequency multiplier.

kHz, so no aliasing of input frequency components occurs below $f_{in} = 40$ kHz. Furthermore, signals at f_{in} that are above $f_{clk}/2$ get aliased to $f_{clk} - f_{in}$. As long as the aliased frequency, $f_{clk} - f_{in}$ is above the filter cutoff $f_{clk}/100$, the aliasing does not affect the circuit performance, since only the total energy at the filter output is used in subsequent processing. For the frequency range in the prototype system, the sampled-data nature of the switching capacitor filter does not affect circuit performance.

The frequency multiplier generates the clock signal for the tracking filter from the local gate drive signal. The clock frequency must be 100 times the desired filter cutoff frequency. As a result, the clock frequency should be 80 times the local cell switching frequency to achieve the desired cutoff performance. As shown in Fig. 3-5, the frequency multiplier consists of a phase detector (PD), a loop filter, a voltage-controlled oscillator (VCO), and a counter.

The PD compares the phase of the local gate drive waveform to the phase of the VCO and generates a phase error signal V_d whose average value depends on the difference in the frequency (and phase) between the local gate drive waveform and the counter output. The phase error is filtered by the low-pass loop filter, and the resulting signal V_2 causes the VCO output frequency (and phase) to change in a direction that reduces V_d. When the circuit is in steady state, the frequency (and phase) of the input clock waveform matches that of the counter output, and the VCO

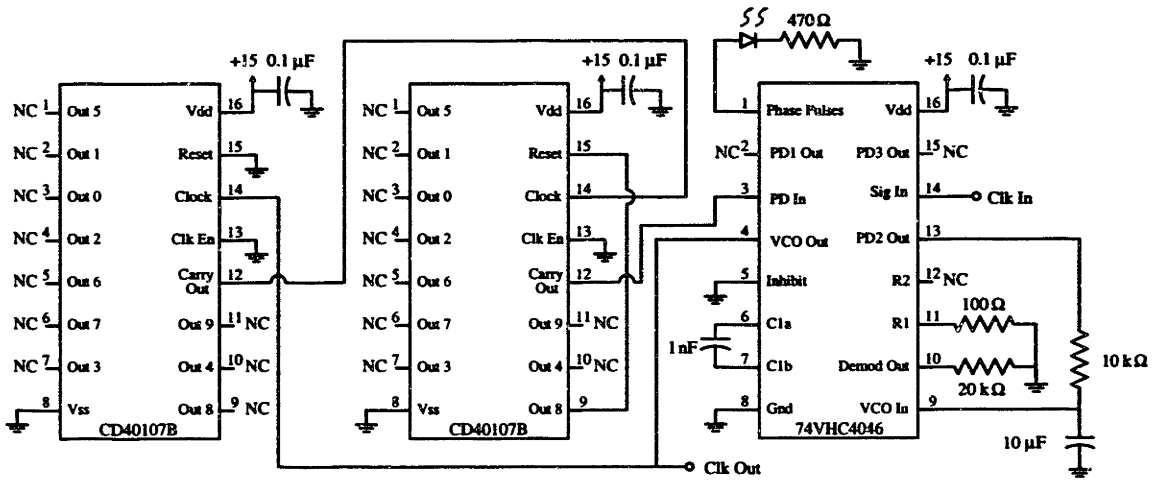

Figure 3-6: Frequency multiplier of the tracking filter stage in the frequency estimator.

output (counter input) is 80 times the local gate drive frequency. Thus, the system acts such that the VCO output frequency is 80 times the local input frequency.

Figure 3-6 shows the schematic of the frequency multiplier. We use the 74VHC4046 phase-locked loop IC and two DC40107B binary counters. R_1 and C_1 of 74VHC4046 are selected such that the VCO center frequency is 1 MHz. The two binary counters act together to divide the VCO output frequency by 80, yielding a divide-by-80 counter. The time constant of the loop filter is set at 0.01 s, which is slow enough to allow the frequency multiplier to track the variations in the switching frequency due to the action of the cell voltage controller.

3.2.3 Rms-to-dc Converter Stage

The rms-to-dc converter stage computes local-time rms values of the switching ripple signals before and after the tracking filter. Analog Devices, AD637, high precision, wideband rms-to-dc converters connected in the two-pole Sallen-Key filter arrangement are used for this purpose [18]. Figure 3-7 shows the schematic of the rms-to-dc converter stage. The averaging time constants of this circuit are designed to be fast enough to track information for the current-sharing loop and slow enough to give good frequency resolution. An analysis of this tradeoff can be found in [15]. We set the averaging and filter capacitor C_{AV}, C_2 and C_3 to be $0.22\mu F$, $0.47\mu F$ and $0.47\mu F$, respectively. This yields a 1% steady-state error and a 1% settling time of 8 ms.

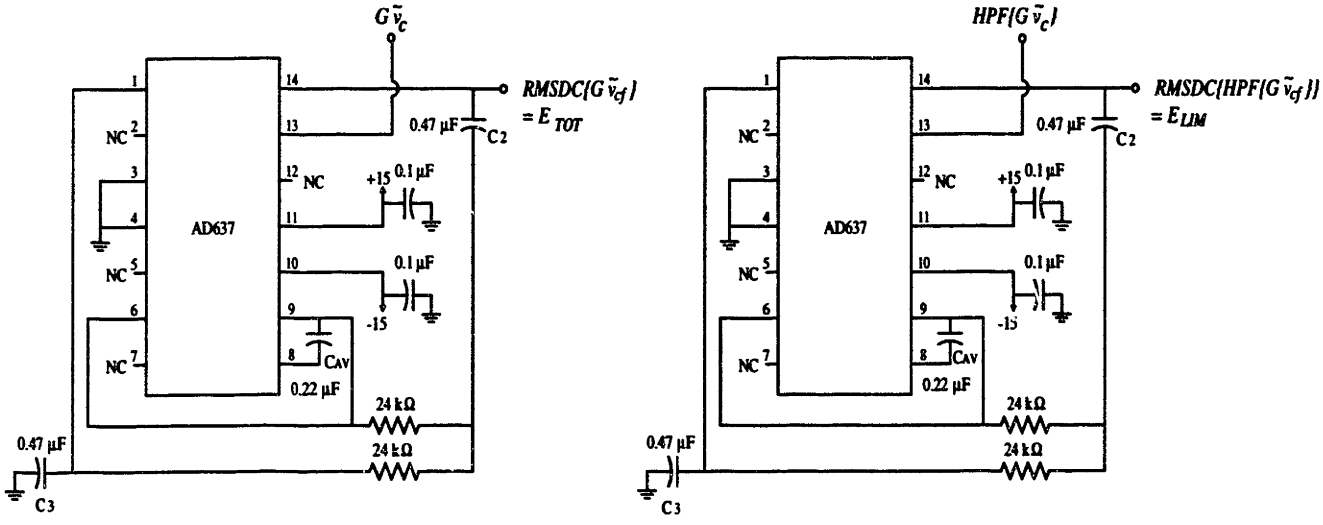

Figure 3-7: Schematic representation of rms-to-dc converter stage of the frequency estimator.

3.3 Current-Sharing Controller

The current-sharing controller adjusts the local cell reference voltage based on the difference between the two rms-to-dc converter outputs of the frequency estimator as illustrated in Fig 3-8.

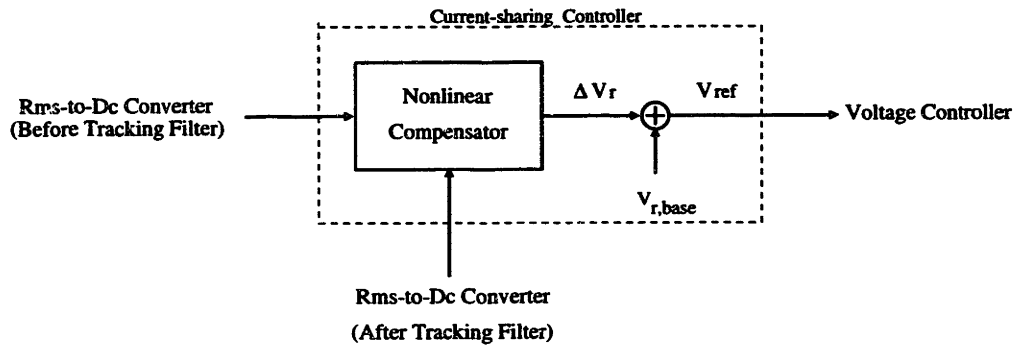

Figure 3-8: Block Diagram of the current-sharing controller.

To set up such a reference adjusting structure, we adopt the Unitrode UC3907 current-sharing IC. Figure 3-9 shows the inner structure of the section of the UC3907 concerned with the current-sharing function [12].

The UC3907 is designed to implement a single-wire current-sharing scheme in which the local voltage reference is shifted based on the difference between the local cell current and the signal on the current-sharing bus. We take advantage of this feature and replace the local-current signal and the share-bus signal with the two rms-to-dc converter output signals, so the UC3907 can instead be caused to adjust its local reference voltage to make two rms-to-dc converter outputs converge. While the UC3907 can implement the voltage control loop as well, this feature was not used in our circuit. Instead, as illustrated in Fig 3-10, the internal adjusted reference voltage generated by the UC3907 was extracted and amplified for use in an external voltage control compensator. The internal reference of the UC3907 varies in the range of 2.00 V to approximately 2.1 V. The circuit which extracts the internal reference amplifies it by a factor of 2.5, yielding a reference voltage range of 5.00 V to 5.25 V (5% adjustment). In our circuit connections, the current share bus input of the

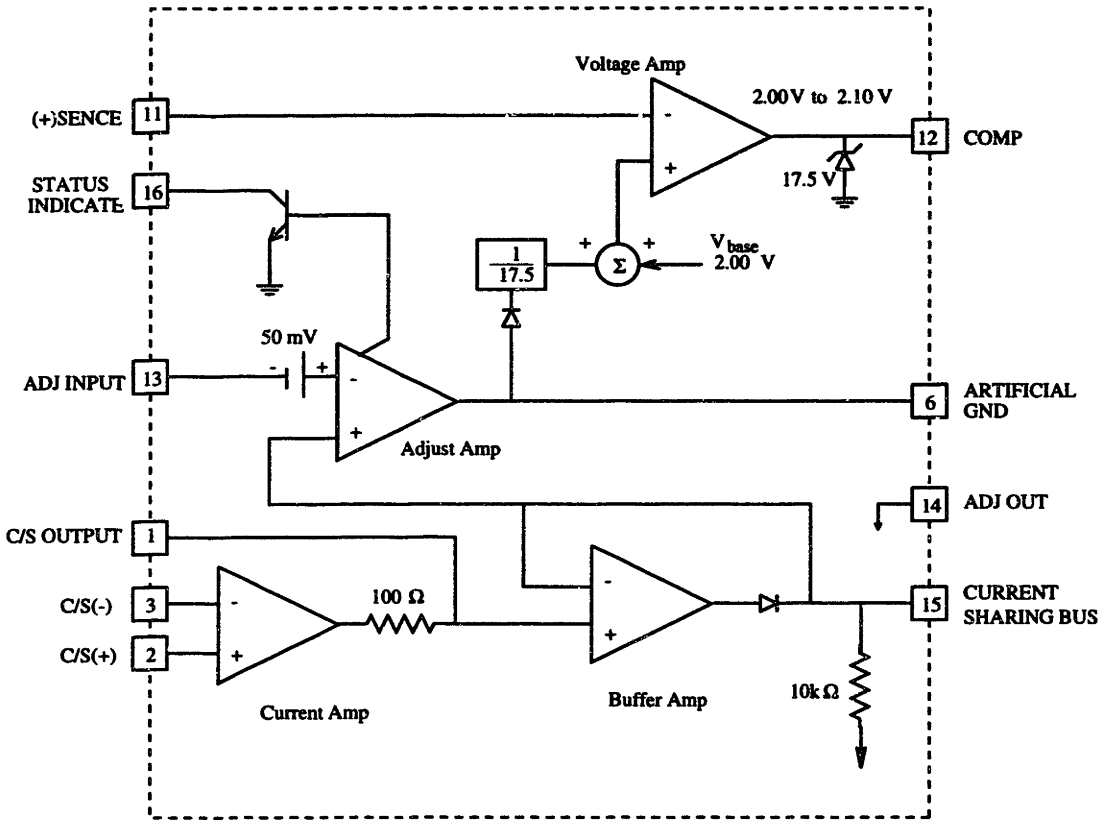

Figure 3-9: Current-sharing structure of UC3907.

UC3907 requires a minimum input of 200 mV and allows a maximum input of 15 V. To match this input range, the rms-to-dc converter outputs are processed through a gain of 3.2 and an offset of 200 mV before being applied to the UC3907.

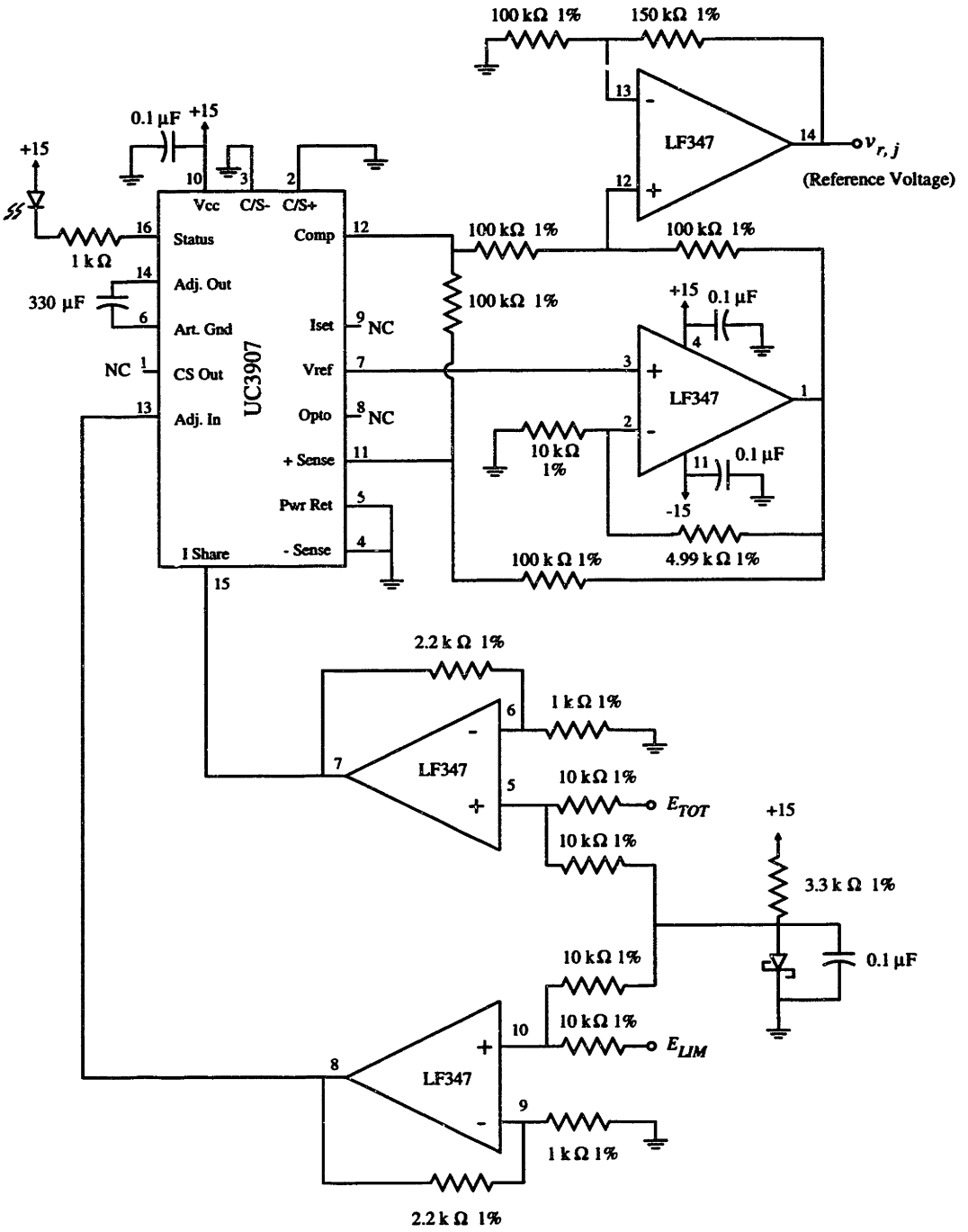

Figure 3-10: Schematic representation of the current-sharing controller used in the prototype system.

3.4 Voltage Controller

The voltage controller generates the output current reference based on the error between voltage reference (from the current-sharing controller) and the output voltage. The voltage control loop bandwidth is limited by switching frequency and load range. The controller must yield sufficiently small steady-state error and stable dynamics across load, yet not respond to switching frequency components in the output. To achieve these goals, we employ a lag compensator. The transfer function of the lag compensator is:

$$H(s) = \frac{k(T_z s + 1)}{T_p s + 1} \tag{3.1}$$

where k, T_p and T_z are the dc-gain, the zero time constant and the pole time constant, respectively. We chose $k = 0.16$, $T_p = 0.0159$ and $T_z = 0.00159$ for our circuit (see Appendix B.2). This compensator yields an output voltage control bandwidth which is far below the 1 kHz switching frequency. Figure 3-11 shows a root locus for the closed-loop system poles as the load resistance is changed from 166 Ω to 3000 Ω. We can see that this compensator achieves acceptable dynamics across the load range of the system.

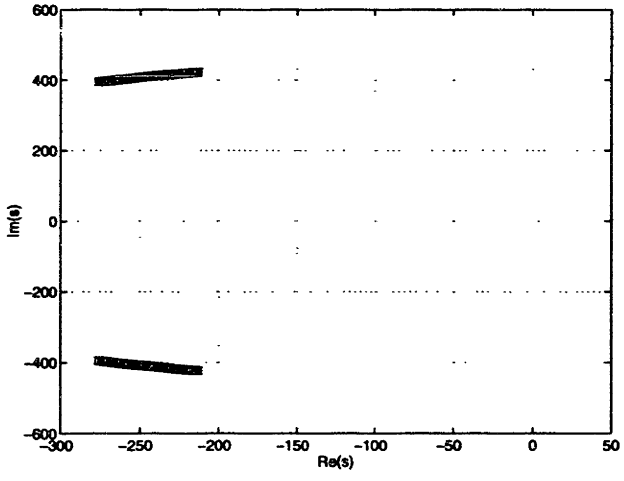

Figure 3-11: Locus of the system poles as the load resistance is changed from 166 Ω to 3000 Ω.

The voltage controller circuit implementation is illustrated in Fig. 3-12. The clamping circuit at the output ensures that the commanded reference current remains in the design range of 1-10 mA (1 V represents to 5 mA in the circuit).

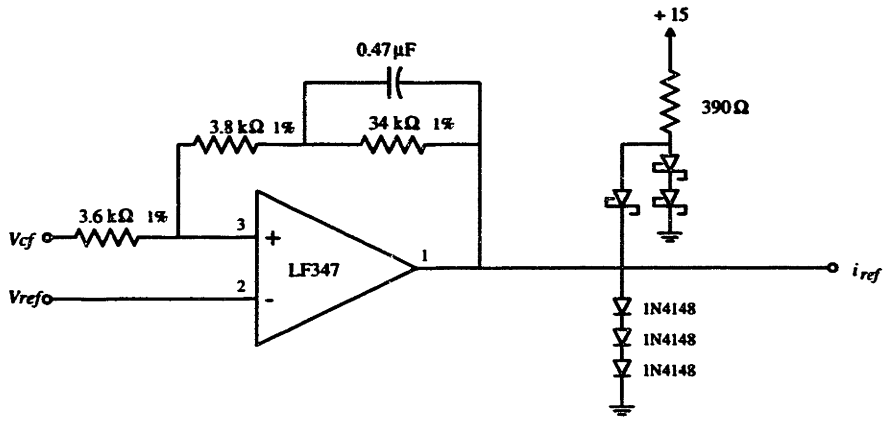

Figure 3-12: Voltage controller circuit for the prototype system.

3.5 Power Stage

The Power Stage is comprised of a buck converter and its current controller. In the buck converter as illustrated in Fig. 3-13, the transister VN0300 is turned on and off by switching signal LOSET so that the voltage of pin # 6 in the op-amp LF411 switches between 0 V and 10 V. When V_x is at 10 V, the inductor current increases and when V_x is at 0 V, the inductor current flows through diode D_2, and decreases. An INA106 differential amplifier is used to sense the output current, an LF411 is used to sense the output voltage.

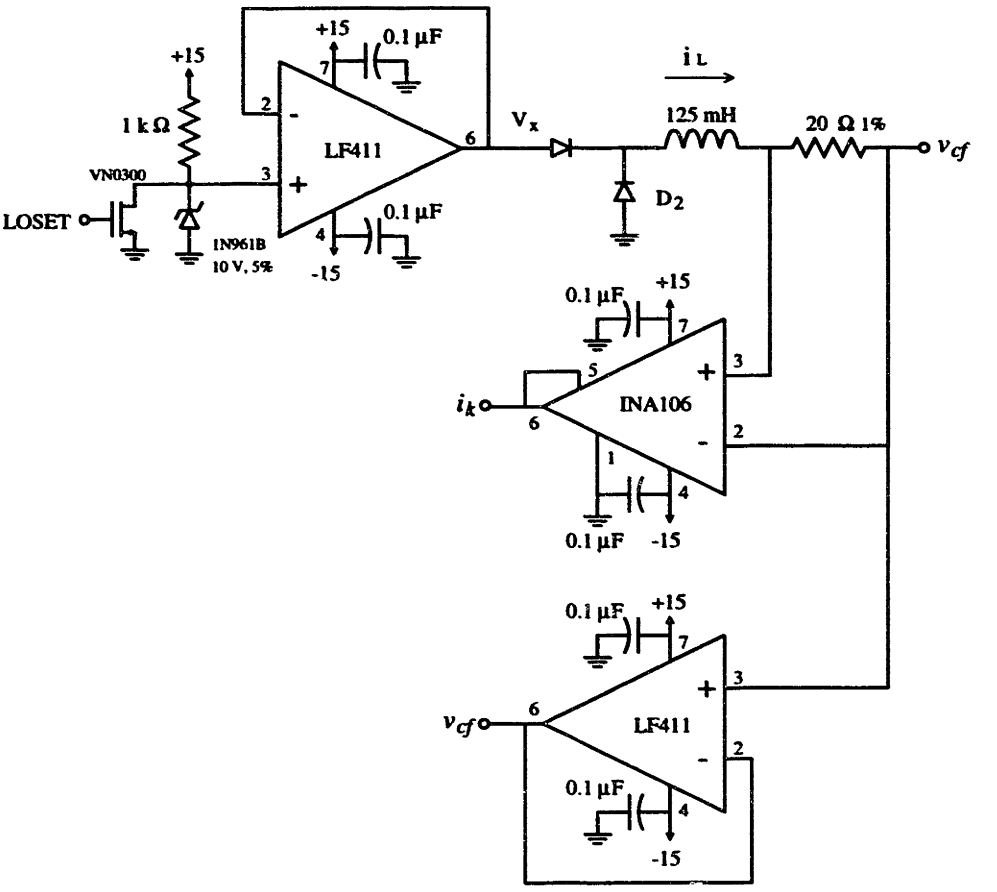

Figure 3-13: Schematic representation of the buck converter power stage for the prototype system.

Figure 3-14 shows the current controller that drives the buck converter to operate at the edge of discontinuous conduction mode (EDM). The current controller is designed to generate a switching cycle in which the output current linearly increases until it reaches twice the desired average output current, then decreases until it reaches 0 and repeats. This yields a triangular output current waveform (see Appendix A.1). In the current controller, thereby, the output current is compared with a negative limit, 0 V, and a positive limit, $2i_{\mathrm{ref,k}}$, which is twice the output current reference of the k^{th} cell. The flip-flop, DM74LS279, generates the gate drive signal, LOSET. The power stage operates in the following cycle. Until the output current reaches the positive limit, the output of comparator PM219, pin # 12 is clamped at 5 V so that $\bar{S}_2$ and $\bar{R}_4$ of the flip-flop are high. In this state, $\bar{Q}_2$, LOSET, is low, which means that the output voltage of the power stage buffer is 10 V, and the inductor current will increase.

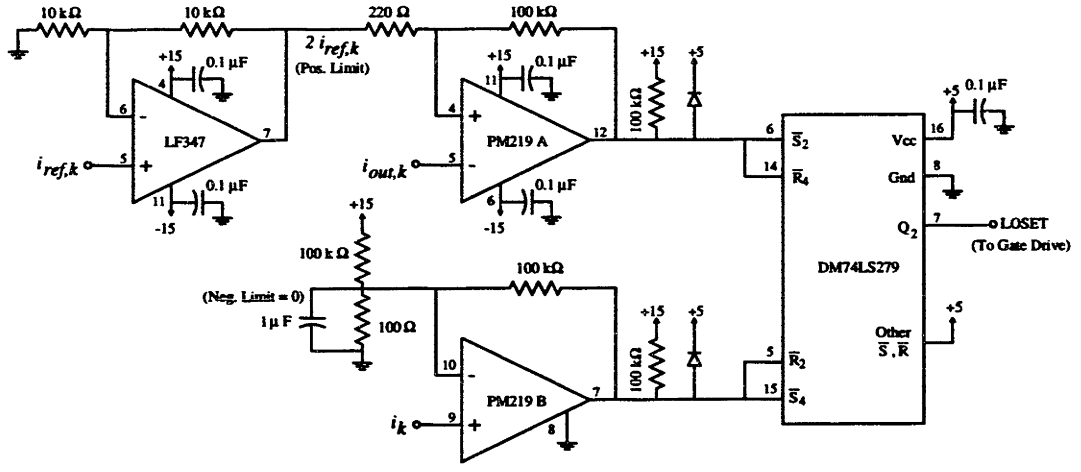

Figure 3-14: Current controller for EDM operation of the buck converter in the prototype system.

When the output current reaches the positive limit, the state is changed. During this time, the output of the PM219, pin # 12 changes to 0 V and pin # 5 is clamped at 5 V. This causes $\bar{S}_4$ and $\bar{R}_2$ of the flip-flop to be high so that $\bar{Q}_2$, LOSET, is high. Thus, the output voltage of the power stage buffer is 0 V, and the inductor current

decreases. Once the output current reaches the negative limit, the state returns to that of the beginning and the cycle starts over again. Figure 3-15 shows output voltage ripple, output current and drive signal (LOSET) of the buck converter operating in the edge of discontinuous conduction mode. As expected, the output current is triangular. We can also see that frequency of the switching ripple on the output voltage matches that of the drive signal (LOSET).

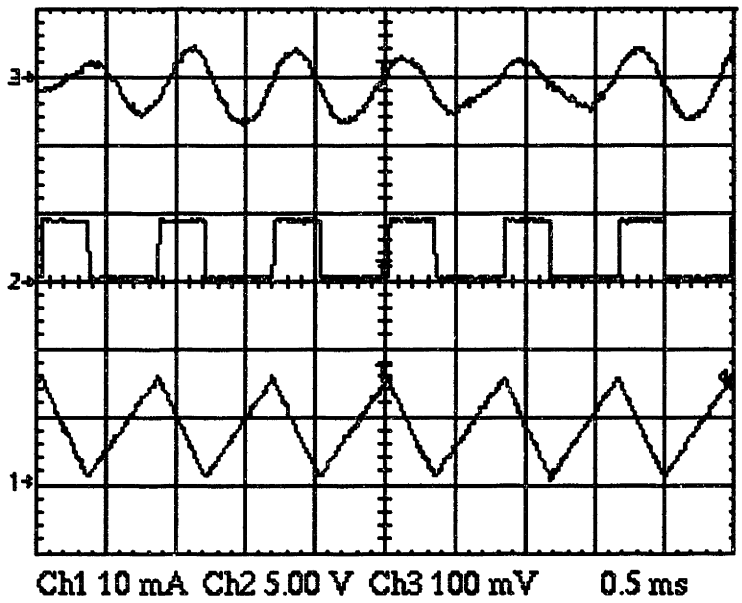

Figure 3-15: Waveform of three-cell buck converter operating at EDM (R_{load} = 278 Ω): Ch1 is the output current, Ch2 is the switching signal (LOSET) and Ch3 is the switching ripple on the output voltage

This chapter described the structure of a buck converter cell implementing switching ripple based method of current-sharing control. The subsystems needed to implement the system were described one by one and their circuit schematics were explained. In the next chapter, we will show experimental results from this system and discuss the viability of this system.

Chapter 4

Experimental Results

Chapter 3 presented the implementation of a prototype cellular converter system using the switching ripple based method. In this chapter, we focus on the current-sharing experiments, using the prototype system. Section 4.1 describes the experimental setup. Then, we discuss the static current-sharing test in Section 4.2 and introduce a load regulation test in Section 4.3. The transient current-sharing test is described and compared to the Simulink simulation in Section 4.4. Finally, Section 4.5 discusses the load step test.

4.1 Cellular Converter Testing

The circuits introduced in Chapter 3 were implemented on protoboards and vectorboards to allow easy modification. The circuits consist of three identical cells that each have their own estimator, voltage controller and power stage.

4.1.1 Test Equipment

The system was powered with ± 15 V from a dual dc supply, Hewlett-Packard HP6205B. A Tektronix TDS 420A oscilloscope was used to measure output voltage and output current. To observe the voltage ripple frequency content, a signal analyzer, Hewlett-Pacard HP3561A was used. Data were retrieved from the signal analyzer with Na-

tional Instruments' Interactive Control (IBIC) program. Figure 4-1 shows a diagram of the cellular converter test setup.

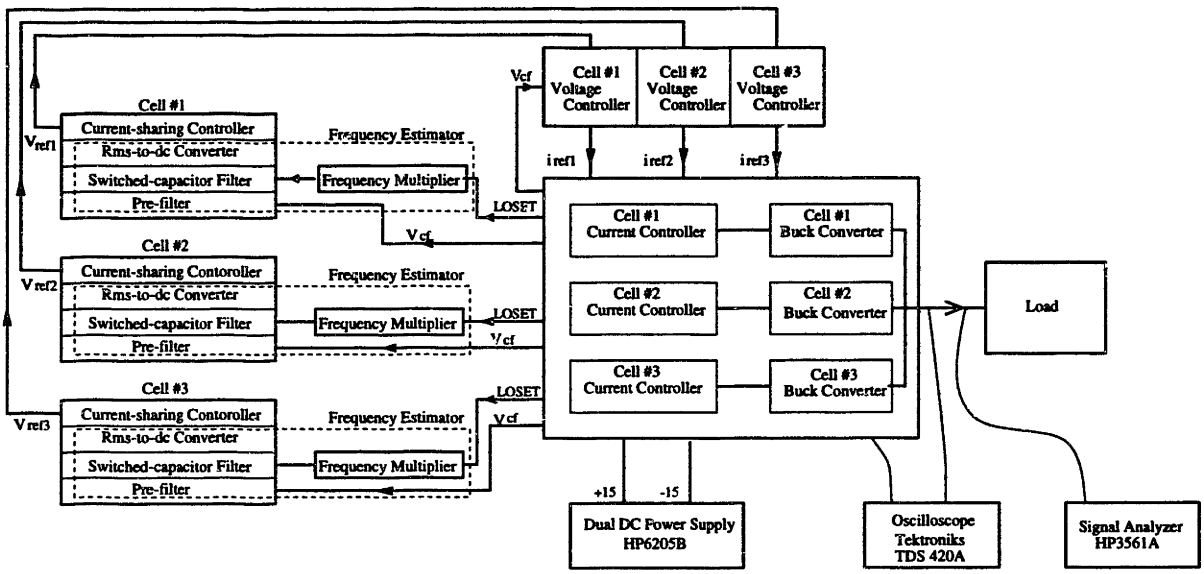

Figure 4-1: Diagram of the cellular converter testing.

4.1.2 Current-Sharing Control Turn-off Switch

In the prototype system, the current-sharing function can be turned on and off by a switch in order to study the effectiveness of the current-sharing implementation. Current sharing is turned off by grounding the current-sharing adjustment input of the UC3907 in Fig. 3-10. The switch works in the following way. Since all current sharing ICs, UC3907, are not identical, each UC3907's adjustment range is slightly different from the others. For example, for the three cell converter case, the adjustment ranges of the cells could vary as shown in Fig 4-2. Thus, in our experiments without current-sharing control, we eliminate the adjustment functions of the UC3907 and fix the voltage reference at each cell's maximum or minimum value of the adjustment range, resulting in a non-current-sharing condition.

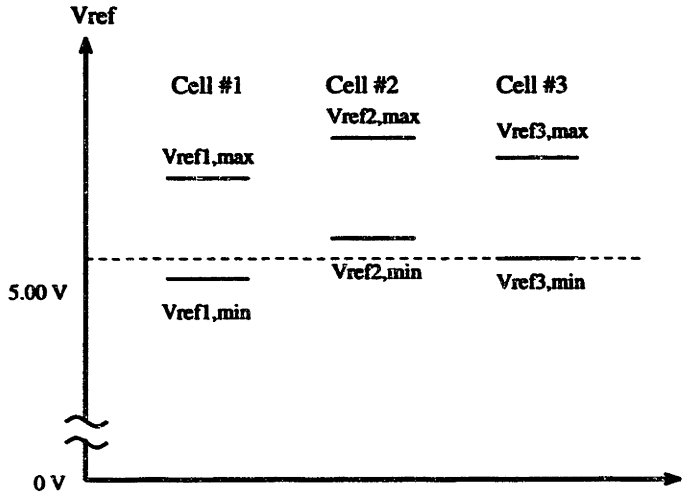

Figure 4-2: Variation of the V_{ref} range in UC3907.

Two switch positions are employed. Position 1 shorts the adjusting bus (pin #13) to ground. Position 2 connects the adjusting bus to +15 V, as shown in Fig 4-3.

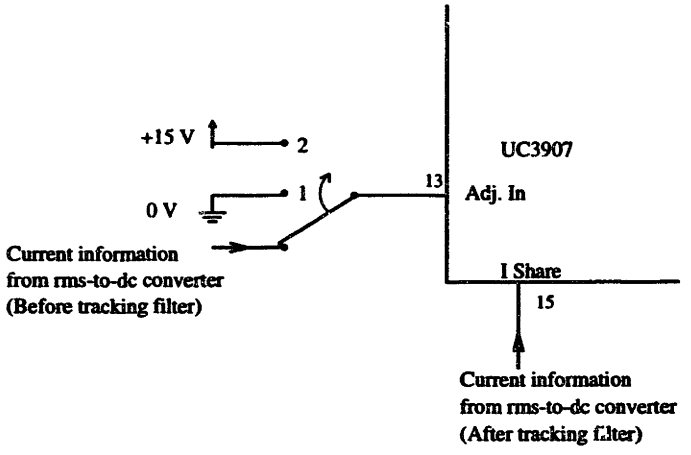

Figure 4-3: Connection of current-sharing control turn-off switch.

Position 1 was used in Section 4.2, 4.4 and 4.5, and Position 2 was used in Section 4.3. In Position 1, the connection between the adjusting bus and ground sends a signal that there are some cells supplying higher current than the local cell. As a result, the local cell's voltage reference gets driven to its maximum value in order to catch up to the other cells' currents. In Position 2, the connection between the adjusting bus and +15 V sends a signal that the local cell is supplying the highest current, and the

Table 4.1: Adjusting ranges of voltage references of UC3709 in the prototype circuit.

	Cell #1	Cell#2	Cell#3
Max Vref	5.27 V	5.22 V	5.25 V
Min Vref	5.00 V	4.96 V	4.99 V

local cell's voltage reference is driven to its minimum value. Since the cell voltage reference adjustment ranges have slightly different maximum and minimum values, the cell voltage references are fixed at slightly different values, resulting in a loss of current-sharing. Table 4.1 shows the maximum and minimum values of the voltage references' adjustment ranges of UC3709 in our prototype circuit.

4.2 Static Current-Sharing Test

To observe current-sharing performance of the system over the load range, we conducted static current-sharing tests for both two-cell and three-cell cases, both with and without current-sharing control. The tests were performed by varying the load current from 5 % to 100 % of rated load and observing the cell reference currents. Figure 4-4 shows the plots of the reference current (equal to the average output current) of each cell versus the total converter output current without current-sharing control for the two-cell case. In this case, the currents were heavily imbalanced, except at the very light and heavy load condition. This current-sharing behavior can be understood as follows. Without current-sharing control, the two cell voltage references are different as previously explained. Because the cells have a low (dc) output impedance, the small voltage reference imbalance causes large current imbalances over most of the load range. At light and heavy loads, however, the clamping limits on the cell reference currents caused the cells to share current more evenly.

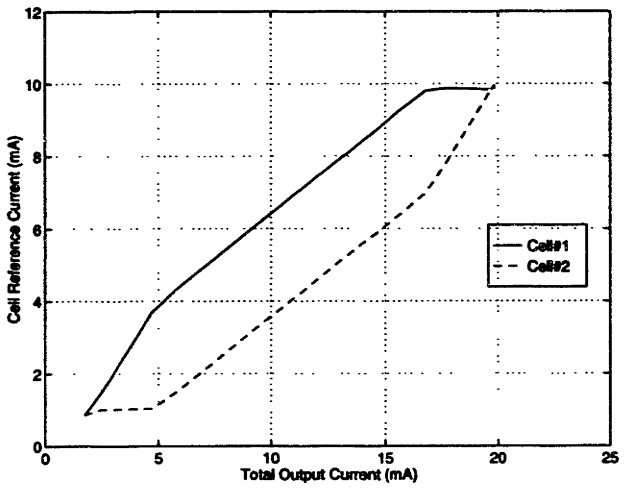

Figure 4-4: Static current-sharing characteristic of the two converter cells without current-sharing control.

Figure 4-5 shows the cell currents with current-sharing control for the two-cell case. We can see that the cell currents balance within 5%, due to the current sharing control.

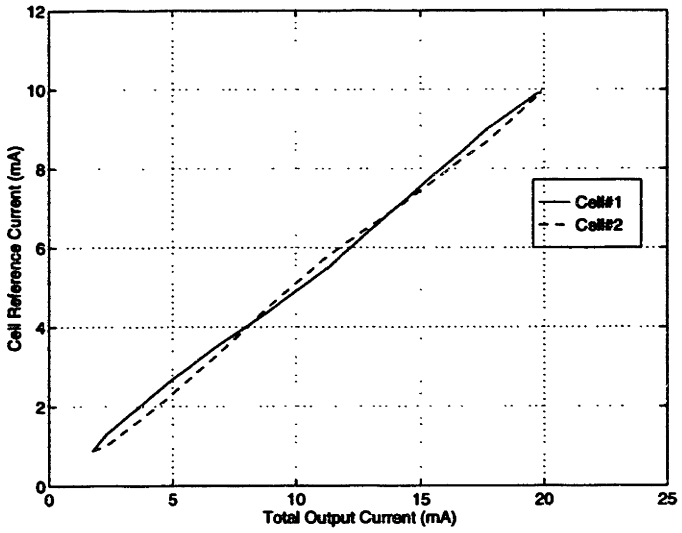

Figure 4-5: Static current-sharing characteristic of the two converter cells with current-sharing control.

Figures 4-6 and 4-7 show the cell currents without and with current-sharing control for the three-cell case. As we saw in the two-cell case, the heavy current imbalance that occurs without current-sharing control is eliminated when current-sharing control is implemented.

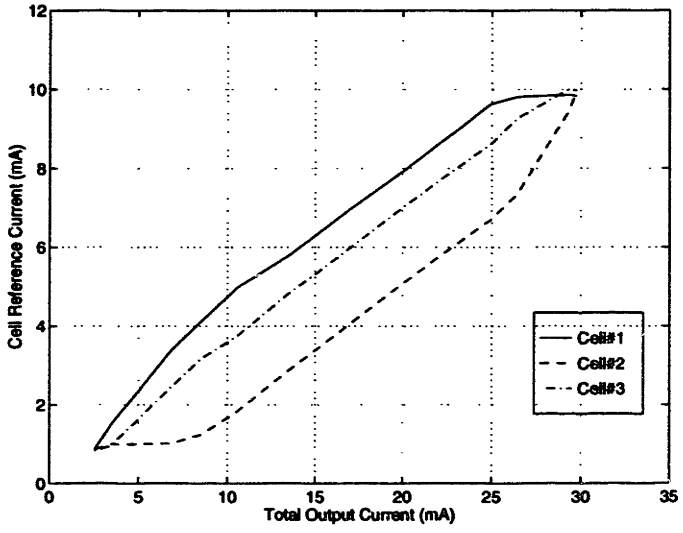

Figure 4-6: Static current-sharing characteristic of the three converter cells without current-sharing control.

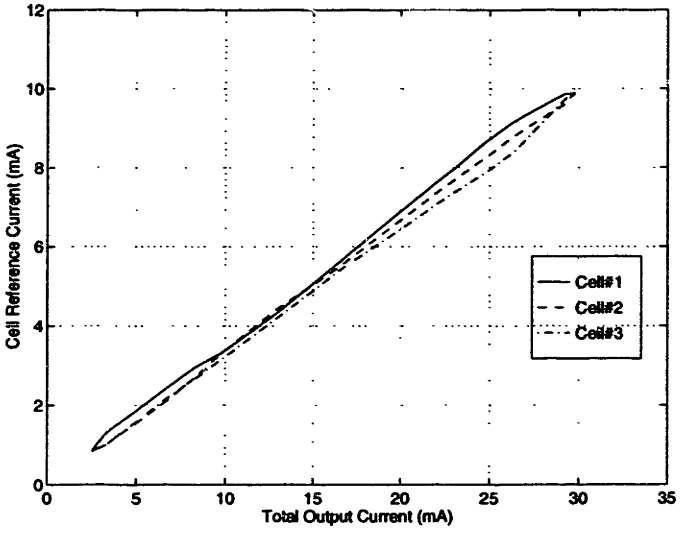

Figure 4-7: Static current-sharing characteristic of the two converter cells with current-sharing control.

The frequency spectrum of the aggregate output voltage switching ripple was observed using a spectrum analyzer. Figure 4-8 shows a spectrum analyzer plot displaying the frequency content of the output voltage without current-sharing control for the three cells at 60% load. The difference in ripple frequencies among three cells is apparent. These frequencies have an inverse relation to the average output current as explained in Chapter 2. This fact can be recognized in the output current waveform at 60% load as shown in Fig 4-9. There is significant imbalance of amplitudes and switching frequencies among the three cells.

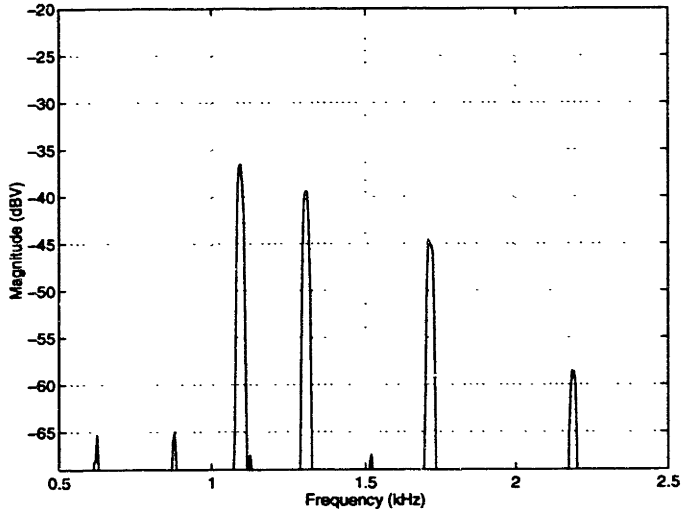

Figure 4-8: Spectrum analyzer plot displaying the frequency content of the output voltage for three cells without current-sharing control at 60% load.

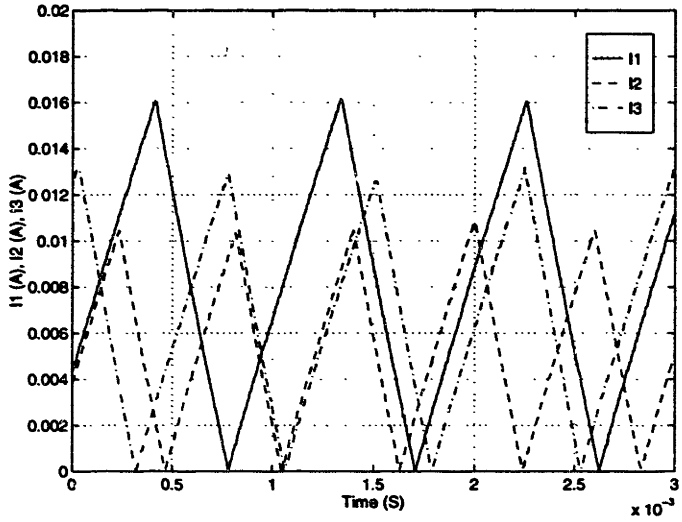

Figure 4-9: Output current waveform of three cells operating without current-sharing control at 60% load.

Figures 4-10 and 4-11 show the spectrum analyzer plot and the output current waveforms with current-sharing control. In this case, the cell ripple frequencies are almost identical, as are the individual cell currents.

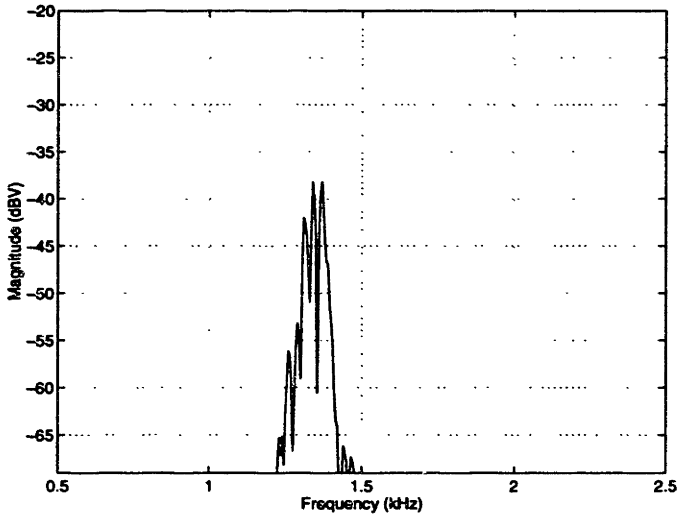

Figure 4-10: Spectrum analyzer plot displaying the frequency content of the output voltage with current-sharing control at 60% load.

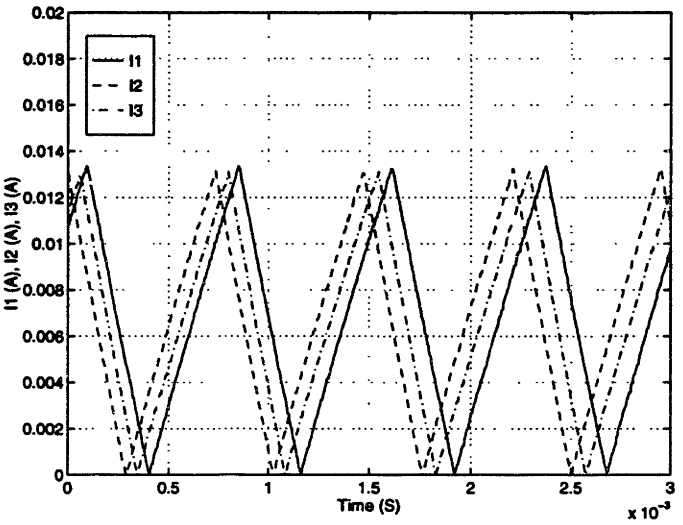

Figure 4-11: Output current waveform of three cell converters with current-sharing control at 60% load.

Table 4.2 summarizes the relationship of voltage reference (V_{ref}), average output current (i_{ref}) and switching frequencies with and without current-sharing control. From these results, we can conclude that the switched ripple based method of current-sharing control works to accurately balance the output currents and frequencies over a wide load range in a steady-state. This is achieved without the use of interconnections for communicating information.

Table 4.2: Measurement results of voltage reference (V_{ref}), average output current (i_{ref}) and switching frequencies with and without current-sharing control.

	Without Current-sharing Control			With Current-sharing Control		
	Cell #1	Cell#2	Cell#3	Cell #1	Cell#2	Cell#3
V ref	5.33 V	5.28 V	5.31 V	5.29 V	5.28 V	5.28 V
i ref	7.95 mA	5.01 mA	7.04 mA	6.88 mA	6.66 mA	6.43 mA
Switching frequency	1.89 kHz	1.34 kHz	1.68 kHz	1.34 kHz	1.34 kHz	1.34 kHz

4.3 Transient Current-Sharing Test

We also observed the transient current sharing behavior of the system. The measurement was conducted by observing the response when current sharing was turned on after the system was in the steady-state without current-sharing control. We compare results for the two-cell case (using cells #1 and #2) to simulations of the type developed in Chapter 2. In the simulation, current-sharing control was based on an integrating compensator with a fixed gain. In the real system, the situation is complicated by the nonlinearity and dynamics of the frequency estimator [19, 20]. The behavior of the frequency estimator plays an important role in determining the dynamics of the system, and should be further investigated in the future. However, for reasonable time-scale separations among the output voltage control dynamics, the frequency estimator dynamics, and the current-sharing dynamics, the frequency estimator can at least roughly be approximated as a fixed gain. Thus, in the simulations, appropriate fixed gain was selected such that the current-sharing control bandwidth was approximately correct. Figure 4-12 shows the transient behavior of voltage references of both cells after current-sharing control is conducted.

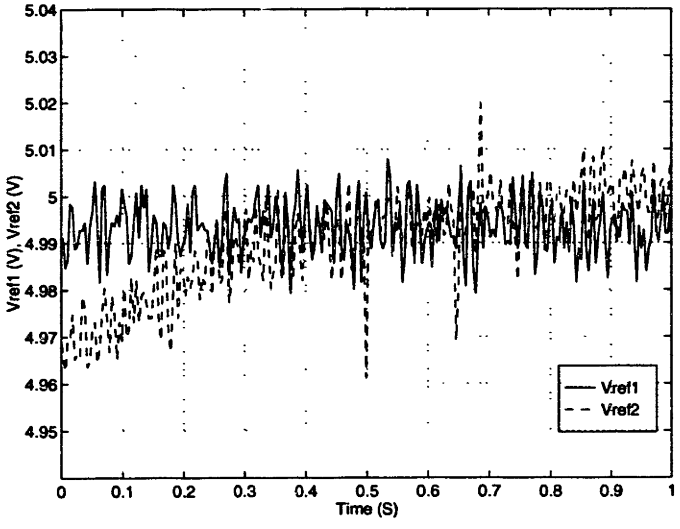

Figure 4-12: Transient response of the voltage references when current sharing is turned on ($R_L = 500\ \Omega$).

Its Simulink simulation explained in Chapter 2 is illustrated in Fig 4-13.

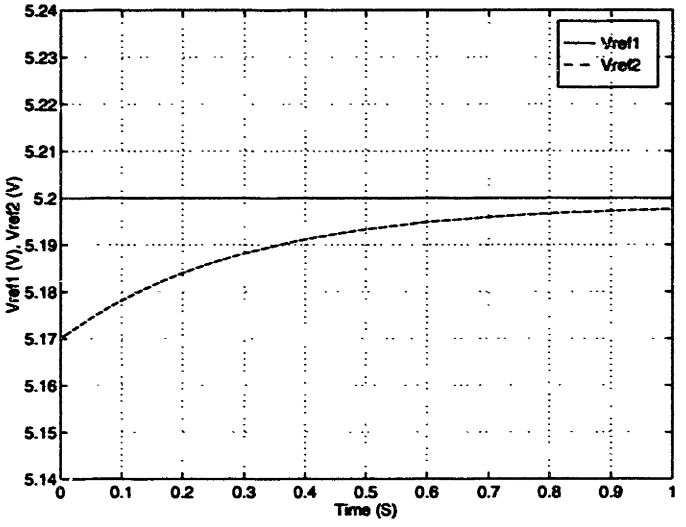

Figure 4-13: Simulated transient response of the voltage references when current sharing is turned on ($R_L = 500\ \Omega$).

From these figures, we can observe the operation of the current-sharing loop. At first, current-sharing is turned off so that the output voltage references of two cells were set to their minimum value. In our circuits, cell #1's voltage reference was higher than that of cell #2 so that the average output current of cell #1's current was larger than that of cell #2's, yielding current imbalance. Once the current-sharing switch was turned on, cell #2's estimator compared its switching frequency to the aggregate switching ripple on the output voltage and recognized that its output current was lower than that of cell #1. Cell #2 increased its voltage reference to make its output current meet cell #1's current. While cell #2's voltage reference was rising, cell #1's converter voltage reference remained at the same value. As a result, the output currents of cell #1 and cell #2 converged. Figures 4-14 and 4-15 show the transient behavior of the average output currents. We can see that after current-sharing control started, both cells' average output currents converged. When the simulation and the experimental results are compared, it turns out that the operation of the current-sharing circuits meets the expectations proposed in our theory.

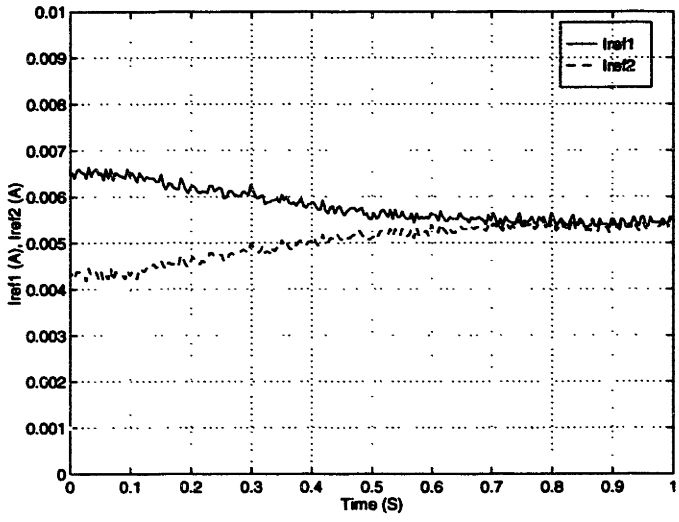

Figure 4-14: Transient response of the average output current when current sharing is turned on ($R_{\mathrm{L}} = 500\ \Omega$).

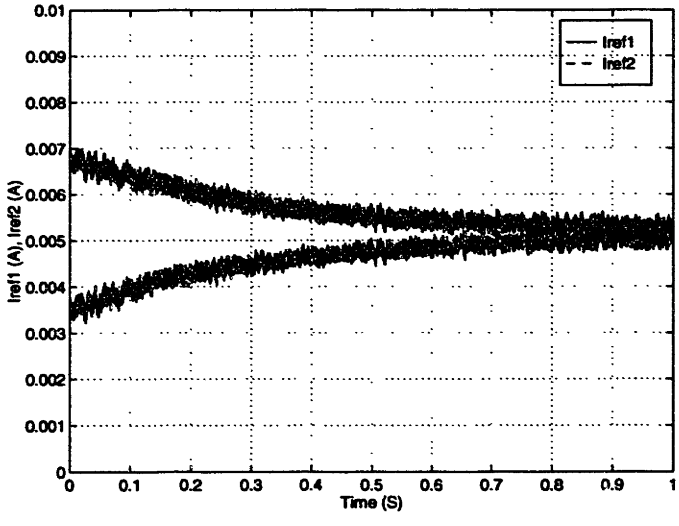

Figure 4-15: Simulated transient response of the average output current when current sharing is turned on ($R_{\mathrm{L}} = 500\ \Omega$).

4.4 System Load Regulation

In obtaining data of the cells' static current-sharing ability, we also acquired voltage regulation characteristics over the range of the system for both the two-cell and three-cell cases with and without current-sharing control. The load regulation characteristics are illustrated in Fig. 4-16 and 4-17. In both two cell converters and three cell converters with current-sharing control, the output voltage varies within 2.9% because each cell adjusts its voltage reference to achieve current-sharing control. We can understand that the ramp that occurred around 50% of the load with current-sharing control was caused by adjusting the voltage reference to achieve current balance. It can be noted that this variation range is associated with the voltage reference adjusting range; hence this variation is almost constant in any number of cells. We can also observe the voltage rise at light load and the voltage droop at the heavy load because the control system clamps the minimum and maximum values. In the case without current-sharing control, voltage regulation occurs; the two cell converters regulate with 3.8% and three cell converters regulate with 3.4%. It can be explained that this voltage regulation is caused by the finite dc-gain k of the lag compensation circuit in the voltage controller.

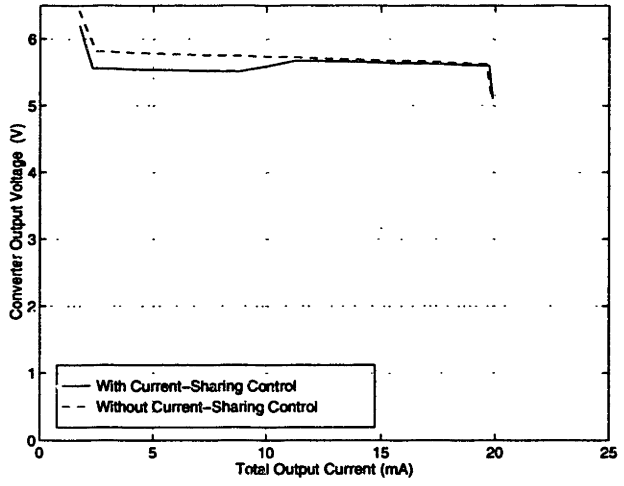

Figure 4-16: Load regulation characteristic of the two cell converters.

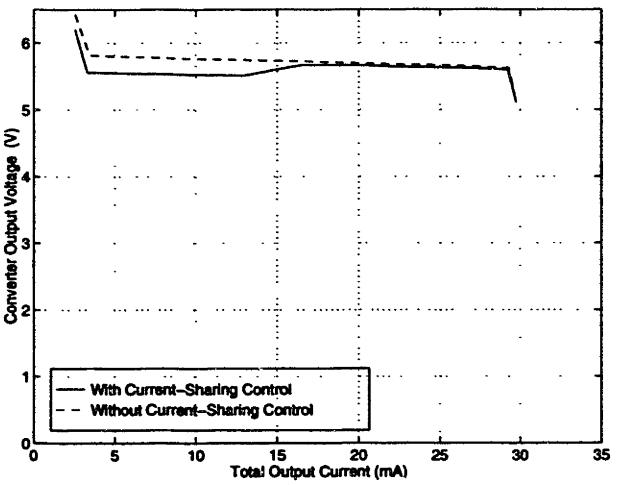

Figure 4-17: Load regulation characteristic of the three cell converters.

4.5 Load Step Test

To demonstrate the stability of the system for a load step transient, load step tests were conducted. Load steps were achieved by connecting and disconnecting an additional resistor every 2.5 s. Figure 4-18 shows the load step circuit used in the test.

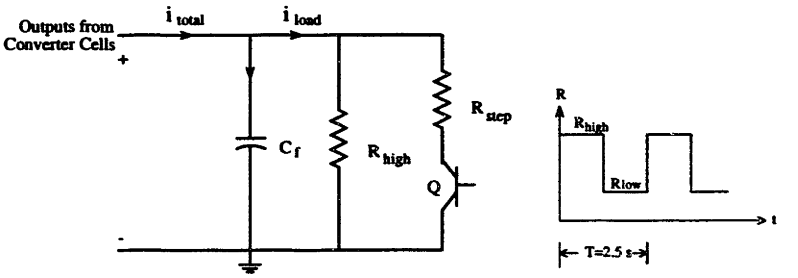

Figure 4-18: Load step circuit used for the prototype system.

The resistance R_{step} is chosen to have the following relation:

$$R_{\text{step}} = \frac{R_{\text{low}} R_{\text{high}}}{R_{\text{low}} - R_{\text{high}}}. \tag{4.1}$$

The test parameters used in the test are listed in Table 4.3.

Table 4.3: Parameters used in load step test.

	R high (75 % Load)	R low (25 % load)	R step
Two Cells	333 Ω	1 k Ω	500 Ω
Three Cells	222 Ω	667 Ω	333 Ω

Figure 4-19 and 4-20 show the oscilloscope measurement of the average output currents in the load step test for the two-cell and three-cell cases. We measured the output current references as a measure of the average cell output currents. This is valid because the average output currents track the output current references accurately.

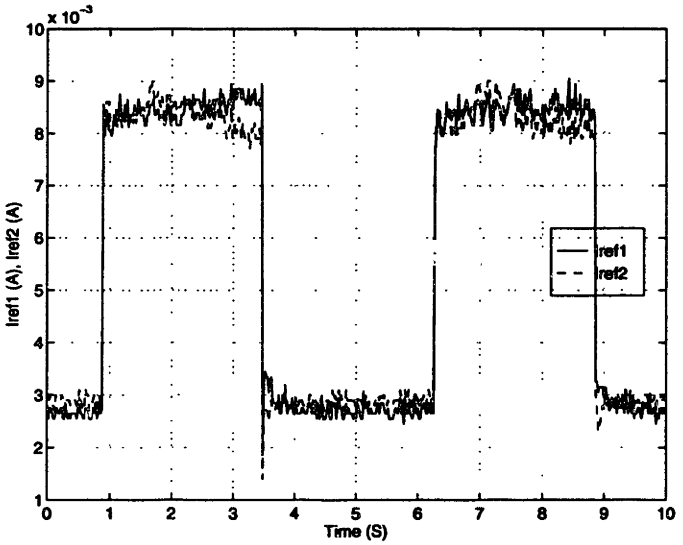

Figure 4-19: Current-sharing behavior of two cell converters for load step between 333 Ω and 1000 Ω (approximately 25% to 75% of full load.)

In the two-cell case, the average output currents of both cells followed the changing of load well. In the case of three cells, when the load stepped to 75% load from

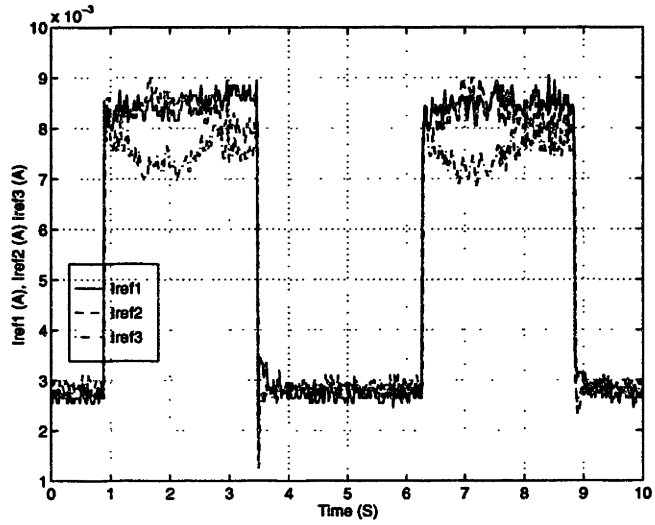

Figure 4-20: Current-sharing behavior of three cell converters for load step between 222 Ω and 667 Ω (approximately 25% to 75% of full load.)

25% load, the average output current overshot by a small amount and the current-sharing controller worked to stabilize the cells' average output current at a single value. It can be seen that the process of current converging in the three-cell converter is more complicated than the case of two cells. Because the current-sharing control is non linear, it is not simple to predict the detailed control behavior; this investigation should be conducted in the future. From these results, we can conclude that the current-sharing behavior is seen to be quite stable for even large load steps.

What may be concluded from the experimental results presented in this chapter is that the switching ripple based method allows accurate and stable current sharing to be achieved over a wide load range without the use of interconnections for communicating current-sharing behavior.

Chapter 5

Conclusions and Recommendations

This thesis has developed a novel approach to current-sharing control, the switching ripple based current-sharing control method. This approach, which is based on encoding the current-sharing information in the switching ripple component of the output voltage, eliminates the need for additional current-sharing interconnections among cells. Elimination of the current-sharing interconnections removes the source of single-point failures, yielding a significant reliability advantage.

The developed method has several advantages. First, because it relies only on each cell detecting the existence of switching frequencies lower than its own, the approach is simple to implement and is unaffected by the harmonic content of the switching ripple. Second, since the current-sharing controllers operate independently, the system is robust against breakdown. Even if some cells in the system fail, the remaining cells still share current. Third, this approach can be applied to any kind of converter with a monotonic relation between switching frequency and average output current. Even converters that do not normally exhibit such a relation can often be adapted to implement one, allowing the approach to be used.

In Chapter 1, we reviewed the typical current-sharing methods with interconnections, and pointed out their limitations. Chapter 2 proposed the switching ripple based current-sharing control. This method is based on the use of the information

contained in the switching ripple component of the output voltage. Since the switching frequency content of all the cells appears as an aggregate switching ripple on the output voltage, each cell can pick up information about other cell currents from the output voltage ripple. Using information about cell switching frequencies determined from the switching ripple, each cell controls its own output current such that no other converter operates at a lower switching frequency than its own. For analytical investigation, a Simulink simulation model demonstrating this control method was introduced. A two-cell buck converter system was used to demonstrate this method. Each simulated cell was operated in the edge of the discontinuous conduction mode (EDM), yielding a switching frequency that was inversely proportional to its output current. Current sharing was achieved by having each cell adjust its output voltage reference such that no other cell is operated at a significantly lower frequency (or higher current). Simulation results illustrated the behavior of the voltage references and output currents under this current-sharing control method.

The implementation of a prototype system with this current-sharing control method was introduced in Chapter 3. The prototype system is a three-cell buck converter system with cells operating in EDM. Each cell has a current-controlled power stage, a voltage controller, a current-sharing controller and a frequency estimator. The power stage was designed to supply 5 V of output voltage and output current ranging from 1 to 10 mA. The voltage controller was designed to yield sufficiently small steady-state error and stable dynamics across the load, and to be insensitive to switching frequency components in the output. In the current-sharing controller, we adopted the Unitrode UC3907 current-sharing IC to adjust output voltage reference. The frequency estimator used by the current-sharing controller was designed to be simple and insensitive to harmonics of the fundamental switching frequencies.

The experimental results in Chapter 4 showed the static and transient performance of the prototype system with both two and three cells operating. The static current-sharing test showed the cell current balance within 5%, due to the current sharing controller. In the transient current-sharing test, we observed that the output voltage reference and output current performed acceptably, as predicted theoretically.

The load regulation test showed that the output voltage varies within 2.9%, which is quite acceptable. The load step test demonstrated the system's stable behavior for even large load steps. From the experimental results, it can be concluded that the switching ripple based method allows accurate and stable current sharing to be achieved over a wide range without the use of interconnections for communicating current-sharing information.

Based on these results, the following recommendations for future work were provided. A detailed analysis of stability of the system with our current-sharing method has not been undertaken. This thesis analyzed the stability of the subsystems individually, but the whole system's performance is investigated by use of simple, rough models, Simulink simulations and experiments. Better analytical models for this current-sharing method will simplify its use in practical applications. Other suggestions include: 1) Testing in high power environments (even if we are successful in the high-power model, we would suggest it be tried with an even higher power system, e.g., 1 kW or more). 2) Test with other converter types with different variations in the switching frequency versus the output current (for example, quasi-resonant converters).

Appendix A

Derivations

A.1 Buck Converter in Edge of Discontinuous Conduction Mode (EDM)

In this thesis, the buck converter operating in the edge of discontinuous conduction mode (EDM) is employed to demonstrate the switching ripple based current sharing control. The basic circuit schematic of the buck converter and the waveform of the inductor current (equal to output current), i_L, in EDM are illustrated in Fig. A-1 and A-2 [21].

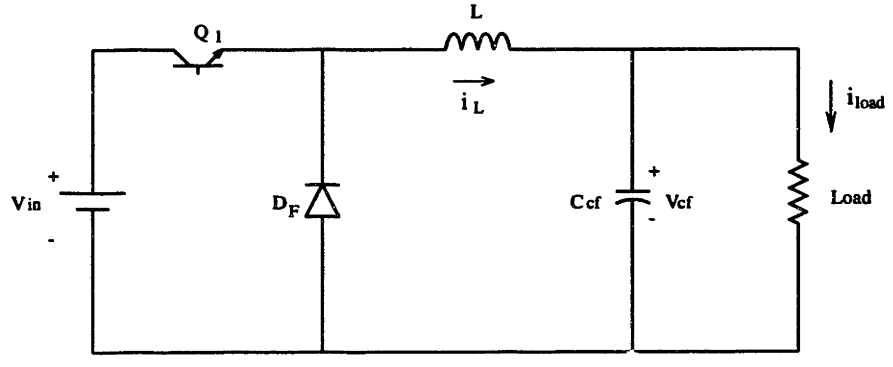

Figure A-1: Circuit schematic of the buck converter.

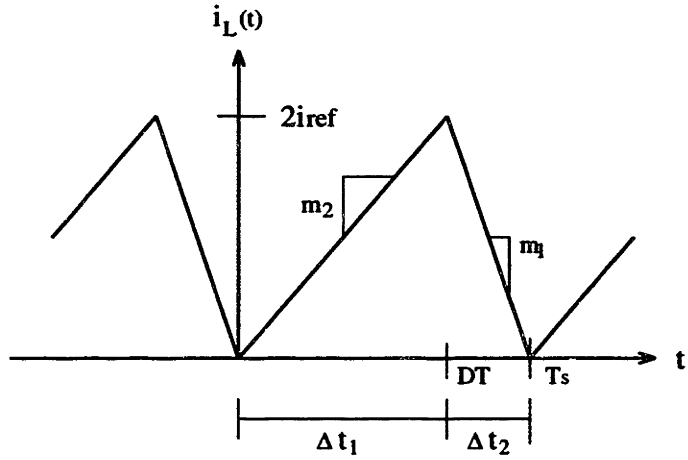

Figure A-2: Waveform of the inductor current in the edge of discontinuous conduction mode (EDM).

Based on the premise that the output filter capacitor, C_f, is large enough to maintain the output voltage constant, we assume that the converter is supplying a constant voltage to an output resistive load. This circuit has the following cycle. First, the transistor, Q, is turned on until its output current, i_L, reaches two times the output current reference, $2i_{ref}$. The equivalent circuit of this mode is illustrated in Fig. A-3. The output current increases linearly from zero to $2i_{ref}$, expressed as the following equation:

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t_1} = \frac{V_L}{L} = \frac{V_{in} - V_{cf}}{L} \tag{A.1}$$

where $\Delta i_L = 2i_{ref}$. The corresponding slope of the capacitor voltage during this time is

$$\frac{dV_{cf}}{dt} = \frac{i_{load} - i_L}{C_f}. \tag{A.2}$$

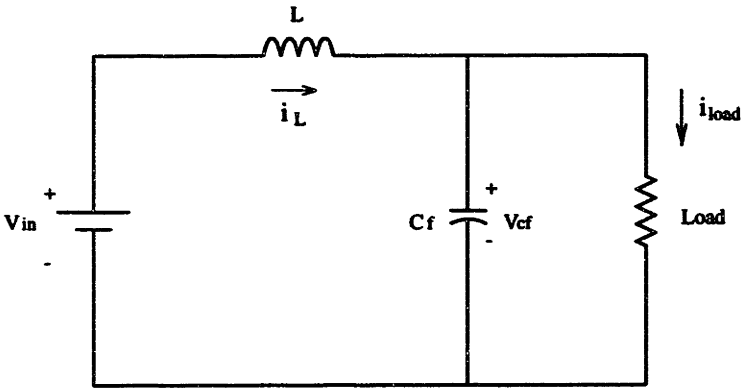

Figure A-3: Equivalent circuit for Fig. A-1 when the transistor Q is on until DT_s.

Then, when the output current reaches two times output current reference, $2i_{ref}$, the transistor Q is turned off until i_L returns to zero. The inductor current decreases linearly, as it circulates through the freewheeling diode D_F as shown in Fig. A-4. The slope of the inductor current and capacitor voltage for this period is expressed as:

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t_2} = \frac{V_L}{L} = \frac{-V_{cf}}{L} \tag{A.3}$$

$$\frac{dV_{cf}}{dt} = \frac{i_{load} - i_L}{C_f}. \tag{A.4}$$

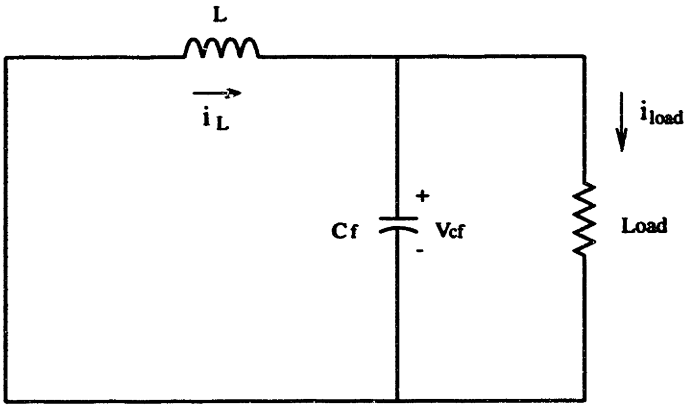

Figure A-4: Equivalent circuit for Fig. A-1 when the transistor Q is off from DT_s to T_s.

The inductor charge and discharge times can be computed from A.1 and A.3 and Fig. A-2:

$$\Delta t_1 = \frac{2Li_{\text{ref}}}{V_{\text{in}} - V_{\text{cf}}} \tag{A.5}$$

$$\Delta t_2 = \frac{2Li_{\text{ref}}}{V_{\text{cf}}}. \tag{A.6}$$

The switching period, T_s, is the sum of the inductor charging time, Δt_1, and discharging time, Δt_2:

$$T_s = \Delta t_1 + \Delta t_2 = \frac{V_{\text{in}} L(2i_{\text{ref}})}{V_{\text{cf}}(V_{\text{in}} - V_{\text{cf}})}. \tag{A.7}$$

From A.7, we can deduce that the switching frequency is inversely proportional to i_{ref}.

Appendix B

Circuit Implementation

B.1 Frequency-dependent Amplifier in the Pre-filter Stage of the Estimator

The amplitude of switching ripple (assuming it to be sinusoidal) in the output voltage is proportional to the output current reference (average output current), i_{ref}, and it is inversely proportional to the switching frequency,f_{sw}, and filter capacitor, C_{f}:

$$\Delta V = \frac{i_{\text{ref}}}{2\pi f_{\text{sw}} C_{\text{f}}}. \tag{B.1}$$

In a buck converter operating in EDM, the switching frequency is related to input voltage, V_{in}, output voltage, V_{cf}, the inductor, L and output current reference i_{ref}:

$$f_{\text{sw}} = \frac{V_{\text{cf}}(V_{\text{in}} - V_{\text{cf}})}{V_{\text{in}} L(2i_{\text{ref}})}. \tag{B.2}$$

B.1 and B.2 represent the relation such that switching ripple in the output voltage is square proportion to the output reference as expressed in B.3:

$$\Delta V = \frac{V_{\text{in}} L(i_{\text{ref}}^2)}{\pi C_{\text{f}} V_{\text{cf}}(V_{\text{in}} - V_{\text{cf}})}. \tag{B.3}$$

From B.3, it is noted that the amplitude of the switching ripple gets smaller in the lighter load (higher switching frequency), resulting in a small signal of the cur-

rent information. Thus, to compensate the light load performance, we employed a frequency-dependent amplifier, which is the cascade of a band limited differentiator and a fixed gain amplifier (gain=34) as shown in Fig B-1.

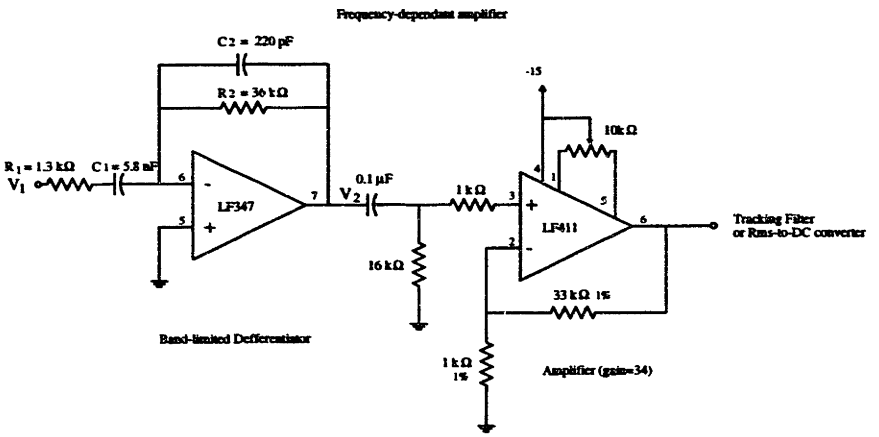

Figure B-1: Circuit schematic of the back converter.

Since the switching frequency of the prototype circuit varies from 1 kHz to 20 kHz, the band limited differentiator is designed to have a gain 1 at 1 kHz, linearly increasing and then flattening out to 14 at 20 kHz. This yields a total gain for the frequency dependent amplifier of 34 at 1 kHz, increasing to 470 at 20 kHz. The fixed gain filter can be tuned to remove dc offset of the pre-filter stage. The transfer function of the band limited differentiator is expressed as follows:

$$\frac{V_2}{V_1}(s) = \frac{C_1 R_2 s}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_1 + R_2 C_2)s + 1}. \tag{B.4}$$

Figure B-2 and B-3 show the magnitude and phase response of the band limited diffrentiator.

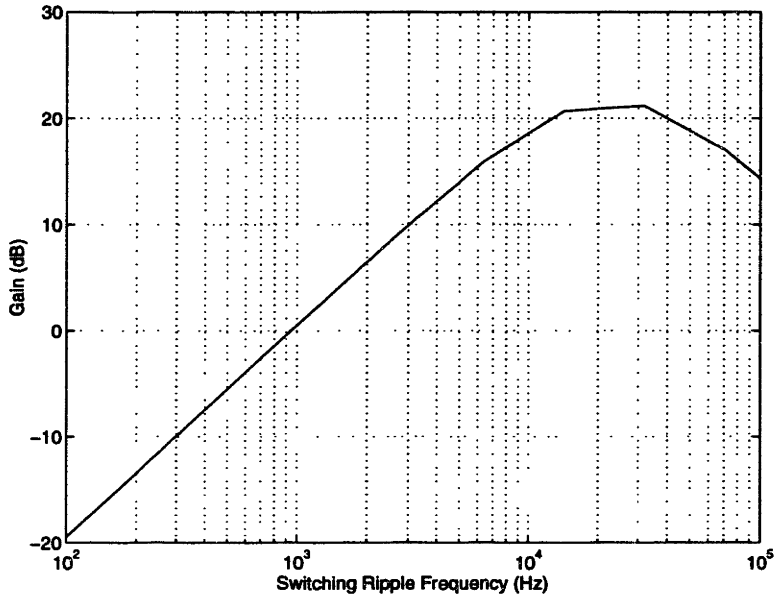

Figure B-2: Magnitude response of the band limited differentiator.

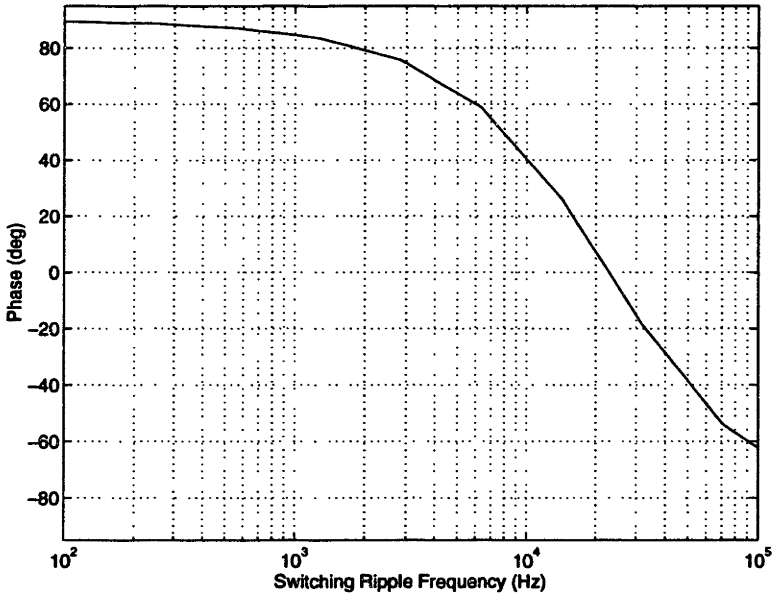

Figure B-3: Phase response of the band limited differentiator.

B.2 Voltage Controller

In the voltage controller, we employ a lag compensator to achieve sufficiently small steady-state error and stable system dynamics across the load range ,while remaining insensitive to switching frequency components in the output voltage. The transfer function of a lag compensator is expressed as follows:

$$H(s) = \frac{k(T_z s + 1)}{T_p s + 1} = \frac{i_{ref}}{V_{ref} - V_{out}} \tag{B.5}$$

where k, T_p and T_z are the dc-gain, the zero time constant and the pole time constant, respectively. The transfer function considering the voltage control loop of our prototype circuit shown in Fig. B-4 is deduced as follows:

$$V_{out} = \frac{R_{load}}{R_{load}C_f s + 1} i_{ref} = \frac{R_{load}}{R_{load}C_f s + 1} \frac{k(T_z s + 1)}{T_p s + 1}(V_{ref} - V_{out}). \tag{B.6}$$

Therefore, we can find the closed-loop transfer function from the reference voltage to the output as:

$$\frac{V_{out}}{V_{ref}}(s) = \frac{kR_{load}(T_z s + 1)}{R_{load}C_f T_p s^2 + (T_p + R_{load}C_f + kR_{load}T_z)s + kR_{load} + 1}. \tag{B.7}$$

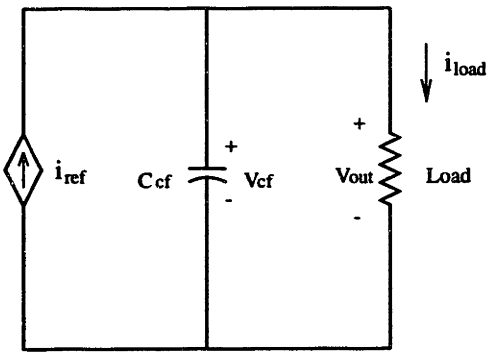

Figure B-4: Control model for the prototype circuit shown in Fig 3-1.

We chose $k = 0.16$, $T_p = 0.0159$ and $T_z = 0.00159$ for our system. Figure B-5

shows the magnitude response of the voltage control transfer function B.7 used in the prototype system at $R_{\text{load}} = 166\ \Omega$ (100% load). The magnitude response indicates that the control loop is relatively insensitive to inputs in the range of the switching frequency (from 1 kHz to 20 kHz). The steady-state error of the voltage controller is also small enough to be acceptable. At 100% load, the dc gain of B.7 is found to be

$$\frac{kR_{\text{load}}}{kR_{\text{load}} + 1} = 0.963 \tag{B.8}$$

yielding a maximum error of less than 4%.

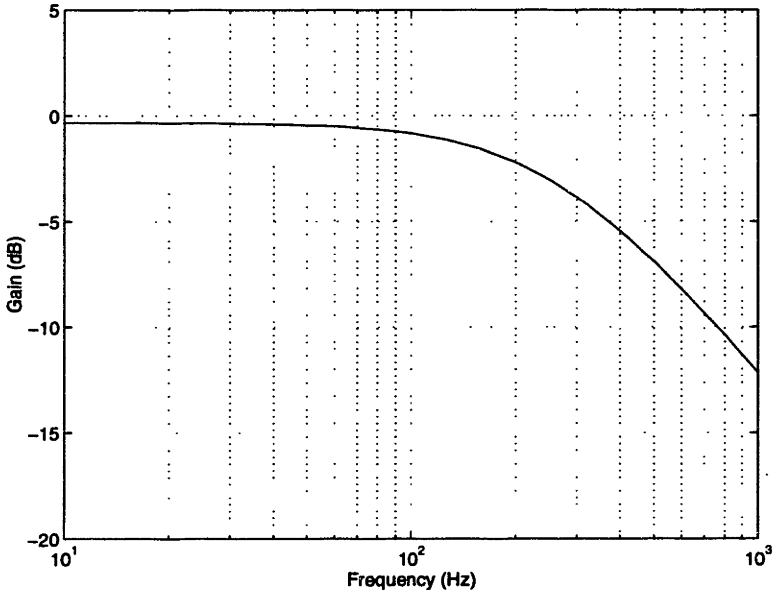

Figure B-5: Magnitude response of the voltage control loop of the prototype system at $R_{\text{load}} = 166\ \Omega$ (100% load).

In the practical circuit, the lag compensator is implemented by an operational amplifier as shown in Fig B-6.

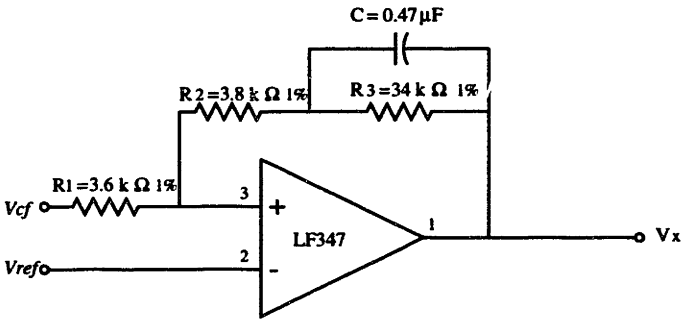

Figure B-6: Lag compensator in the voltage controller.

In the Laplace domain, the transfer characteristic of the circuit can be expressed as:

$$V_x(s) = V_{\text{ref}} + \frac{R_1 + R_2}{R_1} \frac{\frac{R_1 R_2 C}{R_2 + R_3} s + 1}{R_3 C s + 1} (V_{\text{ref}} - V_{\text{out}}). \tag{B.9}$$

Because the output voltage of this circuit, V_x, corresponds to the output current reference with a ratio such that 1 V represents 5 mA, k_c, the gain of the circuit is 200 times k. The parameters of B.9 are determined as follows:

$$k_c = k \times 200 = \frac{R_1 + R_2}{R_1} = 32 \tag{B.10}$$

$$T_z = \frac{R_1 R_2 C}{R_2 + R_3} = 0.00159 \tag{B.11}$$

$$T_p = C R_3 = 0.0159. \tag{B.12}$$

Although the first term of B.9 can be considered as an offset of the voltage controller, it is small enough (3% of the first term) compared with the second term and can be neglected.

B.3 Load Step Circuit

Figuer B-7 shows the schematic of the load step circuit used in section 4.5. This circuit changes the load resistance every 2.5 s.

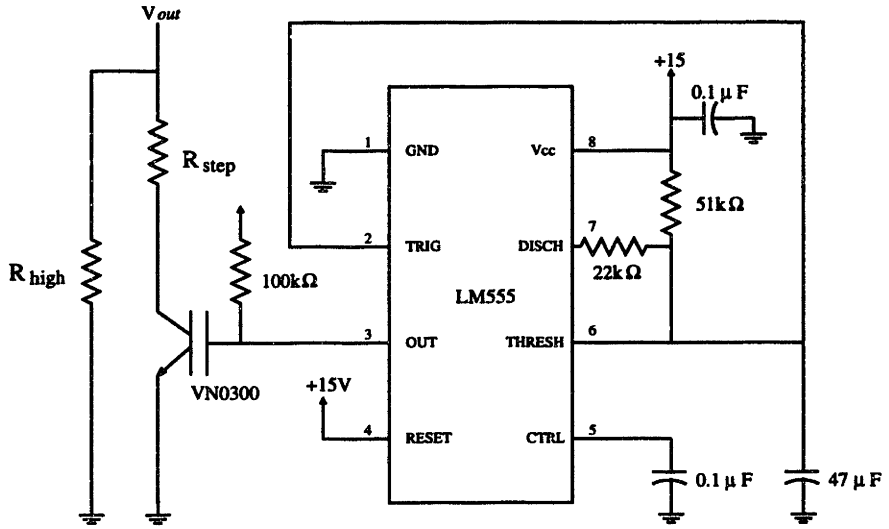

Figure B-7: Load step circuit used in Section 4.5.

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