# Enabling HF Power Conversion: Magnetic Components and a Wide Voltage Range Converter

by

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## Abstract

High frequency switching in power converters offers the benefits of high power density and faster transient response; however, high frequency losses have limited efforts to increase frequency into the HF (3–30 MHz) regime. This thesis addresses two of the dominant frequency-dependent loss mechanisms: magnetic material core loss and switching loss. Appropriate metrics are derived to evaluate magnetic materials in core loss limited components. A survey of material core loss shows the potential for significant performance improvement in the HF regime using materials previously overlooked in the power electronics community. One such material is then used in a high frequency converter which achieves zero-voltage switching over a wide range of voltages and powers (e.g. for grid-connected applications). Using appropriate magnetic materials and converter techniques like those presented here, power densities in certain applications can be improved by an order of magnitude by operating at HF.

Thesis Supervisor: David J. Perreault
Title: Professor

# Acknowledgments

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For all of this support, I am grateful.

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# Chapter 1

# Introduction

## 1.1 Background

**Power Electronics are a Bottleneck for Miniaturized Systems**

Energy delivery is a principal challenge of the modern world. Renewable energy sources require ever more sophisticated power electronic interfaces to handle their inherently variable, unreliable, and unpredictable nature. To better utilize the energy that is produced, electrical loads are becoming more demanding in terms of power factor, efficiency, and effective and fast sleep/wake modes. These loads are also increasingly mobile, both as transportable devices and as the transportation itself, making generated energy even more locally precious. As the capability of information electronics has exponentially expanded through Moore's law to consume less power, provide smarter functionality, and fit in the palms of our hands, their power electronic interfaces have become a primary bottleneck to further advancement.

This is not an accident. While a computer's 1s and 0s are essentially the same whether held on a cm-scale vacuum tube or on the gate of a nm-scale transistor, the energy temporarily stored in a power converter's inductors and capacitors is not. When packed into ever smaller volumes, energy-storing fields can cause losses, overheating, material breakdown, material saturation, nonlinearity, and other negative effects. Power electronic components resist concentrated energies.

Power electronics also tend to resist the high speeds demanded by modern loads.

Dynamic switch on-resistances, magnetic core losses, and even conductive wire resistances all increase (sometimes rapidly) with operating frequency. Parasitic reactances also become more prominent at higher frequencies which put limits on speed and complicate simulation, design, and control.

### High Frequency Offers Performance if Challenges are Overcome

Nevertheless, high operating frequency can be very useful. First, it allows power converters to react rapidly to changing source availability or load demand (e.g. a dormant processor core suddenly demanding full power) [1]. Second, high operating frequency fundamentally allows the use of smaller passive components which typically dominate converter volume and weight. At a basic level, this may be seen in the passive impedances: $Z_L = L\omega$ , $Z_C = 1/C\omega$: Increased frequency allows the use of smaller $L$ and $C$ values and, in turn, physically smaller components.

State-of-the-art switching frequencies for low-medium power, low-medium voltage converters extend to about 1 MHz. Some work has used frequencies over 30 MHz for very low voltage integrated applications and some higher power applications, but logic speeds limit available control techniques at this frequency and very high magnetic losses and parasitics make these kinds of converters difficult to implement. In between, there is a gap in the high frequency (HF, 3–30 MHz) range which potentially offers great opportunities for high density power conversion.

The challenge, then, is clear: how can the advantages of high frequency power conversion and small size be obtained while avoiding their negative repercussions? In this thesis, two approaches are taken to the solve this challenge. The first aims to improve power converter components, specifically magnetic components, through a materials and design investigation. The second aims to provide, at the converter level, a topology and design framework suitable for high frequency operation. It should be noted that these are two contributions to a larger community effort which includes improvements to other components, topologies for different applications, and system-level holistic design – these efforts are very valuable, but outside the scope of this work.

## 1.2 High Frequency Magnetic Materials and Components

### Power Magnetics Loss Inhibits Size and Frequency Scaling

Magnetic components for power electronics typically consist of one more more windings around a ferromagnetic core. By Ampère's law, current through the windings generates a magnetic flux in the core. Through the magnetic flux and Faraday's law, energy may be transferred to a second winding or stored temporarily and extracted via the same winding. The isolation, voltage/current transformation, and energy storage functions of magnetic components are critical to most power converters; nevertheless these useful components can be problematic, for two reasons. First, they often dominate the size and weight of power converters (usually setting the converter height and occupying ~30-50% of converter PCB area). Second, magnetic component losses are often high and increase rapidly with frequency, resisting that route to miniaturization.

The reason for both of these difficulties may be seen in the Steinmetz equation (1.1), a simplified but useful empirical expression for the core loss in a magnetic component. The power loss per unit volume $P_V$ is expressed as a function of frequency $f$ and peak magnetic flux density $B_{pk}$

$$P_V = k f^{\alpha} B_{pk}^{\beta} \tag{1.1}$$

where $k$, $\alpha$, and $\beta$ are the Steinmetz parameters, material constants with appropriate units. Both $\alpha$ and $\beta$ are close to 2 (over a finite range), with $\alpha$ usually somewhat smaller and $\beta$ usually somewhat larger. As magnetic flux is packed into a smaller volume ($B_{pk} \uparrow$) and as frequency increases ($f \uparrow$) power losses quickly result in either unacceptable efficiencies or temperatures.

### Low Permeability Materials Offer High HF Performance

For power magnetic materials at up to a few megahertz, Steinmetz parameters

are published on the material datasheets. However, these data have not been available for higher frequency materials due to both technical and economic factors (see Section 2.1). This has rendered optimized design of cored power magnetic components (i.e. with proper performance tradeoffs) impossible in the HF regime. To open up this design space, we measure and report Steinmetz parameters for a collection of materials suitable for HF operation but previously lacking loss data. To make this possible we use a resonant measurement technique, very different from traditional methods, which provides suitable accuracy at HF (see Appendix B). The data gathered is useful both for design with particular materials and for surveying the materials landscape. This survey reveals the potential for ~45% improvement in magnetic component power density by increasing frequency from a typical ~500 kHz design to about 10 MHz by using commercially available materials that have not been widely used for power conversion applications.

Additionally, we find that materials suited to HF operation have lower permeability ($\mu_r \approx 20-200$) than materials typically used for power inductors and transformers at more conventional frequencies ($\mu_r \approx 800-2000$). These materials will require new design paradigms to accommodate or even take advantage of their non-negligible core reluctances and incomplete flux guidance. In this thesis, we begin this work by demonstrating theoretically and experimentally that low permeability does not present a fundamental obstacle to high performance.

Therefore, we will show that

1. there are commercially available magnetic materials with useful material properties for power magnetics in the HF regime,

2. the advantages of HF operation outweigh the costs in terms of magnetic component performance, and that

3. low permeabilities common to HF magnetic materials need not fundamentally limit component performance.

See [2, 3] for peer-reviewed publication arising from this work on magnetic materials and components.

## 1.3 A High Frequency Wide Input Voltage Converter

### New Components Extend HF Converter Application

Many converter components are becoming more suitable for high frequency operation. Through this work, the opportunities for HF magnetic components have been expanded. Modern ceramic capacitors with low loss are available to hundreds of MHz and beyond, and with continued evolution fo semiconductor processes and design, control circuitry continues to operate at higher speeds with more functionality for less power. Wide band gap semiconductor switches based on gallium nitride (GaN) and silicon carbide (SiC) can switch faster than silicon devices at a given voltage/power due to lower capacitance, higher electron mobility, and majority-carrier physics. In order to take full advantage of high performance components, new topologies and approaches to HF design are necessary at the circuit level to realize highly dense and efficient systems.

In particular, the development of 650 V GaN FETs raises the possibility of implementing universal input (120–265 VAC) grid-connected converters in the HF range. Previous converters have required slow high voltage Si switches or complex stacked topologies to reduce voltage stress on GaN switches.

### HF Converters Offer High Performance at Higher Voltage/Power

High frequency operation has challenges that must be met at the circuit level in addition to the component level. For example, switching losses increase rapidly with both voltage and frequency. All real circuit nodes have parasitic capacitance. When a switch turns on with some voltage across its parasitic capacitor, the capacitor is discharged, and the energy is lost. Although the energy is dissipated in a resistive transient $V-I$ overlap, the total energy lost is not a function of the switch resistance value or the switching time. A similar effect is seen in short-circuit charging, which yields a total $f \cdot CV^2$ power loss. This effect can be avoided through circuit techniques that allow switches to turn on with zero potential across them (zero-voltage-switching

or ZVS). Achieving ZVS at high frequency and high voltage is essential to maintaining thermal and efficiency limits.

As a vehicle for exploring efficient HF converters, we present the design and performance results for a wide-range resonant-transition converter suitable for application in (for example) universal input power factor correction (PFC) stages. Such PFC stages are placed after a grid-connected diode bridge and are designed to draw input current proportional to input voltage, thereby most effectively utilizing the ac grid without corrupting it. Such a PFC converter acts as a rectifier (ac-dc converter), but since the input varies slowly relative to the switching frequency (by roughly five orders of magnitude), it may be considered a dc-dc converter with wide input voltage range. All experimental results will be reported at dc with the understanding that, in full operation, a feedback loop would shape the input current waveform along a line cycle.

## 1.4 Impact

We expect the results of this thesis to be broadly applicable outside of the academic sphere. As the power electronics community moves to implement higher switching frequencies, design of both components and converters will rely on results like these to inform future work and products in industry. Magnetic material data gathered here will be necessary to implement optimized HF inductors and transformers. Additionally, circuit topologies and techniques like those presented here will be critical to achieving HF (and therefore miniaturized) converters that do not succumb to HF loss mechanisms.

Superior power converters will enable greater penetration of renewable energy through flexibility and efficiency improvements, longer battery lives for portable devices, and more intelligent distribution of energy. Relieving this bottleneck will be important in both the near and over the long term.

# Chapter 2

# HF Magnetic Materials and Components

## 2.1 Background

### Unified Circuit and Component Design Minimizes Magnetics Size

Magnetic components are typically the largest and most lossy components in power converters [4]. Their size is not primarily limited by manufacturing capability or modeling barriers (as has been the case for information processing devices), but rather by fundamental physics. A small magnetic component has less area over which to divide core flux ($B \uparrow$) and less area over which to divide winding current ($J \uparrow$) while still providing the same inductance and processing the same current/power. Therefore, both core and winding loss increase as a component shrinks. Efficiency and thermal constraints prevent designers from continuing this process indefinitely, and magnetic components for power applications are constrained to a minimum size which typically is much larger than most other components (switches, control circuitry, capacitors with similar energy storage) [1]. Scaling of magnetic components is inherently challenging [5].

Three principal strategies have been adopted to decrease the size of magnetic components.

1. Reduce the required inductance value through circuit design
2. Reduce the required power/current processing through circuit design
3. More fully utilize the available volume through advanced geometries and material selection

The required inductance value may be decreased by first examining the inductor circuit constitutive relation, $v_L = L\frac{di_L}{dt}$. The required inductance value can principally be reduced by allowing the inductor current to have large swing ($di_L \uparrow$) as in resonant or DCM converters, or by increasing the frequency of operation ($dt \downarrow$).

The required power/current processing can be managed through topological choices that reduce required energy storage and/or divert more of the energy storage requirements to other components (typically capacitors). The extreme end of this process is the switched capacitor (SC) power converter, which uses no magnetic components at all. In a way, such circuits fail to take advantage of the dual nature (voltage and current) of electrical energy and have some severe shortcomings. Modern *resonant* switched capacitor circuits attempt to correct for these disadvantages by reintroducing small magnetic components into the circuit while achieving the majority of the energy storage in capacitors.

Finally, component design has advanced to more fully take advantage of available component volume. Such efforts include thinner insulation on wires, litz wire that more fully utilizes the copper area even at high frequency, 3D printing to optimally cover the whole core surface [6], and the use of printed circuit board (PCB) traces as the component windings for volume sharing and better thermal dissipation. This category also includes materials research into reducing losses, from laminating iron cores to the use of high resistivity ceramic ferrites and powdered-iron cores.

For a given power handling, a magnetic component for high density applications will often have large current swings ($i_{L,ac} \gtrsim I_{L,dc}$), operate at high frequency, and will rely on advanced design approaches.

**Frequency Scaling is Limited by Magnetics Loss**

There are limits to the techniques mentioned above. The current swing cannot be greater than that of an ac inductor which carries no dc current. From a component design perspective, some component design techniques either offer only marginal benefit (e.g. 3D printed windings) or are fixed (e.g. material availability). This leaves little room for improvement.

The remaining approach, frequency scaling, rapidly increases several sources of magnetics loss (and converter loss, see Chapter 3). Limitations on frequency not only limit the density of power stage components, but severely limit the density of elements like EMI filters which are not themselves limited by loss but could be made smaller with higher corner frequency requirements. It is possible to mitigate HF losses and access the benefits of high frequency operation by understanding the sources of HF loss.

*Skin Effect:* A current carrying wire generates a magnetic field, even inside the wire itself. If the current is changing, the changing magnetic field will induce an EMF and hence eddy currents within the wire so as to oppose the change in flux. These currents tend to reinforce the current carried near the edge ("skin") of the wire and cancel the current carried in the center. Current, as a function of depth, is an exponentially decaying function with a characteristic length $\delta = \sqrt{\frac{\rho}{\pi \mu f}}$, known as the skin depth. The net effect is that, for wires significantly larger than a skin depth, current is only carried near the surface ("only within a skin depth"), greatly increasing the effective resistance of the wire.

This effect can be mitigated through the use of flat conductors with high surface area to volume ratios or many small strands of individually insulated wire. The latter, when woven/structured to provide good current sharing among the strands, is known as litz wire (from the German *litzendraht*, woven or braided wire) [7, 8].

*Proximity Effect:* Eddy currents may also be induced in a wire due to other sources of magnetic field, typically other nearby wires. In particular, in a multilayer winding structure, the leakage field that must exist between each layer to satisfy Ampere's law increases with the number of layers, and the ratio of high frequency loss to dc loss increases as roughly the square of the number of layers [9–11]. This effect limits

the applicability of using many (thin) parallel conductors, which effectively build up to a many layer structure. The specific weaving pattern of litz strands effectively mitigates this problem, though multiple layers of litz wire still incurs a proximity effect penalty.

The analysis of proximity effect can quickly become very complicated and the reader is referred to standard texts for reference [7, 9, 11]. It suffices to say that the proximity effect increases with frequency and strongly limits the number of layers of conductor that can be used.

Like the skin effect, the proximity effect can be reduced if the conductors are thin compared to a skin depth. In multi-winding components, primary and secondary windings may also be interleaved such that their opposing currents reduce the net fields $H \propto \sum i$ seen by other conductors.

It should be noted that the mitigation techniques listed above are limited. The skin depth in copper at 10 MHz is 20.6 µm, which is 34 % thinner than 48 AWG wire (roughly the economical limit of individual litz strands), whereas the inverse relationship would be closer to ideal. Even if it were available, such litz wire consumes space in insulation, limiting the window area available for copper. Interleaving transformer primary and secondary turns has a similar effect, but is challenging as every insulating layer (rather than just one) must be rated to for the full isolation voltage rather than the inter-turn voltage.

*Core Loss:* The magnetic core which is used to guide flux and increase inductance (or magnetizing inductance in the case of a transformer) also has losses associated with alternating magnetic fields. Some of these losses are due to hysteresis in the core B-H loop (note that $[B \cdot H]$ = energy, such that the area of the B-H loop is the energy lost per cycle). This hysteresis derives from fundamentally quantum mechanical phenomena which are beyond the scope of this thesis. Nevertheless, the core concept is that microscopic dipoles flip their orientation irreversibly, creating local eddy currents which induce loss. Another component of the loss derives from the macroscopic eddy currents induced in a conducting magnetic core. For this reason, highly conductive iron cores are laminated into magnetically permeable but electri-

cally insulated sheets; high resistivity ferrites suffer less from this effect, but are not immune. Finally, core loss has a component which has frequently been called the "anomalous loss," though there is very little anomalous about it – it is simply a frequency-dependent modification to the so-called "static" hysteresis loss (indeed, the B-H loop expands as frequency increases). As such, it has also been called the "excess eddy current loss" [12]. It should be noted that the fundamental loss mechanisms are, physically, all eddy current losses. The only distinction is the source and scale of interest.

The net effect is a loss which is very difficult to predict from first principles. Even the frequency dependence is uncertain: on a per-cycle basis, the "static" hysteresis loss is independent of frequency, the classical eddy current loss is proportional to frequency, and the "anomalous" loss is frequently unknown.

### Loss Data is Not Available at HF

A more useful approach to core loss is empirical, with the model from Section 1.2 re-written in (2.1) in the form originally conceived by Steinmetz in 1892 [13]:

$$P_V = k_f B_{pk}^{\beta_f} \quad . \tag{2.1}$$

Here there is no explicit frequency dependence; rather, there are different $k_f$ and $\beta_f$ values for each measured frequency. Listing Steinmetz parameters as different values at distinct frequencies ($k_f$,$\beta_f$), rather than as functions of frequency($k(f)$,$\beta(f)$) is the convention most commonly followed in industry and the literature. This formulation recognizes that loss is *not* proportional to $f^\alpha$ across a broad range of (especially high) frequencies.

This approach, while tractable, requires empirical core loss data across the range of frequencies of interest. Measurement of core loss can be tedious and error-prone, leading most designers to rely on data provided by the material manufacturer. Unfortunately, core loss data is only available below ~1 MHz [14], for a few reasons. The first is that core loss is difficult to measure at HF. The (very expensive) equipment

that manufacturers use to automate this process uses a technique that is only accurate at lower frequencies [15]. Measuring core loss at HF would require both an investment in expertise about advanced measurement techniques and an investment of time in the tedious measurement process for which no automated equipment currently exists. There is also little incentive to make such an investment; most power electronics markets have designs below ~1 MHz, and most materials that might be appealing for HF power conversion are typically marketed for signal conditioning applications where large-signal core loss is not considered an important parameter.

Nevertheless, the data that is currently available indicates some promise in the HF regime. Figure 2-1 shows the state of the art prior to the research presented here. The data is presented in terms of performance factor [16–25] (explained in detail in Section 2.2) which is a figure of merit expressing the power handling capability per unit volume and is effectively a material property. The data from Ferroxcube (a leading manufacturer) is taken as representative of typical power magnetic materials. Each point in this curve represents the highest performing material at that frequency. Also listed is data from several VHF materials from the academic literature.

It can be seen that, generally, increasing frequency increases the available power handling density of a component (assuming appropriate material selection), consistent with the logic presented earlier. However, at VHF, available data points to a negative trend with respect to frequency as core losses overtake the advantages of smaller required inductance values. Two motivating conclusions can be drawn from Figure 2-1. First, there is a lack of data in the HF range, making it difficult to design optimized power magnetic components in that range. Second, it may be hypothesized from the trends in Figure 2-1 that HF magnetic materials would outperform their lower- or higher-frequency counterparts. Data gathered in this thesis will show that this is indeed the case.

### Material Figure of Merit Ignores HF Winding Losses

The performance factor rests on several assumptions about magnetic component design. Among these is the assumption that winding loss is not a function of fre-

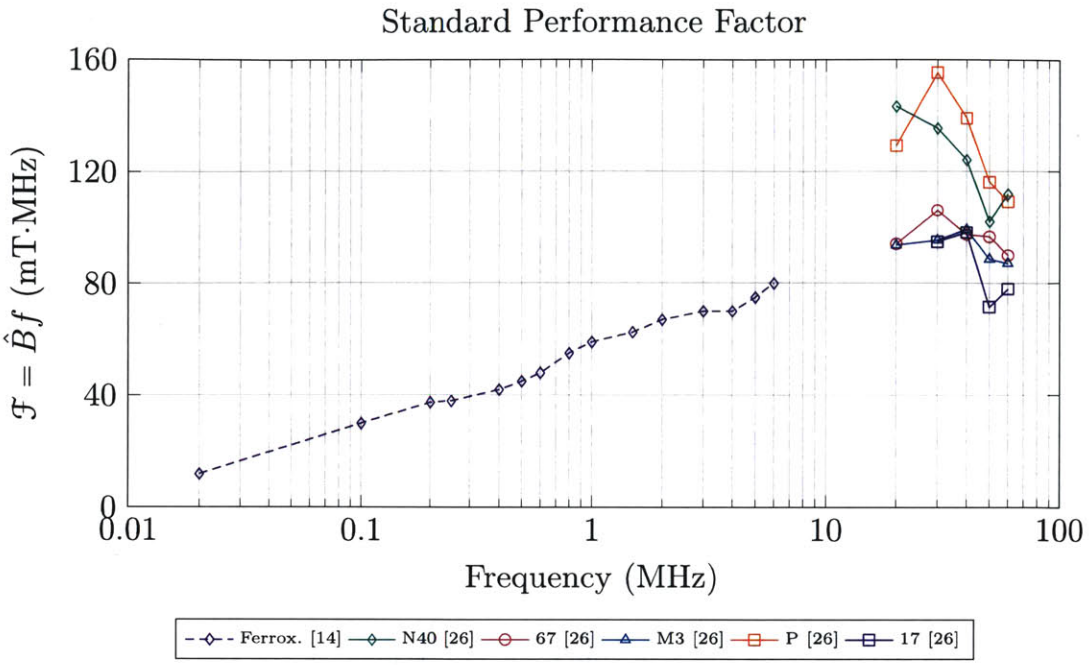



Figure 2-1: Material performance state of the art prior to this work (explanation, etc.)

quency. At HF (indeed, even at MF), this is nearly never the case due to the proximity and skin effects. As such, we first investigate modifications to the concept of performance factor in Section 2.2. Based on more realistic assumptions about HF component design, we arrive at a modified performance factor which takes into account HF winding losses. This modified performance factor is then used to survey magnetic loss data to determine an appropriate operating regime for high density magnetic components. We find that HF operation, with appropriate materials, offers a significant performance increase over lower frequencies (even with the more realistic modified performance factor).

## 2.2 Performance Factors and Modeling

Magnetic component design involves many controllable parameters and hence complex tradeoffs that make optimization difficult. Figures of merit are devised to simplify the design process, allowing for rapid convergence on approximately optimal designs.

One such figure of merit is the performance factor $\mathcal{F}$ which is meant to reflect the power handling per unit volume of a given material [16–25]. As such, it is related to the achievable power density of a component, and hence of a converter. The larger the performance factor $\mathcal{F}$, the more dense a component can be for a given function and loss. With the performance factor, a designer can compare materials against each other across frequency [14].

The performance factor is derived by considering the voltage across and the current through a magnetic component. The voltage across the component is given by $V = \left|\frac{d\phi}{dt}\right|$. For a sinusoidal drive, this is $V = NA_C\hat{B}\omega\sin(\omega t) \propto A_C\hat{B}f$. It can immediately be seen that the voltage relates directly to the frequency and flux density in the component, both of which contribute to core loss. Thus at increased frequency the allowable flux density peak must be lower (or vice-versa). A low loss component will allow larger flux densities for a given frequency or higher frequencies for a given flux density, and hence will have a higher voltage handling.

The current handling for a component may likewise be related to the current density handling of the windings. While not a reflection of the core material itself, winding losses may discount the attractiveness of high frequency operation for a component. Nevertheless, the traditional performance factor $\mathcal{F}$ assumes that the current handling of the windings, the maximum ampere-turns or $NI$, is independent of frequency (i.e. negligible or mitigated skin and proximity effect). Likewise, it is assumed to be independent of the flux density in the core. Thus the relevant current handling proportionality is $I \propto l_c f^0$, where a longer core length allows for proportionally wider windings and hence more current. The frequency component is explicitly included for later modification.

A power (or "VA") handling may be defined as the product of the voltage and current handling for the component. Thus $\text{VA} = V_{pk}I_{pk} \propto (A_C\hat{B}f)\cdot(l_c f^0)$, where the proportionality is meant to isolate fundamental aspects of the core and frequency of operation. The performance factor is the power *density* achievable by the core ($\mathcal{F} \propto \frac{\text{VA}}{A_C l_c}$), and so

$$\mathcal{F}_1 = \hat{B} f^1 \tag{2.2}$$

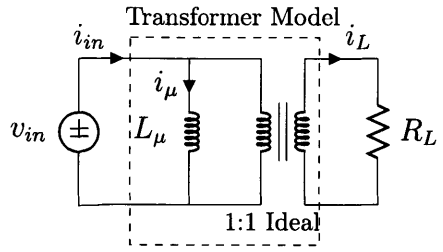
where the explicit 1 in both the subscript of $\mathcal{F}$ and the exponent of $f$ will distinguish the standard performance factor $\mathcal{F}_1$ from its modified counterpart.

It should first be noted that the value of the performance factor depends on the allowable loss level chosen: the core flux $\hat{B}$ is chosen to be that which provides the specified core loss density at the frequency of interest. Typical core loss values are $200\,\mathrm{mW\,cm^{-3}}$ (conservative), $300\,\mathrm{mW\,cm^{-3}}$ (typical), or $500\,\mathrm{mW\,cm^{-3}}$ (with aggressive cooling or high surface area). For notational simplicity, this parameter is usually stated or assumed in context and is omitted from the performance factor expression $\mathcal{F}_1$.

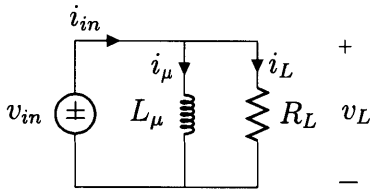
In order to calculate the performance factor, a loss level is first chosen. Then, for any frequency, the maximum sinusoidal flux density amplitude that results in the chosen loss level is found from empirical data or Steinmetz parameters. This flux density is the quantity $\hat{B}$. The product $\hat{B} f^1$ for a given material, plotted against frequency, is a curve which typically rises (as high frequency allows smaller components), peaks, and then falls (as core loss overtakes any high frequency advantage). A material maximizes its power handling density at a particular frequency; thus it is sensible to speak of "low frequency materials" or "high frequency materials" as those which are best utilized and hence "belong" in those regimes.

### Transformer Derivation

The relationship between the performance factor and the power handling of a component may be illustrated in the simple case of a 1:1 transformer driving a resistive load (Fig. 2-2). Let the peak magnetic flux density be limited to $\hat{B}$ in accordance with some loss limit. This will relate to the voltage handling of the transformer. Further, let the surface current density in the windings be limited to $\hat{K} = NI_{in}/l_c$. This will relate to the current handling of the component. The average power delivered to the




(a) Transformer circuit with transformer model.




(b) Simplified Transformer Circuit

Figure 2-2: Transformer circuits used to examine achievable power density and its relationship to performance factor and permeability.

load is given by

$$P_{del} = \frac{1}{2} V_{out} I_{out} \tag{2.3}$$

where capital symbols such as $V_{out}$ and $I_{out}$ represent the peak of the load voltage and current waveforms. The peak load voltage is limited by the allowed magnetic flux density induced in the magnetizing inductance. The relationship is given by Faraday's law:

$$V_{out} = V_{in} = \omega N A_c \hat{B} \tag{2.4}$$

The load current is related to the total current by

$$I_{out} = \sqrt{I_{in}^2 - I_\mu^2} \tag{2.5}$$

where $I_\mu = V_{in}/(\omega \mu L_\mu)$ is the peak current through the equivalent magnetizing inductance.

Thus the power deliverable to the load with constraints on magnetic flux density

and surface current density is given by

$$P_{del} = \frac{1}{2} V_{out} I_L = \frac{1}{2} \omega N A_c \hat{B} \sqrt{\left(\frac{\hat{K} l_c}{N}\right)^2 - \left(\frac{l_c \hat{B}}{N\mu}\right)^2} \tag{2.6}$$

This can be rearranged and expressed in power per unit core volume as:

$$\frac{P_{del}}{A_c l_c} = (\pi \hat{K})(\hat{B} f) \sqrt{1 - \left(\frac{\hat{B}}{\hat{K}\mu}\right)^2} \tag{2.7}$$

where the volumetric power handling is shown proportional to the performance factor $\mathcal{F}_1 = \hat{B} f^1$. The effect of frequency dependent current handling $\hat{K}(f)$ will be discussed in the next section. Core permeability (usually assumed to be large) also plays a role in (2.7). Its impact for low-permeability materials is considered in Section 2.5.

### Modified Performance Factor

The transformer example suggests that the performance factor can be modified to include high frequency winding effects by changing the expression for $\hat{K}$. The most common scenario would be to include only skin effect at HF, as single-layer windings are used to avoid proximity effect losses and litz wire is unlikely to compensate for small skin depths. To maintain fidelity to the winding same loss $I_{rms}^2 R_{eff}$, as the effective resistance increases with frequency ($R_{eff} \uparrow$), the current handling must decrease ($I_{rms} \downarrow$) to maintain constant loss. Since skin-effect resistance increases with $\sqrt{f}$, current handling must decrease as $f^{-\frac{1}{4}}$. The current density limit $\hat{K}$ can then be expressed as $\hat{K} = K_0 f^{-\frac{1}{4}}$. The derivation of the performance factor follows as before, resulting in the modified performance factor:

$$\mathcal{F}_{3/4} = \hat{B} f^{\frac{3}{4}} \quad . \tag{2.8}$$

The original performance factor could be modified to account for different assumptions than for a single layer winding. However, these other modified forms are less likely in practice at HF, and are therefore considered in Appendix A. For the remainder of

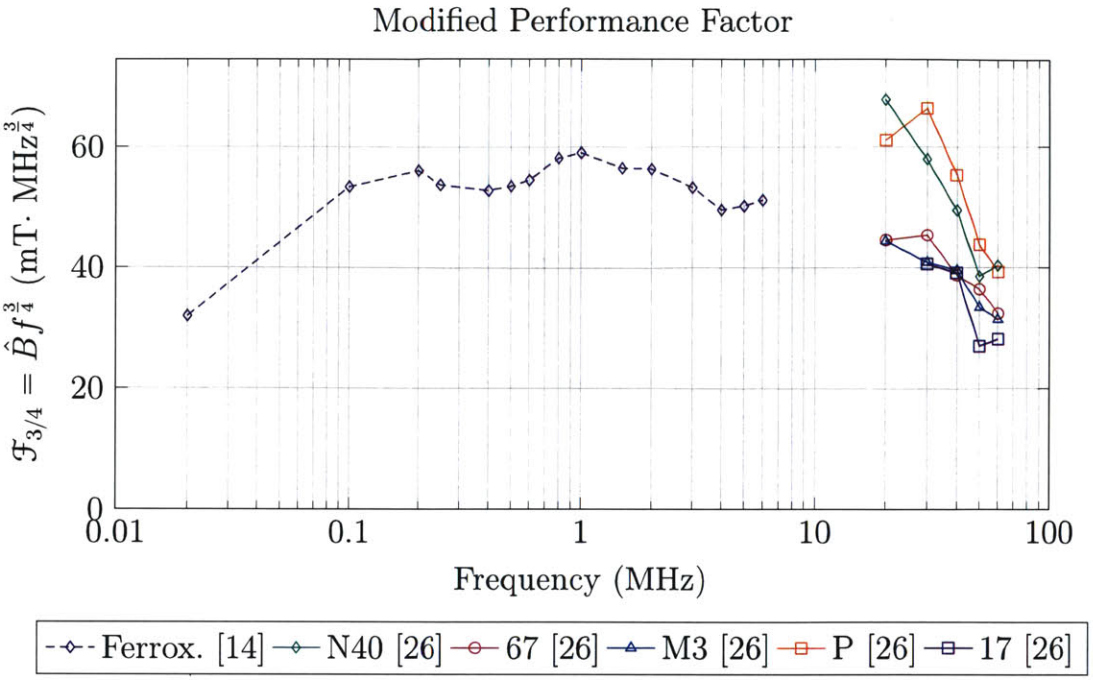



Figure 2-3: Survey of modified performance factor, incorporating data from industry, the literature, and this work.

this thesis, the term "modified performance factor" will refer to $\mathcal{F}_{3/4}$.

From (2.8), it is clear that the modified performance factor discounts the benefit of high frequencies. Whether this makes HF attractive or not, as with the standard performance factor, depends on empirical data of available materials. To illustrate this, compare the standard performance factor calculated from existing data (Fig. 2-1) with the modified performance factor calculated from the same data (Fig. 2-3). The effect of the $f^{-1/4}$ factor is clearly evident, showing that the modified performance factor remains roughly constant throughout the MF regime. However, extrapolating backwards from the VHF data clearly suggests that HF materials have the potential for very high performance.

## 2.3 Core Loss Data Gathering

As discussed in the background, core loss data is lacking for HF materials. Some VHF data exist from academic sources only [26] and, by those frequencies, shows a

rapid decline in performance. Available data in Figures 2-1 and 2-3, however, suggests that HF materials may achieve higher power density than both their MF and VHF counterparts.

Using the method described in Appendix B and [26], we measured core loss characteristics for 20 materials from a variety of manufacturers. Materials were chosen based on complex permeability – stable real parts and low imaginary parts into the HF regime were considered candidates for experiment[1]. Core loss measurements were made under free convection for a set of discrete frequencies and at sufficiently many values of $B_{pk}$ to fit a curve based on the Steinmetz equation (2.1) (empirical data conforms strongly to this model, so only a handful of data points are necessary to curve fit at a given frequency). While core loss data is frequently reported graphically in manufacturer datasheets (as in Figure 2-4), it may be represented more compactly by Steinmetz parameters alone. We report our experimental data in this format in Table 2.1. We also reproduce, for completeness, data from [26] in Table 2.2 in the same manner.

### Applicability of Data

Several factors influence the applicability of the data in Table 2.1. These are considered in Appendix C.

## 2.4 Performance Factor Analysis and Comparison

The core loss data in Table 2.1 is used to calculate both the standard performance factor $\mathcal{F}_1$ and the modified performance factor $\mathcal{F}_{3/4}$, using a loss density of $P_v = 500\,\mathrm{mW\,cm^{-3}}$. The data is presented in Figures 2-5, 2-6 along with previously available data.

Generally, it can be seen that the maximum performance factor of available materials increases roughly as $\sqrt{f}$ between 20 kHz and 100 kHz, indicating that increased

[1]This selection method is only a heuristic, as small-signal measurements like complex permeability do not accurately account for large-signal behavior. Nevertheless, this method helps narrow a very wide field to promising candidate materials.

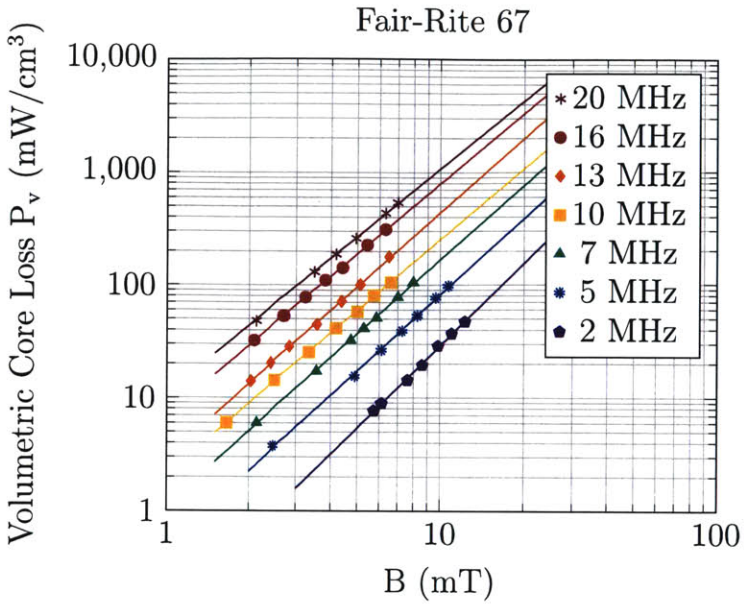



Figure 2-4: Core loss data from Fair-Rite 67 as a sample material suitable for HF operation. Fair-Rite 67 has a nominal relative permeability $\mu_r = 40$.

Table 2.1: Steinmetz parameters measured in this work for commercially available materials at HF, $P_v = k \times B^{\beta}$, where $P_v$ is in mW/cm$^3$ and B is in mT; valid for $P_V < 1000\,\mathrm{mW/cm^3}$.

| Frequency→ | | 2 MHz | | 5 MHz | | 7 MHz | | 10 MHz | | 13 MHz | | 16 MHz | | 20 MHz | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Material | $\mu_r$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ |
| Ceramic Magn. C2010 [27] | 340 | 0.20 | 2.89 | 2.61 | 2.56 | 10.61 | 2.23 | 22.23 | 2.29 | 51.55 | 2.04 | - | - | - | - |
| Ceramic Magn. C2025 [27] | 175 | 0.49 | 2.67 | 3.14 | 2.58 | 11.33 | 2.27 | 30.15 | 2.20 | - | - | - | - | - | - |
| Ceramic Magn. C2050 [27] | 100 | 0.52 | 2.9 | 2.47 | 2.75 | 5.25 | 2.76 | 12.44 | 2.50 | - | - | - | - | - | - |
| Ceramic Magn. C2075 [27] | 50 | - | - | 2.31 | 2.77 | 3.42 | 2.77 | 5.81 | 2.76 | 11.88 | 2.69 | 20.67 | 2.61 | 19.57 | 2.45 |
| Ceramic Magn. CM48 [27] | 190 | 0.59 | 2.68 | 7.49 | 2.33 | 21.5 | 2.17 | 80.01 | 2.05 | - | - | - | - | - | - |
| Ceramic Magn. CM5 [27] | 290 | 0.61 | 2.66 | 9.42 | 2.29 | 22.55 | 2.19 | 42.04 | 2.08 | - | - | - | - | - | - |
| Ceramic Magn. N40 [27] | 15 | - | - | 1.52 | 2.09 | 3.04 | 2.00 | 6.61 | 2.01 | 11.09 | 2.02 | 12.47 | 2.06 | 21.20 | 2.04 |
| Ceramic Magn. XCK [27] | 210 | - | - | 1.07 | 2.75 | 4.86 | 2.44 | - | - | - | - | - | - | - | - |
| Ceramic Magn. XTH2 [27] | 80 | - | - | 0.83 | 2.82 | 1.72 | 2.72 | 3.86 | 2.68 | 7.07 | 2.57 | 15.20 | 2.57 | 42.00 | 2.38 |
| Fair-Rite 52 [28] | 250 | 0.46 | 2.97 | 5.44 | 2.53 | 14.44 | 2.32 | - | - | - | - | - | - | - | - |
| Fair-Rite 61 [28] | 125 | 0.08 | 2.79 | 0.42 | 2.67 | 0.83 | 2.62 | 1.80 | 2.56 | 4.31 | 2.47 | 6.66 | 2.53 | - | - |
| Fair-Rite 67 [28] | 40 | 0.10 | 2.44 | 0.69 | 2.20 | 1.11 | 2.18 | 2.09 | 2.08 | 2.91 | 2.18 | 6.06 | 2.04 | 10.95 | 1.99 |
| Fair-Rite 68 [28] | 16 | - | - | - | - | - | - | 3.92 | 2.2 | - | - | 11.71 | 2.08 | 22.67 | 1.96 |
| Ferroxcube 4F1 [14] | 80 | 0.15 | 2.57 | 1.11 | 2.27 | - | - | 2.86 | 2.28 | 6.53 | 2.09 | 10.89 | 2.05 | 23.20 | 2.14 |
| Metamagnetics HiEff 13 [29] | 425 | 0.11 | 3.06 | 10.44 | 2.10 | 12.69 | 2.32 | - | - | - | - | - | - | - | - |
| Micrometals 2 [30] | 10 | - | - | - | - | - | - | 10.97 | 2.09 | 19.32 | 2.07 | 28.79 | 2.04 | 57.09 | 2.00 |
| National Magn. M [31] | 125 | 0.03 | 3.36 | 0.45 | 2.83 | 1.35 | 2.69 | 2.52 | 2.57 | 5.23 | 2.56 | - | - | - | - |
| National Magn. M2 [31] | 40 | - | - | 0.41 | 2.44 | 0.69 | 2.36 | 1.45 | 2.3 | 2.85 | 2.18 | 5.39 | 2.13 | 12.58 | 2.07 |
| National Magn. M3 [31] | 20 | - | - | 0.85 | 2.10 | 1.66 | 2.03 | 2.55 | 2.05 | 4.87 | 1.95 | 7.54 | 2.01 | 14.44 | 1.98 |
| National Magn. M5 [31] | 7.5 | - | - | - | - | 90.34 | 2.14 | 147.6 | 2.17 | 198.3 | 2.21 | 225.1 | 2.12 | 335.1 | 2.15 |

Table 2.2: Steinmetz parameters measured in [26] (reproduced here for completeness) for commercially produced materials at VHF, $P_v = k \times B^{\beta}$, where $P_v$ is in $mW/cm^3$ and B is in mT; valid for $P_V < 1000\,mW/cm^3$.

| Frequency→ | | 20 MHz | | 30 MHz | | 40 MHz | | 50 MHz | | 60 MHz | | 70 MHz | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Material | $\mu_r$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ | k | $\beta$ |
| National Magn. M3 | 20 | 0.0008 | 3.46 | 0.0068 | 3.24 | 0.191 | 2.45 | 1.03 | 2.15 | 1.76 | 2.11 | - | - |
| Ferronics P | 40 | 0.036 | 2.29 | 0.051 | 2.33 | 0.218 | 2.18 | 0.696 | 2.09 | 1.34 | 2.04 | - | - |
| Fair-Rite 67 | 40 | 0.142 | 2.12 | 0.210 | 2.18 | 0.740 | 2.04 | 1.150 | 2.05 | 2.40 | 1.97 | - | - |
| Ceramic Magn. N40 | 15 | 0.0364 | 2.23 | 0.227 | 2.02 | 0.518 | 2.00 | 0.208 | 2.58 | 0.690 | 2.25 | - | - |
| Micrometals 17 | 4 | - | - | 0.0361 | 2.76 | 0.0825 | 2.72 | 1.860 | 2.10 | 1.95 | 2.16 | 2.35 | 2.22 |

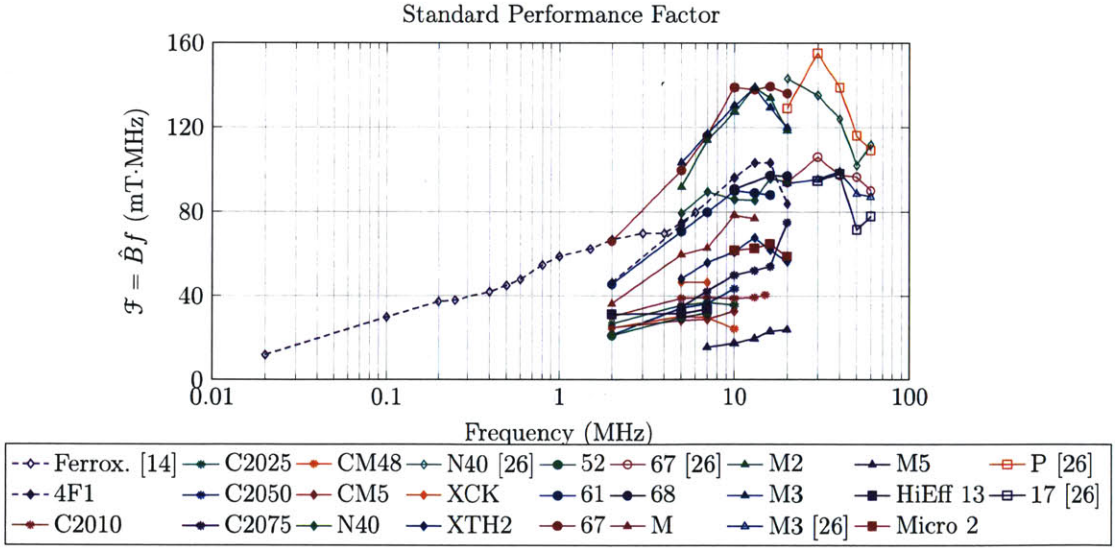



Figure 2-5: Survey of standard performance factor, incorporating data from industry, the literature, and this work.

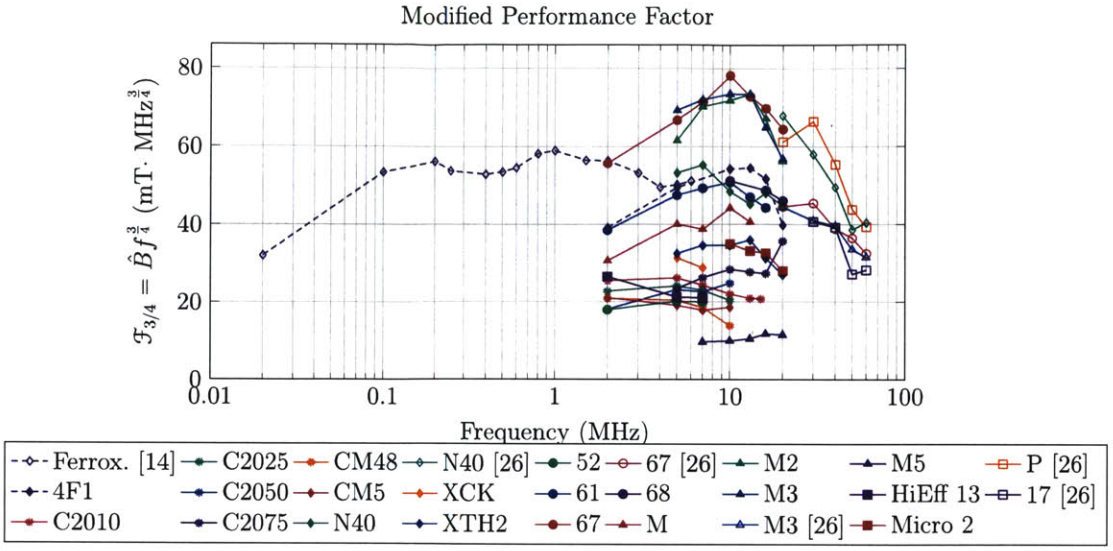



Figure 2-6: Survey of modified performance factor, incorporating data from industry, the literature, and this work.

frequency can improve power density in that regime. From 100 kHz to the edge of the HF regime, the improvement is slower (approximately $\propto f^{1/4}$). Indeed, high frequency winding effects become important in this regime – taking them into account with the modified performance factor shows little improvement up to about 2 MHz.

However, both the standard and modified performance factors indicate that some materials have superior performance in the HF range. The performance increase from 2 to 10 MHz is about 100 % in the standard performance factor (which would apply if, theoretically, frequency-dependent increases in winding losses could be made negligible at HF). The more realistic case of a single layer winding with skin effect is demonstrated by the modified performance factor, which shows approximately 45 % improvement between 1 and 10 MHz.

This improvement is substantial for loss-limited power stage components. Additionally, the size of auxiliary components (e.g. EMI filters) which are not bounded by core loss can be shrunk much more. If the use of HF materials allows the power stage to operate at higher frequency (e.g. 10x) without significant sacrifice (or even some gain), then filter corner frequencies are increased by the same factor (10x). If filter quality factors are held constant, both the capacitive and inductive elements would

be reduced by a factor of $\sqrt{10} \approx 3.16$. Since EMI filters often compose $> 20\,\%$ of system volume, this has a sizable impact on system density. This effect is demonstrated in [32], where a converter operating at 5–10 MHz is smaller than the EMI filter alone of a 100 kHz counterpart with similar specifications.

**Experimental Illustration of Performance Factor**

The performance factor is meant to be proportional to power handling density. This feature is demonstrated experimentally for the modified performance factor in Figure 2-7. Inductors are designed with equal impedance and equal quality factor (for a given sinusoidal current) across frequency. Lower frequency requires a larger inductance $L$, increasing the size. Higher frequency designs suffer from increased losses, requiring more core area to achieve the same $Q$. There is an optimal frequency in between. By comparing with Figure 2-6, it can be seen that the inductor with the highest power density is designed at the frequency where $\mathcal{F}_{3/4}$ peaks (around 9 MHz for Fair-Rite 67). This both shows the validity of the modified performance factor metric and provides a striking visual example of the relationship between frequency, material selection, and final component volume. Similar relationships for lower-frequency materials can be seen in [1, 5, 11].

## 2.5 Low Permeability Materials are Still Useful

Table 2.3: Power inductors designed for identical impedance and large-signal quality factor at an ac current of 1.6 A, corresponding to those in Fig. 2-7.

| **Frequency** MHz | **Impedance** 1 Ω | **Large-Signal Q** | **Volume** $cm^3$ | **P/N** |
|---|---|---|---|---|
| 3.58 | 36.5 | 212 | 1.50 | 5967001801 |
| 8.83 | 33.7 | 193 | 0.49 | 5967001101 |
| 12.90 | 33.4 | 220 | 2.83 | 5967001001 |
| 13.70 | 39.9 | 202 | 7.33 | 5967002701 |

Many of the materials with high performance factor in Figure 2-6 have relatively low permeability ($\mu_r < 250$) for power applications, with some of the highest per-

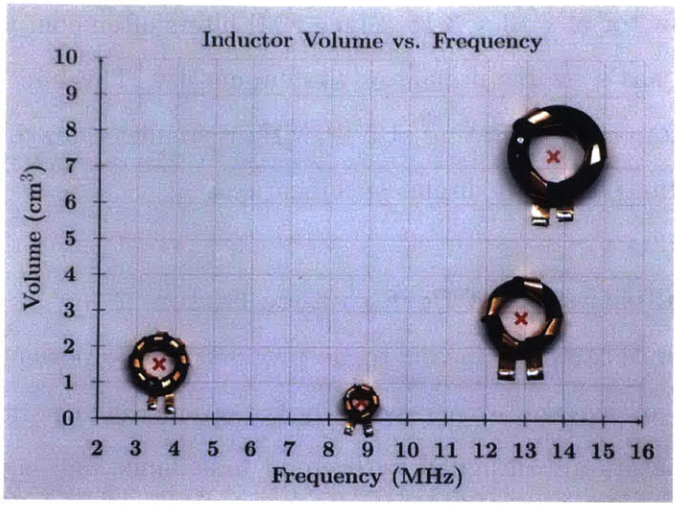



Figure 2-7: Inductors using ungapped toroidal cores of Fair-Rite 67 material ($\mu_r = 40$) designed for sinusoidal current at an impedance level of approximately 35 $\Omega$ and a quality factor of approximately 200 (see Table 2.3). The figure illustrates the inductor volume vs frequency at a given quality factor. Minimum inductor volume (highest power density) is achieved in the frequency range where material performance factor peaks.

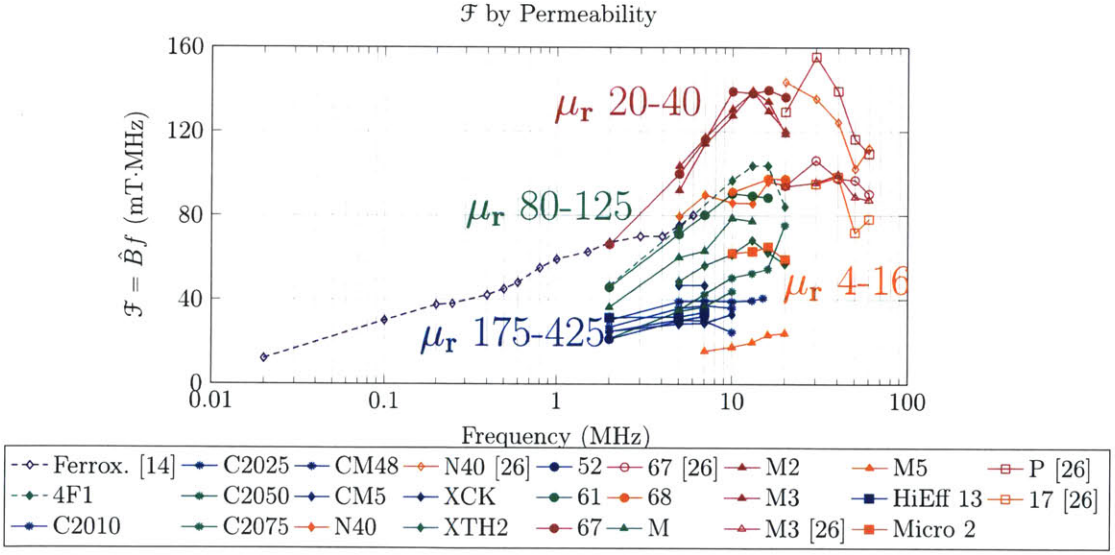



Figure 2-8: Performance factor sorted by permeability. Curves shown in orange are for relative permeabilities of 4–16 , those in red are for relative permeabilities of 20–40 , in green for relative permeabilities of 80–125 and in blue for relative permeabilities of 175–425 . It can be seen that materials having permeabilities of 20–40 often have the highest performance factor in the HF range.

forming materials having $\mu_r \approx 40$ (see Fig. 2-8). High permeability is sometimes thought to be important for the design of magnetic components. However, we will show that only very modest permeabilities are needed for effective HF power magnetics design – a requirement which is easily satisfied by the majority of materials that have experimentally shown high performance at HF. Thus, though neither the standard performance factor $\mathcal{F}$ nor the modified performance factor $\mathcal{F}_{3/4}$ directly depend on permeability, they can still be used to identify high performance materials for HF magnetics design.

### In Inductors

The impact of permeability may most simply be shown for the case of an inductor. In power applications, a gapped inductor is almost always used to reduce core loss [33]. For this case, the inductance value is given by

$$L_{gapped} = \frac{N^2}{\mathcal{R}_{tot}} = \frac{\mu_0 N^2 A_g}{l_g + \frac{l_c}{\mu_r}} \quad . \tag{2.9}$$

where $A_g$ and $l_g$ are the gap area and length, $l_c$ is the length of the core, $N$ is the number of winding turns, and $\mu_r$ is the relative permeability of the core. It can immediately be seen that high permeability has a diminishing impact on inductance once $\frac{l_c}{\mu_r} \ll l_g$.

If the core permeability were decreased (imagining this to be possible independent of other material parameters), the length of the gap $l_g$ would have to be decreased to compensate and maintain the same inductance. Since the total core reluctance $\mathcal{R}_{tot}$ and the number of turns $N$ are held constant, both the flux density swing (and hence core loss) and the winding loss are the same. Therefore, the power handling is independent of permeability until the core reluctance is so large that the gap is no longer necessary ($l_g \rightarrow 0$). Past this point, the only way to maintain inductance while continuing to decrease permeability is to increase the number of turns, compromising winding loss and hence power handling.

Thus there is a permeability threshold above which the material performance is

independent of the actual permeability value for purposes of gapped inductor design. For a given scenario if the permeability threshold were, say, $\mu_r = 10$, then performance would be no different between materials with $\mu_r = 10$ or $\mu_r = 1000$ (other factors held constant). The permeability threshold occurs at the value which produces the desired inductance for the desired core size and number of turns with no gap.

$$\mu_{r,threshold} = \frac{Ll_c}{\mu_0 N^2 A_c} \tag{2.10}$$

Thus, we see diminishing returns on increasing permeability. In the case of inductors, the advantage of permeability decays to zero at the threshold.

### In Transformers

The principle of diminishing returns on permeability for transformers will be shown to also hold for cases where the loss associated with magnetizing the core is considered to be a principal consideration in permeability requirements[2]. In this case, the advantage will merely approach zero as permeability increases.

The transformer calculation was already done in Section 2.2. The resulting power density from (2.7) is repeated here for convenience:

$$\frac{P_{del}}{A_c l_c} = (\pi \hat{K})(\hat{B} f)\sqrt{1 - \left(\frac{\hat{B}}{\hat{K}\mu}\right)^2} \tag{2.7 Revisited}$$

$$= (\text{Constant})(\mathcal{F})(\text{Correction Factor}) \quad .$$

The use of the standard performance factor or the modified performance factor only affects $\hat{K}$ and will be ignored in discussing permeability.

For a transformer, the magnetic material permeability both guides flux and increases the magnetizing impedance. However, in considering additional conduction

[2]Low permeability cores will also have a greater degree of leakage. This challenge can be addressed at the component level through innovative magnetic structures and winding patterns and also at the circuit level by incorporating leakage inductance into circuit operation (e.g. in an LLC converter).

losses required for magnetization of the core, increasing the shunt impedance of the magnetizing inductance is only important when $|Z_\mu| \sim R_L$. Once $|Z_\mu| \gg R_L$, the benefit saturates and additional permeability cannot significantly reduce conduction loss associated with magnetization and thereby improve component performance. The correction factor $\sqrt{1-(\frac{\hat{B}}{\hat{K}\mu})^2}$ approximates to 1 and drops out of consideration. Whether this actually occurs for a case of interest depends on the values of $\hat{B}$ and $\hat{K}$. To show that this is plausible, typical numbers for a medium frequency design are used ($\hat{B} = 100\,\mathrm{mT}$, $\hat{K} = 2\,\mathrm{A\,mm^{-1}}$ for a 1 mm thick layer of litz wire, and $\mu_r = 500$) and the correction factor comes to 0.997, a negligible quantity.

In order to show that permeability does not significantly affect performance in the case of (relatively) low permeability HF materials, it is necessary to set values for $\hat{B}$ and $\hat{K}$. For an efficiency or temperature-rise limited component, a total loss budget $P_{loss}$ is fixed and the allowed magnetic flux density and current density are related generally by

$$P_{loss} = P_{core}(\hat{B}) + P_{cu}(\hat{K}) \quad . \tag{2.11}$$

The copper loss,

$$P_{cu} = \frac{1}{2} I_{in}^2 R_{cu} \tag{2.12}$$

is specified by the total winding resistance in terms of the turn length $l_w$ and the width of one (e.g. foil) turn $w$,

$$R_{cu} = \rho \frac{N l_w}{w \delta} = \rho \frac{N^2 l_w}{l_c \delta} \tag{2.13}$$

assuming a single-layer winding distributed around the full perimeter of the core, $l_c$, in the skin-depth limit. This yields:

$$P_{cu} = \frac{1}{2} I_{tot}^2 \rho \frac{N^2 l_w}{l_c \delta} = \frac{1}{2} \hat{K}^2 \rho \frac{l_c l_w}{\delta} \quad . \tag{2.14}$$

The core loss is given by measured Steinmetz parameters (e.g. those in Section 2.3):

$$P_{core} = A_c l_c k_f \hat{B}^\beta \quad . \tag{2.15}$$

Table 2.4: Parameters for Power Ratio Calculations

| | |
|---|---|
| Outer Diameter | scale × 22.1 mm |
| Inner Diameter | scale × 13.7 mm |
| Thickness | scale × 6.35 mm |
| Temperature Rise | 50 °C |
| Thermal Law [1] | $P_{loss}$ = 0.0475 × Surface Area ($cm^2$) × $\Delta T$ (°C) |
| Frequency | 10 MHz |

A relationship between $\hat{B}$ and $\hat{K}$ that *approximately* delivers maximum power can be found by setting core loss and copper loss equal to each other. While this does not guarantee maximum delivered power for a given loss budget (or maximum efficiency for given power handling), it usually provides a good first-order approximation [33]. The resulting relationship is:

$$\frac{\hat{B}^{\beta/2}}{\hat{K}} = \sqrt{\frac{\rho l_w}{2A_c k_f \delta}} \quad . \tag{2.16}$$

The exact expression can also be used,

$$\hat{K} = \sqrt{(P_{loss} - A_c l_c k_f \hat{B}^{\beta}) \frac{2\delta}{\rho l_c l_w}} \quad . \tag{2.17}$$

Given the constraint relating $\hat{B}$ to $\hat{K}$, the best choice of $\hat{B}$ and $\hat{K}$ is the combination of values which maximizes delivered power. To select $\hat{B}$ and $\hat{K}$, therefore, it is necessary to plug either (2.16) or (2.17) into (2.7) and find the maximum of $P_{del}$ numerically.

To illustrate the realistic effect of permeability on high performance HF cores, we take one material (Fair-Rite 67) as an example and carry out a thought experiment in which we can vary the material permeability alone, leaving its loss characteristics unchanged. We consider a thermally limited design on a toroid of volume 1 $cm^3$ (parameters in Table 2.4). We will find that the real permeability of Fair-Rite 67 ($\mu_r = 40$) is sufficient to fully take advantage of the magnetic core.

We begin with a reference design in which the hypothetical permeability is very

high, and therefore the magnetizing inductance $L_\mu$ is very large and the magnetizing current $I_\mu$ is negligible. We maximize deliverable power using (2.7) for the parameters in Table 2.4. The resulting delivered power is the highest achievable for the given parameters, and deliverable powers at finite permeabilities will be normalized to this maximum reference. The values of $\hat{B}$ and $\hat{K}$ for this design are also kept as references.

We next substitute cores of identical parameters but decreasing permeability. For a first thought experiment, we do not re-optimize for each permeability but continue to use the same values of $\hat{B}$ and $\hat{K}$ as the reference design. As the permeability is decreased, the component achieves less and less deliverable power for the available temperature rise, owing to the increase in magnetizing current. Normalizing the achievable power density at finite permeability to the maximum achievable power density (i.e. for the reference design with infinite permeability) gives a ratio which is denoted the *unoptimized power ratio* $\mathcal{P}$, and the result is plotted in Fig. 2-9.

It can immediately be seen that the benefit of added permeability saturates above a certain point, as expected. Indeed, above $\mu_r = 100$, the difference between the finite-permeability design and the reference (infinite permeability) is almost indiscernible. For permeabilities as low as $\mu_r \approx 22$ (lower than the real permeability of Fair-Rite 67), the component incurs less than 10 % performance loss compared to the reference. Below $\mu_r \approx 22$, performance collapses until the temperature budget is used up by the loss due to the magnetizing current alone and no power can be delivered to the load. It can be seen that the real permeability of Fair-Rite 67 ($\mu_r = 40$) allows it to achieve very nearly the same performance as if it had infinite permeability, i.e. to nearly fully provide the available benefit of a magnetic core.

These conclusions are actually overly pessimistic because we did not reoptimize the design at each finite permeability. If we do reoptimize, the results improve substantially. This experiment follows as before, but the power delivered in (2.7) is maximized for each permeability by changing the operating points $\hat{B}$ and $\hat{K}$. The achievable power for this experiment is also normalized to the reference (high permeability) design and the ratio is denoted the *optimized power ratio* $\mathcal{P}_{opt}$. The results are also plotted in Fig. 2-9.

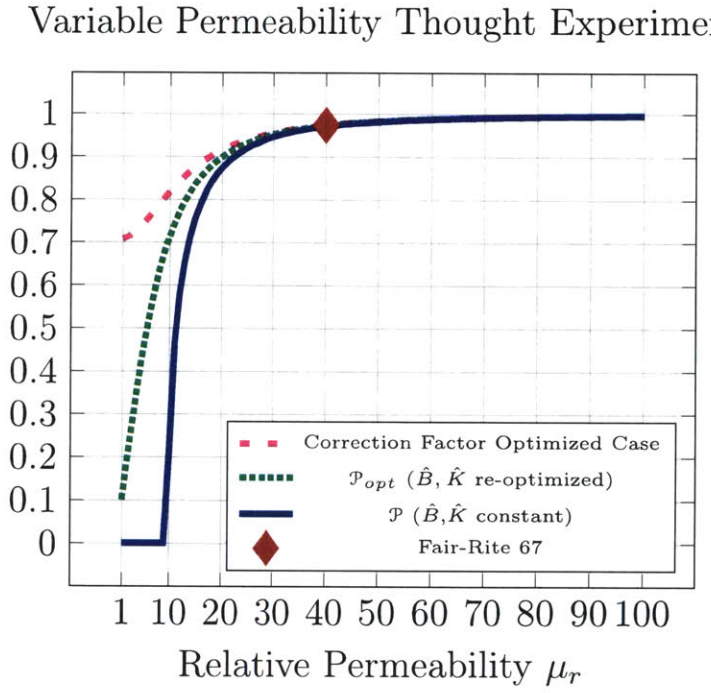



Figure 2-9: A theoretical ensemble of materials with the same material loss parameters but different permeabilities. Each point represents an optimization with (2.7) maximized using the parameters in Table 2.4 with a volume of 1 $\text{cm}^3$. The deliverable power, normalized to a high-permeability design, is plotted where $\hat{B}$ and $\hat{K}$ are held constant ($\mathcal{P}$). The same ratio is also plotted with re-optimized designs ($\mathcal{P}_{opt}$), along with the correction factor for this case. The loss parameters used match those of Fair-Rite 67 at 10 MHz; its permeability ($\mu_r = 40$) is noted on the graph.

It can be seen that $\mathcal{P}_{opt}$ falls off less sharply as permeability is decreased than the unoptimized case $\mathcal{P}$. For example, an optimal component at $\mu_r = 10$ would still provide substantial power delivery while an unoptimized design would have lost all utility at that permeability.

The reason for this improvement lies in the interaction between the $\hat{B} \cdot \hat{K}$ product and the correction factor in (2.7). In Fig. 2-9, the plot for the un-optimized case is its own correction factor, as neither $\hat{B}$ nor $\hat{K}$ are allowed to vary. This is no longer true for the optimized case, so the correction factor is plotted separately. It can be seen that, at low permeability, the deliverable power collapses in the unoptimized case due to the correction factor, whereas the optimized case trades lower $\hat{B}$ for higher $\hat{K}$ to keep the correction factor high. In that case the deliverable power still drops because both the $\hat{B} \cdot \hat{K}$ product and the correction factor are slowly reduced, but the collapse is not as severe.

Based on these thought experiments, it may be concluded that practical designs can achieve high power density with relatively modest permeabilities. The principle of diminishing returns on permeability is demonstrated for some real materials by calculating $\mathcal{P}$ and $\mathcal{P}_{opt}$ using the parameters in Table 2.4 and allowing volume to vary while maintaining the geometric ratios. The results are plotted in Fig. 2-10, from which several conclusions may be drawn. First, the power ratios of the lower permeability materials fall farther below 1 as expected from the previous thought experiments. Second, the lower permeability materials see a greater variation between $\mathcal{P}$ and $\mathcal{P}_{opt}$ in the same way that their values diverge at low permeability in Fig. 2-9. Third, as volume is decreased there is both a decline in achievable performance and a greater deviation between the power ratios. Finally, despite all these effects, in most cases the power ratios for low permeabilities are above 0.9, indicating that permeability has only a small practical influence on performance. Additionally, the balance of core loss and total loss for the optimized case is plotted in Fig. 2-11, and is consistent with the general rule that minimizing total loss usually requires core loss to be equal to or slightly less than copper loss [34].

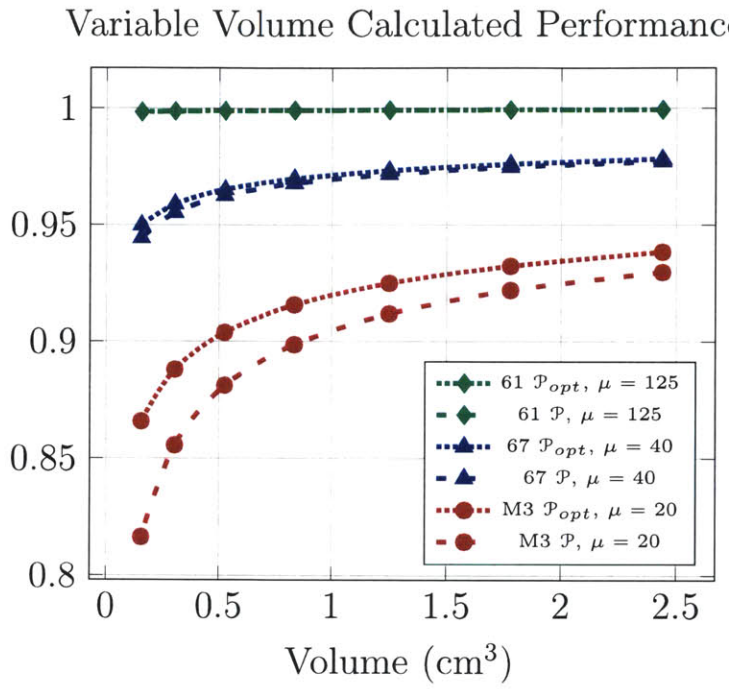



Figure 2-10: Un-optimized and optimized power ratios ($\mathcal{P}$,$\mathcal{P}_{opt}$) for example materials and volumes. Parameters in Table 2.4.

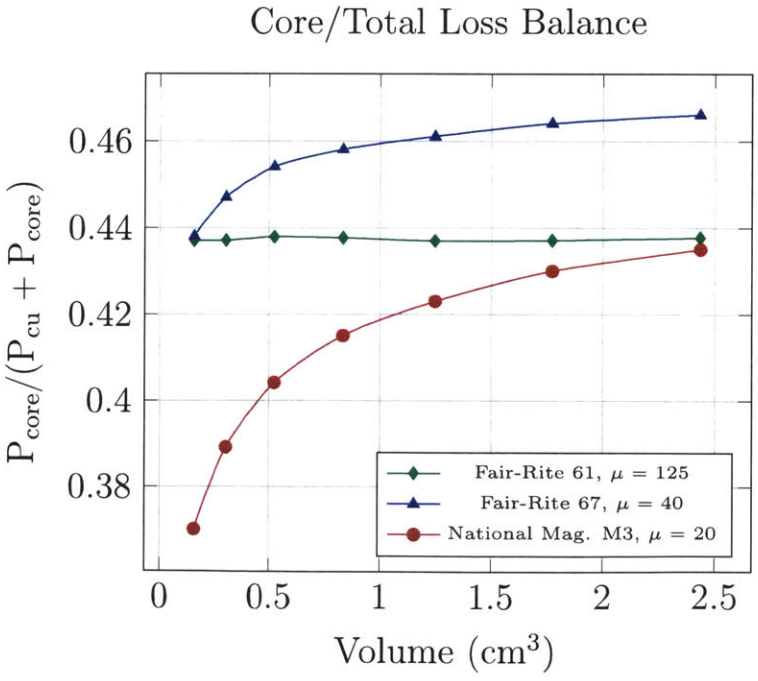



Figure 2-11: The fraction of total loss attributable to core loss for example materials and volumes for the optimized case as in Fig. 2-9. Parameters in Table 2.4.

## 2.6 Conclusion

The drive to increase frequency in power conversion circuits, enabled by advanced circuit designs and wide-band-gap semiconductors, is primarily predicated on the idea that passive components can be made smaller and cheaper, and that systems can achieve higher performance. The extent to which power magnetic components can be improved at higher frequencies hinges on their loss behavior at those frequencies. We have undertaken measurements to produce this necessary data in the HF range, where material data was previously lacking. The results suggest that significant improvements in performance are possible through HF operation using commercially available materials.

Additionally, the extension of the performance factor $\mathcal{F}$ to the high frequency modified performance factor $\mathcal{F}_{3/4}$ allows for a more sober and realistic assessment of the benefits of high frequency operation. Using this metric and the newly gathered data, we foresee a roughly 45 % improvement in loss-limited magnetic component density (with even greater gains in other magnetic components) through designs operating deep in the HF regime using currently-available materials.

Finally, we observe that the materials which offer such promising results have relatively low permeabilities. We conclude that an upper bound exists on the amount of relative permeability necessary to develop optimized components, and that for most designs the actual permeabilities available in high performance HF materials are sufficient to avoid any disadvantage.

# Chapter 3

# A Wide-Operating-Range Converter for High Frequency Operation

## 3.1 Background

### Conventional Converters Are Ill-Suited for Wide-Range HF Operation

It was shown in Chapter 2 that operating frequencies can extend up to at least 10 MHz while still improving the size of magnetic components having loss constraints. Frequencies could further be increased to about 30 MHz while achieving similar power stage density to conventional designs. In making this change, the other advantages of HF operation continue to apply (smaller EMI filters, faster transient responses, etc.).

Nevertheless, even with high peformance magnetic materials and wide-band-gap switching devices, many conventional power converter topologies and control techniques are ill-suited to the HF regime at hundreds of volts and watts. Switching losses in particular limit the application of hard-switched topologies in this space. For example, in a boost converter with $V_{out} = 400\,\text{V}$ and $P_{out} \sim 300\,\text{W}$, appropriate state-of-the-art GaN FETs would have an energy stored in their output capacitances (at turn-on) of about $E_{oss} = 3\,\mu\text{J}$. If the converter is hard-switched (as is convention-

ally done, even in DCM), the switch will dissipate this energy every cycle, resulting in a switching loss of 3 W/MHz. At conventional frequencies, this loss (~0.3 W) may be acceptable; in the MHz regime the loss (~3 W) may be merely tolerable (with good heat sinks); deep in the HF range, the loss (~30 W) would be prohibitive both from thermal and efficiency perspectives. Therefore, circuit-level design must achieve some degree of soft-switching to operate at HF in many applications.

### Soft-Switching Converters Typically Have Narrow Operating Range

Soft switching techniques (e.g. zero voltage turn-on or zero current turn-off) are commonly employed to avoid switching losses and enable high efficiency and/or high power density [35–37]. However, such converters typically lose their soft-switching characteristics (or suffer other disadvantages) outside a particular operating range. For example:

*Resonant converters* (e.g. series, parallel, LLC, etc.) are usually operated under frequency control above the relevant resonant frequency to have inductive loading and achieve ZVS. The operating frequency increases to limit output power; higher frequencies result in low light-load efficiency [38, 39]. Additionally, series-resonant peak voltages and parallel-resonant circulating currents can be much higher than the input/output voltages/currents under some operating conditions, placing extra strain on converter components. This is especially true of quasi-resonant converters and single-switch inverters which must use switches rated for significantly higher voltages than the input/output voltages. Wide frequency variations required by low-Q resonances can also make EMI filter design difficult.

*Phase-shift control* can also be used (typically with full-bridge resonant converters). While this technique can be employed at a single frequency, there are difficulties in achieving soft switching for all of the devices as well as achieving current sharing in the inverter legs, especially as power is varied [40, 41]. Other techniques also lose ZVS as output power is varied, including asymmetrical clamped mode control and asymmetrical pulse width control [42, 43].

*Resonant-transition pulse-width-modulated converters* operate similarly to bound-

ary conduction PWM converters. During resonant phases, the primary inductor is allowed to resonate with the parasitic switch capacitances to discharge them before the switches are turned on [44]. For example, a buck converter may have some dead time after the high-side switch is turned off, allowing the inductor to discharge the device capacitances before the low-side switch is turned on. Additionally, after the inductor current reaches zero and the low-side switch (or diode) is off, the inductor will again resonate with the device capacitances to bring the switching node voltage up and allow the high-side switch to turn on with reduced voltage. While these converters can operate over a wide power range and maintain ZVS, they have significant limitations. Since such converters must allow the inductor current to reach zero (as in boundary conduction mode) and must allow a fixed resonant transition period, they therefore must operate with variable frequency to vary output power. Additionally, these converters can only achieve ZVS for a narrow range of voltages. For example, the resonant-transition buck converter only achieves ZVS for the high-side switch when $V_{in} < 2V_{out}$.

This chapter will present a converter topology and control scheme suitable for HF operation at hundreds of volts and watts. The converter is particularly well-suited to applications which require operation over a wide range of voltages and/or powers, thereby overcoming many of the disadvantages of existing soft-switching topologies. To introduce this converter, it will be compared to the resonant-transition boost converter, which is sometimes used in grid-connected applications.

### The Resonant-Transition Boost Converter Has Limited Voltage Range

One application of wide-operating range converters is in power factor correction (PFC). Such PFC converters are typically connected to a rectified ac source (such as a single-phase ac power grid) and are operated to draw current proportional to their input voltage. This makes the converter look like a resistive load to the grid, drawing real power and minimizing wasteful reactive power. Since such converters must draw current over the a wide portion of the line cycle (ideally the whole line cycle), they inherently must operate with wide input voltage range and wide power range.

A commonly chosen converter for PFC stages is the boost converter, owing to a variety of advantages. First, the boost converter operated in boundary conduction mode (BCM) with constant on-time acts as a natural "loss-free resistor": if the output is held roughly constant by a large buffer capacitor, the peak inductor current, and hence the local-average input current, is proportional to the input voltage. This high-ripple mode also allows the use of a small inductor. A resonant transition can be added after the inductor current reaches zero, allowing for ZVS or near-ZVS turn-on of the low-side switch. The combination of ZVS and high ripple, plus the ease of control, makes the resonant-transition boost converter an attractive choice for PFC stages for high density and high efficiency. Additionally, the input to a boost PFC is directly connected to the main power stage inductor, providing a degree of natural EMI filtering. Finally, the output capacitors needed to buffer the "twice-line-frequency" pulsating power are available at the highest energy density in the ~400 V range [45]. Since these capacitors occupy an appreciable portion of grid-connected converter volume, boosting from the ac line to a dc bus at this voltage is a good choice for size and cost.[1]

The boost converter topology and operating phases for resonant-transition conversion are shown in Fig. 3-1. Inductor current and switching node voltage $V_B$ waveforms are shown in Fig. 3-2. Energy is stored in the inductor while the active switch is on. When the switch turns off, the switching node is charged to $V_{out}$ (usually quickly) and the diode turns on. During the subsequent direct delivery phase, the inductor current decreases to zero. The diode then turns off and the inductor is allowed to resonate with the device capacitances at the switching node. During this resonant phase, the equivalent circuit is an LC resonant tank, offset by $V_{in}$. This circuit's voltages will oscillate with an amplitude of $V_{out} - V_{in}$ around a center of $V_{in}$ (these oscillations will be interrupted by the switch turning on).

It can be seen that the resonant transition can only bring $V_B$ to zero if the output voltage is more than twice the input voltage. If this condition is violated, the switch

[1] There may be an element of self-fulfillment in this observation, as the common use of boost PFC stages has created a market for good 400 V capacitors. Nevertheless, the choice of converter for a *current* application is based on the *current* component options.

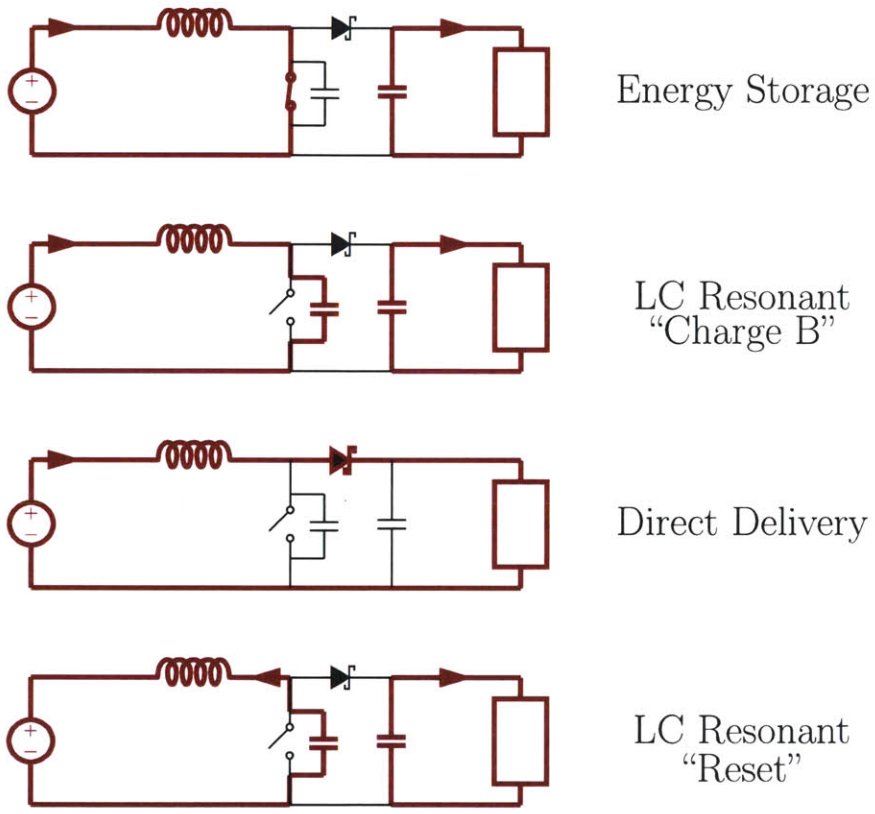



Figure 3-1: Resonant-transition boost converter operating modes. The LC resonant reset phase can achieve ZVS for the active device, but only for $V_{in} < V_{out}/2$. This limitation makes the boost converter less attractive for high frequency operation for dc-dc applications with small step-up ratios or ac applications with high peak input voltages.

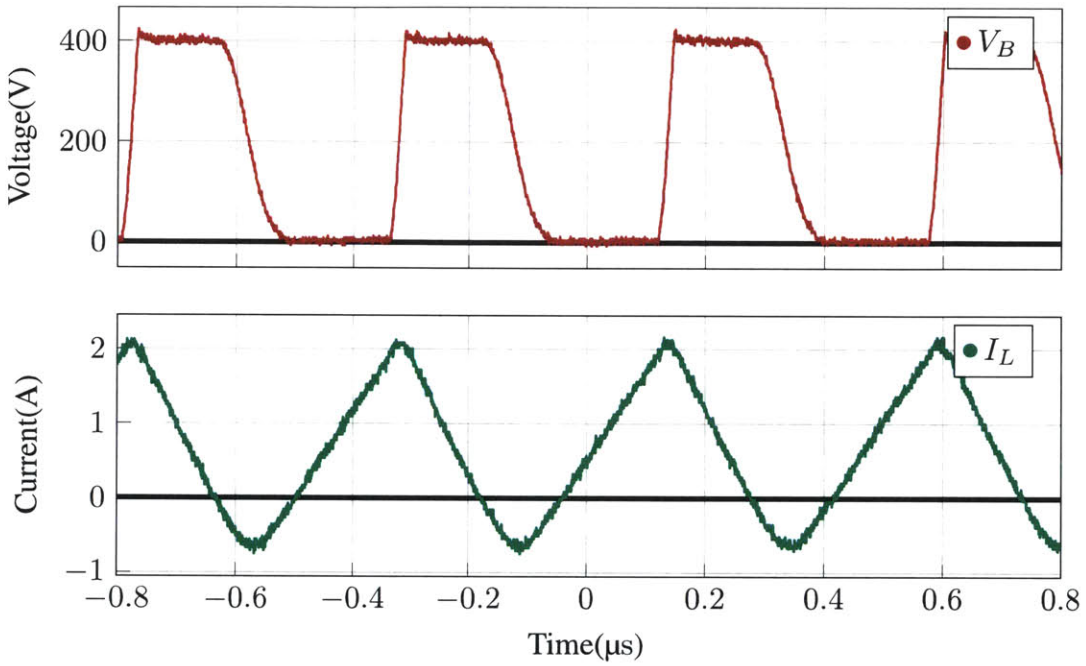



Figure 3-2: Resonant-transition boost mode experimental operating waveforms. The energy storage, direct delivery, and resonant reset phases are clearly visible. The LC resonant phase is very short due to the high initial inductor current at the beginning of that phases; though less visible, it manifests itself in the rounded top corner of the inductor current waveform. It can be seen that the switching node voltage is sufficiently discharged to achieve ZVS turn-on for the active device at the end of the resonant reset phase.

will turn on with some voltage across it, incurring switching loss. This effect makes the resonant-transition boost converter unsuitable for HF operation in applications where the input voltage range includes $V_{in} > V_{out}/2$. While this condition is always satisfied when converting from 120 Vac (e.g. in the United States) to 400 Vdc, it is certain to be violated in "universal input" power factor correction which must operate up to $V_{in}$ = 265 Vac ($V_{pk} \sim 370V$).

## 3.2 Converter Operation

The converter proposed in this work, operated to boost voltage, achieves ZVS across the entire input voltage range $V_{in} < V_{out}$, making it suitable for HF operation.[2] Although the voltage and power range are chosen with power factor correction in view, the converter is applicable in dc-dc conversion as well, and experimental results will only be presented at dc. With proper switch implementation and control, the converter topology is also capable of performing buck functions with wide ZVS range. Such modes are outside the scope of this work and have not been prototyped, and therefore are simply outlined in Appendix D. The converter will be referred to as the "proposed" converter or, due to its distinctively achiving ZVS over a wide voltage range, as a "wide-range resonant-transition converter."

The circuit topology is shown in Fig. 3-3. Although it resembles a non-inverting buck-boost converter, it is operated differently to achieve high efficiency and ZVS. It should be noted that the converter is not limited to the implementation in Fig. 3-3 (e.g. see Appendix D for modes that require SA2 and SB2 to be active devices). Regardless of implementation, the switching node on the input side is labeled node A, with switches SA1 and SA2, while the switching node on the output side is labeled node B, with switches SB1 and SB2.

It may first be noted that leaving SA1 perpetually on makes the simplified circuit

[2]Although it will be considered here for application in a universal input, 400 V output converter, it should be noted that the converter topology is very flexible outside this application space. Indeed, proper implementation and control allow the converter to achieve ZVS for all active devices for any conversion ratio; the additional design and control aspects to do so will be explored in detail in the future.

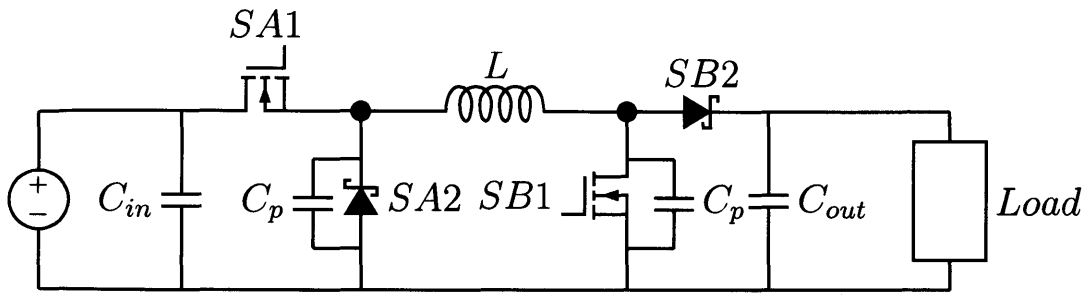



Figure 3-3: The universal ZVS converter configured for boost operation. The diodes can be replaced with active switches for synchronous rectification and/or operating in ZVS buck modes. The capacitances $C_p$ may constitute the parasitic device capacitances or added capacitances, though maximum frequencies may be limited by large $C_p$.

topologically equivalent to a boost converter, and hence may be operated in resonant-transition boost mode. While this mode does not achieve ZVS over the whole input voltage range, as already noted, it is still useful for achieving efficiency and good input-side EMI characteristics when requirements for ZVS are met.

The circuit also admits a modified boost mode which achieves ZVS for any input voltage (below the output voltage). Operating waveforms for this mode are shown in Fig. 3-4, with experimental operating waveforms in Fig. 3-10. With both switches closed, the inductor stores energy from the input and the load voltage is supported by the output capacitor. Next, SB1 is turned off. The parasitic capacitance at node B is charged (usually quickly) by the inductor current and the converter enters a direct delivery phase. After a set time, SA1 is then turned off. The parasitic capacitance at node A is discharged[3] by the remaining inductor current and the converter enters an indirect delivery phase. Once the inductor has delivered all of its stored energy to the output ($i_L \rightarrow 0$), both diodes turn off and the converter enters the resonant-transition "reset" phase. Unlike the boost converter, with a resonant transition centered around $V_{in}$, the transition in the proposed converter centers on $V_{out}/2$ due to the previous discharge of node A and the absence of an offset voltage source in the CLC resonant

[3]If the inductor current at this step is insufficient to discharge node A, the converter may not achieve true ZVS during the resonant reset transition. This constraint limits the minimum power the converter can process since a minimum energy storage (and hence delivery) is required for ZVS.

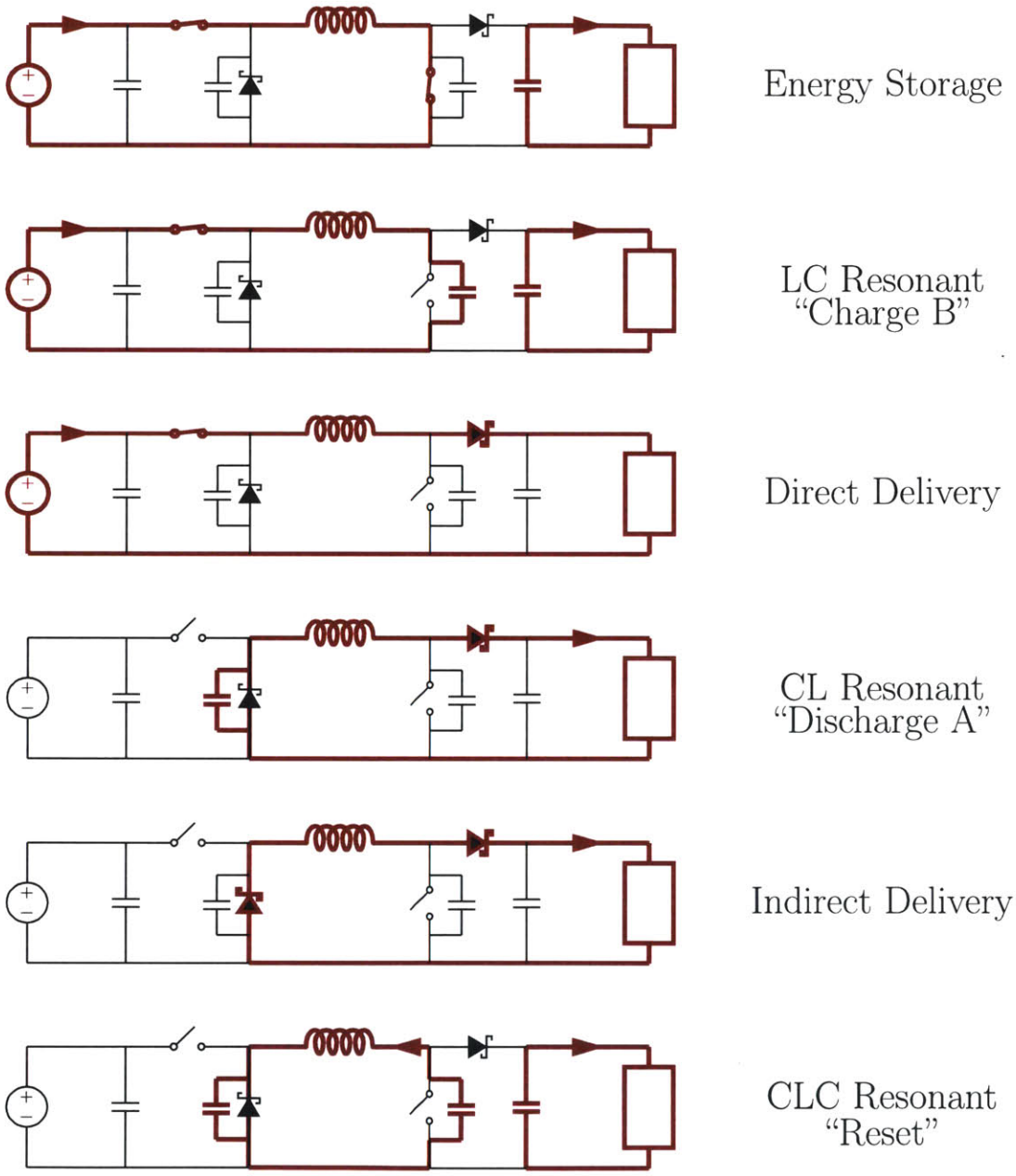



Figure 3-4: The universal input boost converter operating in modified boost mode. The CLC resonant reset phase permits ZVS for both active switches for any input voltage. The LC and CL resonant phases permit ZVS for the other switches, even if replaced with active devices.

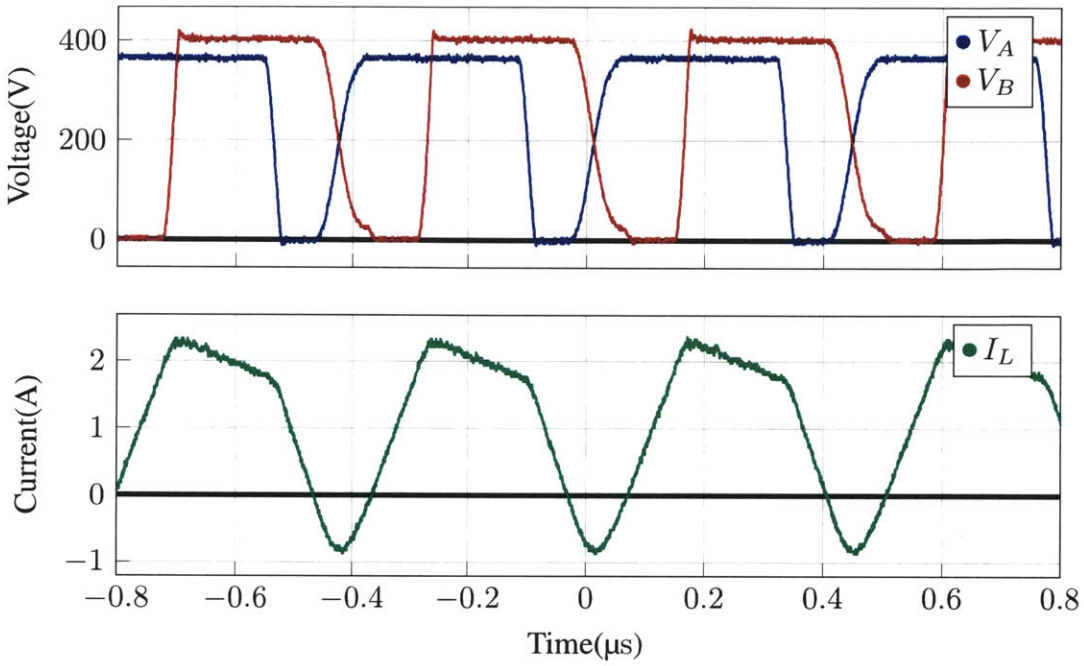



Figure 3-5: Modified boost mode experimental operating waveforms for $V_{in} = 355\,\mathrm{V}$, $P_{out} = 349\,\mathrm{W}$, $\eta = 98\,\%$. The energy storage, direct delivery, indirect delivery, and resonant reset phases are clearly visible. The LC and CL resonant phases are very short due to the high initial inductor current at the beginning of those phases; though less visible, they manifest themselves in the rounded corners of the inductor current waveform. It can be seen that the switching node voltages are sufficiently discharged to achieve ZVS turn-on for both active devices at the end of the resonant reset phase.

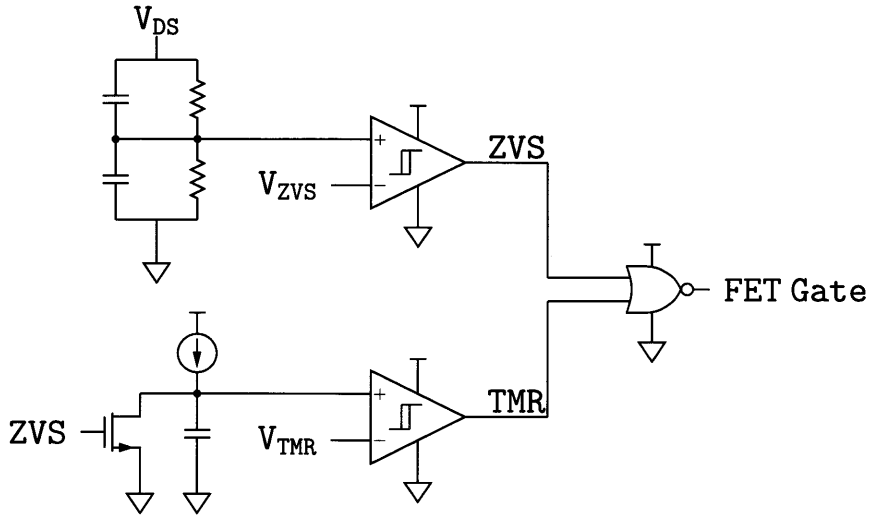



Figure 3-6: Actuation control circuit for the active switches. Signal ground is connected to the source of the FET being controlled, while signal $V_{DS}$ is connected to the drain. Local ZVS detection turns the switch on in response to the resonant drain-source voltage transition. This signal also starts a ramp timer, which turns the switch off after a specified time.

path. The resonant transition will bring[4] node A to $V_{in}$ and node B to ground, accomplishing ZVS for both switches when they turn on.

The active switches may be controlled by local ZVS detection (for turn-on) and ramp timers (for turn-off), as shown in Fig. 3-6. In this approach, the voltage across the switch $V_{DS}$ is stepped down across both resistors and capacitors to ensure fidelity to the rapidly changing switch voltage. When the stepped-down $V_{DS}$ crosses some threshold, the comparator turns the switch on. The threshold may be chosen to be very close to zero or at some intermediate value in order to pre-empt the zero-voltage transition and allow for some delay through the subsequent logic. The output of the ZVS detection comparator also releases the ramp generator which serves as a timer. When the ramp timer reaches its threshold voltage, the corresponding comparator turns the switch off again, completing the cycle.

[4]The resonant transition, in isolation, would bring node A to $V_{out}$. However, with SA1 implemented as a MOSFET or GaN FET, the (equivalent) body diode will turn on once $V_A$ reaches $V_{in}$. This interruption to a true resonant transition actually aids in achieving ZVS on SB1 quickly and reliably in the presence of nonlinearities.

## 3.3 Advantages and Opportunities

The wide-range resonant-transition converter has a number of advantages over other soft-switched converters. First, as already noted, the converter achieves ZVS for the entire input voltage range $V_{in} < V_{out}$ and for a wide range of powers, making it particularly well-suited to power factor correction. This is an advantage over the resonant-transition boost converter, which only achieves ZVS for half of that range. The presence of the input-side active switch in the wide-range resonant-transition converter also provides natural avenues to avoid inrush current which must be addressed in the boost converter.[5]

Additionally, the switches need only be rated for the input or output voltage, as opposed to some resonant and quasi-resonant converters whose active devices must block resonant voltages. Additionally, the proposed converter has a brief resonant phase (relative to the switching period), which wastes less energy in resonant "circulating current," and also provides operation over a variable but relatively narrow frequency range.

The wide-range resonant-transition converter may operate at a single frequency or, to achieve even wider power range, over a relatively narrow frequency range. This is because there is an additional control handle on power, namely the distribution of times that the converter spends in each phase. At some frequency, a short energy storage time and a long direct delivery time create a "wide and short" inductor current waveform, which transmits low power. At the same frequency, a longer energy storage time and a shorter direct delivery time yields a higher peak inductor current and a higher net power transferred.[6] Thus, power may be varied at a single frequency, simplifying EMI filter design. Frequency may be varied to vary power as well, but

[5]To prevent inrush current problems, the boost converter is frequently implemented with a series switching element before the inductor which is simply left in the on state except during start-up. Thus, the presence of SA1 in the wide-range resonant-transition converter, even when operated in resonant-transition boost mode, does not necessarily add "extra" loss or complexity in comparison.

[6]Continuing this process at the same frequency could yield a direct delivery time of zero and an energy storage time of about half of the switching period. This mode of operation is equivalent to a "resonant-transition buck-boost" mode. It transmits a moderate amount of power, but it suffers from low efficiency due to its high peak inductor current. Barring other advantages to this mode of operation, it is avoided.

using both control techniques allows the frequency variation to remain small.[7]

## 3.4 Design and Optimization

The principal design challenge in the ideal wide-range resonant-transition converter is selection of the inductor value $L$. Conceptually, the range of allowable inductance values is set by the desired power and operating frequency ranges (selection of the prototype inductor is discussed in Section 3.5).

The maximum output power and minimum frequency set the maximum inductance. Any larger of an inductance value would prevent the inductor from storing energy quickly enough within the maximum period. Naturally the converter could deliver larger powers if it allowed more time per period, sacrificing some of the advantages of HF operation.

The minimum output power and maximum frequency set the minimum inductor value. Any smaller of an inductance value would store energy too quickly, and controlling for power would result in too-high frequencies. Such frequencies may be too quick for circuit logic (greatly disrupting real operation) or may incur higher loss.

For detailed analysis of circuit timing and its relationship to processed power, see Appendix E.

Another practical design consideration is the nonlinearity in the device capacitances. These nonlinearities can be very large (a factor of 10 across operating voltage in some cases) and can cause the converter to lose ZVS even under otherwise ideal conditions. Consider a nonlinear capacitance across the switches which reduces in value with larger voltage across it. Consider also a smaller capacitance with similar behavior across the diodes . Entering the resonant phase, both SA1 and SB1 in Fig. 3-3 have large voltages across them, resulting in small total node capacitances.

[7]While variations over a wide frequency range can make EMI filter design more challenging, varying over a small range can actually be beneficial when frequency is varied regularly (e.g. if frequency varies over an ac line cycle). Variations in frequency prevent a single spectral spike in the frequency domain, which can actually loosen constraints on EMI filters. "Spread-spectrum" techniques are sometimes used in conventional converter control ICs for just this purpose, e.g. the LTC6902 multiphase clock.

The resonant transition proceeds quickly and stores very little energy in the inductor. Once the switch voltages reach a lower voltage where the capacitance increases (e.g. ~40 V may be a reasonable value for some devices), the capacitances increase dramatically. The voltage polarity on the inductor is already oriented to decrease inductor current, and the inductor does not have enough energy to complete the resonant transition in the face of much larger capacitance values. Thus, ZVS is not achieved, incurring loss or the failure of the detection logic to turn the switches on again.

Nonlinear capacitors with opposite voltage characteristics could compensate for the above problem, but such capacitors tend to be lossy and large. A better solution relies on the fact that the problem is not nonlinear capacitance *per se*, but rather asymmetric nonlinearity such that the net capacitances are small at the beginning and large at the end of the resonant transition. If the capacitance were large at both the beginning and end of the transition, ZVS could be achieved. Such a compensating capacitance is already present in the circuit in the diodes which have similar capacitance characteristics, but whose voltages are large (small) when the switch voltages are small (large). Though the diode capacitances are often smaller than the switches', a parallel combination can achieve a practically balanced total node capacitance.

## 3.5 Prototype Implementation

A prototype was designed and implemented as a dc-dc converter operating from 0–400 Vdc with an output voltage of 400 Vdc. This implementation could be used in a power factor correction stage permitting universal input voltage and utilizing a 400 Vdc bus. The converter was designed to operate between 2–5 MHz and deliver up to 500 W from $V_{in} = 375V$, for a design compatible with power factor correction at 300 W average across an ac line cycle. Some implementation details are listed in Table 3.1.

The switches and diodes were selected first, due both to the low availability of high frequency devices in the target voltage range and also in order to use concrete

parasitic capacitance values in simulation to determine the inductor size.

To the author's knowledge, the only commercially available GaN FETs with blocking voltages significantly above 400 V at the time of design were a series of 650 V devices from GaN Systems and Transphorm. A similar series of pre-production devices from Navitas Semiconductor were also made available by sample. The Navitas devices were chosen for low on resistance and to experiment with iDrive (the integrated gate driver on some Navitas products).

Despite higher availability of SiC diodes designed for high frequency at several hundred volts, actual selection of HF diodes can still be problematic. Such diodes have been shown to fall short of the performance metrics stated on the datasheet when operated at high frequency [46]. Thus, power diode selection at this time may be based on published performance and/or personal experience verifying that a particular diode "works well" at high frequency. The diodes for this converter were implemented as C3D1P7060Q 600 V SiC Schottky diodes from Cree (now "Wolfspeed"). These were chosen for their small size and because they are known to this research group to maintain reasonable performance in the HF range.

With the devices selected, the converter was simulated in SPICE to determine the required inductor value, according to the limitations in Section 3.4. While the converter operation could be examined analytically, the complexity of the analysis (especially due to device nonlinearities) makes such analysis both difficult and prone to error (nevertheless, calculations are included in Appendix E. Simulations were initially run with switching signals manually chosen to achieve ZVS without much body diode conduction.

It was found through simulation that the range of powers that both achieves ZVS and stays within a given frequency range changes in two ways with inductor value. As the inductor value decreases, the achievable power range both increases in magnitude and widens in range. For example, if a 20 µH inductor allows the converter to process 50–100 W (for a given frequency range), then a 10 µH inductor might allow the converter to process 75–200 W. For the converter prototype here with device capacitances, power range, and frequency range listed above, the allowable inductor

size was found to be between 8–20 µH.

The inductor was designed using Fair-Rite 67 as core material because it has the lowest loss in the 2–5 MHz range (see Section 2.3). Unfortunately, this and most other materials examined in Chapter 2 are only commercially available in rod and toroid shapes. Experiments were performed with a toroidal core design (manually cut in half with a slow-speed gravity-fed diamond saw to create a gap), as well as with a "horseshoe" shape core, i.e. one half of a toroid left as a magnetic open circuit (similar to a rod). Such an inductor shape may be useful for shaping the emitted magnetic field (e.g. to keep it away from conductors and sensitive circuit elements). In general, large gap sizes were required to keep core loss low such that the straight-field approximation in the gap no longer held. Obtaining a sufficiently high reluctance magnetic path was most straightforwardly achieved using a large-gap magnetic circuit.

In all cases, the core PN was 5967002701 with windings consisting of 450-strand, 48 AWG litz wire (about 31 µm diamter). The the horseshoe inductor used for efficiency measurements had 21 turns. From 2–5 MHz, the skin depth in copper is about 29–46 µm; it is expected that the skin effect is mostly mitigated. At higher frequencies this may no longer be true. Nevertheless, 48 AWG is the smallest strand size that is economically available. The nominal inductance value was found to be 16 µH for the horseshoe inductor.

The switch actuation circuit (illustrated previously in Fig. 3-6) was implemented with the devices listed in Table 3.1. All devices were primarily chosen for high speed. The iDrive integrated driver on the Navitas devices was found to have a significantly long propagation delay (~20 ns); therefore the final prototype replaced the iDrive FETs with simple "three terminal" devices from the same family and used parallel TinyLogic series buffers (nominal propagation delay ~3 ns) to drive the gate instead. The second implementation also replaces the LTC6752 comparators with devices from the ADCMP600 series, though it makes little difference. The two devices are nearly the same in specification and have identical packaging and pinout. The ADCMP600 differs only in that it can operate with $V_{DD} = 5V$ which was used as the control

Table 3.1: Device implementation in two prototype iterations of the wide-range resonant-transition converter.

| Device | Implementation 1 | Implementation 2 |
|---|---|---|
| Comparators | LTC6752-1 | ADCMP600-1 |
| NOR Gate | 74LVC1G27 | 74LVC1G27 |
| OR Gate | 74LVC1G32 | 74 LVC1G32 |
| FET | Navitas 6131 | Navitas 6103 |
| Driver | iDrive | NC7WZ16[8] |
| Isolated DC-DC | DCP01B | RP-0509S |
| Microcontroller | PIC24F16KM204 | PIC24FV16KM202 |

supply voltage in the second iteration.

The capacitor and resistor values were chosen to allow for high speed and to match the availability of (especially the high voltage) components. Other than selecting properly voltage-rated components and small packages for high density, no special care was required in selection of these passive components.

The rest of the control circuitry was less crucial to the operation of the circuit. The isolated dc-dc converter to power the flying control logic was originally implemented as the DCP01B with which this group has previous good experience. The RP-0509S in the second implementation has similar specifications; it simply had a slightly more agreeable form factor. It should be noted that both of these devices have isolation capactiances under 5 pF. Care should be taken to avoid a similar class of 1–2 W isolated converter modules in smaller packages with much higher isolation capacitances. The microcontroller was originally implemented with the PIC24F16KM204 for its variety of analog functions (including DACs). These features were not fully exploited in either implementation, though the integrated DACs could have replaced one of the discrete DACs on the board. The second iteration used a microcontroller from the same family (for the familiarity of the author and continuity of code), though with fewer pins and functions in a smaller package.

[8]Two devices at two buffers each, for a total of four buffers in parallel per FET

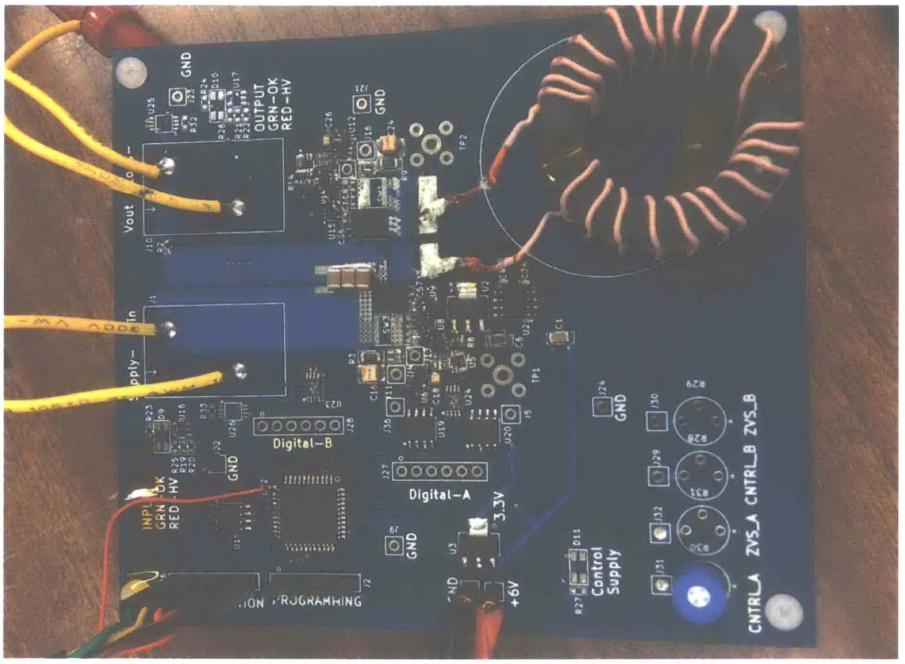



Figure 3-7: Photograph of the first implementation PCB along with a gapped toroidal inductor (used for initial experiments; results not reported). The input- and output-side FETs are visible, with the corresponding diodes and capacitors directly underneath.

## 3.6 Experimental Performance

Experiments were conducted with a BK-8522 electronic load set as a constant 400 V, a KLP 600-4-1.2k power supply, and GDM-8341 digital multimeters. The multimeter were operated to measure both voltage and current which, due to loss in the wires, could have introduced some inaccuracy. This inaccuracy was estimated to be low due to the relatively high power, low current, and low line resistance; this was confirmed with "four-point" measurements using additional meters. The experimental setup is shown in Fig. 3-9.

The converter was operated in modified boost mode across a range of input voltages and output powers. For a set of example waveforms for regular boost mode, see Fig. 3-2. An example of modified boost mode waveforms is shown in Fig. 3-10; another operating point is shown in Fig. ??. Summary efficiency results are shown in Fig. 3-11. It can be seen that, by achieving ZVS, the converter maintains and even

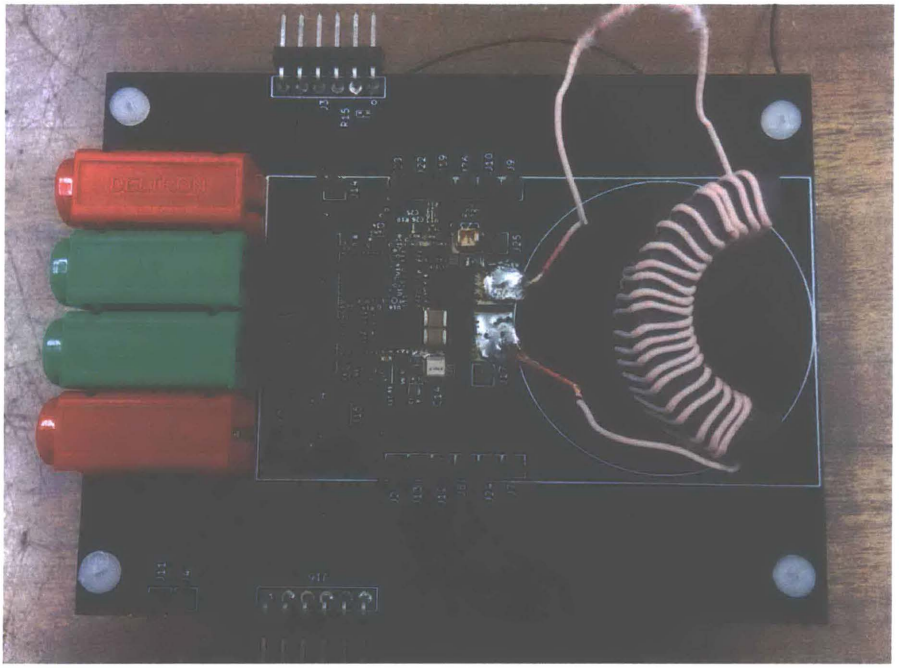


Figure 3-8: Photograph of the second implementation PCB along with the "horse-shoe" inductor used for experiments on both boards. The input-side FET, diodes, and capacitors are visible, with the return path (node A) on the second layer directly underneath. The output-side FET is visible, with the corresponding diodes and capacitors on the bottom side directly underneath. The isolated dc-dc converter (RP-0509S) used to power the controls and driver for SA1 is clearly visible; it was chosen for this version for its smaller footprint (the inductor still sets the converter height). Other components are relatively small.


Figure 3-9: Setup used to evaluate experimental prototypes. The meters, supply, and load are visible on the right. The DC supply at the top was used to power the controls (and a fan in some cases). The board communicated with and was controlled by the computer at the left through a serial-to-usb adapter cable.

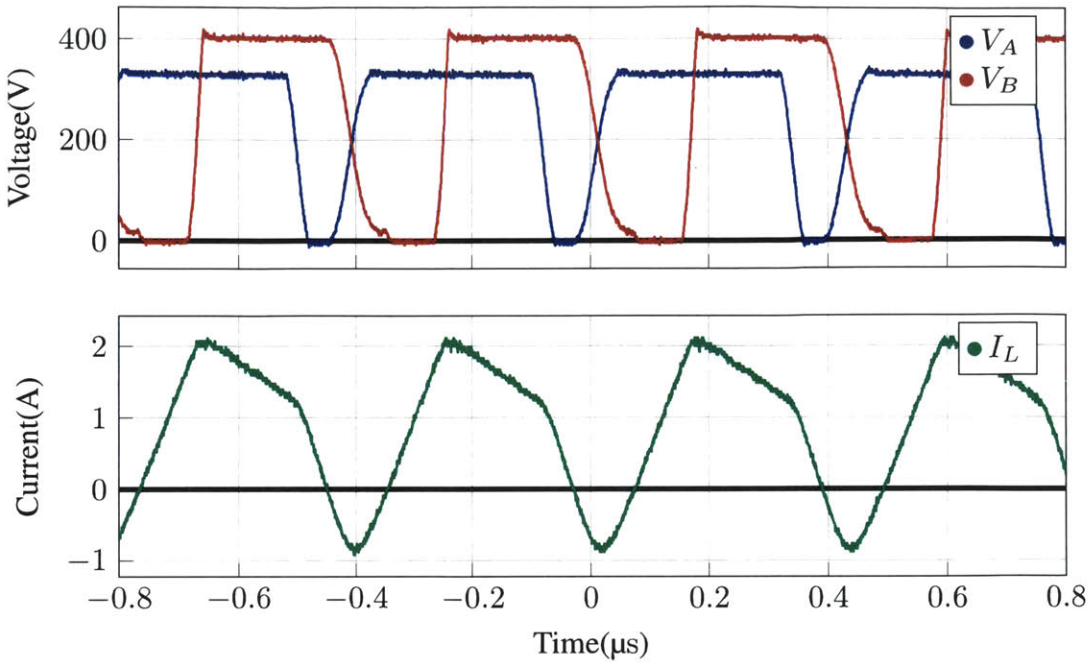



Figure 3-10: Modified boost mode experimental operating waveforms for $V_{in} = 322\,\mathrm{V}$, $P_{out} = 256\,\mathrm{W}$, $\eta = 98.2\,\%$. Compared to Figure 3-10, the energy storage and direct delivery phases show different slopes in the inductor current corresponding to the change in input voltage value. It will be noted that the frequency difference is relatively small despite the change in output power.

improves efficiency at high input voltage. Converter efficiencies drop at high conversion ratios and at light-load. Nevertheless, other techniques can be used to maintain high efficiency (burst mode operation at high power, transmitting more power near the peak of the line cycle in an ac application, etc.).

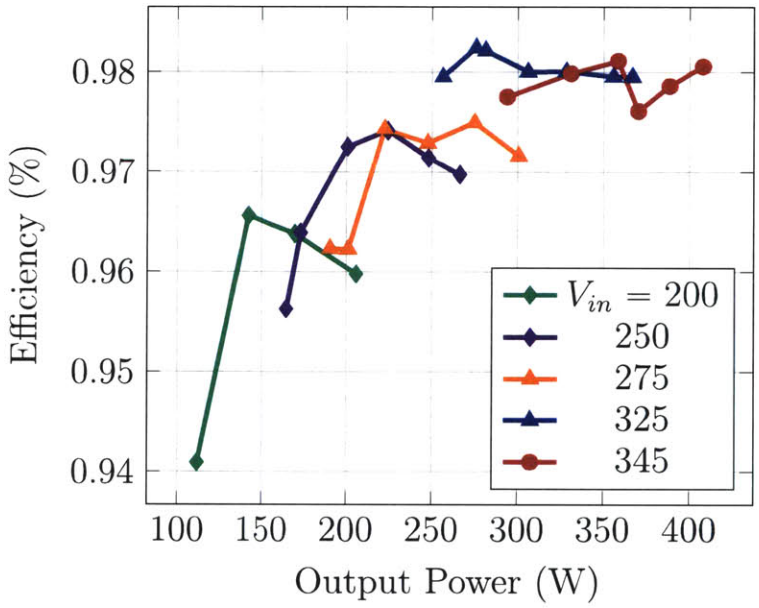



Figure 3-11: Experimental efficiency in modified boost mode across power and input voltage. All operating conditions had measured frequencies between 2–3 MHz. The high efficiency at high voltage is possible because the converter achieves ZVS; hard switching would have cost several percentage points of efficiency and it is unlikely the devices could withstand the corresponding temperature rise.

# Chapter 4

# Conclusion

Power converters operating at high switching frequencies can achieve a number of benefits, including smaller physical size, less expense, and faster transient response. Achieving these benefits is only possible if the associated loss mechanisms are managed to maintain high efficiency and tolerable temperatures for high density circuits. This work helps contend with two of the primary sources of loss that traditionally limit frequency increases: magnetic core losses and switching losses.

In Chapter 2, a modified performance factor was developed in order to properly evaluate magnetic materials at high frequency. With this metric, and an appropriate core loss measurement technique, it was shown empirically that magnetic materials exist which maintain the potential for high power density well into the HF regime. The maximum performance factor was shown to actually increase until about 10 MHz and to still achieve reasonable values until about 30 MHz. Future advances may create materials that achieve even higher performance factors out to higher frequencies.

It was also found empirically that many of the high performance materials in the HF regime were low permeability NiZn ferrites. Through analysis that incorporated empirical data, it was shown that magnetizing a core with low permeability need not pose fundamental limits to the effectiveness of such materials. The effect of additional leakage field was not considered directly, though future work may demonstrate the ability to use that flux advantageously.

In Chapter 3, the need to achieve soft switching to maintain efficiency at high

frequency was addressed. While soft switching has been in use for decades, a need was identified for circuit topologies and control techniques that can maintain soft switching (ZVS in particular) across a wide range of voltages and powers. A "wide-range resonant-transition converter" (consisting of a topology and switch actuation schemes) was proposed which can achieve ZVS for any $v_{in} < v_{out}$ for step-up functions. Step-down conversions were also analyzed in Appendix D which maintain ZVS for any $v_{in} > v_{out}$. It was shown that a second control handle (aside from frequency) allowed the converter to process a range of powers while keeping frequency to a relatively narrow band. The wide-range resonant-transition converter's advantages and possible applications were discussed.

A prototype wide input, fixed output dc-dc converter was designed to operate at the same voltages that would correspond to universal input power factor correction (one promising application of the converter). It was demonstrated experimentally that the converter achieves ZVS across the voltage range, maintains high efficiency across voltage and power, and can be designed to accommodate the parasitics and performance limitations of currently available devices and components. The converter operated at several MHz, and it was argued that there is no fundamental limitation to operation near 10 MHz, which would take full advantage of available magnetic materials.

Thus, the potential for improved performance at HF was demonstrated. Magnetic materials and devices available today are capable of high efficiency deep into the HF regime. Converter topologies like the one proposed here continue to expand the range of applications for high frequency power conversion. It is the author's hope that these results will enable the development of high performance converters in industry and encourage material, component, and circuit investigations in fundamental research laboratories and in academia.

# Appendix A

# Modified Performance Factor Background and Variations

Performance factor is developed considering limitations on power loss for a given core size, under several assumptions. The first assumption is to neglect variations in ac winding resistance (and hence winding loss) with frequency such that, for a given winding, the achievable ampere-turns ($NI_{pk}$) is independent of the frequency. The second assumption is that the waveform shapes are sinusoidal, and the third assumption is that the flux density is limited by power loss in the core, not by saturation. Because the instantaneous voltage across a winding is proportional to $dB/dt$, the maximum rms value of the voltage at a given power loss per volume $P_v$ is proportional to magnetic flux density and frequency, $V_{pk} \propto \hat{B} \cdot f$. Given fixed waveform shapes, the power or VA is proportional to the product of rms current and voltage, and thus to the performance factor.

$$\text{VA} = V_{pk} I_{pk} \propto (\hat{B} f) \times (I_{max} = \text{constant}) \propto \mathcal{F} \tag{A.1}$$

A plot of performance factor as a function of frequency for a collection of materials provides a quick way to compare materials and identify the highest performance materials at a given frequency, or to identify the frequency range where a particular material is most useful [14]. However, the assumptions underlying the traditional

performance factor impose some limits on its usefulness, and some modified performance factors have been proposed to overcome these limits. In [47], a modified performance factor is proposed to consider saturation flux density also. The proposal is to simply take the geometric mean of saturation flux density (a consideration for dc current) and conventional performance factor (a consideration for ac current) to obtain $\mathcal{F}_{dc+ac} = \sqrt{B_s \cdot \mathcal{F}}$. Although no rigorous justification is given for this formulation, it appears to be useful in design examples provided in [47]. In [48], another modified performance factor is proposed, $\mathcal{F}_{\frac{3}{4}} = \hat{B} f^{\frac{3}{4}}$. The ¾ exponent is said to account for high-frequency winding effects.

At MHz frequencies, high-frequency winding effects are consistently important, and magnetics design is often dominated by core loss rather than saturation considerations. Thus, we choose to examine $\mathcal{F}_{\frac{3}{4}}$ in more detail. First we note that for comparing different materials at a fixed frequency, the choice between conventional ($\mathcal{F}$) and modified ($\mathcal{F}_{\frac{3}{4}}$) performance factors does not matter—either will lead to the same conclusions as they differ by only a fixed factor of $f^{\frac{1}{4}}$. However, if the goal is to select an operating frequency, they may lead to different conclusions, with $\mathcal{F}$ indicating a larger benefit to increasing frequency, but with that advantage discounted based on high-frequency winding loss when $\mathcal{F}_{\frac{3}{4}}$ is used.

We extend the theory in [48] and designate $\mathcal{F}_w = \hat{B} f^w$ as the modified performance factor, where $w$ is a parameter selected based on the analysis of winding loss in each case. The choice of $f^{\frac{3}{4}}$ in [48] is based on the assumption that $R_{ac} \propto f^{\frac{1}{2}}$, as is the case with simple skin effect. To maintain a constant power loss in a given winding, the maximum current handling is proportional to $1/\sqrt{R_{ac}}$, which is proportional to $f^{-\frac{1}{4}}$. More generally, for fixed loss with varying numbers of turns, $I \propto f^{-\frac{1}{4}}/N$. The voltage is proportional to $N\hat{B}f$, so the product of voltage and current is proportional to $\hat{B} f^{\frac{3}{4}}$. Hence $\mathcal{F}_{\frac{3}{4}}$ is appropriate for components with windings whose ac resistance is determined by simple skin effect, and thus is a good choice for use in the HF range.

However, in many practical situations the assumption that winding resistance is dominated by skin effect is not valid. In particular, for multi-layer windings including litz wire windings, proximity effect is also important. To determine the appropriate

type of modified performance factor to use for these cases, we assume that the winding is optimized for the particular frequency to be used. As discussed in [49], there are several possible constraints one might adopt for optimizing a multi-layer winding, so we consider each in turn to find the corresponding modified performance factor, $\mathcal{F}_w = \hat{B} f^w$. The results, derived below, are listed in Table A.1.

One scenario is a multi-layer winding with a fixed number of layers, with the conductor thickness in each layer optimized to minimize ac resistance at the operating frequency. This is Case 2 in [49] and is also the case considered in the winding optimization analysis in [10]. The result, for $p$ layers, is an optimized winding resistance that is reduced by a factor of $1/\sqrt{p}$ from the resistance of a single-layer winding, using a layer thickness of approximately $1.3\delta/\sqrt{p}$. Thus, the frequency dependence is the same as for a single-layer winding, which is simply the case in which the fixed value of $p$ is equal to 1, and for any fixed value of $p$, the appropriate modified performance factor is $\mathcal{F}_{\frac{3}{4}} = \hat{B} f^{\frac{3}{4}}$.

Unfortunately, for frequencies in the HF range, the optimum thickness for a many-layered winding can be thinner than is easily practical. Litz wire becomes very expensive with strands smaller than 50 µm in diameter and is not commercially available with strands smaller than about 30 µm. Although foil is available at low cost down to single-digit micrometer thicknesses, applying it effectively in multiple parallel layers can be difficult [50]. Thus, another situation of interest is a minimum thickness constraint on the layers of a multi-layer winding. In this case, as reviewed in [49], the resistance is reduced relative to the resistance of a single-layer winding by a factor of about $\frac{2}{3}\frac{t_{min}}{\delta}$, where $t_{min}$ is the minimum thickness constraint and $\delta$ is the skin depth, for thicknesses below about 1.5 skin depths. Given that the resistance of a single-layer winding is proportional to $1/\delta$, we see the optimized multilayer design under this constraint has resistance proportional to $1/\delta^2$, and thus proportional to frequency. As shown in Table A.1, this results in a modified performance factor $\mathcal{F}_{\frac{1}{2}} = \hat{B} f^{\frac{1}{2}}$. It is important to note this is only valid for combinations of frequency and minimum thickness such that $t_{min} < 1.5\delta$; beyond that point, a single layer would be preferable, and $\mathcal{F}_{\frac{3}{4}}$ should be used instead.

A particular example of this is litz wire for which we take AWG 48 (32 µm) as the smallest practical strand diameter, $d_{min}$. The corresponding effective layer thickness is $0.584 d_{min}$ [49], or 18.7 µm. This is equal to $1.5\delta$ at 28 MHz at room temperature in copper, indicating in this case that magnetic materials could be evaluated using $\mathcal{F}_{\frac{1}{2}}$ for frequencies up to 28 MHz. The lower power of $f$ (½ instead of ¾) in the performance factor for this case indicates the diminishing value of litz wire over the HF frequency range, and in practice, litz wire is not usually worthwhile above the low end of the HF range (though it has been used effectively in the 5–10 MHz range, e.g. [32,51]).

A third case is a multi-layer winding with a fixed number of wire strands, with the strand diameter optimized. With the number of strands $n$ fixed at one, this corresponds to a simple solid-wire winding. Larger values of $n$ correspond to litz wire with a fixed number of strands. As the diameter of the strands is varied, the number of turns that fit in one layer of the winding varies, and so the number of layers varies. Thus, this case is different from the case of a fixed number of layers. Designs optimized under this constraint have a ratio of ac resistance to dc resistance $F_r = 1.5$, and wire diameter proportional to $1/f^{\frac{1}{3}}$ [7,52]. This results in ac resistance proportional to $f^{\frac{2}{3}}$, and $\mathcal{F}_{\frac{2}{3}} = \hat{B} f^{\frac{2}{3}}$. In the HF range, multi-layer solid-wire windings are a poor choice and litz wire is limited by strand diameter rather than by the feasible or economical number of strands. Thus, this version of modified performance factor is more relevant to the LF than to the HF range, but it is included in Table A.1 for completeness.

A final case to consider is one in which an advanced winding technology eliminates skin- and proximity-effect losses and makes the ac resistance equal to the dc resistance, and the achievable winding resistances is not limited by number of strands, number of layers, or a minimum thickness constraint, but instead by the available space in the winding window. In this case, the ordinary performance factor $\mathcal{F}$ is the appropriate measure, just as it is for lower frequency designs where skin and proximity effects are not significant. For example, at tens of kilohertz, litz wire can perform well enough in many cases that an initial design can be based on the assumption that skin and

Table A.1: Optimized ac resistance as a function of frequency for different assumptions and resulting performance factor formulation

| Case | $R_{ac}$ vs. $f$ | $NI$ vs. $f$ | Corresponding performance factor |
|---|---|---|---|
| No significant ac resistance effects | $R_{ac} \propto f^0$ | $NI \propto f^0$ | $\mathcal{F}_1 = \hat{B}f$ |
| Single-layer winding or other fixed number of foil layers or effective wire layers | $R_{ac} \propto f^{\frac{1}{2}}$ | $NI \propto f^{-\frac{1}{4}}$ | $\mathcal{F}_{\frac{3}{4}} = \hat{B}f^{\frac{3}{4}}$ |
| Fixed layer or strand thickness | $R_{ac} \propto f$ | $NI \propto f^{-\frac{1}{2}}$ | $\mathcal{F}_{\frac{1}{2}} = \hat{B}f^{\frac{1}{2}}$ |
| Fixed number of wire strands with many layers | $R_{ac} \propto f^{\frac{2}{3}}$ | $NI \propto f^{-\frac{1}{3}}$ | $\mathcal{F}_{\frac{2}{3}} = \hat{B}f^{\frac{2}{3}}$ |

proximity effect are eliminated, although care is needed in the litz wire design to ensure that this goal is achieved [8]. For HF windings, skin and proximity effect are still serious issues even with the best available litz wire. Possible methods to make HF windings that approach the performance of litz wire at lower frequencies are discussed in [50].

The different performance factors in Table A.1 can be summarized as follows:

- Without significant ac resistance effects, conventional performance factor is appropriate.
- With ac resistance effects, and with a single-layer winding, as is often the most practical solution for frequencies in the HF range, the appropriate modified performance factor is $\mathcal{F}_{\frac{3}{4}}$. This result also applies to any fixed number of layers, if the thickness of the layers is optimized for the frequency of operation.
- If the fixed constraint is instead the minimum layer thickness or wire diameter, and the number of layers or strands is optimized for the frequency of operation, the appropriate performance factor is $\mathcal{F}_{\frac{1}{2}}$.
- The intermediate case of a multilayer wire winding with a fixed number of strands results in $\mathcal{F}_{\frac{2}{3}}$, but is rarely relevant to the HF range.

Thus, in our generalized definition of high-frequency performance factor $\mathcal{F}_w = \hat{B}f^w$, we choose values of $w$ between $\frac{1}{2}$ and 1 based on the winding design constraints

anticipated in the application of interest. Because a single-layer winding is the most common choice for frequencies in the HF range, we choose to use $w = \frac{3}{4}$, and thus $\mathcal{F}_{\frac{3}{4}} = \hat{B}f^{\frac{3}{4}}$ for comparing core materials in Section 2.4 (in addition to traditional performance factor $\mathcal{F} = \hat{B}f$). Nevertheless, for specific types of winding designs and different frequency ranges, the different modified performance factors listed in Table A.1 can be chosen accordingly.

# Appendix B

# Core Loss Measurement Methods

Core loss measurement approaches may be divided into calorimetric methods [53–59] and electrical methods, which include the classical two-winding method [33, 53–55, 60, 61] and resonant techniques [26, 62–65]. The two-winding method is sensitive to phase errors, which become increasingly difficult to control at higher frequencies. Phase errors can be reduced by adding a resonant capacitor to the drive winding and using the sum of the sense winding voltage and the capacitor voltage for the voltage measurement [62, 64]. A variation on this approach uses an air-core transformer in place of the capacitor to cancel the reactive component over a wider frequency range [63, 64]. Although the sensitivity to phase error is reduced by the methods of [62–64], the phase information is still necessary in the measurement. An alternative to two-winding methods is the resonant $Q$ measurement approach in [26]. Either approach can be accurate in the HF range, but in the resonant $Q$ approach phase measurement is not required, eliminating that source of error.

For the above reasons, we elected to use the resonant $Q$ approach from [26], since it is suitable for accurate measurements in the HF range. The measurement setup consists of an RF power amplifier source in series with a high-$Q$ resonant tank, as in Fig. B-1. Due to the low impedance of the measurement circuit at resonance, a $50\,\Omega$ to $3\,\Omega$ transmission line transformer (AVTECH AVX-M4) is used to better match the output impedance of the power amplifier. A low-$Q$ parallel resonant filter is also added to remove any harmonic components from the input to the measurement

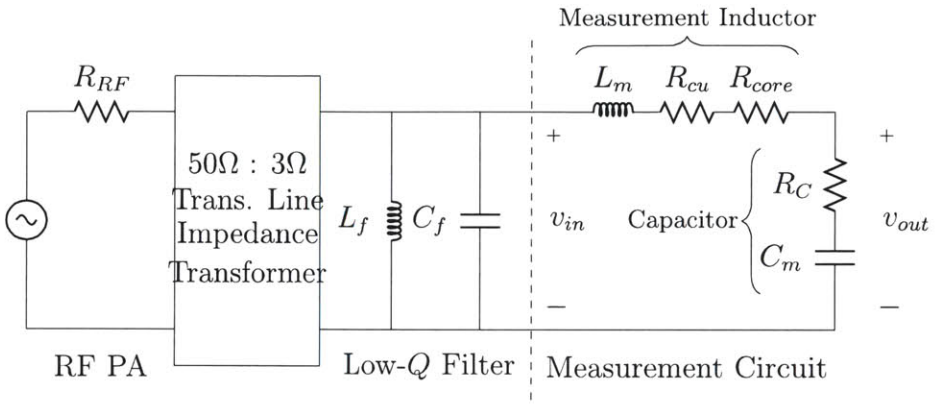



Figure B-1: Circuit schematic used for core loss measurement.

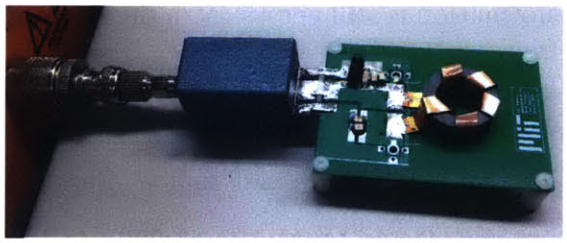


Figure B-2: Image of a test circuit in operation. The power amplifier (orange, left) connects to the board through the transmission line transformer (blue). The input filter, measurement inductor, and resonant capacitor are visible.

circuit. These components are simply added to ensure that the input voltage to the measurement circuit is a single-frequency sinusoid. As will be described, the measurement itself only depends on $v_{in,pk}$ and $v_{out,pk}$, so the actual implementation to the left of the dotted line in Fig. B-1 is immaterial so long as good drive waveform quality is obtained.

The voltage at the input to the tank and the output voltage (i.e. the voltage across the resonant capacitor) are measured with respect to ground. At the undamped resonant frequency $\omega_r = 1/\sqrt{LC}$ the quality factor of the inductor is simply the ratio of the output to the input voltage amplitudes

$$\frac{V_{out-pk}}{V_{in-pk}} = \left| \frac{R_C + \frac{1}{j\omega_r C_m}}{R_{core} + R_{cu} + R_C} \right| \approx \frac{\omega_r L_m}{R_{core} + R_{cu}}$$

$$= Q_{L_m} \tag{B.1}$$

where $R_C$ is the equivalent series resistance (ESR) of the capacitor, and $R_{cu}$ and $R_{core}$ are equivalent series resistances representing winding (copper) loss and core loss, respectively. In the above derivation, the reactance of the capacitor cancels that of the inductor at the resonant frequency. The approximation is also made that the capacitor equivalent series resistance is small with respect to the modeled inductor resistance.

The circuit resistance modeling core loss can be calculated from measured values

$$R_{core} = \frac{2\pi f_s L V_{in-pk}}{V_{out-pk}} - R_C - R_{cu} \tag{B.2}$$

where the copper resistance is estimated from measurements of an air-core inductor of identical construction and/or through numerical modeling. The current through the inductor and capacitor is the same (and known from the measured $V_C = V_{out}$) so volumetric power loss can be computed directly:

$$P_V = \frac{I_{L-pk}^2 R_{core}}{2V_L} \tag{B.3}$$

Possible sources of error and mitigation strategies are covered in [26]. This approach can yield core loss measurements that are accurate to better than 20 %, which is sufficient for design purposes and within the lot-to-lot variation of typical materials.

# Appendix C

# DC Bias and Other Effects

There are several factors which limit the applicability of the Steinmetz equation to losses in practical power converters. It is known, for some ferrites, that the combination of high permittivity and high permeability in very large cores can lead to dimensional resonance and flux skin effect phenomena at high frequencies [66, 67]. These effects can cause changes in permeability and increased losses at higher frequencies and in larger core sizes. While these effects can be significant in large cores, they are unlikely to be significant in the small cores ($\sim$1 cm) of low permeability ($\mu_r \sim 100$) studied here. These effects were not directly observed in the experiments outlined here, and will not be considered further in this work.

While loss characteristics for magnetic materials are measured and reported for sinusoidal ac magnetic flux densities (equivalently, sinusoidal ac currents), these waveforms are only encountered for a small subset of power converter topologies (e.g. resonant converters). Magnetic components often have magnetizing currents with significant harmonic components, such as triangular or trapezoidal waveforms, and may have significant dc components (e.g. in continuous conduction mode buck or boost converters). It is known that harmonic content increases core loss beyond that predicted by summing the loss contributions of each harmonic in a waveform (an incorrect approach, due to the non-linear nature of material core loss). Nevertheless, several well-justified approaches have been developed to accurately account for such losses [68–71].

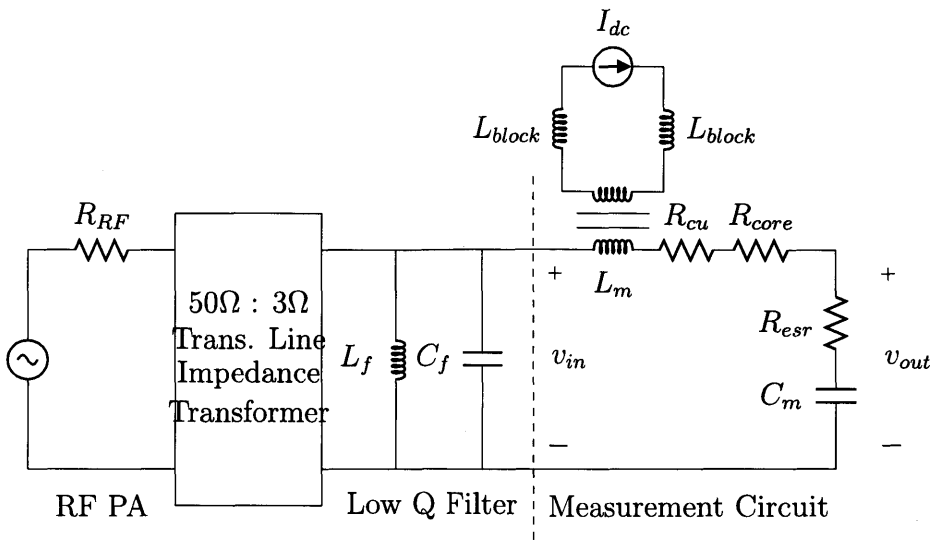



Figure C-1: Measurement circuit for evaluating material performance with both ac flux and superimposed dc bias.

It is also known that waveforms with significant dc components lead to higher core losses than otherwise identical waveforms without any bias, despite the fact that the dc component does not cause dynamic dipole rotation or domain wall motion. These effects have been documented, but no general theory (neither empirical nor from first principles) exists to allow designers to take this effect into account. It should be noted that this effect is independent from concerns about core saturation, and occurs even when peak flux densities are well below saturation.

We investigated the effect of dc bias on core loss for NiZn materials in the HF regime, and found that core loss typically increased substantially with large superimposed dc magnetic flux densities. Measurements with dc bias were done using the same test setup as in Fig. B-1 with modifications to provide a flux bias to the core. A secondary winding was applied to the measurement inductor, and a dc power supply was used to apply a constant current through the secondary winding to impose a dc flux density bias on the core (see Fig. C-1). Two large air-core inductors (designed according to the guidelines in [72]) were placed in series with the secondary winding in order to provide a constant current through it while not exposing the power supply to high voltages due to transformer coupling from the resonant measurement circuit.

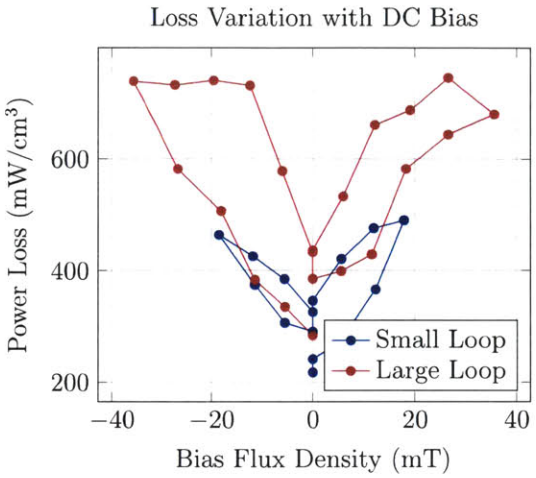



Figure C-2: Core loss increase of National Magnetics M ($\mu_r = 125$) at 10 MHz with ac flux swing held constant at 6.5 mT and dc bias slowly changing. The small loop experiment was conducted first, followed by the large loop. Bias flux can increase loss density by at least a factor of three, with significant hysteresis.

An ac flux density was applied to the core, and the dc bias was varied in both positive and negative directions. The change in loss was measured, and the change in inductance (i.e. effective permeability) was inferred from the change in resonant frequency. The results are shown in Figs. C-2 and C-3. Loss increases and inductance changes are substantial, and show significant hysteresis which make such effects difficult to account for in dynamic operation.

It can be seen that flux density waveforms with significant dc components can result in large undesirable effects which are difficult to model and predict. Therefore, designers should be aware that, greatly increased core losses may result in magnetic components with NiZn ferrites at HF in designs having large dc bias levels. One useful heuristic is to design such that the dc component is on the same order or less than the tolerable ac magnitude since loss was not observed to escalate under these conditions. For the general case it is unknown whether the dc value alone or its ratio to the ac magnitude is (most) important.

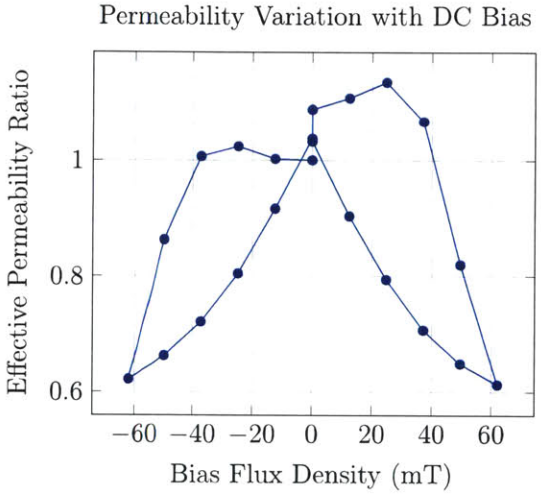



Figure C-3: Ratio of effective permeability $\mu_{eff}$ (with bias) to initial permeability $\mu_{r,i} = 125$ (without bias) of Fair-Rite 61 with ac flux swing held constant at 2.9 mT and dc bias slowly changing. The measurement was done on an ungapped toroid driven at a frequency of 10 MHz. The inductance of the device under test is inferred from the resonant frequency, which changes with dc bias, and the permeability ratio is equal to the inductance ratio.

# Appendix D

# ZVS Buck Modes In The Wide-Range Resonant-Transition Converter

When the converter proposed in Chapter 3 is implemented and operated as explained in Section 3.2, it performs a step-up function that achieves ZVS across the entire input voltage range, $V_{in} < V_{out}$. If the converter is implemented with more active devices, it can perform step-down functions as well, achieving ZVS for any $V_{in} > V_{out}$. In an all-active device implementation, and with the proper operating modes, the converter can achieve ZVS for any combination of input and output voltages.

Figure D-1 shows an all-active device implementation and the operating phases for voltage step-down. If switch SB2 is turned on perpetually (and SB1 is left off perpetually), the simplified circuit is topologically equivalent to a buck converter, which has a resonant-transition mode of operation. With SA1 on, the converter begins in a direct delivery phase which also stores energy in the inductor. After SA1 is turned off, the inductor discharges node A and switch SA2 turns on with zero volts. The subsequent indirect delivery phase lasts until the inductor current reaches zero, at which point SA2 is turned off.[1] The following CL resonant reset phase charges

[1]If SA2 is implemented as a diode, both its zero-voltage turn-on and zero-current turn-off will occur automatically.

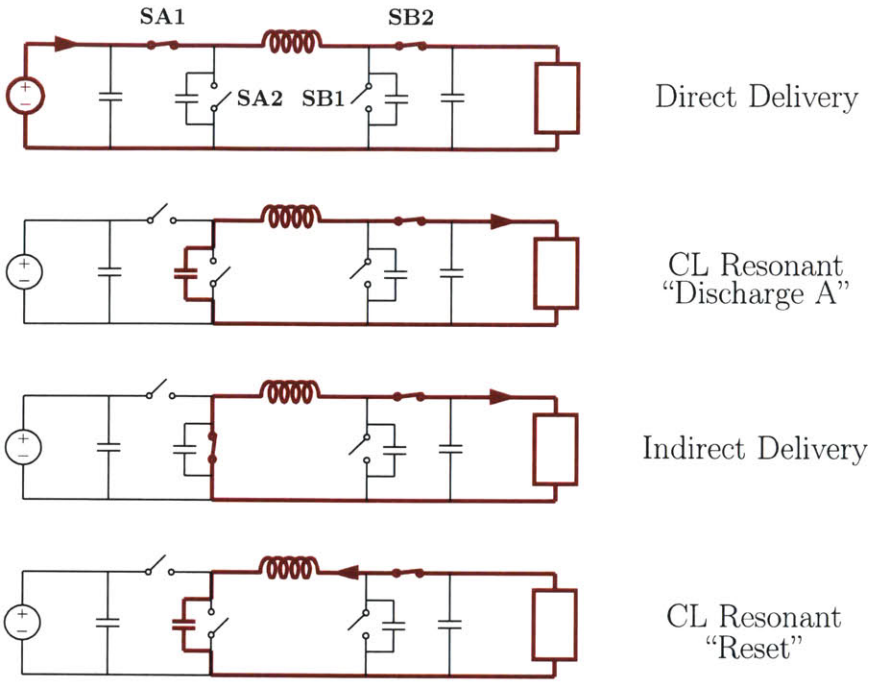



Figure D-1: Resonant-transition buck operating modes for the universal ZVS converter. The indirect delivery phase may be terminated when the inductor current reaches zero or, with SB2 as an active device, may allow some reverse current to ensure ZVS on SA1 for any output voltage. This all-switch implementation can also be operated in either of the boost modes presented in Chapter 3.

node A, at which point SA1 can turn on with reduced voltage across it. However, like the resonant-transition boost converter, this mode only achieves ZVS for a limited conversion ratio. In this case, node A will be charged to (at most) $2V_{out}$, so that this converter can only achieve true ZVS for $V_{out} > V_{in}/2$.

With SA2 implemented as an active device, the converter can achieve ZVS for larger step-down ratios (modified buck mode). This is achieved with similar operation through the direct delivery, CL resonant discharge, and indirect delivery phases. However, when the inductor current reaches zero, switch SA2 is left on to begin to carry reverse current. When SA2 is turned off, the converter enters the CL resonant reset phase with resonant frequency $\omega_0$, but with an initial inductor current which aids in bringing node A all the way to $V_{in}$ to achieve ZVS for SA1. It should be noted that SA2 still achieves ZVS at the end of the CL resonant discharge phase, just as in the resonant-transition buck mode.

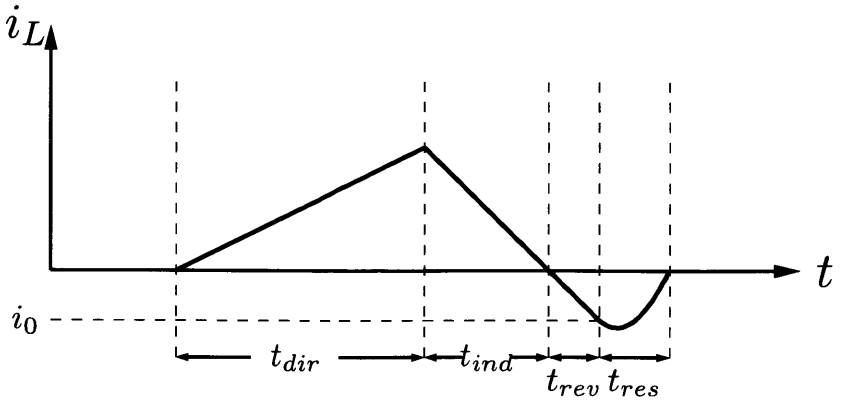



Figure D-2: Inductor current waveform for modified buck mode. The negative inductor current at the end of $t_{rev}$ serves as an initial condition to the resonant transition so that ZVS can be achieved on SA1.

The time period $t_{rev}$ that SA2 must conduct reverse current depends on the circuit parameters and the input/output voltages (though, importantly, it does not require any current sensing). The time evolution of the voltage at node A during the resonant reset phase can be written as:

$$v_A = \frac{i_0}{C\omega_0}\sin(\omega_0 t) - V_{out}\cos(\omega_0 t) + V_{out} \tag{D.1}$$

where it can be verified that $v_a(0) = 0, i_L(0) = C\frac{dv_C}{dt} = i_0$, and the peak voltage with no initial current would be $v_{A,max}|_{i_0=0} = 2V_{out}$ as in the resonant transition buck mode.

The time for node A to reach its peak voltage $t_{res}$ can be found by maximizing (D.1):

$$\begin{aligned} &\frac{i_0}{C}\cos(\omega_0 t_{pk}) + V_{out}\omega_0 \sin(\omega_0 t_{pk}) = 0 \\ &\Rightarrow \omega_0 t_{pk} = \tan^{-1}(\frac{-i_0}{V_{out}\omega_0 C}) \end{aligned} \tag{D.2}$$

Care must be taken such that the $\tan^{-1}$ function does not return an angle in the wrong quadrant. The expected angle lies between 90° (for very high initial current)

and 180° (for zero initial current). This constraint can be applied directly to yield:

$$\omega_0 t_{pk} = 180° - \text{atan}(\frac{i_0}{V_{out}\omega_0 C}) = 180° - \text{atan}(\varphi) \tag{D.3}$$

where $\varphi$ is used as shorthand for the ratio in the argument of the arctangent, and the atan function always returns a value between 0 and 90 degrees for positive arguments. The following trigonometric identities are also useful,

$$\sin(180° - \text{atan}(x)) = \frac{x}{\sqrt{x^2+1}} \qquad \cos(180° - \text{atan}(x)) = \frac{-1}{\sqrt{x^2+1}}$$

Equation (D.2) and the above trigonometric identities are combined with (D.1) to give the peak voltage in terms of initial current:

$$i_0 = V_{out}\sqrt{\frac{C}{L}}\sqrt{(\frac{v_{pk}}{V_{out}} - 1)^2 - 1} \tag{D.4}$$

where, to achieve ZVS, the initial current $i_0$ must be at least enough for the peak voltage to reach the input voltage ($v_{pk} \rightarrow V_{in}$ in (D.4)).

To achieve this inductor current at the beginning of the resonant phase, SA2 must conduct reverse current for $t_{rev}$ in the previous phase (indirect delivery). This time is given by:

$$t_{rev} = \frac{Li_0}{V_{out}} = \sqrt{LC}\sqrt{(\frac{V_{in}}{V_{out}} - 1)^2 - 1} \tag{D.5}$$

For purposes of control, the needed quantity is the total on-time for SA2, which is on for the entire indirect delivery phase $t_{ind} + t_{rev}$. The inductor current during both the direct deliverty and indirect delivery phases is linear in time, so the on-time for SA2 is given by

$$t_{SA2-on} = t_{ind} + t_{rev} = \frac{V_{in} - V_{out}}{V_{out}} t_1 + \sqrt{LC}\sqrt{(\frac{V_{in}}{V_{out}} - 1)^2 - 1} \tag{D.6}$$

Thus, the on time required for SA2 (in order to ultimately achieve ZVS on SA1) can be calculated based on the on time of SA1, passive component values, and the input/output voltages. No current measurement is required, which would be difficult

at high frequency.

# Appendix E

# Wide-Range Resonant-Transition Circuit Analysis

In the modified boost mode of the wide-range resonant-transition converter, the energy storage time $t_{str}$ and the direct delivery time $t_{dir}$ are fixed by the on-time of SA1 and SB1[1]. The resonant phase $t_{res}$ is also fixed by the device capacitances and inductor value.

The remaining time period, the indirect delivery phase $t_{dir}$, can be determined from volt-second balance on the inductor. During the energy storage phase the inductor voltage is $V_{in}$; during the direct delivery phase it is $V_{in} - V_{out}$; during the indirect delivery phase it is $V_{out}$; during the resonant phase the voltage is not constant, but its average may be assumed to be (close to) zero since the equivalent CLC circuit completes a half-period resonant oscillation. Volt-second balance on the inductor yields:

$$V_{in}t_{str} + (V_{in} - V_{out})t_{dir} - V_{out}t_{ind} = 0 \tag{E.1}$$

[1]It is assumed that resonant transitions after SA1 and SB1 are turned off, respectively, are short compared to a switching period, since these resonant transitions begin with an initial inductor current. If these time periods are important, they may be calculated in a manner similar to that used in Appendix D

$$\Rightarrow t_{ind} = t_{dir} + \frac{V_{in}}{V_{out}}(t_{str} + t_{dir}) \tag{E.2}$$

Once the distribution of timing is known, the peak current $i_{pk}$ and the current at the end of the direct delivery phase $i_2$ can be found. From this information, the average power delivered to the output can be computed. Current is only delivered to the output through SB2, so $< i_{out} >=< i_{SB2} >$, which can be computed as:

$$\langle i_{out} \rangle = \frac{1}{T}\left[0.5(i_{pk} + i_2)t_{dir} + 0.5 i_2 t_{ind}\right] \tag{E.3}$$

Substituting $i_{pk} = \frac{V_{in}t_{str}}{L}$ and $i_2 = \frac{V_{out}t_{ind}}{L}$ and simplifying, it is found that

$$\langle i_{out} \rangle = \frac{V_{in}^2 t_{str}^2 + V_{in}^2 t_{str} t_{dir} + V_{in}^2 t_{dir}(t_{str} + t_{dir}) - V_{in} V_{out} t_{dir}^2}{2L(V_{out} t_{str} + V_{out} t_{res} + V_{in}(t_{str} + t_{dir}))} \tag{E.4}$$

As an example, take Fig. 3-10, which has $V_{in} = 355$, $V_{out} = 400$, $t_{str} = 100n$, $t_{dir} = 150n$, $t_{ind} = 75n$, and $t_{res} = 100n$. Plugging into (E.4) yields an output current of $\langle i_{out} \rangle = 0.925$, which corresponds to an output power of $P_{out} = 370$. The actual measured output power was 355 W, which is within 5 % of the calculated value. The error is understood to be even smaller than that, as the above calculation does not take losses into account. With a measured efficiency of $\eta = 98\%$, the calculated output power is within measurement error of the measured output power.

Equation (E.4) also shows that the converter can approximately achieve automatic power factor correction similar to that achieved by the BCM boost PFC. Taking $\langle i_{in} \rangle / V_{in}$ where $\langle i_{in} \rangle = \frac{V_{out}}{V_{in}} \langle i_{out} \rangle$ yields:

$$\frac{\langle i_{in} \rangle}{V_{in}} = \frac{t_{str}^2 + t_{str} t_{dir} + t_{dir}(t_{str} + t_{dir}) - \frac{V_{out}}{V_{in}} t_{dir}^2}{2L(t_{str} + t_{res} + \frac{V_{in}}{V_{out}}(t_{str} + t_{dir}))} \tag{E.5}$$

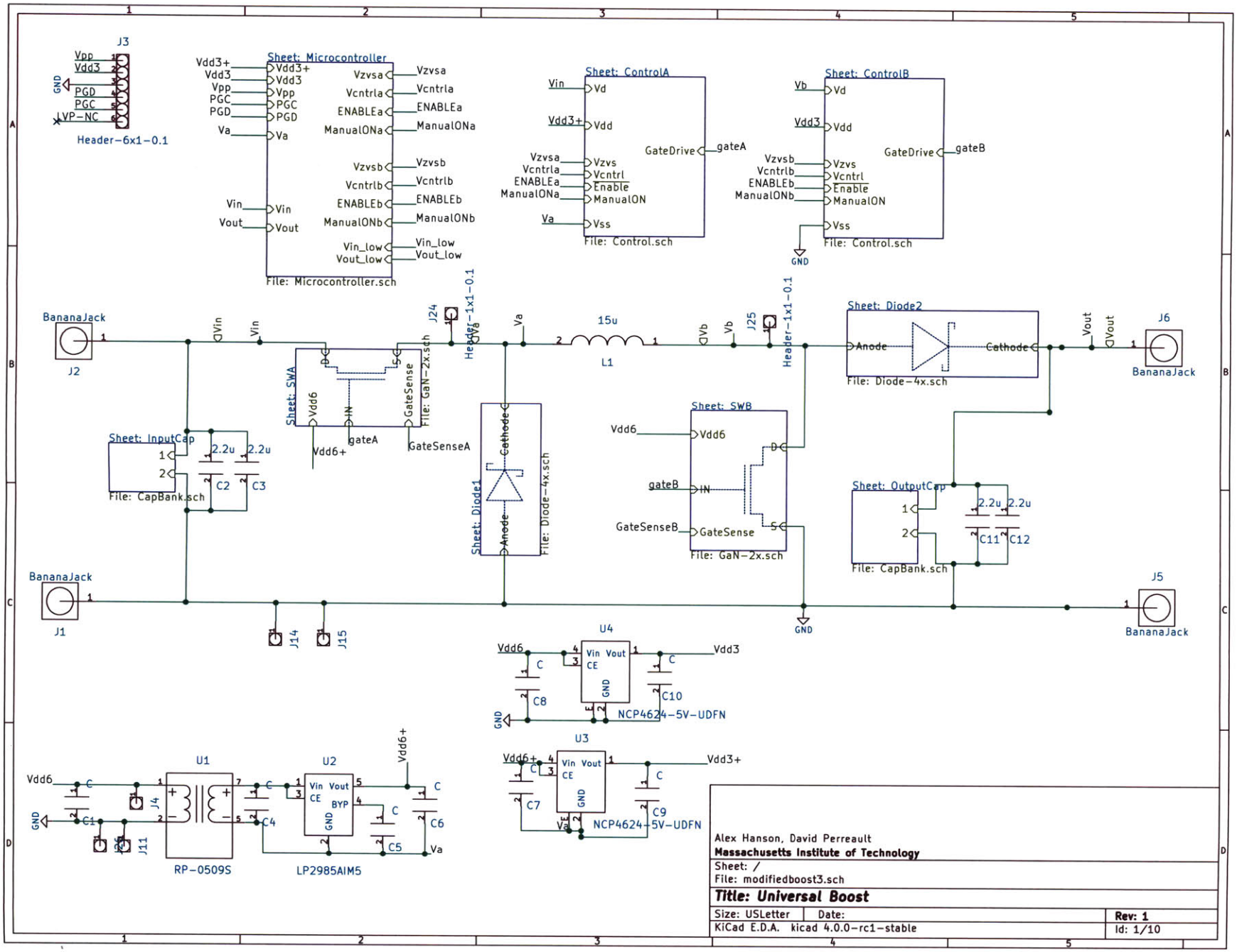
For a converter to operate with unity power factor, its input current must be proportional to its input voltage. It is apparent from (E.5) that this is not quite the case for modified boost mode for the wide-range resonant-transition converter. Nevertheless, the $V_{in}$-dependent terms in (E.5) are somewhat anchored by accompanying constant terms, and may be dwarfed by those terms in many circumstances. Indeed, taking

a reasonable scenario like $t_{dir} = 1.5t_{str}$, $t_{res} = 0.75t_{str}$, it can be shown that the large signal "resistance" of the converter changes by less than 30 % over the range $1 < \frac{V_{out}}{V_{in}} < 2$. Thus the converter may achieve good power factor without changing switch on-times over the course of the line-cycle (allowing for variable on-times on that time scale would naturally permit unity power factor).

# Appendix F

# Converter PCB Schematics

The following pages show the schematics used to generate the prototype PCB for the second prototype implementation. This implementation is closest to the final implementation in the first prototype as well, which had space/pads for components which were ultimately not utilized.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Vpp
Vdd3
GND
PGD
PGC
LVP-NC
Header-6x1-0.1
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Vdd3+
Vdd3
Vpp
PGC
PGD
Va
Vin
Vout
Vzvsa
Vcntrla
ENABLEa
ManualONa
Vzvsb
Vcntrlb
ENABLEb
ManualONb
Vin_low
Vout_low
File: Microcontroller.sch
Sheet: ControlA
Vd
Vdd
Vzvs
Vcntrl
Enable
ManualON
Vss
GateDrive
gateA
File: Control.sch
Sheet: ControlB
Vb
gateB
GND
BananaJack
J2
J24
Header-1x1-0.1
15u
L1
J25
Sheet: Diode2
Anode
Cathode
File: Diode-4x.sch
J6
Sheet: SWA
Vdd6
IN
GateSense
File: GaN-2x.sch
gateA
GateSenseA
Sheet: InputCap
2.2u
C2
C3
File: CapBank.sch
Sheet: Diode1
Sheet: SWB
gateB
GateSenseB
Sheet: OutputCap
C11
C12
J1
J14
J15
J5
U4
Vdd3
C8
C10
NCP4624-5V-UDFN
U3
Vdd3+
C7
C9
U1
U2
J4
J11
C1
C4
C5
C6
RP-0509S
LP2985AIM5
Alex Hanson, David Perreault
Massachusetts Institute of Technology
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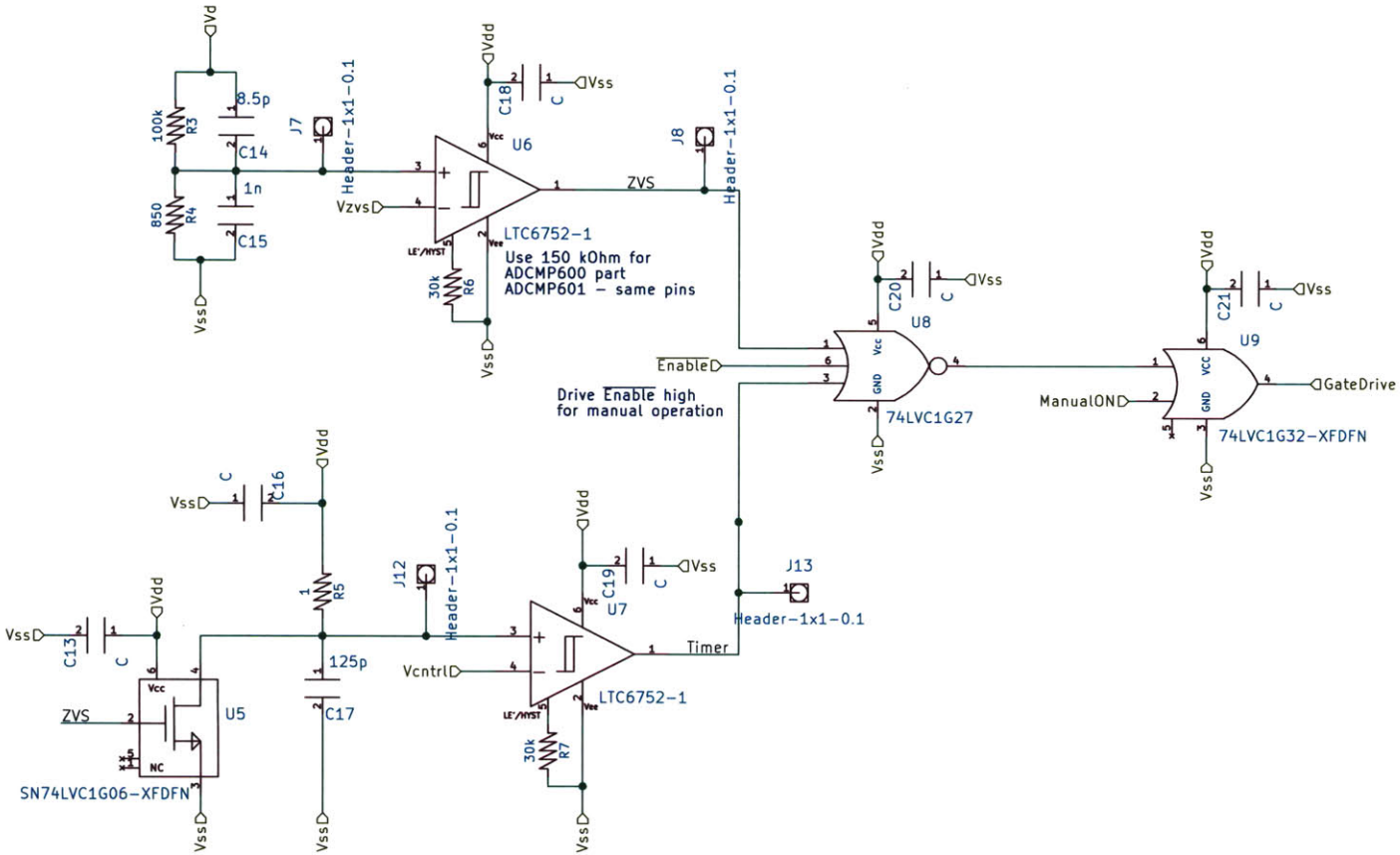
Size: USLetter
Date:
Rev: 1
KiCad E.D.A. kicad 4.0.0-rc1-stable
Id: 1/10

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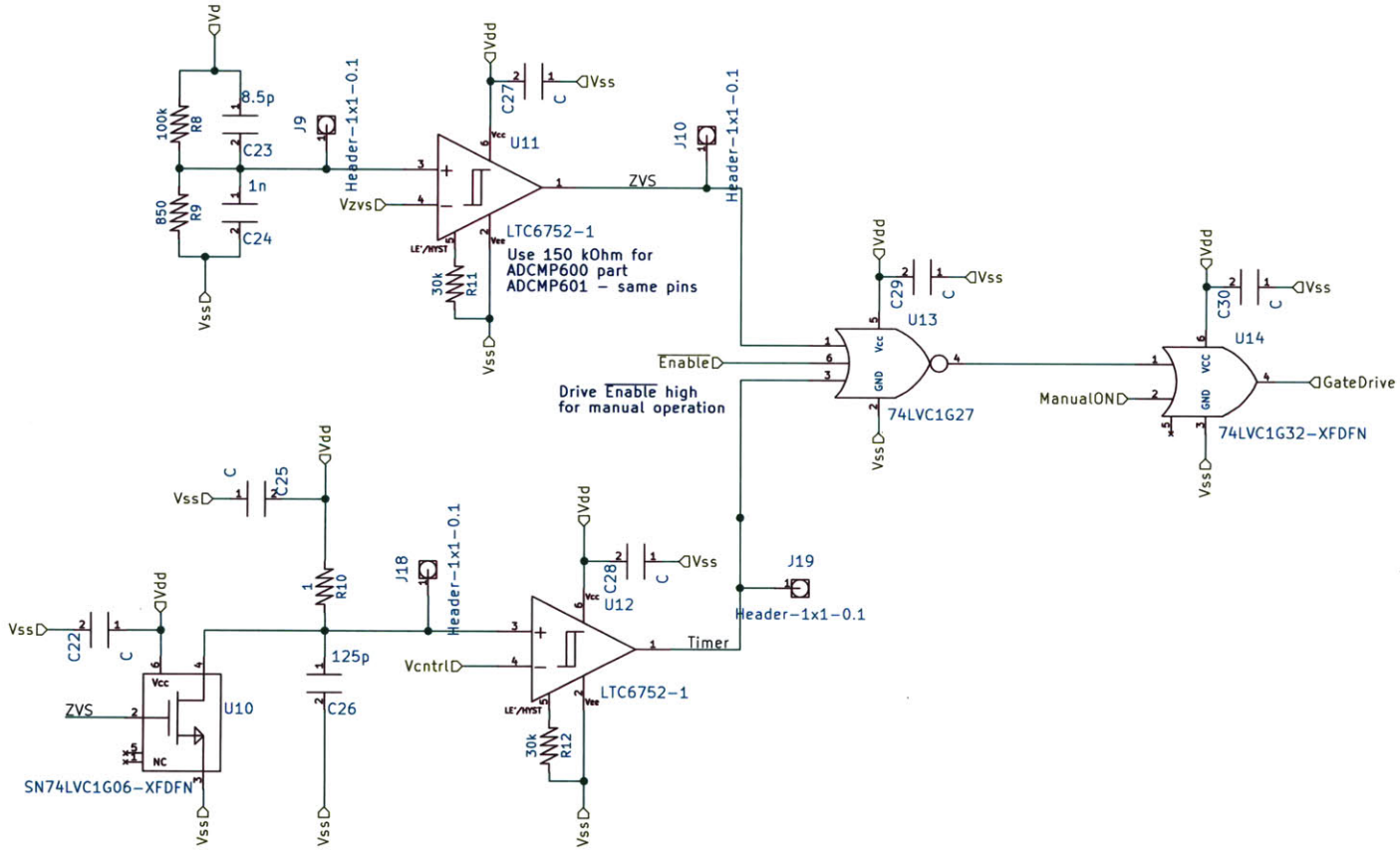


86

| | |
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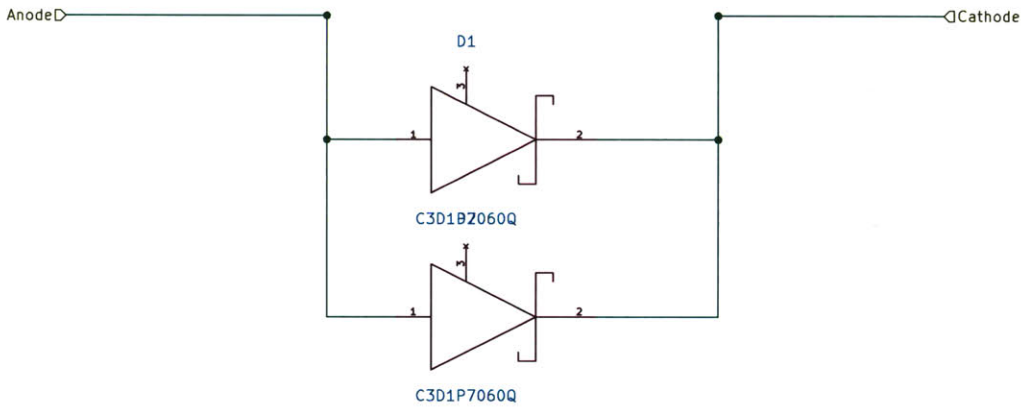


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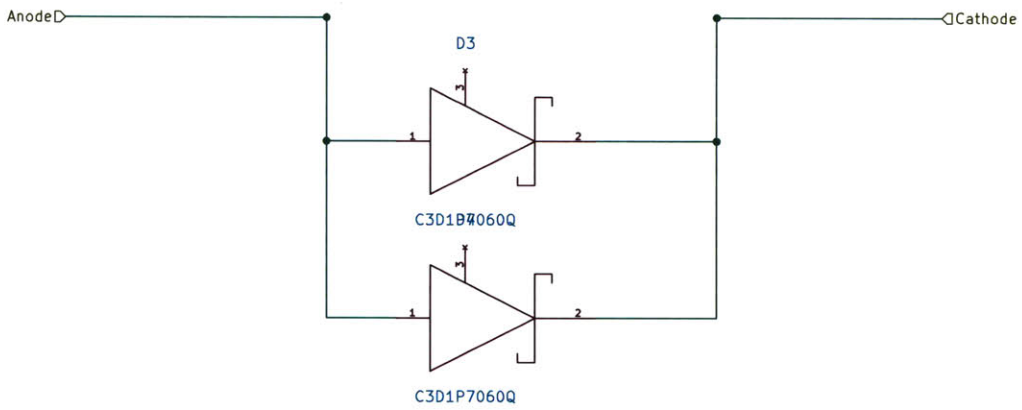


100

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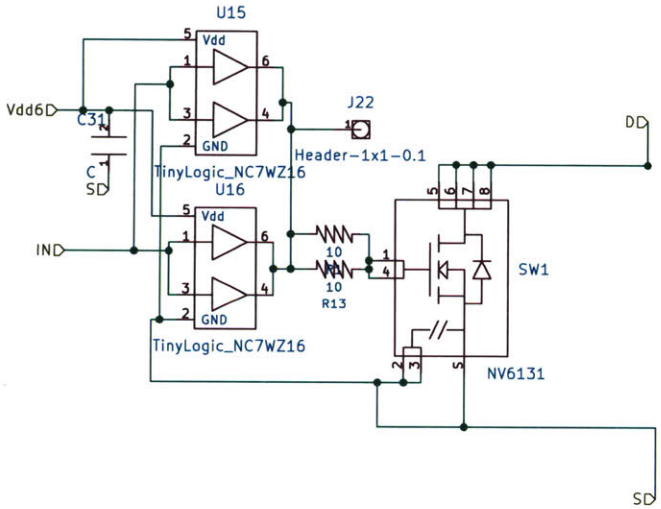


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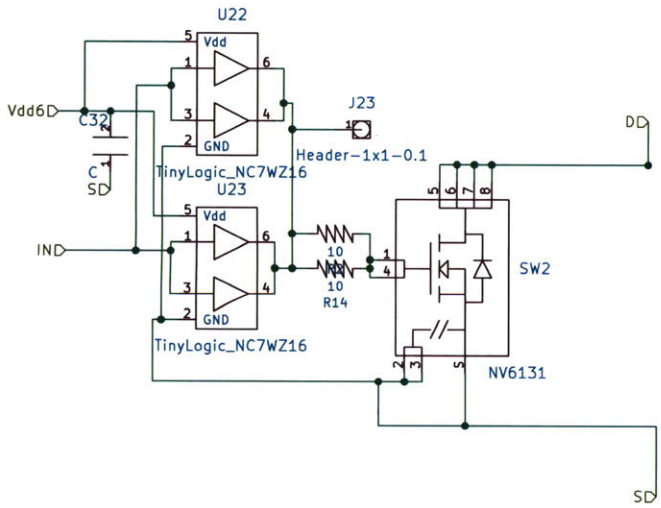


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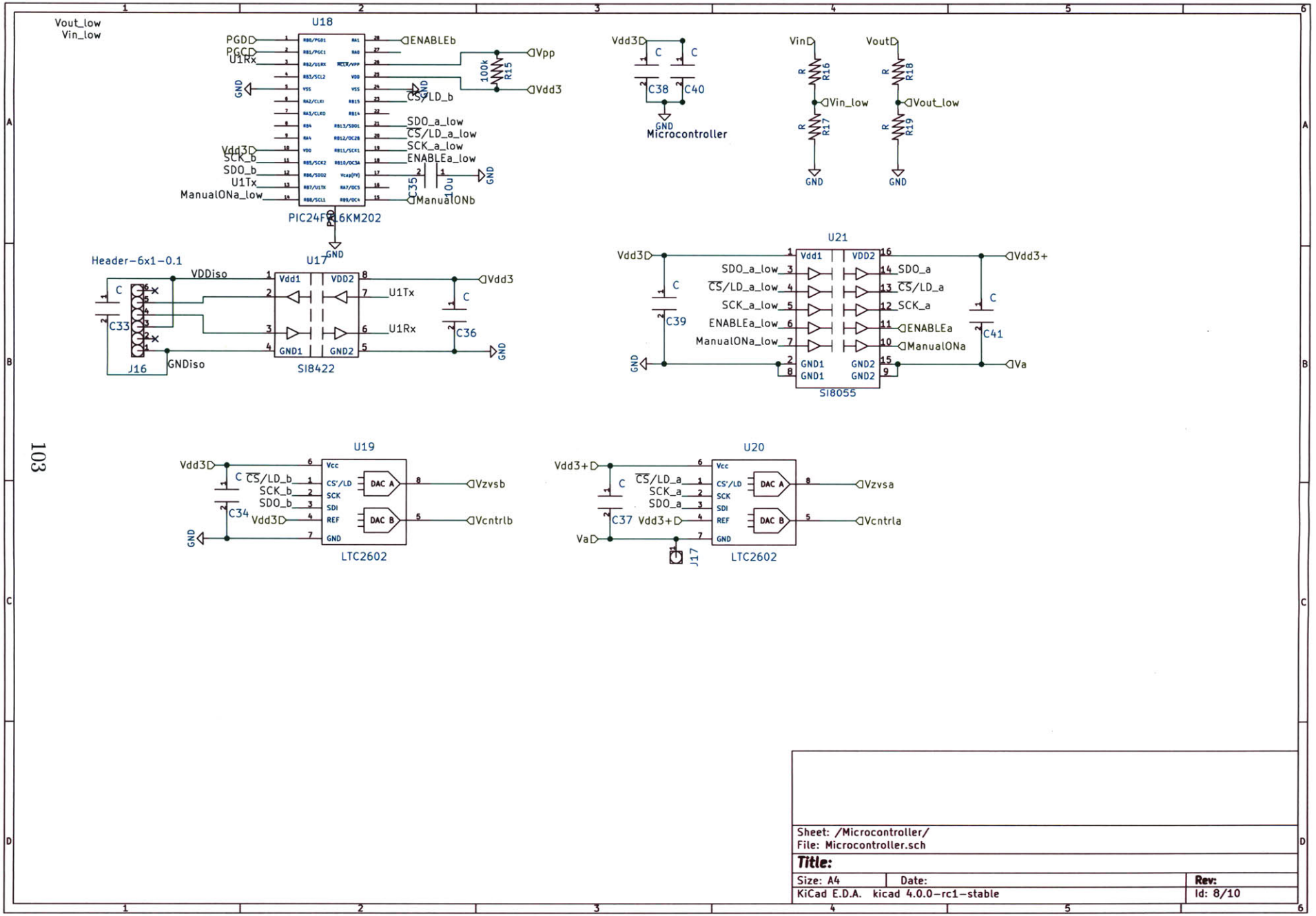


103

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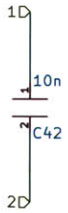


104

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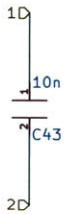


105

| | |
|---|---|
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| File: CapBank.sch | |
| **Title:** | |
| Size: A4 | Date: |
| KiCad E.D.A. kicad 4.0.0-rc1-stable | Id: 10/10 |

# Appendix G

# Microcontroller Code

This appendix contains the microcontroller code used on the PIC24F16KM204 in the first prototype implementation (as the experimental results were presented for that version). The code for the second implementation is relatively unchanged (mostly pin assignments, etc.).

D:/Dropbox (MIT)/ModifiedBoost/uC Code/modifiedboost.c

```
  1 /*
  2  * File:   modifiedboost.c
  3  * Author: Alex
  4  *
  5  * Created on December 9, 2015, 10:56 AM
  6  */
  7
  8
  9 #include "p24f16km204.h"
 10 #include "stdio.h"
 11 #include "string.h"
 12
 13 #define INITPWMPERIOD 16
 14 #define INITPWMON 1
 15
 16
 17 // <editor-fold defaultstate="collapsed" desc="Configuration Bits Setup">
 18
 19
 20
 21 // Configuration Bits to make the part run from Internal FRCDIV
 22 // Oscillator.
 23 _FBS
 24 (
 25         BWRP_OFF & // Boot Segment Write Protect (Disabled)
 26         BSS_OFF // Boot segment Protect (No boot flash segment)
 27         )
 28
 29 _FGS
 30 (
 31         GWRP_OFF & // General Segment Flash Write Protect (General
segment may be written)
 32         GCP_OFF // General Segment Code Protect (No Protection)
 33         )
 34
 35 _FOSCSEL
 36 (
 37         FNOSC_FRCPLL &
 38         //FNOSC_FRCDIV &  // Oscillator Select (8MHz FRC with Postscaler
(FRCDIV))
 39         //Note that the default for CLKDIV is to divide by 2 (4 MHz clock
```

```
=> Fcy = 2 MHz)
  40          SOSCSRC_DIG & // SOSC Source Type (Analog Mode for use with
crystal)
  41          LPRCSEL_HP // LPRC Power and Accuracy (High Power/High Accuracy)
  42          & IESO_OFF // Internal External Switch Over bit (Internal
External Switchover mode enabled (Two-speed Start-up enabled))
  43          )
  44
  45 _FOSC
  46 (
  47          POSCMOD_NONE & // Primary Oscillator Mode (Primary oscillator
disabled)
  48          //OSCIOFNC_IO &   // CLKO Enable Configuration bit (CLKO output
signal enabled)
  49          POSCFREQ_MS & // Primary Oscillator Frequency Range Configuration
bits (Primary oscillator/external clock frequency between 100kHz to 8MHz)
  50          //SOSCSEL_SOSCHP &// SOSC Power Selection Configuration bits
(Secondary Oscillator configured for high-power operation)
  51          FCKSM_CSECME // Clock Switching and Monitor Selection (Clock
Switching and Fail-safe Clock Monitor Enabled)
  52          )
  53
  54 _FWDT
  55 (
  56          WDTPS_PS32768 & // Watchdog Timer Postscale Select bits (1:32768)
  57          FWPSA_PR128 & // WDT Prescaler bit (WDT prescaler ratio of 1:128)
  58          FWDTEN_OFF & // Watchdog Timer Enable bits (WDT disabled in
hardware; SWDTEN bit disabled)
  59          WINDIS_OFF // Windowed Watchdog Timer Disable bit (Standard WDT
selected (windowed WDT disabled))
  60          )
  61
  62 // Warning:
  63 // Always enable MCLRE_ON config bit setting so that the MCLR pin
function will
  64 // work for low-voltage In-Circuit Serial Programming (ICSP). The
Microstick
  65 // programming circuitry only supports low-voltage ICSP. If you disable
MCLR pin
  66 // functionality, a high-voltage ICSP tool will be required to
re-program the
```

```
 67 // part in the future.
 68 _FPOR
 69 (
 70         BOREN_BOR3 & // Brown-out Reset Enable bits (Enabled in hardware;
SBOREN bit disabled)
 71         PWRTEN_ON & // Power-up Timer Enable (PWRT enabled)
 72         I2C1SEL_PRI & // Alternate I2C1 Pin Mapping bit (Default
SCL1/SDA1 Pins for I2C1)
 73         BORV_V18 // Brown-out Reset Voltage bits (Brown-out Reset at
1.8V)
 74         // & MCLRE_ON        // MCLR Pin Enable bit (RA5 input disabled;
MCLR enabled)
 75         )
 76
 77 _FICD
 78 (
 79         ICS_PGx3 // ICD Pin Placement Select (EMUC/EMUD share PGC3/PGD3)
 80         )
 81 // </editor-fold>
 82
 83 // <editor-fold defaultstate="collapsed" desc="Function Prototypes">
 84
 85
 86 void SetupPWM(void);
 87 void EnablePWM(void);
 88 void SetupSPIa(void);
 89 void SetupSPIb(void);
 90 void WriteSPIa(unsigned int* dacinput, char select);
 91 void WriteSPIb(unsigned int* dacinput, char select);
 92 void SetupDAC(void);
 93 void WriteDAC(void);
 94 void SetupADC(void);
 95 void SetupUART(void);
 96 void WriteScreen(char s[50]);
 97 void SetPWMperiod(int i);
 98 void SetPWMon(int i);
 99 void StartupCycle(void);
100 void SetupTrigger(void);
101 void TriggerPulse(void);
102 void WriteVcntrla(void);
103 void WriteVout(void);
```

```
104 void WriteMenu(unsigned int* vcntrlb, unsigned int* vzvsb, unsigned int*
vzvsa, unsigned int* vcntrla);
105 void DisableManual(void);
106 void BuckBoostMode(void);
107
108         // </editor-fold>
109
110
111
112
113
114
115
116 int main(void) {
117
118     //Enable B should be digital, on
119     TRISAbits.TRISA7 = 0;
120     LATAbits.LATA7 = 1;
121
122     //EnableA should be digital, output, on
123     TRISCbits.TRISC8 = 0;
124     LATCbits.LATC8 = 1;
125
126     TRISBbits.TRISB10 = 0; // Set Pin 10 to output
127     LATBbits.LATB10 = 0; // Set Pin 10 to 0 (for now)  Should always be
off unless PWM-ing
128
129     ANSBbits.ANSB6 = 0; //Set pin 42 (OC1F) to digital output
130     TRISBbits.TRISB6 = 0;
131     LATBbits.LATB6 = 0; //Should always be off unless PWM-ing
132
133     CLKDIV = 0x0000; //Stop dividing clock by 2 (to achieve 32 MHz)
134     //char dummy;
135
136     unsigned int vcntrlb = 21000; //changed 2016.04.01 from 21000;//Low
voltage23831;
137     unsigned int vzvsb = 10000; //15760;//Low voltage 15760; //100 Vout,
65 Vin, large inductor, 24000 works
138     unsigned int vcntrla = 24000; //changed 2016.04.01 from 26000;//Low
voltage 30000;
139     unsigned int vzvsa = 31000; //changed 2016.04.01 from 14000;//Low
```

```
voltage 15760;  //100 Vout, 65 Vin, large inductor, 37000 works
 140
 141
 142     SetupUART();
 143     SetupADC();
 144     SetupPWM();
 145     SetupSPIa();
 146     SetupSPIb();
 147     WriteSPIa(&vzvsa,'z');
 148     WriteSPIa(&vcntrla,'c');
 149     WriteSPIb(&vzvsb, 'z');
 150     WriteSPIb(&vcntrlb, 'c');
 151     SetupDAC();
 152
 153
 154     IEC0bits.U1RXIE = 0; //Turn off interrupt (maybe better placed within
menu function)
 155     //Wait forever
 156     while (1) {
 157         WriteMenu(&vcntrlb, &vzvsb, &vzvsa, &vcntrla);
 158     }
 159
 160     return 0;
 161 }
 162
 163
 164
 165
 166 void __attribute__((__interrupt__, no_auto_psv)) _U1RXInterrupt(void) {
 167     char i = 0;
 168
 169     i = U1RXREG;
 170     //U1TXREG = 'a';
 171
 172     U1TXREG = i;
 173
 174     if (i == 'a') {
 175         DAC1DAT = 0b1101000100000000;
 176         U1TXREG = 10; //New Line
 177         U1TXREG = 13; //Carriage Return
 178         U1TXREG = 'a'; //Letter 'a'
```

```
179     }
180
181     if (i == 'b') {
182         DAC1DAT = 0b0110100010000000;
183         U1TXREG = 10;
184         U1TXREG = 13;
185         U1TXREG = 'b';
186     }
187
188
189     IFS0bits.U1RXIF = 0;
190 }
191
192 void __attribute__((__interrupt__, no_auto_psv)) _ADC1Interrupt(void) {
193     char buf[10];
194
195     int ADCVal;
196
197     double ADCFloat = 0;
198
199     U1TXREG = 10;
200     U1TXREG = 13;
201
202     ADCVal = ADC1BUF5;
203     ADCFloat = ((double) ADCVal) * (double) (3.3 / 4096);
204
205
206     sprintf(buf, "%f", ADCFloat);
207
208     WriteScreen(buf);
209
210     //WriteSPI(53620);
211
212     IFS0bits.AD1IF = 0;
213 }
214
215
216
217
218
219 void SetupPWM(void) {
```

```
220     /* Drive RB10 (Pin 8, OC1C) low and make it an output */
221     //ANSBbits.ANSB10 = 0;  //Set Pin 10 to Digital; pin 1 has no analog
connected
222     TRISBbits.TRISB10 = 0; // Set Pin 10 to output
223     LATBbits.LATB10 = 0; // Set Pin 10 to 0 (for now)  Should always be
off unless PWM-ing
224
225     ANSBbits.ANSB6 = 0; //Set pin 42 (OC1F) to digital output
226     TRISBbits.TRISB6 = 0;
227     LATBbits.LATB6 = 0; //Should always be off unless PWM-ing
228
229     Nop();
230
231
232     CCP1CON1L = 0b0010000000000100;
233     //See PIC24FV16KM204 Family Datasheet Page 150
234     //Bit 15: Disable Module (0)    (will enable last thing)
235     //Bit 14: Unimplemented (0) Doesn't really matter
236     //Bit 13: Stop in Idle (1) Doesn't really matter
237     //Bit 12: Reserved (0) Doesn't really matter
238     //Bit 11: Synchronous clock selected (0)
239     //Bit 10-8: System clock selected (000)
240     //Bit 7-6: Time prescale set at 1:1 (00)
241     //Bit 5: 16-bit time base selected (0)
242     //Bit 4: Output compare/PWM selected (0)
243     //Bit 3-0: Dual edge compare mode, buffered (same as PWM) (0101 for
PWM, 0100 for non-buffered)
244
245     CCP1CON1H = 0x0000;
246     //As near as I can tell, nothing I care to use; zeros disable
functions
247
248     CCP1CON2L = 0b1000000000000000;
249     //Bit 15: PWM restarts when complete (1)
250     //Bit 14: Shutdown occurs immediately (vs time base reset) (0)
251     //Bit 13: Unimplemented (0) Doesn't really matter
252     //Bit 12: Normal operation (no manual shutdown) (0)
253     //Bit 11-8: Unimplemented (0000) Doesn't really matter
254     //Bit 7-0: Auto shutdown for none of the 8 sources (00000000)
255
256     CCP1CON2H = 0b0000010000000111;
```

```
257     //Bit 15: Update by output enable bits occurs immediately (0)
258     //Bit 14: Unimplemented (0) Doesn't really matter
259     //Bit 13-8: Link output pins <F-A> to CCP module (100100)  OC1C and
OC1F
260     //Bit 7-6: Level-sensitive Input Capture Mode (00) Doesn't matter for
PWM
261     //Bit 5: Unimplemented (0)
262     //Bit 4-3: Auxiliary Output disabled (00)
263     //Bit 2-0: Input capture source select unused (111)
264
265     CCP1CON3L = 0x0000;
266     //Bit 15-6: Unimplemented (0)
267     //Bit 5-0: Dead time disabled (000000)
268
269     CCP1CON3H = 0b0000000000001010;
270     //Bit 15: Normal output, no trigger required (0)
271     //Bit 14-12: Do not extend one-shot trigger event (000)
272     //Bit 11: Unimplemented (0)
273     //Bit 10-8: Steerable single output mode (all pins same) (000)
274     //Bit 7-6: Unimplemented (00);
275     //Bit 5: Outputs A,C,E are active high (0)
276     //Bit 4: Outputs B,D,F are active high (0) (technically not available
in CCP4)
277     //Bit 3-2: Outputs A,C,E driven inactive when shutdown event occurs
(10)
278     //Bit 1-0: Outputs B,D,F driven inactive when shutdown event occurs
(10) (technically not available)
279
280     CCP1RAL = 0;
281     //Begin the pulse when the timer resets (0 count lag)
282
283     CCP1RBL = 0b00001001;
284     //End the pulse at 100 counts (binary 1100100)
285     //End pulse at 9 counts (binary 00001001))
286
287
288
289     CCP1PRL = 0b00001010;
290     //Configure timebase period to 128 counts (binary 10000000)
291     //Configure timebase to 10 counts (binary 1010))
292
```

```
293     //Duty cycle = CCP4RB / CCP4PRL = 100 / 128 = 0.78
294
295
296 }
297
298 void SetPWMperiod(int i) {
299     CCP1PRL = i;
300 }
301
302 void SetPWMon(int i) {
303
304     if (i > CCP1PRL) {
305         char buf[50];
306         sprintf(buf, "Error: on-time %d > period %d", i, CCP1PRL);
307         WriteScreen(buf);
308         return;
309     }
310
311     CCP1RBL = i;
312 }
313
314 void EnablePWM(void) {
315     CCP1TMRL = 0;
316     //Initialize timer prior to enable module
317     CCP1CON1Lbits.CCPON = 1;
318 }
319
320 void SetupSPIb(void) {
321     //ANSBbits.ANSB11 = 0; // (pin9 is not analog connected)
322     TRISBbits.TRISB11 = 0;
323
324     ANSBbits.ANSB13 = 0; //(pin 11)
325     TRISBbits.TRISB13 = 0;
326
327     ANSBbits.ANSB15 = 0; // (pin 15)
328     TRISBbits.TRISB15 = 0;
329     LATBbits.LATB15 = 1; //Idle high
330
331     SSP1STAT = 0b0000000001000000;
332     //Status register for MSSP1
333     //Bit 6: CKE - some confusion on this point, but setting to 1 to
```

```
match graph on 58 page 18
 334
 335     SSP1CON1 = 0b0000000000000000;
 336     //Bit 15-8: Unimplemented (00000000)
 337     //Bit 7: WCOL No Collision (0)
 338     //Bit 6: SSPOV No overflow (0)
 339     //Bit 5: SSPEN Not enabled (0) (will enable last thing)
 340     //Bit 4: CKP clock idle low (0)
 341     //Bit 3-0: SSPM<3:0> SPI master mode with clock Fosc/2 = Fcy (0000)
 342
 343     SSP1CON3 = 0b0000000000000000;
 344     //Bit 15-8: Unimplemented (00000000)
 345     //Bit 7: ACKTIM unused in SPI (0)
 346     //Bit 6: PCIE unused in SPI (0)
 347     //Bit 5: SCIE unused in SPI (0)
 348     //Bit 4: BOEN unused in SPI master (0)
 349     //Bit 3: SDAHT unused in SPI (0)
 350     //Bit 2: SBCDE unused in SPI (0)
 351     //Bit 1: AHEN unused in SPI (0)
 352     //BIt 0: DHEN unused in SPI (0)
 353
 354     SSP1CON1bits.SSPEN = 1;
 355 }
 356
 357 void SetupSPIa(void) {
 358     //ANSCbits.ANSC5 = 0; //
 359     TRISCbits.TRISC5 = 0;
 360
 361     //ANSCbits.ANSC4 = 0; //(pin 11)
 362     TRISCbits.TRISC4 = 0;
 363
 364
 365     //ANSAbits.ANSA9 = 0; // (pin 15)
 366     TRISAbits.TRISA9 = 0;
 367     LATAbits.LATA9 = 1; //Idle high
 368
 369     SSP2STAT = 0b0000000001000000;
 370     //Status register for MSSP2
 371     //Bit 6: CKE - some confusion on this point, but setting to 1 to
match graph on 58 page 18
 372
```

```
373     SSP2CON1 = 0b0000000000000000;
374     //Bit 15-8: Unimplemented (00000000)
375     //Bit 7: WCOL No Collision (0)
376     //Bit 6: SSPOV No overflow (0)
377     //Bit 5: SSPEN Not enabled (0) (will enable last thing)
378     //Bit 4: CKP clock idle low (0)
379     //Bit 3-0: SSPM<3:0> SPI master mode with clock Fosc/2 = Fcy (0000)
380
381     SSP2CON3 = 0b0000000000000000;
382     //Bit 15-8: Unimplemented (00000000)
383     //Bit 7: ACKTIM unused in SPI (0)
384     //Bit 6: PCIE unused in SPI (0)
385     //Bit 5: SCIE unused in SPI (0)
386     //Bit 4: BOEN unused in SPI master (0)
387     //Bit 3: SDAHT unused in SPI (0)
388     //Bit 2: SBCDE unused in SPI (0)
389     //Bit 1: AHEN unused in SPI (0)
390     //BIt 0: DHEN unused in SPI (0)
391
392     SSP2CON1bits.SSPEN = 1;
393 }
394
395
396
397 void WriteSPIb(unsigned int* dacinput, char select) {
398     //Write Sequence
399     //Writing to SSP1BUF should get 8 bits into the transmit register
400     //Writing 3 times should transmit 24 bits, or one "word" for the
LTC2602
401     int i;
402     unsigned int temp;
403     //while(SSP1STATbits.BF == 1);  This line (sometimes) caused infinite
delays
404
405     int mode;
406
407
408
409     //    char buf[10];
410     //    sprintf(buf,"%u",*dacinput);
411     //    WriteScreen("\n\r");
```

```
412     //    WriteScreen(buf);
413
414     switch (select) {
415         case 'c':
416             mode = 0b0000000000110001; //VcntrlB
417             break;
418         case 'z':
419             mode = 0b0000000000110000; //VcntrlB
420             break;
421         default:
422             ;
423     }
424
425
426
427
428
429
430
431
432
433
434     LATBbits.LATB15 = 0; //Active low
435
436     SSP1BUF = mode;
437     //SSP1BUF = 0x0000 & p[0];
438     //Data out
439     //Bit 15-8: Unused for 8 bit SPI I think
440     //Bit 7-4: COMMAND C<3:0> (0011) - Write and update module n
441     //Bit 3-0: ADDRESS A<3:0> )0001) - DAC B
442
443     //while(SSP1STATbits.BF == 1);
444     for (i = 0; i < 20; i++) {
445     }
446
447     temp = *dacinput;
448     temp = temp >> 8;
449     //temp = temp & 0x0011;
450
451     //    sprintf(buf,"%u",temp);
452     //    WriteScreen("\n\r");
```

```
453     //    WriteScreen(buf);
454
455     //SSP1BUF = 0b0000000011010001;
456     //SSP1BUF = 0x0000 & temp;
457     SSP1BUF = temp;
458     //Bit 15-8: Unused for 8 bit SPI I think
459     //Bit 7-0; 8 MSBs of data
460
461     for (i = 0; i < 20; i++) {
462     }
463
464     //while(SSP1STATbits.BF == 1);
465
466     temp = (*dacinput) & 0x0011;
467     //SSP1BUF = 0b0000000001110100;
468     //SSP1BUF = 0x00 & p[0];
469     SSP1BUF = temp;
470     //Bit 15-8: Unused for 8 bit SPI I think
471     //Bit 7-0; 8 LSBs of data
472
473     for (i = 0; i < 20; i++) {
474     }
475
476     LATBbits.LATB15 = 1; //back to idle high
477     //TriggerPulse();
478 }
479
480
481 void WriteSPIa(unsigned int* dacinput, char select) {
482     //Write Sequence
483     //Writing to SSP1BUF should get 8 bits into the transmit register
484     //Writing 3 times should transmit 24 bits, or one "word" for the
LTC2602
485     int i;
486     unsigned int temp;
487     //while(SSP1STATbits.BF == 1);  This line (sometimes) caused infinite
delays
488
489     int mode;
490
491
```

```
492
493     //    char buf[10];
494     //    sprintf(buf,"%u",*dacinput);
495     //    WriteScreen("\n\r");
496     //    WriteScreen(buf);
497
498     switch (select) {
499         case 'c':
500             mode = 0b0000000000110001; //VcntrlB
501             break;
502         case 'z':
503             mode = 0b0000000000110000; //VcntrlB
504             break;
505         default:
506             ;
507     }
508
509
510
511
512
513
514
515
516
517
518     LATAbits.LATA9 = 0; //Active low
519
520     SSP2BUF = mode;
521     //SSP1BUF = 0x0000 & p[0];
522     //Data out
523     //Bit 15-8: Unused for 8 bit SPI I think
524     //Bit 7-4: COMMAND C<3:0> (0011) - Write and update module n
525     //Bit 3-0: ADDRESS A<3:0> )0001) - DAC B
526
527     //while(SSP1STATbits.BF == 1);
528     for (i = 0; i < 20; i++) {
529     }
530
531     temp = *dacinput;
532     temp = temp >> 8;
```

```
533     //temp = temp & 0x0011;
534
535     //    sprintf(buf,"%u",temp);
536     //    WriteScreen("\n\r");
537     //    WriteScreen(buf);
538
539     //SSP1BUF = 0b0000000011010001;
540     //SSP1BUF = 0x0000 & temp;
541     SSP2BUF = temp;
542     //Bit 15-8: Unused for 8 bit SPI I think
543     //Bit 7-0; 8 MSBs of data
544
545     for (i = 0; i < 20; i++) {
546     }
547
548     //while(SSP1STATbits.BF == 1);
549
550     temp = (*dacinput) & 0x0011;
551     //SSP1BUF = 0b0000000001110100;
552     //SSP1BUF = 0x00 & p[0];
553     SSP2BUF = temp;
554     //Bit 15-8: Unused for 8 bit SPI I think
555     //Bit 7-0; 8 LSBs of data
556
557     for (i = 0; i < 20; i++) {
558     }
559
560     LATAbits.LATA9 = 1; //back to idle high
561     //TriggerPulse();
562 }
563
564
565
566 void SetupDAC(void) {
567     ANSBbits.ANSB14 = 0; // Set B14 (Pin 14) to digital
568     //Assume DAC will take over PIN 14 when enabled
569
570     DAC2CON = 0b0000100010000010;
571     //Bit 15: DAC enable (0) turn on last thing
572     //Bit 14: Unimplemented (0)
573     //Bit 13: DAC does not stop in idle (0)
```

```
574     //Bit 12: Dac does not stop in sleep (0)
575     //Bit 11: DAC data left justified (1)
576     //Bit 10-9: Unimplemented (00)
577     //Bit 8: DAC output updates when DAT written (0)
578     //Bit 7: DAC output buffer eneabled (1)
579     //Bit 6-2: DAC trigger 1 (00000) Should be unused b/c Bit 8  = 0
580     //Bit 1-0: Select AVdd as positive reference (10)
581
582
583     DAC2DAT = 0b1101000100000000;
584     //Bit 15-10: Data for 209 which is (209/2^8)*3.3 = 2.7 V
585     //Bit 9-0: Unimplemented b/c left justified (00000000)
586
587
588
589     DAC2CONbits.DACEN = 1;
590     //Enable module
591 }
592
593 void WriteDAC(void) {
594     DAC2DAT = 0b1101000100000000;
595     //Bit 15-10: Data for 209 which is (209/2^8)*3.3 = 2.7 V
596     //Bit 9-0: Unimplemented b/c left justified (00000000)
597 }
598
599 void SetupADC(void) {
600     ANSBbits.ANSB8 = 1;
601     TRISBbits.TRISB8 = 1;
602     //Set Pin 44 = RB8 (Vout_low) as analog input
603
604     ANSBbits.ANSB3 = 1;
605     TRISBbits.TRISB3 = 1;
606     //Set PIN 24 (Vctrl_a_pot) as analog, set as input
607
608
609     AD1CON1 = 0b0000010001110110;
610     //Bit 15: ADON - AD is off (0) (will turn on last thing)
611     //Bit 14: Unimplemented (0)
612     //Bit 13: ADSIDL - AD does not stop in idle (0)
613     //Bit 12: Values stored according to source (0) - not implemented in
this family
```

```
 614     //Bit 11: Extended DMA features off (0) - not implemented in this
family
 615     //Bit 10: MODE12 - 12 bit operation (1)
 616     //Bit 9-8: FORM<1:0> - Data format absolute decimal, unsigned, right
justified (00)
 617     //Bit 7-4: SSRC<3:0> - SAMP bit cleared after Tad clock cycles (auto
convert mode) (0111)
 618     //Bit 3: Unimplemented (0)
 619     //Bit 2: ASAM - Automatically sample after last conversion (1)
(automatically sets Bit 1)
 620     //Bit 1: SAMP (1)
 621     //Bit 0: DONE - AD conversion status bit (0) (read bit only anyway)
 622
 623     AD1CON2 = 0b0000110011111000;
 624     //Bit 15-14: PVCFG<1:0> - Reference value at Vdd (00)
 625     //Bit 13: NVCFG0 - Negative reference at Vss (0)
 626     //Bit 12: Offset calibration with normal inputs (0) - unimplemented
in this family
 627     //Bit 11: BUFREGEN - Buffer decided by converted channel (1)
 628     //Bit 10: CSCNA - Do Scan inputs (1)
 629     //Bit 9-8: Unimplemented (00)
 630     //Bit 7: BUFS - Buffer fill status bit (0) (read-only anyway)
 631     //Bit 6-2: SMPI<4:0> - Interrupts after each conversion (00000)
(every other 00001)
 632     //Bit 1: BUFM - Split buffer mode off (0) (not applicable if Bit 11
set anyway)
 633     //Bit 0: ALTS - Alternate input mode select off (0)
 634
 635     AD1CON3 = 0b0001111100011111;
 636     //Bit 15: ADRC - Use system clock (0)
 637     //Bit 14: EXTSAM - (0) (status bit for A/D still sampling or not past
SAMP=0)
 638     //Bit 13: Charge pump disabled (0) - reserved in this family
 639     //Bit 12-8: SAMC<4:0> - Auto-sample time 1 Tad (00001) (1 Tad (00000)
 640     //Bit 7-0: ADCS<7:0> - A/D conversion clock Tad = 8 Tcy (00000111) (1
Tcy 00000000)
 641
 642
 643     //AD1CON4 not implemented
 644
 645     AD1CON5 = 0b0000000000000000;
```

```
646     //Bit 15: Auto scan enable (1)
647     //Bit 14: Full power after scan (0)
648     //Bit 13: CTMU not enabled by A/D (0)
649     //Bit 12: Band gap not enabled by A/D (0)
650     //Bit 11: On chip regulator not enabled by A/D (0)
651     //Bit 10: Unimplemented (0)
652     //Bit 9-8: No interrupt for threshold detect(00)
653     //Bit 7-4: Unimplemented (0000)
654     //Bit 3-2: Write determined by buffer register (00) (legacy)
655     //Bit 1-0: Less than mode (00)
656
657     AD1CHS = 0b0000000000000101; //Ignored when CSCNA is enabled
658     //Bit 15-13: AVss set as negative input select Sample B (000)
659     //Bit 12-8: MUX B positive input is AN0 (00000)
660     //Bit 7-5: Sample A channel 0 negative in put is AVss (000)
661     //Bit 4-0: Channel 0 positive input is AN5 (00101)
662
663     //AD1CHITH - appears to be a read-only status register
664     //AD1CHITL - appears to be a read-only status register
665
666     AD1CSSH = 0b0000000000010000;
667     //Bit 15: Unimplemented (0);
668     //Bit 14-10: A/D input selection (00000)
669     //Bit 9-8: Unimplemented (0);
670     //Bit 7-0: A/D input selection (00010000)
671     //Want AN20 = Pin 44 = Vout
672
673     AD1CSSL = 0b0000000000100000; //Enabled
674     //Bit 15-0: A/D input scan selection, only AN5 (000000000010000)
675     // or none (0000000000000000)
676
677
678
679     AD1CTMENH = 0b0000000000000000;
680     //Bit 15-8: Unimplemented (0)
681     //Bit 7-0: CTMEN<23:16> - CTMU disabled for each channel (00000000)
682
683     AD1CTMENL = 0b0000000000000000;
684     //Bit 15-0: CTMEN<15:0> - CTMU disabled for all channels (0)
685
686     IFS0bits.AD1IF = 0;
```

```
687     IEC0bits.AD1IE = 0; //Do not enable interrupts
688
689     AD1CON1bits.ADON = 1;
690     //Enable ADC
691 }
692
693 void SetupUART(void) {
694     U1MODE = 0b0100000010000000;
695     //Bit 15: UEN - UART disable (0) (will turn on last)
696     //Bit 14: UFRZ - freeze in debug mode on (1)
697     //Bit 13: USIDL - Do not stop in idle mode (0)
698     //Bit 12: IREN - IrDA disabled (0)
699     //Bit 11: RTSMD - flow control mode (0) (won't use those pins anyway)
700     //Bit 10: ALTIO - do not use alternate pins (0)
701     //Bit 9-8: UEN<1:0> - Enable RX and TX pins; not CTS, RTS or BCLK
(00)
702     //Bit 7: WAKE - wake up during sleep enabled (1)
703     //Bit 6: LPBACK - loopback mode disabled (0)
704     //Bit 5: ABAUD - one-time auto baud measurement not taking place (0)
705     //Bit 4: RXINV - idle state is '1' (0)
706     //Bit 3: BRGH - low speed (0)
707     //Bit 2-1: PDSEL<1:0> - 8 bit data, no parity (00)
708     //Bit 0: STSEL - one stop bit (0)
709
710     U1STA = 0b0000010000000000;
711     //Bit 15,13: UTXISEL<1:0> - interrupt when transfer to Tshift (00)
712     //Bit 14: UTXINV - transmit idle state is '1' (0)
713     //Bit 12: Unimplemented (0)
714     //Bit 11: UTXBRK - sync break transmission disabled (0)
715     //Bit 10: UTXEN - transmitter disabled (0) (will enable later)
716     //Bit 9: UTXBF - status bit for full buffer register (0)
717     //Bit 8: TRMT - status bit for full shift register (0)
718     //Bit 7-6: URXISEL<1:0> - interrupt flag set when character received
(00)
719     //Bit 5: ADDEN - address detect mode disabled (0)
720     //Bit 4: RIDLE - status bit for receiver idle (0)
721     //Bit 3: PERR - status bit for parity error (0)
722     //Bit 2: FERR - status bit for framing error (0)
723     //Bit 1: OERR - status bit for buffer overflow (0)
724     //Bit 0: URXDA - status bit for receive buffer available (0)
725
```

```
726     U1RXREG = 0b0000000000000000;
727     //Bit 15-9: Unimplemented (0000000)
728     //Bit 8: Data bit 8 in 9-bit mode (0)
729     //Bit 7-0: Data bits 7-0 (00000000)
730     //Not sure if I can set these bits; just helps bookkeep in code
731
732     U1TXREG = 0x0000000000000000;
733     //Bit 15-9: Unimplemented (0000000)
734     //Bit 8: Data bit 8 in 9-bit mode (0)
735     //Bit 7-0: Data bits 7-0 (00000000)
736
737     U1BRG = 0b000000001100111;
738     //Bit 15-0: Baud Rate Generator Divisor bits
739     //For 8 MHz internal clock, Fcy = 4 MHz -- see baud rate tables
740     //Choose BRG = 0d25 in this case for Baud = 9600
741     //0d25 = 0b0000000000011001
742     //Actual measured Fcy = 2 MHz: for Baud of 9600 with BRGH=0, want
0d12
743     //0d13 = 0000000000001100;
744     //Fcy = F/2.  F = 4 MHz if divided by 2 in non-volatile memory.
745     //Works at 4 MHz: 0b000000000001100 corresponds to 9600
746     //At 32 MHz (Fcy = 16 MHz) for 9600, want 0d103 => 1100111
747
748     //Enable the U1 module
749     U1MODEbits.UARTEN = 1;
750     Nop();
751
752     //Enable transmit for the U1 module
753     U1STAbits.UTXEN = 1;
754     Nop();
755
756     //Turn off
757     IFS0bits.U1RXIF = 0;
758     IFS0bits.U1TXIF = 0;
759     IEC0bits.U1RXIE = 1;
760     IEC0bits.U1TXIE = 0;
761     IPC2bits.U1RXIP = 0b111;
762 }
763
764 void WriteMenu(unsigned int* vcntrlb, unsigned int* vzvsb, unsigned int*
vzvsa, unsigned int* vcntrla) {
```

```
765     char selection;
766
767     WriteScreen("\n\n\n\n\r***Modified Boost Menu***");
768     WriteScreen("\n\ra:IncVzvsB\tz:DecVzvsB");
769     WriteScreen("\n\rs:IncVzvsA\tx:DecVzvsA");
770
771     WriteScreen("\n\rd:PwmPeriod+\tc:PwmPeriod-");
772     WriteScreen("\n\rf:PwmOn+\tv:PwmOn-");
773     WriteScreen("\n\rg:IncVcntrlb\tb:DecVcntrlb");
774     WriteScreen("\n\rh:IncVcntrla\tn:DecVcntrla");
775     WriteScreen("\n\rq:Startup\tw:BuckBoostMode");
776     WriteScreen("\n\re:ManualDisable\ty:none");
777
778     WriteScreen("\n\n\r");
779     while (U1STAbits.URXDA == 0) {
780     }
781     selection = U1RXREG;
782     U1TXREG = selection;
783     //WriteScreen(": ");
784
785
786
787     switch (selection) {
788         case 'a':
789             //WriteScreen("Inc VzvsB");
790             *vzvsb = *vzvsb + 1000;
791             WriteSPIb(vzvsb, 'z');
792             break;
793         case 'z':
794             //WriteScreen("Inc VzvsB");
795             *vzvsb = *vzvsb - 1000;
796             WriteSPIb(vzvsb, 'z');
797             break;
798         case 's':
799             *vzvsa = *vzvsa + 1000;
800             WriteSPIa(vzvsa,'z');
801             break;
802         case 'x':
803             *vzvsa = *vzvsa - 1000;
804             WriteSPIa(vzvsa,'z');
805             break;
```

```
806         case 'q':
807             //WriteScreen("Startup Cycle Begin");
808             StartupCycle();
809             DisableManual();
810             break;
811         case 'd':
812             //WriteScreen("Inc PWM Period");
813             SetPWMperiod(CCP1PRL + 1);
814             break;
815         case 'c':
816             //WriteScreen("Dec PWM Period");
817             SetPWMperiod(CCP1PRL - 1);
818             break;
819         case 'f':
820             //WriteScreen("Inc PWM On");
821             SetPWMon(CCP1RBL + 1);
822             break;
823         case 'v':
824             //WriteScreen("Dec PWM On");
825             SetPWMon(CCP1RBL - 1);
826             break;
827         case 'g':
828             //WriteScreen("Inc VcntrlB");
829             *vcntrlb = *vcntrlb + 1000;
830             WriteSPIb(vcntrlb, 'c');
831             break;
832         case 'b':
833             //WriteScreen("Dec VcntrlB");
834             *vcntrlb = *vcntrlb - 1000;
835             WriteSPIb(vcntrlb, 'c');
836             break;
837         case 'h':
838             *vcntrla = *vcntrla + 1000;
839             WriteSPIa(vcntrla,'c');
840             break;
841         case 'n':
842             *vcntrla = *vcntrla - 1000;
843             WriteSPIa(vcntrla,'c');
844             break;
845         case 'e':
846             //WriteScreen("Manual Off");
```

```
847                 DisableManual();
848                 break;
849             case 'w':
850                 //WriteScreen("Buck Boost On");
851                 BuckBoostMode();
852                 break;
853             default:
854                 WriteScreen("Invalid Selection");
855         }
856
857
858
859 }
860
861 void WriteScreen(char s[50]) {
862     char *p;
863     p = s;
864     while (*p) {
865         while (!(U1STAbits.TRMT)) {
866         }
867         U1TXREG = *p++;
868     }
869 }
870
871 void StartupCycle(void) {
872     int n; //a count variable
873     int j; //a count variable
874
875     //EnableB should be digital, output, on
876     TRISAbits.TRISA7 = 0;
877     LATAbits.LATA7 = 1;
878
879     //EnableA should be digital, output, on
880     TRISCbits.TRISC8 = 0;
881     LATCbits.LATC8 = 1;
882
883
884     //Buck Mode
885     CCP1CON2Hbits.OCFEN = 1; //ManualON A connected to PWM
886     CCP1CON2Hbits.OCCEN = 0; //ManualON B disconnected from PWM, normal
digital IO
```

```
887
888
889     SetPWMperiod(INITPWMPERIOD); //Setup initial PWM period
890     SetPWMon(INITPWMON); //Setup initial PWM on time (ON = D*T)
891     EnablePWM(); //Activate PWM
892
893
894
895     //Bring buck duty cycle up to just under 1
896     for (n = INITPWMON; n < INITPWMPERIOD; n++) {
897         SetPWMon(n);
898         for (j = 0; j < 50; j++) {
899         } //Delay
900     } //End duty cycle for loop
901
902     //Switch to boost mode
903     CCP1CON2Hbits.OCFEN = 0; //ManualON A
904     CCP1CON2Hbits.OCCEN = 1; //ManualON B
905
906     //Technically the converter is boosting with D close to 1, but this
will last for less than a cycle
907
908     //Bring boost duty cycle up so that Vo/Vi = 3
909     for (n = 1; n < INITPWMPERIOD * 9 / 16; n++) {
910         SetPWMon(n);
911         for (j = 0; j < 50; j++) {
912         }
913     }
914
915     TriggerPulse();
916
917 }
918
919 void SetupTrigger(void) {
920     //ANSAbits.ANSA10 = 0; //Set RA4 = Pin 34 to digital
921     TRISAbits.TRISA10 = 0; //Set RA4 = Pin 34 to output
922     LATAbits.LATA10 = 0; //Set RA4 = Pin 34 to 0 to initialize
923     //Or RA10 = Pin 12
924
925 }
926
```

```
927 void TriggerPulse(void) {
928
929     LATAbits.LATA10 = 1;
930
931     LATAbits.LATA10 = 0;
932 }
933
934 void WriteVout(void) {
935     int ADCVal;
936     double ADCFloat;
937     char buf[10];
938
939     ADCVal = ADC1BUF20;
940     ADCFloat = ((double) ADCVal) * (double) (3.3 / 4096);
941     sprintf(buf, "%f", ADCFloat);
942     WriteScreen("\n\r");
943     WriteScreen(buf);
944 }
945
946 void WriteVcntrla(void) {
947     int ADCVal;
948     double ADCFloat;
949     char buf[10];
950
951     ADCVal = ADC1BUF5;
952     ADCFloat = ((double) ADCVal) * (double) (3.3 / 4096);
953     sprintf(buf, "%f", ADCFloat);
954     WriteScreen("\n\r");
955     WriteScreen(buf);
956 }
957
958
959 void BuckBoostMode(void) {
960     CCP1CON2Hbits.OCFEN = 1; //ManualON A
961     CCP1CON2Hbits.OCCEN = 1; //ManualON B
962
963     SetPWMon(8);
964 }
965
966
967 void DisableManual(void) {
```

```
 968     //ManualOnB = OC1C = Pin 8 = RB10
 969     //EnableB = A7 = Pin 6
 970     //EnableA = C8 = Pin 4
 971     int i;
 972
 973     //TriggerPulse();
 974     LATBbits.LATB6 = 1;         //Set ManualONA to 1 (won't take effect
until next commands)
 975     LATBbits.LATB10 = 1;        // Set ManualONB to 1 (won't take effect
until next command)
 976
 977     CCP1CON2Hbits.OCCEN = 0;    //ManualON B regular digital IO
 978     CCP1CON2Hbits.OCFEN = 0;    //ManualON A regular digital IO
 979
 980     //for(i=0;i<2;i++){}
 981
 982     //TriggerPulse();
 983     LATBbits.LATB6 = 0;         //Set ManualONA to 0;
 984     LATBbits.LATB10 = 0;        //Set ManualONB to 0; wait for a few
cycles
 985     for (i = 0; i < 2; i++) {
 986     }
 987
 988
 989
 990     LATBbits.LATB10 = 1;        //Set ManualONB to 1, disable manual mode
as fast as possible
 991     LATBbits.LATB6 = 1;         //Set ManualONA to 1, disable manual mode
as fast as possible
 992     //for(i=0;i<1;i++){}
 993     //TriggerPulse();
 994
 995     //Turn EnableB Off
 996     LATAbits.LATA7 = 0;
 997     LATBbits.LATB10 = 0;
 998
 999     //Turn EnableA off
1000     LATCbits.LATC8 = 0;
1001     LATBbits.LATB6 = 0;  //Uncomment for mod boost mode; comment for
regular boost mode
1002
```

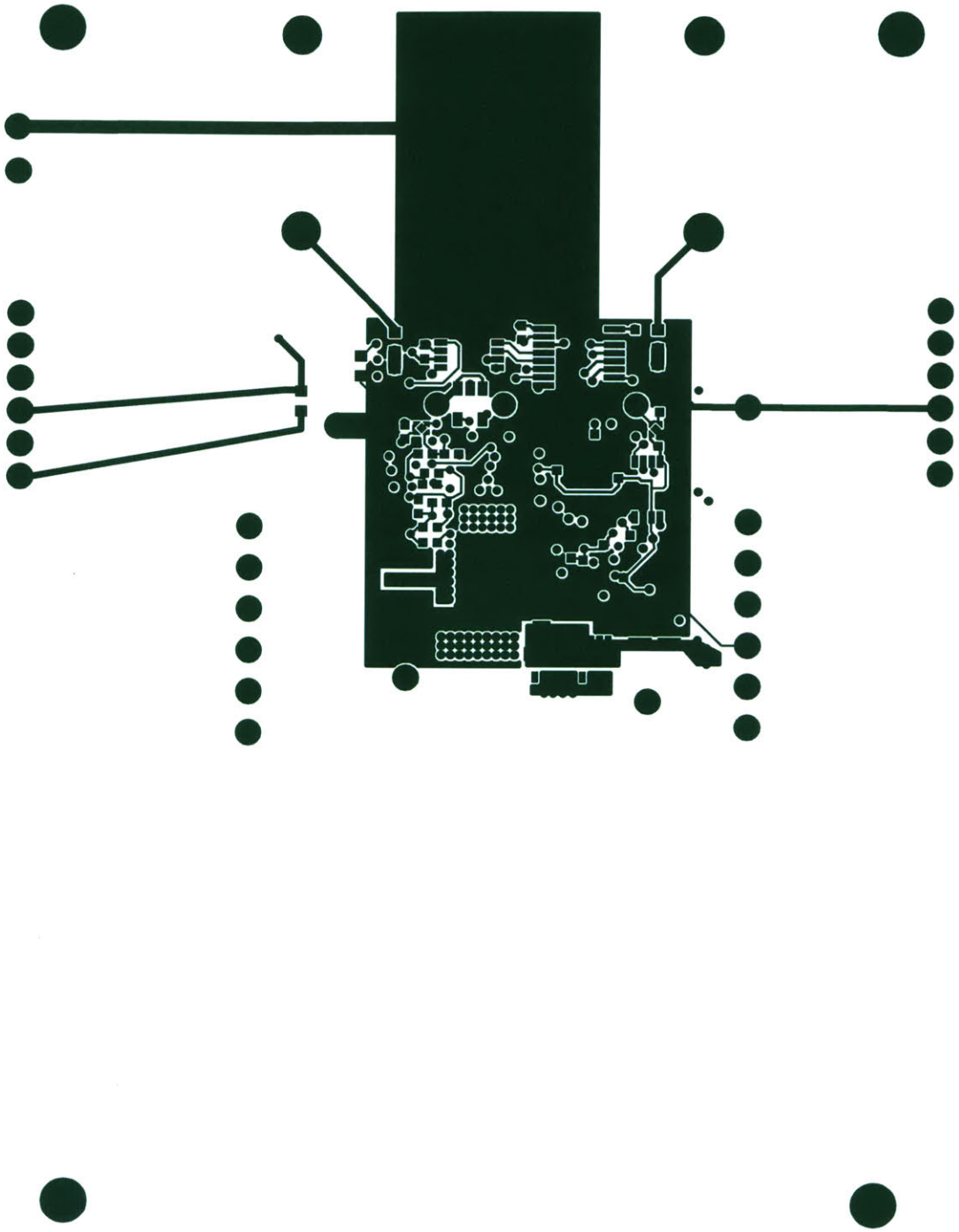
```
1003      //TriggerPulse();
1004      //Turn EnableA Off
1005
1006
1007
1008
1009 }
```

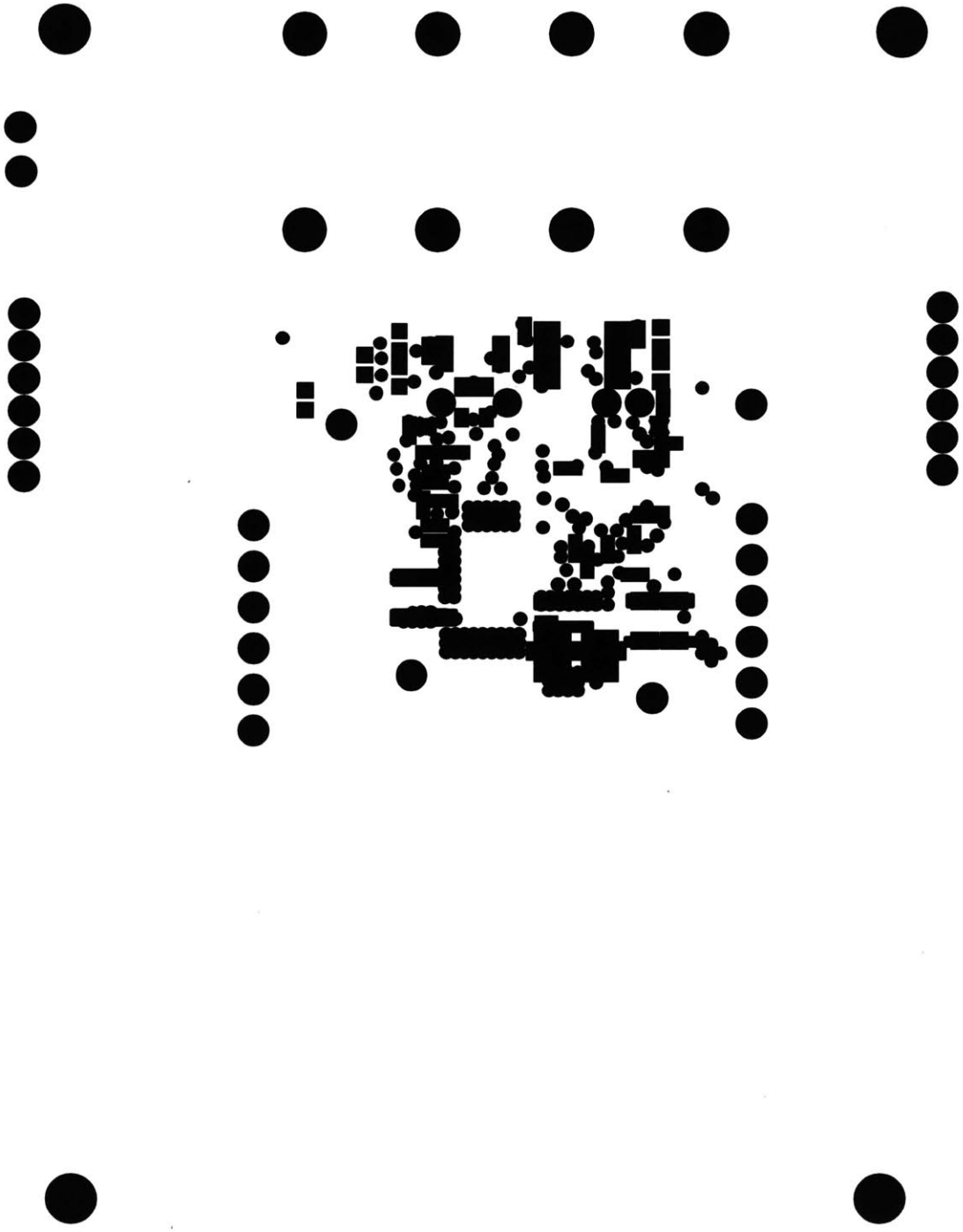
# Appendix H

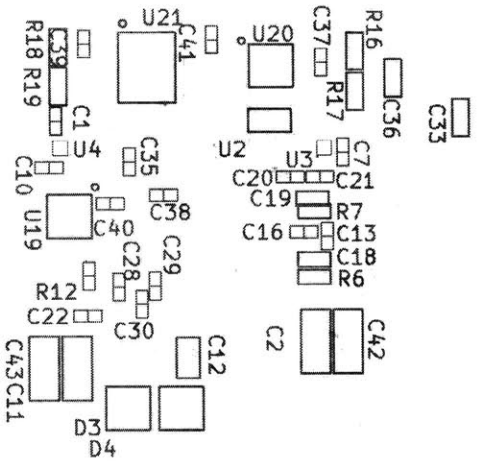
# PCB Layout Reference

The following pages contain a reference for the PCB layout for the second version prototype converter (shown at scale 2x). The files are listed in the following order:

1. Bottom Copper
2. Bottom Soldermask
3. Bottom Silkscreen
4. Top Copper
5. Top Soldermask
6. Top Silkscreen
7. L2 (Inner 1) Copper
8. L3 (Inner 2) Copper
9. Drill





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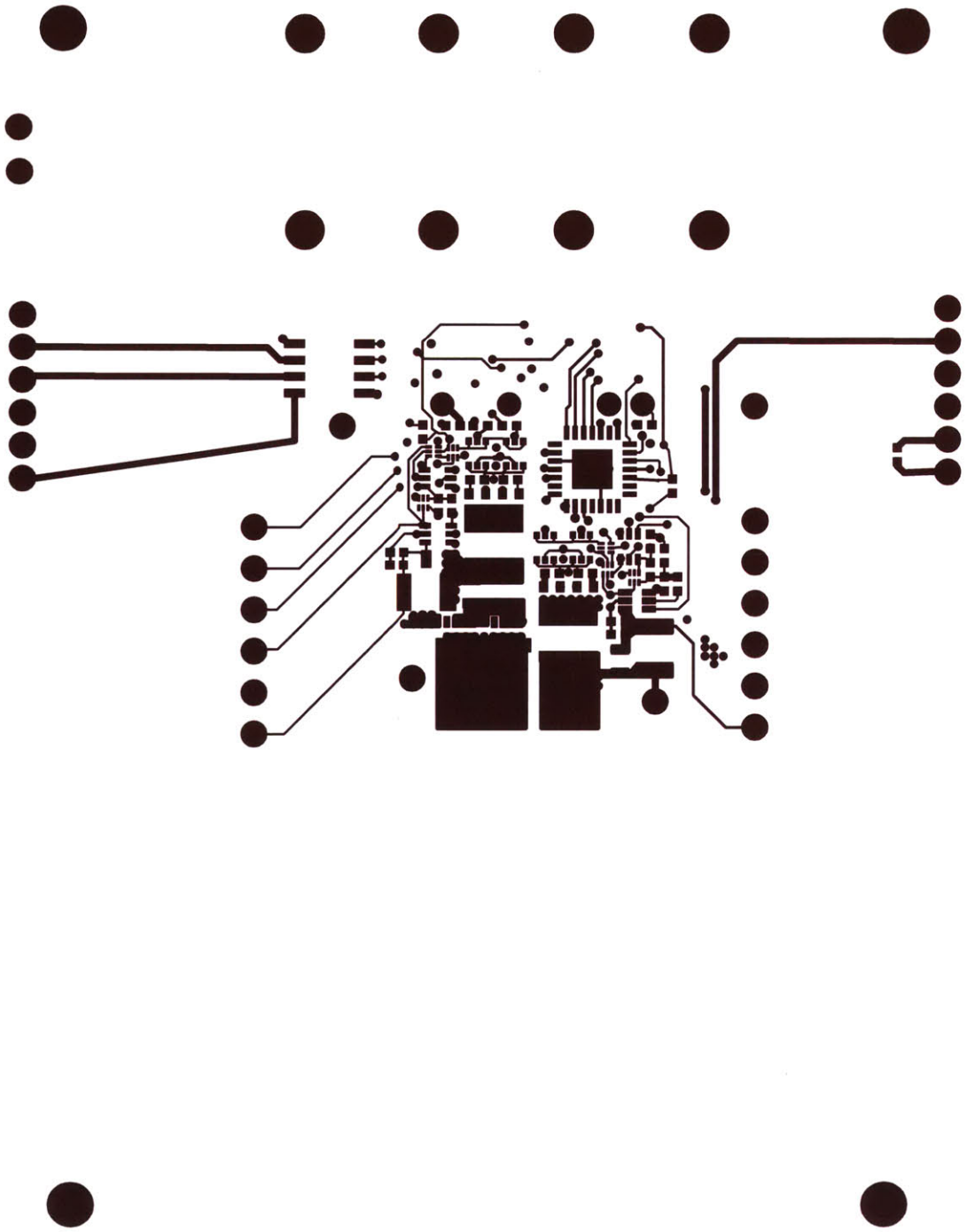
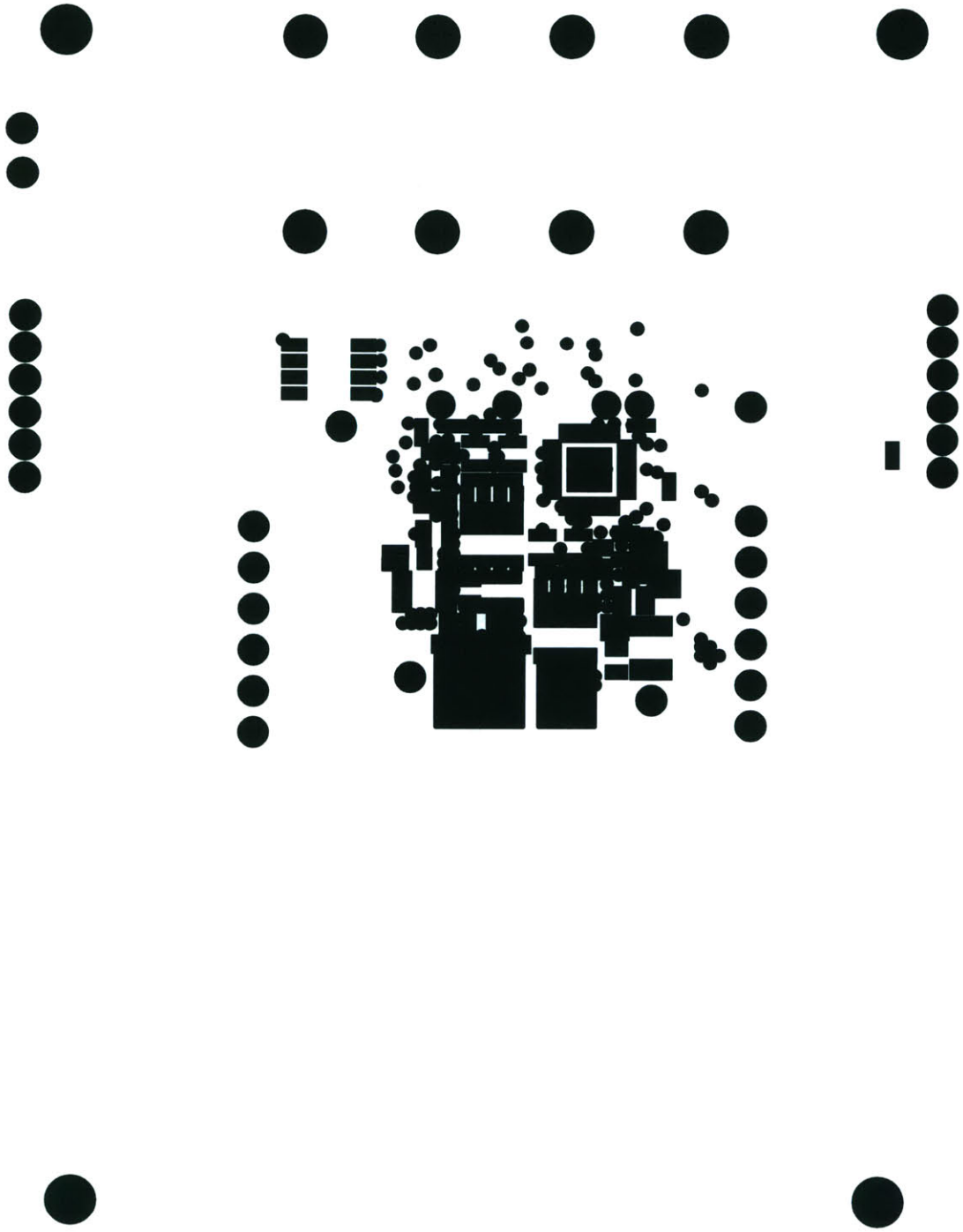
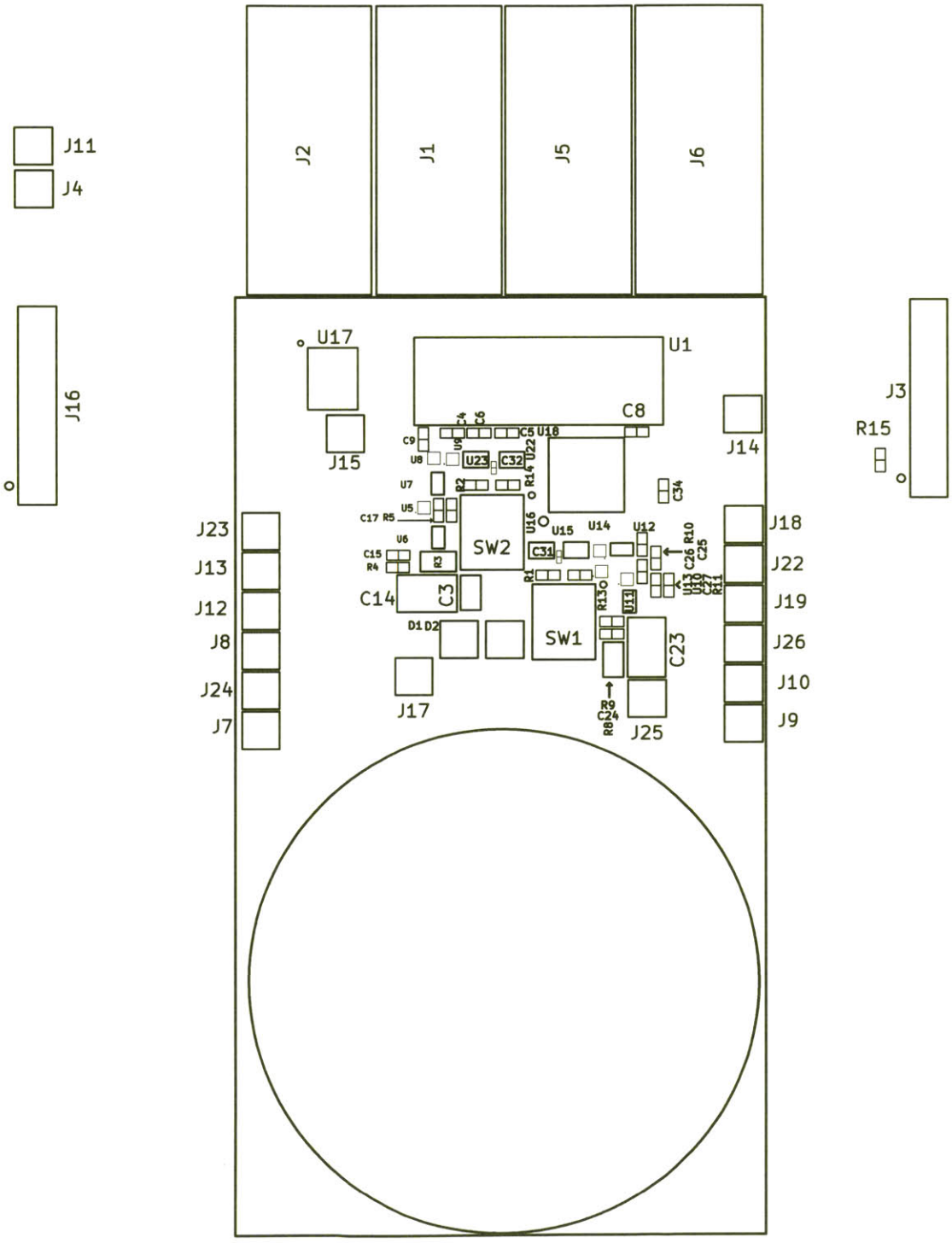
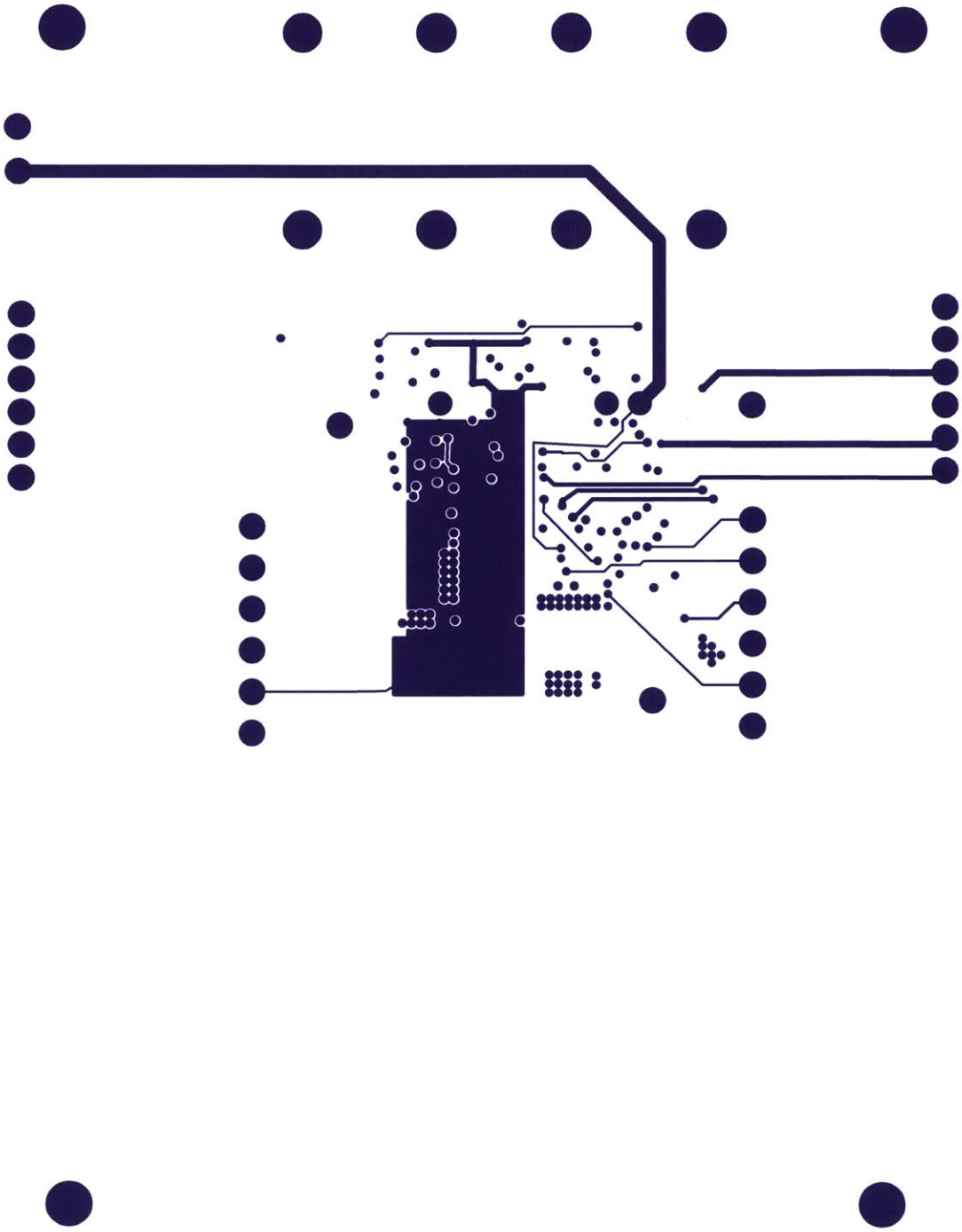
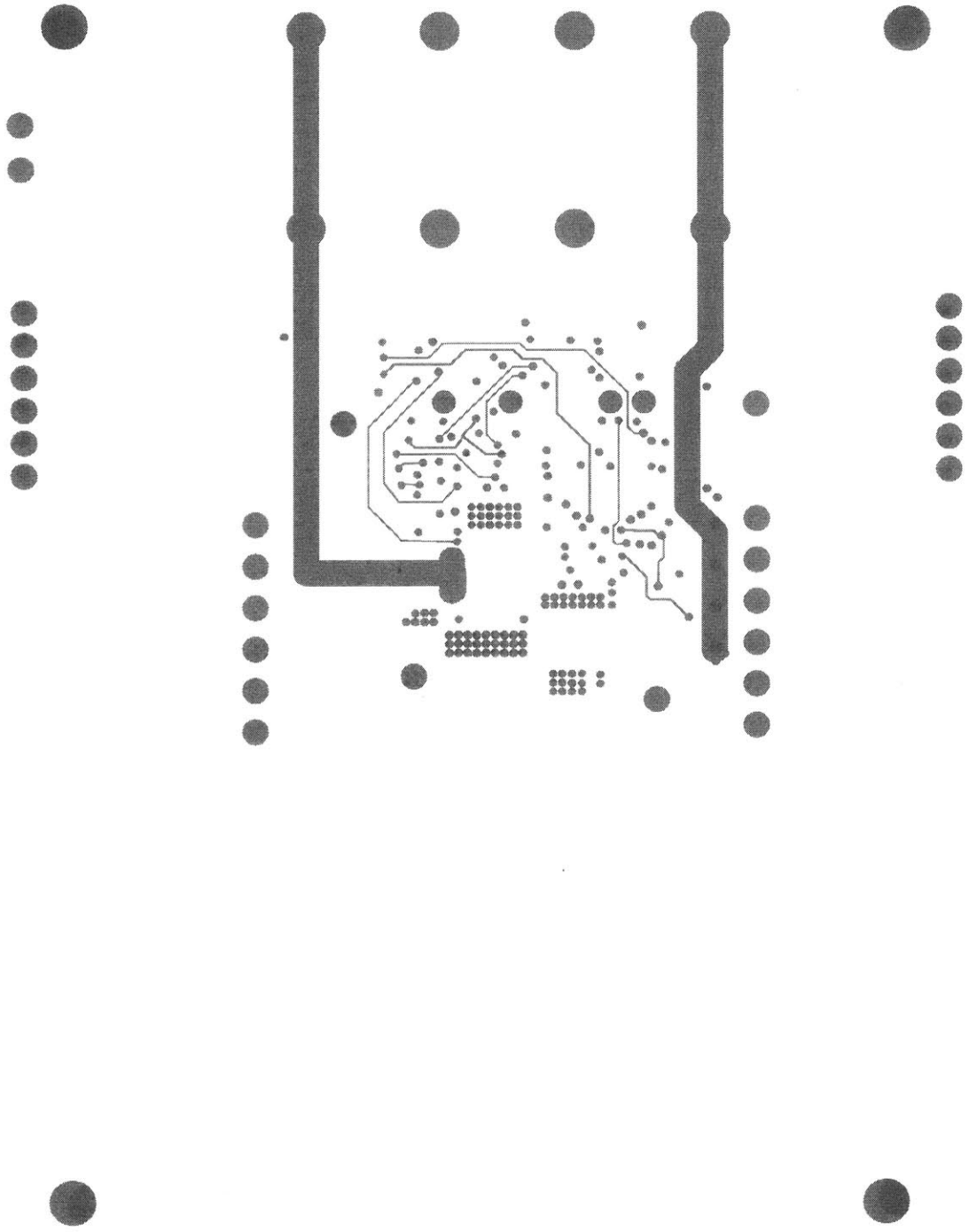
**Apr 2016**

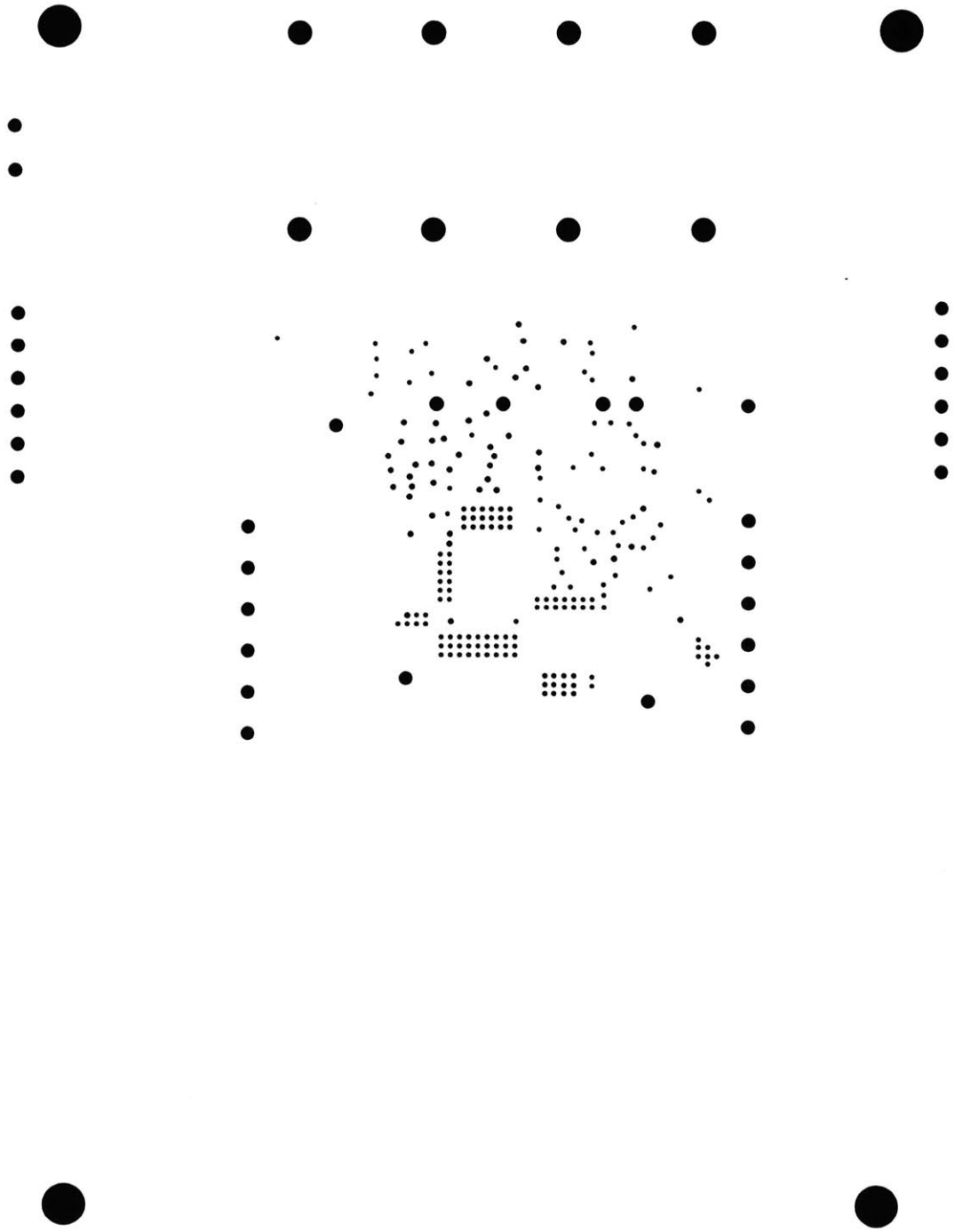





J11
J4
J16
J2
J1
J5
J6
U17
U1
C8
J15
J14
J3
R15
J23
J13
J12
J8
J24
J7
J18
J22
J19
J26
J10
J9
SW2
SW1
C14
C3
C23
J17
J25
C4
C6
C5
U18
C9
U9
U22
U8
U23
C32
R14
U7
R2
C34
U5
C17
R5
U16
U15
U14
U12
R10
C25
U6
C15
R4
R3
C31
R1
R13
U11
C26
U13
U10
C24
R11
D1
D2
R9
R8
C24







# Appendix I

# LTSpice Simulation Files

The following pages contain the plain text `.asc` files which may reproduce the simulation workbench in LTSpice. The comments at the top of each, designated by a *, may need to be omitted. The files appear in the following order:

1. Top Level - uses the other items as subcircuit models of the power devices and control logic.
2. Control Logic
3. FET Model - applies to both NV6131 and NV6105 low $R_{on}$ GaN switches.
4. Diode Model - applies to the Cree C3D1P7060Q.

```
*Top level file for simulation

Version 4
SHEET 1 2080 1076
WIRE -176 -992 -208 -992
WIRE -128 -992 -176 -992
WIRE 240 -992 0 -992
WIRE 256 -992 240 -992
WIRE 336 -992 256 -992
WIRE 528 -992 416 -992
WIRE 592 -992 528 -992
WIRE 800 -992 592 -992
WIRE 944 -992 928 -992
WIRE 1056 -992 944 -992
WIRE 1104 -992 1056 -992
WIRE -208 -928 -208 -992
WIRE 944 -928 944 -992
WIRE 1104 -928 1104 -992
WIRE 240 -912 240 -992
WIRE 592 -912 592 -992
WIRE -64 -896 -64 -928
WIRE -16 -896 -64 -896
WIRE 0 -896 -16 -896
WIRE 480 -848 448 -848
WIRE 528 -848 480 -848
WIRE -208 -736 -208 -848
WIRE 240 -736 240 -784
WIRE 240 -736 -208 -736
WIRE 592 -736 592 -784
WIRE 592 -736 240 -736
WIRE 944 -736 944 -864
WIRE 944 -736 592 -736
WIRE 1104 -736 1104 -864
WIRE 1104 -736 944 -736
WIRE -208 -688 -208 -736
WIRE -96 -576 -128 -576
WIRE 16 -576 -16 -576
WIRE 48 -576 16 -576
WIRE -96 -416 -128 -416
WIRE 32 -416 -16 -416
WIRE 48 -416 32 -416
WIRE 544 -352 464 -352
WIRE 656 -352 624 -352
WIRE 656 -288 656 -352
WIRE 1056 -256 976 -256
WIRE 1088 -256 1056 -256
WIRE 464 -224 448 -224
```

```
WIRE 592 -224 464 -224
WIRE 816 -224 720 -224
WIRE 832 -224 816 -224
WIRE 976 -208 976 -256
WIRE 320 -192 256 -192
WIRE 464 -192 400 -192
WIRE 592 -192 464 -192
WIRE 464 -144 416 -144
WIRE 592 -144 464 -144
WIRE 416 -112 416 -144
WIRE 656 -80 656 -128
WIRE 976 -80 976 -128
WIRE 416 0 416 -32
FLAG -208 -688 0
FLAG -176 -992 vi
FLAG 16 -576 vgs_a
FLAG 528 -992 vb
FLAG 1056 -992 vout
FLAG 256 -992 va
FLAG -128 -416 0
FLAG -16 -896 vgs_a
FLAG 480 -848 vgs_b
FLAG -128 -576 va
FLAG 656 -80 0
FLAG 464 -352 0
FLAG 976 -80 0
FLAG 464 -224 vb
FLAG 256 -192 0
FLAG 416 0 0
FLAG 816 -224 pregateb
FLAG 1056 -256 gateb
FLAG 32 -416 vgs_b
FLAG 464 -192 Vcntrl
FLAG 464 -144 VZVS
SYMBOL voltage -208 -944 R0
WINDOW 123 0 0 Left 2
WINDOW 39 0 0 Left 2
SYMATTR InstName V1
SYMATTR Value 90
SYMBOL ind 320 -976 R270
WINDOW 0 32 56 VTop 2
WINDOW 3 5 56 VBottom 2
SYMATTR InstName La
SYMATTR Value {L}
SYMATTR SpiceLine Rser={RL}
SYMBOL cap 928 -928 R0
SYMATTR InstName C3
```

```
SYMATTR Value 100オ
SYMATTR SpiceLine Rser=0 Rpar=0
SYMBOL voltage 0 -576 R90
WINDOW 123 0 0 Left 2
WINDOW 39 0 0 Left 2
WINDOW 0 -55 71 VLeft 2
WINDOW 3 64 224 VLeft 2
SYMATTR InstName V4
SYMATTR Value 6
SYMBOL zener 1120 -864 R180
WINDOW 0 24 64 Left 2
WINDOW 3 24 0 Left 2
SYMATTR InstName D3
SYMATTR Value ZN380
SYMBOL voltage 0 -416 R90
WINDOW 123 0 0 Left 2
WINDOW 39 0 0 Left 2
WINDOW 0 -55 71 VLeft 2
WINDOW 3 64 224 VLeft 2
SYMATTR InstName V2
SYMATTR Value PULSE(0 6 500p 100p 100p {Tb} {1/fs} {fs})
SYMBOL NVswitch -64 -992 R270
SYMATTR InstName X1
SYMBOL NVswitch 592 -848 R0
SYMATTR InstName X2
SYMBOL creediode 240 -848 R270
SYMATTR InstName X3
SYMBOL creediode 864 -992 R0
SYMATTR InstName X4
SYMBOL voltage 640 -352 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
WINDOW 123 0 0 Left 2
WINDOW 39 -4 56 VBottom 2
SYMATTR InstName V3
SYMATTR Value 3.3
SYMATTR SpiceLine Rser=.1m
SYMBOL MyUB-Logic 656 -208 R0
SYMATTR InstName X5
SYMBOL voltage 416 -192 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
WINDOW 123 0 0 Left 2
WINDOW 39 -4 56 VBottom 2
SYMATTR InstName V6
SYMATTR Value .66
SYMATTR SpiceLine Rser=.1m
```

```
SYMBOL voltage 416 -128 R0
WINDOW 123 0 0 Left 2
WINDOW 39 24 44 Left 2
SYMATTR SpiceLine Rser=.1m
SYMATTR InstName V7
SYMATTR Value .35
SYMBOL bv 976 -224 R0
SYMATTR InstName B1
SYMATTR Value V=delay( V(pregateb)*6/3.3, 5n )
TEXT 632 -632 Left 2 !.param Ta= 90n
TEXT 632 -672 Left 2 !.param fs=3.5e6
TEXT 304 -672 Left 2 !.model ZN380 D(BV=380)
TEXT 304 -640 Left 2 !.ic V(vout)=380.5
TEXT 632 -592 Left 2 !.param Tb=200n
TEXT 864 -688 Left 2 !.tran 0 {end} {start} {mintime} uic
TEXT 864 -656 Left 2 !.param start =  1000/fs
TEXT 864 -624 Left 2 !.param end = start+100/fs
TEXT 864 -584 Left 2 !.param mintime = 1/(fs*500)
TEXT 632 -552 Left 2 !.param L = 15u
TEXT 632 -512 Left 2 !.param RL = L*2*3.1416*fs/100
TEXT 1088 -200 Left 2 ;Represents driver with 5n delay
```

```
*Sheet for control logic; must be included for top level to read

Version 4
SHEET 1 1236 1172
WIRE -800 -496 -800 -528
WIRE -800 -496 -848 -496
WIRE -736 -496 -800 -496
WIRE -848 -464 -848 -496
WIRE -736 -464 -736 -496
WIRE -304 -416 -304 -496
WIRE -416 -400 -448 -400
WIRE -336 -400 -416 -400
WIRE -112 -384 -272 -384
WIRE 32 -384 -112 -384
WIRE -736 -368 -736 -384
WIRE -576 -368 -736 -368
WIRE -336 -368 -576 -368
WIRE -848 -352 -848 -400
WIRE -736 -352 -736 -368
WIRE -736 -352 -848 -352
WIRE -736 -320 -736 -352
WIRE -304 -320 -304 -352
WIRE -848 -304 -848 -352
WIRE -848 -224 -848 -240
WIRE -800 -224 -848 -224
WIRE -736 -224 -736 -240
WIRE -736 -224 -800 -224
WIRE -800 -176 -800 -224
WIRE -784 128 -864 128
WIRE -768 128 -784 128
WIRE -528 128 -704 128
WIRE 32 128 32 -384
WIRE 384 128 32 128
WIRE -528 144 -528 128
WIRE 384 144 352 144
WIRE 352 160 352 144
WIRE 352 160 304 160
WIRE 384 160 352 160
WIRE 352 176 352 160
WIRE 384 176 352 176
WIRE 544 176 448 176
WIRE 560 176 544 176
WIRE 384 192 32 192
WIRE 400 208 400 192
WIRE -592 384 -592 368
WIRE -592 384 -688 384
WIRE -592 400 -592 384
WIRE -448 400 -448 368
WIRE -688 416 -688 384
WIRE -208 496 -208 448
WIRE -304 512 -320 512
WIRE -240 512 -304 512
WIRE -96 528 -176 528
WIRE 32 528 32 192
```

```
WIRE 32 528 -96 528
WIRE -688 544 -688 480
WIRE -688 544 -736 544
WIRE -592 544 -592 480
WIRE -592 544 -688 544
WIRE -512 544 -592 544
WIRE -448 544 -448 480
WIRE -448 544 -512 544
WIRE -304 544 -448 544
WIRE -240 544 -304 544
WIRE -736 608 -736 544
WIRE -512 608 -512 544
WIRE -784 624 -896 624
WIRE -208 640 -208 560
WIRE -784 704 -784 672
WIRE -736 704 -736 688
WIRE -736 704 -784 704
WIRE -512 768 -512 672
WIRE -736 800 -736 704
WIRE -736 816 -736 800
FLAG -304 512 Vcntrl
FLAG -208 448 Vdd
FLAG -304 -496 Vdd
FLAG -800 -528 Vds
FLAG -800 -176 Vss
FLAG -304 -320 Vss
FLAG -208 640 Vss
FLAG -512 768 Vss
FLAG -736 800 Vss
FLAG 400 208 Vss
FLAG -864 128 Vss
FLAG 304 160 Vss
FLAG -304 544 Vramp
FLAG -112 -384 ZVS
FLAG -896 624 ZVS
FLAG 544 176 Q
FLAG -96 528 Timer
FLAG -576 -368 Vds_div
FLAG -416 -400 VZVS
SYMBOL Comparators\\LTC6752 -304 -448 R0
SYMATTR InstName U1
SYMBOL Comparators\\LTC6752 -208 464 R0
SYMATTR InstName U2
SYMBOL PowerProducts\\LT3092 -528 256 R0
SYMATTR InstName U3
SYMBOL res -464 384 R0
SYMATTR InstName R1
SYMATTR Value 100
SYMBOL res -608 384 R0
SYMATTR InstName R2
SYMATTR Value 10k
SYMBOL cap -528 608 R0
SYMATTR InstName C1
SYMATTR Value 300p
```

```
SYMATTR SpiceLine Rser=1m
SYMBOL res -752 -480 R0
SYMATTR InstName R3
SYMATTR Value 100k
SYMBOL res -752 -336 R0
SYMATTR InstName R4
SYMATTR Value 850
SYMBOL cap -864 -464 R0
SYMATTR InstName C2
SYMATTR Value 8.5p
SYMBOL cap -864 -304 R0
SYMATTR InstName C3
SYMATTR Value 1n
SYMBOL voltage -688 128 R90
WINDOW 123 0 0 Left 2
WINDOW 39 102 55 VRight 2
WINDOW 0 44 86 VRight 2
WINDOW 3 70 90 VRight 2
SYMATTR SpiceLine Rser=1m
SYMATTR InstName V2
SYMATTR Value 6
SYMBOL Digital\\or 416 96 R0
WINDOW 3 -8 36 Invisible 2
SYMATTR Value Vhigh = 3.3 Vlow=0 Trise=1n Tfall=1n Td=2.1n
SYMATTR InstName A1
SYMBOL cap -704 416 R0
SYMATTR InstName C4
SYMATTR Value 20p
SYMATTR SpiceLine Rser=1m
SYMBOL sw -736 704 M180
SYMATTR InstName S1
SYMATTR Value tran
TEXT -624 -632 Left 2 ;ZVS Detector
TEXT -1288 -392 Left 2 ;10k and 85 => Div by 120
TEXT 72 832 Left 2 !.model tran SW(Ron=10m, Roff = 10meg, Vt=1.6)
TEXT 8 -552 Left 2 ;Also consider LT1720 (dual package; lines up well
with NOR)\nLT1720 comes in S8, MS8, DFN packages\nLTC6752 variants come
in S5, SC6, MS8 packages
TEXT 328 24 Left 2 ;74LVC1G02\n - SOT353, SOT553, various DFN
TEXT -1304 280 Left 2 ;LT3092 \n - ST, TS8, DFN packages\nAlso consider
LM334 S\n - TO-92, SO8 packages
TEXT -1328 72 Left 2 ;Ought to be the same as \nVdd if possible; will
depend \non dropout of current source
TEXT -600 -8 Left 2 ;Ramp
RECTANGLE Normal -48 -112 -984 -600 2
RECTANGLE Normal 752 944 -1408 -688 2
RECTANGLE Normal -48 848 -984 24 2
```

```
* Sheet to serve as model for Cree diode; necessary for top level to read

Version 4
SHEET 1 1820 680
WIRE 80 16 -64 16
WIRE 256 16 144 16
WIRE -64 64 -64 16
WIRE -64 64 -144 64
WIRE 256 64 256 16
WIRE 336 64 256 64
WIRE -64 128 -64 64
WIRE 48 128 -64 128
WIRE 256 128 256 64
WIRE 256 128 112 128
FLAG -144 64 in
FLAG 336 64 out
SYMBOL diode 48 144 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 0 32 VBottom 2
SYMATTR InstName D1
SYMATTR Value C3D1P7060Q
SYMBOL cap 144 0 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 -64 30 VTop 2
SYMATTR InstName C1
SYMATTR Value Q=1e-
12*if(x>200,6*x+1530,if(x>30,10*x+730,if(x>4,30*x+129,if(x>0.4,60*x+9.2,8
3*x))))
TEXT -176 208 Left 2 !.model C3D1P7060Q D(Vfwd=1.2,Ron=0.1613)
TEXT -408 272 Left 2 ;C1 out in Q=1e-
12*if(x>200,6*x+1530,if(x>30,10*x+730,if(x>4,30*x+129,if(x>0.4,60*x+9.2,i
f(x>0,83*x,0)))))
TEXT -360 -128 Left 2 ;CREE C3D1P7060, SiC Schottky\nDiode uses piecewise
linear model; Nonlinear capacitor Q(V) also modeled as piecewise linear
```

```
*Sheet to model Navitas 6131 or 6105 devices; necessary for top level to
read

Version 4
SHEET 1 1912 680
WIRE 288 -48 288 -112
WIRE 288 -48 64 -48
WIRE 64 -16 64 -48
WIRE 288 0 288 -48
WIRE 288 0 208 0
WIRE 448 0 288 0
WIRE 560 0 448 0
WIRE 208 80 208 0
WIRE 448 80 448 0
WIRE 560 80 560 0
WIRE 16 96 -32 96
WIRE 64 96 64 48
WIRE 64 96 16 96
WIRE 160 96 64 96
WIRE 16 144 16 96
WIRE 208 224 208 160
WIRE 288 224 208 224
WIRE 448 224 448 144
WIRE 448 224 288 224
WIRE 560 224 560 144
WIRE 560 224 448 224
WIRE 16 272 16 208
WIRE 160 272 160 144
WIRE 160 272 16 272
WIRE 288 272 288 224
WIRE 288 272 160 272
WIRE 288 304 288 272
FLAG 288 -112 nodeD
FLAG 288 304 nodeS
FLAG -32 96 nodeG
SYMBOL sw 208 176 M180
SYMATTR InstName S1
SYMATTR Value NV1130
SYMBOL diode 464 144 R180
WINDOW 0 24 64 Left 2
WINDOW 3 24 0 Left 2
SYMATTR InstName D1
SYMATTR Value NV1130Body
SYMBOL cap 48 -16 R0
SYMATTR InstName Cgd
SYMATTR Value 1p
SYMBOL cap 0 144 R0
SYMATTR InstName Cgs
SYMATTR Value 75p
SYMBOL cap 544 80 R0
SYMATTR InstName C1
SYMATTR Value Q=1e-12*if(x>200,0.5*x+612,if(x>40,0.7*x+572,15*x))
TEXT 64 424 Left 2 !.model NV1130 SW(Ron=0.32, Roff=1Meg, Vt=3, Vh=-3)
TEXT 64 456 Left 2 !.model NV1130Body D(Vfwd = 2.25, Ron = 0.35)
```

```
TEXT -72 520 Left 2 ;Body diode modeled on EPC 2027 (450 V) since NV1130
datasheet does not include its characteristic
TEXT -72 560 Left 2 ;Cds nodeD nodeS Q=1e-
12*if(x>200,0.5*x+612,if(x>40,0.7*x+572,if(x>-2,15*x,1e-12)))
TEXT -72 600 Left 2 ;Using Ron = 0.32 to account for high junction
temperature (not 0.16 at 25 C)
```

# Bibliography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