DLTS Characterization of Aluminum Gettering of Iron Contaminants in Boron-Doped Silicon

by

Jeanne A. Thienprasit

Submitted to the Department of Physics and the Department of Materials Science and Engineering in Partial Fulfillment of the Requirements for the Degrees of

Bachelor of Science in Physics

and

Bachelor of Science in Materials Science and Engineering

at the Massachusetts Institute of Technology

May 1996

© 1996 Massachusetts Institute of Technology All rights reserved

Signature of the Author	
	May 10, 1996
Certified by Lionel C. Kim	nerling, Professor of Materials Science and Engineering
	Thesis Advisor
Accepted By	Professor David K. Roylance
	Chairman, Undergraduate Thesis Committee for the
	Department of Materials Science and Engineering
Accepted By	
	Professor June Matthews
	Chairman, Undergraduate Thesis Committee for the Department of Physics
MASSACHUSETIS INSTITUTE OF TECHNOLOGY	·

JUN 21 1996 ARCHIVES

LIBRARIES

Abstract

Deep Level Transient Spectroscopy (DLTS) is a highly accurate method of directly measuring transient phenomena such as deep level trap activity. By using DLTS the effect of using aluminum to getter iron contaminants from silicon is studied. The activity at the iron-boron pair trap level at $E_v + 0.10$ is used to monitor the success of gettering with different heat treatments. Preliminary studies with Electron Beam Induced Current, (EBIC) and DLTS show that iron concentrations drop from the doped level of 1×10^{14} cm⁻³ to a post-gettering level of 2×10^{12} cm⁻³ with gettering heat treatment of 800°C for 120 minutes. This 98% gettering efficiency bodes well for the development of aluminum gettering for use in manufacturing.

Table of Contents

1. Introduction

- 1.1 Transition Metal Contamination
- 1.2 Possible Solutions
- 1.3 Project Objective

2. Background

- 2.1 Iron Boron Pairs
- 2.2 Relationships Between Trap Parameters
- 2.3 Gettering
- 2.3.1 Possible Intrinsic Gettering by Oxide Clusters
- 2.3.2 Extrinsic Iron Gettering by Aluminum in Boron-Doped Silicon
- 2.4 Deep Level Transient Spectroscopy
- 2.4.1 DLTS Theory
- 2.4.2 DLTS Analysis
- 2.4.2.1 Capture Cross Section
- 2.4.2.2 Thermal Emission Rate
- 2.4.2.3 Trap Depth
- 2.4.3 Leakage Current
- 3. Experiment
- 3.1 Sample Preparation
- 3.2 DLTS Parameters
- 4. Conclusions
- 5. Future Work

1. Introduction

One of the most pressing problems facing the development of higher performance electronic materials is contamination of silicon substrates especially by transition metals. These metal impurities are very mobile and will diffuse long distances during heat treatments common in silicon processing. This becomes a problem when the unwanted contaminants encounter extended defect sites leading to larger leakage currents and lower breakdown voltages.

1.1 Transition Metal Contamination

Heavy metal impurities can be introduced to silicon during processing, often through the use of stainless steel fixtures, furnace contamination, and metal handling tools. Common metal impurities found in silicon are copper, nickel, gold and iron. Heat treatments of silicon wafers accelerate the contamination. In this study, iron contamination is profiled. Iron is particularly insidious because of the high amount of steel that is used in equipment and tools. Even at room temperature, a significant amount iron will diffuse into silicon.

In boron-doped (p-type) silicon contaminated with iron, the concern is that iron will be drawn due to electrostatic attraction toward the boron dopant sites and form iron-boron pairs. These pairs form deep-levels within the band gap of silicon at which recombination can occur. This leads to shorter lifetimes and poor device quality.

1.2 Possible Solutions

Two approaches to avoiding degradation of device characteristics are removing sources of the contamination, or neutralizing the effect of the iron within the device. Unfortunately, eliminating exposure of the silicon to potential sources of metal contamination is almost impossible due use of metals in much of the equipment and tools used in processing. By limiting the use of metal in equipment and tools in the processing, especially during heat treatment, transition metal contamination can be decreased. Also reducing heat treatment temperatures whenever possible also decreases contamination.

The second approach is to neutralize the transition metal contaminants. One process of accomplishing this is called gettering. Gettering removes contaminants from active device areas by trapping them at defects or in solution in inactive areas. It is this approach that is outlined in this study.

In the gettering process studied, the contaminated silicon wafer is coated with aluminum and then heat treated to produce Al acceptors at the surface. At high temperatures, Fe-B pairs are broken then Fe migrates toward the higher solubility Aluminum layer. The heat treatment allows the aluminum to interact with the iron because the electrostatic attraction between the boron and the iron becomes less dominant at the higher temperatures. For successful gettering, the iron contaminants should then remain trapped at the Al silicon boundary throughout the rest of the processing steps.

1.3 Project Objective

The goal of this study is the characterization of the iron contaminated boron doped silicon wafers as a function of different heat treatments to eventually develop effective gettering processes to remove Fe contaminants from active device regions. Ultimately,

characterization of this process could be used in the development of a iron gettering process for use in a manufacturing environment.

2. Background

2.1 Iron-Boron Pairs

In boron-doped p-type silicon, the boron is a substitution defect in the silicon diamond cubic lattice. The iron ions in the silicon occupy the tetrahedral interstitial sites. Due to the Coulombic interaction potential between the iron ions and the boron acceptors, iron-boron pairs can be formed described by the following reaction:

$$Fe_i^+ + B_s^- = (Fe_iB_s)^o$$
 (1)

When forming the bond, the outer shell of the electrons on the iron ions are transferred from the 4s state to the 3d state, while the boron atom 3d electrons are promoted to the sp³ allowing tetrahedral bonding between the two. Iron will occupy the nearest tetrahedral sites to the substitution boron sites.

At room temperature, much of the iron contained in the silicon will form Fe-B pairs when equilibrium is reached because the Coulomb force is dominant at this temperature. Iron-acceptor pairs will only form in a p-type wafer because positively charged iron ions are attracted by the negatively charged dopant acceptors. The Coulomb force is characterized by the following¹:

$$F_{\text{Coulomb}} = \frac{\varepsilon kT}{4\pi D(Fe_i)[B_s]} = \frac{557T}{D(Fe_i)[B_s]}$$
 (2)

-

¹ Reference: [1]

away from nearest interstitial sites neighbors to the boron. The fraction of iron ions to iron-boron pairs is given by the following²:

$$f = \frac{[B_s]}{ZN} \exp(\frac{E_b}{kT}) = 5 \times 10^{-24} [B_s] \exp(\frac{E_b}{kT})$$
 (3)

Formation of iron-boron pairs creates two deep levels within the silicon band gap. Due to the presence of Fe, levels formerly in the valence band are shifted into the gap by the Coulomb forces. The levels are shifted because the potential energy of the system is lowered by the pairing of the iron ions with the boron dopants. The new levels occur at $E_v + 0.10$ and $E_c - 0.29$ in the silicon band gap. The first, $E_v + 0.10$, corresponds to a level that is corresponds to the shifted $Fe^{+/++}$ deep donor state which becomes the new ($Fe^{+/++}B_s$)^{-0/+}. The second, $E_c - 0.29$ is the shifted $Fe^{-0/+}$ acceptor state now identified as ($Fe_i^{-0/+}B_s^{-}$)⁻⁰. Also a third deep level is present when isolated iron is present. This $Fe^{-0/+}$ state is located at $E_v + 0.38$. The charge of each state is determined by the relative concentrations of iron to boron. In the samples studied, the iron concentration is approximately 10^{14} cm⁻³ while the boron concentration is approximately 10^{15} cm⁻³. This ratio shifts the Fermi level in between the isolated iron state and the deep donor state. (See Figure 1)

In this project the boron concentration is an order of magnitude greater therefore all the iron should have formed iron-boron pairs. The effect of the gettering can then be monitored by following the change in the concentration of the number of iron-boron (donor state) traps and their defining characteristics such as capture cross section, and emission rates.

2.2 Relationships Between Trap Parameters

6

² Reference: [1]

a) HC Ec - 0.29 eV ——— $Fe_i^{0/+}B_s^-$

Ev + 0.38 eV ----- Fe $_i^{0/+}$

Ev + 0.10 eV ——— $Fe_i^{+/++}B_s^-$

Ev F

Figure 1a: Iron induced deep levels in boron doped silicon. Levels are maked with their positions relative to the band gap and with their possible charge states.

b) Ec.

Fe. +

Εť

----- Fe_i⁺B_s

Ev

Figure 1b: For [B] > [Fe] the deep levels and charge states induced by iron boron pairing.

The capture cross-section of a trap is cross-sectional area around a trap site within which a carrier will be trapped. The emission rate is the average rate at which trapped carriers escape or at which new carriers are generated. These trap parameters are related by the definition³:

$$\tau_{trap} = \frac{1}{\sigma < v_c > [trap]} \tag{4}$$

where τ_{trap} is the minority carrier lifetime contribution of each trap state, σ is the capture cross-section of the trap and <ve> is the average velocity of the minority carrier.

The trap lifetime is related to the emission rate by the following⁴:

$$e_n = \frac{1}{\tau} \tag{5}$$

2.3 Gettering

Gettering is the process of drawing unwanted contaminants away from active device regions and trapping them so they are not re-released during the remainder of the processing steps. Three steps in effective gettering are: 1) Dissolution of the impurity into solid solution rather than in the form of a stable precipitate at the gettering temperature 2) Diffusion of the impurity to an inactive region 3) Trapping of the impurity outside the active device region throughout the remaining processing steps.⁵

Gettering processes can be divided in to two classes: intrinsic and extrinsic. Intrinsic gettering employs defects found within the wafer to draw and trap the

³ Reference: [14]
⁴ Reference: [14]
⁵ Wolf and Tauber pp.61-70

contaminants, while extrinsic gettering involves the creation of a layer of extended defects or chemically reactive sites to draw and trap the contaminants.

For example, extrinsic gettering of metals impurities in silicon is often accomplished by forming a glassy layer on the surface of the wafer doped with a high concentration of phosphorous, boron or arsenic. When brought to high temperatures, the metal impurities are drawn to the layer as result of the concentration and stress gradients between the wafer and the glassy layer. After being drawn to the surface layer the impurities are subsequently trapped at the dopant sites by electrostatic force between the metal and the dopant. However, in iron contaminated boron doped CZ growth silicon, the following gettering mechanisms dominate. (See Figure 2)

2.3.1 Possible Intrinsic Gettering At Oxide Clusters

Czochralski (CZ) silicon grown crystals are used. This method of growth often produces silicon crystals with a substantial amount of oxygen (typically between $5x10^{17}$ to $1x10^{18}$ oxygen atoms/cm³)⁶. As the silicon cools, the solubility of the oxygen decreases and oxygen inclusions may form. These inclusions could act as a gettering sites for iron as the iron is trapped at defect sites between the clusters and the surrounding silicon matrix.

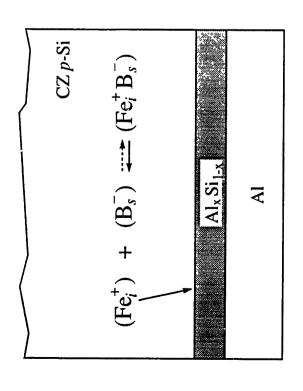
2.3.2 Extrinsic Iron Gettering by Aluminum in Boron-Doped Silicon

Two extrinsic gettering mechanisms are postulated to explain iron gettering by aluminum. The first is driven differences in iron solubility in silicon and aluminum/aluminum silicide. Since iron has a higher solubility in aluminum/aluminum

8

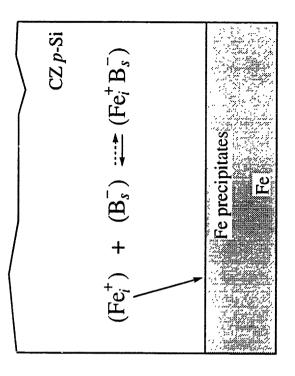
⁶ Wolf and Tauber p. 59

Possible Gettering Mechanisms



Segregation induced gettering:

 $C_s(Fe)$ in $Al_xSi_{1-x} >> C_s(Fe)$ in silicon



Fe precipitation induced gettering:

[Fe] supersaturation at contact surface

Any Internal Gettering by Oxygen Precipitates (CZ p-type silicon)?

Figure 2: Possible gettering mechanisms for iron contaminated boron doped silicon. Aluminum gettering is shown on the left. Iron gettering and intrinsic oxide will also be explored in future work.

silicide (Al_xSi_{1-x}) than in silicon alone the iron should diffuse toward the Al_xSi_{1-x} region. When iron contaminants reach the Al_xSi_{1-x} layer, a solid solution of aluminum, silicon and iron could be formed. Also the defects at the boundary between the Al_xSi_{1-x} and the silicon could form traps for the iron contaminants.

2.4 Deep Level Transient Spectroscopy (DLTS)

Deep level transient spectroscopy is a method of using capacitance measurements across a reverse-biased p-n diode to examine deep levels in a band gap. In this case, Schottky barriers are used instead of p-n diodes. Transient capacitance measurements across diode allow measurement of trap activity where steady state methods fail to detect such transient phenomenon. DLTS also has the advantage over other methods of testing because it directly measures the electrical activity of a sample. It is highly accurate; concentrations as small as 10⁻¹¹ cm⁻³ have been measured. In this project, DLTS is used to measure the concentrations of Fe-B pairs in the silicon wafer by characterizing the trap sites as a function of different gettering treatments.

2.4.1 DLTS Theory

When a p-n junction (or Schottky barrier) with a deep level in its depletion region is placed under reverse bias, trap will be filled. If a capacitance measurement is taken right after the reverse bias pulse the trap will be filled. At a later time, after the thermal energy of the system allows the trapped carriers to escape the capacitance will be smaller. (See Figure 3) The magnitude of the difference in capacitance can be used to determine the trap parameters such as emission rate and trap depth.

Figure 3a: Induced charge separation between the trapped holes and the ekectrons in the valence band (leading to capacitance) when reverse bias is applied..

Ec <u>P</u>

Ev

Figure 3b: As trapped carriers are thermally excited and annihilated the capacitance decreases.

Emission will not occur unless there is enough thermal energy in the system for the trapped carriers to escape the trap. By scanning over a temperature range and noting the temperature at which the trap begins to emit the trap depth can be determined. (See Figure 4)⁷

Finding the correct sample interval is important to getting useable data. If the time between t_1 and t_2 is too short, the peak of the capacitance difference will be wide and short making it harder to determine the true value of the temperature of the peak. If the time between t_1 and t_2 is too long, the time between reverse pulses will also need to long making the time between data points on the capacitance difference curve large. The interval chosen must be a balance between these two effects. Appendix A shows the components of a typical DLTS setup.

2.4.2 Analysis of DLTS Data

2.4.2.1 Capture Cross Section

Capture cross section easily found by measuring the capture rate of the majority carrier. Since the capture rate of majority carrier is known to exponential at zero or forward bias. By measuring taking the natural log of the change in capacitance with respect to the time between reverse bias pulses it is possible to determine the majority carrier capture rate. This rate can then be plugged into the following equation to find the capture cross section (σ_n) :

$$\sigma_{p} = \frac{c_{p}}{\langle v_{p} \rangle p} \tag{5}$$

_

⁷ From Reference: [7]

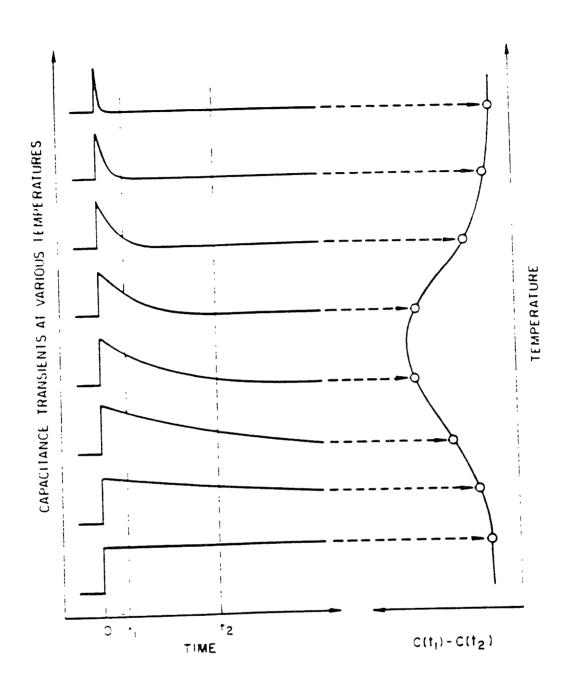


Figure 4: The depictions on the left show the change in capacitance behavior as a function of temperature. (t_1 and t_2 define the rate window) On the right, the resulting peak of the capacitance difference is shown.

where c_p is the majority carrier capture rate, $\langle v_p \rangle$ is the average velocity of the majority carrier and p is the concentration of the majority carrier.

2.4.2.2 Thermal Emission Rate

The thermal emission rate can be determined by adjusting the rate window at which signal comes through. Since the discharge from the trap is known to be The emission rate, the inverse of the trap time constant is then given by:

$$e_n = \frac{1}{\tau} = \ln(\frac{t_2 - t_1}{t_2/t_1}) \tag{6}$$

here e_n is the thermal emission rate of the minority carrier, τ is the carrier lifetime and t_1 and t_2 are the times defining the rate window.

2.4.2.3 Trap Depth

The thermal emission spectrum is assumed to have a Boltzman distribution. It can be described using the following equation⁸:

$$e_n = \left(\frac{\sigma_n < v_n > N_c}{g}\right) \exp\left(\frac{-\Delta E}{kT}\right)$$
 (7)

where g is the degeneracy of the state, N_c is the density of states at the conduction band, and ΔE is the trap depth.

The pre-exponential term is assumed to be proportional to T^2 assuming that capture cross-section is not temperature dependent. (This is generally not true but to a first order approximation it can be assumed.) Then by graphing -kln (e_n/T^2) vs. 1/T, the slope of the resulting line should be the trap depth. See Appendix A for sample analysis.

2.4.3 Leakage Current

To gather useful data the Schottky diode should have a small leakage current. The ideal diode equation for a Schottky diode is:

$$I = I_o \left[\exp \left(\frac{qV}{kT} \right) - 1 \right] \tag{8}$$

where I_o is the leakage current. For a reasonable, Schottky diode, I_o would in the 10⁻⁶ Ampere range. Low leakage currents allow smaller pulsing power and thus more accuracy.

3. Experiment

3.1 Sample Preparation

To characterize the effect of using aluminum to getter iron from boron doped silicon a variety of treatments were employed. Silicon wafers with a boron concentration of 1.3×10^{15} cm⁻³ were deposited with iron and annealed at 1000° C for 3 hours. This treatment allowed to the iron concentration in the silicon to come to approximately 1.42×10^{14} cm⁻³.

The iron on the surface of the wafer is then etched off. An aluminum layer was the deposited onto the silicon and the wafer was again annealed for times ranging from 10 to 120 minutes at 600°C, 700°C, or 800°C. (See Appendix B) After the heat treatment, the Al and Al_xSi_{1-x} were etched off from one side. The samples were etched and polished to

⁸ Reference [7]

halfway through the sample. Circular Schottky contacts, 1.8 mm in diameter, were then deposited on the etched side. (The aluminum/aluminum silicide layer on the backside acts a electrical contact to the p-type material in the Schottky diode.) DLTS is used to observe the change in the number of carriers trapped by the Fe-B pair state. (See Figure 5)

3.2 DLTS Parameters

The samples will be pulsed in cycles of 3V reverse bias to 0V forward bias. The temperature ranges from freeze out at about 40 K to room temperature at 300 K. The temperature increases at a rate of 0.1 K/sec.

4. Conclusions

Due to time constraints no DLTS spectra of the samples prepared above have been taken. Previously, some samples were tested using Electron Beam Induced Current microscopy EBIC to determine if gettering had an effect on lifetime. The results are shown in the following table⁹:

Sample Description	Iron Concentration (cm ⁻³)	Diffusion Length (µm)
Reference	0	160
800°C, 120 min Anneal	2x10 ¹²	29
800°C, 10 min Anneal	5x10 ¹³	19
Iron Contaminated	1x10 ¹⁴	10
No anneal		

⁹ Reference [16]

Experimental Procedure

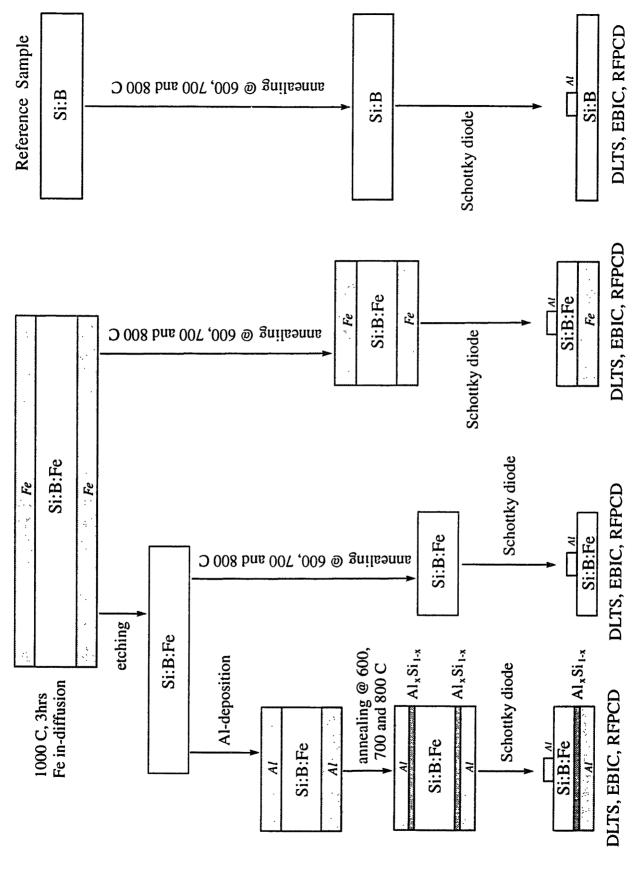


Figure 5: Experimental procedure for sample preparation. Branch on the left describes the samples for this project. Other branches describe future work

This preliminary data shows that lifetime does increase with gettering time. Unfortunately, EBIC measurements are not direct measurements of lifetime. As mentioned before, DLTS spectra need to be taken to directly and accurately characterize the effect of using aluminum to getter iron.

Earlier DLTS work on similar samples show that aluminum is effective in gettering iron. Other samples also show the success of using aluminum to getter iron. (See Figure 6) This data was taken from samples with a lower iron concentration $\sim 1 \times 10^{14}$ cm⁻³. After testing is completed 800°C, this data may be scaled to compare against the new samples with the higher iron concentration of 1.42×10^{14} cm⁻³.

5. Future Work

The work included in this thesis is only a small part of a larger project to characterize the aluminum gettering process. Further experiments to determine whether the only effect being measured is the gettering of iron contaminants by aluminum are scheduled. By taking DLTS spectra from samples with no aluminum deposition that undergo the same heat treatments as the samples studied here, the effect of heat treating the sample alone would be measured. Also heat treatment of samples with the iron layer left on will be studied to see the effectiveness of iron gettering of iron contaminants. Finally, a more complete reference group of samples will be studied to see if the heat treatment alone affects the uncontaminated sample. (Refer to Figure 5)

Another point of interest is the degeneration of the iron-boron pairs into boron sites and iron inclusions with subsequent heat treatments. If the iron gettering is performed in the middle of a process subsequent heat treatments could dissociate the iron-boron pairs

Preliminary Experimental Evidence of Al Gettering Effect

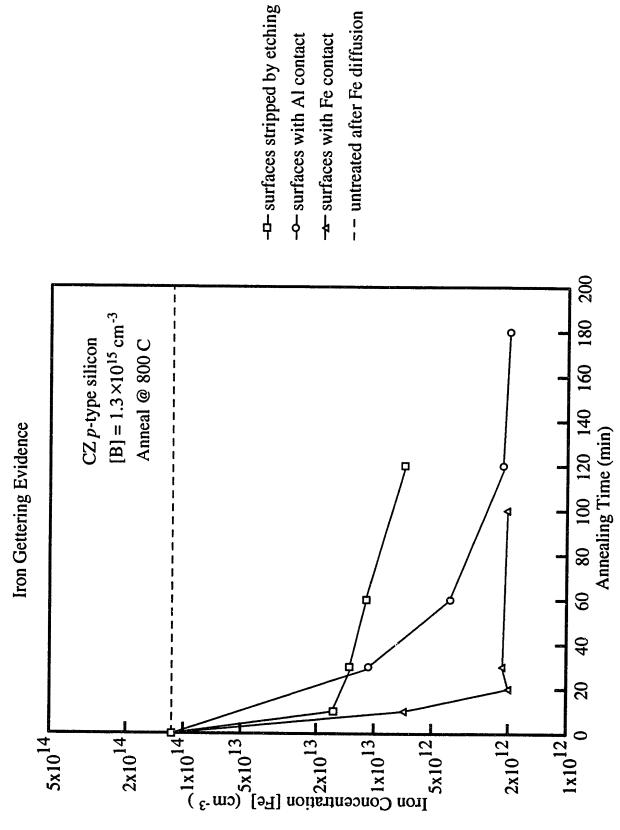


Figure 6: Data marked with diamods show effect of aluminum gettering of iron using a heat treatment of 800°C anneal. Other data show effect of other gettering mechanisms in iron contaminated boron doped silicon.

leaving iron inclusions (and their associated deep level recombination sites) or let the iron diffuse back into the sample. Before aluminum gettering is practiced in a manufacturing environment these issues should be addressed.

Appendix A

Figure A1 shows a sample of a DLTS spectrum. The sample being tested is a reference sample which was contaminated with iron but not subjected to an annealing step. As expected there is only the single Fe-B peak. To gather data on trap parameters a variety of rate windows must be used. The data shown is only for one rate window that was used in testing this sample.

Data from this sample and others are used to demonstrate analysis. Data from the same sample with five different rate windows were taken. The table below shows the raw data:

t ₁ (ms)	t ₂ (ms)	(ms)	e _n (ms ⁻¹)	Peak Temp (K)	$1/T_{\text{peak}} (K^{-1})$
0.4	0.8	0.223	4.486	61.9	0.162
1	3	2.089	0.479	58.7	0.0170
1	5	4.379	0.228	57.4	0.0174
3	9	6.6269	0.159	55.5	0.0180
10	30	20.898	0.047	52.80	0.0189

By graphing the $-kln(e/T^2)$ vs. 1/T, the trap depth and the capture cross section can be found. The trap depth is found the slope of the line divided by k (Boltzman constant) and the capture cross section is the y-intecept divided by the other terms in the coefficient as defined in the section above. (See Figure A2) For this data the trap depth is found to be 0.125 eV.

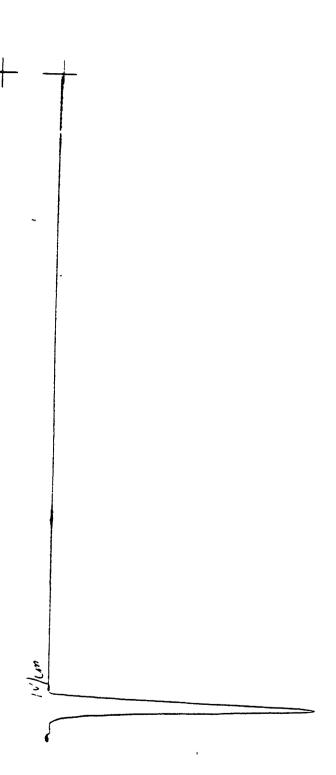


Figure A1: A typical DLTS spectrum. The y-axis is the DLTS output. The x-axis is temperature.

Capture Cross Section and Trap Energy 0.0016 0.0014 0.0013 0.0012 0.0017 0.018 0.019

Figure A2: A graph of the $-\ln(e_n/T^2)$ vs. 1/T.

Appendix B

The following table is a summary of heat treatment and characteristics of the samples prepared. Annealing times and temperatures refer to annealing done after deposition of aluminum unless otherwise noted. Original thickness refers to thickness of samples with both surfaces coated with aluminum unless noted. And final thickness refers to thickness of the samples after polishing before Schottky barrier deposition.

Annealing	Annealing	Original Thickness	Final Thickness	
Temperature (oC)	Time	(microns)	(microns)	
	(minutes)			
600	10	520	270	
600	30	530	250	
600	60	520	260	
600	120	480	210	
700	10	530	260	
700	30	540	270	
700	90	530	240	
700	120	560	200	
800	120	•	280	
800 - undoped*	120	-	540	
Fe-doped*	-	-	570	

^{*}No aluminum deposited on these samples

THESIS PROCESSING SLIP FIXED FIELD: ill ______name _ index ______ biblio ____ Aero Dewey Eng Hum

	Lindgren	Music		cience	and the same
TITLE VA	ARIES: P				
NAME V	ARIES: ►	4 Ati	hya		
IMPRINT	ion: 26	OPYRIGHT	Γ)		
	EGREE: B				:&E
SUPERV	/ISORS:				

____cat'r:

DEPT: Phy

PYEAR: 1996

→ DEGREE: B.S.

NAME: THIENPRASIT, Jeanne

date:

NOTES: