Investigation and Application of High-Efficiency Large-Step-Down Power Conversion Architectures

by

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Abstract

In this thesis, we introduce two large-step-down dc-dc converter architectures that are designed to provide zero-voltage switching of the power devices. While the techniques used in these converters can be used in a wide range of applications, the operating voltage and power levels used in this thesis are for data centers, where dc distribution power delivery is expected to see its first deployment. The nominal 380 V bus voltage will need to be converted to 12 V using a high-efficiency dc-dc converter that can deliver several hundred watts of power to each rack to power the servers. The converters are expected to operate efficiently across a wide input voltage range of 260 V to 410 V and down to powers in the tens of watts range.

The first converter architecture is based on the concept of an Impedance Control Network (ICN) resonant converter. Using phase-shift control along with a specifically designed impedance network, this converter can maintain resistive loading of the inverters as the input voltage varies. To back down in power, the converter can be efficiently operated using burst (on/off) mode control. To deliver lower power, we introduce an additional control technique using Variable Frequency Multiplier (VFX) inverters and/or rectifiers.

The second converter architecture combines the properties of an active bridge converter with multiple stacked inverters, a multi-winding single core transformer, and a reconfigurable rectifier. The stacked inverter topology improves the range of powers over which zero-voltage switching can be achieved. The multi-winding transformer and reconfigurable rectifier further extend the efficient operating range to very low powers by reducing core loss and increasing zero-voltage switching capability.

Both proposed architectures are suitable for large-step-down, wide-input voltage, wide-output power applications such as dc-dc converters for dc distribution.

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When I applied to graduate schools, I applied for Master's only because I figured only a couple more years of school would be enough. Little did I know that I would be spending many more years at MIT than I had originally anticipated. In just a few short weeks, it became abundantly clear to me that MIT was an amazing place full of an incredible diversity of people. I am just so happy to have been a part of this community. Thank you to all my friends who have made me believe I have truly found paradise – Stephen, Michael, Phil, Nick, Dave, Ian, Grant, Seoyoung, Morgan, Richard, Aaron, Kevin, Chi, Kendall, Marianna, Janet, Francine and so many more.

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I would also like to thank my family. Mom and Dad, you have taught me well and I know I would not be here today without your love and support. I know I can always depend on you, and no

matter how much I learn, you will still have things to teach me. Thank you, for all you have done my entire life.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Direct-current (dc) systems are beginning to become more prominent due to the increasing usage of inherently dc devices such as solar photovoltaic (PV) systems, battery systems, LEDs, electronic loads, etc., as well as an effective means of connecting all of these components together through the use of increasingly efficient power electronic converters. Improvements in performance of power electronics coupled with their expanded use could lead to dramatic reductions in electricity consumption (as much as 20-30% by some estimates [1,2]).

A particular need is for high conversion ratio converters that can take in hundreds of volts and deliver tens of volts efficiently. Furthermore, these converters must be able to maintain high efficiency across a wide operating range. Presently, power electronics at the grid-interface level have poor efficiency (typically only 70-90% at full load), and their efficiency typically falls off rapidly at reduced loads, such that average efficiency and losses are even worse. For example, it has been estimated that power supply losses account for 20 to 70% of all energy that electronic products consume [3]. There is thus a need to develop improved power electronics that:

1. Provide greatly improved peak and average efficiencies;
2. Provide reduced size, weight and cost to enable greater adoption and utilization; and
3. Effectively handle large conversion ratios and wide operating ranges.

The research proposed for this thesis targets these challenges.

1.1 Motivation

Take the application of dc distribution within a building. As internet and cloud-based data and services become more ubiquitous in today's society, more attention is being paid to the amount of energy consumed by the data centers that store and manipulate that information [4]. Therefore, dc distribution (nominally at 380 V dc) is being seriously considered as an alternative to ac distribution in commercial buildings and data centers, as it offers higher efficiency, higher reliability, more effective management of power factor correction, and easier integration of distributed renewable sources and energy storage [5,6,7]. This nominal voltage is selected because it is close to the output voltage provided by many single-phase ac/dc power factor correction converters for grid interface, so there are many components with large production volume, good price, and performance for that voltage range. Early demonstrations show that 380 V dc distribution architectures can result in energy savings of around 15% over 208 V ac

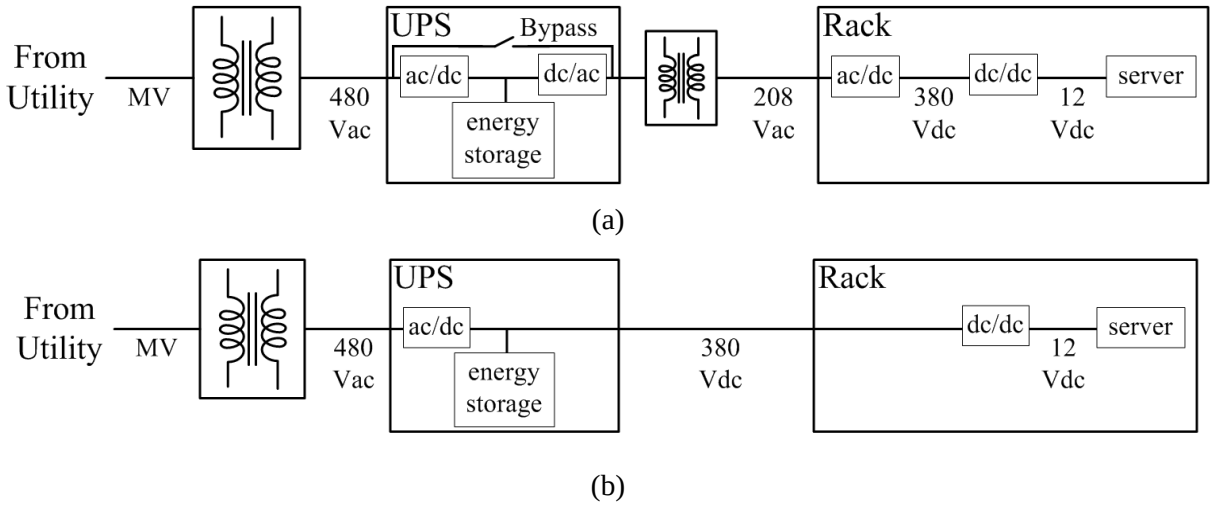


Figure 1-1: Data center power delivery structure for (a) 208 V ac distribution and (b) 380 V dc distribution [8,9].

distribution in data centers due to the higher distribution voltage and fewer voltage conversion stages in dc distribution systems as shown in Figure 1-1 [8,9].

A 380 V dc distribution standard is under development in the US and Europe [5,6,7], and could have a significant impact owing to the large amount of energy consumed in data centers (between 1 and 2% of total electrical energy consumption by some estimates) [3,4,10]. Crucial to the effectiveness of dc distribution, however, are the dc-dc converters that convert the voltage. In data centers, where this dc distribution architecture is expected to see its first deployment [11], the 380 V (actually 260 V - 410 V when transient holdup considerations are included [9]) will need to be converted to 12 V using a dc-dc converter located in each rack to power the servers. To make this architecture compelling, however, converters that can maintain high efficiency across the full input voltage range and output power range will be needed.

Ever increasing attention is being paid to the efficiency of power supplies for computers and servers. To be ENERGY STAR certified, power supplies must adhere to certain efficiency levels across output power as shown in Table 1-1 [12]. While the current standard only mentions ac-dc power supplies, the inclusion of dc-dc power supplies is expected in version 3 and is mentioned on the ENERGY STAR website [13]. Another metric for power supply efficiency is the 80 PLUS performance specification, which has a tiered system of efficiencies as seen in Table 1-2 [14]. The testing protocol does include dc-dc power supplies but does not have a specification for power factor, total harmonic distortion and frequency [15]. The efficiency is calculated as the ratio of output (dc) power to the input (dc) power. These two efforts indicate a lot of interest in and need for high efficiency power supplies that can perform well even down to 10% of rated load.

Table 1-1: Power Supply Efficiency Requirements [12]

PSU Type	Rated Output Power	10% Load	20% Load	50% Load	100% Load
Multi-output (Ac-Dc)	All Output Levels	N/A	85%	88%	85%
Single-output (Ac-Dc)	All Output Levels	80%	88%	92%	88%

Table 1-2: 80 PLUS Certification Efficiency Requirements for 115V Internal Non-Redundant Power Supplies [14]

80 PLUS Certification	10% Load	20% Load	50% Load	100% Load
80 PLUS	--	80%	80%	80% / PFC 0.90
80 PLUS Bronze	--	82%	85% / PFC 0.90	82%
80 PLUS Silver	--	85%	88% / PFC 0.90	85%
80 PLUS Gold	--	87%	90% / PFC 0.90	87%
80 PLUS Platinum	--	90%	92% / PFC 0.95	89%
80 PLUS Titanium	90%	92% / PFC 0.95	94%	90%

Other applications that require a 380 V converter may include but are not limited to the dc-dc bus converters following three-phase power factor correction circuits, microgrid interfaces, and renewable energy sources [16]. These applications use high voltages that require high voltage rated switches. Therefore, ways to reduce switch stress are also important [17]. Wide-input voltage dc-dc converters operating between hundreds of volts and tens of volts are also important to applications such as hybrid and electric vehicles (such as for charging and converting among different voltage domains within the vehicle itself) [18].

1.2 State of the Art

Developing technologies to achieve greater efficiency and miniaturization of power converters that deliver energy from high-voltage dc to low-voltage dc loads is challenging, as the high input voltage and large voltage conversion ratios tend to lead to large semiconductor switch and magnetic core losses, and the wide operating range (e.g., input voltage or operating power) places constraints on many design techniques.

To reduce switching loss, many power converters utilize soft-switching techniques - zero-voltage switching (ZVS) and/or zero-current switching (ZCS) – in which the switch voltage and/or current are zero at the switching transition. For example, consider the idealized half-bridge structure loaded with a current source as shown in Figure 1-2(a). Such a structure can be seen in a dc-dc buck converter, for example. The idealized current and voltage waveforms of the switches are shown in Figure 1-2(c). When a switch is on, it is conducting the load current. When the switch is off, it is blocking the input voltage. In

practice though, each switch has non-ideal parasitics and limitations which greatly influence the voltage and current behavior at the turn-on and turn-off transitions. Some of these non-ideal elements are shown in Figure 1-2(b). Namely, in parallel with each switch are a diode and a capacitor representing the intrinsic body diode and capacitance often found internal to a transistor. Due to capacitance, the voltage across each device cannot change instantaneously. Similarly, the current through each switch cannot change instantaneously. A simplified view of these effects can be seen in the zoomed in waveforms of Figure 1-2(d) which focuses on the turn-on and turn-off transitions. When Q_1 is turned off, its current ramps down, but the load current must remain constant so the difference in current comes from the two capacitors. This capacitor current slowly charges C_1 and discharges C_2 which causes the voltage to slowly change. During this time, it can be seen that the product of switch current and switch voltage is not zero for Q_1, but it is low due to the slow change in voltage. In this case, Q_1 exhibits zero-voltage turn off. Once the current through Q_1 reaches zero, the current continues to be supplied through the capacitors until the voltage across C_2 reaches $-V_D$, the voltage at which D_2 turns on and conducts the full load current. At this point Q_2 can turn on and its current ramps up linearly. Once again, the product of switch current and switch voltage is not zero but is low due to the relatively low voltage drop of the diode when compared to the input voltage. In this scenario, Q_2 is considered to have zero-voltage turn on. This particular switch transition where Q_1 turns off and Q_2 turns on is considered to be an example of ZVS.

On the other hand, Q_1 turning on does not exhibit ZVS. When Q_2 is turned off, its current will ramp down linearly with D_2 supplying the difference in current to the load. Again, this is considered to be a zero-voltage turn off because the voltage across the switch is close to zero. When Q_1 is turned on, its current ramps up linearly with D_2 still supplying the difference in current. While D_2 continues to conduct, the voltage across Q_1 is V_{in} plus V_D. Only when the current through Q_1 reaches the full load current can the voltage begin to fall because the diode is no longer conducting. Now, the product of switch current and switch voltage for Q_1 is much higher indicating overlap loss. Additionally, the $\frac{1}{2}CV^2$ energy that was stored in the capacitor must be dissipated and the only way to dissipate it is through the switch (in particularly through the switch resistance not shown in Figure 1-2(c)) and is indicated by the large spike in current through Q_1. This loss is exacerbated when frequency is increased, when the input voltage is high, and when the switch capacitance is high, which is often the case for high voltage devices. Not only is switching loss an issue, but there is often large amplitude high frequency ringing in the current and voltage waveforms during a hard-switched transition when parasitic inductance is considered. This ringing can require increased voltage ratings on the switching devices due to overshoot as well as undesirable Electromagnetic Interference (EMI) effects. Without soft switching, transistor switching loss can prevent high efficiency from being obtained and also limits power density (owing to the need to operate at low switching frequencies).

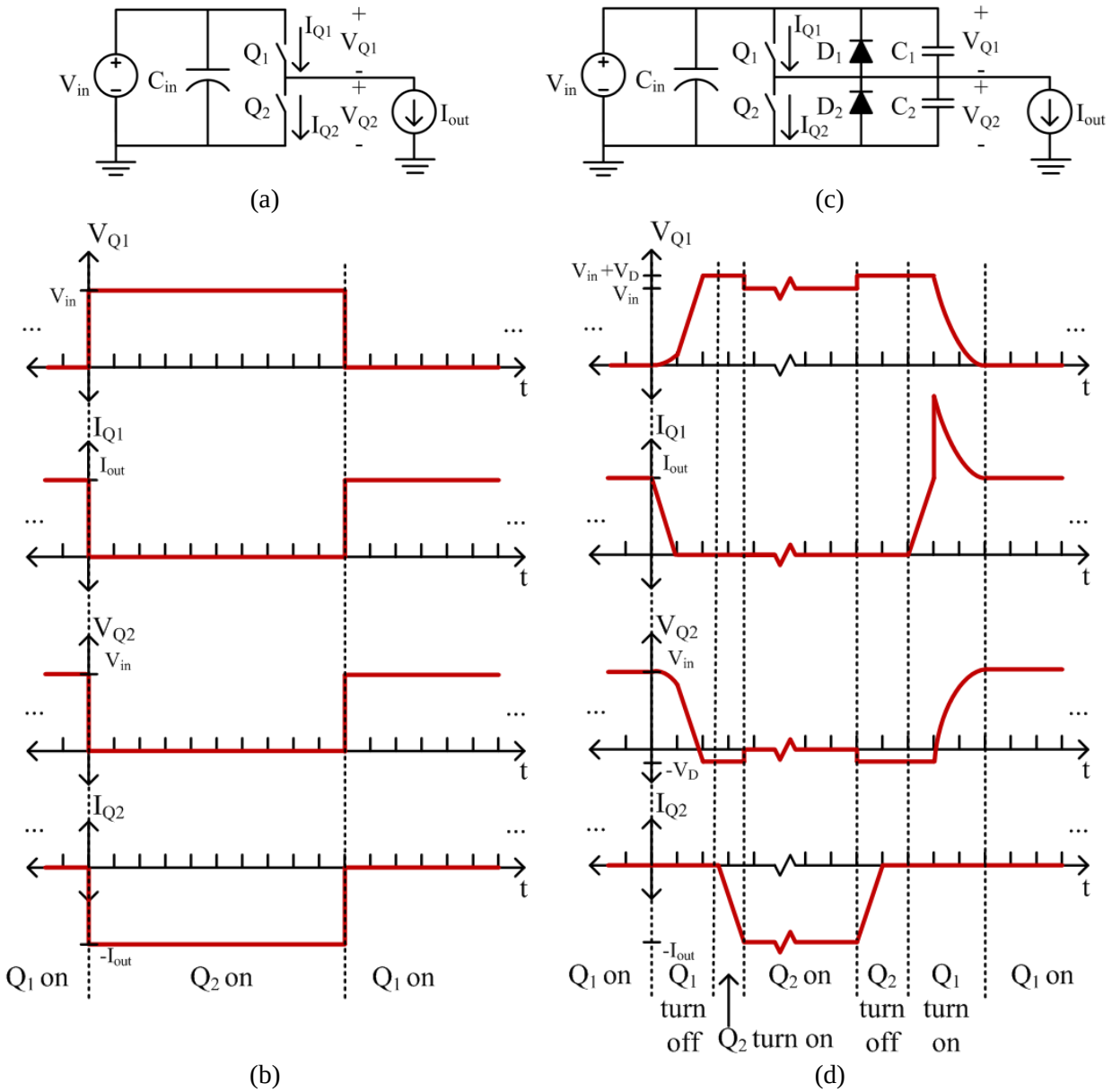


Figure 1-2: (a) An ideal half-bridge supplying a constant load current and its corresponding (b) idealized switch voltage and current waveforms. (c) A half-bridge switch structure with discrete parallel diode and capacitance representing the intrinsic body diode and capacitance of a transistor supplying the same constant load current. (d) The turn on and turn off switch transitions for a non-ideal half-bridge structure with constant current load. Both switches can turn off with low voltage but only the bottom switch can turn on at low voltage. The top switch has overlap loss as it begins conducting while still sustaining the full input voltage, $V_{in,}$ plus the bottom diode's forward voltage drop, V_D. It must also dissipate the energy stored in the parallel capacitance as indicated by the large spike in current.

Unlike the example above, there are converter topologies that can provide alternating or bidirectional current to the half-bridge inverter to enable soft-switching by charging and discharging the intrinsic capacitance on all transitions. This thesis will expand upon two families of dc-dc converters - resonant converters and dual active bridge converters. Soft-switching techniques often provide high efficiency operation but only under specific operating conditions. Performance tends to degrade greatly when considering requirements of operation across widely varying input voltage and wide output power. In particular, as the input voltage varies from nominal or the output power decreases, the circuit waveforms begin to deviate from desirable characteristics (e.g., ZVS/ZCS is lost, conduction current increases, etc.). This challenge in maintaining high efficiency is tied to both the circuit design and the control methodology.

1.2.1 Resonant Converters

Resonant converters deliver power from a dc input to a dc output, but with an approximately sinusoidal intermediate ac waveform (e.g., current), with the ac usually implemented at high frequency to minimize component size. A benefit of many resonant converters is that the ac intermediate waveforms can often be used to provide soft switching for the inverter and/or rectifier stages, facilitating high-frequency operation and low EMI. One common technique used to enable output control while maintaining soft-switching in resonant converters (e.g., series, parallel, series-parallel, LLC converters, etc.) is through frequency control. By modulating the converter switching frequency, and using a resonant "tank" with a high frequency selectivity, variations in input voltage can be countered so that the output voltage is not affected [19,20,21]. At the nominal input voltage, the switching frequency is set so that a resonant tank will have desirable characteristics at the fundamental frequency while other harmonics are filtered out. As the input voltage varies, the switching frequency is varied so that the reactive elements begin to absorb the changes in voltage thereby keeping the output voltage constant. Take for example, a simplified version of a series resonant converter with a half-bridge inverter as shown in Figure 1-3(a). If designed properly, the resonant tank (L_R,C_R) will look like a short at a given switching frequency and a high impedance at frequencies far away from this switching frequency. This has the effect of shaping the inverter current to be sinusoidal even if the inverter voltage is a square wave as shown in Figure 1-3(b). At the nominal input voltage, and when the inverter is switched at the nominal frequency (i.e., $f_s = 1/T_0$), the current will also be in phase with the fundamental of the voltage providing resistive loading of the inverter and ZVS/ZCS. (Technically, there is usually a minimal amount of current at the voltage transition to ensure ZVS such as demonstrated earlier, which requires operation at a frequency somewhat above the tank resonant frequency to achieve.) When the input voltage increases above the nominal value, without any control handle, the output voltage would also increase. To prevent this, the switching frequency is

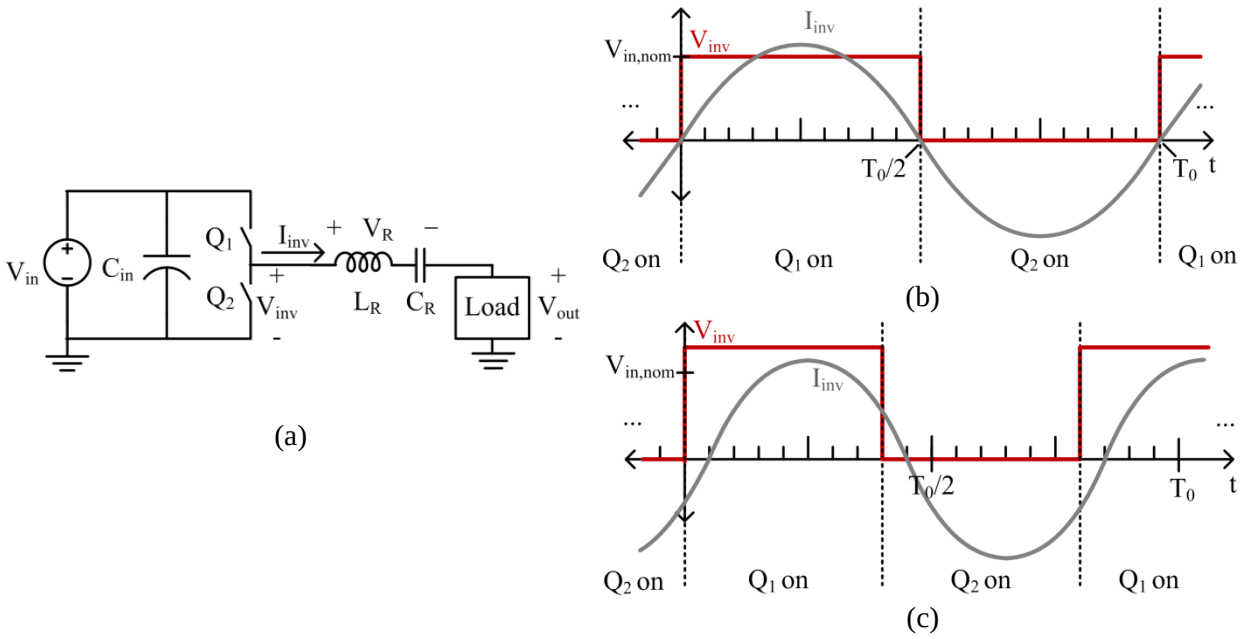


Figure 1-3: (a) An ideal half-bridge supplying a load through a series resonant tank comprising inductor L_R and capacitor C_R. (b) Idealized inverter square wave voltage and sinusoidal current waveforms when the input voltage, V_{in}, is equal to the nominal input voltage. (c) Idealized inverter square wave voltage and sinusoidal current waveforms when the input voltage, V_{in}, is more than the nominal input voltage and the frequency has been increased so that the voltage across the resonant tank, V_R, increases to prevent the load voltage from increasing. It can be seen that the inverter current becomes inductive and lags the voltage.

increased so that the resonant tank will begin to look inductive and develop a positive voltage drop across it in order to keep the output voltage fixed. Now that there is some inductive loading, the current will begin to lag the voltage, as seen in Figure 1-3(c). While ZVS can be maintained, the increase in frequency can cause several loss mechanisms including additional reactive current adding additional conduction loss for the same delivered power. The additional challenge to varying frequency is the potential for increased switching loss when frequency increases, challenges in designing magnetic components and EMI filters to work well under a wide frequency range, and the potential for circulating currents that do not back off with power for some kinds of resonant tanks, such as parallel-resonant tanks [19].

To alleviate the challenges of operating under a wide frequency, another method of control that can be applied to resonant bridge converters at fixed frequency is phase-shift control [22,23,24]. In this method, multiple inverter legs are phase-shifted from each other to counteract variations in input voltage and maintain output power. Take for example, a simplified version of a series resonant converter with two half-bridge inverters as shown in Figure 1-4(a). When the input voltage is at the nominal value, the two inverters are switched together, with one lagging the other by half a period as shown in Figure 1-4(b). This results in inverter currents that are in phase with the inverter voltages for resistive loading and soft-switching. When the input voltage increases above the nominal value, the two inverters are phase-shifted

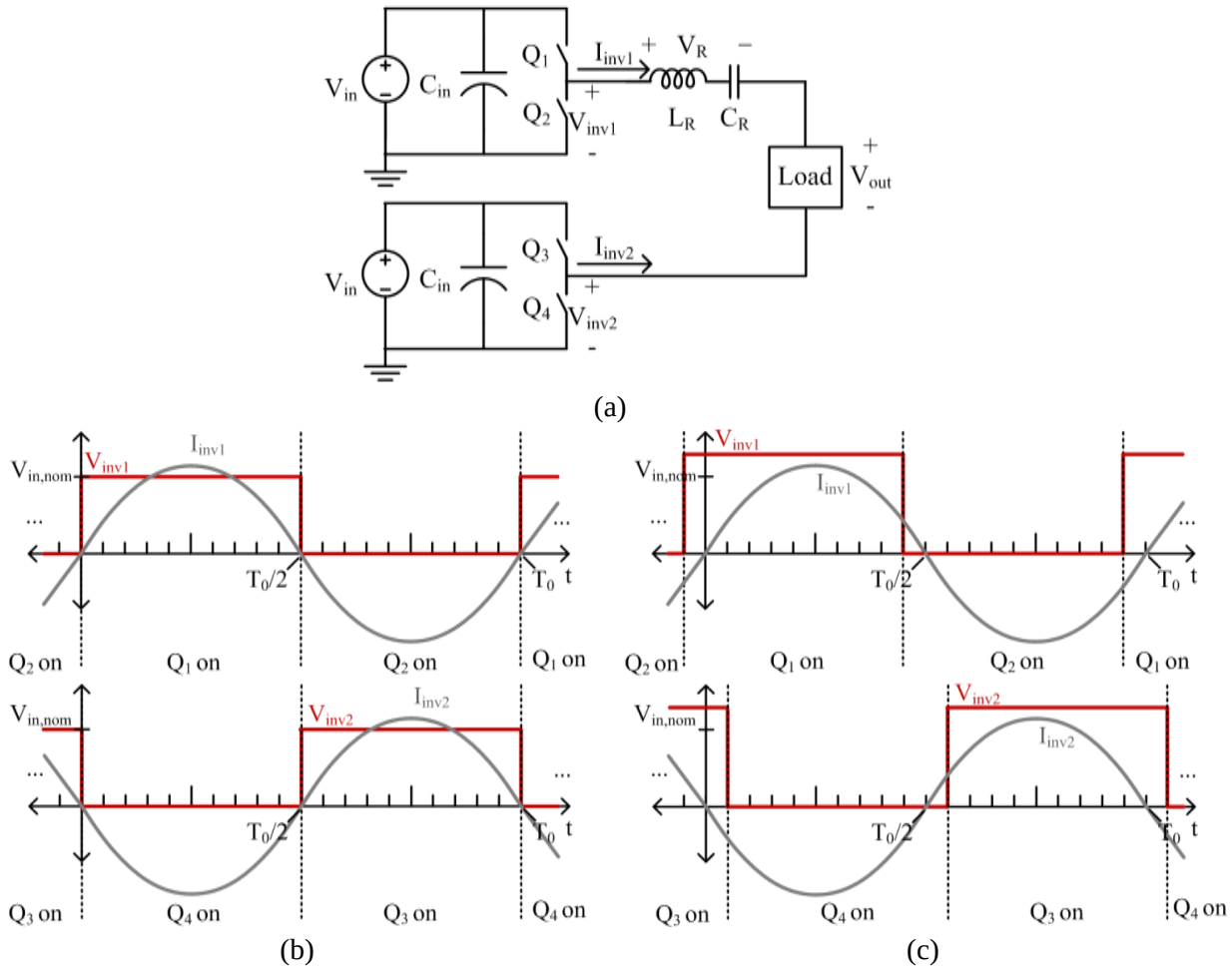


Figure 1-4: (a) Two ideal half-bridges supplying a load through a series resonant tank comprising inductor L_R and capacitor C_R. (b) Idealized inverter square wave voltage and sinusoidal current waveforms when the input voltage, V_{in}, is equal to the nominal input voltage. The bottom inverter's waveforms are one half cycle delayed from the top inverter's waveforms. (c) Idealized inverter square wave voltage and sinusoidal current waveforms when the input voltage, V_{in}, is more than the nominal input voltage. The bottom inverter is delayed, or phase-shifted, further from the top inverter so that the average voltage across the load does not increase. Under this scenario, the top inverter current lags the top inverter voltage and the bottom inverter current leads the bottom inverter voltage.

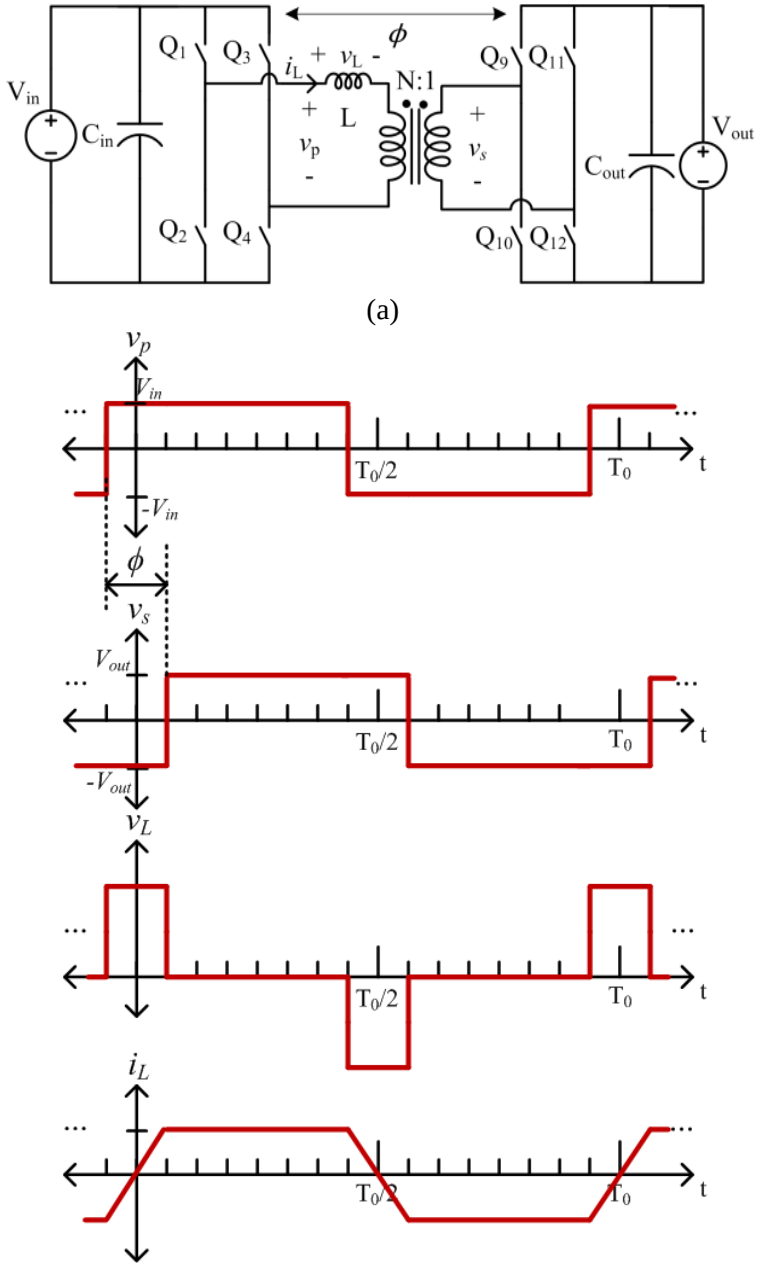
from each other as shown in Figure 1-4(c). This results in a three-level voltage at the output. While the peak of the output voltage may be higher, the average is maintained due to the level at zero that the phase-shift creates. Unfortunately, as the inverters are phase shifted from each other, it is possible for asymmetric current waveforms to arise. In Figure 1-4(c), the top inverter current lags the top inverter voltage while the bottom inverter current leads the bottom inverter voltage. This asymmetry can increase conduction loss due to reactive current as well as a loss of ZVS, particularly in the inverter leg that begins to see capacitive current. For converters with very high input voltages, the loss of ZVS can result in substantial power loss and decrease in efficiency.

For both the frequency controlled and phase-shifted resonant converters, ZVS and minimal conduction loss are possible at the nominal input voltage; however, when the input voltage is increased, both types of converters begin to suffer increased loss for the same power delivered. This is because the inverter current becomes more reactive. Furthermore, the design of magnetics and EMI filters for the frequency controlled converter becomes challenging due to the wide frequency operation. On the other hand, the fixed frequency phase-shifted converters suffer from capacitive loading of one or more inverters resulting in the loss of soft-switching, which can drastically affect efficiency in the presence of high input voltages and frequencies.

1.2.2 Dual Active Bridge Converters

The Dual Active Bridge (DAB) converter is another soft-switched converter, but one in which the intermediate ac waveforms are not sinusoidal. It has gained significant interest due to many desirable characteristics such as bidirectional power flow capability, high power density, low component count, soft-switching capability, isolation and high efficiency [25,26]. For these reasons, DAB converters are popular for use in data centers, electric vehicles and grid interfaces [27,28,29,30]. As shown in Figure 1-5(a), the traditional DAB features a relatively simple design comprised of a full bridge inverter coupled to an active full bridge rectifier through an energy transfer inductance and transformer. For some designs, the energy transfer inductance can come from the leakage inductance of the transformer such that no discrete inductors are needed, providing a very compact design.

To control the amount of power, one bridge is phase-shifted from the other to generate a voltage across the inductor and a corresponding increase or decrease in the current as demonstrated in Figure 1-5(b). The power will flow from the leading bridge to the lagging bridge, so bidirectional power flow is easily achieved. If the transformer turns ratio is the same as the input voltage to output voltage ratio, the energy transfer inductance will ideally have zero voltage across it for a majority of the switching cycle. When this is the case, the current remains flat and results in a flattop trapezoidal current. Under this condition, the converter can operate very efficiently because the RMS current to average current ratio is close to one, providing minimal conduction loss. Also, the resulting current is mostly in phase with the two square bridge voltages and above a certain power level can achieve soft-switching of all devices. (Viewed another way, the DAB provides significant energy transfer through both the fundamental and third harmonic components of current, which provides excellent energy transfer for a given conduction loss.) The DAB is attractive because it achieves very high efficiencies when the transformer ratio is well matched to the input-to-output voltage ratio and at high power where the converter achieves ZVS.



(b)

Figure 1-5: (a) A Dual Active Bridge (DAB) converter using a full-bridge inverter and rectifier. Two bridges are phase-shifted from each other across a transformer with turns ratio, N, and an inductance, L. (b) Example operating waveforms of the DAB where the rectifier square wave voltage is phase-shifted by angle, ϕ, after the inverter square wave. In this illustration, the dc input voltage to dc output voltage ratio is equal to the transformer turns ratio, resulting in a flattop trapezoidal current.

When the DAB is operated across a wide range of voltages and powers, its efficiency can degrade dramatically. If the transformer turns ratio does not match the input-to-output voltage ratio, the RMS current can increase and one of the bridges may lose zero-voltage switching, increasing loss. For example, Figure 1-6(a) shows the operating waveforms when the input voltage is higher than the nominal input voltage (the input voltage at which the voltage after the inverter divided by the voltage at the rectifier is equal to the transformer turns ratio). As can be seen, the inductor will have a non-zero voltage across it for the full switching cycle resulting in a current that is always increasing or decreasing. This leads to a higher RMS current and an increase in conduction loss. In this particular example, it is possible for the rectifier to lose ZVS because of the continual sloping. On the other hand, Figure 1-6(b) shows the operating waveforms when the input voltage is lower than the nominal input voltage. Again, the inductor current is always increasing or decreasing and this particular sloping can cause the inverter to lose ZVS.

The DAB converter can also suffer substantial efficiency degradation as load decreases. To reduce power, the phase shift is reduced resulting in a lower overall inductor current at the switching transitions as demonstrated in Figure 1-6(c). At low currents, the available current is not enough to provide lossless voltage transitions and the DAB can lose ZVS, substantially increasing switching loss. Furthermore, because the voltage applied to the transformer remains constant, the transformer core loss stays constant across power (for a given voltage conversion ratio). Consequently, the core loss can become a significant portion of the total power as the power decreases, yielding reduced light-load efficiency.

1.3 Thesis Scope and Objectives

The work presented in this thesis is targeted at providing converter architectures targeted at addressing the limitations of resonant and DAB converters to operate across wide input voltage and load ranges. Namely, it is important that the converter can maintain soft-switching and low conduction loss across the full operating range. We further consider topologies of the various inverter, transformation, and rectifier stages to allow for improved large-step-down performance and reduced switch stress. Techniques to reduce magnetic core loss are also beneficial, especially at low power levels. Another important consideration in the design of converters is power density. While power density is not a particular focus of this work, several techniques and design choices employed do inherently improve power density.

The first topology presented is the Impedance Control Network (ICN) resonant converter. The ICN technique uses phase-shift control paired with a specifically designed lossless multiport network (termed an “Impedance Control Network”) to enable both zero-voltage and near-zero-current switching to be maintained across input voltage variation. Unlike traditional resonant converters, this topology can maintain resistive loading of the inverters across a wide operating range and therefore efficiency does not

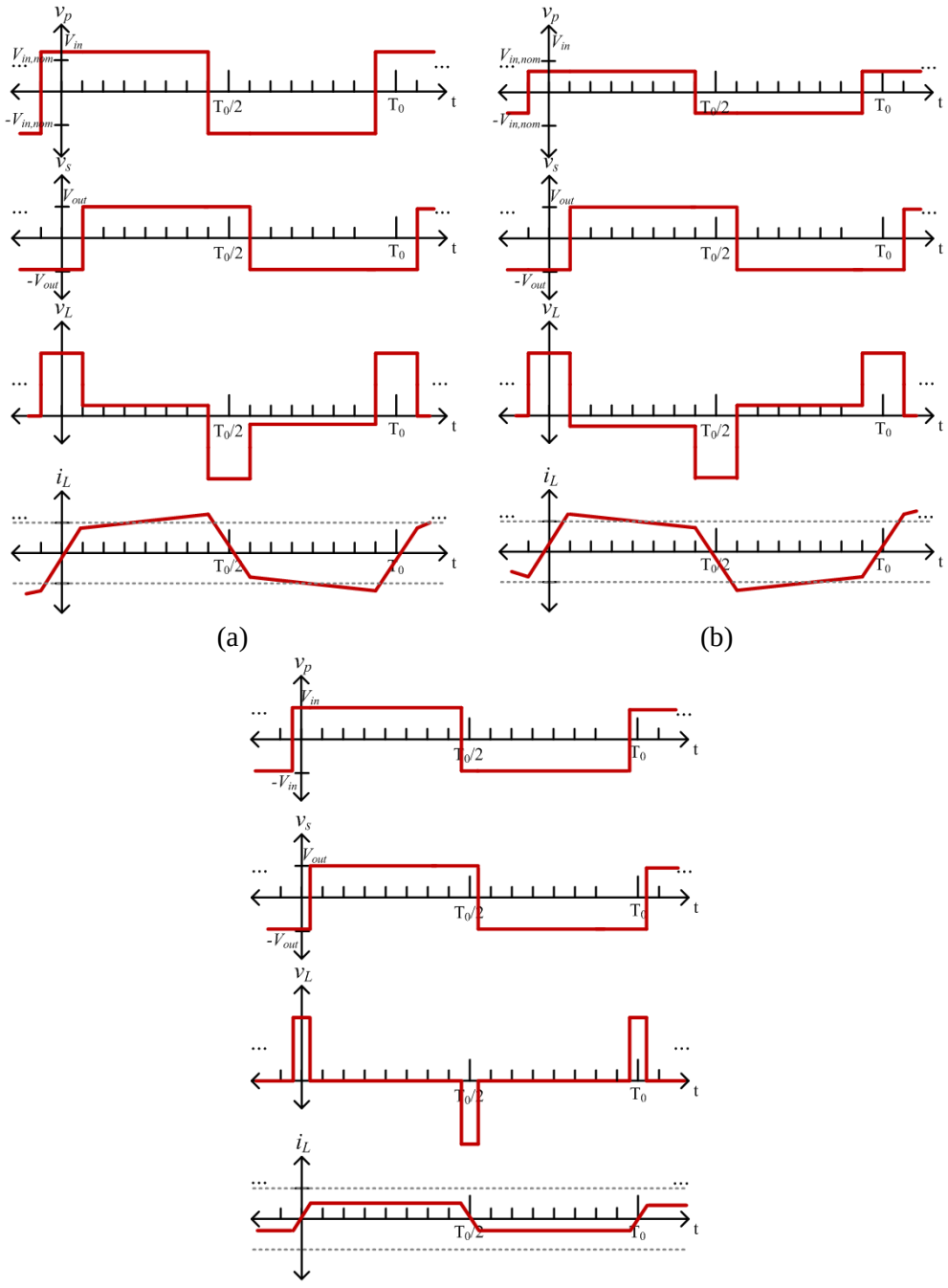


Figure 1-6: (a) Example operating waveforms of the DAB with an input voltage that is higher than the nominal input voltage (the voltage at which the input voltage divided by the output voltage is equal to the transformer turns ratio). Because the input-to-output voltage ratio is greater than the transformer turns ratio, the current no longer has a flat top. The grey dashed lines in the current plot represent the amount of current necessary to ensure ZVS on both the rectifier and inverter. In this example, the rectifier loses ZVS. (b) Example operating waveforms of the DAB with an input voltage that is lower than the nominal input voltage so that the input-to-output voltage ratio is lower than the transformer turns ratio. In this example, the inverter loses ZVS. (c) Example operating waveforms of the DAB operated with a low phase shift for low power. In this example, both the inverter and the rectifier lose ZVS.

degrade with increasing input voltage. The implementation focused on here naturally provides small variation in open-loop power across the input voltage conversion range. This particular work focuses on large-step-down applications (from high input voltages to small output voltages, such as needed for data center server power supplies); the only other (contemporaneous) work exploring ICN techniques [31,32,33,34] focused on isolated step-up conversion, which presents very different design considerations and limits. Output power variation can be modulated using burst mode to keep efficiency high because soft-switching can be maintained and magnetic core loss backs down with power. Another way to back down in power is through a technique called Variable Frequency Multiplier (VFX). In this thesis, VFX is applied to the inverter and rectifier stages to help modulate power but it can also be used on the inverter stage for wide input voltage operation as demonstrated in [35].

The second topology is that of a reconfigurable stacked active bridge converter which is optimized for extremely high efficiency across a very wide power range (including both at full power as well as under light-load conditions). Unlike traditional active bridge topologies, the topology presented in this thesis offers an inverter stage design that can dramatically improve device performance which significantly extends the range of powers over which high efficiency is achieved and offers a substantial reduction in losses at very low power. The unique transformation stage paired with a reconfigurable rectifier enable a low-power operating mode that provides soft-switching and reduced magnetic core loss at very low powers without the need for a complex control scheme. Additionally, the design techniques applied to the transformer result in a single integrated magnetic component that combines two transformers and two energy transfer inductances into one compact design, further improving efficiency and power density.

While this work focuses on a specification for high-step-down conversion from several hundred volts down to tens of volts, such as for data center power supply applications, the overall theory and individual techniques of either converter topology can be applied in numerous applications.

1.4 Thesis Organization

There are six chapters in this thesis. Following this introductory chapter, Chapter 2 introduces and develops in detail the theory of the Impedance Control Network (ICN) resonant converter as well as the design and operation of each of the individual inverter, transformation, and rectifier stages. To validate the theory, an experimental prototype is built and its design and selection of components is discussed thoroughly. Finally, voltage and current waveforms, efficiency, and performance of the prototype across a wide range of operating points are presented.

The general theory behind the Variable Frequency Multiplier (VFX) technique is discussed in Chapter 3. To demonstrate its operation, the VFX technique is applied to the inverter stage of the ICN

and its impact on the operation of the converter is analyzed. Simulated voltage and current waveforms of the ICN converter under VFX operation are shown to demonstrate the application of the theory.

Chapter 4 presents a second converter topology which uses a very similar inverter stage as the ICN converter of Chapter 2 but has a very different transformation stage and a modified rectifier stage. This chapter will contain a thorough discussion of the general design and modes of operation behind this reconfigurable double stacked active bridge converter. Chapter 5 will continue the presentation by including details on the design and construction of a prototype for the converter pursued as well as two other prototype boards used as benchmarks for comparisons in performance. Voltage and current waveforms demonstrating the operation as well as efficiency curves illustrating the benefits of the proposed design techniques are shown and discussed.

The thesis is concluded in Chapter 6, which presents a summary, conclusions and directions for future work.

Included in this thesis are multiple Appendices. Several MATLAB scripts that were used in the theory, implementation design and analysis of experimental data can be found in Appendix A. To aide in the design of the winding layer stack for the various planar magnetic components, a software tool co-developed by the author within the power electronics group at MIT called *M2Spice* was used. The geometry files that were used as inputs to this software tool are included in Appendix B. To understand how each circuit works, many LTSpice simulations were run. Appendix C has simulation schematics and information for many of the topology design variants explored in this thesis. The various prototype Gerber files for each printed circuit board (PCB) layer can be seen in Appendix D and an EAGLE layout schematic and a Bill of Materials (BOM) for each converter that was built and tested is located in Appendix E. All prototypes were run with an open-loop control. The parameters and settings for starting up and running the converter can be found in Appendix F.

Chapter 2

Impedance Control Network Resonant Converter

This thesis chapter describes the development of a new type of resonant power converter which we've termed an "Impedance Control Network" resonant converter. A conceptual block diagram of the proposed converter system architecture is shown in Figure 2-1. It incorporates multiple inverters and one or more rectifiers operated together under phase-shift control, along with a transformation stage incorporating an "Impedance Control Network" (ICN) as shown in Figure 2-1(a). The ICN operates to shape the operating waveforms under phase-shift control to maintain simultaneous zero-voltage switching (ZVS) and near zero-current switching (ZCS) of the transistors across the converter operating range (e.g., across input voltage), thereby minimizing stress and switching loss, which are valuable for achieving high efficiency and power density. This chapter will first discuss the inversion, transformation, and rectification stages in a general manner, covering the theory and operation of the ICN. It will then go into detail on how each of these stages is implemented for an experimental prototype. Finally, experimental waveforms and performance will be presented for a range of operating points.

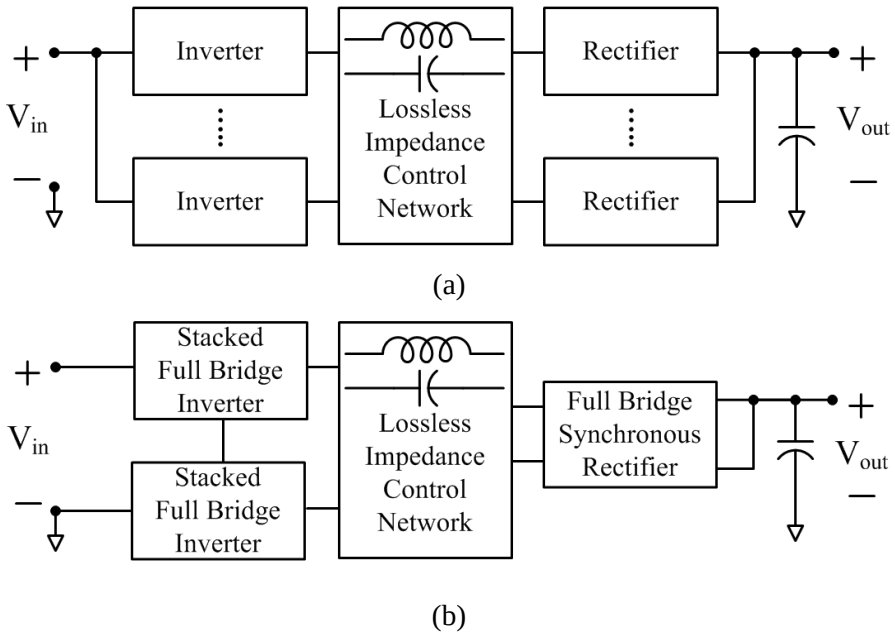


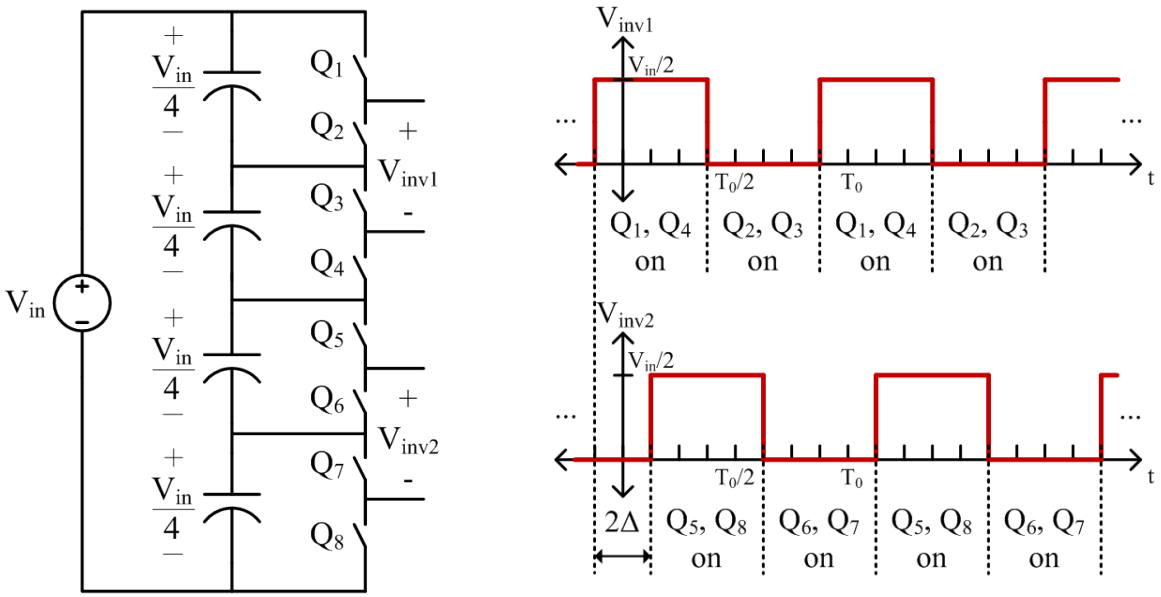
Figure 2-1: Architecture of the proposed Impedance Control Network (ICN) resonant converter in its (a) most general form, and (b) as pursued here. A plurality of phase-shifted inverters and one or more rectifiers interact through a lossless impedance control network that ensures desirable operating points for the inverter and rectifier blocks.

2.1 Theory of the Proposed Architecture

This thesis develops and implements an ICN architecture that targets high, wide-range input voltage and low, approximately constant output voltage. (While it is not explored in detail here, it is noted that wider-range output voltage could be addressed by incorporating a resistance compression network [36,37] into the impedance control network structure and utilizing multiple rectifiers.) To implement the proposed high-to-low voltage conversion system, we exploit an ICN-based architecture utilizing a "double stacked-bridge" inverter structure and a single full bridge synchronous rectifier as shown in Figure 2-1(b). Each of the subsystems of this particular converter is covered in the following subsections.

2.1.1 Double Stacked-Bridge Inverter

The inverter stage takes in the full dc input voltage and, in this topology, converts it to two separate high frequency ac voltages. The inverter structure chosen is that of a "double stacked-bridge" inverter system as illustrated in Figure 2-2(a). That is, we employ a stacked full bridge and stack that with a second stacked full bridge. Each of the two stacked-bridge inverters acts as one of the multiple inverters for the ICN system. Each half-bridge in the double stacked-bridge ideally sees only a quarter of the full input voltage (though there is some difference among the individual level voltages in practice). Under normal operation, each of the half-bridges is operated at the desired output frequency ($f_0 = 1/T_0$)



(a) (b)

Figure 2-2: (a) A double stacked-bridge inverter. The input voltage V_{in} is split into four (nominally equal) values with voltage balance maintained passively or through active control. The two stacked full bridge inverters deliver output voltages designated as V_{inv1} and V_{inv2} for the top and bottom inverter, respectively. (b) Operating switch waveforms to generate symmetric square waves for V_{inv1} and V_{inv2} with period T_0 and an example phase shift of 2Δ between inverters. The switch dead-times provided to enable ZVS and avoid shoot-through are not illustrated for simplicity.

and a 50% duty ratio (neglecting ZVS transition time). To generate a symmetric square waveform for the two inverter outputs, V_{inv1} and V_{inv2}, the bottom half-bridge of each stacked-bridge is delayed half a cycle, $\Delta t = 0.5 \cdot T_0$, from the top half-bridge. The relative phase shift, 2Δ, between the two generated square waves, V_{inv1} and V_{inv2}, is used as one of the major control handles in the system. More details of the inverter operating waveforms and switching pattern can be seen in Figure 2-2(b). This double stacked-bridge inverter structure enables synthesis of the desired operating waveforms while keeping individual device voltage ratings low compared to the (high) input voltage, which is valuable for achieving high efficiency.

2.1.2 Transformation Stage: Lossless Impedance Control Network

Interfacing the inverters and rectifier is the transformation stage, which uses a novel lossless impedance control network (ICN) and associated controls that allow ZVS and near ZCS to be maintained over a wide input voltage range. The ICN shares some of the features of the Chireix Power Combiner that is sometimes used in RF outphasing power amplifiers [38,39], but operates differently (and with different control behavior) owing to the effect of the input impedance characteristics of the rectifier and its use to maintain ZVS/near ZCS across the operating range. As will be seen, the ICN reactances are utilized to offset apparent loading reactances on each inverter owing to their interaction under phase-shift control.

Figure 2-3 shows the architecture employed for the ICN as well as the double stacked-bridge inverter previously mentioned. The output of each inverter is fed into the primary winding of a transformer. A series blocking capacitor, C_B, takes the dc component of the inverter voltage so that the voltage at the primary winding is centered around zero to avoid core saturation. The secondary winding of each transformer is connected to a series connection of reactive elements which are in turn coupled to the rectifier. These elements form the impedance control network, and their values are carefully selected. Each series combination of reactances serves two distinct purposes. First, they filter out harmonics such that the currents i_1 and i_2 in Figure 2-3 will be approximately sinusoidal with a frequency of f_0. Second, to achieve ZVS and near ZCS, the fundamental current must be approximately in phase with the voltage (with current lagging by only enough to ensure ZVS transitions, though we initially treat the case of making them exactly in phase). In order to achieve this, the value of the net reactance in the top branch and the value of the net reactance in the bottom branch of Figure 2-3 are selected to be equal in magnitude but opposite in sign (i.e., +jX and –jX) at the switching frequency.

To analyze the power transfer in this system, we consider power transfer through the fundamental components of voltage and current. To do so, the inverter outputs (as seen at the transformer secondaries where they are labeled as v_1 and v_2 of Figure 2-3) may be modeled by voltage sources representing the fundamental component of their output voltage, and the rectifier can be modeled as an equivalent resistor,

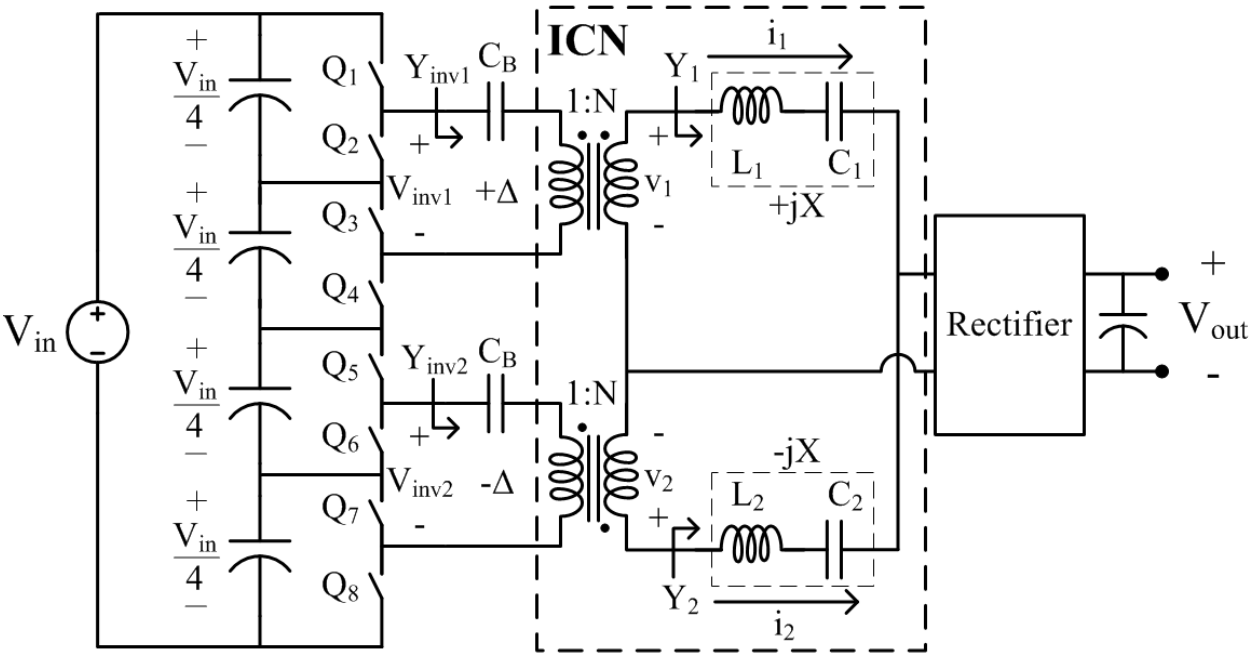


Figure 2-3: An ICN resonant converter comprising a pair of stacked bridges that are also stacked. The top inverter is phase-shifted by 2Δ ahead of the bottom inverter. The two series LC branches, L_1C_1 and L_2C_2, are selected to have equal and opposite reactances (i.e., +jX and –jX) at the switching frequency.

R, as shown in Figure 2-4 (where we note that the appropriate value of resistance depends upon operating point). Each voltage source and the current it contributes to each branch can be broken down and analyzed separately through superposition as demonstrated in Figure 2-5.

Let us denote the source voltages in phasor notation as:

$$\hat{V}_1 = Ve^{+j\Delta} \ , \tag{2.1}$$

$$\hat{V}_2 = Ve^{-j\Delta} \ , \tag{2.2}$$

where $\hat{V}_1$ and $\hat{V}_2$ are the source voltages that come from the top and bottom inverter after being scaled by the transformers, respectively. It is assumed that each source voltage has the same magnitude, V, and either a positive or negative angle, +Δ and – Δ. (Note: the phase angle is illustrated as being zero in Figure 2-5(c) and Figure 2-5(d).) Each source sees an impedance of:

$$Z_1 = jX + R||-jX = \frac{X^2}{R - jX} \ , \tag{2.3}$$

$$Z_2 = -jX + R||jX = \frac{X^2}{R + jX} \ . \tag{2.4}$$

From this, the currents that flow through the positive and negative reactive element from $\hat{V}_1$ can be calculated as:

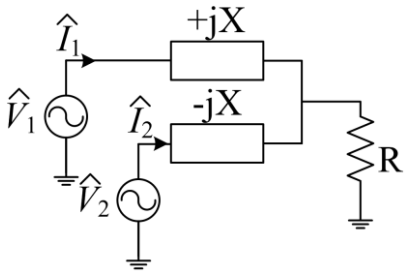


Figure 2-4: Simplified representation of the lossless ICN structure coupled with an equivalent resistive load.

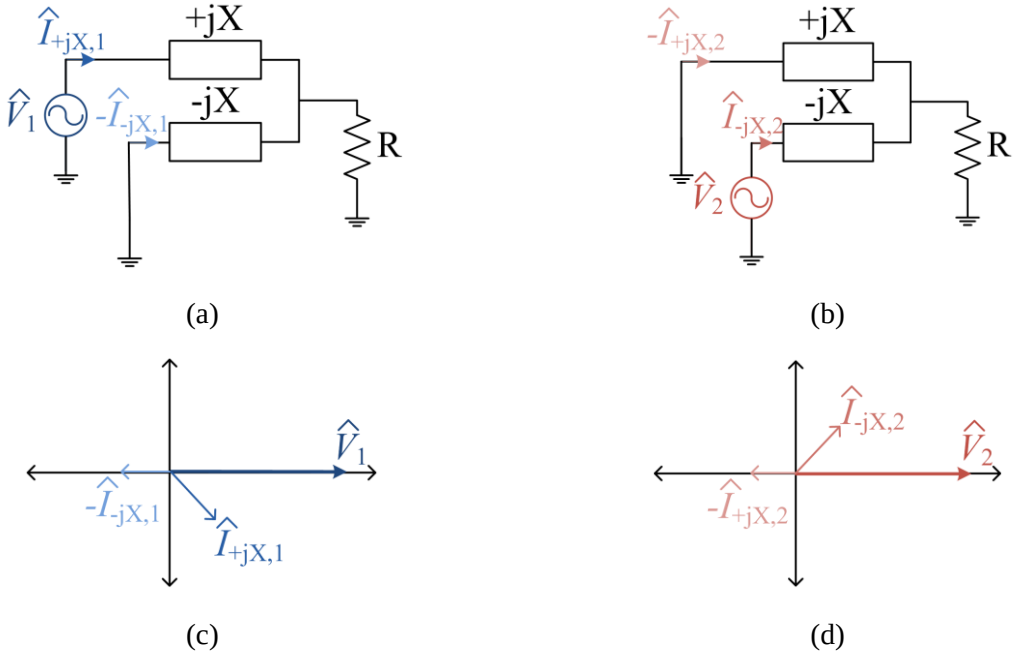


Figure 2-5: Superposition analysis of the ICN structure of Figure 2-4. By suppressing (a) V_2 and (b) V_1 independently, we can easily analyze the current flowing through each reactive component from (c) V_1 and (d) V_2 for a given set of reactance, X, and resistance, R.

$$\hat{I}_{+jX,1} = \frac{\hat{V}_1}{Z_1} = Ve^{+j\Delta}\frac{R - jX}{X^2}\ , \tag{2.5}$$

$$\hat{I}_{-jX,1} = \frac{R}{R - jX}\hat{I}_{+jX,1} = Ve^{+j\Delta}\frac{R}{X^2}\ , \tag{2.6}$$

and similarly through the negative and positive reactive element from $\hat{V}_2$:

$$\hat{I}_{-jX,2} = \frac{\hat{V}_2}{Z_2} = Ve^{-j\Delta}\frac{R + jX}{X^2}\ , \tag{2.7}$$

$$\hat{I}_{+jX,2} = \frac{R}{R + jX}\hat{I}_{-jX,2} = Ve^{-j\Delta}\frac{R}{X^2}\ . \tag{2.8}$$

Ultimately, the current that flows through $\hat{V}_1$ and $\hat{V}_2$ is a combination of the individual currents:

$$\hat{I}_1 = \hat{I}_{+jX,1} + -\hat{I}_{+jX,2} \ , \tag{2.9}$$

$$\hat{I}_1 = \frac{V}{X}\sin(\Delta) + j\left(\frac{2RV}{X^2}\sin(\Delta) - \frac{V}{X}\cos(\Delta)\right) \ , \tag{2.10}$$

$$\hat{I}_2 = -\hat{I}_{-jX,1} + \hat{I}_{-jX,2} \ , \tag{2.11}$$

$$\hat{I}_2 = \frac{V}{X}\sin(\Delta) - j\left(\frac{2RV}{X^2}\sin(\Delta) - \frac{V}{X}\cos(\Delta)\right). \tag{2.12}$$

For resistive loading of the sources, the angle of $\hat{I}_1$ and $\hat{I}_2$ should be Δ and $-\Delta$, respectively as shown in Figure 2-6. This is true when

$$\sin(2\Delta) = \frac{X}{R} \ . \tag{2.13}$$

Since (2.13) can be true for more than one angle and different values of X and R, consider the effective admittance seen by one of the sources:

$$\hat{Y}_1 = \frac{\hat{I}_1}{\hat{V}_1} = \frac{2R\sin^2(\Delta)}{X^2} + j\left(\frac{2R}{X^2}\sin(\Delta)\cos(\Delta) - \frac{1}{X}\right) \ . \tag{2.14}$$

(Note that here we define the "effective admittance" of the sources as that seen at one transformer output port with the other inverter active as shown in Figure 2-3.) At this point, the resistance, R, can be replaced with circuit parameters that are well-defined, such as the input voltage, V_{in}, the output voltage, V_{out}, and the transformer turns ratio, N. First, the power delivered by each source is:

$$P_1 = P_2 = \frac{1}{2}Re\{\hat{V}_1\hat{I}_1\} = \frac{V^2R}{X^2}\sin^2(\Delta) \ , \tag{2.15}$$

where in this case, V for the two stacked half-bridges is

$$V = \frac{NV_{in}}{\pi} \ . \tag{2.16}$$

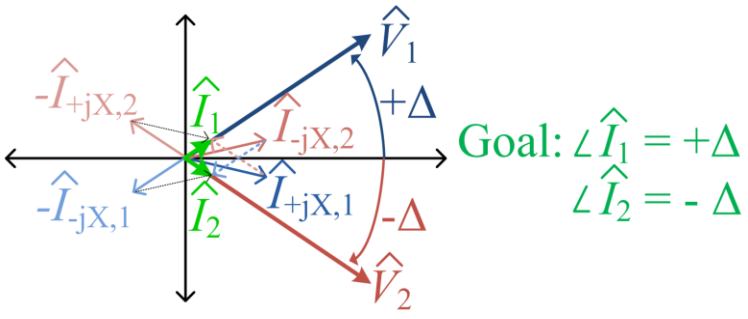


Figure 2-6: Superposition of currents and voltages in the ICN. With a specific phase shift between source voltages, the source currents can be in phase with the voltages, thereby providing resistive loading and improved efficiency.

Furthermore, a full bridge rectifier switched in phase with the drive current can be modeled with an equivalent resistance [19]:

$$R = \frac{8V_{out}^2}{\pi^2 P_{out}} \ . \tag{2.17}$$

Using conservation of power, the equivalent resistance can be rewritten as:

$$R = \frac{2V_{out}X}{NV_{in}\sin(\Delta)} \ . \tag{2.18}$$

Combining these equations, the effective admittances seen by the two inverters (Y_{inv1} and Y_{inv2}) can be expressed as:

$$\hat{Y}_{inv1} = \hat{Y}_{inv2}^{*} = \frac{4V_{\text{out}}\sin\Delta}{NV_{\text{in}}X} + j\left(\frac{4V_{\text{out}}\cos\Delta}{NV_{\text{in}}X} - \frac{1}{X}\right) \ . \tag{2.19}$$

Here, by "effective admittance" of the inverters we mean the ac current to voltage ratio at each inverter output, V_{inv1} and V_{inv2}, with both inverters active as labeled in Figure 2-3.

With this design, the effective susceptance seen by the two inverters can be made zero or arbitrarily small when the two inverters are operated with a specific phase shift between them, as shown in Figure 2-7. The phase shift at which the susceptance seen by the inverters becomes zero can be written as a function of the input-output voltage conversion ratio:

$$\Delta = \cos^{-1}\left(\frac{NV_{\text{in}}}{4V_{\text{out}}}\right) \ . \tag{2.20}$$

Hence, by varying this phase shift as the input voltage varies, the admittance seen by the inverters can be kept purely conductive across the full input voltage operating range of the dc-dc converter (i.e., inverter currents remaining in phase with inverter voltages). Adjusting frequency, impedance slightly, or by adding an inductive preload to the inverter (e.g., [40]) to provide a modest inductive loading component for ZVS transitions, this allows the inverter switches to have simultaneous ZVS and near ZCS capability across the range of voltage conversion ratios, thus reducing switching losses and boosting converter efficiency.

When operated in the manner described, one can achieve good operation over a wide range of voltage conversion ratios. At a given switching frequency, the output power of an inverter loaded with a fixed resistor is proportional to the square of the input voltage and the conductance seen by the inverter. In conventional designs, this can often lead to large variations in power delivery with input voltage that must be addressed (e.g., by oversizing the inverter components and/or using frequency or burst control to modulate power). However, since the effective conductance seen by the inverters in this system decreases with increasing voltage (see Figure 2-7), the variation in output power can be limited to a narrow range across a wide input voltage range. This enables improved sizing of inverter components and

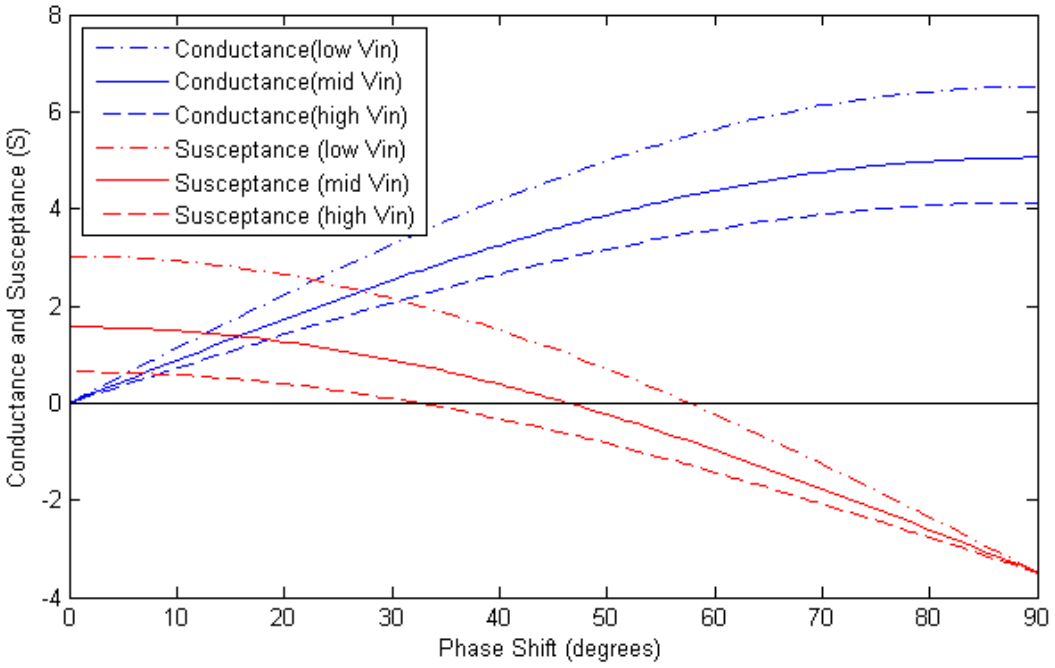


Figure 2-7: Effective conductance and susceptance from (2.19) seen by the two inverters in Figure 2-3 (at ports defined by V_{inv1} and V_{inv2}) as a function of their relative phase shift for example low, medium, and high dc input voltage values: 260V, 335V and 410V. For these plots, V_{out} is 12V, N is 0.1, and X is 0.2639Ω. Both inverters see the same conductance, but one sees the negative of the susceptance shown above.

use of fixed-frequency operation, with consequent benefits for efficiency. By combining (2.15), (2.16), (2.18), and (2.20) and applying trigonometric manipulations, the output power can be expressed as:

$$P_{out} = \frac{NV_{\text{in}}\sqrt{16V_{\text{out}}^2 - N^2V_{\text{in}}^2}}{\pi^2 X} \ . \tag{2.21}$$

Given the variation in output power with input voltage in (2.21), the variation can be minimized if the converter is designed to deliver the same output power at its minimum and maximum input voltages, $V_{\text{in,min}}$ and $V_{\text{in,max}}$, respectively as illustrated in Figure 2-8. This design methodology can be mathematically expressed as:

$$P_{out}(V_{\text{in,min}}) = P_{out}(V_{\text{in,max}}) = P_{out,\text{rated}} \ . \tag{2.22}$$

The system of equations given by (2.22) can be used to determine the following closed-form analytical expressions for the transformer turns ratio N and the reactance X:

$$N = \frac{4V_{\text{out}}}{\sqrt{V_{\text{in,min}}^2 + V_{\text{in,max}}^2}} \ , \tag{2.23}$$

$$X = \frac{NV_{\text{in,min}}\sqrt{16V_{\text{out}}^2 - N^2V_{\text{in,min}}^2}}{\pi^2 P_{out,\text{rated}}} \,. \tag{2.24}$$

A plot of the theoretical output power of (2.21) using (2.23) and (2.24) with V_{out} of 12 V, $V_{\text{in,min}}$ of 260V, $V_{\text{in,max}}$ of 410V, and $P_{out,\text{rated}}$ of 400W is shown in Figure 2-9. It can be seen that for a 1.6:1 input voltage range, the maximum output power is only about 10% greater than the designed rated output power. (This compares to ~150% increase over designed rated power for a single inverter running across a similar voltage range into a fixed resistor.) The output power of the converter can be further controlled to values below those in Figure 2-8 using a other methods, such as burst (on/off) control strategy in which the operation of the converter is modulated on and off at a frequency much lower than its switching frequency [41,42,43,44,45,46,47]. There are multiple ways burst mode can be realized. One way is that

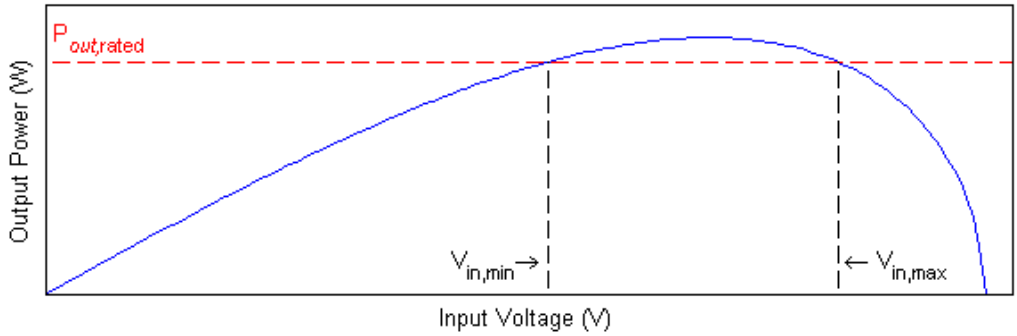


Figure 2-8: The output power of (2.21) as a function of input voltage for the topology implementation of Figure 2-3. For these plots, V_{in} ranges from 0 V to 500 V, V_{out} is 12V, N is 0.1, and X is 0.2639Ω. In order to minimize variance in output power across the input voltage range while guaranteeing a specified power capability, the rated output power should be achieved at the minimum and maximum input voltages as illustrated by the dashed lines.

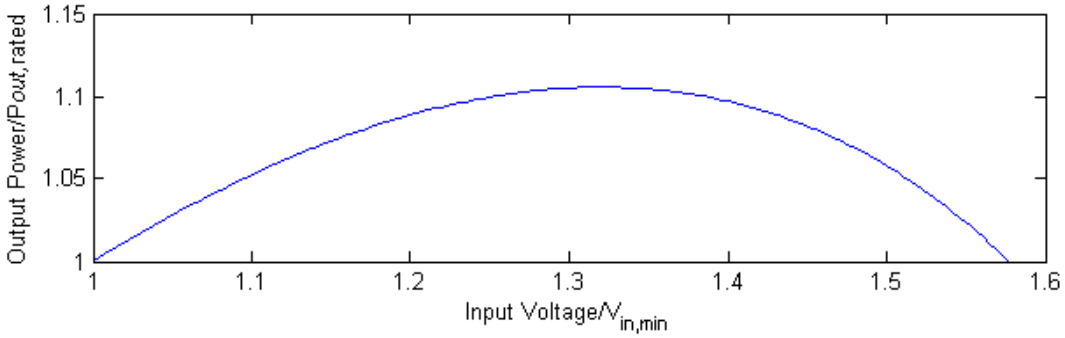


Figure 2-9: Variation in output power as a function of input voltage for the ICN converter operated with the phase-shift between two inverters controlled to provide zero effective susceptance of the inverters. With the design parameters of (2.23) and (2.24), converter power varies only minimally (~10%) over the designed output power, $P_{out,\text{rated}}$, of 400 W even though the input voltage increases almost 60% from its minimum value (i.e., V_{in} = 260 V – 410 V at V_{out} =12V).

the converter can be turned on and off at a fixed frequency but the on-time duty ratio would vary as the output power varies as a percentage of the rated output power [43]. Another method is to let the frequency (and duty ratio) vary as the converter tries to maintain a parameter, such as output voltage, within a defined hysteresis band or tolerated values (e.g., [41,42,44,45,46,47]). On/Off control is desirable because converter losses back off proportionally to power delivered, thus enabling efficient operation to be maintained over a wide power range.

2.1.3 Rectification Stage

The final stage of this converter takes in the alternating current and converts it to a constant current that is delivered to the dc load through the means of a full bridge rectifier. Such rectifiers can be implemented with a diode bridge as shown in Figure 2-10(a), or with other diode-based rectifiers such as half-bridge/voltage doubler rectifier, diode-based current-doubler rectifier, or diode-based resonant rectifier (e.g., [48,49]). However at such low output voltages and high output currents, device loss due to the forward voltage drop of one or more diodes would drastically affect the performance and reduce efficiency. Therefore, synchronous rectification, in which resistive FET forward drops take the place of diode drops, is strongly preferred. For the specific design treated here, we utilize a synchronous full bridge rectifier (Figure 2-10(b)) which is used and controlled to act as a diode bridge rectifier (i.e., with switching of the active switches in phase with the current, as with a diode rectifier). To further reduce conduction loss and spread out thermal rise presented by the high output current, devices can be placed in parallel (Figure 2-10(c)) at the expense of increased gating loss.

Because a full bridge rectifier is used, the center nodes of each half-bridge will either be at V_{out} or at ground. At the switch transition, this will cause a sharp dv/dt. To prevent unwanted harmonic injection from the rectifier to the rest of the circuit, one or more resonant tanks can be used for filtering.

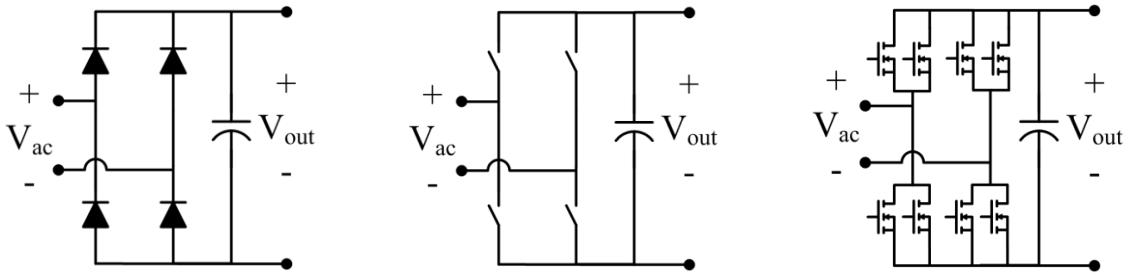
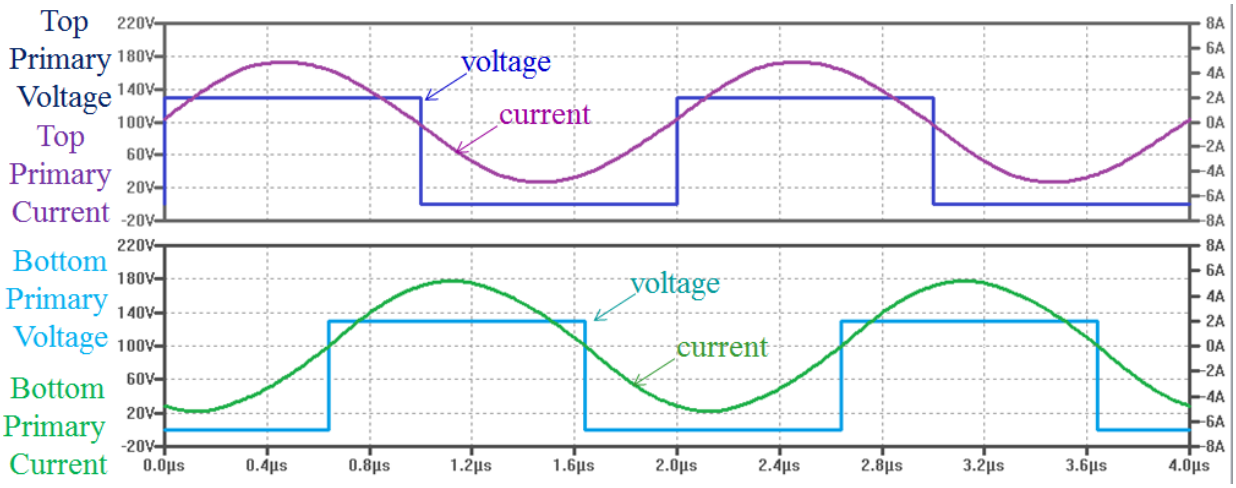


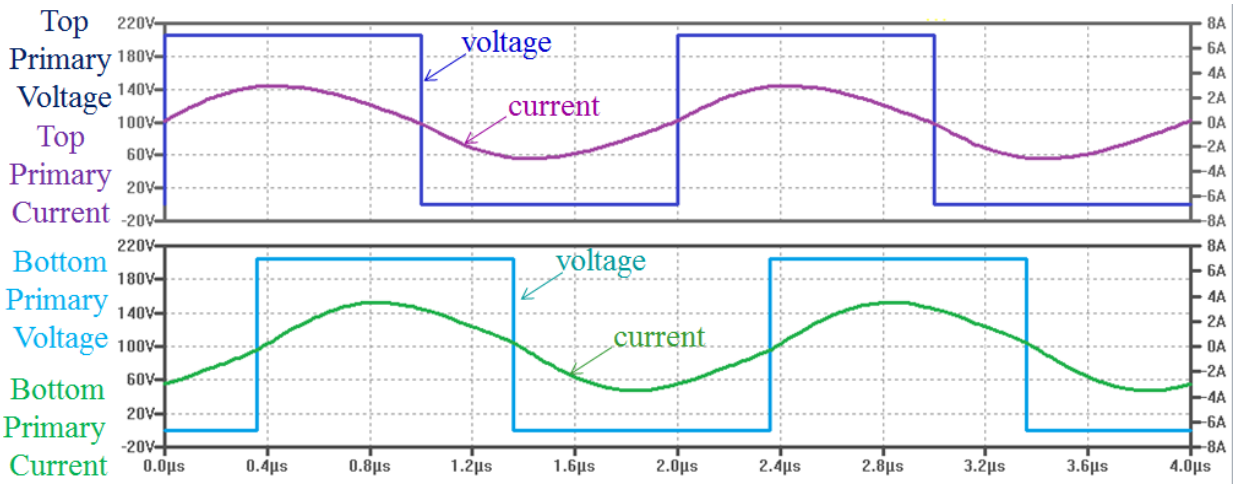
Figure 2-10: Three variants of a full bridge rectifier using (a) diodes, (b) active devices, and (c) paralleled FETs used to implement the switches.

2.1.4 Simulation of the Proposed Architecture

Extensive simulation was done before a prototype was built in order to gain insight into the theory assuming lossless ideal circuit components. An early simulation result using the theoretical phase shift across input voltage and series resonant tanks with a quality factor around 4 at the output of each transformer and before the rectifier is shown in Figure 2-11. The details of the simulation can be found in Appendix C. For all waveforms, the current is sinusoidal and in phase with the voltage. However, a real circuit will have several parasitic mechanisms that affect the operation. A simulation incorporating some common parasitics (e.g., switch parasitics, component resistances, core loss) was used to evaluate



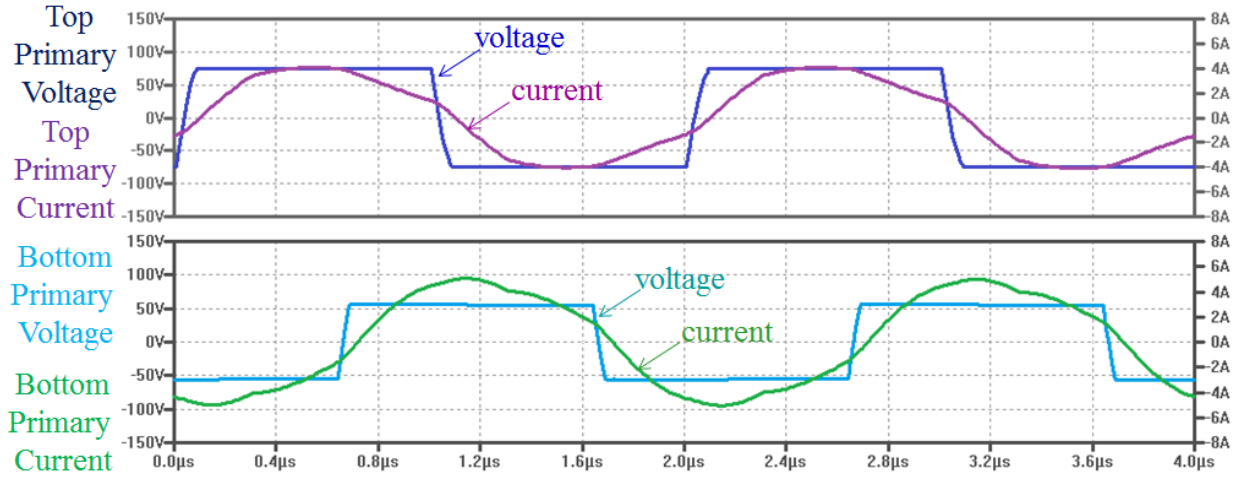
(a)



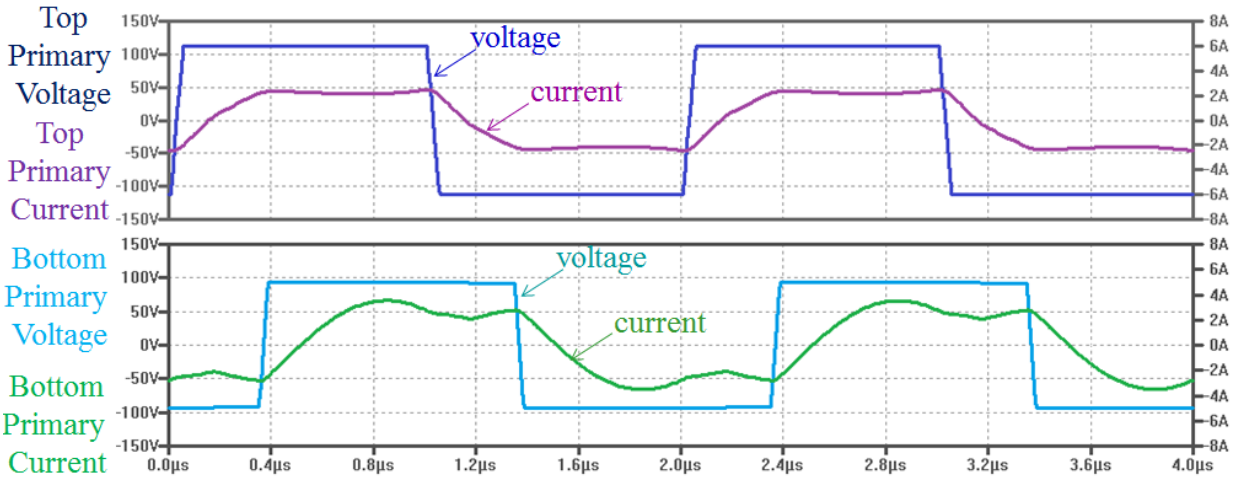
(b)

Figure 2-11: Early simulation results showing ZVS and ZCS of a lossless ICN resonant converter with an input voltage of (a) 260 V and (b) 410 V. The output voltage was 12 V, and the output power was 400 W. For all plots, the top pane shows the primary voltage and current for the top transformer and the bottom pane shows the primary voltage and current for the bottom transformer. For all plots, the current is sinusoidal and crosses zero almost simultaneously with the square wave voltage transitions.

practical components for implementation. Some examples of things that were determined through simulation before the construction of the prototype are the need for a resonant tank on the rectifier, the amount of magnetizing inductance on the transformer necessary to ensure ZVS across the full input voltage range, and the quality factor of the resonant tanks. Some non-ideal behaviors in the waveforms such as voltage amplitudes and harmonic content of transformer currents were observed in simulation as shown in Figure 2-12. This turned out to match very well to the performance on the bench. Given the relative accuracy of the simulation, it was later used to help model and quantify loss parasitics given certain experimental measurements. Details on the final version of the simulation are in Appendix C.



(a)



(b)

Figure 2-12: Early simulation results showing ZVS and ZCS of a more practical ICN resonant converter with an input voltage of (a) 260 V and (b) 410 V. The output voltage was 12 V, and the output power was 400 W. For all plots, the top pane shows the primary voltage and current for the top transformer and the bottom pane shows the primary voltage and current for the bottom transformer.

2.2 Experimental Implementation

A prototype converter was developed to experimentally validate the theory of the ICN converter presented in the previous section. Figure 2-13 shows the design of a prototype converter implementing the proposed approach. The components used and their values are summarized in Table 2-1 and the converter specifications are listed in Table 2-2. (A complete schematic and bill of materials is shown in Appendix E and printed circuit board layouts are shown in Appendix D.) The output power rating is listed as 350 W to account for losses and nonidealities in the circuit but calculations for components is done with an idealized output power rating of 400 W.

2.2.1 Switching Devices

To achieve high efficiency, active switches are used for the inverters and the rectifier. With a regular full bridge inverter, the inverter switches would have to be capable of blocking the full input voltage, which is 410 V in this design, plus safety margins. As mentioned previously, the double stacked-bridge inverter allows us to used devices that have much lower voltage ratings. This topology could possibly use 150V devices with adequate safety margin, however 200V devices were chosen to provide significant design margin. As an alternative to silicon (Si), gallium nitride (GaN) is an emerging material for power devices which offers lower gate capacitance and on-resistance for a given voltage rating [50]. Furthermore, the devices produced by Efficient Power Conversion (EPC) are not packaged, allowing for a much smaller volume when compared to conventional devices and packages, with consequent benefits for

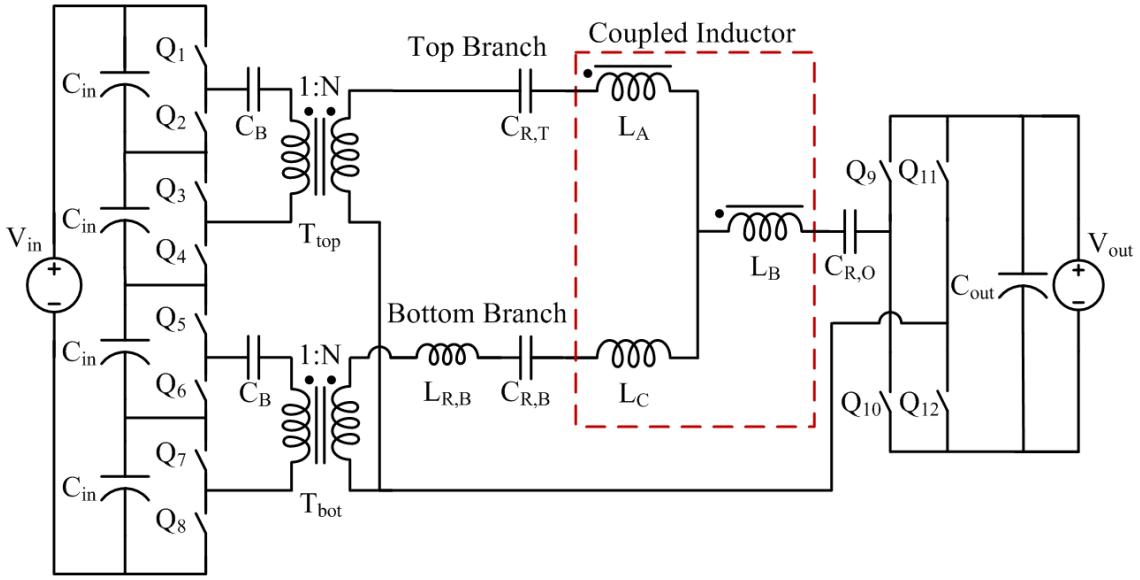


Figure 2-13: Proposed implementation of the ICN converter. The ICN incorporates harmonic filtering through the use of resonant tanks as well as two equal but opposite impedances. This structure contains four magnetic structures - two transformers, a coupled inductor (indicated by the red-dashed box), and a resonant inductor.

Table 2-1: Components for Prototype Converter

Component	Description		Value
Q_1-Q_8	EPC2010 200V/12A eGaN® FETs		-
Q_9-Q_{12}	2 parallel EPC2023 30V/60A eGaN® FETs		-
C_B	TDK 250V X7T ceramic		6.6 µF
N	10 turn primary, 1 turn secondary		0.1
T_{top}	EPCOS EILP43-N49 core 8 layer, 4 oz PCB winding with one layer of		42 µH[a]
T_{bot}	5 mil foil on top		
$C_{R,T}$	TDK 50V X7R ceramic		varies[b]
$L_{R,B}$	EPCOS EIR23-N49 core, 4 layer, 4 oz, 1-turn PCB winding		125 nH
$C_{R,B}$	TDK 50V NP0 ceramic TDK 50V C0G ceramic		30 nF paralleled w/ 600 nF
L_A	EPCOS EILP18-N49 core 4 layer, 4 oz PCB winding	1 turn	45nH
L_B		1 turn	45 nH
L_C		-	-22.5nH
$C_{R,O}$	TDK 50V NP0 ceramic		1.13 µF
C_{in}	TDK 250V X7T ceramic Nichicon 200V electrolytic		7.6 µF paralleled w/ 56 µF
C_{out}	TDK 16V X7S ceramic TDK 35V X7R ceramic United Chemi-Con 16V electrolytic		100 µF x 10 paralleled w/ 10 µF x 24 paralleled w/ 1000 µF x 10

[a] magnetizing inductance seen from primary

[b] this capacitance is tuned to match the actual impedance seen in L_A

Table 2-2: Converter Specifications

Parameter	Description	Value
V_{in}	Nominal Input Voltage	380 V
	Input voltage range	260 V- 410 V
V_{out}	Output voltage	12 V
P_{out}	Output power rating	350W
f_{sw}	Switching frequency	500 kHz

interconnect parasitics. Initially, only a few types of EPC GaN power devices were commercially available and their maximum voltage rating was 200 V. Therefore, this topology presented us with an opportunity to use GaN-based FETs for the inverter stage in order to increase efficiency.

The inverter switches are realized with EPC2010 GaN-on-Si switches. Although the inverter stage is comprised of four stacked half-bridges and a half-bridge driver for GaN FETs exists (TI LM5113), it can only sustain up to 100 V on the switch node, which is just below the range required for this converter. (A subsequent driver is under development at the time of writing that would provide much larger level shifting voltages.) Therefore, each individual inverter GaN FET is controlled with TI LM5114 drivers with the high-side driver bootstrapped.

The rectifier is a synchronous full bridge realized with EPC2023 GaN switches. In order to increase efficiency, each half-bridge in the full bridge rectifier comprises two parallel half-bridges. Since the total voltage across each half-bridge is only 12 V, each half-bridge can be controlled with TI LM5113 drivers.

All drivers are powered and controlled from a control board developed by David Otten of MIT and pictured in Figure 2-14 [51]. The controller is a general purpose gate drive board that can provide isolated gate signals for up to 9 half-bridge circuits, 4 of which are used for the inverter stage and 4 of which are used for the rectifier stage. Due to the stacked nature of this converter, each half-bridge is provided with an isolated 1 watt power supply to run the gate driver. A schematic showing the isolation and power circuitry for one half-bridge channel is illustrated in Figure 2-15.

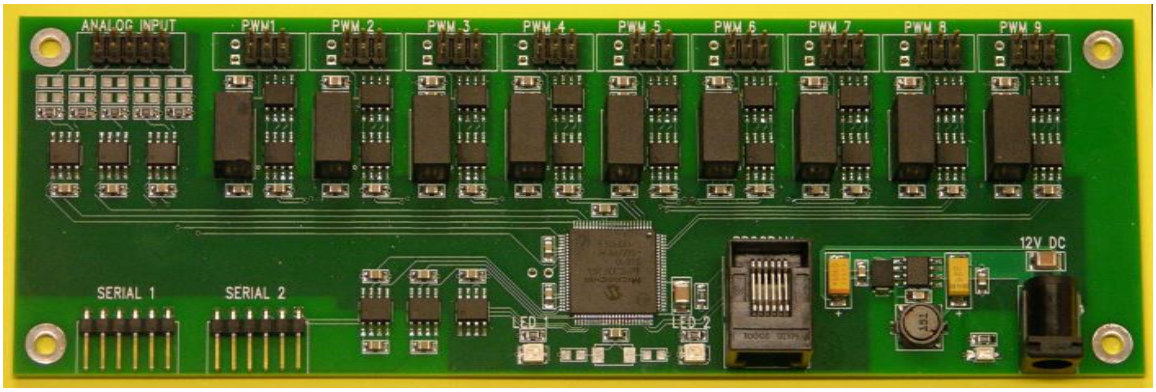


Figure 2-14: Front View of the ICN Controller.

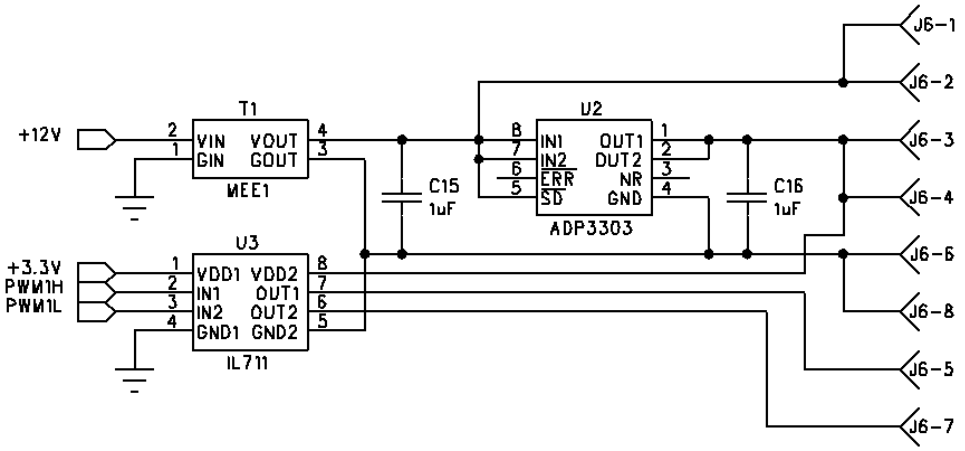


Figure 2-15: Schematic showing the isolation and power circuitry for one half-bridge channel [51]. In this particular schematic, isolated gate drive power is supplied by a muRata MEE1 Series 1W isolated DC/DC converter that delivers an unregulated 9 V to the main converter board. That 9 V is also regulated to 5 V using an Analog Devices ADP3303 low dropout linear regulator, which is delivered to the main board. To provide isolation, the gate drive signals are routed through a NVE Corporations IL711 two-channel digital isolator before going to the main converter board.

2.2.2 Transformer Design

The two transformers employed in the circuit of Figure 2-13 are identical. Using an output voltage of 12 V, a minimum input voltage of 260 V, and a maximum input voltage of 410 V, the turns ratio as determined by (2.23) is 0.099 (approximately, 0.1, practically implemented with a 10-turn primary and 1-turn secondary). Each transformer is designed to conduct a maximum of 4 A_{RMS} in the 10-turn primary winding and 40 A_{RMS} in the 1-turn secondary winding. The primary winding can see a voltage above 100 V and each transformer will process roughly 200 W of power.

Planar magnetic components have become attractive in recent years for a variety of reasons. [52] gives an excellent overview of planar magnetic technology and some of its key advantages. In summary of [52], low profile cores can be used leading to increased power density and a higher surface area to volume ratio for better heat dissipation. Since printed circuit board (PCB) technology can be used, there is increased manufacturability and repeatability. This also makes modeling and prediction of characteristics more accurate. Additionally, the windings can be integrated into the same board as the rest of a power electronic circuit reducing interconnect loss. Finally, the design of planar magnetic windings on a PCB can be more complicated but it also allows for interleaving which can significantly reduce leakage inductance as well as skin and proximity effects.

Despite all the advantages listed above, there are some undesirable characteristics also mentioned in [52]. Especially with E cores, the windings will extend outside the core footprint, thereby increasing the total surface area of the component. Furthermore, the wide winding width of the turns along with the short distance between layers will lead to much higher winding capacitances when compared to traditional wire-wound components. These challenges are non-trivial and can drastically affect the operation of the circuit if ignored.

To attain the benefits of planar magnetics, the transformer windings are implemented in a printed circuit board (PCB). Given the high turns ratio and secondary current, multiple layers are needed; the configuration of the layers is quite important as discussed in [53,54,55,56]. To minimize winding resistance as a result of skin and proximity effect (i.e., current only traveling on the surface of a conductor and one conductor's fields inducing eddy currents in other conductors), it is widely understood that a fully interleaved structure is optimal. To help aid in understanding the number of layers that should be employed in the winding layer stack, a software tool – *M2Spice* – that can rapidly compute the element values, and automatically generate a SPICE netlist was used. This tool is based off a modular layer model presented in [56] and is open-sourced[1]. The magnetic geometry information is first processed by *M2Spice*, which produces a netlist for a subcircuit that captures the electrical behavior of the magnetic component. This netlist is combined with a netlist that represents other elements in the circuit (e.g., capacitors,

[1] *M2Spice* [Online]. Available: http://www.rle.mit.edu/per/M2Spice/

resistors, switching devices, etc.) and fed into a SPICE simulation platform (e.g., LTSpice). Based on the simulated circuit performance, designers can very quickly adjust the geometry of the magnetic component (e.g., layer thickness, interleaving patterns, core shapes, etc.), and iterate the design. It should be noted that *M2Spice* is not used to precisely calculate the winding loss, but it can be used to generally compare designs.

To reduce the number of design iterations, *M2Spice* was used for only one core size. Therefore, a primary sweep of various core materials and shapes was done first in order to determine the best material to reduce core loss for 500 kHz operation and best shape to reduce approximate winding loss. It was determined that N49 had the best performance of tested materials. N49 core loss is compared to other materials in Figure 2-16 [57,58,59]. A MATLAB script was then generated to investigate the performance of various core shapes offered that use N49 (See Appendix A). Available planar core shapes include low profile RM cores, ER cores and low profile E cores. ER cores tend to yield lower winding loss and lower leakage but E cores have a higher cross sectional area for magnetic flux for a given "box volume". This script calculated both core loss and winding loss. It was observed that a majority of the loss was found in the windings due to the high secondary current and the resistance limitations owing to skin depth effects. This would necessitate the paralleling of secondary layers and the importance of reducing loss due to proximity effect. Based on these considerations, it was decided that an EILP43 core set would be used for each transformer.

Knowing the core geometry, *M2Spice* was used to determine the optimal winding layer stack. Several variations were simulated and the losses predicted by SPICE are listed in Table 2-3 (See Appendix B for *M2Spice* geometry files). Increasing the layer count from 4 to 8 gives substantial reduction in predicted loss (>40%). However, only marginal improvements were found when the layer

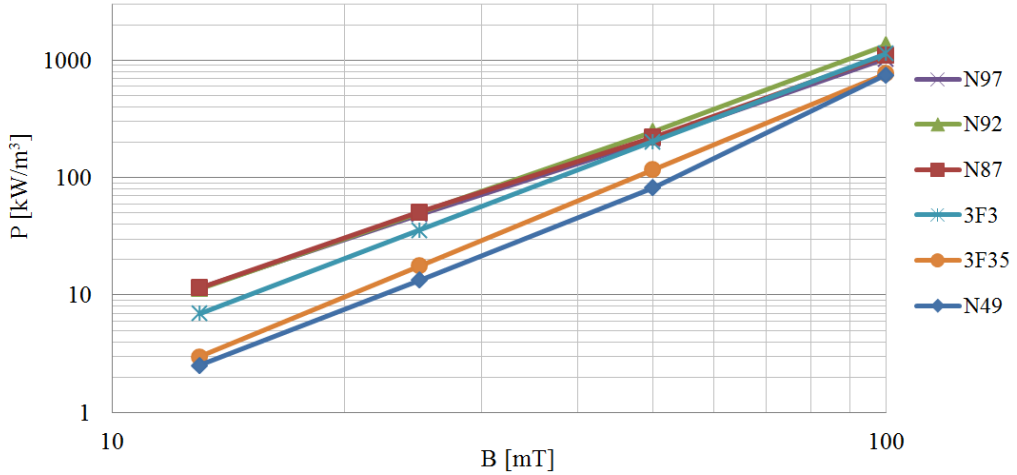


Figure 2-16: Magnetic core loss per volume as a function of magnetic flux density for several materials operated at 500 kHz and assuming a temperature of 100 °C [57,58,59]

Table 2-3: SPICE simulation predicted loss for various transformer interleaving patterns, assuming the use of 4 oz. weight copper. P: primary layer with 5 series connected turns; S: secondary layer with 1 single turn. "PSPS" represents a four layer interleaving pattern: the 1st and 3rd layers are two primary layers with 5 turns, the 2nd and 4th layers are two secondary layers with 1 turn. The 1st layer is the topmost layer and closest to the I core.

Layer Stack	SPICE Predicted Loss	
	260 V_{in}	**410 V_{in}**
SSPP	6.8846 W	3.8068 W
PPSS	6.9307 W	3.7261 W
SPPS	4.7508 W	2.9148 W
PSSP	4.7524 W	2.8963 W
SPSP	4.6187 W	2.8678 W
PSPS	4.6439 W	2.8465 W
SSPPSSPP	3.0320 W	2.2267 W
PPSSPPSS	3.0516 W	2.1986 W
PSSPPSSP	2.5920 W	2.0331 W
SPPSSPPS	2.5863 W	2.0291 W
SPSPSPSP	2.4138 W	1.9593 W
PSPSPSPS	2.4260 W	1.9548 W
PSPSPSPSPSPSPSPS	1.5206 W	1.8011 W
SPSPSPSPSPSPSPSP	1.4689 W	1.7934 W

count increased beyond 8, which was verified in [60]. 2D and 3D effects are not incorporated into *M2Spice* and very high layer counts could suffer drastically. Higher layer counts also incur cost penalties. For these reasons the transformer layer count was chosen as 8. Table 2-3 also shows that a fully interleaved structure has lower losses when compared to a non-interleaved structure owing to reductions in proximity effect. Therefore, the PCB stackup has the primary turns and the secondary turns alternating layers as shown in Figure 2-17. This pattern also reduces leakage inductance. It was not a design goal to minimize leakage inductance (since it can be used for harmonic filtering); rather an interleaved configuration is selected to minimize the ac resistance.

In practice, the winding losses are higher than what *M2Spice* predicts owing to 2D and 3D effects. For extra conductance while maintaining interleaving, a 5-mil foil wrapped in kaptop tape for insulation was cut in the same shape as the PCB secondary winding and was added above the PCB (resulting in effectively a 9-layer structure, with the secondary on both top – as foil – and on the bottom). *M2Spice* predicts that this arrangement will have a predicted loss of 2.3151 W at 260 V_{in} and 1.9709 W at 410 V_{in}, which are comparable to the losses of the 8 layer PCB winding stack without any additional foil windings.

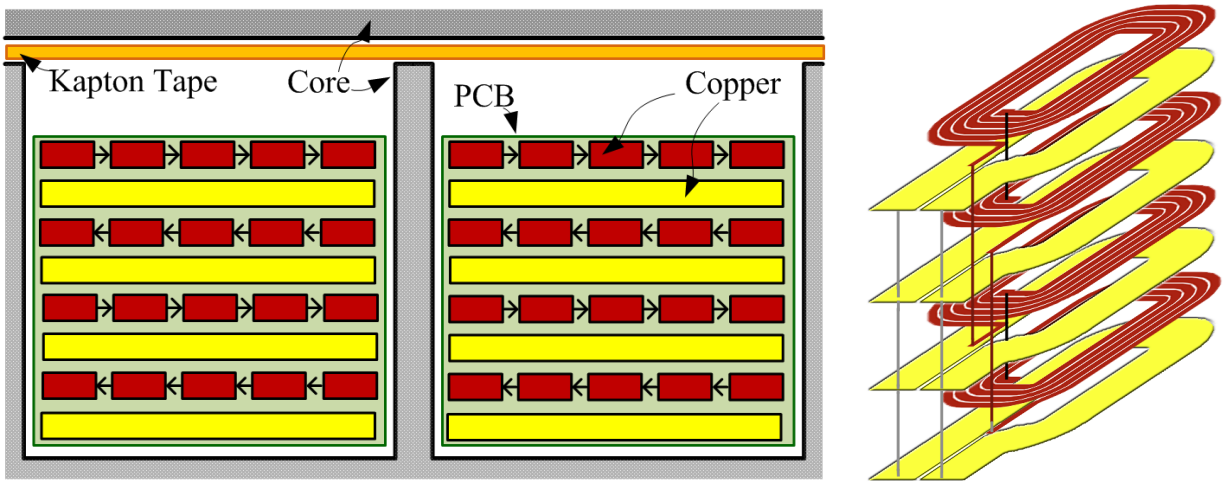
The choice of copper thickness depends heavily on frequency and the level of interleaving. From Dowell's equation and approximating the waveforms to be sinusoidal, the optimal ratio of layer thickness to skin depth is given in [61] to be:

$$\Delta_{opt} = \left(\frac{15}{5p^2 - 1}\right)^{1/4} \tag{2.25}$$

where p is the number of consecutive layers of a primary or secondary winding. The winding structure we consider will have fully interleaved windings such that only one consecutive layer of primary exists followed by only one consecutive layer of secondary (i.e., a p of 1). The optimal ratio is calculated to be 1.39 so the thickness of the winding should be 1.39 times the skin depth at the operating frequency. The general equation for skin depth is

$$\delta = \sqrt{\frac{2}{2\pi f \mu \sigma}} \tag{2.26}$$

where f is the fundamental frequency, μ is the permeability, and σ is the conductivity at the operating temperature.



(a) (b)

Figure 2-17: PCB winding structure for the transformer showing both (a) a cross sectional view and (b) a 3D view. The 3D view shows the interconnection between the layers. The 1st and 3rd layer form one series connected primary winding and the 5th and 7th layer form a second series connected winding. Both primary windings are then connected in parallel. All even layers comprise the secondary winding and are connected in parallel. (The foil secondary winding is not shown.) The core used is an EPCOS EILP43 using N49 material and a gap of ~0.75 mm is created using kapton tape.

Table 2-4: Skin depth variable values

Variable	Description	Value
f	Fundamental frequency (Hz)	500 000
μ_0	Permeability of free space ($H \cdot m^{-1}$)	$4\pi \times 10^{-7}$
μ_{Cu}	Permeability of copper ($H \cdot m^{-1}$)	$\approx 1.2566 \times 10^{-6}$
$\sigma_{Cu\text{-}20}$	Conductivity of copper at 20 °C (S/m)	5.96×10^{7}
$\sigma_{Cu\text{-}100}$	Conductivity of copper at 100 °C (S/m)	4.35×10^{7}

Table 2-4 shows various values for these variables. The skin depth of 100 °C copper at 500 kHz is approximately 108 μm. The choice of 4 oz copper (140 μm thickness) will be roughly optimal (i.e., yield the lowest ac loss) for a frequency of 500 kHz and fully interleaved winding structure. This copper thickness is also what was used to generate the loss values of Table 2-3. Given the dimensions of the EILP43 core set, a finished thickness of 62 mils was chosen in order to avoid any fringing effects from the air gap between the core halves [62,63] although in actuality a 70 mil board was the thinnest that could be manufactured for such a high layer count and thickness (A detailed PCB layout and nominal board stackup for the transformer windings is shown in Appendix D).

A gap of approximately 0.75 mm is inserted between the two core halves using kapton tape. This gap is used to lower the magnetizing inductance which will provide a magnetizing current for use in ZVS soft switching of the inverter devices. In this way, the inverter current is the superposition of a sinusoidal waveform created by the ICN network and a triangle waveform created by the transformer magnetizing inductance. This triangle waveform has positive and negative peaks at the switching transition which help maintain ZVS across the full input voltage range. A magnetizing inductance of 42 μH was chosen based on simulations.

To summarize, the transformers are made using EPCOS EILP43-N49 cores with a winding structure implemented in an 8-layer, 4 oz copper PCB plus a single-turn 5 mil foil on top. The general structure, which can be seen in Figure 2-17, includes a 10-turn primary winding and a 1-turn secondary winding. The primary winding is split in half between two series-connected layers. There are two full sets of primary windings which are connected in parallel with each other. Sandwiching each layer containing a primary winding is a single-turn secondary winding. The four PCB secondary windings plus the foil secondary winding are connected in parallel. Because of the interleaved layers, the transformer provides low loss, but does not provide sufficient leakage inductance to be used in the ICN as can be seen in the model of Figure 2-18. The winding resistance was measured using an impedance analyzer without the core. These values represent a lower bound on the winding resistance. The addition of the core could impose some proximity effect and increase the ac resistance of the winding, but interleaving should help

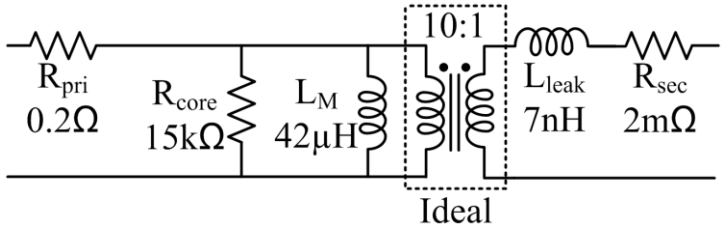


Figure 2-18: Transformer circuit model used in simulation. In this model, R_{pri}, R_{sec}, and L_{leak} are parasitic elements. L_M is the magnetizing inductance that was specifically chosen and R_{core} is a means of incorporating the core loss. It should be noted that these are approximate values and may vary for the actual experimental setup.

reduce this loss. The magnetizing inductance is measured using the impedance analyzer. The resistance representing core loss is calculated from the estimated power loss through the core (dependent on voltage across the core, the frequency, and manufacturer core loss data which can be found in the MATLAB code of Appendix A). The leakage of the transformer is calculated based on the energy methods of [53] after knowing the PCB layer spacing and copper thickness (see Appendix D).

2.2.3 Coupled Inductor Design

The ICN structure is partially realized through a coupled magnetic structure (outlined in a red-dashed box in Figure 2-13) that reduces the loss in the resonant tank magnetic components for the system. In a single magnetic component, one can achieve portions of the ICN reactances as well as an inductor for the output resonant tank ($L_B/C_{R,O}$) which is used to suppress harmonic injection from the rectifier. An example of how such an inductor can be implemented is shown in Figure 2-19(a) and the equivalent circuit "T" model [64,65] is shown in Figure 2-19(b).

For the structure shown in Figure 2-19(a), we can mathematically derive the equivalent inductor values shown in Figure 2-19(b). Let the specific inductance in (nH per turn^2) of the core be A_L. Let there be N_L turns between terminals a and c, and N_L turns between c and b for a center-tapped inductor. Relating this to the equivalent circuit model of Figure 2-19(b) we get the following set of equations:

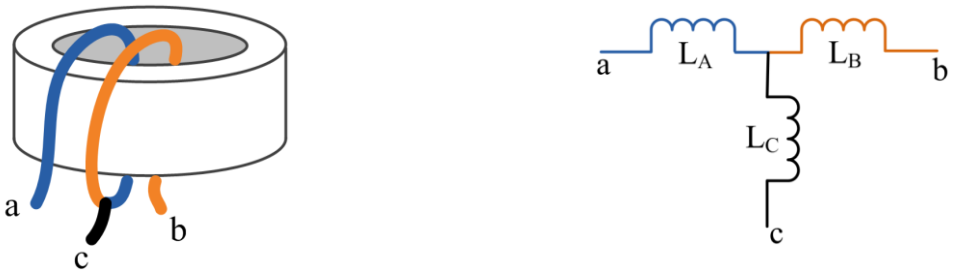
$$L_A + L_C = N_L^2 A_L , \tag{2.27}$$

$$L_B + L_C = N_L^2 A_L , \tag{2.28}$$

$$L_A + L_B = 4N_L^2 A_L . \tag{2.29}$$

Subtracting (2.28) from (2.27) gives:

$$L_A = L_B \tag{2.30}$$



(a) (b)

Figure 2-19: Coupled inductor (a) example implementation and (b) equivalent circuit model. This implementation uses a toroidal magnetic core and each inductor is composed of only one turn. This model is referred to as the "T" model [64,65]. Inductors L_A, L_B and L_C are the apparent inductors of the T model of the coupled magnetic winding.

and substituting (2.30) into (2.29) gives:

$$L_A = L_B = 2N_L^2 A_L \tag{2.31}$$

Lastly, substituting (2.31) into (2.27) results in:

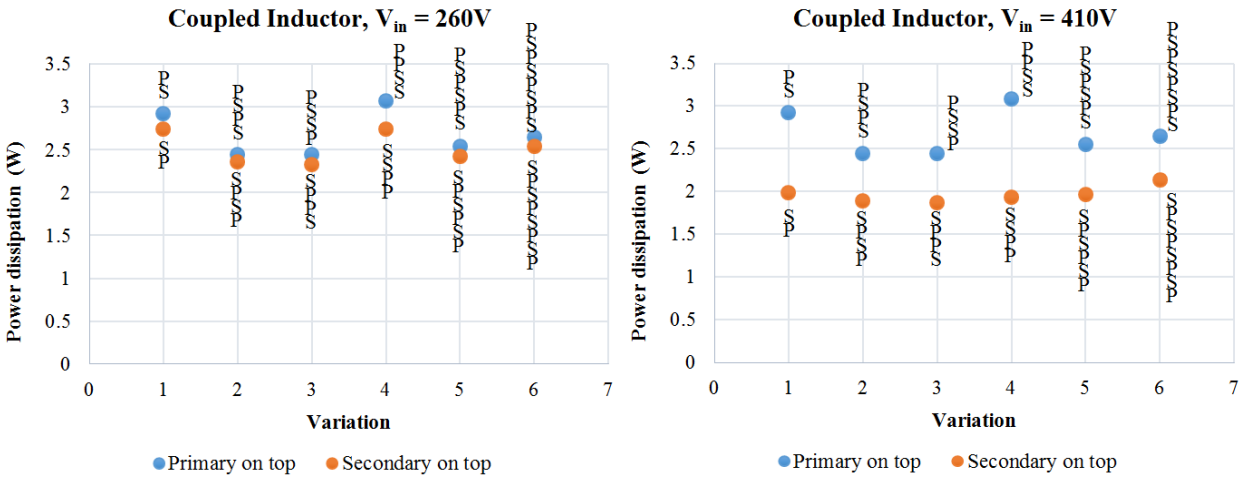
$$L_C = \ -N_L^2 A_L \,. \tag{2.32}$$

The negative inductance contributes to the negative impedance in Figure 2-3. Because the magnitude of L_C is only half that of L_A, additional capacitors are needed to obtain the full value for -jX.

Because this component will be conducting over 30 A_{rms} of current in each winding, only one turn is used for each winding element for a total of two turns around the center leg. This means that the specific inductance, A_L, will have to be very precise to get the desired impedance. For this prototype converter, the impedance is determined from (2.24) using a minimum input voltage of 260 V, an output voltage of 12 V, a turns ratio N of 0.1, and an output power rating of 400 W. From this we get an impedance of 0.2639 Ω. When this is converted to an inductance using an operating frequency of 500 kHz, we get 84 nH for L_A meaning the specific inductance should be around 42 nH/turn^2.

Similar to the transformer design, *M2Spice* was used to determine the best winding layer stack up. Again, a planar design is desirable to reduce interconnect loss and to keep ac losses low. Out of the low profile E cores available, EILP18 in N49 from EPCOS was the most promising given the operating frequency and low inductance required, which could not be achieved with some of the larger cores (see Appendix A for the appropriate MATLAB script). For this magnetic component in particular, *M2Spice* helps to inform the design where intuition may be lacking. This coupled inductor straddles the space between a transformer and an inductor as it has two ports driven by current sources and the third port delivers the summation of those two currents. Therefore, each winding will see a different current that will generate magnetic fields that cancel in part of the cycle and add together in the remainder. Furthermore, the amplitude, phase, and shape of each current source are highly dependent on the circuit behavior.

Using the geometry from the EILP18 core set, different layer configurations were input into *M2Spice* and the netlists were simulated (see Appendix B for *M2Spice* geometry files). From Figure 2-20(a) and Figure 2-20(b) it can be seen that the number of layers, the order of the layers, and the shape of the current (as affected by the input voltage) all make an impact on the estimated loss. In general, using a fully interleaved alternating pattern will result in lower losses. Increasing the layer count from two to four also will reduce loss. Increasing the layer count beyond four does not necessarily reduce loss and may actually increase loss. Perhaps what is most interesting is that the losses will vary depending on which winding is closer to the airgap. In this case, it is optimal to place the secondary winding on top. That is, the winding that will carry the summation of the current from both transformers and goes to the



(a) (b)

Figure 2-20: Coupled inductor loss as the layer stack varies for an input voltage of (a) 260 V and (b) 410 V. The primary winding carries the current that goes through the top branch of Figure 2-13 and the secondary winding carries the current that goes to the output rectifier. The top layer is closest to the gap.

output rectifier should be placed closest to the airgap. This observation has been experimentally verified in [60]. In the verification setup, a facimile of the final planar PCB-integrated coupled inductor is implemented with the Coilcraft Planar Transformer Prototyping Kit [66]. The core is a PL140 core, the gap is created with kapton tape and the primary and secondary windings are implemented with single-turn stamps as shown in Figure 2-21. To avoid the impact of temperature rise in experiments, a prototype version of the converter using this facsimile inductor was operated in a low-power mode with 100 V input voltage, 5 V output voltage, and 10 A output current. The total loss of the converter with different coupled inductor implementations was measured. The predicted trend from SPICE and measured losses in multiple experimental setups are shown in Figure 2-21. It can be seen that the trend that using parallel layers reduces the loss, having the secondary layer closer to the gap reduces the loss, and that a more efficient coupled inductor design can help to reduce the total converter loss. It should be noted that exact loss values from SPICE are not shown because quantitative predictions of total converter loss are not very accurate, in part because the SPICE model does not include many practical details (e.g., PCB trace losses).

To summarize, the coupled inductor is made using an EPCOS EILP18-N49 core with a winding structure implemented in a 4-layer, 4 oz copper PCB. The general structure, which can be seen in Figure 2-22, includes a two turns that are center tapped. Each winding comprises two parallel layers which are fully interleaved. The winding that conducts the output current is on top, placing it closest to the gap which is implemented in several layers of kapton tape on each of the centerpost and outer posts for a total gap length of approximately 2 mm. A PCB layout for the windings is shown in Appendix D.

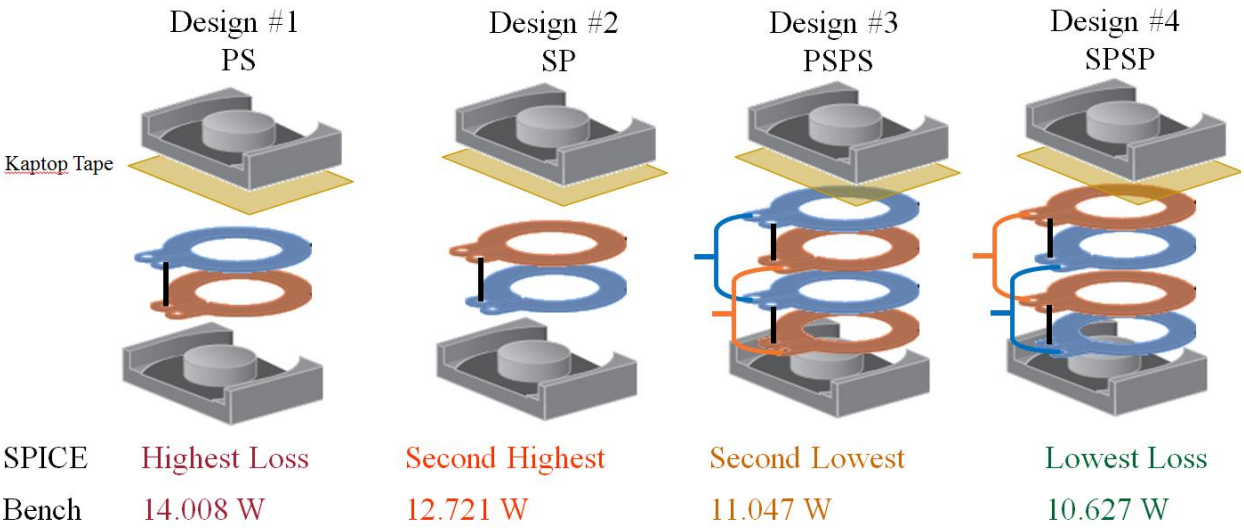


Figure 2-21: Coupled inductor design variants that were experimentally tested in the ICN converter to determine the optimal design. This was used to compare against the results that were gathered from using *M2Spice* generated netlists in simulation. Shown under each design is the comparative loss that SPICE predicted and the actual loss of the circuit when running the converter with an input voltage of 100 V, output voltage of 5 V, and output current of 10 A.

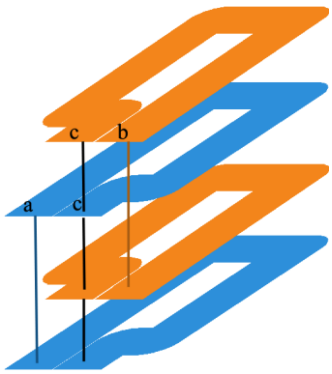
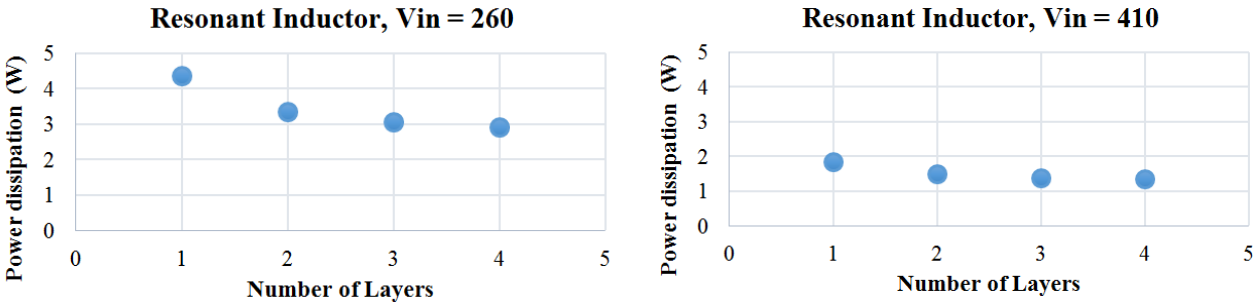


Figure 2-22: Winding structure for the coupled inductor. Ports a, b, and c correspond to those shown in Figure 2-19. A detailed PCB layout is shown in Appendix D.

2.2.4 Resonant Inductor Design

The final magnetic component is the resonant inductor $L_{R,B}$ found in the bottom branch of Figure 2-13. As was done in the previous sections, a MATLAB script (see Appendix A) was used to determine the core geometry and *M2Spice* was used to determine how many layers to use (see Appendix B for *M2Spice* geometry files). In order to handle the high current, a single turn winding using parallel layers is desired. EPCOS EIR23-N49 was a low loss geometry and based on *M2Spice* analysis, four layers seemed to be the point of marginal returns as can be seen in Figure 2-23. Since this is a standard inductor, there is



(a) (b)

Figure 2-23: Resonant inductor loss as the number of layers increases for (a) 260 V_{in} and (b) 410 V_{in}.

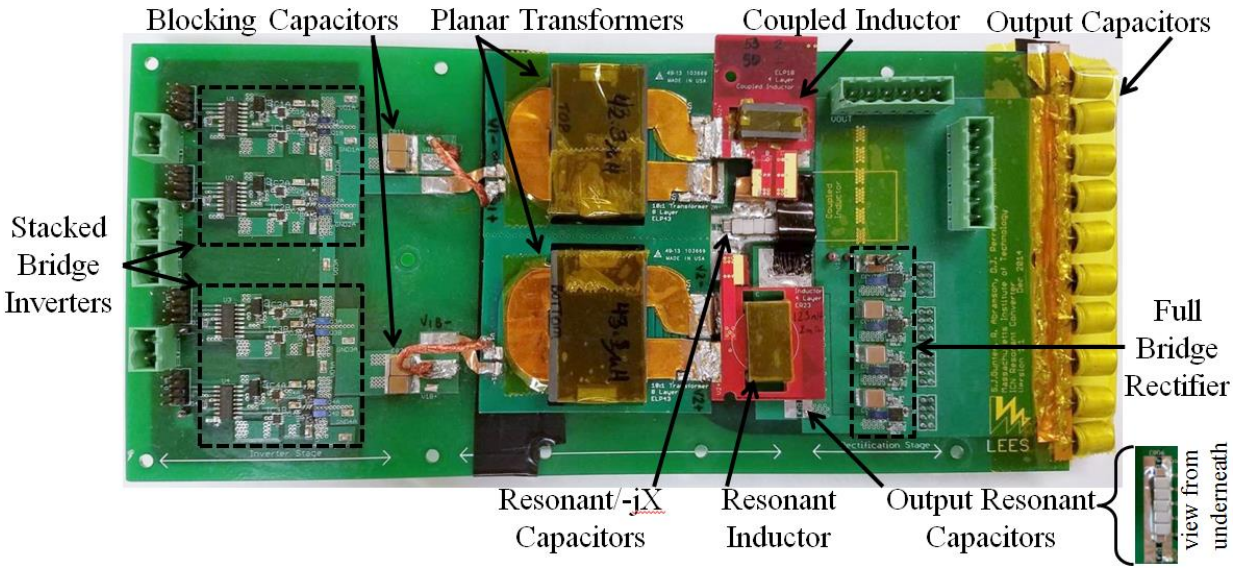
Figure 2-24: Winding structure for the resonant inductor. A detailed PCB layout and circuit board stackup for the windings is shown in Appendix D.

no interleaving benefit. The planar winding structure can be seen in Figure 2-24. A gap of approximately 0.5 mm is created between the two core halves using kapton tape.

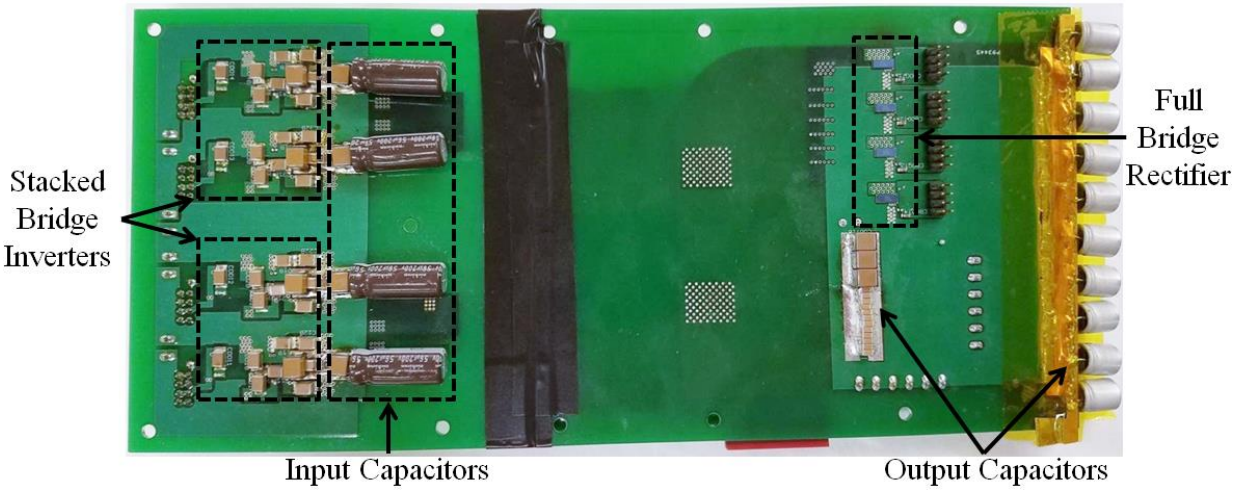
2.3 ICN Converter Performance

For the prototype converter, the inverter stage, magnetic components, and rectifier stage are implemented on separate boards to allow rapid replacement and refinement of the three individual stages. Nonetheless, the approach is compatible with full integration of the components. However, very careful attention needs to be paid to the traces and parasitic capacitance. Figure 2-25 shows the top and bottom views of the final converter prototype. PCB layouts, and complete schematics and bill of materials are shown in Appendix D and Appendix E. A photograph of the experimental setup used to measure the system performance is shown in Figure 2-26 and the equipment used is listed in Table 2-5.

A computer is used to set and send the gate drive signals using the control board developed by David Otten of MIT. It is also used to manually record operating parameters and data measured by the various meters. A single dc power supply is used to power the board and an electronic load operated in voltage source mode is used on the output. A power meter is used to measure the dc input voltage, dc input current, dc output voltage, and dc output current. It also calculates and displays a time-averaged



(a)



(b)

Figure 2-25: Populated ICN resonant converter showing both (a) top and (b) bottom views.

power and efficiency. This is extremely helpful due to the open-loop nature of the control. Other digital multimeters can be used to monitor the voltage across each inverter half-bridge. A dc fan blows air across the high current output stage to prevent thermal overload and a thermal camera is used to take thermal measurements. To reach the nominal operating point, the converter is first run with an input voltage of 20 V and an output voltage of 1 V. Using (2.20), each phase-shift is calculated as 1.0472 radians or 16.67% of the period. The total phase-shift used is 661.44 ns (or 33.24% of the period at the operating frequency of 502.5 kHz) between the two inverters. A phase-shift of 372.32 ns is used between the leading inverter and the rectifier and is based on simulation. The input voltage and output voltage are increased until an

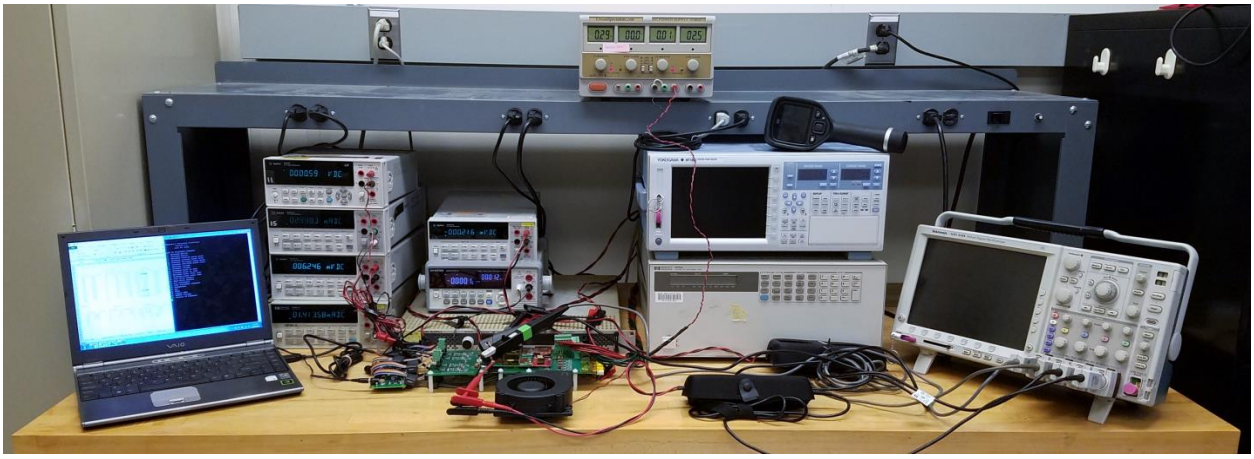


Figure 2-26: Experimental test setup for running the proposed ICN resonant converter. Several meters are used to measure various parameters such as dc input voltage, dc input current, dc output voltage, dc output current, gate drive voltage, gate drive current, and transformer voltage and current waveforms. A comprehensive list of equipment used is found in Table 2-5.

Table 2-5: List of equipment used to run and take measurements for the Impendance Control Network resonant converter

Equipment Description	Model	Purpose
Laptop	Sony Vaio VGN-SZ160P	Essential for operating the converter
DC Power Supply	KLP600-4-1.2K	
System DC Electronic Load	HP6050A	
Mixed Signal Oscilloscope	Tektronix MSO 4104	Used to measure voltage and current waveforms
High Voltage Differential Probe (x2)	Tektronix P2505 (x2)	
High Voltage Differential probe	Tektronix P6251	
Passive voltage probe	Tektronix 6139B	
Current Probe (x2)	Tektronix TCP202A (x2)	
Power Meter	Yokogawa WT1800	Used for efficiency measurements
Digital Multimeters (multiple)	Agilent 34401A (multiple)	
Thermal Camera	FLIR-E63900	Used for thermal measurements
DC Power Supply	HY3002D-3	Used to prevent thermal overload
Fan	Sunon PMB1212 PLB2-A	

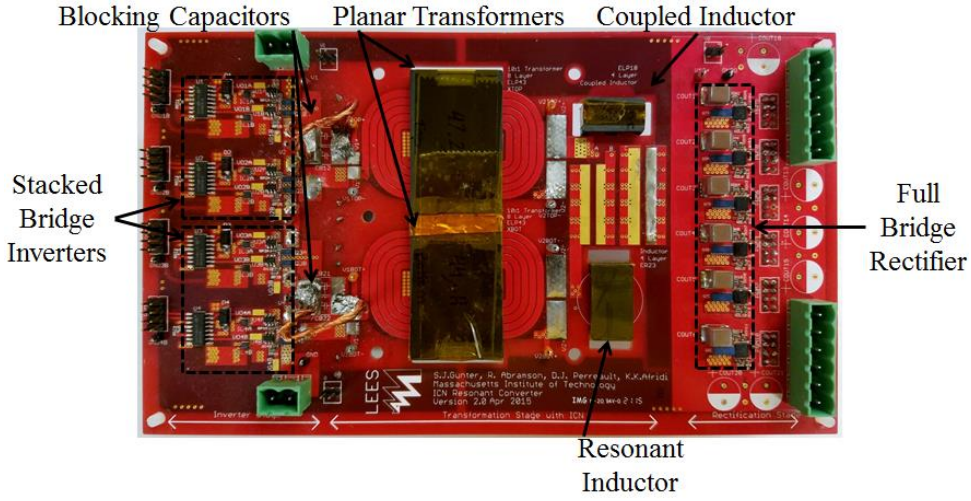
input voltage of 240 V and an output voltage of 12 V is reached. After that, only the input voltage is increased and the phase-shift is adjusted manually using preset inverter and rectifier phase-shift values based on the input voltage. Full details of the converter startup and operating parameters can be found in Appendix F.

A fully integrated board (pictured in Figure 2-27) was developed and performed very well during the startup routine. (The detailed layout of the fully integrated board can be found in Appendix D.) Figure 2-28 shows the output power and efficiency comparison between the fully integrated board and the final version of the non-integrated prototype of Figure 2-25. Unfortunately beyond an input voltage of 200 V, one or more inverter switches would consistently blow up. After extensive attempts to debug the integrated board, it was concluded that the improved layout of the output stage (beyond the secondary of the transformer) had much lower trace inductance than the original prototype design. Combine this with the fact that planar transformers tend to have very high interwinding capacitance, it is believed that the high dv/dt of the negative terminal of the rectifier input voltage caused significant harmonic injection through the transformer to the inverter. This ultimately resulted in unwanted shoot-through of the inverter devices. If harmonic filtering had been implemented on both rectifier switch nodes (instead of just one node as proposed), this problem may have been avoided at the cost of increasing component count and power loss. The inductors from this fully integrated board were used in the final converter shown in Figure 2-25 to help improve performance of the magnetic components.

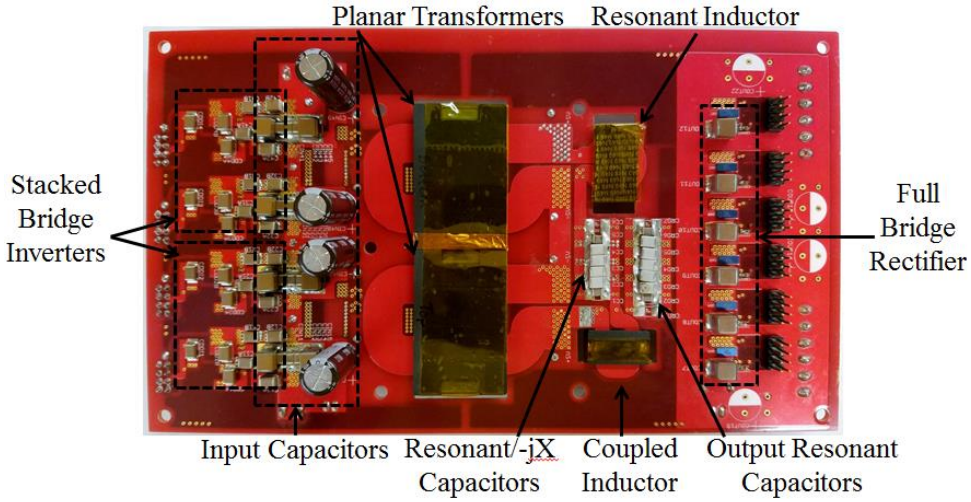
2.3.1 Converter Waveforms across Input Voltage

Waveforms taken on the bench show promising converter performance. The waveforms for the endpoints of the input voltage range as well as the nominal operating point are shown in Figure 2-29 and Figure 2-30, respectively. The applied voltage across the primaries of the top and bottom transformer are shown (in blue and cyan, respectively); from these waveforms, the behavior of the inverter switches is still represented. Across the full operating region, we get ZVS switching as predicted by the design models. In Figure 2-29 and Figure 2-30, this is indicated by the gentle rise in the transformer voltage without substantial ringing at the peak. Upon closer inspection, it can be seen that there is a minor rise or dip in the voltage just after the transition and right before a long flat period. This is likely due to conduction of the "body diode" of the transistor, further indicating a ZVS transition.

Also shown in Figure 2-29 is that the (transformer primary) current is fairly sinusoidal at the low end of the input voltage range and begins to become trapezoidal towards the high end of the input voltage range. We can also see that the phase shift between the inverters decreases as the input voltage increases, reflecting the proposed control method. The phase shift used is the same as the phase shift that is calculated from (2.20) (details listed in Appendix F). In general, both currents are relatively in phase with



(a)



(b)

Figure 2-27: Populated fully integrated converter showing both (a) top and (b) bottom views.

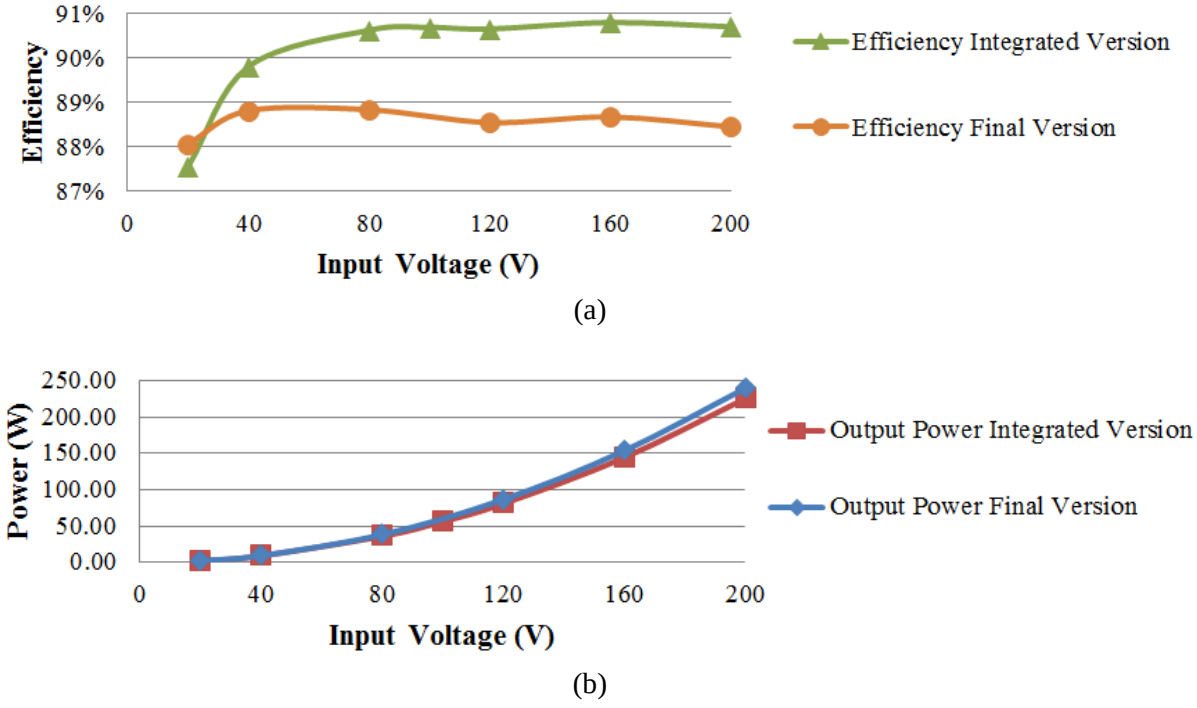
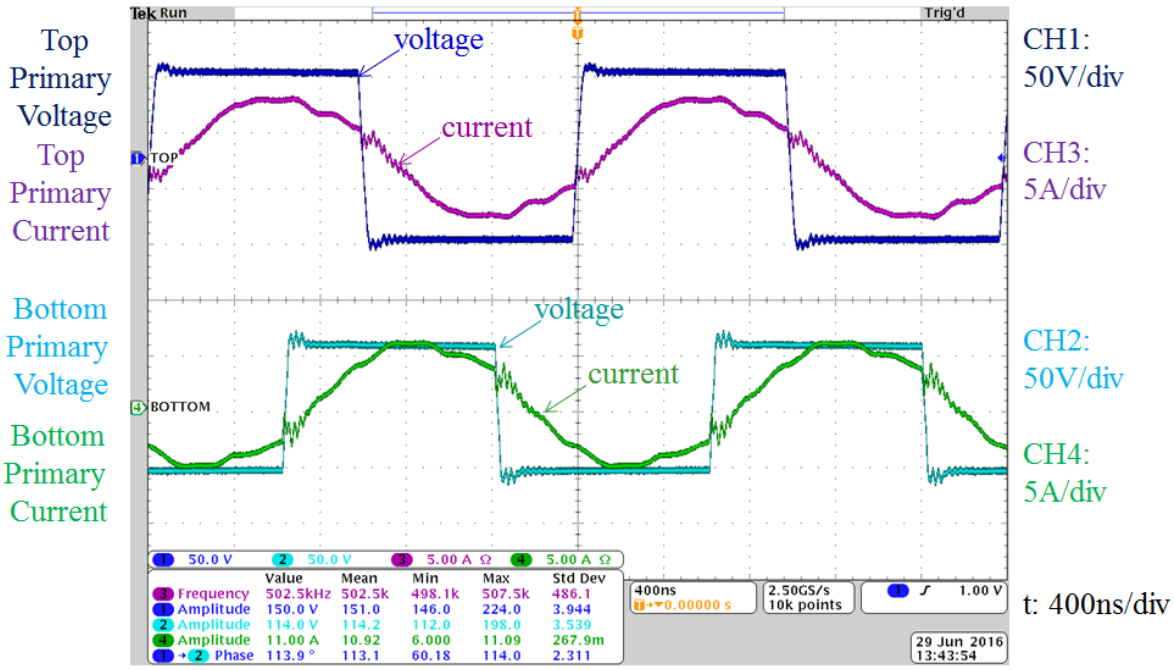
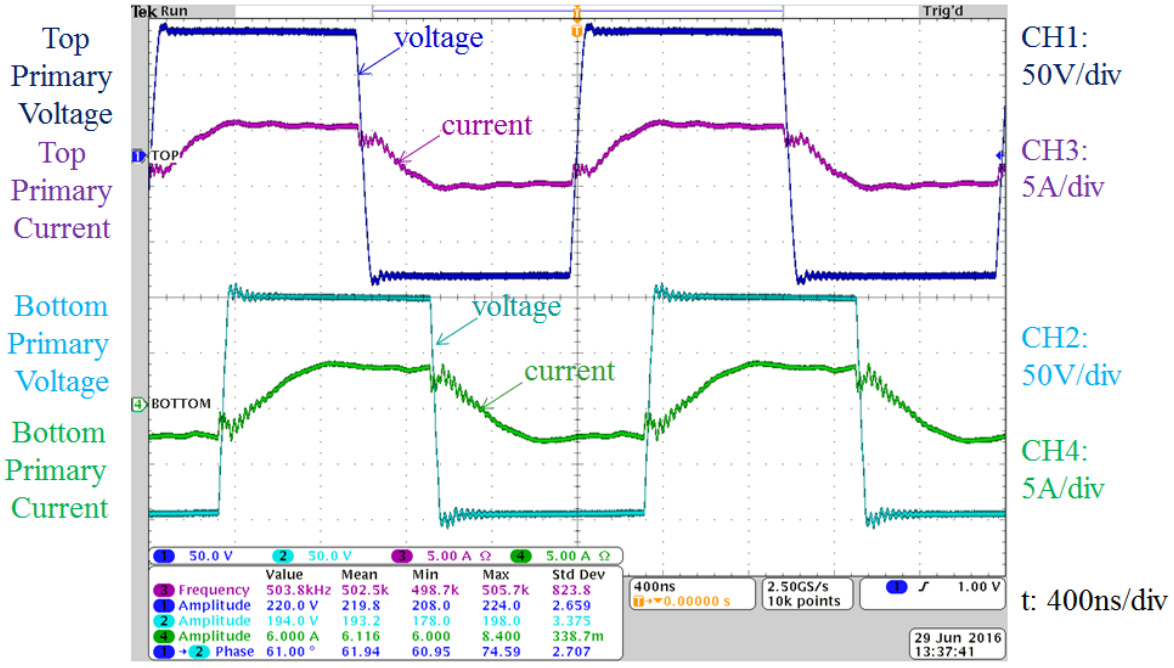


Figure 2-28: Efficiency comparison between the fully integrated board of Figure 2-27 and the final version of the prototype that is not fully integrated. Across the same input voltage range, the power delivered by both converters was comparable but the efficiency was higher for the fully integrated version showing promise in developing a more refined ICN resonant converter prototype.



(a)



(b)

Figure 2-29: Scope captures for input voltages of (a) 260 V and (b) 410 V with the output voltage fixed at 12 V by an electronic load. The top set of waveforms shows the voltage across the primary of the top transformer and the current into the primary. The second set shows the voltage across the primary of the bottom transformer and the current into the primary.

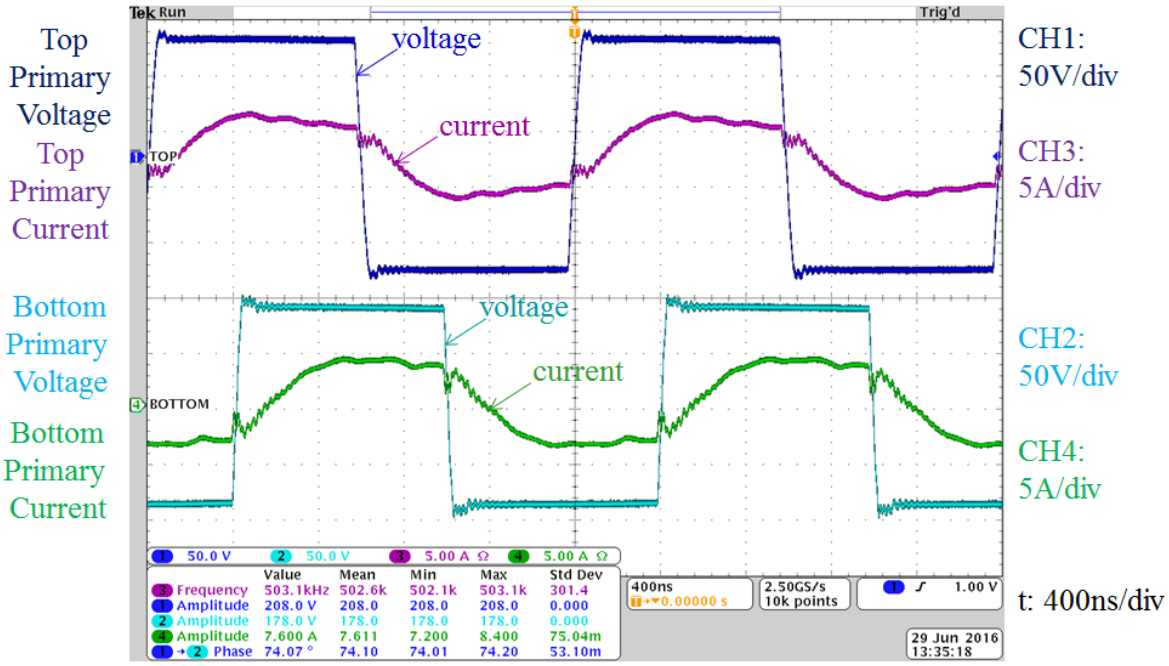


Figure 2-30: Scope captures for the nominal input voltage of 380 V with the output voltage fixed at 12 V by an electronic load. The top set of waveforms shows the voltage across the primary of the top transformer and the current into the primary. The second set shows the voltage across the primary of the bottom transformer and the current into the primary.

the voltage with enough current at the switch transition to ensure soft switching. Unlike traditional phase shift control, the current does not become asymmetric as the input voltage varies.

It can be observed that there is a slight imbalance between primary voltages and currents, reflecting a modest imbalance in the level of voltages of the inverter stack. While this deviates from assumptions made in the theoretical derivation, this behavior actually is expected and can be predicted in simulation. Figure 2-31 shows the voltage distribution of the four input capacitors across the full input voltage operating range of the converter. The voltage imbalance on the bench tracks fairly well with the voltage imbalance predicted in simulation. It should be noted that there are no voltage balancing circuits. Figure 2-32 shows a comparison of experimental and simulated waveforms at the minimum and maximum input voltages. It is believed that the imbalance is a result of the realization of the positive and negative impedance through an inductor and a set of capacitors, respectively, and their impact to the shape and behavior of the current. The imbalance helps ensure that there is equal power transfer between the two transformers.

Power and efficiency measurements for the power stage have been taken and are shown in Figure 2-33. Note that these measurements do not include control or gating losses but these are known to be negligible compared to the power stage losses. The input power is fairly well matched to the shape of theoretical power shown in Figure 2-9. Mismatch can be attributed to small deviations in the turns ratio

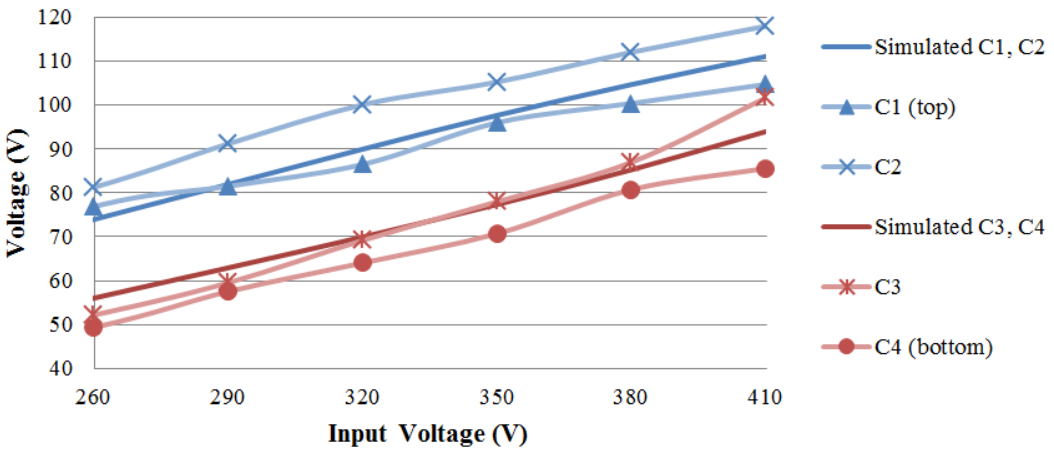
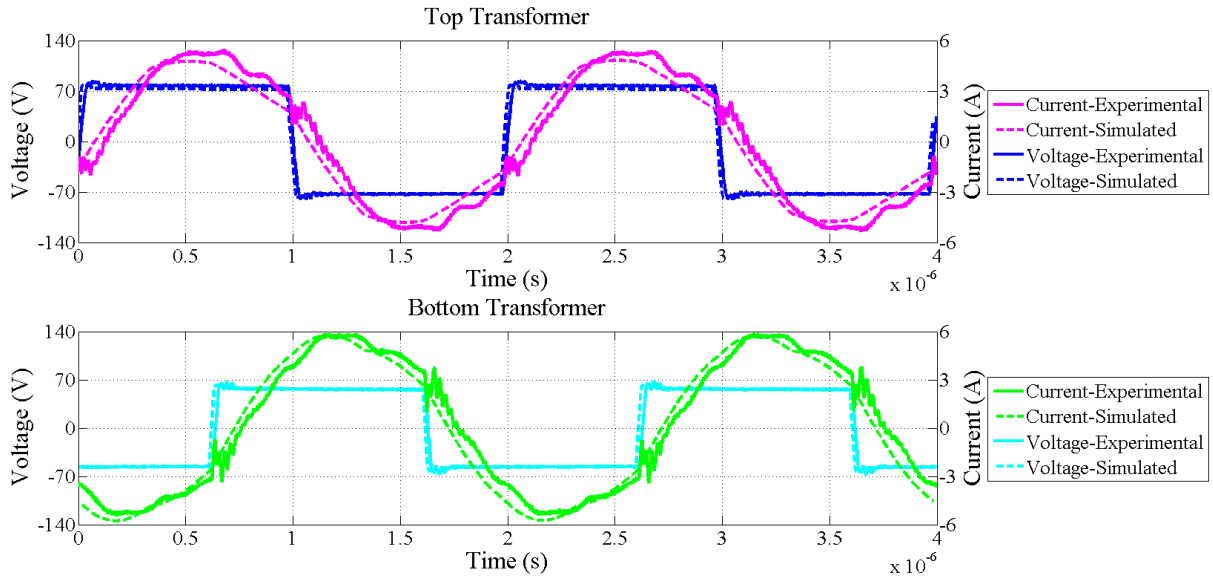


Figure 2-31: Voltage across the input capacitors based on simulation and experimental data. The four input capacitors are stacked across the input voltage with C1 on top above C2 which is above C3 which is above C4. In simulation, C1 and C2 have the same voltage across them and C3 and C4 have the same voltage. In practice, there is some variance between the voltages.

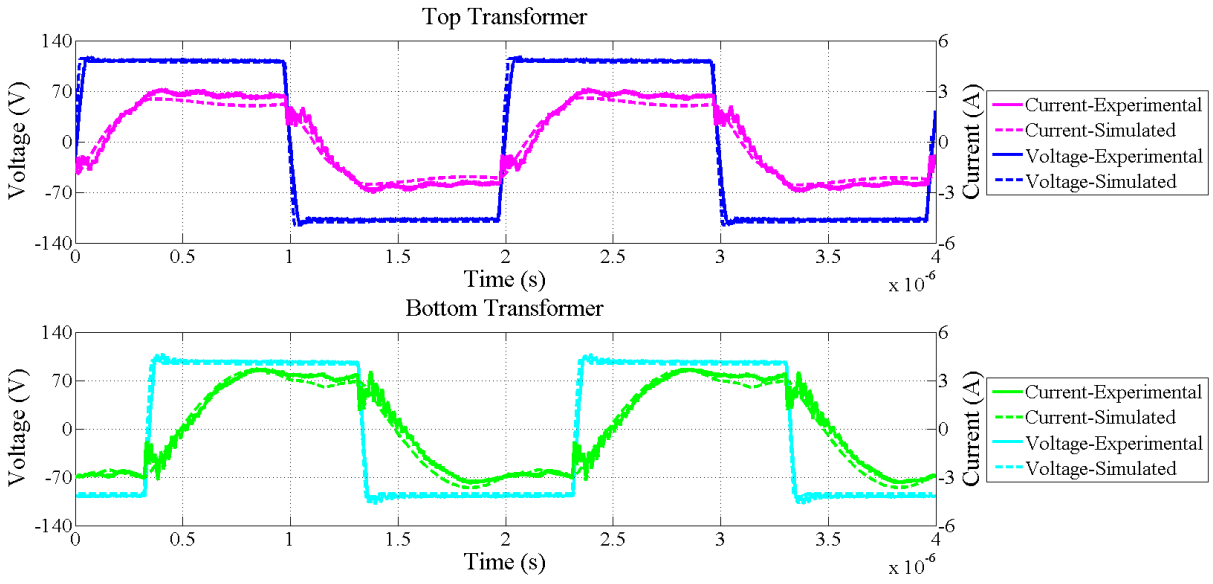
and impedances from the calculated values of (2.23) and (2.24). Impedance mismatching could be tuned through the addition of series capacitance. This characteristic confirms the theoretical prediction in Section 2.1 regarding the ability to provide a very flat power characteristic versus input voltage. At the same time, the output power and efficiency is significantly lower than the theoretical prediction. Inefficiencies in the circuit cause the output power to drop below the theoretical value. Theoretical calculations assume lossless components but the real circuit includes several loss mechanisms. In order to understand the dominant loss mechanisms, a loss analysis was performed, as described below.

2.3.2 Converter Loss Analysis

Figure 2-34 shows the operating temperature distribution of the board across the voltage range as measured with a FLIR E6 infrared camera; no correction for emissivity of various sections was employed. For this particular prototype, the main loss mechanism is conduction loss as seen in the breakdown of Figure 2-35. The total loss is found from the experimental data (dc input power minus dc output power) and the breakdown of the loss is estimated through impedance measurements taken on the board or manufacturer datasheet parameters and incorporated into the simulation. A more detailed discussion of the how the losses were estimated can be found in Appendix C. With an input voltage of 260V, the converter delivers 365 W to the output and with an input voltage of 410V, the converter delivers 368 W. Despite delivering roughly the same amount of power, the converter operates much more efficiently at the higher input voltage. This further supports the notion that conduction loss is the dominant loss factor for this prototype because many of the circuit currents are higher for 260V than for 410V. (This loss mechanism is exacerbated by the construction technique used for the prototype.)



(a)



(b)

Figure 2-32: Simulated and experimental waveforms for input voltages of (a) 260V and (b) 410V. The top pane of each set of waveforms shows the voltage across the primary of the top transformer and the current into the primary. The second pane shows the voltage across the primary of the bottom transformer and the current into the primary. For all plots, the solid line is the experimental data of Figure 2-29 and the dashed line is the simulated data.

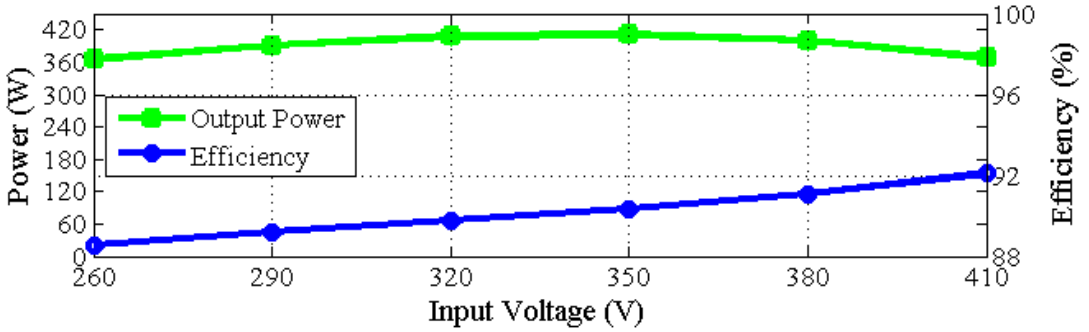


Figure 2-33: Experimental results for power stage output power and efficiency.

(a) (b)

Figure 2-34: Thermal images of the board operating at an input voltage of (a) 260 V and (b) 410 V. A fan can be seen at the bottom and is intended to keep the output stage (particularly the switching devices) from overheating.

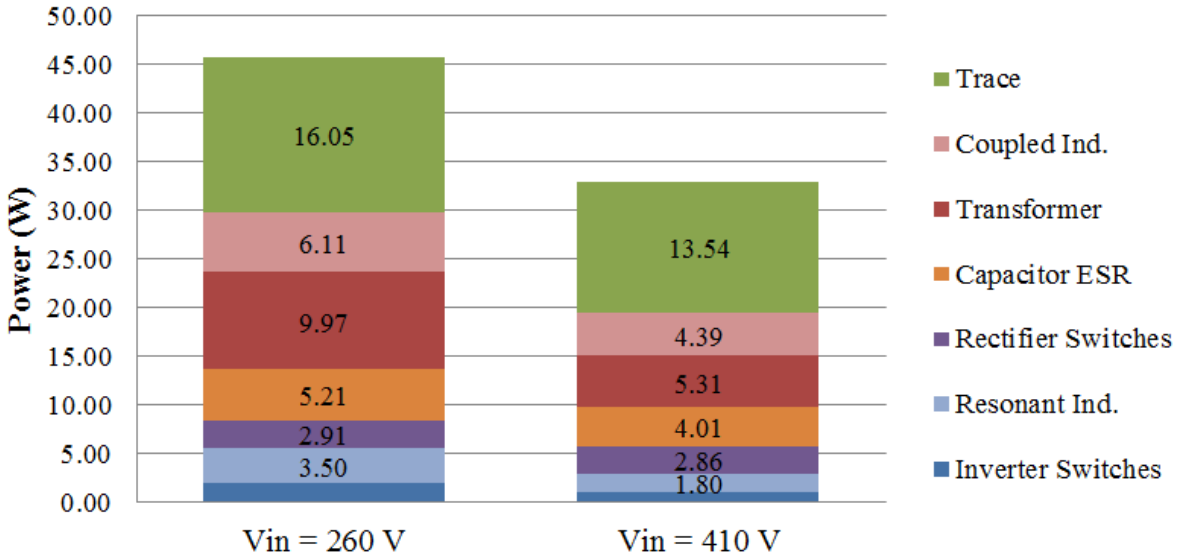


Figure 2-35: Simulated breakdown and comparison of loss for input voltages of 260V and 410V. At both of these operating points, the power delivered to the output is approximately equal at around 365W.

Thermal imaging (see Figure 2-34) also shows that the highest temperature rise is seen beyond the secondary of the transformer, most likely due to the large currents there. It can also be seen that the windings have a much higher temperature rise than the magnetic cores (assuming that the emissivities are not too different in the image) further indicating conduction loss as the dominant loss mechanism. Ways to improve performance include a greatly refined prototype having a higher degree of integration, optimization of the control and switching dead-time, and fine-tuned impedances.

2.3.3 Converter Performance across Output Power

As mentioned in Section 2.1.2, the converter can operate at varying output powers by using burst mode or on/off control. For this setup, an open-loop variable frequency, variable duty ratio burst is used to maintain the output voltage ripple of the electronic load in resistive mode to within ±2% of the desired output voltage of 12 V. The number of cycles on and number of cycles off were selected based on visual measurements to keep output voltage ripple (as measured by a Tektronix P6251 differential probe) seen on the oscilloscope within ±240 mV bands while simultaneously delivering the desired power at the desired output voltage (both parameters are displayed on the power meter). For example, to deliver about 50% of the power to the load, the converter is turned on and delivers full power for about 100 cycles and then is turned off and delivers no power for another 100 cycles as show in Figure 2-37. With sufficient output capacitance, the output voltage ripple can be kept small. Full details on the number of cycles on and cycles off for each operating point can be found in Appendix F. The control board does have inputs

for up to five external analog signals so closed-loop control is possible. Equivalent closed-loop control circuits are readily implemented (e.g., [41]).

Using this burst scheme, it can be seen that the power can be significantly lowered without drastically impacting the efficiency. Figure 2-36 shows that 50% of the power can be delivered and the efficiency only drops a small amount across the entire input voltage range (0.3% at 260 V_{in} to 1.05% at 410 V_{in}) using the burst scheme described. The minor drop in efficiency can be attributed to transients that occur at the startup and shut down as well as to losses in the ESR of the output capacitors. As can be seen from the waveforms in Figure 2-38 and Figure 2-39, the inverter switches experience hard switching for a couple of transitions during startup and shutdown as indicated by the large ringing in the current. On the other hand, the voltage across the transformer drops significantly when the converter is off helping to reduce core loss. Alternatively, if the converter was run continuously but with a lower current, it is likely core loss would remain constant and that ZVS would be completely lost due to insufficient current at all switch transitions. This burst method allows for mostly ZVS operation for efficient conversion across a wide range of power levels.

Of particular importance is the converter performance at the nominal input voltage of 380 V and across a wide range of power. As seen in Figure 2-40, the converter can deliver a peak efficiency of 90.83% at its rated output power of 350 W. It can maintain an efficiency of greater than 86.5% down to 35W (or 10% of rated power). In order keep efficiency high while also keeping the output voltage ripple within ±2%, the burst frequency and duty ratio change across power levels. To deliver 35 W, the converter is on for 57 cycles and off for 586 cycles resulting in a burst frequency of 780 Hz (see Figure 2-41(a)). To deliver 350 W, the converter is on for 178 cycles and off for 26 cycles resulting in a burst frequency of 2.5 kHz (see Figure 2-41(b)). Full details on each of the operating points plotted in Figure 2-40 can be found in Appendix F.

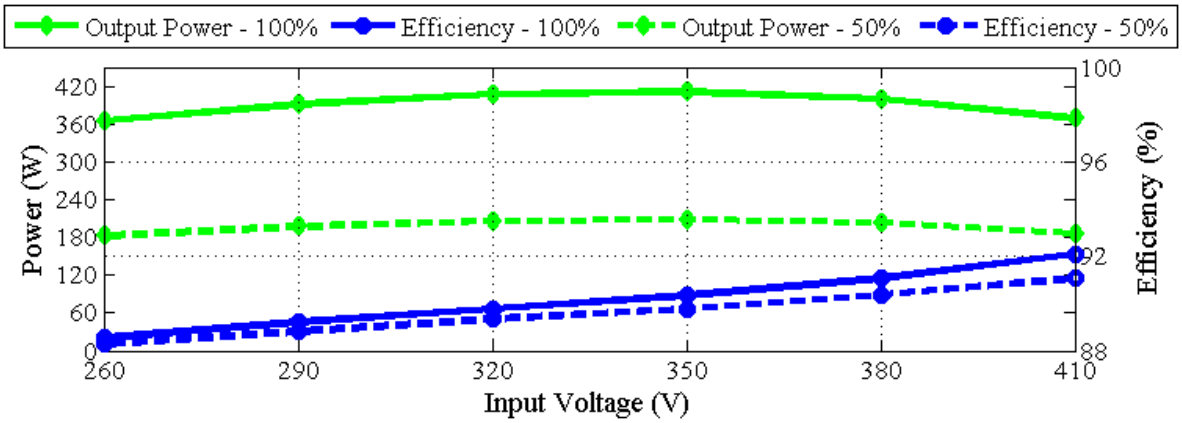
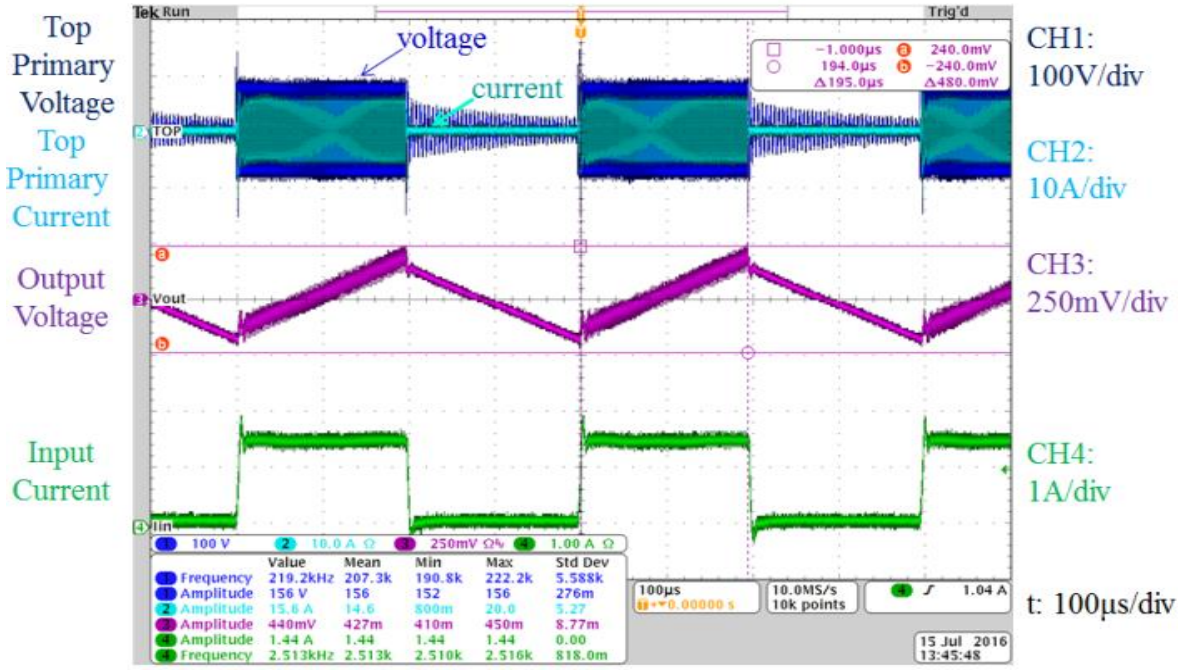
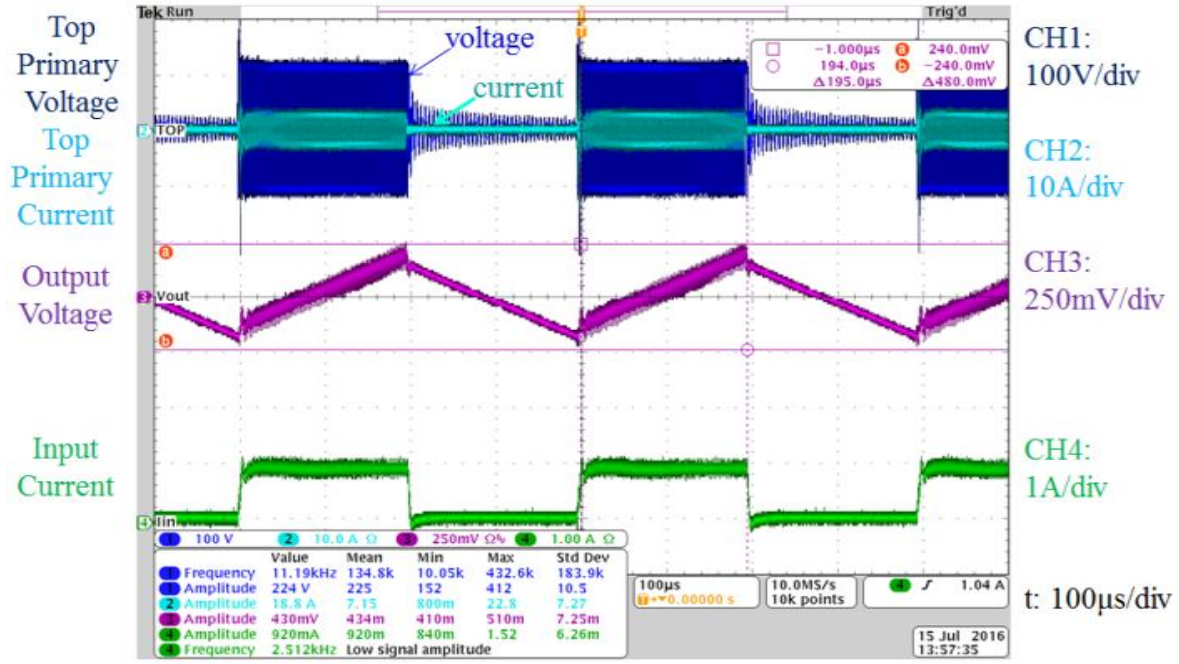


Figure 2-36: Experimental results for power stage output power and efficiency when operated at a 100% power and with a 50% burst duty ratio to deliver 50% power.

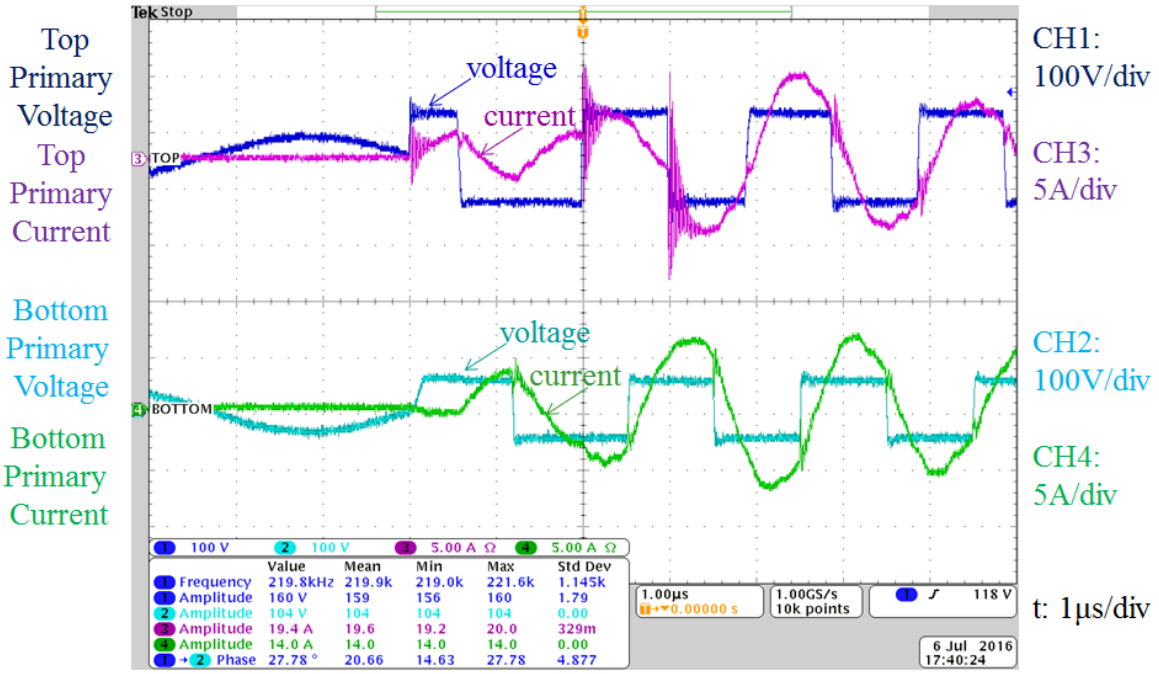


(a)

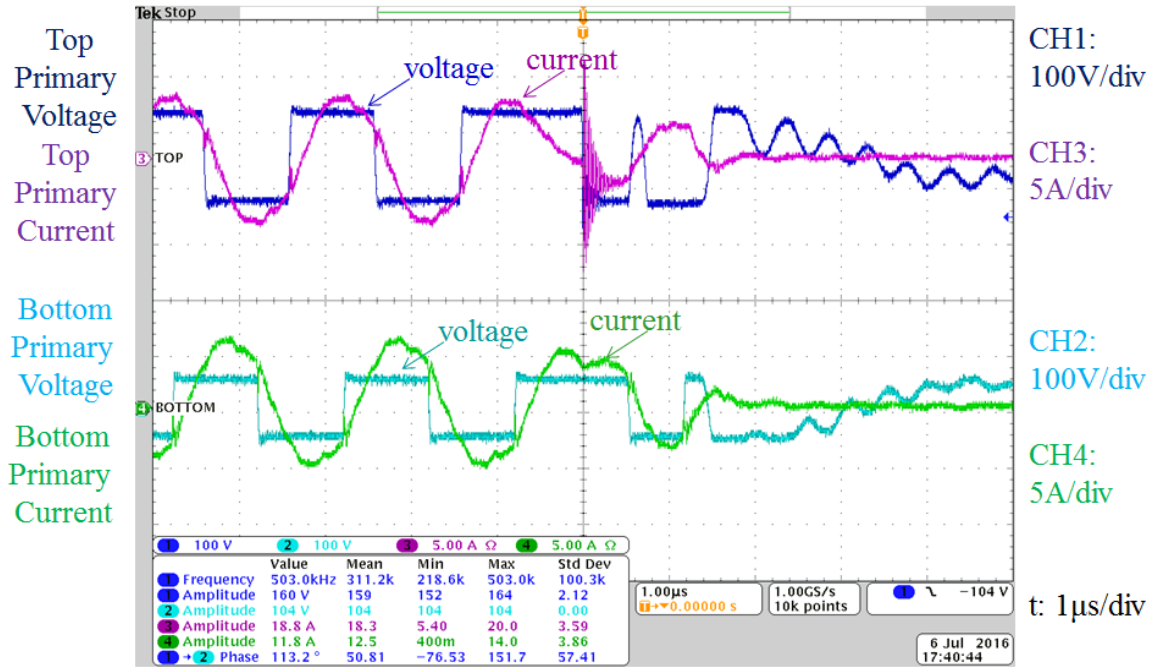


(b)

Figure 2-37: Converter voltages and currents when operating with a 50% burst duty cycle at a frequency of 2.5 kHz and an input voltage of (a) 260 V and (b) 410 V. For each screenshot, the top two waveforms are the primary voltage and current for the top transformer, the middle waveform is the ac component of the output voltage and the bottom waveform is the input current from the power supply. The horizontal cursor bars are set at +240 mV and -240 mV, which define the voltage ripple bands to stay within ±2%.

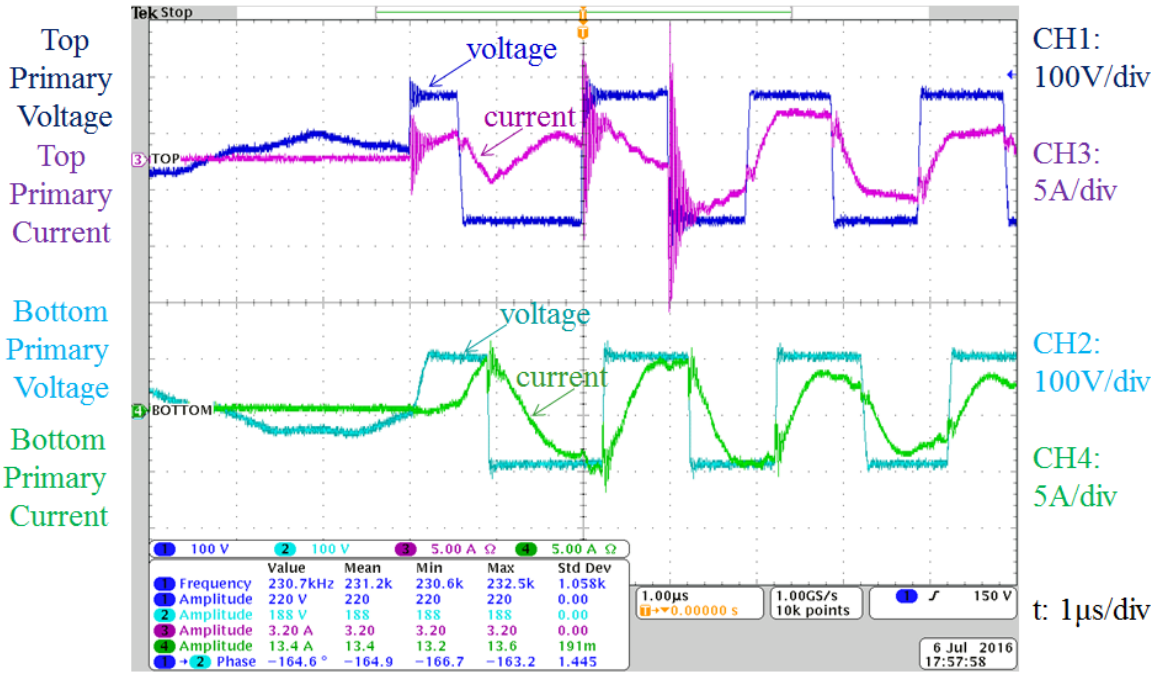


(a)

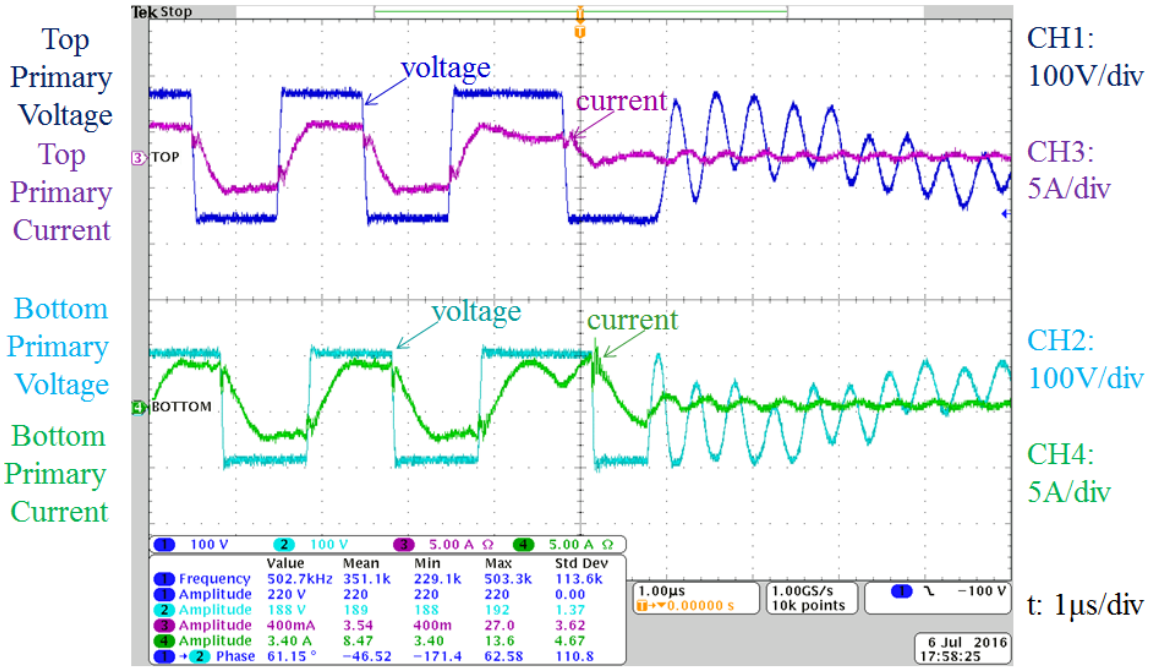


(c)

Figure 2-38: Transformer primary voltages and currents during (a) startup and (b) shutdown when operating under burst mode with an input voltage of 260 V. For each screenshot, the top two waveforms are the primary voltage and current for the top transformer and the bottom two waveforms are the primary voltage and current for the bottom transformer. It can be seen that steady state currents and soft switching are reached within a couple of switching cycles and when the converter is turned off, the transformer current quickly goes to zero.



(a)



(c)

Figure 2-39: Transformer primary voltages and currents during (a) startup and (b) shutdown when operating under burst mode with an input voltage of 410 V. For each screenshot, the top two waveforms are the primary voltage and current for the top transformer and the bottom two waveforms are the primary voltage and current for the bottom transformer. It can be seen that steady state currents and soft switching are reached within a couple of switching cycles and when the converter is turned off, the transformer current quickly goes to zero.

In order to increase the efficiency of the ICN converter at low load, a new control technique can be applied to the inverter and rectifier switches, which is discussed in the next chapter. Given the high component count, particularly with magnetic components carrying high current, the converter is limited in its efficiency. (The construction method used for the prototype also hurts achievable efficiency owing to loss in interconnects.) In order to improve the overall performance, another topology is demonstrated in Chapter 4.

2.4 Summary of the ICN Resonant Converter

In general, the ICN resonant converter exhibits many of the characteristics that are presented in theory and the experimental prototype waveforms are well matched to what is seen in simulation. As the input voltage is varied, the two inverters can be phase shifted such that their currents are in phase with their voltages in order to keep circulating currents low and efficiency high. Also important for efficiency, across a wide input voltage range, the converter can maintain soft-switching transitions, which is particularly important when converting from hundreds of volts. Across a wide output power, burst mode can be used to maintain high efficiency.

On the other hand, the particular specifications used for this prototype do present a challenge for the ICN technique. Namely, the output current of over 30 A_{rms} causes significant loss in many of the components which results in a lower efficiency than originally desired. The ICN converter has exhibited efficiencies in excess of 96% in a step-up application [67] and is promising for a number of other applications as well. Thus, the development of the ICN approach described here is expected to have value in a variety of applications with significant variations in input voltage.

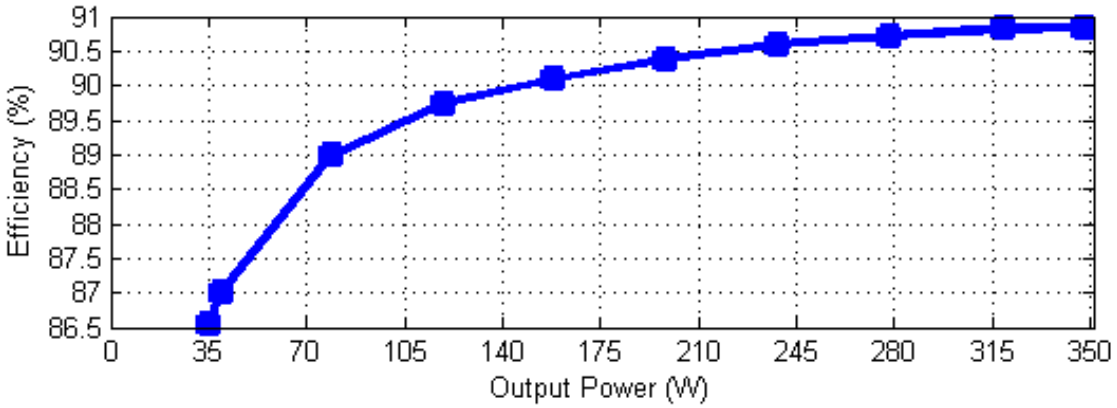
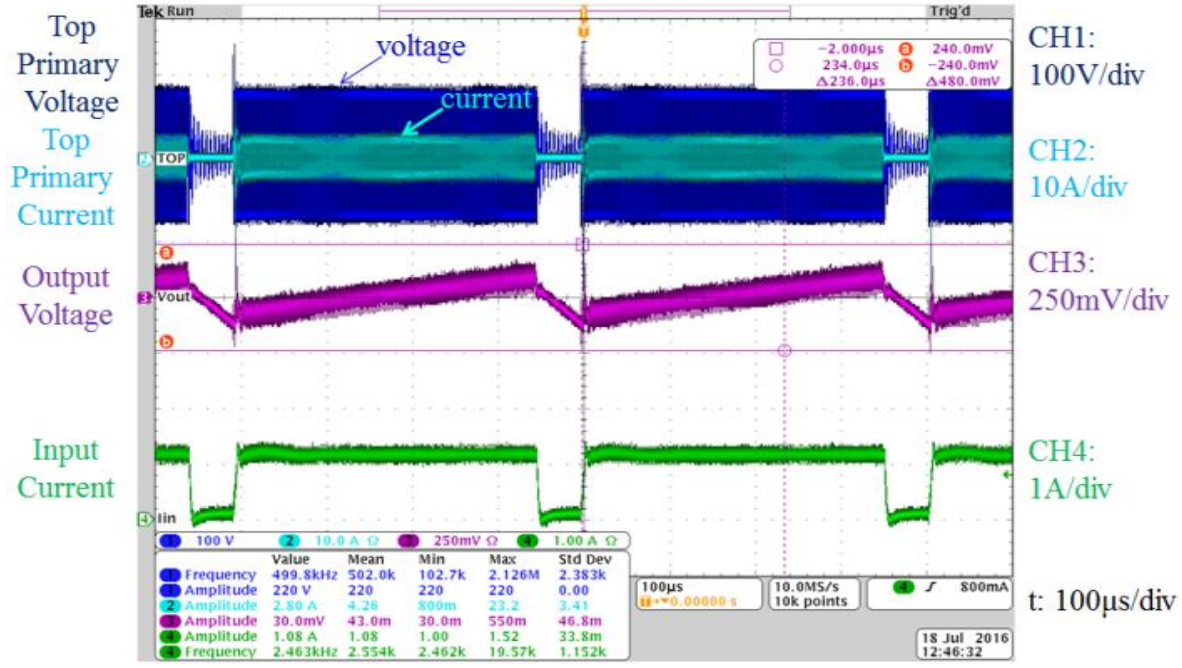


Figure 2-40: Efficiency across output power when operated with an input voltage of 380 V and using burst mode to control the power and keep the output voltage at 12 V.

(a)



(b)

Figure 2-41: Converter voltages and currents when operating under burst mode to deliver (a) 35 W and (b) 350 W at 380 V_{in}. For each screenshot, the top two waveforms are the primary voltage and current for the top transformer, the middle waveform is the ac component of the output voltage and the bottom waveform is the input current from the power supply. The horizontal cursor bars are set at +240 mV and -240 mV, which define the voltage ripple bands to stay within ±2%.

Chapter 3

Variable Frequency Multiplier

In the previous chapter, we propose modulating the output power of the Impedance Control Network (ICN) converter by using on/off control. In general, this method backs down in losses as power decreases allowing for efficient operation at lower power levels, however as the converter output power drops to very low levels (e.g., 10% load), the efficiency drops quickly, in part due to transient effects during startup and shutdown of the on/off control. This chapter will discuss a new operating mode which can be used at these lower power levels to help improve efficiency. First we will present the theory of the "frequency multiplier" operating modes. Then we will apply the operation to the ICN converter and discuss its effect on the output power. Finally, we present a limited set of experimental results.

3.1 Theory of the Proposed Method

In the inverter stage shown in Figure 3-1, we take the dc input voltage and pass it through two inverters and then a rectifier. A key design strategy we introduce is the use of additional "frequency multiplier" operating modes of the inverter and rectifier stages to achieve and maintain high performance across a wide operating range. Frequency multiplier circuits are often used in extremely high-frequency RF applications (e.g., where transistor f_T is a concern), and are sometimes used in switched-mode inverters and power amplifiers (e.g., [68,69]). While it has been proposed to employ frequency multipliers in dc-dc converters (e.g., [70]), this is not usually done, as the output power of a frequency multiplier inverter is inherently low relative to the needed device ratings. However, here we utilize frequency multiplication as an *additional* operating mode of the inverter (and/or rectifier), for reduced output power conditions. In this

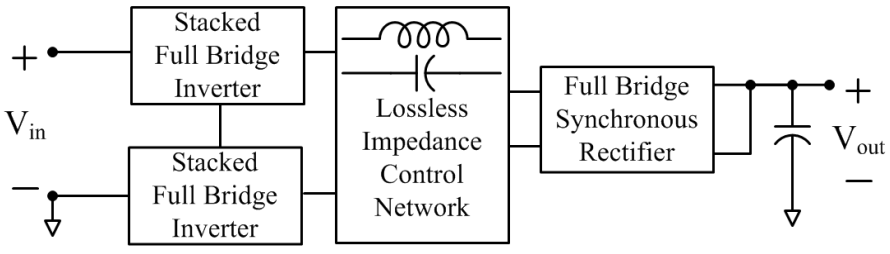


Figure 3-1: Architecture of the proposed Impedance Control Network (ICN) resonant converter as pursued here. A plurality of phase-shifted inverters and one or more rectifiers interact through a lossless impedance control network that ensures desirable operating points for the inverter and rectifier blocks.

context, frequency multiplication can be used to *extend* the efficient operating range of a converter and improve its performance for low powers [35,71].

To illustrate the novel strategy we pursue, consider operation of the stacked-bridge inverter of Figure 3-2. This splits the input voltage V_{in} in two, with each half bridge ideally provided with a voltage $V_{DC} = 0.5 \cdot V_{in}$. By controlling *the fundamental switching period* T_A of the constituent half-bridge inverters, in addition to the duty ratios D_1 and D_2 of the bottom and top half-bridge inverters, and the time delay Δt between them, we can synthesize inverter output waveforms $v_{out}(t)$ that have desirable characteristics at a frequency f_0 (operating period $T_0 = 1/f_0$) needed to drive the load network. The inverter system can be controlled to synthesize an output frequency f_0 that is a *multiple* of the fundamental inverter switching frequency $f_A = 1/T_A$ (i.e., such that the stacked-bridge inverter is operated as a *frequency multiplier).* Moreover, through proper selection of operating points, we can vary the multiplier ratio, providing "gear shifts" in operation, while preserving soft switching and other desired operating characteristics.

Consider Fourier analysis of the inverter of Figure 3-2. If one of the constituent half-bridges is operated with duty ratio D_1 and period T_A with an even operating waveform, the half-bridge output voltage waveform can be expressed as the following Fourier series:

$$v_{x1}(t) = D_1 V_{DC} + \sum_{n}^{\infty} \frac{2V_{DC}}{\pi n} \sin(n\pi D_1) \cos(\frac{2\pi n t}{T_A}) \tag{3.1}$$

where V_{DC} is the voltage across the half-bridge and n is the harmonic.

Figure 3-3 shows the amplitude of the fundamental of this waveform and its harmonics as a function of duty ratio (normalized to the maximum of $2 \cdot V_{DC}/\pi$). We can select duty ratios,

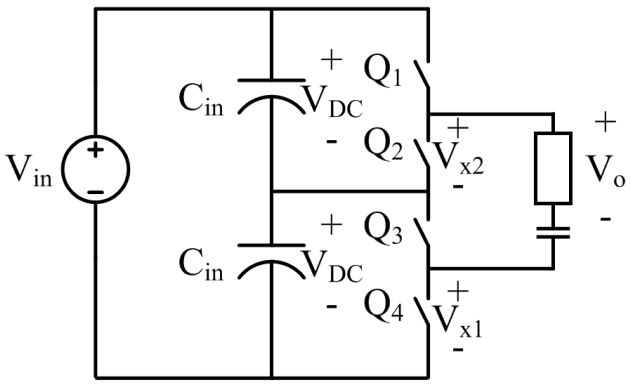


Figure 3-2: A stacked-bridge inverter. The total bus voltage V_{in} is split in two (nominally) equal values of $V_{DC} = 0.5\ V_{in}$, with voltage balance maintained passively or through active control. The inverter output voltage is V_{out}, shown across an element representing the input to the load network.

delays and switching periods of the half-bridge inverters to develop different operating modes. Operating the inverters at the desired output frequency ($T_A = T_0$), with a delay of half a cycle $\Delta t = 0.5 \cdot T_A$ between the half bridges and with identical duty ratios $D_1 = D_2 = 0.5$, we get the output waveform v_o of Figure 3-4(a). This is the normal inverter operation one would utilize, which we term "fundamental" mode operation. However, if we operate the half-bridge inverters at a fundamental frequency that is half that of the desired output ($T_A = 2 \cdot T_0$), set $D_1 = 0.25$, $D_2 = 0.75$, and set $\Delta t = 0.75 \cdot T_A$, we get a "frequency doubler" mode that yields output waveform v_o of Figure 3-4(b). Figure 3-5 shows the proposed gate drive signals to generate the waveform of Figure

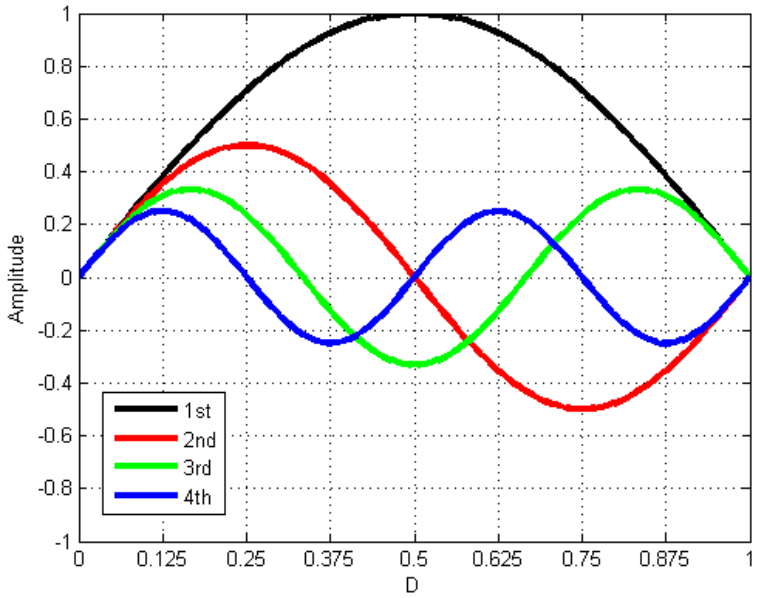
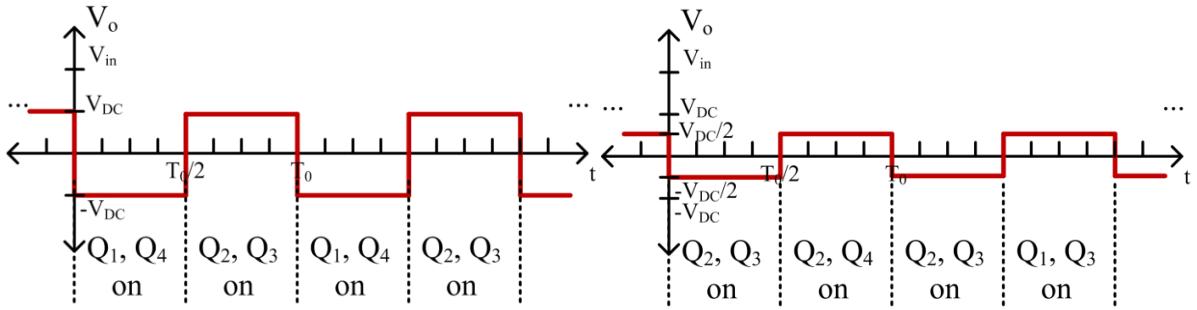


Figure 3-3: Normalized Fourier amplitudes of a square wave with duty ratio D.



(a) (b)

Figure 3-4: Output voltage waveforms of the stacked-bridge inverter of Figure 3-2. (a) Operation in fundamental mode, where each half-bridge inverter switches $f_0 = 1/T_0$ and at a 50% duty ratio. (b) Operation in VFX mode. In this case the half-bridge inverters each operate at *half* that of the desired output frequency with one half bridge having duty ratio of 25% and the second half bridge having duty ratio of 75%. The net output voltage is at the same frequency as the fundamental mode, but provides half the output voltage, while the individual transistors switch at half the rate as in fundamental mode.

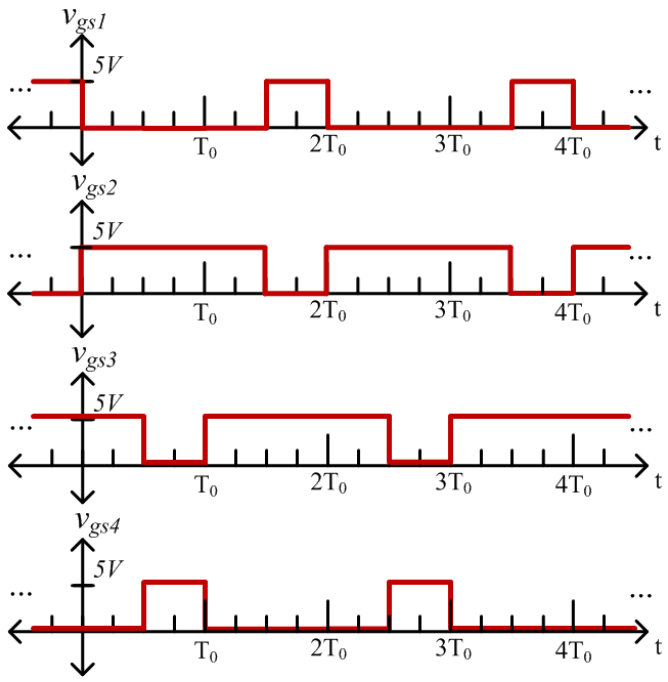


Figure 3-5: One example implementation of the gate drive signals for the stacked inverter when operated in "frequency doubler" mode or "VFX" mode. In this mode, the duty cycle of the devices is either 25% or 75% and switching period is $2T_0$.

3-4(b). This operating point cancels the fundamental of the half-bridge waveforms and reinforces their second harmonic (see Figure 3-3). Consequently, the output waveform has the same frequency f_0 as the previous case, but *half* the output amplitude, and with the individual transistors switching at half the rate (reducing gating and switching loss). The current from the loading network provides soft switching opportunities for the individual transistors at each transition, just as in fundamental mode. Operated in this manner, the inverter acts as a frequency multiplier with varying multiplier ratios (1x and 2x in this case). The flexibility provided by this second "VFX" mode of operation is valuable for efficiently spanning wide ranges in power and voltage, while preserving other system operating characteristics.

The VFX technique is not limited to the inverter stage. It can also be applied to the rectifier stage. Consider the full bridge rectifier of Figure 3-6(a). In fundamental mode, the voltage at the input to the rectifier will have the waveform of Figure 3-6 (b), which alternates from $+V_{out}$ to $-V_{out}$. The switches have been labeled so that when the gate signals of Figure 3-5 are applied to them, the voltage at the input to the rectifier will now have the waveform of Figure 3-6 (c), which alternates from $+V_{out}/2$ to $-V_{out}/2$.

Depending on the desired power level given a certain input voltage, any number of combination of stages and operating modes can be employed as will be discussed in the next section.

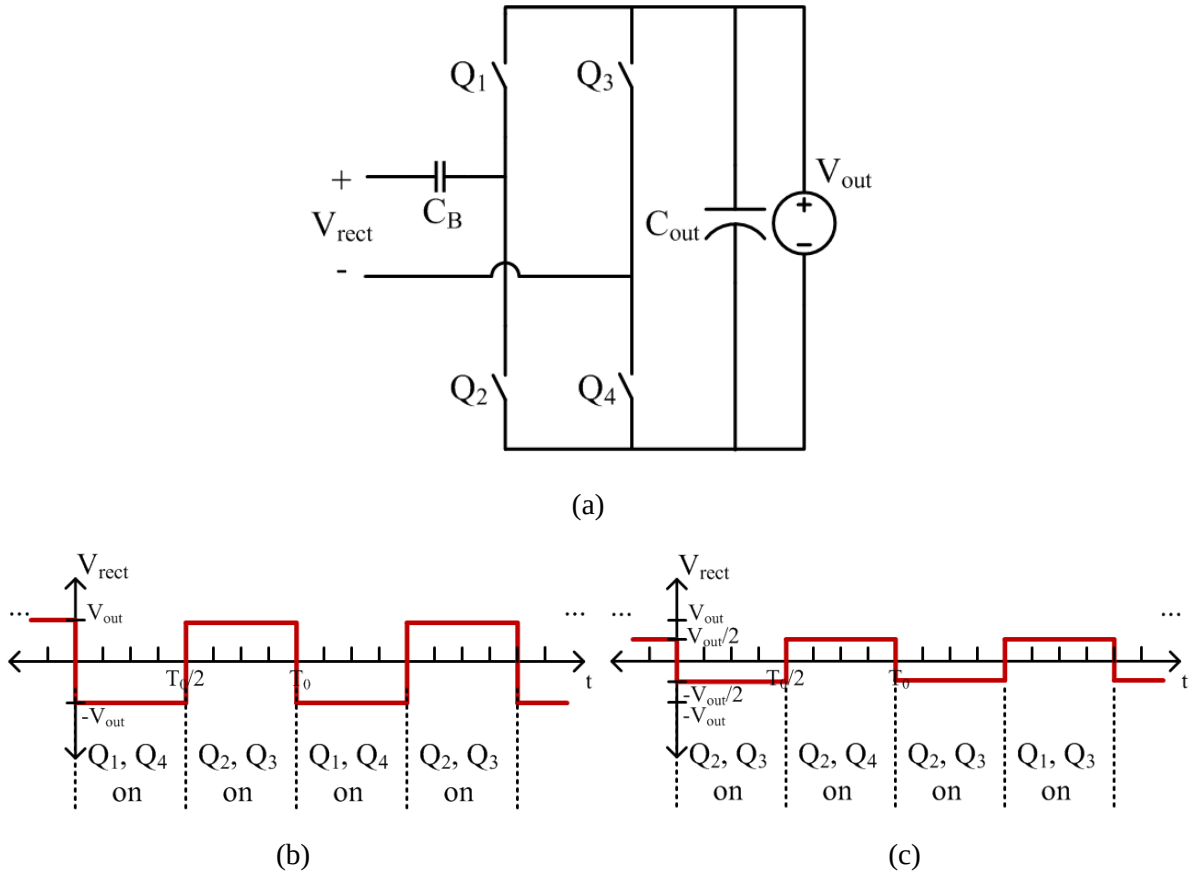


Figure 3-6: (a) A full bridge rectifier. The voltage at the input to the rectifier, V_{rect}, is shaped by the active devices and depends on operating mode. (b) Operation in fundamental mode, where each half-bridge switches at $f_0 = 1/T_0$ and at a 50% duty ratio. (c) Operation in VFX mode. In this case the half-bridges each operate at *half* that of the desired output frequency with one half-bridge having duty ratio of 25% and the second half-bridge having duty ratio of 75%. The net rectifier voltage is at the same frequency as the fundamental mode, but provides half the voltage amplitude, while the individual transistors switch at half the rate as in fundamental mode.

3.2 Application of the Frequency Multiplier Technique

Consider application of this technique on the inverter stage of the ICN converter, shown again in Figure 3-7. The ICN resonant converter uses two stacked-bridge inverters across the input to deliver two inverter output voltages. This circuit can be operated either in fundamental mode or in frequency-multiplier mode for each inverter. Because in frequency-multiplier mode the fundamental components of the individual half-bridge inverters are cancelled at the transformer inputs, the transformers and ICN components see only the net output drive frequency f_0 (= $1/T_0$) and harmonics, enabling component size and core loss to be minimized. There is no adjustment needed in the components between operating modes. When operated in VFX mode, the output power is lowered. To understand this, one must revisit

the power curve. Shown in Figure 3-8 is the power curve with key operating points highlighted. As discussed in the previous chapter, the converter is designed to have low variance in output power across the input voltage range of 260 V to 410 V as shown in the red portion of the curve of Figure 3-8. When operated in VFX mode, the ICN sees an effective input voltage that is reduced by a factor of two and will deliver power as if the input voltage range was from 130 V to 205 V even though the converter is still operating with an input voltage between 260 V and 410 V. From 130 V to 205 V, the power curve is lower, and so the ICN converter delivers a lower power, shown as the blue portion of the curve of Figure 3-8 referred over to the input voltage operating range. A benefit of operating in VFX mode is that the

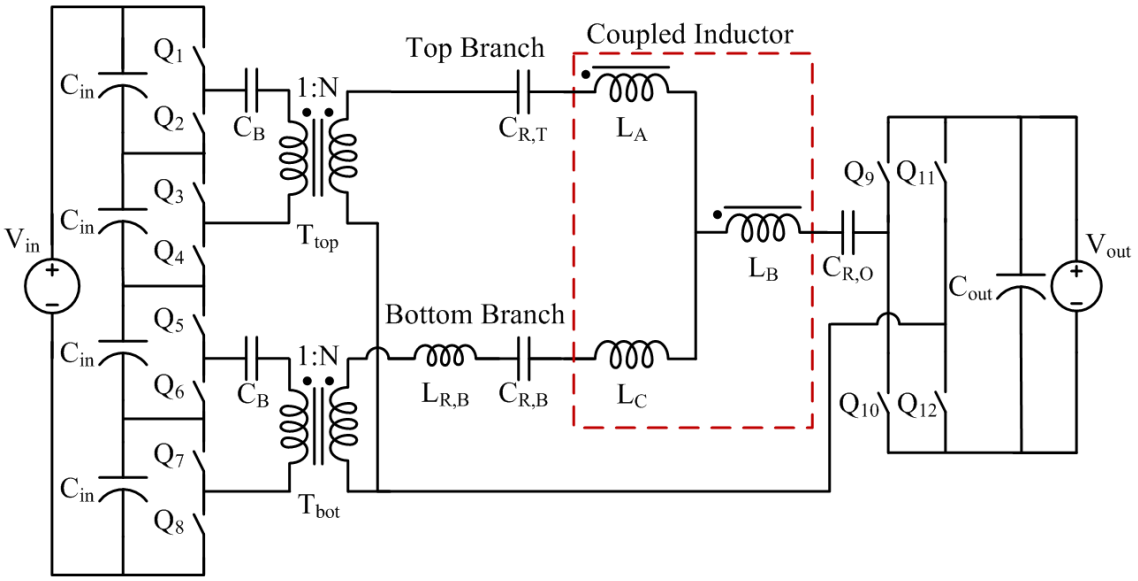


Figure 3-7: Proposed implementation of the ICN converter. The ICN incorporates harmonic filtering through the use of resonant tanks as well as two equal but opposite impedances. This structure contains four magnetic structures - two transformers, a coupled inductor (indicated by the red-dashed box), and a resonant inductor.

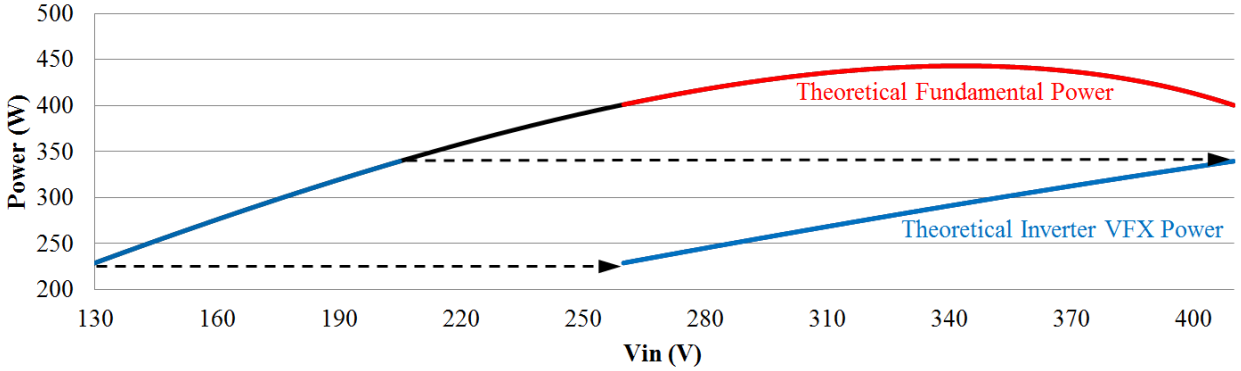


Figure 3-8: Variation in output power as a function of input voltage for the ICN converter operated with the phase-shift between the two inverters controlled to provide zero effective susceptance of the inverters. Converter power varies only minimally over the voltage range of fundamental operation (i.e., 260 V – 410 V). During VFX mode on the inverter, the transformation stage sees half the input voltage and therefore the additional power capabilities are also highlighted.

input voltage to the transformer is lower so core loss can be reduced. As with the fundamental mode, the converter is designed and operated to maintain zero voltage switching for all switch transitions so that efficiency can be kept high. To reach power levels even further below the curve of Figure 3-8, one can still employ the burst mode scheme of Chapter 2 and/or another operating mode using VFX can be used.

It can be seen from Figure 3-8, that the theoretical VFX power is not flat across the input voltage range. In addition to operating the inverters in VFX mode, the rectifier can be simultaneously operated in VFX mode. This has the effect of halving the output voltage. The entire output power profile will now be adjusted based on:

$$P_{out,VFX} = \frac{N\frac{V_{\text{in}}}{2}\sqrt{16\frac{V_{out}}{2}^2 - N^2\frac{V_{in}}{2}^2}}{\pi^2 X}. \tag{3.2}$$

The major change is that now both the input voltage and the output voltage are effectively halved. This new VFX output power is compared to the original fundamental power in Figure 3-9 with a turns ratio, *N*, of 0.1, an output voltage of 12, and an impedance, X, of 0.2639. While the original power capability delivered power around 400 W, the new power capability delivers around 100 W when VFX is applied to both the inverter and the rectifier stages. Unlike when VFX is applied to the inverter alone, the power curve is fairly flat across the input voltage range when it is applied to the inverter and rectifier simultaneously.

Applying VFX to the rectifier alone will also reshape the power curve. Instead of lowering the curve completely, the curve will "shrink" with input voltage (see Figure 3-10). For this particular set of converter specifications (e.g., input voltage range, turns ratio, and impedance), applying VFX to the rectifier alone will actually yield no power delivery when the input voltage is above 260 V. This is probably not a very useful mode of operation for this particular application.

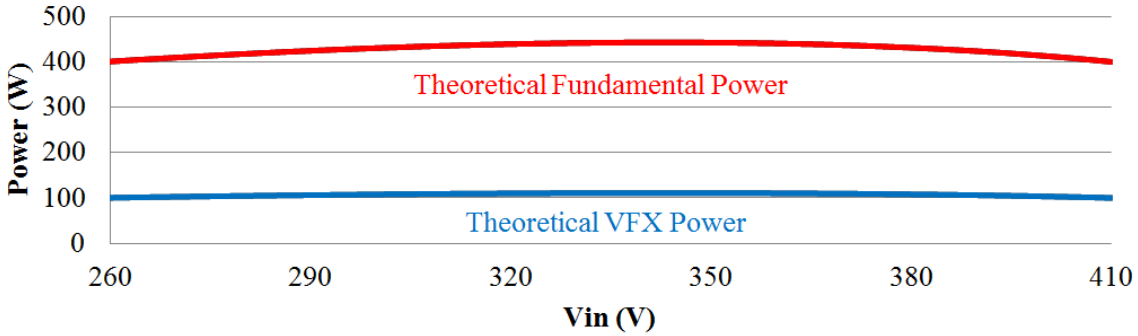


Figure 3-9: Variation in output power as a function of input voltage for the ICN converter operated with the phase-shift between the two inverters controlled to provide zero effective susceptance of the inverters. Converter power varies only minimally over the voltage range of fundamental operation (i.e., 260 V – 410 V). During VFX mode on both the inverter and the rectifier, the output power profile is lowered. The additional power capability, approximately a quarter of the original, is highlighted.

To understand the effect that VFX has on the power equation, turn to Figure 3-10. It can be seen that applying VFX to just the inverter stage will elongate the original fundamental power curve with respect to input voltage without changing the amplitude. Applying VFX to just the rectifier will shrink the original fundamental power curve with respect to input voltage and lower its amplitude. Applying VFX to both inverter and rectifier stages will have the effect of reducing the original fundamental power curve amplitude. This particular curve can also be seen as a combination of the two effects seen by applying VFX to each stage individually. For example, taking the purple curve of Figure 3-10 and elongating it with respect to the input voltage will also yield the green curve of Figure 3-10.

3.2.1 Simulation of the Proposed Frequency Multiplier Method

The simulations used in Chapter 2 can also be used to understand how the ICN converter operates in VFX mode. To go from fundamental mode to VFX mode in the inverter stage, only the drive signals for the inverter switching devices must be modified. One of the modifications is that the switching frequency is reduced by a factor of two (e.g., from 500 kHz in fundamental mode to 250 kHz in VFX mode). Another modification is that the calculation for the phase shift must be adjusted because now the apparent voltage is halved. The following two equations compare the phase shifts between the two modes:

$$\Delta_{\text{fundamental}} = \cos^{-1}\left(\frac{NV_{\text{in}}}{4V_{\text{out}}}\right) \tag{3.3}$$

$$\Delta_{\text{VFX}} = \cos^{-1}\left(\frac{N\frac{V_{in}}{2}}{4V_{\text{out}}}\right) \tag{3.4}$$

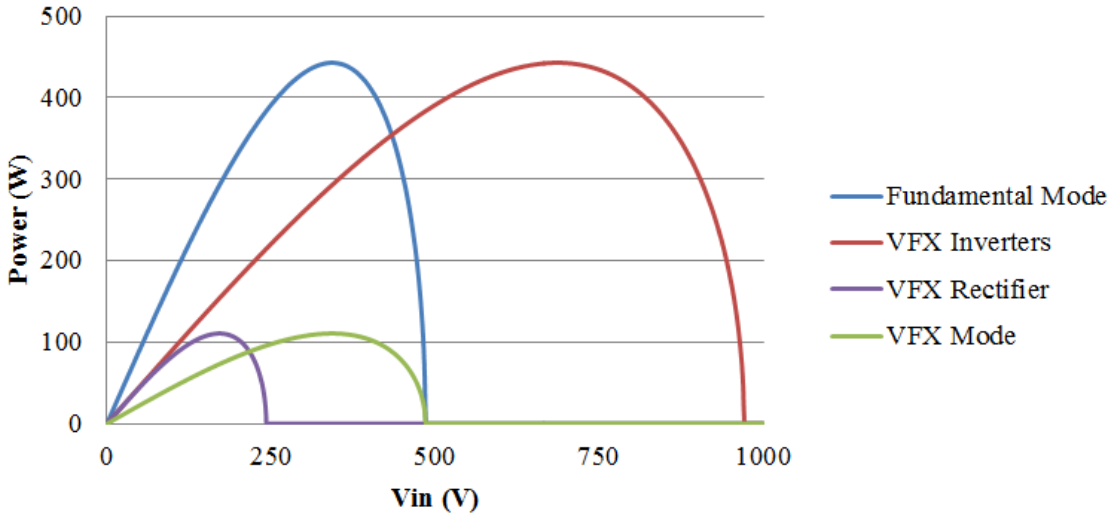


Figure 3-10: Variation in output power as a function of input voltage for the ICN converter operated under four different modes: fundamental mode (blue curve), VFX mode applied to the inverters (red curve), VFX mode applied to the rectifier (purple curve), and VFX applied to both inverters and rectifier (green curve).

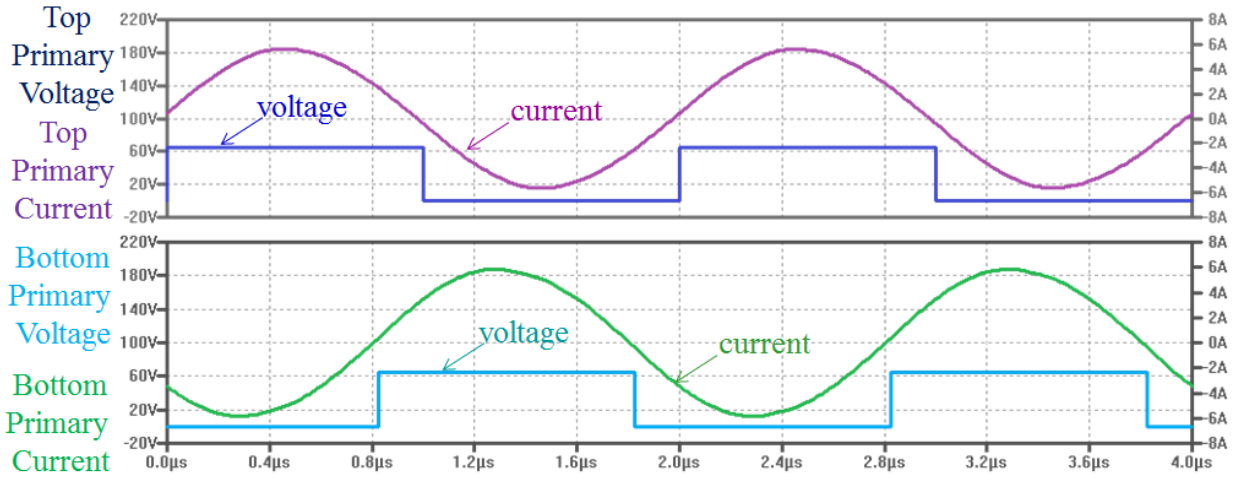
These phase shifts are in radians. When converting from radians to seconds, the fundamental switching period should be used for either operating mode.

In fundamental mode, all inverter switches had a 50% duty ratio (not accounting for dead time) but in VFX mode, the inverter switches will have either 25% duty ratio or 75% duty ratio. In our implementation, the top and bottom switch of each inverter have a 25% duty ratio (e.g., Q_1 and Q_4 of Figure 3-7) and the middle two switches have a duty ratio of 75% (e.g., Q_2 and Q_3 of Figure 3-7).

Figure 3-11 shows simulation results from an ideal and lossless model of the converter when the inverters are operated in VFX mode. The details of the simulation can be found in Appendix C. As was seen in Chapter 2, the current is sinusoidal and in phase with the voltage. To understand how VFX mode compares to fundamental mode, turn to the waveforms of Figure 3-12. It can be seen that the VFX voltage is half the amplitude of the fundamental voltage while the current has a higher amplitude. It can also be seen that the phase shift between the inverters is higher for the VFX mode, which is consistent with the theory that a lower input voltage has a higher phase shift (see Figure 2-7). For all waveforms, the current is in phase with the voltage

As demonstrated in Chapter 2, a simulation approximating the components and loss of the final prototype generated waveforms that matched well with the waveforms seen on the bench. This simulation can be found in Appendix C and can be adjusted to operate the inverters in VFX mode (also included in Appendix C). The results of the simulations for a practical design are shown in Figure 3-13. For these simulations, it can be seen that the current is fairly sinusoidal for an input voltage of 260 V as well as 410 V. The current is mostly in phase with the voltage for all operating points. In simulation, the converter does appear to have near ZVS of the top inverter when the inverters are operated under VFX mode with an input of 410 V as the voltage slowly rises up but starts to level out before the full amplitude is reached.

This same simulation can also be adjusted to simultaneously operate the rectifier in VFX mode. The results of this simulation are shown in Figure 3-14. For this simulation, the phase shift between the inverters is the same as in fundamental mode (because both input and output voltages are halved together so the ratio does not change) and the rectifier is operated to have a phase shift that is halfway between the two inverters. As mentioned before, the output power is about a quarter of the power delivered in fundamental mode. Because the power is lower, so too is the inverter current and it can be seen that the top inverter loses ZVS. This will negatively impact the efficiency. It is unclear if delivering less than a quarter of the rated power using this particular mode of VFX is more efficient than burst mode and will heavily depend on the switching loss mechanisms.



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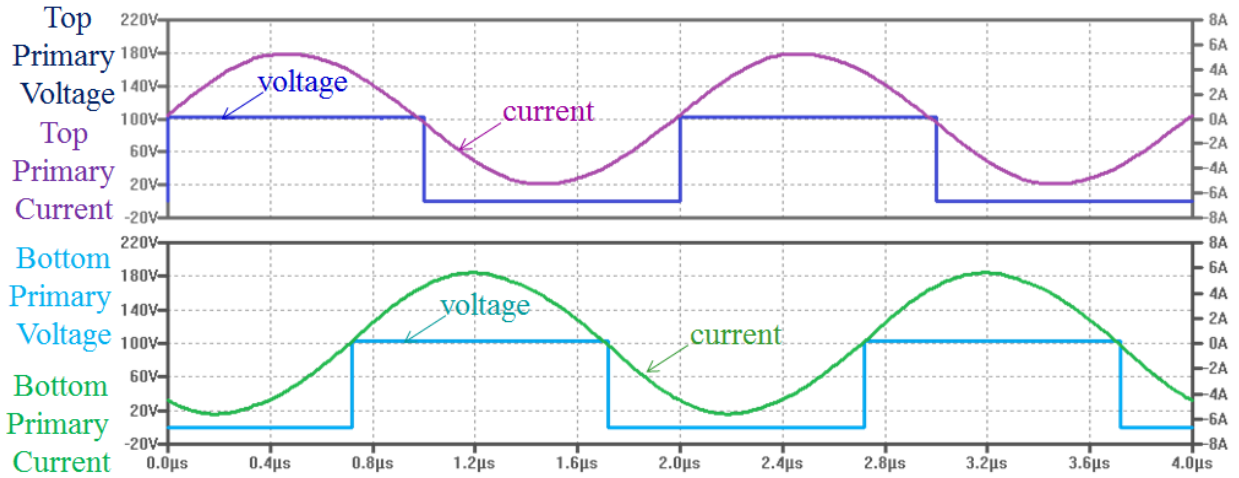
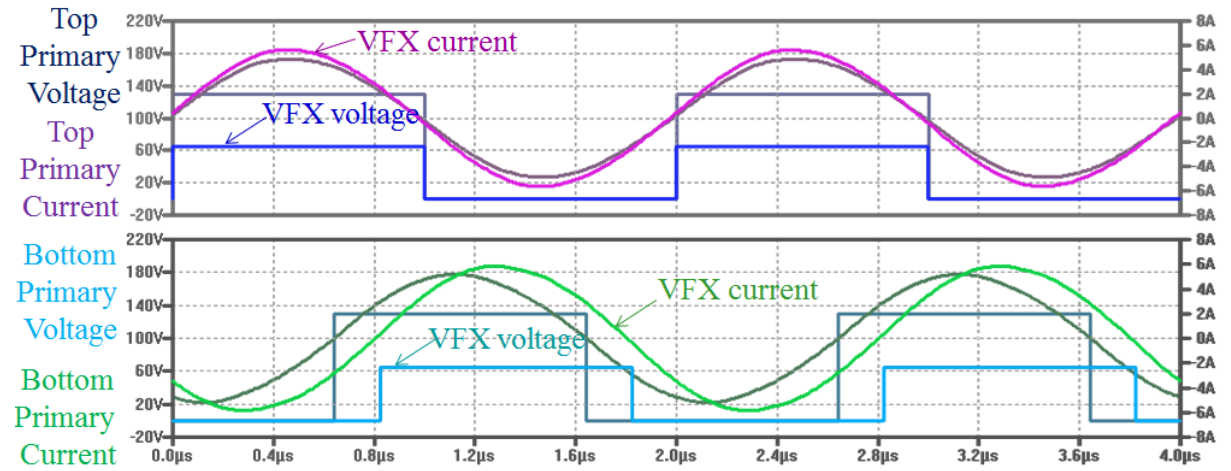


(b)

Figure 3-11: Simulation results showing ZVS and ZCS of a lossless ICN resonant converter when the inverters are operated in VFX mode with an input voltage of (a) 260 V and (b) 410 V. The output voltage was 12 V, and the output power was 400 W. For all plots, the top pane shows the primary voltage and current for the top transformer and the bottom pane shows the primary voltage and current for the bottom transformer. For all plots, the current is sinusoidal and crosses zero almost simultaneously with the square wave voltage transitions.



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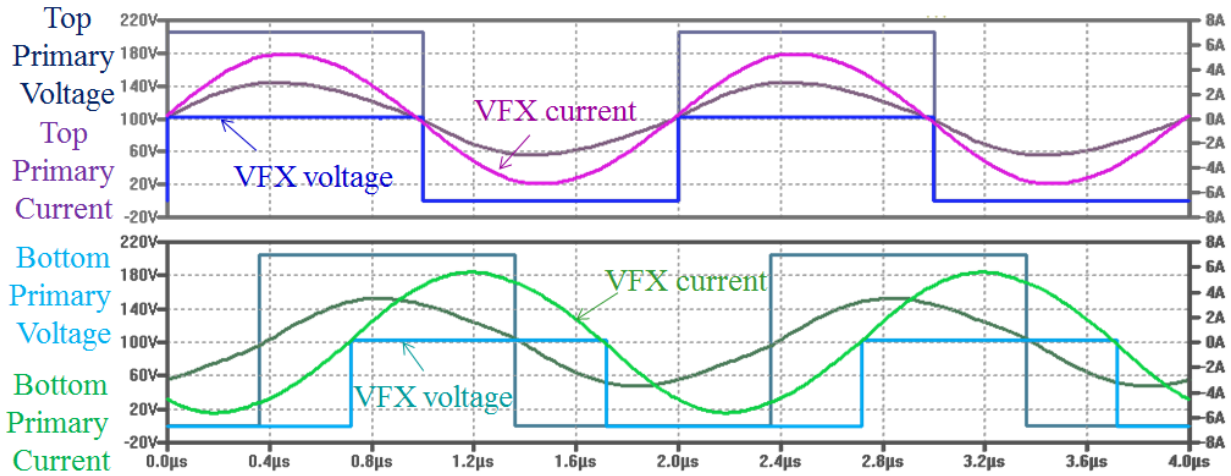
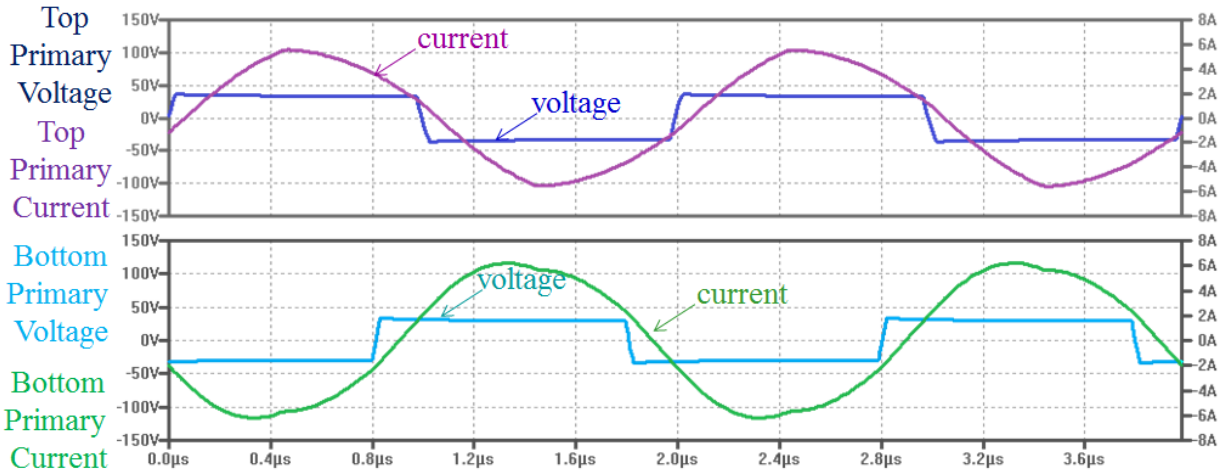
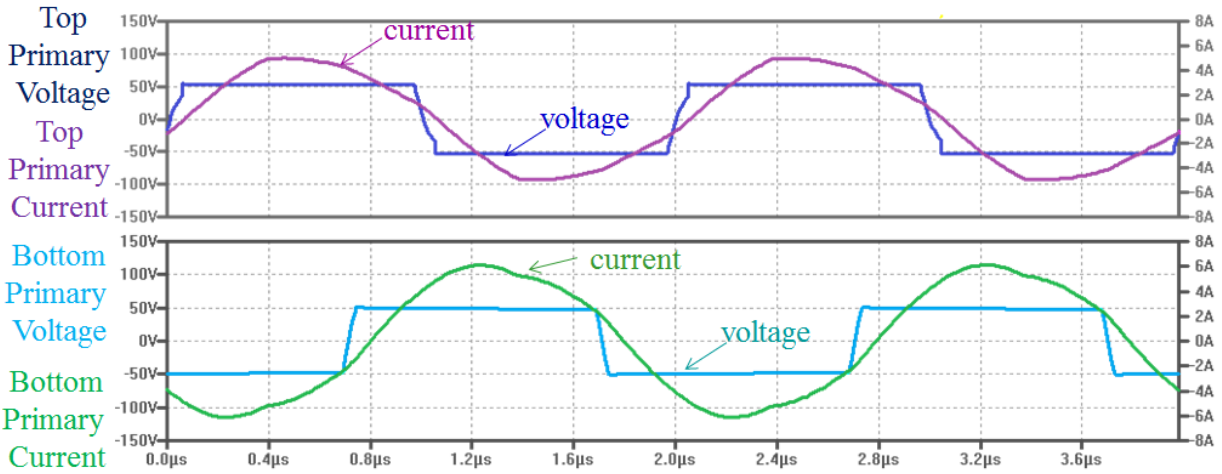


(b)

Figure 3-12: Simulation results comparing the operation of a lossless ICN resonant converter in fundamental and inverter VFX modes with an input voltage of (a) 260 V and (b) 410 V. The output voltage was 12 V, and the output power was 400 W. For all plots, the top pane shows the primary voltage and current for the top transformer and the bottom pane shows the primary voltage and current for the bottom transformer. The brighter waveforms are from VFX operation while the darker waveforms are for fundamental operation.

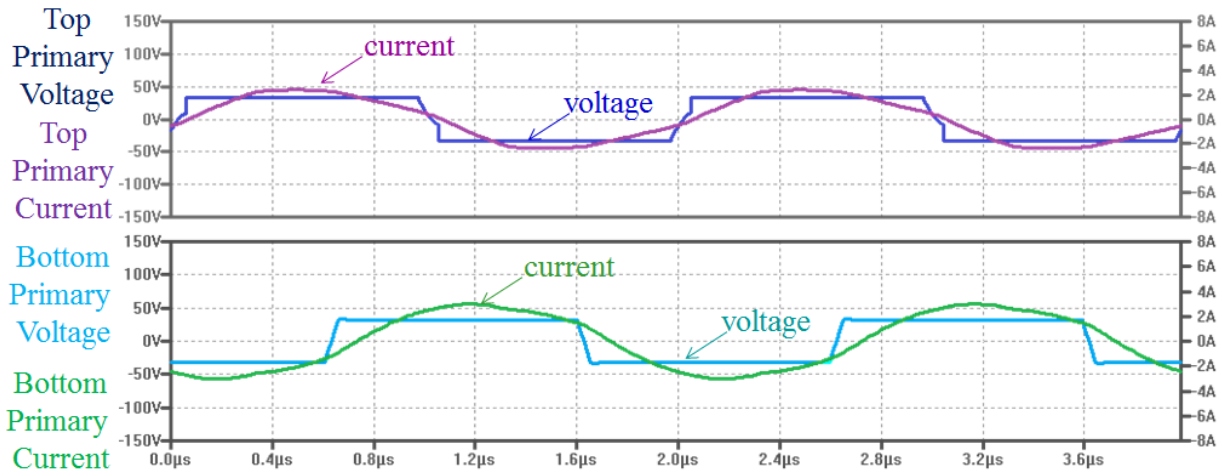


(a)

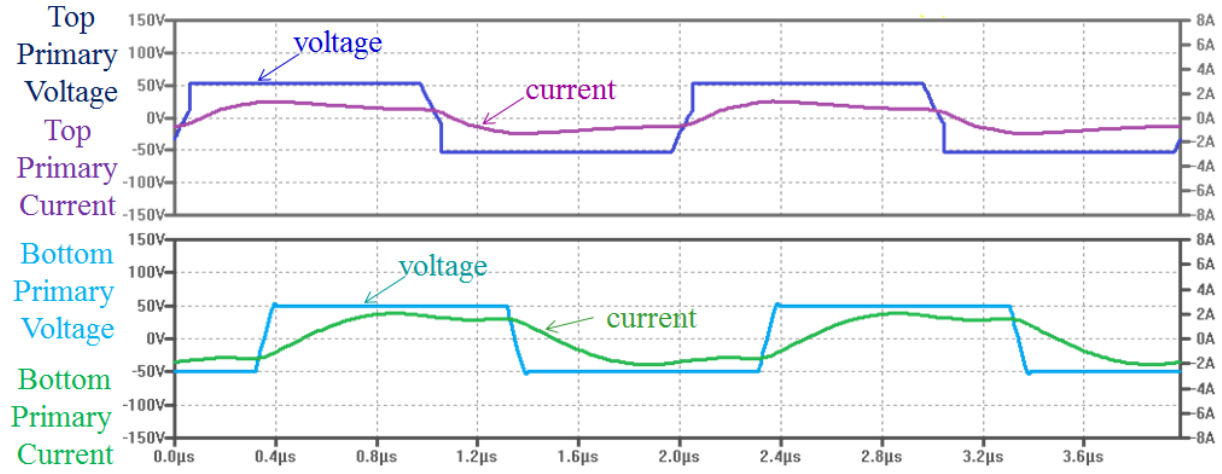


(b)

Figure 3-13: Simulation results of a more practical ICN resonant converter when the inverters are operated in VFX mode with an input voltage of (a) 260 V and (b) 410 V. The output voltage was 12 V. For all plots, the top pane shows the primary voltage and current for the top transformer and the bottom pane shows the primary voltage and current for the bottom transformer.



(a)



(b)

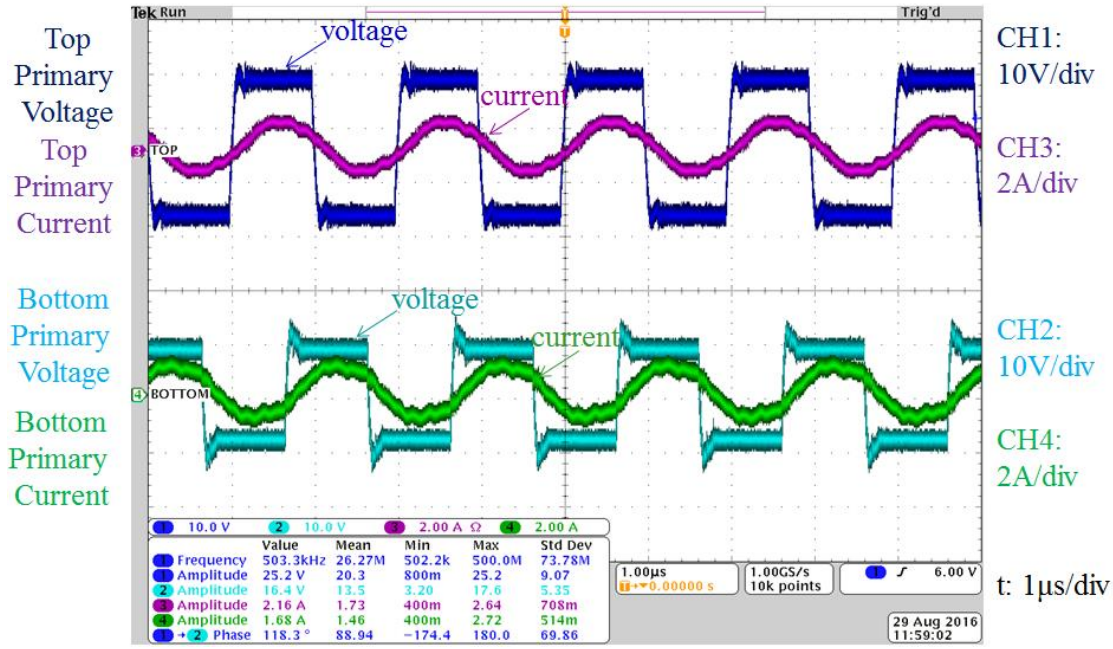
Figure 3-14: Simulation results of a more practical ICN resonant converter when both the inverters and the rectifier are operated in VFX mode with an input voltage of (a) 260 V and (b) 410 V. The output voltage was 12 V, and the output power was approximately 90 W. For all plots, the top pane shows the primary voltage and current for the top transformer and the bottom pane shows the primary voltage and current for the bottom transformer.

3.2.2 Experimental Application

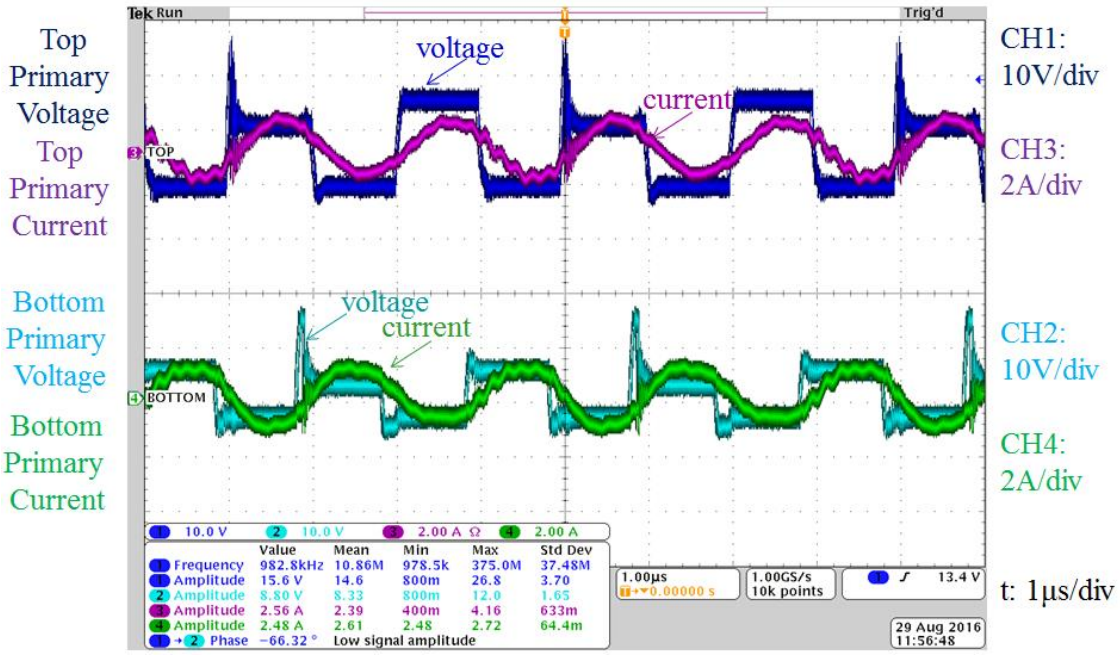
Consider the waveforms of Figure 3-15(a) when the prototype of Chapter 2 (see Figure 2-25) is operated in fundamental mode with an input voltage of 40 V, and output voltage of 2 V, a phase shift of 661 ns (or 33.1% of the period) between the two inverters, 372 ns (or 18.6% of the period) between the leading inverter and the rectifier, and a dead-time of 90 ns for both inverter and rectifier half-bridges. The voltage at each transformer primary is a square wave, and the current into each transformer primary is a sinusoidal waveform that is in phase with the voltage waveform. The amplitude of the top transformer's primary voltage is 25.2 V and the amplitude of the bottom transformer's primary voltage is 16.4 V. At 10V/div, the top voltage waveform spans almost three divisions and the bottom voltage waveform spans almost two divisions. The top transformer primary current has an amplitude of 2.16 A and the bottom transformer primary current has an amplitude of 1.68 A.

VFX can be applied to the experimental prototype by simply changing the half-bridge drive signals with no adjustments made to the physical components. Figure 3-15(b) shows the same primary voltage and primary current waveforms, but now when the converter is operated in VFX mode. The input voltage is still 40 V and the output voltage is 2 V. The phase shift between the two inverters is now 834 ns (or 41.7% of the period) and the phase shift between the leading inverter and the rectifier is 468 ns (or 23.4% of the period). The voltage waveforms are still square waves, but there is a difference in amplitude between each cycle. In general, the amplitude is lower than when operated in fundamental mode - an amplitude of 15.6 V for the top transformer's primary voltage, and an amplitude of 8.80 V for the bottom transformer's primary voltage. At 10 V/div, the top transformer voltage spans either 1.5 divisions with smooth transitions or 1 division with a large spike at the rising edge. The bottom transformer voltage spans about 1 division with smooth transitions or half a division with a large spike at the rising edge. For all cycles, the current is fairly sinusoidal and mostly in phase with the voltage. The amplitude is slightly higher for the current in VFX mode – 2.56 A for the top transformer primary and 2.48 A for the bottom transformer primary. As predicted by theory, the amplitude of the voltage is lower, by approximately a factor of two between fundamental mode and VFX and the current is slightly higher when operated in VFX mode. Unfortunately, the experimental implementation of VFX does exhibit non-idealities.

To understand what causes these non-idealities, we focus in on the gate drive signal. Of particular concern is the gate drive signal v_{gs3} of Figure 3-5 which should stay on for 75% of the inverter switch period. However, inspection of this particular gate drive signal (as seen before the driver) of Figure 3-16 shows that after 25% of the cycle, the signal goes to zero momentarily. The cause for this shutdown is due to the way the microprocessor handles the control signals. The converter operating frequency is still set to 502.5 kHz so at the beginning of each cycle, the microcontroller conservatively sets all high-side signals to zero (to avoid overshoot). This causes an issue with the high-side signals that



(a)



(b)

Figure 3-15: Experimental waveforms of the ICN resonant converter prototype with an input voltage of 40 V and an output voltage of 2 V when operated in (a) fundamental mode and (b) VFX mode for the inverters. For all plots, the top set of waveforms shows the voltage across the primary of the top transformer and the current into the primary. The second set shows the voltage across the primary of the bottom transformer and the current into the primary.

have double the switching period and are intended to remain on from one high frequency cycle to the next (i.e., v_{gs3} for Q_3 and v_{gs7} for Q_7). Zooming in on that particular turn off instance (shown in Figure 3-17), it can be seen that the converter has enough current so that Q_3 can turn off at ZVS but the quick turn on again occurs when there is insufficient current to ensure ZVS. This presents two major issues. The first is that as Q_3 (and similarly Q_7) turns off, there is a corresponding rise in the voltage across the transformer, forming a large spike. This results in an imbalance in the amplitude of the transformer voltage between cycles. The second issue is that as Q_3 (and similarly Q_7) turns back on, this is a hard-switched transition. Because this occurs every other cycle, this represents a significant amount of loss and the overall performance of the converter is much lower. At this operating point, the converter delivers 4.6 W at an efficiency of 79%. Under fundamental mode operation, with the input voltage at 40 V and the output voltage at 2 V, the converter could deliver 9.2 W at an efficiency of 88.7%. Bursting the converter on for 100 cycles and off for another 100 cycles can deliver 4.5 W at an efficiency of 88.2%, which is much higher than the efficiency of the VFX mode in the presence of hard-switching. This problem persists at higher voltages too. When operated with an input voltage of 160 V, an output voltage of 8 V and maintaining the same phase shift and dead-time as before, the converter delivers 72 W at an efficiency of 76.8%, while operation in burst mode gives an efficiency of 88.1% when delivering 73.8 W to the load.

3.3 Summary of the VFX Technique

This chapter presented another operating mode of the Impedance Control Network resonant converter geared toward low power operation. The technique makes use of variable frequency multiplier (VFX) inverters to reduce the effective voltage seen at the primary of each transformer and VFX rectifiers to reduce the voltage seen at the rectifier. It was shown in on an experimental prototype that the VFX inverter technique is able to reduce the voltage at the primary of the transformer while still maintaining a current into the primary that is in phase with the voltage. The converter also delivers a much lower power, approximately 50% what it would in the regular operation presented in Chapter 2. Unfortunately, the particular implementation of the control scheme causes two inverter devices to experience a hard-switched transition every other cycle. VFX can be a promising technique, but due to issues with the microcontroller, the efficiency advantages of the VFX method could not be fully validated for this prototype. The technique has been successfully applied to other converters to offer a different mode of operation when the input voltage varies [35] rather than for a variation in output power.

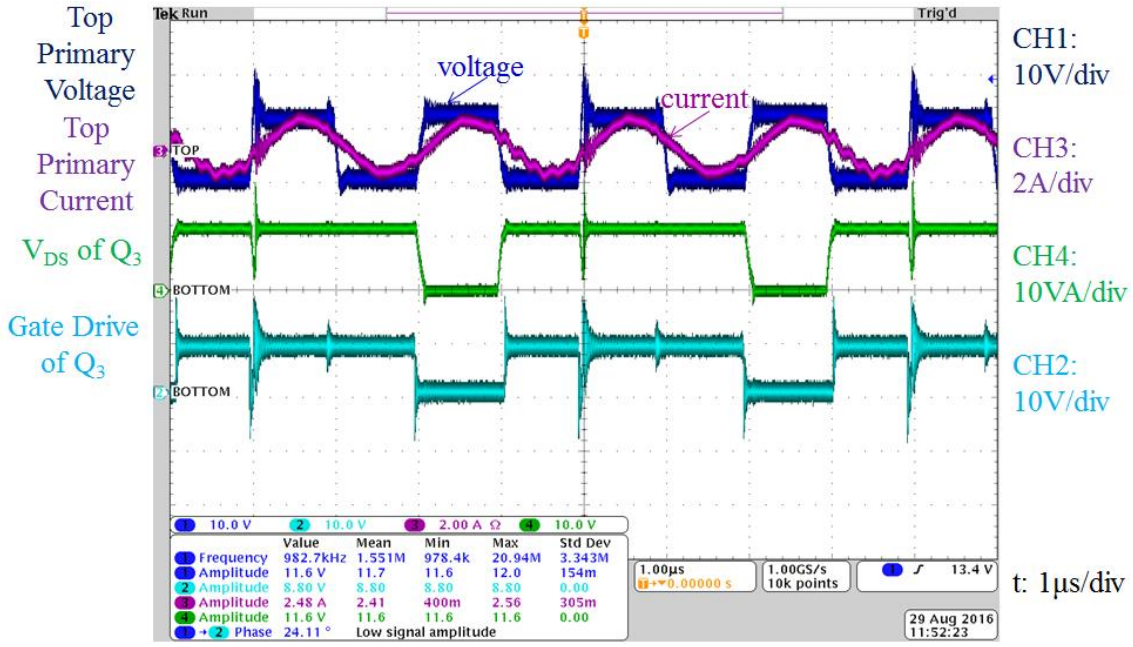


Figure 3-16: Experimental waveforms of the ICN resonant converter prototype with an input voltage of 40 V and an output voltage of 2 V when operated in VFX mode. The top set of waveforms shows the voltage across the primary of the top transformer and the current into the primary. The middle (green) waveform shows the voltage across Q_3 of Figure 3-7. The last (cyan) waveform shows the voltage into the driver for Q_3.

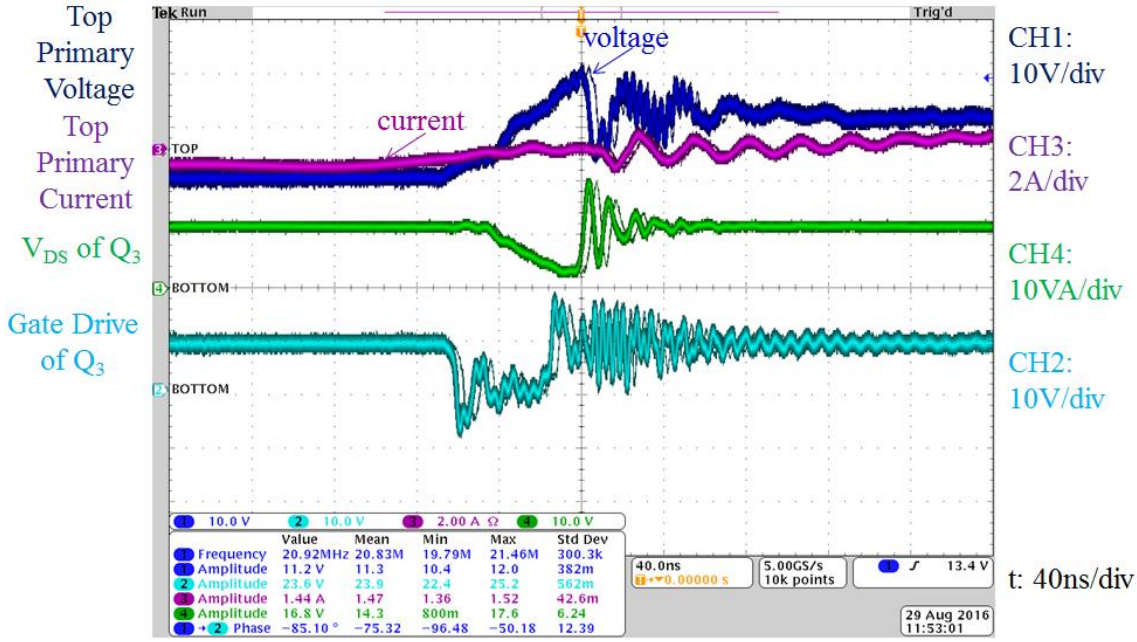


Figure 3-17: Experimental waveforms of the ICN resonant converter prototype with an input voltage of 40 V and an output voltage of 2 V when operated in VFX mode. The top set of waveforms shows the voltage across the primary of the top transformer and the current into the primary. The middle (green) waveform shows the voltage across Q_3 of Figure 3-7. The last (cyan) waveform shows the voltage into the driver for Q_3.

Chapter 4

Reconfigurable Double Stacked Active Bridge Converter Theory

As discussed in Chapter 1, the Dual Active Bridge (DAB) converter (shown again in Figure 4-1(a)) has received much attention due to its compact design that can achieve high efficiency at nominal operating points [25,26]. Unfortunately, it can suffer losses when operated under a wide voltage or power operating range as zero-voltage switching (ZVS) is lost and core loss becomes a dominant loss mechanism. Much effort has been applied to improve the performance of the DAB converter, particularly at low power. The governing equation for the output power can be expressed as

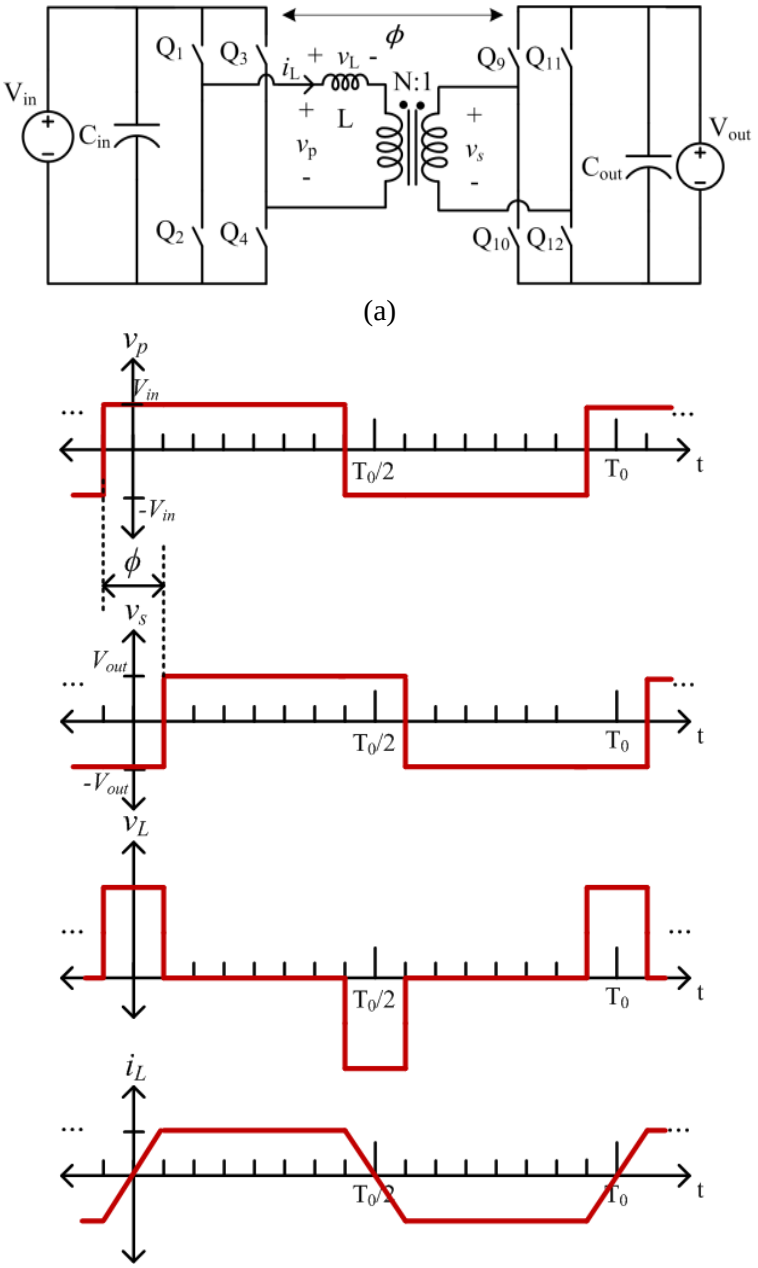
$$P_{out} = \frac{V_p V_s N}{2\pi f_s L}\phi(1 - \frac{\phi}{\pi}) \tag{4.1}$$

where V_p is the effective primary voltage, V_s is the effective secondary voltage, N is the transformer turns ratio, f_s is the switching frequency in Hz, L is the energy transfer inductance (which is usually the transformer leakage inductance and any additional discrete inductance all referred to the primary), and ϕ is the phase shift in radians. To control power, any number of parameters can be modulated such as the switching frequency, inductance or phase shift. Sometimes, other parameters such as input and output voltage affect the power and other parameters will need to compensate for this variance.

Some propose applying software-based compensation methods to the basic DAB converter topology to shape the current waveform to improve performance at the expense of increasing the number of times a switch turns on and off during one period [72]. Other control techniques applied to the conventional DAB topology include burst mode, multi-level voltages, and/or frequency variation depending on the input-output voltage ratio and output power, but these require sophisticated control algorithms dependent on real-time circuit parameters [73,74]. Simple phase-shift control can be maintained if a dual leakage transformer is used and the frequency is varied to keep the RMS current low but this requires a very complex transformer design with multiple core components and a frequency that must be tuned depending on the operating point to yield the highest efficiency [75]. Another variant on the DAB converter is to alter the topology to enable another mode of operation, as in the case of [76] where the DAB converter can be reconfigured to operate as a flyback converter in low power conditions but under certain operating limitations.

This thesis proposes an active bridge converter that derives an efficiency benefit across the full range of powers from the topology itself and can maintain the simple phase-shift control of that shown in Figure 4-1(b). The topology can be implemented without any overly complex, multi-core transformer

structures and can be operated efficiently at a fixed frequency. An additional mode of operation provided by the topology can further reduce loss at very low powers by improving ZVS capability, reducing switching frequency (and any associated gating or switching loss), and lowering core loss without the need for a complex control algorithm.



(b)

Figure 4-1: (a) A Dual Active Bridge (DAB) converter using a full-bridge inverter and rectifier. Two bridges are phase-shifted from each other across a transformer with turns ratio, *N*, and an inductance, *L*. (b) Example operating waveforms of the DAB where the rectifier square wave voltage is phase-shifted, ϕ, after the inverter square wave. In this figure, the input voltage to output voltage ratio is equal to the transformer turns ratio, resulting in a flattop trapezoidal current.

4.1 Theory of the Proposed Architecture

At the basis of many of the active bridge converter architectures is an active inverter stage that is phase-shifted from an active rectifier stage. Traditionally, the inverter stage and rectifier stage are both active full bridges as shown in Figure 4-1(a). As the two bridges are phase-shifted from each other, a voltage appears across some inductance, which can either be a discrete inductor or the leakage inductance of the transformer, typically referred to the primary as shown in Figure 4-1(a). The bidirectional current that flows through this inductance is used to charge and discharge the intrinsic capacitance of all active switching devices. When the current is high enough, it can provide soft-switching of all devices on all transitions. A significant challenge of the traditional DAB converter is when the current is too low and there is not enough energy to fully discharge and charge the intrinsic switch capacitance. The amount of energy stored in the switch capacitance is affected by two circuit parameters – the value of the switch capacitance and the voltage across the switch. Therefore, in order to maintain or improve ZVS capability, the current available to charge and discharge the switch capacitance will need to be increased, the capacitance of the switch will have to be lowered, or the voltage across the switch will need to be lowered. The proposed topology and design choices accomplish all of these things as detailed in the following subsections.

4.1.1 Double Stacked-Bridge Inverter

A useful figure-of-merit for switch devices in soft-switched converters is the product of the resistance of the device when it is on (and conducting current) and the capacitance across the switch when it is off (and blocking voltage). This RC product for the switch quantitatively determines the switch conduction loss of the class E inverter [45], and is likely useful for comparing switches for other soft-switched topologies. This is because these two parameters affect the main switch loss mechanisms in the power stage of a converter. For high frequency converters, a low capacitance is often desirable, since the switch capacitance determines the external current requirement to transition the switch for ZVS switching and determines a component of the switching loss if hard switching is entered. On the other hand, the on-resistance is not only proportional to the switch conduction loss, but also defines the maximum current that a device can carry. So while a suite of devices may be available, a circuit designer may be limited in device selection based on these ratings and intrinsic parameters, with a lower RC product reflecting a more desirable switch. For a family of switching devices with the same voltage rating, there is a tradeoff between the on-resistance, $R_{DS,ON}$, and the output capacitance, C_{OSS}. As $R_{DS,ON}$ is lowered, the C_{OSS} will increase and vice versa as can be seen in Table 4-1 for 200V Efficient Power Conversion (EPC) enhanced gallium nitride (eGAN) FETs [77].

For a given switch technology, the figure-of-merit $R_{DS,ON}C_{OSS}$ product increases as the rated voltage increases as can be seen in Figure 4-2 for EPC eGaN devices. Down to a certain point, the performance of a device can be improved by lowering its rated voltage to the extent that a series combination of two switches each with half the rated voltage would have much better performance than a single switch with the full rating. Moreover, in some ranges one has difficulty finding switches of a desired performance class that individually have sufficient rated voltage. Consequently, many high-voltage power circuits can greatly benefit from "subdividing" large voltages such that one can use multiple lower-voltage switches. This work focuses on large-step-down conversion architectures where the input voltage is in the hundreds of volts range. The focus of this section is on the design of the inverter stage where the benefit of circuit "stacking" to reduce the voltage ratings of individual devices is expected to be the greatest; however the techniques and methodology discussed can also be applied to the rectifier stage.

Table 4-1: Typical Characteristics of 200V EPC eGaN FET switching devices as obtained from manufacturer datasheets [77]

Part Number	$R_{DS,ON}$ (mΩ) V_{GS} = 5 V	C_{OSS} (pF) V_{GS} = 0 V, V_{DS} = 100 V	Figure-of-Merit $R_{DS,ON}$ C_{OSS}
EPC2012C	70	64	4480
EPC2019	36	110	3960
EPC2010C	18	240	4320
EPC2034	10	530	5300

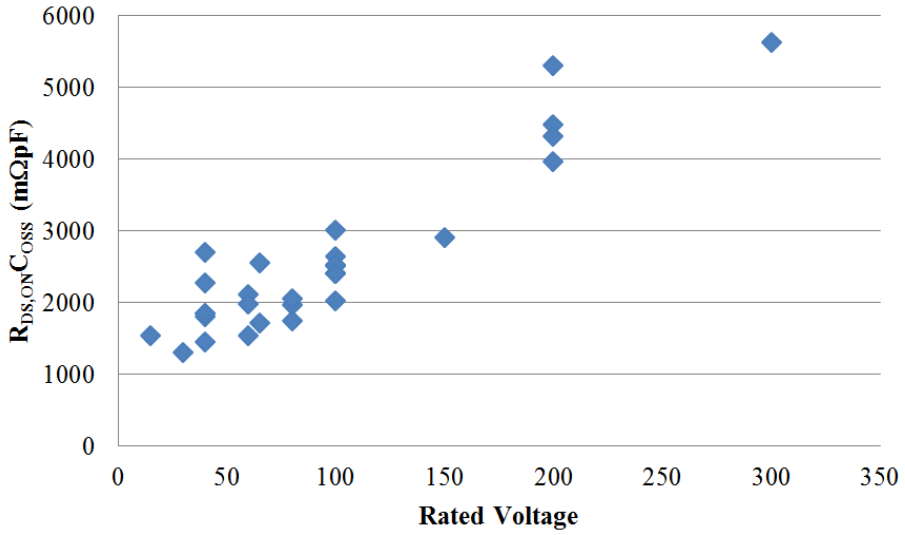
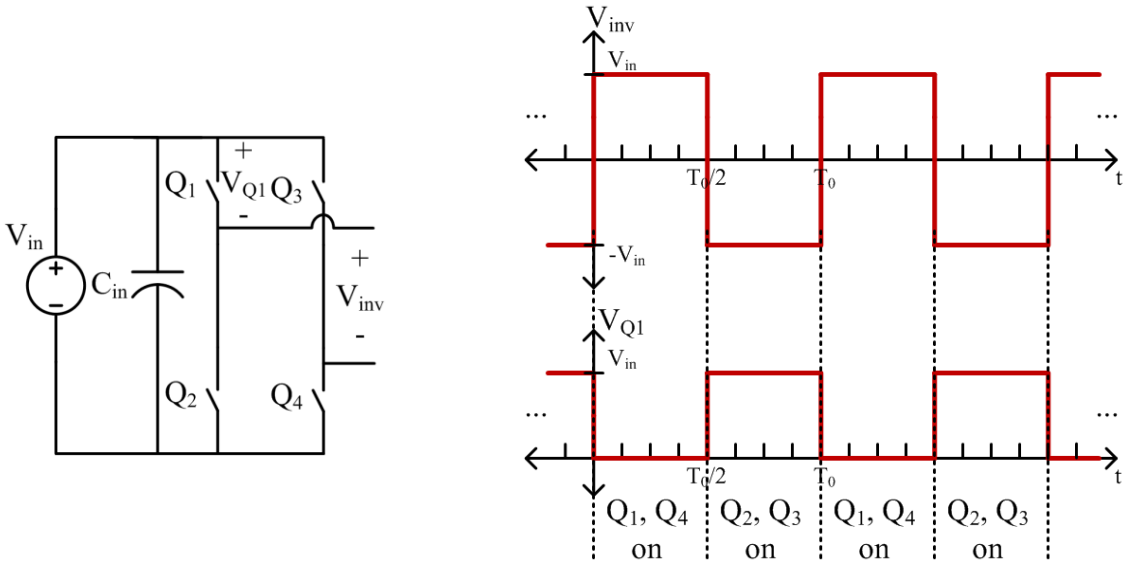


Figure 4-2: $R_{DS,ON}C_{OSS}$ figure-of-merit for various EPC eGaN devices across rated voltage. For each data point, the $R_{DS,ON}$ is the typical on-resistance in mΩ when the gate-to-source voltage is 5V. The C_{OSS} value indicated is the switch output capacitance in pF at half the rated switch voltage. Devices evaluated from manufacturer datasheets online [77] as of Aug., 2016.

First consider the full bridge inverter as shown in Figure 4-3(a). When operated in the manner shown by the waveforms of Figure 4-3(b), each switch must be able to block a voltage that is equal to the input voltage. Usually, the devices are overrated above this input voltage value to allow for some safety margin and to be able to handle transient overvoltage conditions. Generally, the amount of energy each switch capacitance stores is

$$E_{Coss} = \frac{1}{2} C_{OSS,eff} V_{sw}^2 \tag{4.2}$$

where $C_{OSS,eff}$ is the effective linear capacitance that stores the same amount of energy as the actual switch output capacitance when charged from zero to V_{SW}. This effective capacitance is important because the output capacitance is not constant across applied voltage as illustrated in Figure 4-4. For the full bridge



(a) (b)

Figure 4-3: (a) A full bridge inverter that delivers an output voltage designated as V_{inv}. The voltage across switch Q_1 is explicitly labeled. (b) Operating switch waveforms to generate a square wave for V_{inv} with period T_0 and the corresponding voltage across Q_1. While only the voltage across Q_1 is shown, all switches see a voltage profile with the same amplitude.

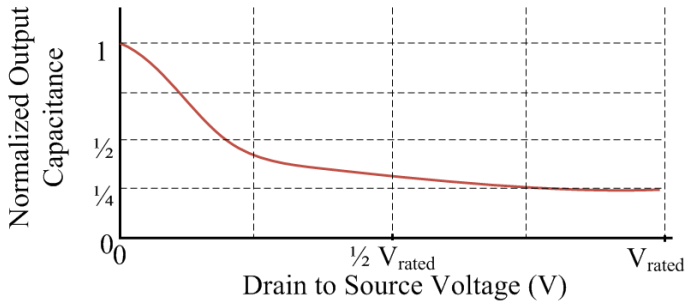


Figure 4-4: Example device capacitance across drain-to-source voltage. The output capacitance at low voltages is much higher than the output capacitance at higher drain-to-source voltages.

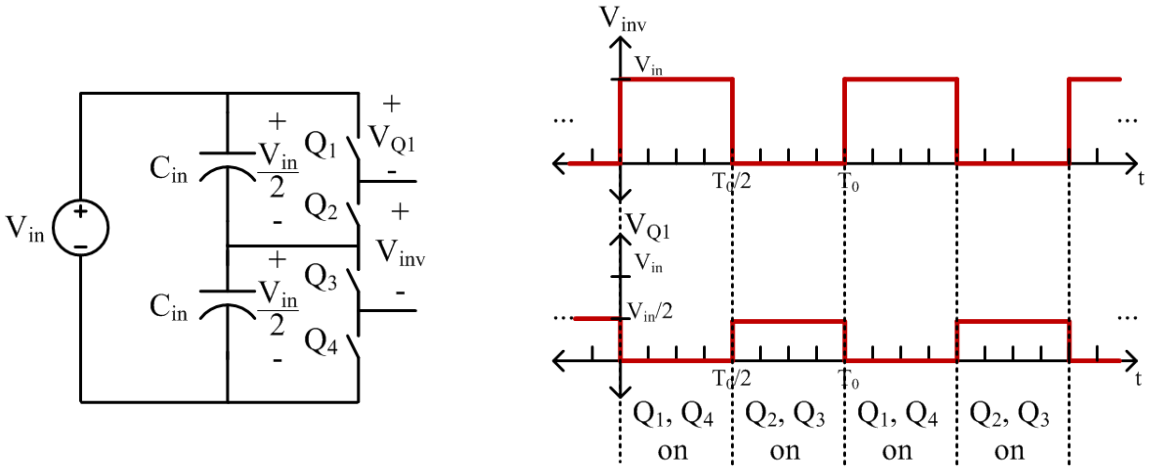
inverter of Figure 4-3(a), each switch capacitance would either store or release

$$E_{Coss,FB} = \frac{1}{2} C_{OSS,eff} V_{in}^2 \ . \tag{4.3}$$

Instead of the traditional full bridge inverter, consider the stacked-bridge inverter of Figure 4-5(a). Similar to the full bridge inverter, a square wave voltage can be generated; however, it only swings between zero and the input voltage as shown in Figure 4-5(b). As can be seen from the waveforms, each switch only needs to be able to block half of the input voltage for balanced voltages on the input capacitors. For a constant effective switch capacitance, this means that the energy stored or released in each switch capacitor of the stacked-bridge inverter is

$$E_{Coss,SB} = \frac{1}{2} C_{OSS,eff} \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{8} C_{OSS,eff} V_{in}^2 \ , \tag{4.4}$$

which is a quarter of the amount of energy for the full bridge inverter (assuming the two types of switches have the same capacitance). There are other effects and benefits of stacking as well. The stacked-bridge inverter delivers a lower voltage to the transformer than the full bridge inverter. This means that for the same power delivery, the stacked-bridge inverter will require a higher current which is also beneficial for achieving ZVS. And as mentioned earlier, lower voltage rated devices can be used which can translate into lower switch capacitance due to a lower (better) figure-of-merit. All of these factors can combine to provide favorable performance in the active bridge converter. A potential argument against stacking the devices in this way is the need for isolated gate drive signals, extra capacitors such as the blocking capacitor between the inverter and the transformer as shown in Figure 4-6, and potentially the need for



(a) (b)

Figure 4-5: (a) A stacked full bridge inverter that delivers an output voltage designated as V_{inv}. The voltage across switch Q_1 is explicitly labeled. (b) Operating switch waveforms to generate a square wave for V_{inv} with period T_0 and the corresponding voltage across Q_1. While only the voltage across Q_1 is shown, all switches see a voltage profile with the same amplitude.

voltage balancing circuits to maintain the voltage distribution across the stack. In practice, these issues have not been found to be a source of concern and can be easily addressed with well-chosen components and passive balancing circuits, if needed.

The stacking technique does not have to be limited to a single stacked full bridge design. As seen in the design of the Impedance Control Network (ICN) converter of Chapter 2, a double stacked inverter is possible as shown in Figure 4-7(a). As can be seen from the waveforms of Figure 4-7(b), each switch only needs to be able to block a quarter of the input voltage. This time, the energy stored or released in

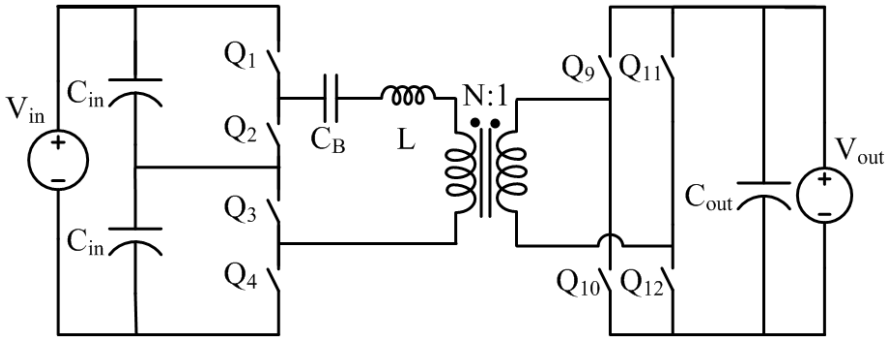
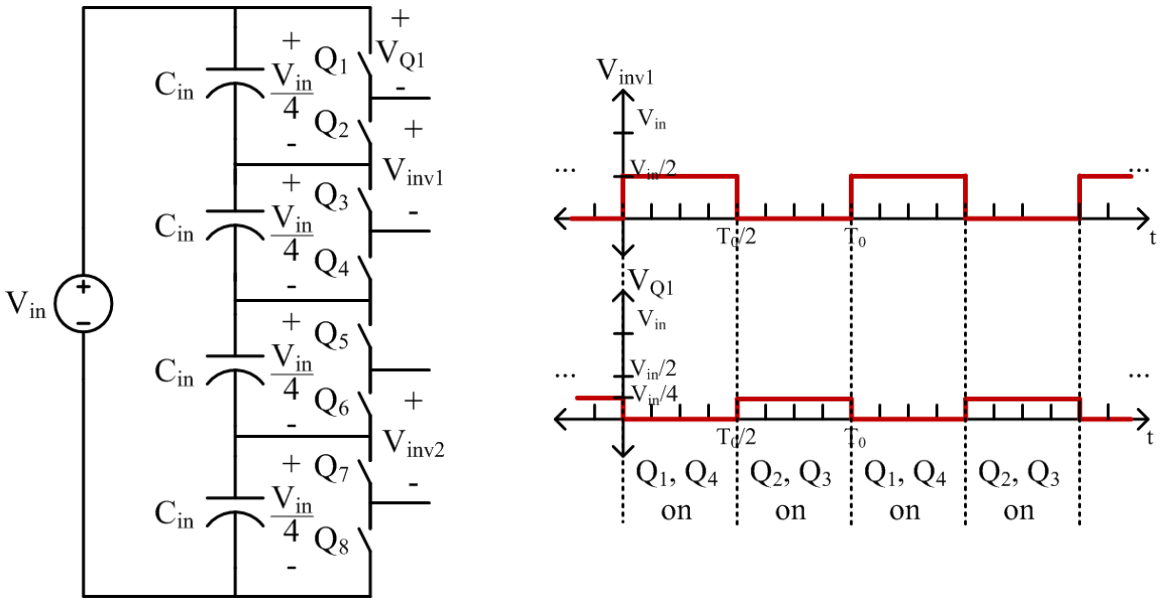


Figure 4-6: Circuit diagram for an active bridge converter using a stacked full-bridge on the input and a full bridge on the output. A blocking capacitor, C_B, is used to remove the dc component in the inverter output voltage



(a) (b)

Figure 4-7: (a) A double stacked-bridge inverter that delivers two output voltages designated as V_{inv1} and V_{inv2}. The voltage across switch Q_1 is explicitly labeled. (b) Operating switch waveforms to generate a square wave for V_{inv1} with period T_0 and the corresponding voltage across Q_1. While only one inverter voltage is shown, the other inverter voltage can have the same profile. Similarly, while only the voltage across Q_1 is shown, all switches see a voltage profile with the same amplitude.

each switch capacitance of the double stacked inverter is

$$E_{Coss,DS} = \frac{1}{2} C_{OSS,avg} \left(\frac{V_{in}}{4}\right)^2 = \frac{1}{32}\, C_{OSS,avg} V_{in}^2 , \tag{4.5}$$

which is a quarter of the amount of energy for the single stacked-bridge inverter and a sixteenth of the amount of energy for the full bridge inverter. The double stacked design does not necessarily result in higher inverter current for the same power when compared to the single stacked design, but the even lower voltage rating on the switches for the double stacked design can derive a benefit that the single stacked design could not achieve. The input voltage range of interest for this work is from 260 V to 410 V, with a nominal input voltage of 380 V. For the single stacked inverter, the devices would need to be able to block a minimum 205 V while for the double stacked inverter, the devices would need to be able to block a minimum 102.5 V. As shown in Table 4-1 and Figure 4-2, EPC has a number of GaN-based devices at 200 V and only one device at a higher voltage of 300 V. Therefore, the double stacked inverter can easily use EPC GaN-based devices while the single stacked inverter is limited to one device (from EPC). The benefit of using a GaN-based device over a Si-based device is that for the same rated voltage, the figure-of-merit can be lower and the EPC devices tend to have much smaller footprints, which helps in achieving high power density [50]. Therefore, for this (fairly common) input voltage range, the double-stack technique has multiple means of improving the device performance – by lowering the rated voltage and by enabling the use of an emerging technology.

Similar to the single stacked inverter, the arguments against this double stacked design include the need for isolated gate drive signals for each stacked half-bridge, extra blocking capacitors, and the potential need for multiple voltage balancing circuits. In addition, this topology has more active switching devices which could complicate the control scheme and result in additional gating loss. Furthermore, there are now two inverter outputs, which must be combined. Because lower rated devices can be used, it is possible that the gate charge of each individual device can be much lower so that the overall gating loss for the double stacked inverter is comparable to the gating loss for the single-stack inverter (see gate power analysis for this work in [78]). In order to keep the control scheme quite simple and to efficiently and effectively combine the two inverter outputs, a unique three-port leakage transformer was developed, as will be discussed in the next subsection.

In summary, to overcome some of the challenges of a traditional DAB converter to achieve ZVS at low power levels, it was determined that stacking switching devices can improve the overall performance. The benefits of stacking include using lower voltage rated devices, decreasing the amount of energy stored in the intrinsic capacitance of the switching device, increasing the current available for ZVS, and enabling the use of emerging switch technologies. Moreover, as will be discussed in a later

subsection, the double stacked inverter architecture chosen for this work, combined with the rest of the circuit topology can facilitate a unique operating mode that further increases converter performance.

4.1.2 Single Magnetic Component

One of the reasons the traditional DAB converter is attractive is because it can provide isolation and has a low component count. For some designs, the transformer and energy transfer inductance can be realized in a single magnetic component. Because the double stacked inverter design of the previous section can have multiple inverter outputs, it will require some way of combining them. Three possible ways of doing this are shown in Figure 4-8. The topology chosen for this thesis is that of Figure 4-8(c); we implement this structure with a special magnetic component such that the two transformers and the two energy transfer inductances of Figure 4-8(c) are combined into a single magnetic structure. As described below, the proposed magnetic component uses a single standard three-legged transformer core and a winding structure that can be easily implemented in a printed circuit board (PCB). Not only does this topology and magnetic structure provide a very compact design, but it also enables a unique operating mode, which will be discussed in a later subsection.

In designing the single magnetic component (three-port leakage transformer) for this topology, consider the simplified physical implementation shown in Figure 4-9(a). In this implementation, there are three windings, each around the leg of a three-legged core. Such a structure could be implemented using an EE, EELP, EILP core set, amongst others. To analyze the behavior of the proposed structure, a magnetic reluctance circuit model can be used, as shown in Figure 4-9(b). To simplify the analysis, let us consider a core that has a very high permeability such that the reluctance of each branch is approximately zero, i.e.,

$$\lim_{\mu\to\infty} \quad \Re_1 \quad = \lim_{\mu\to\infty} \quad \Re_2 \quad = \lim_{\mu\to\infty} \quad \Re_3 \quad = 0 \tag{4.6}$$

where μ is the permeability of the core, $\Re_1$ is the reluctance of one of the outer legs, $\Re_2$ is the reluctance of the other outer leg, and $\Re_3$ is the reluctance of the center leg. Operating under such an assumption, Kirchhoff's voltage law (KVL) and current law (KCL) can be applied to the equivalent circuit model to produce the following set of equations:

$$N_1 i_1 = N_2 i_2 = N_3 i_3 \tag{4.7}$$

$$\Phi_1 + \Phi_2 + \Phi_3 = 0 \tag{4.8}$$

where N_1 is the number of turns wound around one of the outer legs, i_1 is the current through the N_1 turns, and Φ_1 is the resultant magnetic flux through that leg. N_2 is the number of turns wound around the other outer leg, i_2 is the current through the N_2 turns, and Φ_2 is the resultant magnetic flux through that leg. N_3

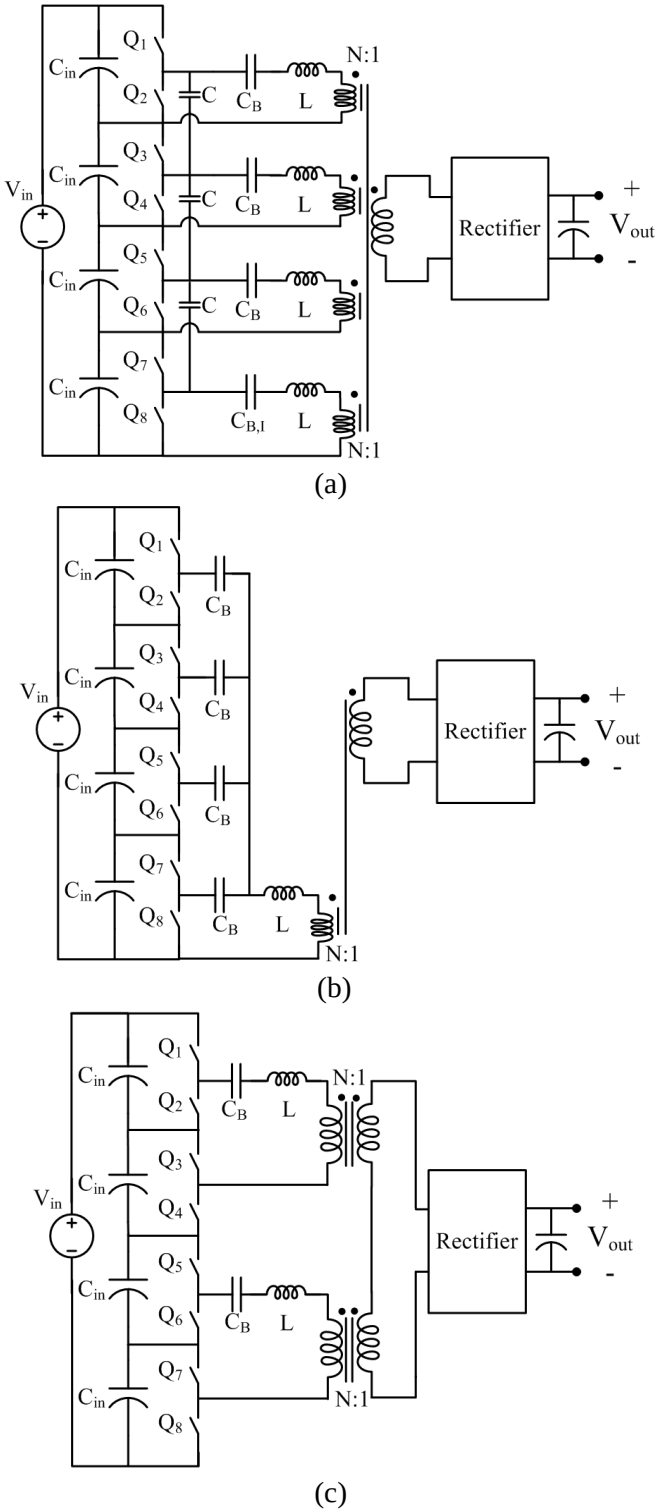


Figure 4-8: Three possible variants of an active bridge converter with a double stacked-bridge inverter. (a) The outputs of four half-bridges are combined through a four primary, one secondary transformer structure. Voltage difference is compensated through the use of multiple interconnected capacitors. (b) The outputs of four half-bridges are connected in parallel before a single primary, single secondary transformer. (c) The outputs of two stacked full bridges are fed through two (single primary, single secondary) transformers whose secondaries are connected in series.

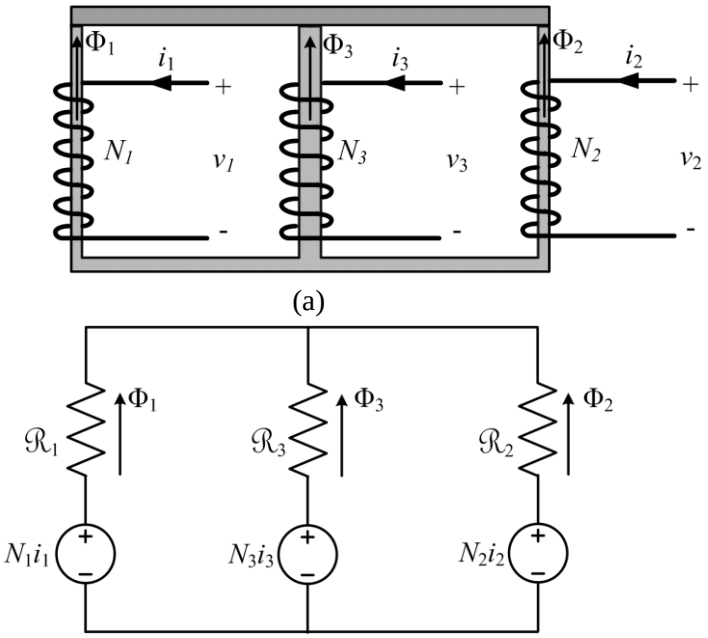


Figure 4-9: (a) An example physical implementation of a three-winding magnetic component for use in the topology of Figure 4-8(c). This implementation has three windings on three separate legs. The N_1, N_2, and N_3 turns generate a flux of Φ_1, Φ_2, and Φ_3, respectively. (b) A magnetic reluctance circuit model of the three-winding magnetic structure. The magnetic flux generated from the windings will travel through the reluctance, $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$ of each core leg. In this simplified model we neglect other flux paths (e.g., flux return paths outside the core) which are important for realizing the transformer leakage inductance.

is the number of turns wound around the center leg, i_3 is the current through the N_3 turns, and Φ_3 is the resultant magnetic flux through that leg. Taking the time derivative of (4.8) yields

$$\frac{d\Phi_1}{dt} + \frac{d\Phi_2}{dt} + \frac{d\Phi_3}{dt} = 0 \tag{4.9}$$

which can be combined with the relationship that

$$v = N\frac{d\Phi}{dt} \tag{4.10}$$

to give the following expression

$$\frac{v_1}{N_1} + \frac{v_2}{N_2} + \frac{v_3}{N_3} = 0 \tag{4.11}$$

where v_1 is the voltage across the N_1 outer leg winding, v_2 is the voltage across the N_2 outer leg winding, and v_3 is the voltage across the N_3 center leg winding.

For the topology of Figure 4-8(c), this work proposes a winding structure that wraps two primary windings around the two outer legs and a secondary winding around the center leg. Each primary winding will have the same number of turns, and the secondary will be a single-turn winding because it will be carrying high current. The expression of (4.11) can be simplified and rewritten as follows

$$\frac{v_p}{N} + \frac{v_p}{N} + \frac{v_s}{1} = 0 \tag{4.12}$$

$$\frac{2v_p}{v_s} = N_{eff} \tag{4.13}$$

where v_p is the voltage across each primary, v_s is the voltage across the secondary, N is the physical transformer turns ratio, and N_{eff} is the effective (or apparent) transformation ratio of the transformer counting from a single transformer input winding to the output winding, (or, equivalently from one inverter output) assuming that both input windings are driven in the same manner. The above equations assume that the same voltage is being applied to each primary, but this does not have to be the case. For example, it is possible to apply zero voltage across one of the transformer primary windings. By doing this, the core loss can be reduced by a factor of two. Under this condition, (4.12) and (4.13) now become

$$\frac{v_p}{N} + \frac{0}{N} + \frac{v_s}{1} = 0 \tag{4.14}$$

$$\frac{v_p}{v_s} = N_{eff} \tag{4.15}$$

It can be seen that the effective turns ratio is different (in fact it is half of the previous effective turns ratio). As discussed in the introductory chapter, the DAB can operate across a wide range of voltages, but the performance degrades when the transformer turns ratio does not match the input-to-output voltage ratio. In order to keep the effective transformation ratio equal to the physical transformer turns ratio, a reconfigurable rectifier is proposed in the next subsection. The details of the construction of the single magnetic component for the prototype converter can be found in the experimental verification section.

In a practical design, there is finite permeability in the core which leads to non-zero core reluctance as well as reluctance outside the core that contributes to leakage. A more sophisticated reluctance model incorporating these reluctances is seen in Figure 4-10. In this model, the reluctance of the core is divided into several components based on the geometry of the core. These are the reluctance of each of the legs, $\Re_{outer1}$, $\Re_{outer2}$, and $\Re_{center}$; the reluctance through the top of the core between the legs, $\Re_{top1}$ and $\Re_{top2}$; as well as the reluctance through the bottom of the core between the legs, $\Re_{bottom1}$ and $\Re_{bottom2}$. There are also reluctances that represent a path for flux outside of the core, $\Re_{lk1}$ and $\Re_{lk2}$. The reluctance is defined as

$$\Re = \frac{l}{\mu A} \tag{4.16}$$

where l is the physical magnetic path length, μ is the permeability of the material, and A is the cross-sectional area of the path. The permeability of the core can be several magnitudes higher than air so often times the reluctance of the core is much lower than that of air. This usually means that a majority of the

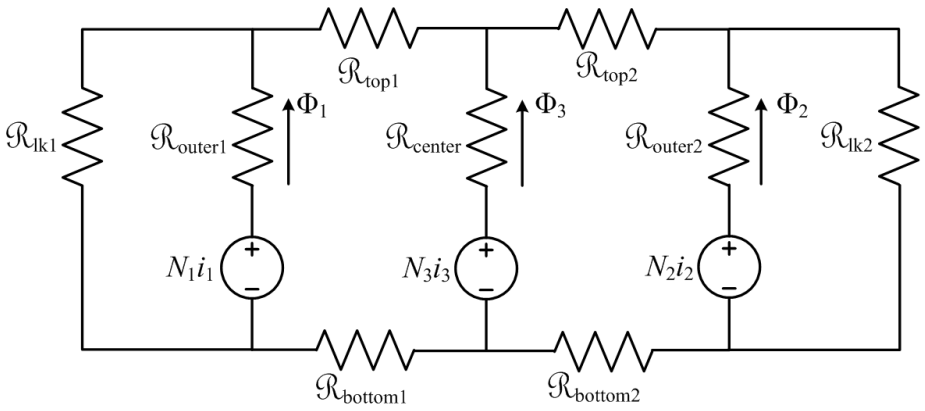


Figure 4-10: A magnetic reluctance circuit model of the three-winding magnetic structure incorporating core and leakage reluctance. The magnetic flux generated from the outer windings will travel through the reluctance, $\mathcal{R}_{outer1}$ and $\mathcal{R}_{outer2}$ of each core leg. The flux is then split between the reluctance in the top of the core, $\mathcal{R}_{top1}$ and $\mathcal{R}_{top2}$, and the reluctance outside the core, $\mathcal{R}_{lk1}$ and $\mathcal{R}_{lk2}$.

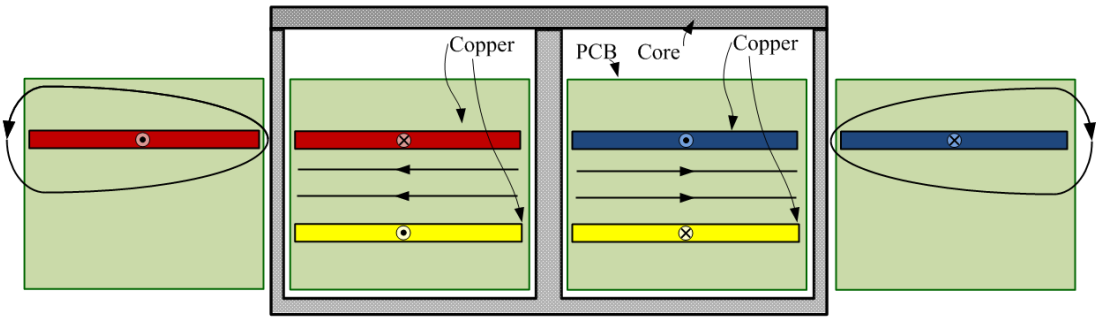


Figure 4-11: A cross sectional view of a simplified winding structure of the three-winding magnetic component. For illustration, some magnetic field lines are drawn simply to represent their presence but they are not intended accurately represent the shape or magnitude.

flux travels through the core and only a fraction of the flux goes through the reluctance that is outside the core. The proposed winding design has windings that are outside the core. A simplified cross-sectional view of this winding structure can be seen in Figure 4-11. By Ampere's law, each copper layer will generate a magnetic field. In a traditional transformer design where the windings are within the core and wrapped around the center leg, these field lines will be between the windings. These are the horizontal field lines seen in Figure 4-11. This winding design features primary windings that are outside the core, which are generating field lines that do not link to the secondary winding. There is energy associated with these field lines and the energy stored can be linked back to the leakage inductance as approximated by:

$$E_{lk} = \frac{\mu_0}{2} \sum\int H^2 dV = \frac{1}{2} L_{lk} I^2 \tag{4.17}$$

where μ_0 is the permeability of free space, H is the field strength, V is the volume that the field occupies, L_{lk} is the leakage inductance, and I is the current through the copper. The proposed winding structure

implemented in PCB has very wide windings outside the core and comprise a large area, which will affect the volume of the field lines (similar to what one would see with an air-core inductor). It is through this particular implementation of the three winding structure that we are able to get a sufficient amount of leakage inductance. All said, the reluctance of the core will contribute to magnetizing inductance and the reluctance outside of the core will contribute to leakage inductance. A first order model of the three-port winding structure and associated leakage and magnetizing inductances is shown in Figure 4-12. By measuring each port, one can get a good approximation of the magnetizing and leakage inductances. By shorting v_2 and v_3 and measuring the impedance as seen from v_1, one can get a good approximation for the total primary-referred leakage inductance (assuming very large magnetizing inductances). Due to the symmetry of the design, it would be fair to assume that the leakage is distributed evenly between the two primary windings. By leaving all ports open, and measuring the impedance at v_1 or v_2, one can get a good approximation of the magnetizing inductance (assuming leakage is small in comparison). There are other parasitic elements (e.g., capacitance and resistance) and coupling inductances (e.g., leakage between each primary) which can quickly add complexity to the model.

The proposed magnetic implementation has several associated benefits. The first is a compact design – a single core can be used instead of two separate cores. The second is a reduction in winding loss – as compared to windings around two cores with the two secondary windings connected in series, this design has a single secondary winding, which results in half as much winding length. The third benefit is the realization of the energy transfer inductance – because part of the primary winding is physically outside the core, this design has sufficient primary-referred leakage inductance so that no discrete inductors are needed in the final build. A fourth benefit of this double primary, single secondary structure is the ease of only energizing one of the primary windings and shorting the other – this reduces

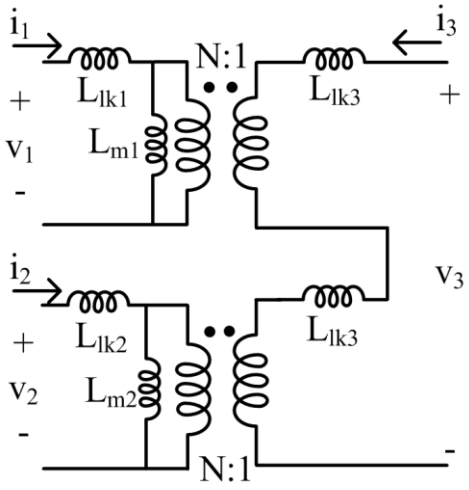


Figure 4-12: A three-port model of the proposed three-winding magnetic structure.

core loss, which is particularly useful at low powers. For the physical design of such a transformer, please refer to Section 5.1.2.

4.1.3 Reconfigurable Rectifier

As mentioned in the previous subsection, the double stacked-bridge inverter paired with the double primary, single secondary transformer could have more than one mode of operation. In one mode, both transformer primaries are energized resulting in an effective transformation ratio of (4.13). If only one transformer primary is energized while the other is shorted, the effective transformation ratio is reduced by a factor of two as stated in (4.15). In order to keep the converter operating near the ideal conversion ratio for trapezoidal transformer current waveforms, either the physical transformer turns ratio must be halved or the voltage that appears across the secondary winding must be reduced by a factor of two. The second option can be achieved with the addition of an active switch and additional output capacitors.

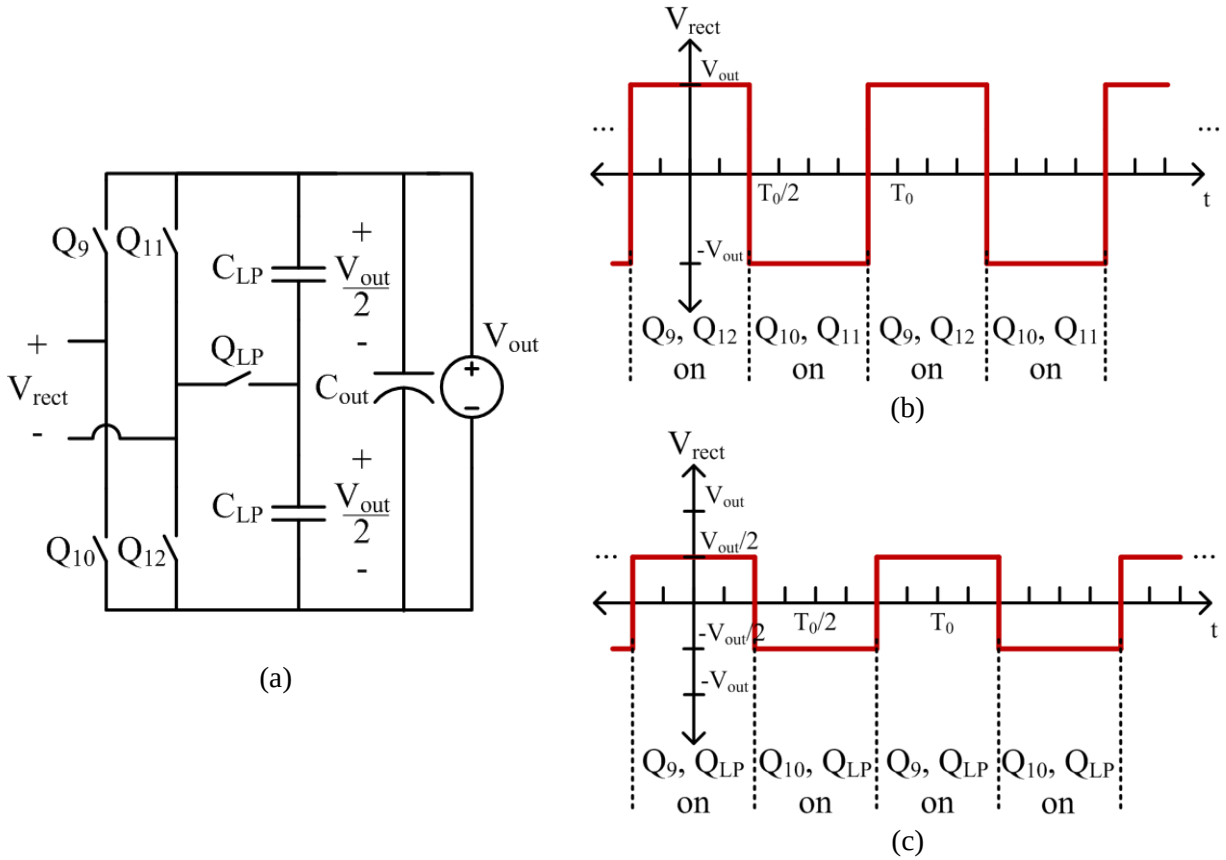


Figure 4-13: (a) Proposed topology for the reconfigurable rectifier that can either operate as a regular full bridge rectifier or as a half-bridge rectifier. (b) Operating voltage waveform at the rectifier input when operated as a full bridge rectifier. During this mode, Q_{LP} remains off. (c) Operating voltage waveform at the rectifier input when operated as a half-bridge rectifier. During this mode, Q_{11} and Q_{12} remain off and Q_{LP} remains on. The voltage at the rectifier input is supplied by one of the C_{LP} capacitors, which is nominally at half of the output voltage.

Consider the rectifier shown in Figure 4-13(a), which is a full bridge rectifier with the addition of a switch, Q_{LP}, connecting the negative terminal of the rectifier input to the center node of two stacked capacitors across the output. If Q_{LP} is left off, the rectifier can be operated as a full bridge rectifier so that the voltage to the input of the rectifier alternates between $\pm V_{out}$ (where V_{out} is the output voltage of the converter) as shown in Figure 4-13(b). Alternatively, Q_{LP} can be left on. To prevent shoot-through, the half-bridge that is connected to Q_{LP} must remain off while the other half-bridge (which is connected to the positive terminal of the rectifier input voltage) would continue to operate. The rectifier in this condition acts as a half-bridge or voltage-doubler rectifier. The voltage to the input of the rectifier would now alternate between $\pm V_{out}/2$ as shown in Figure 4-13(c). This voltage would be supplied by the two stacked capacitors. Therefore, a reconfigurable rectifier can be implemented to operate as either a full bridge rectifier or a half-bridge rectifier to match the operating needs of the converter. This capability can be used to further maintain high performance operation across a wide range of power levels.

4.2 Operating Modes

Given the discussion in the previous subsections, the full active bridge topology proposed for this thesis is shown in Figure 4-14. It comprises a double stacked-bridge inverter coupled to a reconfigurable

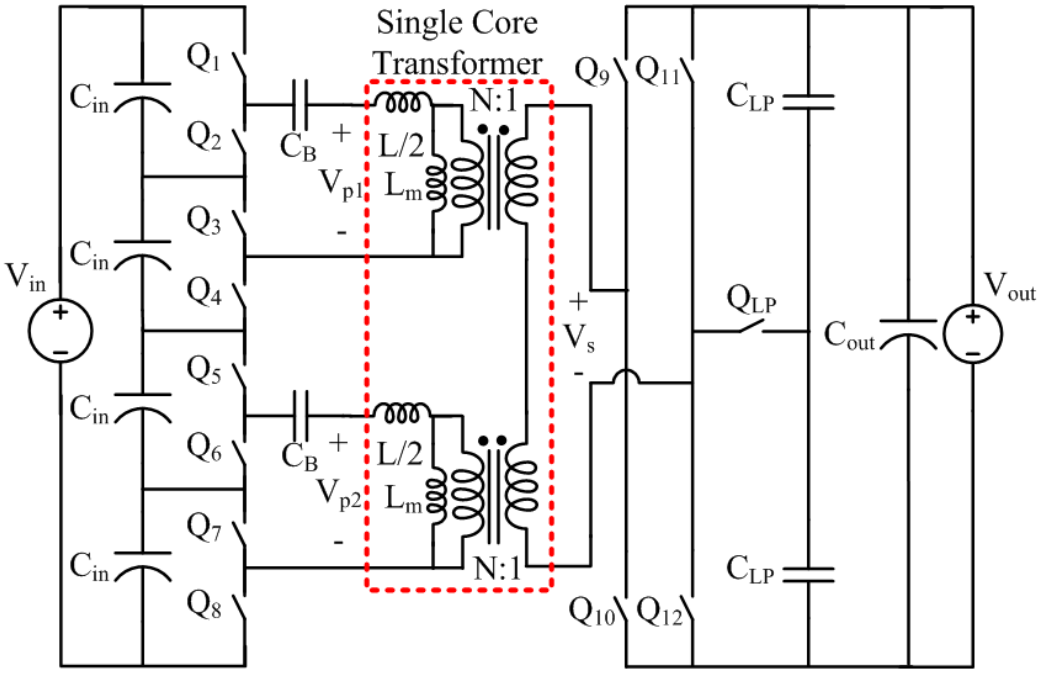


Figure 4-14: Circuit diagram for the proposed system. The dashed red box contains an equivalent circuit model for the single magnetic component. Each of the stacked full bridges feeds the primary winding of a single-core, three-winding transformer. An auxiliary switch, Q_{LP}, and capacitors C_{LP} in the rectifier allow for a mode switch into a low power mode. A blocking cap, C_B, is used to remove the DC component in the square-wave output of each stacked-bridge. The total primary-referred leakage inductance, *L*, is split between the two primaries.

rectifier via a special three-winding leakage transformer that provides power combining and energy storage, in addition to isolation and voltage transformation. As hinted earlier, there are a multiple of ways to operate this converter.

The first mode of operation to be discussed will be referred to as "normal mode." Under normal mode operation, both of the stacked full bridge inverters generate square voltage waveforms that are in phase with each other as shown in Figure 4-15. The rectifier is operated as a full-bridge rectifier and generates a rectifier input voltage that is lagging the inverter voltage waveforms. To describe this operation another way, the two primary windings will see identical square-wave voltages and the secondary winding will see a square-wave voltage that is phase-shifted behind the primary voltages so that energy is transferred from the inverter to the rectifier as given by

$$P_{out} = \frac{\left(\frac{V_{in}}{4} + \frac{V_{in}}{4}\right) V_{out} N}{2\pi f_s L} \phi \left(1 - \frac{\phi}{\pi}\right) \tag{4.18}$$

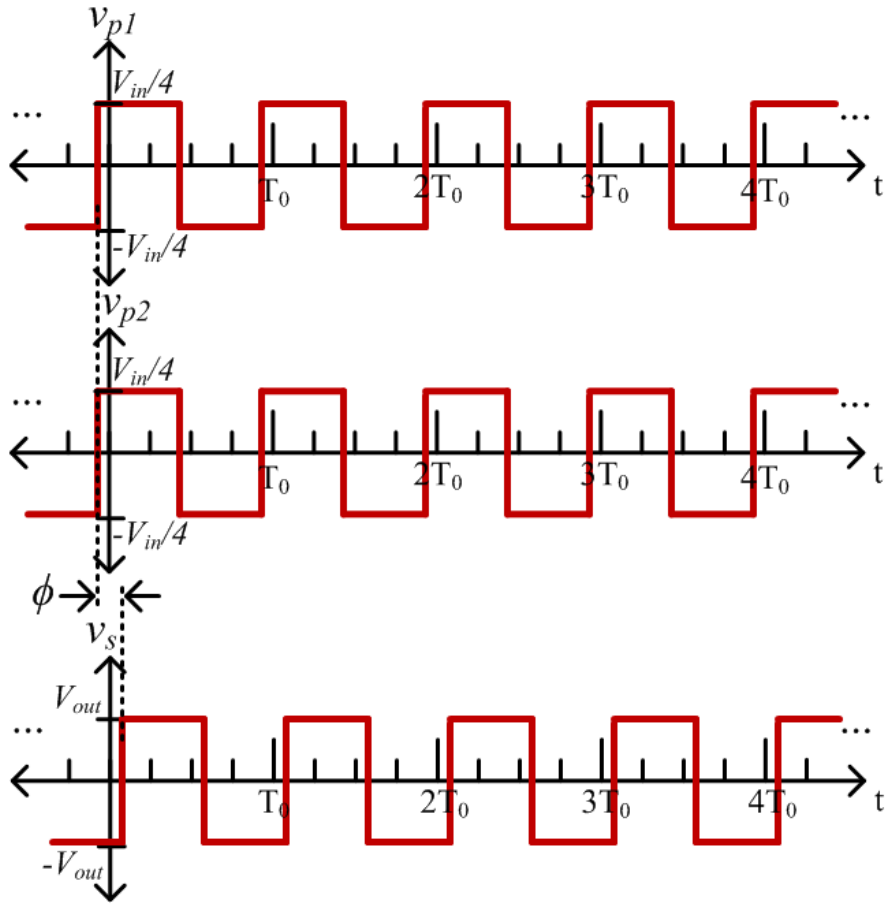


Figure 4-15: Transformer voltage waveforms when operated in normal mode. Both transformer primary windings see an identical square-wave voltage. The secondary voltage is also a square-wave and is phase-shifted behind the primary voltages by ϕ (in radians). In this mode, the switching period of the primary and secondary voltages is T_0.

where V_{in} is the converter dc input voltage, V_{out} is the converter dc output voltage, N is the physical transformer primary-to-secondary turns ratio, f_s is the switching frequency in Hz, L is the total primary-referred leakage inductance of the transformer which is used for energy transfer, and ϕ is the phase shift between the inverter and rectifier in radians. It can be seen that the effective primary voltage is not simply the input voltage and this is due to the nature of the stacked inverter and double primary transformer. To modulate power, the phase shift between the inverter and rectifier is varied.

This particular combination of double stacked-bridge inverter, three-winding transformer, and reconfigurable rectifier offers another operating mode, which is referred to as the "low-power" mode. To operate in low-power mode, one transformer primary winding is shorted at any given time. Shorting a transformer primary can be achieved by closing both top (or bottom) switches of each associated half-bridge in the stacked full bridge. In Figure 4-14, this would correspond to closing Q_1 and Q_3 (or Q_2 and Q_4) to short the top transformer primary and closing Q_5 and Q_7 (or Q_6 and Q_8) to short the bottom transformer primary.

For this thesis, we propose the voltage waveforms shown in Figure 4-16 for operating in low-power mode. (For simplification, dead-time is not explicitly marked but is an important factor in ensuring ZVS.) The proposed method energizes one primary winding while the other is shorted. In the next period, the other primary winding is energized while the previously energized one is shorted. The primaries are alternated to balance out the flux in the core and voltage across the input capacitors. The energized primary is alternated every cycle for ease of gate drive signal implementation. Figure 4-17 shows the proposed gate drive signals for the double stacked inverter. When operated in this way, the switching frequency for the inverter devices can be reduced by a factor of two and only two of the four rectifier devices are switched (which also helps lower gating loss and any other associated switching loss). The gate drive signals for each half-bridge are identical, with only a phase shift of ½ T_0 between the four half-bridges. To apply the short across the transformer, Q_2 and Q_4 are closed or Q_6 and Q_8 are closed. This means that two of the four stacked input capacitors are connected to the rest of the circuit more often. Because of the way the transformer is being shorted, this particular implementation will require balancing circuits within each stacked-bridge inverter so that the four input capacitors can maintain voltage balance. Such a circuit can be implemented with a passive switched capacitor network on the inverter as shown in Figure 4-18. Further balancing circuits could be installed to ensure equal voltage across all input capacitors, but for this particular architecture and operation, this is not found to be necessary.

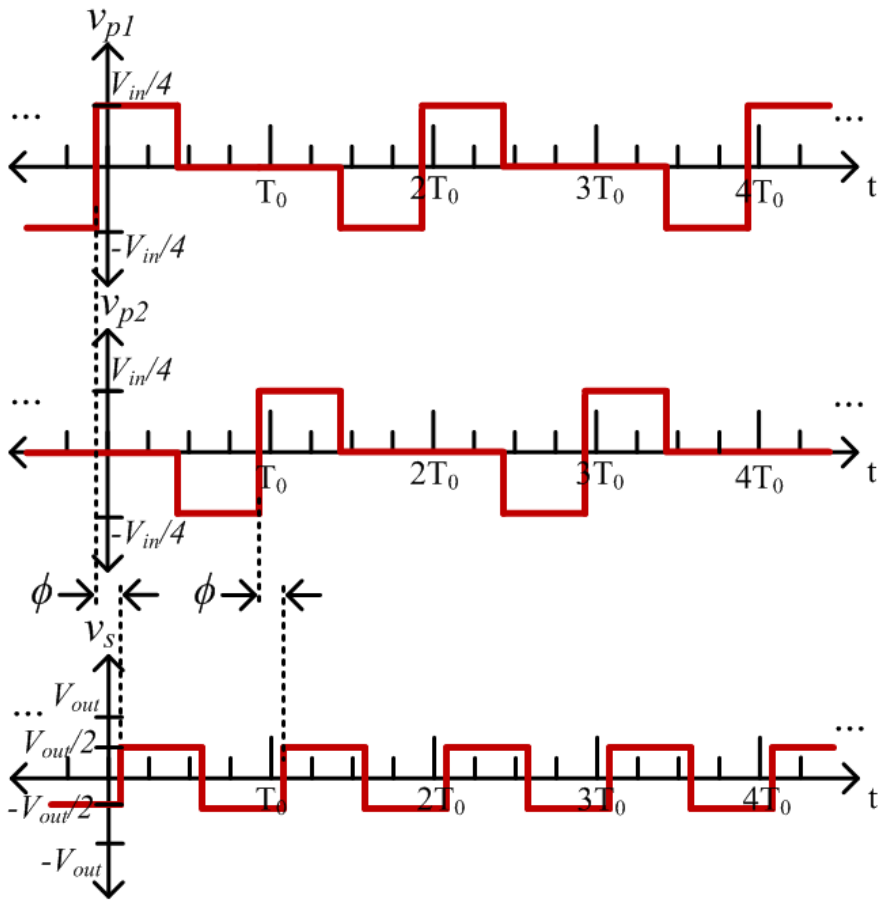


Figure 4-16: One example implementation of the transformer voltage waveforms when operated in low-power mode. One transformer primary winding is energized while the other is shorted. This particular scheme alternates which primary is energized every cycle. The secondary voltage is still a square-wave but now with half the amplitude as compared to the normal mode operation. It is still phase-shifted behind the primary voltages by ϕ (in radians). In this mode, the switching period of the primary voltage (and inverter) is now $2T_0$ and the secondary voltage (and rectifier) is still T_0.

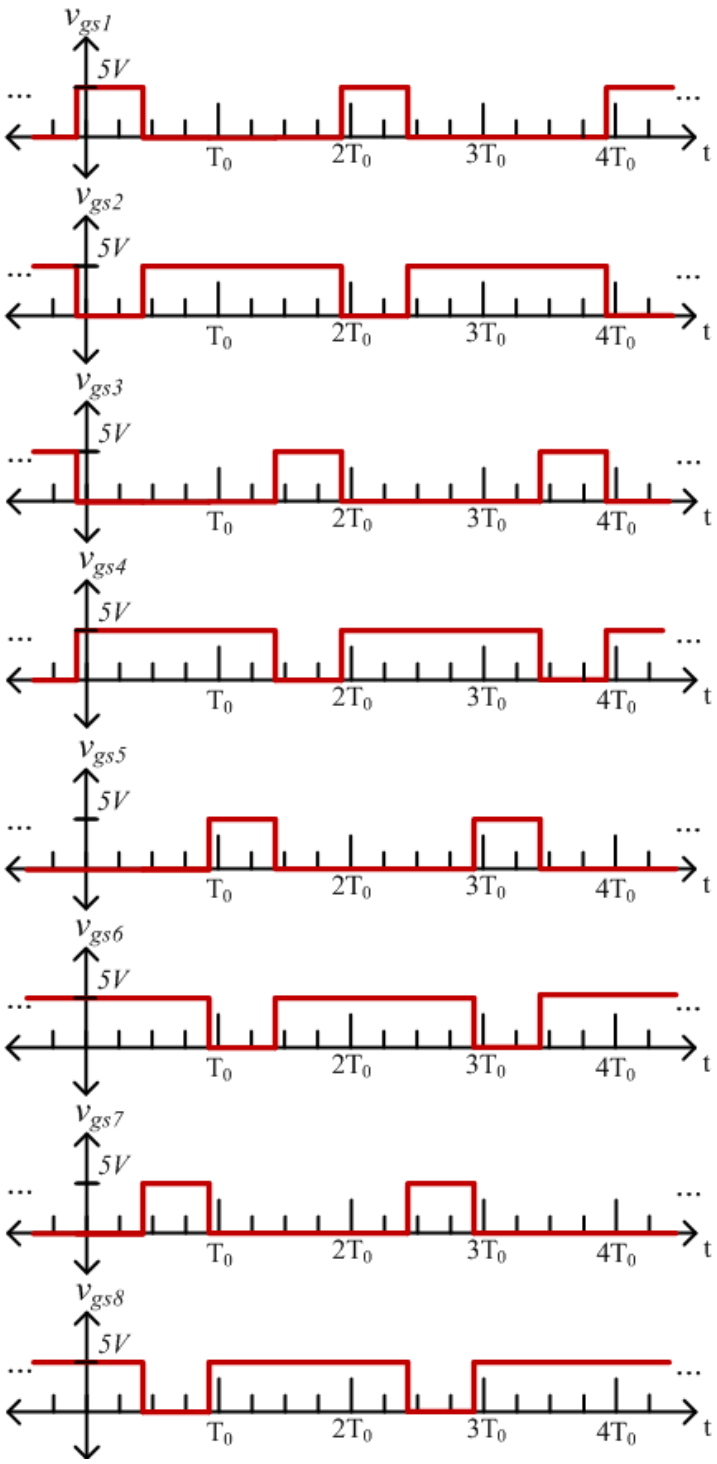


Figure 4-17: One example implementation of the gate drive signals for the double stacked inverter when operated in low-power mode. Through these signals one transformer primary winding is energized while the other is shorted. This particular scheme alternates which primary is energized every cycle. In this mode, the duty cycle of the devices is either 25% or 75% and switching period is $2T_0$. Each half-bridge signal is simply phase-shifted from the following half-bridge signal (i.e., the half-bridge that is stacked underneath) by $\frac{1}{2}T_0$.

It should be noted that, in low-power mode, both primary windings will see a current as shown in Figure 4-19, but only one winding at a time will have real power transfer and generate a magnetic flux in the core. Additionally, the inverter current may vary from cycle to cycle due to the addition of the current that goes to the magnetizing inductance. This means that when a primary winding has a positive voltage across it, the inverter current will have a more positive slope than when the voltage is zero, which can be seen upon close inspection of Figure 4-19. To reduce this effect, a high magnetizing inductance for each core path is desirable.

In order for the apparent transformation ratio to match the physical turns ratio of the transformer, the rectifier is operated as a half-bridge rectifier so that the amplitude of the voltage at the secondary of the transformer is reduced by a factor of two, as seen in Figure 4-16.

The power transfer during low-power operation can be expressed as:

$$P_{out} = \frac{\left(\frac{V_{in}}{4} + 0\right)\frac{V_{out}}{2}\,N}{2\pi f_s L}\,\phi\left(1 - \frac{\phi}{\pi}\right) \tag{4.19}$$

where now the effective primary voltage is reduced by a factor of two and the effective secondary voltage is reduced by a factor of two. Compared to normal mode operation, for the same operating parameters (e.g., input voltage, output voltage, phase shift, etc.), the low power mode naturally delivers a quarter of

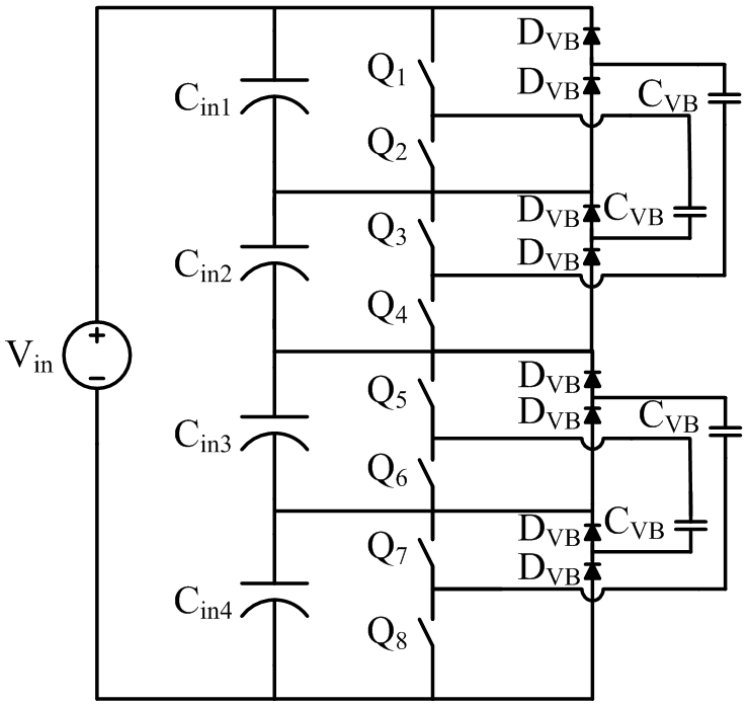


Figure 4-18: A double stacked-bridge inverter with passive voltage balancing circuits on each stacked full-bridge inverter. This switched capacitor networked comprised of multiple diodes and capacitors will balance the voltage between capacitors C_{in1} and C_{in2} and the voltage between capacitors C_{in3} and C_{in4}.

the output power. Because the phase-shift is unchanged, this means that the inductor current still ramps up the same amount and subsequently the current available for ZVS is higher (when compared to a low phase shift under normal mode operation). As will be demonstrated in later sections, this mode is geared toward output powers below 25% of the rated power when ZVS is normally lost and core loss is a major loss mechanism.

In summary, when the converter is operated from full load to 25% load, it is operated in normal mode where both transformer primaries see the same square-wave voltage and the rectifier is operated as a full-bridge. When the converter is operated from 25% load and lower, it is operated in low-power mode where only one transformer primary is energized and the rectifier is operated as a half-bridge in order to increase efficiency. Both modes use phase-shift control to modulate power.

4.3 Simulation

Simulating the converter can give great insight into the performance and tradeoffs before experimental prototypes are designed and constructed. The theory discussed in the previous sections can be evaluated and tested in simulation first and later validated on the bench. For a preliminary analysis, various topologies and operating modes were simulated under the following conditions: V_{in} = 380 V, V_{out} = 12 V, f_s = 500 kHz, and $P_{out,rated}$ = 400 W. Three different topologies were simulated: 1) the traditional full bridge DAB converter, 2) the single stacked active bridge converter, 3) the proposed double stacked

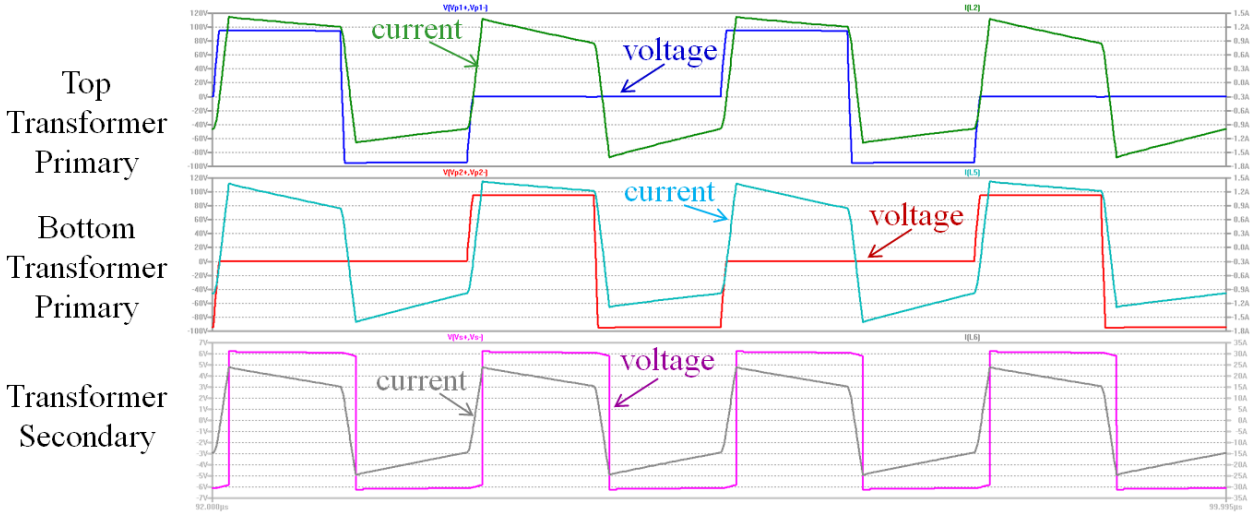


Figure 4-19: Simulation results of the proposed reconfigurable double stacked active bridge converter when operated in low-power mode with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 0.308 radians (approximately 5% of the total period). It can be seen that every cycle, one transformer winding is shorted while the other is energized. Current continues to flow through all windings. The slope of the transformer primary current varies depending on if the winding is energized or shorted due to the magnetizing inductance, which is 256 µH in this simulation.

active bridge converter. The double stacked active bridge converter was simulated using two modes of operation – normal mode and low-power mode.

For the simulations, the switches were modeled off of commercially available GaN devices with proper voltage ratings for the topology. The traditional full bridge DAB converter was simulated using GaN Systems 650 V GS66516T devices with the switch resistance estimated as 70 mΩ and off-state capacitance of 134 pF based on their datasheet [79]. The single stacked active bridge converter was simulated using EPC's only 300 V device (EPC2025), with the switch resistance estimated as 140 mΩ and effective off-state capacitance of 106.25 pF based on their datasheet [77]. The double stacked active bridge converter was simulated using EPC's lowest capacitance 200 V device (EPC2012C), with the switch resistance estimated as 105 mΩ and off-state capacitance of 102.5 pF. The off-state capacitance for all three devices is similar. The devices and their parameters are listed in Table 4-2. For the transformer model, the full bridge converter was simulated with a leakage of 32.832 μH and a 32:1 turns ratio. The single stacked active bridge converter was simulated with an energy transfer inductance of 8.208 μH and a 16:1 turns ratio. The double stacked active bridge converter was simulated with an energy transfer inductance of 4.104 μH on each primary and a 16:1 turns ratio for each transformer. These inductances were chosen so that full power is delivered at the same phase shift of roughly 5% of the total period. The transformer turns ratio is chosen to ensure trapezoidal current. Dead-time of the inverter switches is adjusted for the simulations to ensure that the switch capacitance can charge or discharge fully. If it cannot, the dead-time is chosen such that the voltage across the switch falls as close to zero as possible to minimize switching loss. Full details of the simulations and the operating parameters used can be found in Appendix C.

Figure 4-20 shows the efficiency curves from all three topologies as well as the double stacked design operated under low-power mode. It can be seen that the traditional full bridge DAB converter has much lower efficiency across the full power range. This is because it experiences hard switching. In order to have ZVS, this particular design would have to operate at much higher powers or have much better devices. The selection for GaN devices commercially available for 400 V applications is quite limited. Comparatively, the single stacked inverter design performs much better, with loss reduced by

Table 4-2: Characteristics of commercially available GaN FET switching devices as obtained from manufacturer datasheets [77,79]

Part Number	Rated Voltage (V)	Typical $R_{DS,ON}$ (mΩ)	$R_{DS,ON}$ (mΩ)	Typical C_{OSS} (pF) V_{GS} = 0 V	$C_{OSS,eff}$ (pF) V_{GS} = 0 V
EPC2012C	200	70	105 @ 100 °C	64 @ 100V	102.5 @ 100V
EPC2025	300	90	140 @ 100 °C	62.5 @ 200 V	106.25 @ 200 V
GS66516T	650	27	70 @ 150 °C	134 @ 400 V	134 @ 400 V

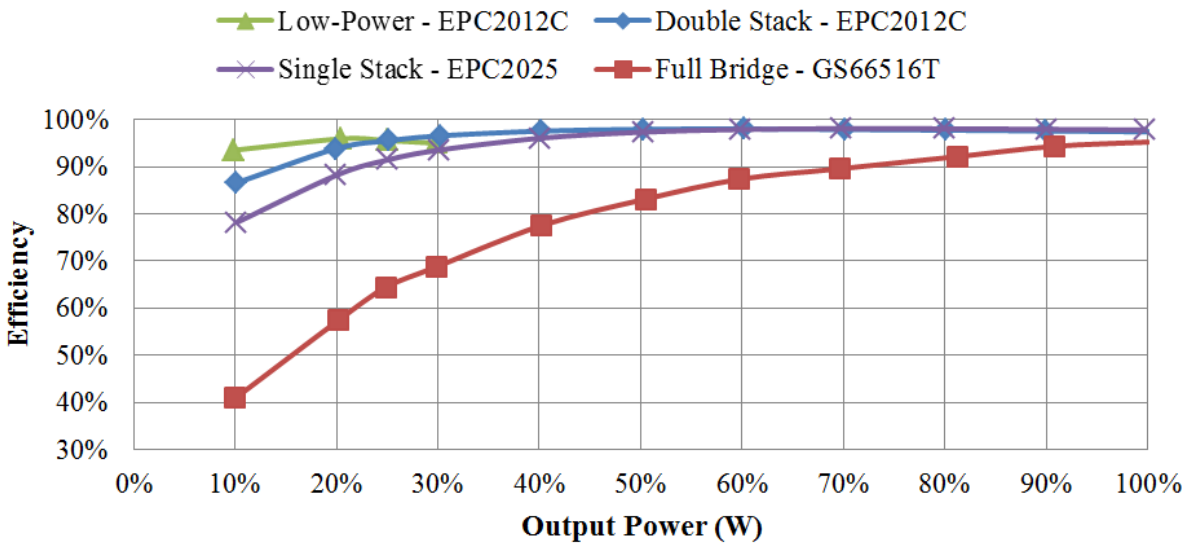


Figure 4-20: Simulated power stage efficiencies of the traditional full bridge DAB converter, the single stacked active bridge converter, and the proposed double stacked active bridge converter (operated in normal and low-power mode) using commercially available GaN-based switching devices. Simulation conditions were: V_{in} = 380 V, V_{out} = 12 V, f_s = 500 kHz, L = 8.204 µH, and $P_{out,rated}$ = 400 W.

about a factor of two across the full power range. Even better still is the performance of the proposed double stacked inverter design. It can be seen that the low-power mode adds an additional boost in efficiency for 25% load and below keeping the simulated efficiency above 93.5% from full load to 10% load.

4.4 Summary of the Proposed Reconfigurable Double Stacked Topology

The proposed reconfigurable double stacked active bridge topology has many associated benefits when compared to a traditional full-bridge DAB topology. Stacking of the inverters can improve device performance not only at the nominal operating point, but also across a wide output power range. The unique three-port magnetic design provides a very compact and efficient means of combining the output from the two inverters as well as providing the energy transfer inductance with a single magnetic core. The three inversion, transformation, and reconfigurable rectification stages can work together to offer multiple modes of operation to further improve converter performance.

This chapter presented the theory of the converter topology. The next chapter presents the details on the design and operation of an experimental prototype. The performance of this prototype is further compared to two other prototypes to quantify the benefits of varying design choices.

Chapter 5

Reconfigurable Double Stacked Active Bridge Converter Implementation

This chapter continues the discussion of the reconfigurable double stacked active bridge converter of Chapter 4. A prototype converter was developed to experimentally validate the theory and benefits of the reconfigurable stacked-bridge active converter. This chapter will first cover the basis for the component selection as well as details on the design choices and characterization of the magnetic component. It will then present experimental results when operated across a wide input voltage and wide output power in normal and low-power mode. Additional experimental results are presented for a converter using an alternate switch technology and for a converter using only a single stacked-bridge inverter.

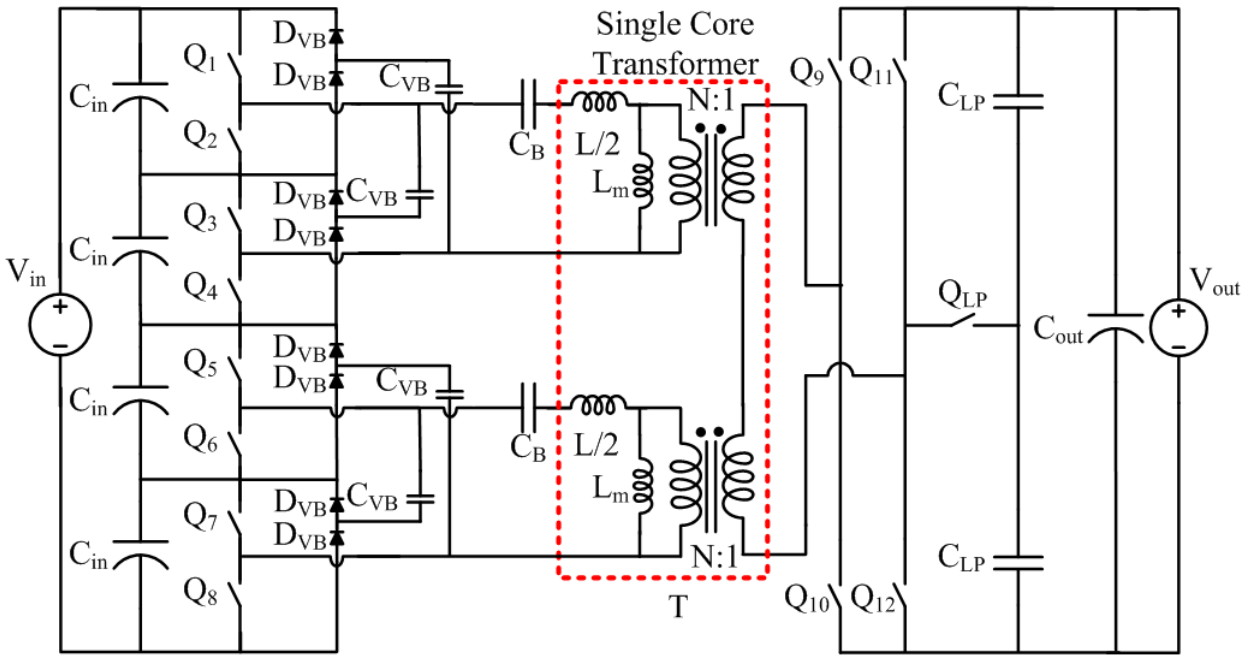


Figure 5-1: Proposed implementation of the reconfigurable double stacked active bridge converter. The dashed red box contains an equivalent circuit model for the single magnetic component. Each of the stacked full bridges feeds the primary winding of a single-core, three-winding transformer. Passive switched capacitor balancing circuits are included. An auxiliary switch, Q_{LP}, and capacitors C_{LP} in the rectifier allow for a mode switch into a low power mode. A blocking cap, C_B, is used to remove the DC component in the square-wave output of each stacked-bridge. The total primary-referred leakage inductance, L, is split between the two primaries. Each primary has a magnetizing inductance, L_m.

5.1 Component Selection and Design

Figure 5-1 shows the design of a prototype converter implementing the proposed approach. Key to the success of the reconfigurable double stacked active bridge converter is the selection of the right components and an optimized design of the three-winding magnetic component. The components used and their values are summarized in Table 5-1 and the converter specifications are listed in Table 5-2. (A complete schematic and bill of materials is shown in Appendix E, and printed circuit board layouts are shown in Appendix D.)

Table 5-1: Components for Prototype GaN-Based Converter

Component	Description	Value
Q_1-Q_8	EPC2012C 200V/5A eGaN® FETs	-
Q_9-Q_{12}	3 parallel EPC2023 30V/60A eGaN® FETs	-
Q_{LP}	2 source-tied EPC2023 30V/60A eGaN® FETs	-
D_{VB}	MMBD3004BRM 300V/225mA Diode Array[a]	-
C_{VB}	TDK 250V X7T ceramic	1 μF
C_B	TDK 250V X7T ceramic	3.3 μF x 2 (paralleled)
N	16 turn primary, 1 turn secondary	16
T	EPCOS EILP43-N49 core 8 layer, 4 oz PCB winding	~925 μH[b]
L	Total primary referred leakage inductance	32 μH[c]
C_{LP}	TDK 16V X7S ceramic United Chemi-Con 16V electrolytic	100 μF x 2 paralleled w/ 1000 μF
C_{in}	TDK 250V X7T ceramic	3.3 μF x (3 paralleled)
C_{out}	TDK 16V X7S ceramic United Chemi-Con 16V electrolytic	100 μF x 12paralleled w/ 1000 μF

[a] the four diodes per stacked-bridge inverter are included in each array

[b] approximate magnetizing inductance at 175 kHz seen from each primary with the other windings open-circuited

[c] value based on experimental data, both based on impedance measurement across one primary with the other windings shorted and on data from when the converter is running

Table 5-2: Converter Specifications

Parameter	Description	Value
V_{in}	Nominal Input Voltage	380 V
	Input voltage range	260 V- 410 V
V_{out}	Output voltage	12 V
$P_{out,rated}$	Output power rating	300W
f_{sw}	Switching frequency	175 kHz

5.1.1 Switching Devices

The double stacked-bridge inverter allows us to use reduced-voltage devices such as 200V GaN power devices. However, given a selection of options, it is not immediately clear which device among those available is best. As mentioned in Chapter 4, there is often a tradeoff between the on-resistance and the output capacitance. For devices with low resistance, there are lower conduction losses, but the dead-time (the time when both devices in a half-bridge are off) and/or the amount of current available for ZVS will have to be increased (see [26] for a discussion of tradeoffs between capacitance and ZVS range for active bridge converters). For this active bridge converter, the dead-time can also affect the phase shift – if the dead-time is too large, then the phase shift would have to be increased in order to generate the desired output power. At some power level, as the inverter current decreases below a certain level, increasing the dead-time alone will not ensure ZVS. For this particular converter design, it was determined that using the GaN FET with the lowest output capacitance would have more favorable performance at low output powers with a negligible efficiency drop at full power. This decision is based on simulation results using the on-resistance at 100 °C and effective output capacitance listed in Table 5-3 to result in the efficiency curves of Figure 5-2. Full details of the simulations and the operating parameters used can be found in Appendix C.

The inverter switches are realized with EPC2012C GaN-on-Si switches. Each individual inverter GaN FET is controlled with a Texas Instruments (TI) UCC27611DRVT driver (preferred over the TI LM5113 because of its integrated voltage regulator) with the high-side driver bootstrapped.

The rectifier is a synchronous full bridge realized with EPC2023 GaN switches. In order to increase efficiency, each half-bridge in the full bridge rectifier comprises three parallel half-bridges. Each half-bridge is controlled with TI LM5113 drivers.

The auxiliary switch used to reconfigure the rectifier is realized using two back-to-back EPC2023 devices with their sources connected so that voltage can be blocked and current can flow in both directions. Both are driven by a single TI UCC27611DRV.

All drivers are powered and controlled from the same control board presented in Section 2.2.1, but operated with a different control scheme (e.g., the inverters are not phase-shifted from each other and there is a low-power mode). Full details on the control parameters can be found in Appendix F.

5.1.2 Transformer Implementation

Based on the previous discussion of Section 4.1.2, the single magnetic component is implemented as a planar magnetic component (i.e., with printed circuit board windings) on an E core structure. It has two primary windings each around an outer leg of a three-legged core and a single-turn secondary around the center leg. Based on (4.12) and (4.13), the optimal turns ratio for this topology is

Table 5-3: Characteristics of 200V EPC eGaN FET switching devices as obtained from manufacturer datasheets [77]

Part Number	Typical $R_{DS,ON}$ (mΩ)	$R_{DS,ON}$ (mΩ) @ 100 °C	Typical C_{OSS} (pF) V_{GS} = 0 V, V_{DS} = 100 V	$C_{OSS,eff}$ (pF) V_{GS} = 0 V, V_{DS} = 100 V
EPC2012C	70	105	64	102.5
EPC2019	36	55	110	185
EPC2010C	18	40	240	300
EPC2034	10	13	530	800

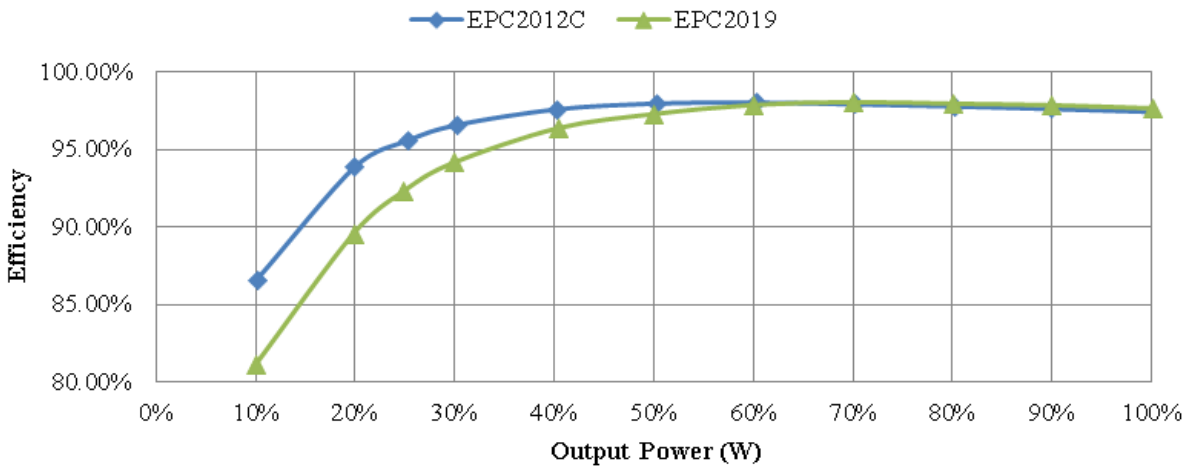


Figure 5-2: Simulated power stage efficiencies of the reconfigurable double stacked active bridge converter using EPC2012C ($R_{DS,ON}$ = 105 mΩ, $C_{OSS,eff}$ = 102.5 pF) and EPC2019 ($R_{DS,ON}$ = 55 mΩ, $C_{OSS,eff}$ = 185 pF) for the inverter switches. For these simulations, V_{in} = 380 V, V_{out} = 12V, f_s = 500 kHz, and $P_{out,rated}$ is 400W. Each transformer of Figure 5-1 has a turns ratio of 16 to 1 and an energy transfer inductance of 4.104 μH (so that L = 8.208 μH). At full power, the simulated efficiency using the EPC2012C devices is 0.25% lower than the efficiency using the EPC2019 devices. At 10% load, in the presence of hard switching, the efficiency using the EPC2012C devices is 5.5% higher than the efficiency using the EPC 2019 devices.

$$N_{opt} = \frac{2v_p}{v_s} = \frac{\frac{V_{in}}{4} + \frac{V_{in}}{4}}{V_{out}}, \tag{5.1}$$

such that the three windings have turns ratios N_{opt}:N_{opt}:1, with 1 representing the secondary. The nominal input voltage for this converter is 380V and the output voltage is 12V so that the optimal physical turns ratio of the transformer is 15.833-to-1. For practical reasons, each transformer primary will have 16 turns so it is anticipated that the current may not be a completely flattop trapezoidal waveform at the nominal operating condition.

Important considerations in the design of the transformer design are the operating frequency, which determines the magnitude of the magnetic flux, and the core area, which affects the flux density and subsequently the core loss as given by the following equations

$$B_{pk1} = \frac{V_{pk} \times \frac{T_0}{2}}{N \times \frac{A_e}{2}} = \frac{V_{pk}}{N \times 2 \times f_s \times \frac{A_e}{2}} = B_{pk2} \ , \tag{5.2}$$

$$P_{core} = K \times \left(\frac{f}{f_o}\right)^{\alpha} \left(\left(\frac{B_{pk1}}{B_o}\right)^{\beta} + \left(\frac{B_{pk2}}{B_o}\right)^{\beta}\right) \times \frac{V_c}{2} \tag{5.3}$$

where B_{pk1} is the peak magnetic flux density of one transformer primary in T, B_{pk2} is the peak magnetic flux density of the other transformer primary, V_{pk} is the peak voltage that the transformer primary sees (95 V nominally and a maximum of 102.5 V for our application), and A_e is the effective area of the core in m^2, which is halved in (5.2) because the primaries are wound around the outer leg instead of the center leg. The core loss equation of (5.3) is based on how EPCOS defines the loss parameters K (in kW/cm^3), α, β, f_o (in Hz) and B_o (in T) used in their magnetic design tool (MDT) [57]. These parameters are only defined at frequencies of 25 kHz, 50 kHz, 100 kHz, 200 kHz, 300 kHz, and 500 kHz. Values for higher frequencies are not available, although they still do provide loss curves at 700 kHz and 1 MHz. Using the loss equation for 500 kHz can be accurate for a range of frequencies above 500 kHz, but it does appear to lose accuracy at 700 kHz based on the provided curve. Therefore, the prediction of core loss at frequencies above 500 kHz is most likely lower than the actual loss. Details on the exact values used for these loss parameters as well as the calculation of the losses in this section can be found in the MATLAB code of Appendix A. Finally, V_c is the volume of the core in cm^3.

Based on the design of magnetics in Chapter 2, this converter will use a planar transformer with fully interleaved PCB windings using EPCOS N49 material. For a given operating frequency, (e.g., 500 kHz), different core sizes will result in different core loss based on (5.3). A preliminary analysis of core sizes, core loss, and winding resistance is shown in Table 5-4. From this initial analysis, the EILP43 core set is most favorable. The core loss is also heavily dependent on the switching frequency. Figure 5-3 shows a plot of the core loss across the different core sets, where each line represents a different

Table 5-4: Transformer core loss for EPCOS N49 material and winding resistance assuming an input voltage of 410 V, and operating frequency of 500 kHz, 1 skin-depth of conduction (single sided), 1 PCB layer per winding and operation at 100 °C.

Core	B_{pk} (T)	Core Loss (W)	Secondary Winding Resistance (Ω)	Primary Winding Resistance (Ω)
EILP14/3.5/5	0.8788	57.0161	0.0015	0.3840
EILP18/4/10	0.3226	11.7158	0.0018	0.4608
EILP22/6/16	0.1623	4.4541	0.0021	0.5376
EILP32/6/20	0.0980	2.4442	0.0018	0.4608
EILP38/8/25	0.0657	1.4989	0.0018	0.4608
EILP43/10/28	0.0556	1.2812	0.0017	0.4352

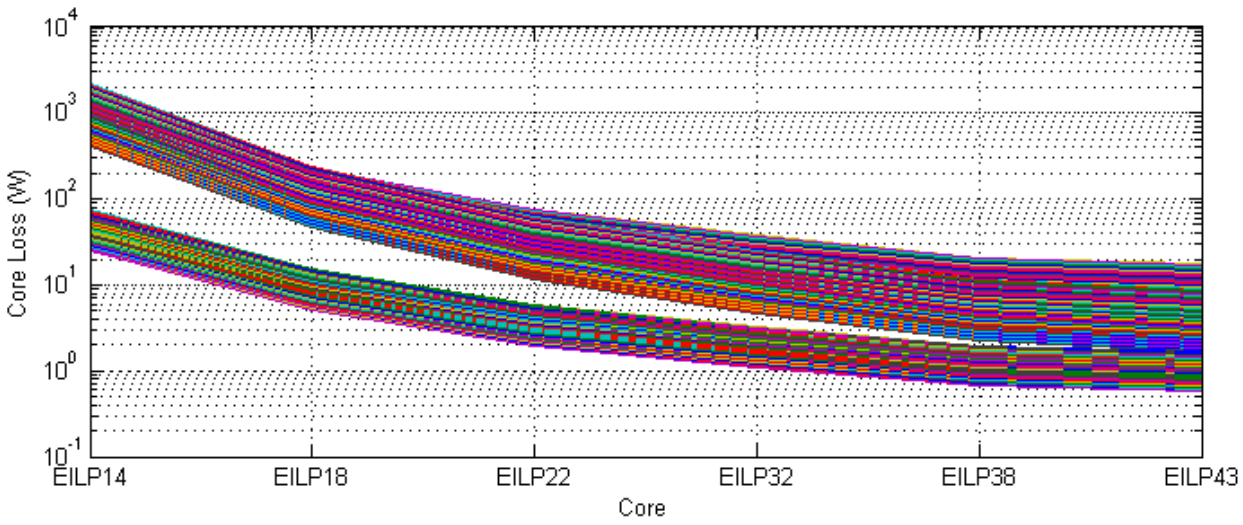


Figure 5-3: Core loss across core geometry. Each line represents a frequency from 100 kHz to 1 MHz. Calculations are based on a transformer primary voltage of ±95Vfor half a cycle. Core loss is calculated based on (5.3) with the parameters taken from the EPCOS MDT [57] depending on first the frequency and then the magnetic flux density. (The gap in the plot is due to inconsistencies between the core loss equation and the magnetic flux density over which it is valid. Because the loss is so high, this core would not be chosen.) The MATLAB code to generate this plot is provided in Appendix A.

frequency from 100 kHz to 1 MHz. Again, EILP43 appears to have the lowest loss for a given frequency.

Table 5-4 also lists the winding resistance amongst the various geometries. This is calculated as follows

$$R = \frac{\rho l}{A} = \frac{\rho\left(2ID + 2W + \frac{\pi(OD - ID)}{2}\right)}{\frac{\delta(OD - ID)}{2}}, \tag{5.4}$$

where ρ is the resistivity of copper in Ω-m (taken at 100 °C), l is the mean-length of one turn, which is related to the outer diameter, *OD*, the inner diameter, *ID*, and the width, *W*, of the core. Finally, *A* is the area of conduction, which is related to the skin-depth, δ, the outer diameter, and the inner diameter. An example of these dimensions is shown in Figure 5-4 for an E core. From Table 5-4, it can be seen that the resistance is pretty similar, so for a given current, the estimated winding loss will be roughly similar across core sets. The current through the transformer will depend heavily on the frequency because this affects the total power. For the same power transfer, a lower frequency will require a lower phase shift which can impact the RMS current values. Nonetheless, a preliminary analysis assumes a fixed current across frequency to generate the plot seen in Figure 5-5.

The total loss in the magnetic component is a summation of the core loss and winding loss. Across each frequency, there is a design that yields the minimum loss and this loss is plotted in Figure 5-6. From this graph, it can be seen that the loss predicted by the simplified models used is relatively flat

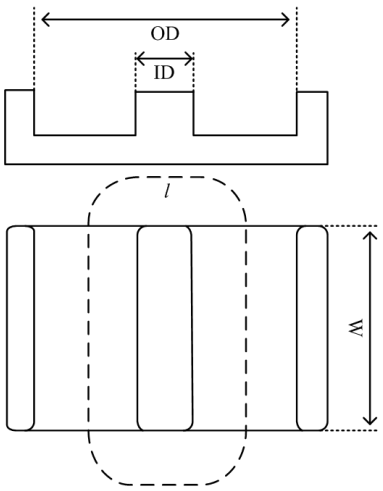


Figure 5-4: Example of how parameters to calculate resistance are listed on a datasheet.

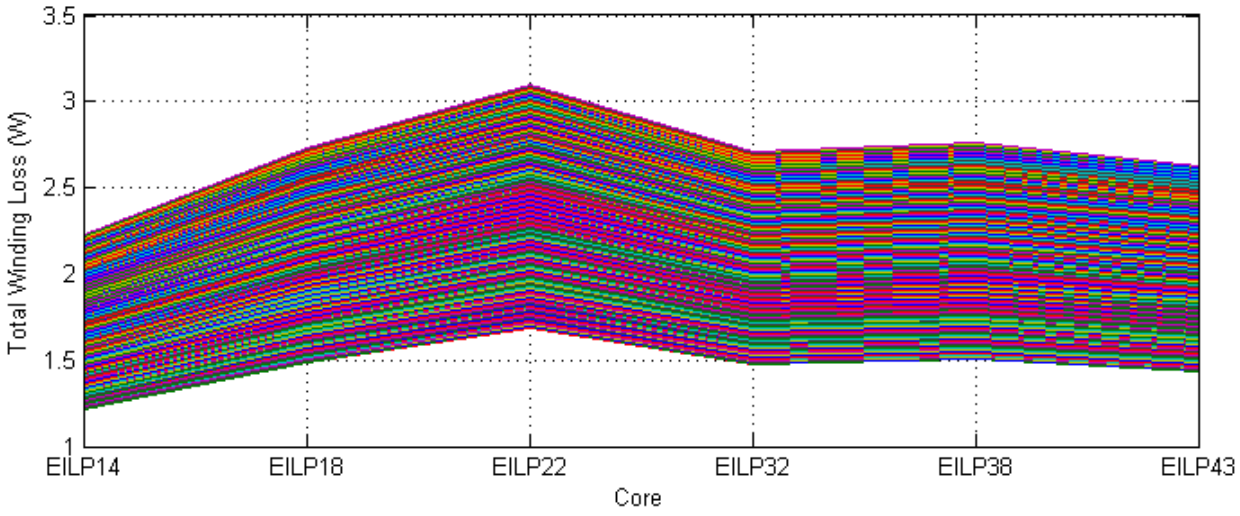


Figure 5-5: Winding loss across core geometry. Each line represents a frequency from 100 kHz to 1 MHz. Calculations are based on a transformer secondary RMS current of 37.169 A – determined from a simulation with V_{in} = 380 V, V_{out} = 12V, f_s = 500 kHz, L = 8.204 µH, and P_{out} = 400W. Winding loss for the secondary is calculated based on the mean length of a single turn, assuming one skin-depth of conduction (up to 140 µH) spread out across 4 PCB layers. It is assumed that each winding has the same winding loss, so the total winding loss is three times the loss of the secondary winding. The MATLAB code to generate this plot is provided in Appendix A.

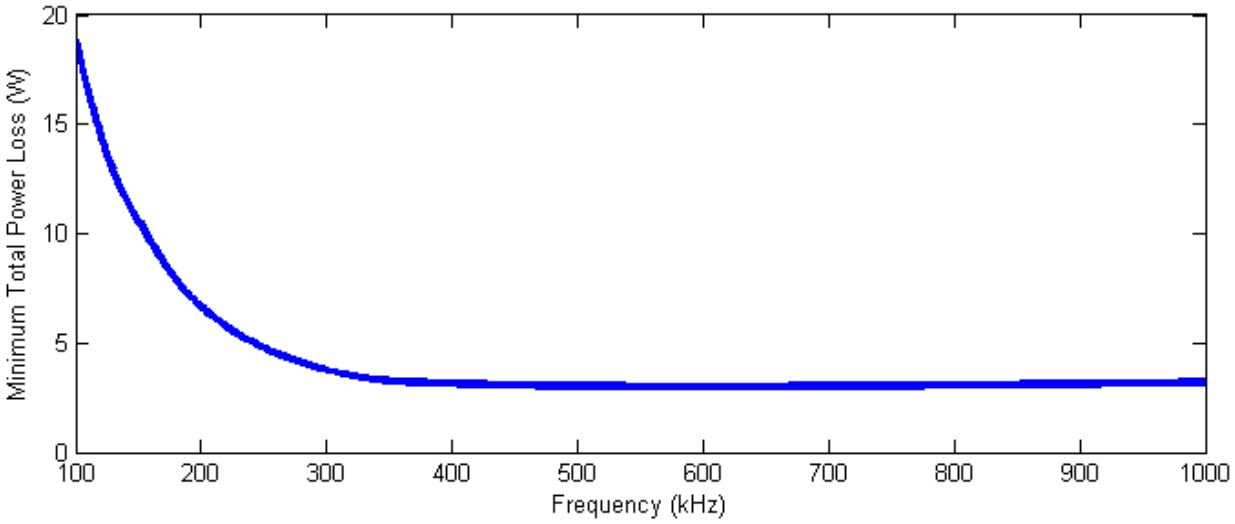


Figure 5-6: Total power loss for the lowest lost design across frequency. The total loss is calculated as the summation of the core loss and the winding loss (which were shown in Figure 5-3 and Figure 5-5, respectively). The line represents the lowest loss across six different core sets. The MATLAB code to generate this plot is provided in Appendix A.

from 400 kHz to 1 MHz. The core loss model uses EPCOS loss parameters K, α, β, f_o and B_o found in their MDT [57] but these are only defined up to 500 kHz. The core loss at frequencies above 500 kHz is likely higher than predicted. Given this, the transformer and converter were initially designed to operate at 500 kHz, but in actuality the amount of leakage inductance can heavily affect the power transfer capability. The phase shift can be used to compensate for deviations in leakage inductance (and hence reactance), but there is a maximum phase shift of $\pi/2$ (or 25% of the switching period), beyond which no more real power can be processed. There are also practical limits to the amount of phase shift that can be used due to RMS current conduction loss. A general discussion on this for DAB converters can be found in [26] and a detailed analysis for the proposed converter can be found in the Master's thesis of Rose Abramson, a co-developer of this work [78]. Therefore, our converter is actually operated at 175 kHz to be able to process 300 W at a reasonable phase shift of about 3.64% of the switching period. Based on Figure 5-6, this potentially doubles our core loss, but this is addressed at low powers by the low-power mode. It is noted that a different core material might be preferable at this reduced frequency, but this was not explored experimentally. Figure 5-7 shows a selection of EPCOS materials and their power loss for a flux density of 100 mT to 200 mT. With an input voltage of 380 V and operating at 175 kHz, one would see approximately 150 mT of flux density using ELP43.

The leakage in the transformer comes from the winding structure which is shown in Figure 4-24. For the reasons discussed in the design of the transformer in Section 2.2.2, this structure uses a fully interleaved winding pattern with multiple layers dedicated to each winding. Intended to operate at 500

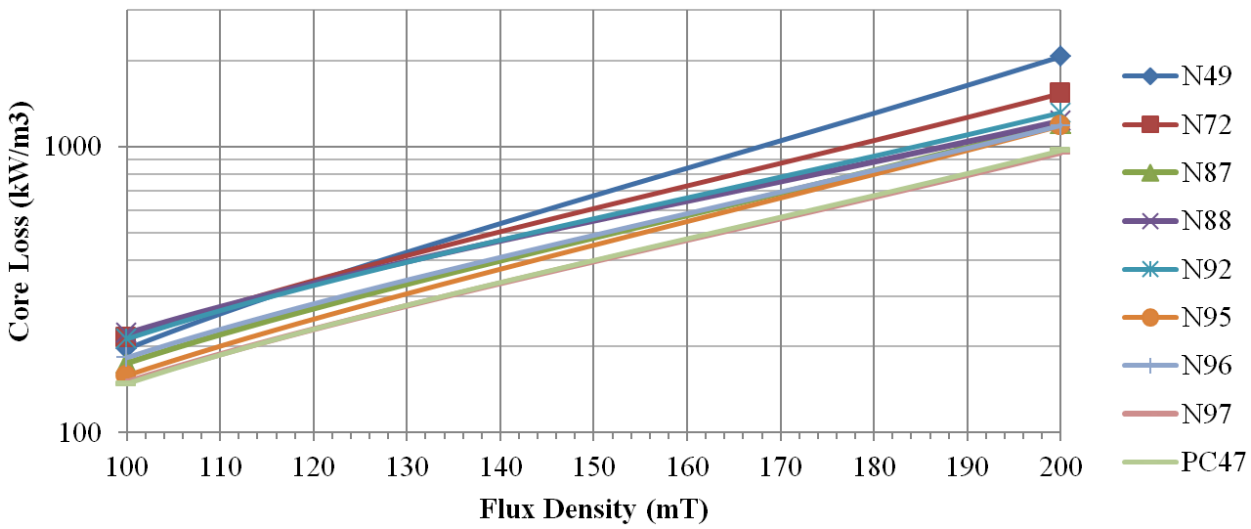


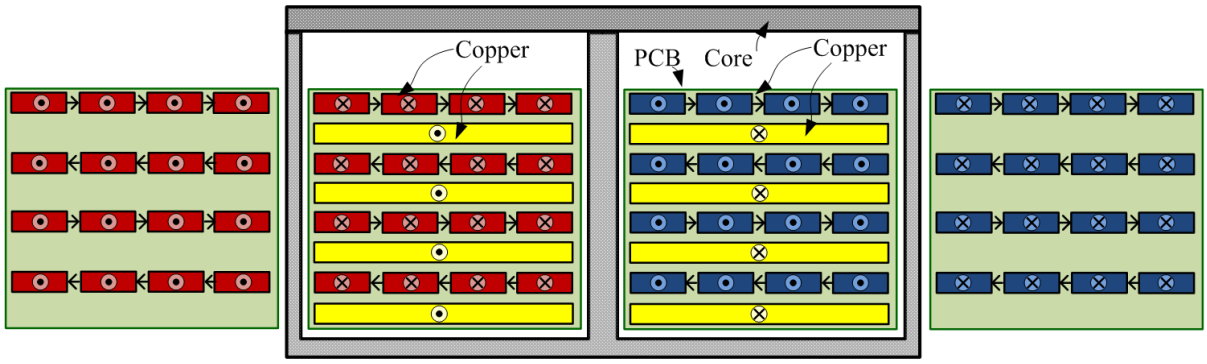
Figure 5-7: Core loss per unit volume across flux density for several EPCOS materials at 200 kHz and 100 °C [57]. The range of flux densities shown is relevant for an input voltage of 380 V and ELP43 core area.

kHz, the design features eight layers using 4 oz. copper. Unlike the design of the transformers for the ICN converter of Chapter 2, this one features turns that are outside of the core. Leakage flux outside of the transformer is driven by current in this outer copper. This helps provide the leakage inductance so that a single core can be used. With all windings open, the inductance at 175 kHz across one primary is 945 µH and the inductance across the other primary is 939 µH. The inductance at 175 kHz across one primary with the other two windings shorted is 32.1 µH. It is believed that this is the total primary-referred leakage inductance of the transformer. Another method we use to determine the total leakage inductance is through running the converter and using the input voltage, output voltage, frequency, phase shift, and output power to back calculate the inductance:

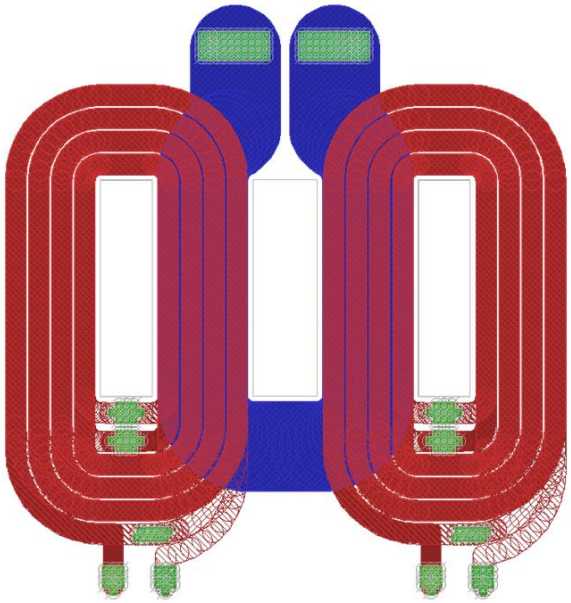
$$L_{eff} = \frac{\left(\frac{V_{in}}{4} + \frac{V_{in}}{4}\right) V_{out} N}{2\pi f_s P_{out}} \phi\left(1 - \frac{\phi}{\pi}\right) \tag{5.5}$$

It should be noted that the effective inductance will vary with efficiency. Typically, the lower the converter efficiency, the higher the effective leakage inductance.

Three winding methods were tested and compared before selecting that of Figure 5-8 for the final prototype. The first variant uses an in-board fully interleaved planar transformer winding structure as shown in Figure 5-8. The second variant is shown in Figure 5-9 and is the same as the first except a layer of 2 mil thick copper foil is wrapped around the outside the transformer with the intent of using this "shorted turn" to cancel some of the leakage flux that travels outside the core, thereby reducing the effective leakage inductance. The third variant bypasses the primary windings of the PCB and instead



(a)



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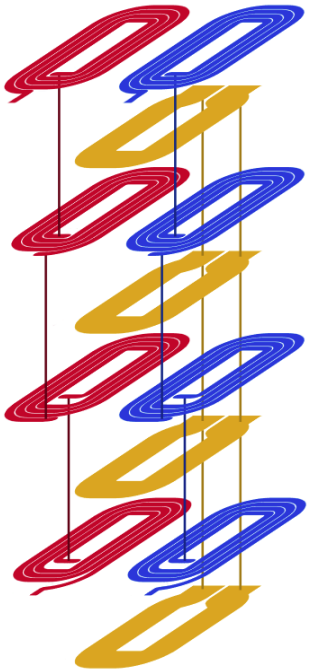


(c)

Figure 5-8: PCB winding structure for the transformer showing (a) a cross sectional view, (b) a top view, and (c) a 3D view using the EPCOS EILP43 core set in N49 material. The 3D view shows the interconnection between the 8 layers. Each odd layer (as counted from the top) has two sets of four turns for the two primary windings. All four odd layers are then connected in series to form two 16-turn primary windings. All even layers comprise the single-turn secondary winding and are connected in parallel. The windings are in 4 oz. copper. The track width of the primary windings is 2.5908 mm with 0.42 mm spacing between them. The track width of the secondary winding is 11.7 mm. The board is an 8-layer FR4 board with a finished thickness of 97 mil. Full details on the design can be seen in the layout files of Appendix D.

uses hand wound litz windings along the top plate of the core set, far from the secondary windings, as shown in Figure 5-10. The calculated effective inductance for three transformer variants is shown in Figure 5-11. From Figure 5-11, several trends can be seen. The first is that for the first and third variants, when the efficiency was low, the calculated leakage was higher. The second is that shielding the transformer with the "shorted turn" around the E core will decrease the leakage inductance by about 30% so that the same power can be delivered at a lower phase shift. It is from this that we experimentally demonstrate that external flux driven by the outer windings provides leakage inductance. But, the cost of this shielded design is an increase in circulating currents within the copper shield itself so that efficiency is ultimately lower. The hand-wound litz primary windings also lower the leakage since the windings themselves are much closer to the core, but these windings results in lower efficiency as the power is increased, most likely due to proximity effect because the primary and secondary windings are no longer interleaved. The testing of this particular variant was cut short because there was a very large voltage mismatch between the two primaries indicating the strong need for precise symmetry between windings – something that is easily accomplished in planar PCB windings. Overall, we select the design of Figure 5-8, and approximate the total primary-referred leakage inductance for this particular design to be around 32 μH (or about 16 μH per primary). In truth, the leakage inductance is distributed across primary and secondary windings and some of these effects can be seen in the waveforms of the next section.

In summary, the proposed three-winding transformer structure uses an EPCOS EILP43 core in N49 material and an interleaved 8-layer, 4 oz. PCB winding to minimize both core and winding loss. The primary turns that exist outside of the core contribute to the energy transfer leakage inductance of approximately 32 μH. It is noted that the proposed transformer structure is highly effective, and future exploration on the details of its optimal design (e.g., for current sharing among layers, optimizing leakage parameters, etc.) is likely to be fruitful.

5.1.3 Benchmark Prototypes

Earlier, two claims were made about the converter performance. The first is that by using a double stacked-bridge inverter structure, we could achieve better performance across a wider range of output power levels, even when compared to a single stacked-bridge inverter design. The second is that for the same voltage rating, we could get an improvement in performance by using GaN-based devices over Si-based devices. To validate these claims, two variants of the prototype boards were laid out. One board is designed for GaN-based inverter switches while the other board uses D2PAK Si-based devices. (The D2PAK pad offers the ease of swapping devices.) The components of the two boards are identical except for the inverter switches and their gate-drive resistances (due to the different gate capacitances of

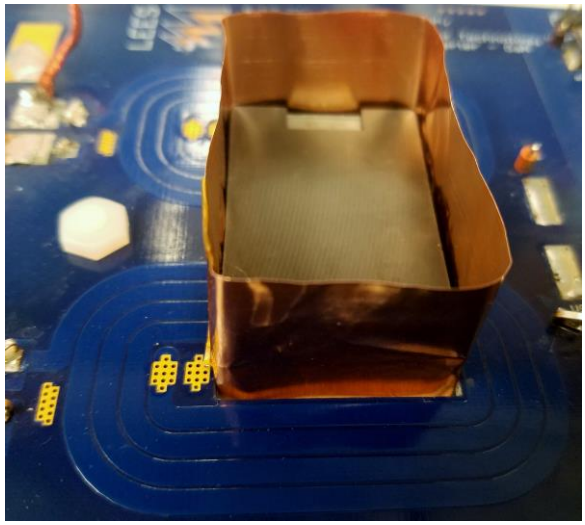
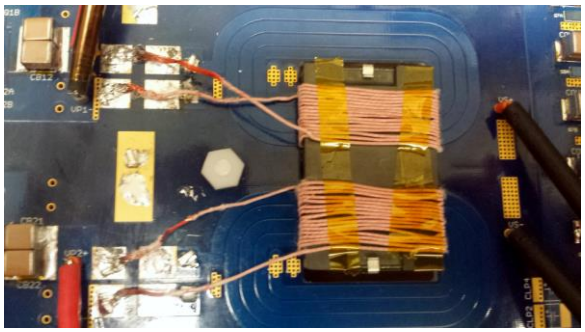
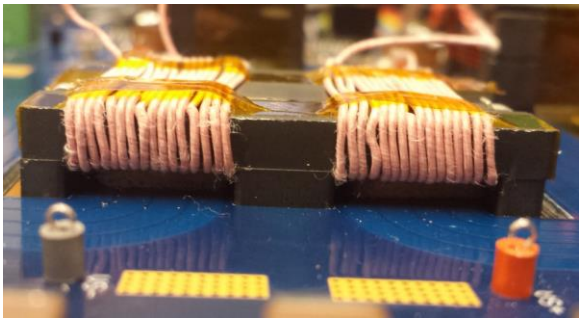


Figure 5-9: Transformer design variant with a 2 mil thick copper shield. The copper wraps around the transformer and is perpendicular to the board. It extends about 1 cm above the top of the core and below the bottom of the core.

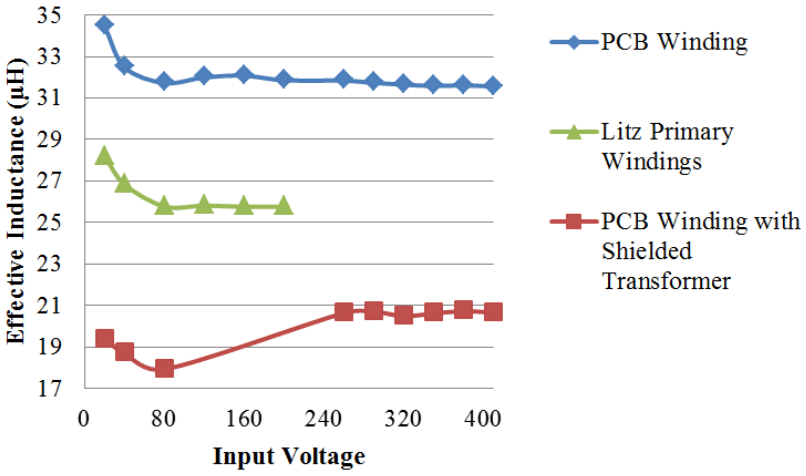


(a)

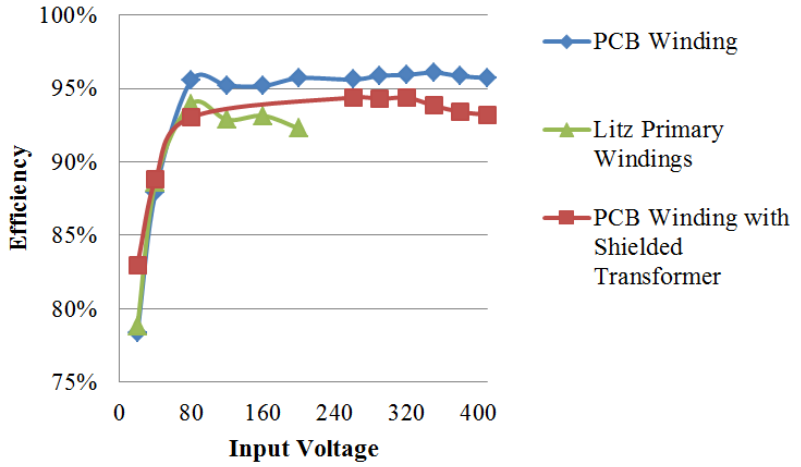


(b)

Figure 5-10: (a) Top view and (b) side view of the transformer variant with hand wound primary windings using litz wire (40 strands of 40 AWG). The onboard PCB primary windings are not connected in this case. The inductance as measured from one primary with the other primary shorted and the secondary open circuited is around 450 μH at 100 kHz and 770 μH at 500 kHz. There is a resonant peak around 760 kHz.



(a)



(b)

Figure 5-11: Calculated (a) effective inductance and (b) efficiency for three variants of the transformer design across input voltage. For all measurements, the converter was run at 175 kHz. The input-to-output voltage was kept constant at a ratio of 32 (e.g., when V_{in} = 20 V, V_{out} = 0.625 V). The first variant is the transformer as designed with a PCB winding with fully interleaved primary and secondary layers. The second variant is the same as the first except a copper foil is wrapped around the outside of the transformer core. The third variant uses the planar secondary winding but two hand-wound litz primaries. The first and third variant were run with a phase-shift of 6.24% of the total period, while the second variant was run with a phase-shift of 6.24% initially but then it was reduced to 3.9% to keep power level consistent with the other designs.

the devices). For the GaN-based board, the 200V EPC2012C is used. For the Si-based board, the Fairchild Semiconductor 200V FQD10N20L is used. The two boards have identical layouts for the transformation stage and the rectifier stage. There are only minor differences in the inverter stage due to the size difference between the D2PAK and the EPC GaN power devices. PCB layouts for both designs are shown in Appendix D and complete schematics and BOM are shown in Appendix E.

To compare between a double stacked inverter and a single stacked inverter, a single stacked inverter version is constructed by modifying the prototype board as suggested in Figure 5-12 where certain components are not populated and a foil short is used to connect the two transformer primaries and another is used to short out the unused input capacitors. For this design, higher voltage rated components are needed (see BOM of Appendix E). As the availability and maturity of GaN-based devices at higher voltage ratings are very limited, Si-based devices are used for this prototype. For the single stacked board, the Infineon Technologies 500 V superjunction MOSFET IPD50R280CE is used. For an in-depth discussion on the selection of the Si-based devices, please refer to [78].

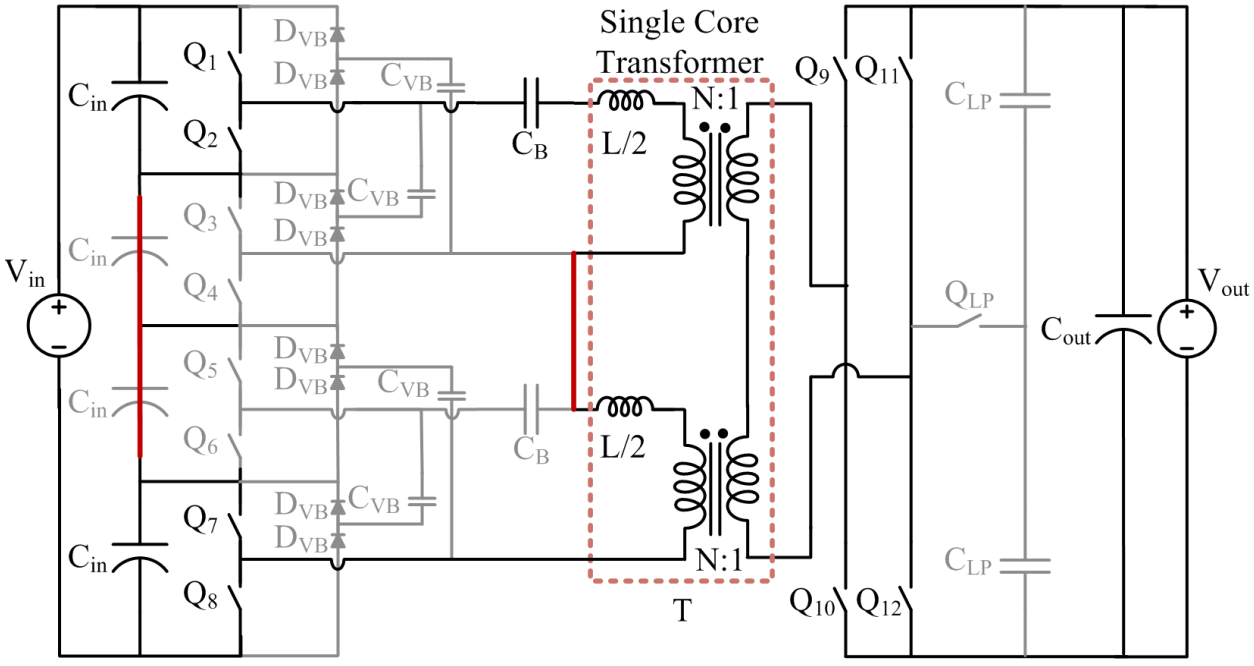


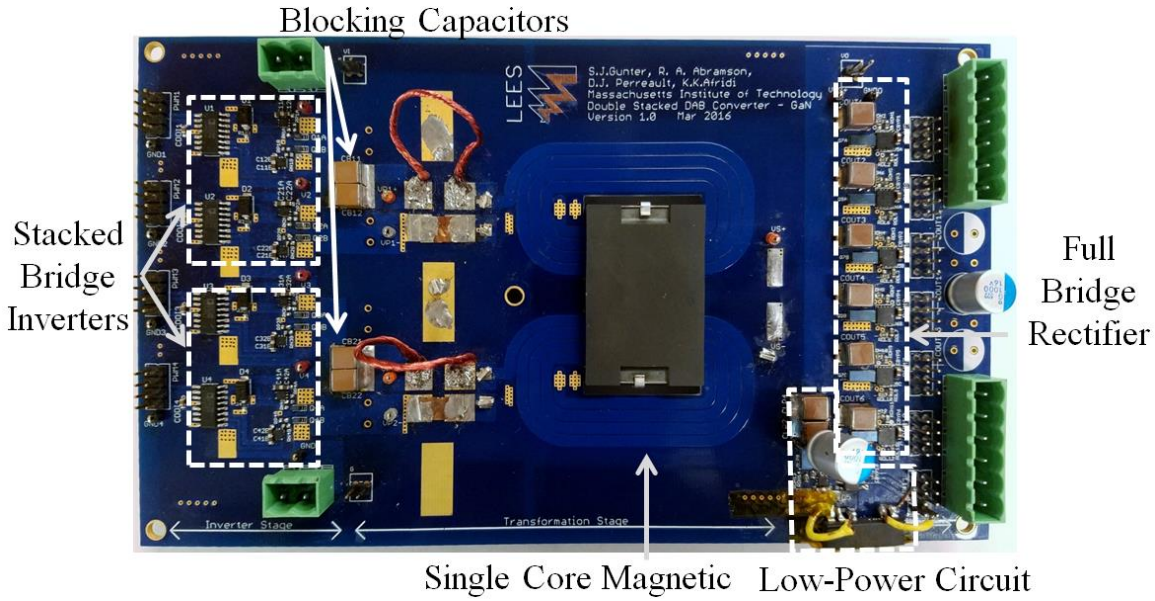
Figure 5-12: Proposed transformation of the reconfigurable double stacked active bridge converter into a single stacked active bridge converter. Several components are not populated and are shown in grey. There are two shorts applied, shown in solid red. The first is to connect the two primary windings in series. The second is to short two input capacitors which are not used.

5.2 Converter Performance

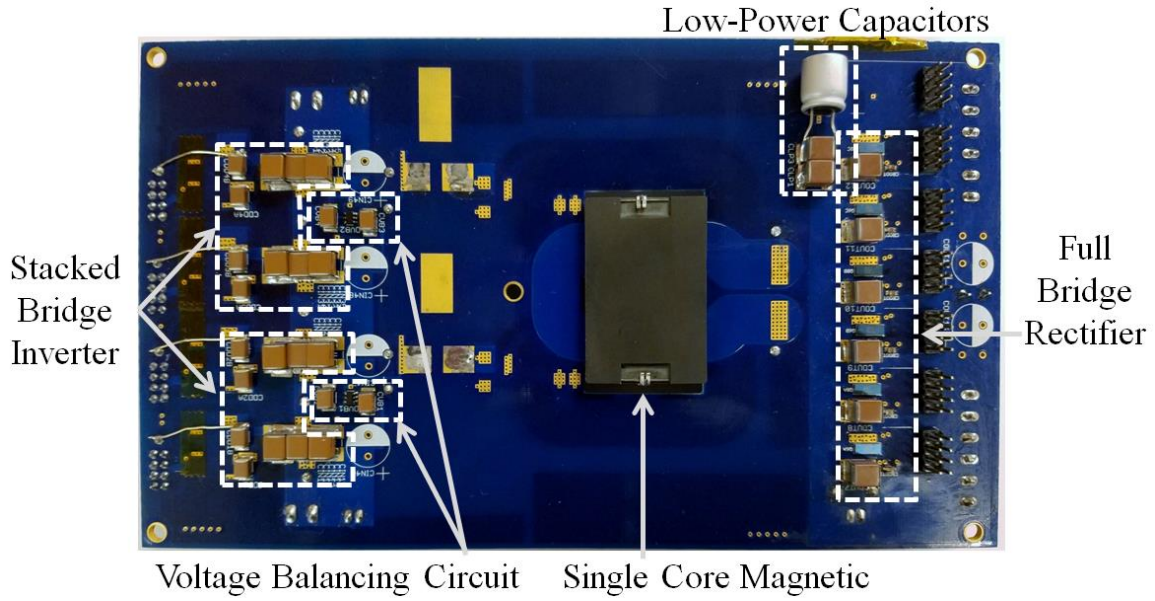
For the prototype converters, the inverter stage, transformation stage, and full-bridge rectifier stage are all implemented on the same board. There is provision for the auxiliary low-power switch and capacitors on this same board, but it was found that a daughter board placed close to the output of the transformer resulted in higher performance. The daughter board was constructed using a spare board and helps to reduce the ac resistance of the current path by being placed closer to the transformer. Figure 5-13 shows the top and bottom views of the GaN-based double stacked-bridge converter showing the original placement of the low-power circuit. Figure 5-14 shows the top and bottom views of the Si-based double stacked-bridge converter showing the placement of the daughter board for the low-power devices. One can clearly see the size difference between the (barely visible) GaN and Si devices. Figure 5-15 shows the top and bottom views of the Si-based single stacked-bridge converter, illustrating the several unpopulated components and a few paths with foil shorts.

The experimental test setup shown in Figure 5-16 uses the equipment listed in Table 5-5. A computer is used to set and send the gate drive signals using the control board developed by David Otten of MIT. It is also used to manually record operating parameters and data measured by the various meters. A single dc power supply (KLP600-4-1.2K) is used to power the board and an electronic load (HP6050A) operated in voltage source mode is used on the output. Three differential voltage probes (two Tektronix P2505 and one Tektronix THDP0200) are used to measure the two primary voltages and the secondary voltage which is displayed on an oscilloscope. The remaining fourth channel is used to measure the top transformer primary current with a Tektronix TCP202 current probe. Although not always measured, it was verified that the other transformer primary current is the same during normal mode and is phase-shifted by one cycle in low-power mode because of the difference in magnetizing current. A Yokogawa WT1800 power meter is used to measure the dc input voltage, dc input current, dc output voltage, and dc output current. It also calculates and displays a time-averaged power and efficiency. This is extremely helpful due to the open-loop nature of the control. Other digital multimeters are used to measure the voltage and current supplied to an inverter and rectifier half-bridge. A dc fan blows air across the high current output stage to prevent thermal overload (approximately 1600 LFM of air flow). A FLIR E6 thermal camera is used to take thermal measurements.

To reach the nominal operating point, the converter is first run with an input voltage of 20 V, an output voltage of 0.625 V, and a phase-shift of 208 ns. The input voltage and output voltage are increased (at the same ratio) until 380 V_{in}, 12 V_{out}, 215 W is reached. Then the phase shift is varied depending on the desired power. Full details of the converter startup and operating parameters can be found in Appendix F.

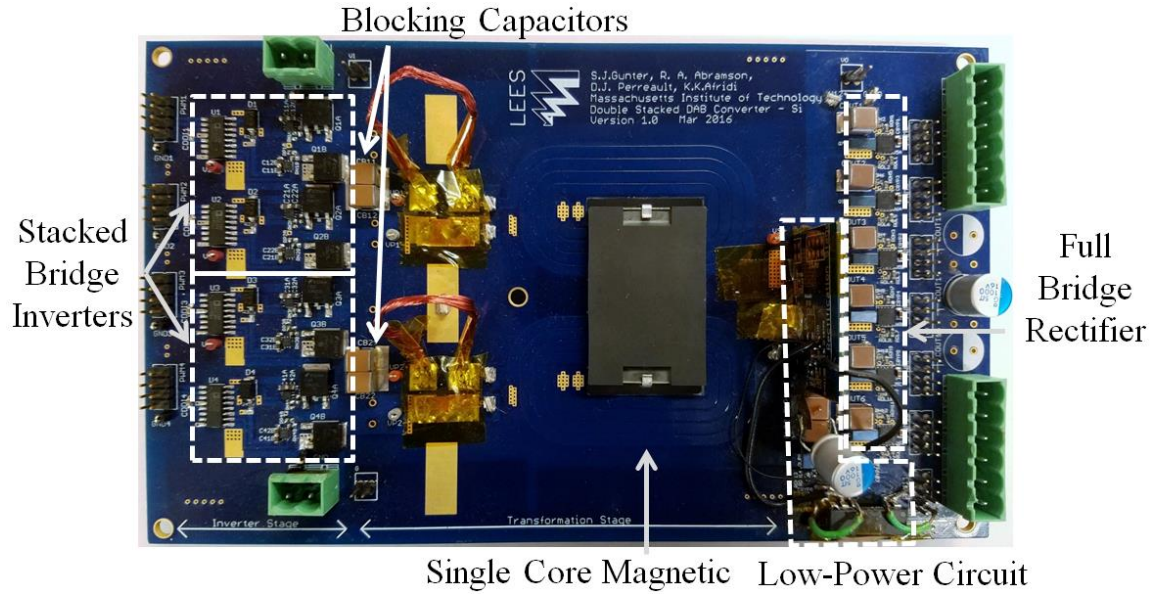


(a)

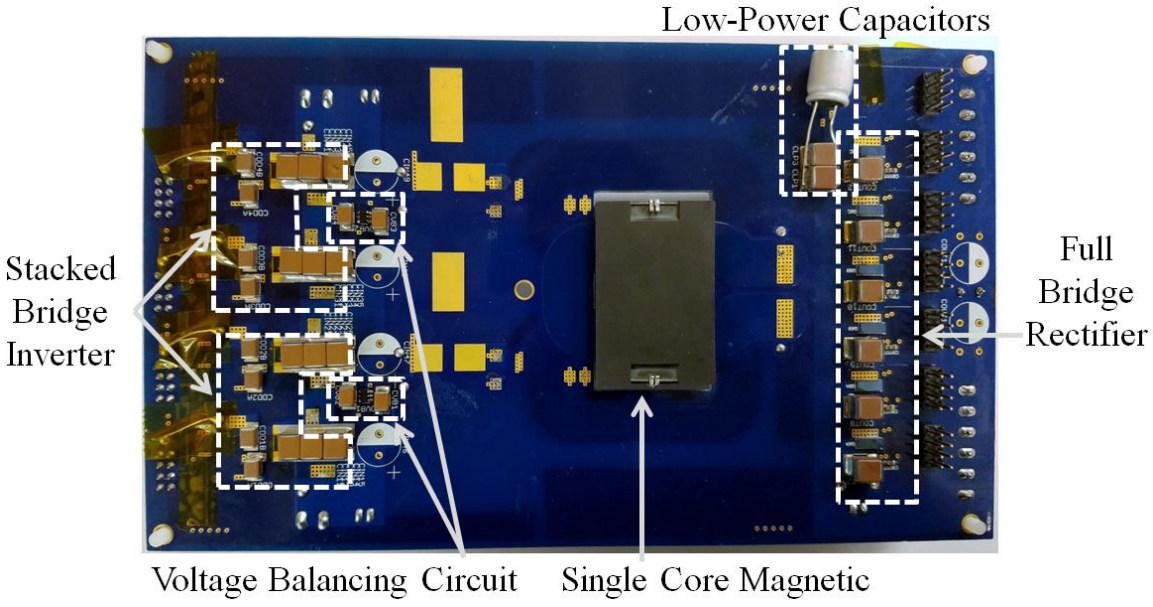


(b)

Figure 5-13: Populated GaN-based reconfigurable double stacked active bridge converter showing both (a) top and (b) bottom views. These photos most clearly show the single magnetic component with two primary windings and a single 1-turn secondary. A low-power circuit is in place on the board, but a daughter board (not shown) connected closer to the secondary of the transformer can improve the performance.

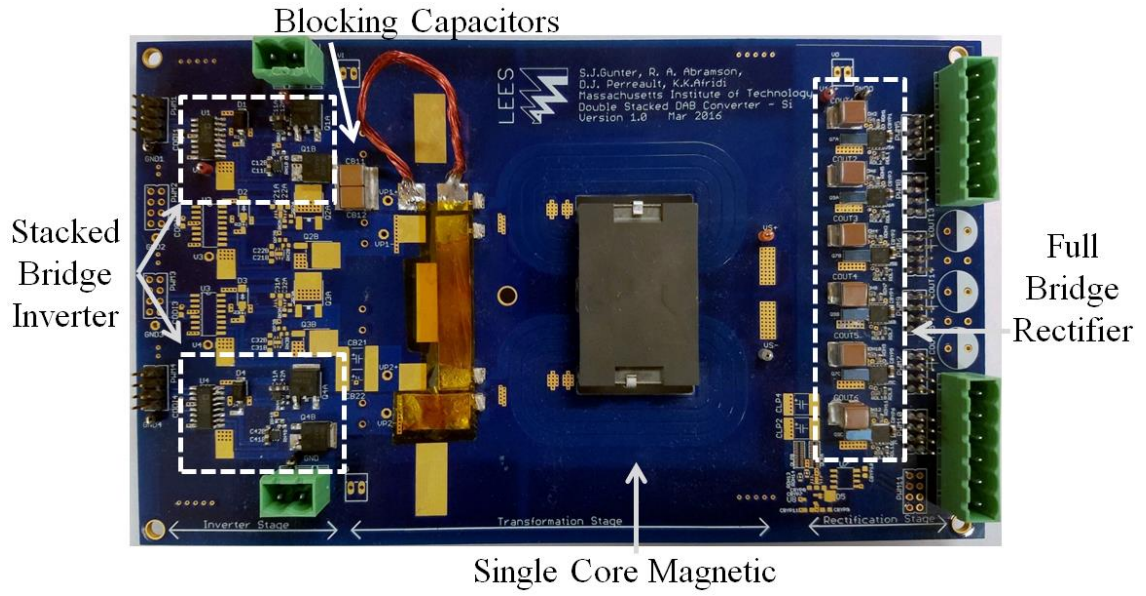


(a)

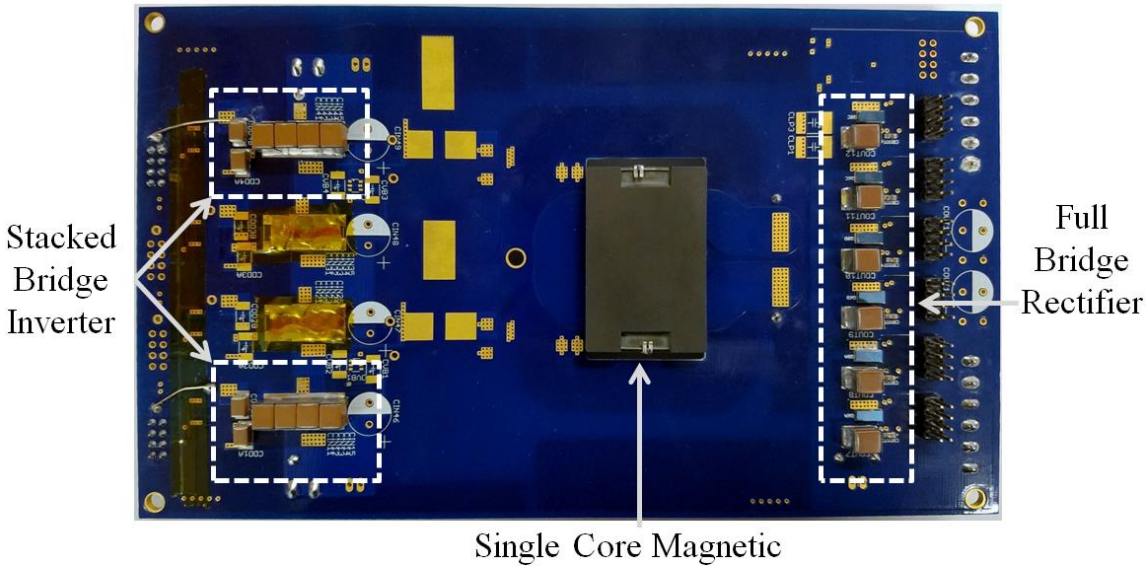


(b)

Figure 5-14: Populated Si-based reconfigurable double stacked active bridge converter showing both (a) top and (b) bottom views. A daughter board with the low-power auxiliary vertically mounted closer to the secondary of the transformer to improve the performance. The low-power capacitors are still on the main board.



(a)



(b)

Figure 5-15: Populated Si-based single stacked active bridge converter showing both (a) top and (b) bottom views. Only two half-bridges are populated with the other two shorted. The two transformer primaries are connected in series with a foil short. The voltage balancing circuits and the auxiliary low-power circuit are not populated.

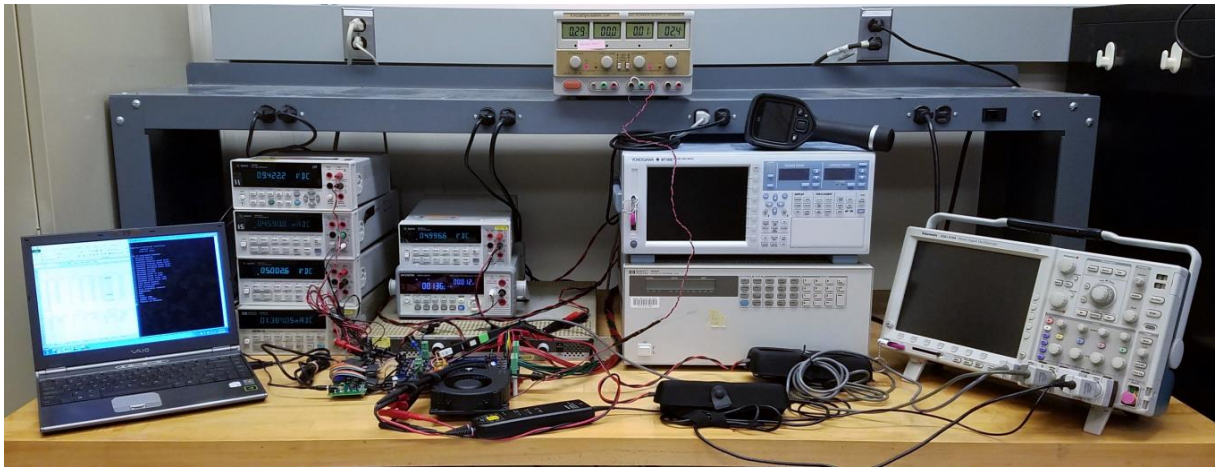


Figure 5-16: Experimental test setup for running the reconfigurable double stacked active bridge converter. Several meters are used to measure various parameters such as dc input voltage, dc input current, dc output voltage, dc output current, gate drive voltage, gate drive current, and transformer voltage and current waveforms. A comprehensive list of equipment used is found in Table 5-5.

Table 5-5: List of equipment used to run and take measurements for the reconfigurable double stacked active bridge converter

Equipment Description	Model	Purpose
Laptop	Sony Vaio VGN-SZ160P	Essential for operating the converter
DC Power Supply	KLP600-4-1.2K	
System DC Electronic Load	HP6050A	
Mixed Signal Oscilloscope	Tektronix MSO 4104	Used to measure voltage and current waveforms
High Voltage Differential Probe (x3)	Tektronix P2505 (x2), Tektronix THDP0200 (x1)	
Current Probe	Tektronix TCP202A	
Power Meter	Yokogawa WT1800	Used for efficiency measurements
Digital Multimeters (multiple)	Agilent 34401A (multiple)	
Thermal Camera	FLIR-E63900	Used for thermal measurements
DC Power Supply	HY3002D-3	Used to prevent thermal overload
Fan	Sunon PMB1212 PLB2-A	

5.2.1 Converter Waveforms Across Input Voltage

It is well known that the traditional Dual Active Bridge (DAB) converter works very well when its input voltage to output voltage ratio is the same as the physical turns ratio of the transformer. If the input voltage to output voltage ratio is higher or lower than the turns ratio, then the current will no longer continue to be a flattop trapezoidal waveform. This behavior is illustrated in Figure 5-17. This behavior can lead to increased loss from the higher RMS current (for the same average current) and potentially

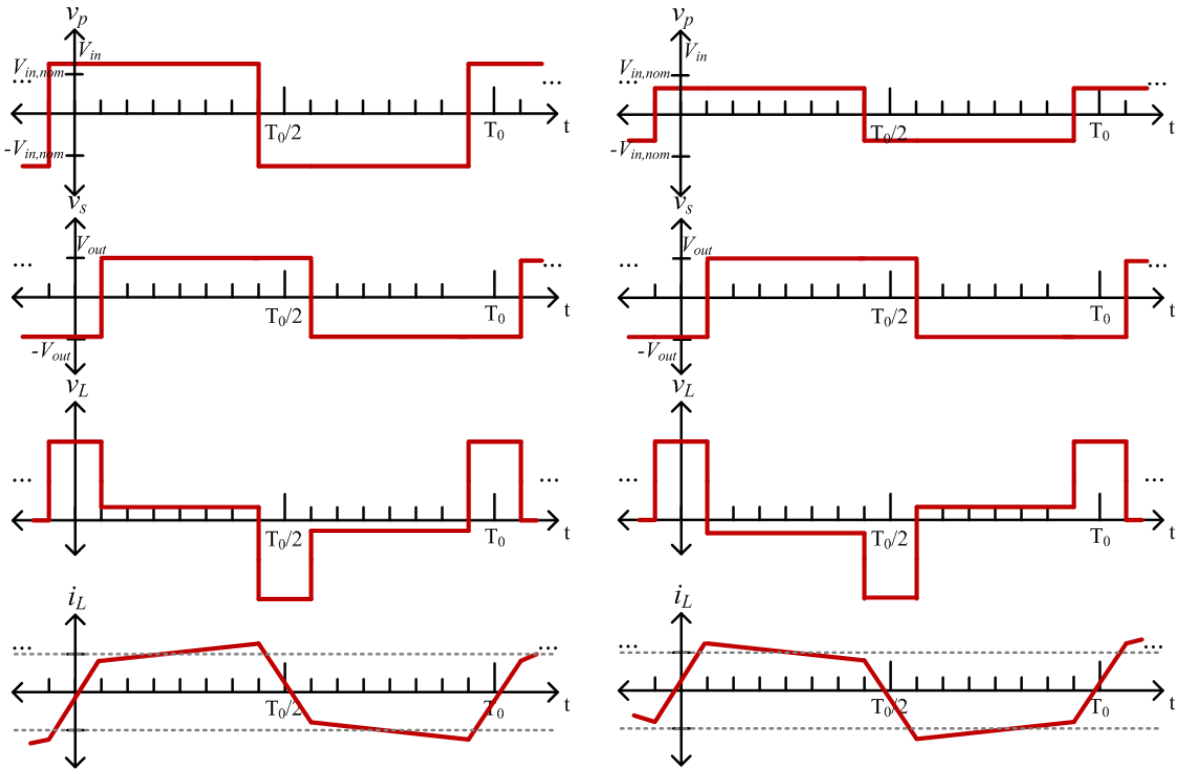
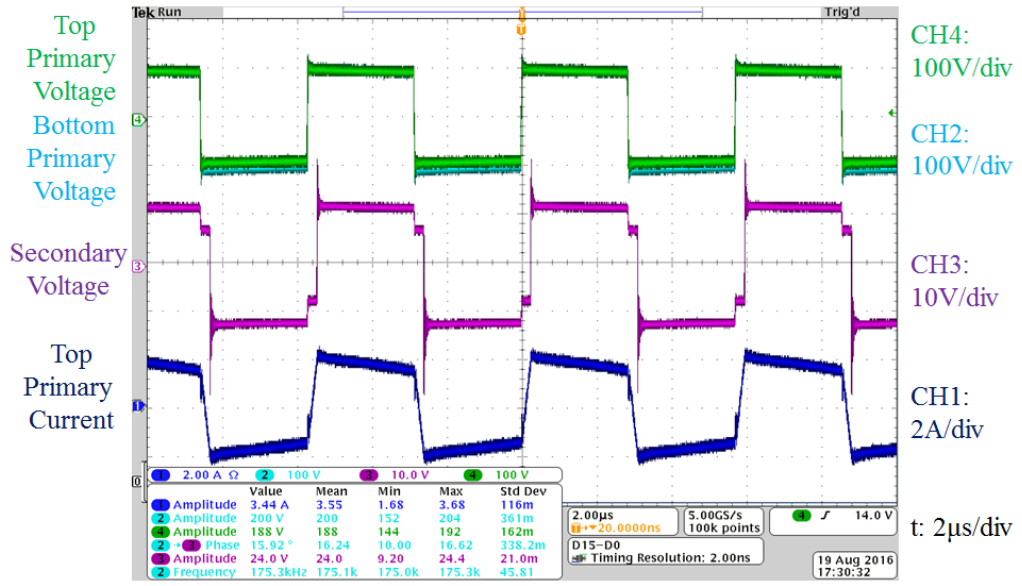


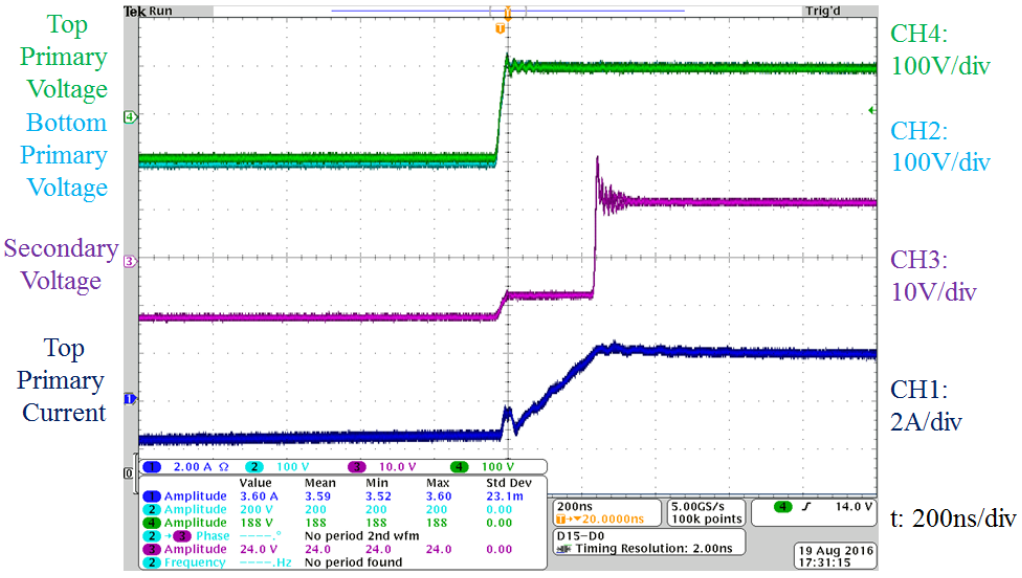
Figure 5-17: (a) Example operating waveforms of the DAB with an input voltage that is higher than the nominal input voltage (the voltage at which the input voltage divided by the output voltage is equal to the transformer turns ratio). Because the input-to-output voltage ratio is greater than the transformer turns ratio, the current no longer has a flat top. The grey dashed lines in the current plot represent the amount of current necessary to ensure ZVS on both the rectifier and inverter. In this example, the rectifier loses ZVS. (b) Example operating waveforms of the DAB with an input voltage that is lower than the nominal input voltage so that the input-to-output voltage ratio is lower than the transformer turns ratio. In this example, the inverter loses ZVS.

from a loss of ZVS. By using lower device off-state capacitance, we are able to help alleviate some of these loss mechanisms and maintain high efficiency for a range of input voltages.

Due to the increased current, we examine the operation of the Si-based reconfigurable double stacked active bridge converter of Figure 5-13. The EPC2012C device is rated for a continuous current of 5 A, however precaution was taken to avoid thermal overload of the device. The nominal operating point is with an input voltage of 380 V, an output voltage of 12 V, and 300 W delivered to the load using a phase shift of 287 ns (or approximately 5% of the 175 kHz switching period). Figure 5-18 shows the transformer primary and secondary waveforms at this operating point. It can be seen that the current into the top primary is not exactly a flattop trapezoidal waveform because the 190 V applied to the primaries divided by the 12 V applied to the secondary is lower than the physical turns ratio of the transformer (15.833 versus 16). The small dip in the secondary voltage before each switch transition indicates the presence of some leakage inductance distributed along the secondary winding. The primary current has a



(a)



(b)

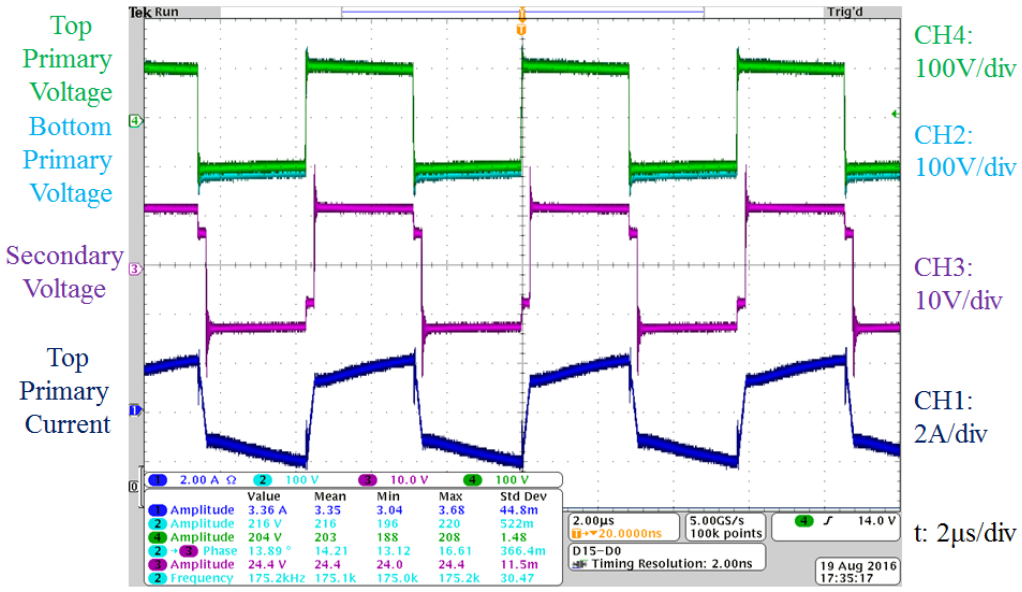
Figure 5-18: Operating waveforms for the Si-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, P_{out} = 301 W, and ϕ = 0.3156 radians. (a) Shows four periods and (b) zooms in on the switch transitions. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

small divot right when the transformer voltage switches from low to high. This is the ZVS current for the inverter and is an important factor in achieving the high efficiency 95.4%.

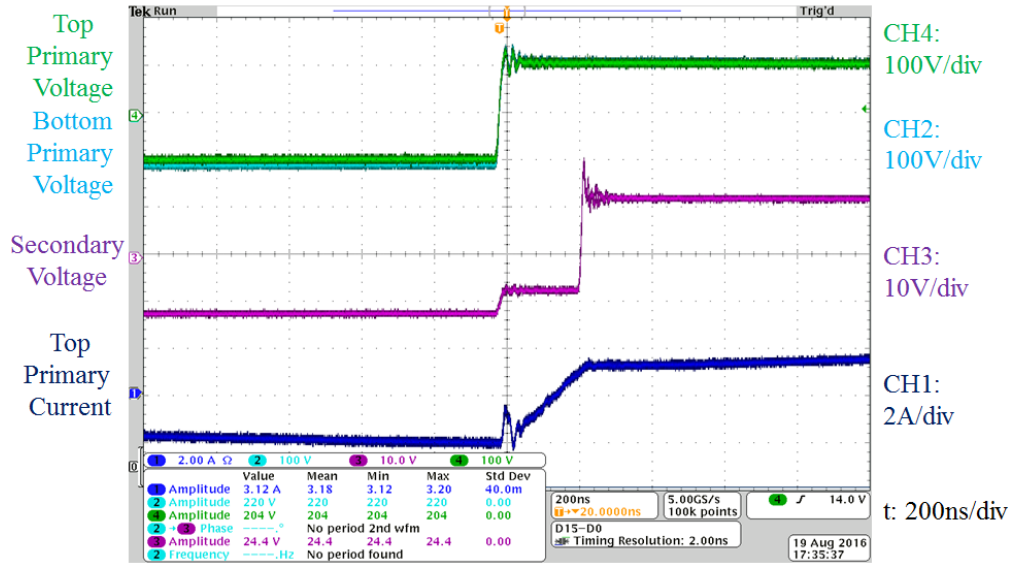
As a comparison, consider the operating point when the input voltage is increased to 410 V. For the same phase shift, an increase in the input voltage will increase the output power. To compensate, the phase shift is lowered to 250.64 ns (or approximately 4.4% of the 175 kHz period). Figure 5-19 shows the transformer primary and secondary voltage waveforms at this operating point. It can be seen that the current into the top primary slopes upward when the transformer primary voltage is high because now the 205 V applied to the primaries divided by the 12 V applied to the secondary is higher than the physical turns ratio of the transformer (17.083 versus 16). The current still has the divot and ZVS is still achieved on the inverter for a total efficiency of 96%. This efficiency is actually higher and may be due the lower phase shift and a lower dc input current so the transformer winding loss may be lower.

On the other end, consider a lower input voltage of 350 V. The phase shift is now increased to 334 ns (or approximately 5.8% of the 175 kHz period). The waveforms of Figure 5-20 show that the current is sloping significantly because now the 175 V applied to the primaries divided by the 12 V applied to the secondary is even lower than the physical turns ratio of the transformer (14.58 versus 16). The current of Figure 5-20(b) still has a divot and ZVS is still achieved, but the current is closely reaching the limit at which full ZVS can be achieved. At this input voltage, the converter can operate reasonably efficiently, at 94.1% but is lower likely due to the higher dc input current combined with the higher phase shift and non-flattop trapezoidal current which has a higher RMS current.

This converter was designed and built to operate very efficiently around the nominal operating point of 380 V_{in} where it is expected to operate for a vast majority of the time. It can operate quite well from an input voltage of 350 V to 410 V as demonstrated. Below this voltage, the RMS current at full load begins to present a problem for the rectifier devices of the prototype. While we do parallel rectifier devices to spread out power dissipation and a fan blows air across the output stage (at approximately 1600 LFM), some devices did experience thermal overload (over 140 °C) when operated at an input voltage of 320 V as power was increased to 300 W. It's possible this limitation in the prototype design can be alleviated through better measures for cooling the devices. If a very wide input voltage range is desired for normal operation, the turns ratio of the transformer could be lowered to be optimal somewhere around the midpoint of the input voltage range. Power supplies for 380 V distribution are expected to be able to run for just over 15 minutes at 260 V, but nominally they are expected to run from 360 V to 410 V [9]. An issue with the non-packaged EPC GaN devices is that when they fail, they tend to destroy the pad they were soldered to, potentially damaging the board. To prevent this from happening, the converter is simulated to the lower input voltage range instead of experimentally run.

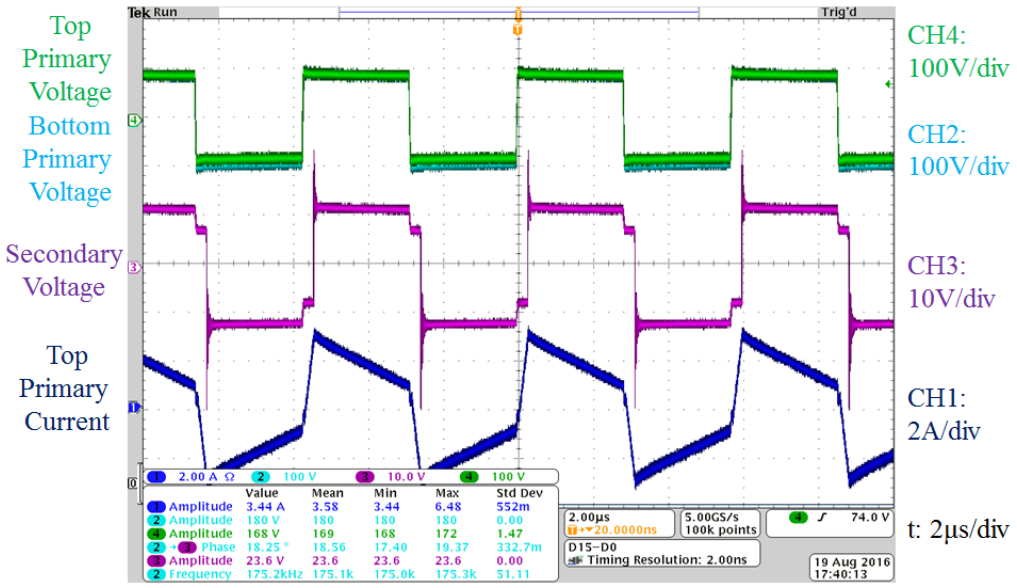


(a)

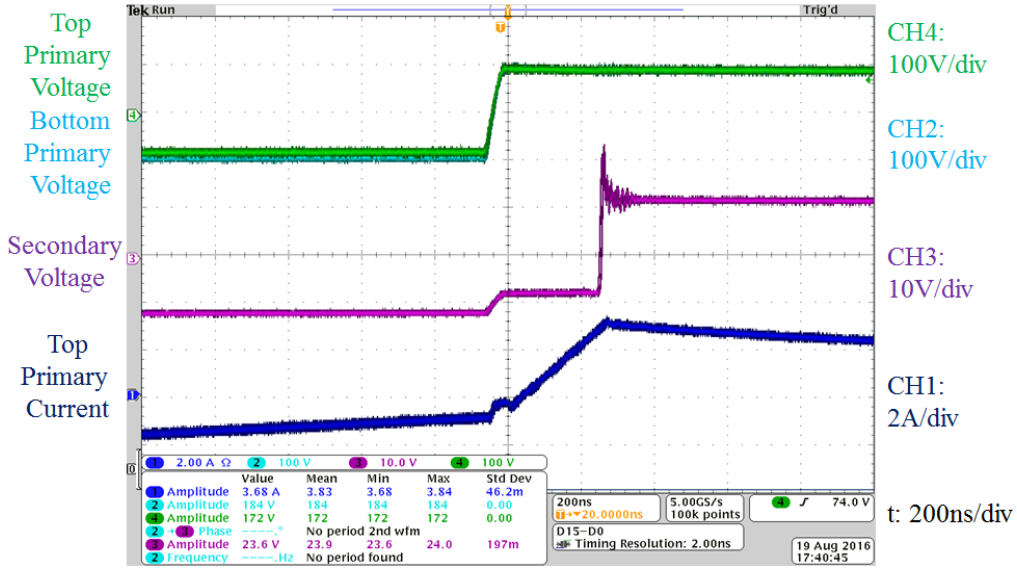


(b)

Figure 5-19: Operating waveforms for the Si-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 410 V, V_{out} = 12 V, P_{out} = 299 W, and ϕ = 0.2756 radians. (a) Shows four periods and (b) zooms in on the switch transitions. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.



(a)



(b)

Figure 5-20: Operating waveforms for the Si-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 350 V, V_{out} = 12 V, P_{out} = 299 W, and ϕ = 0.3671 radians. (a) Shows four periods and (b) zooms in on the switch transitions. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

A simulation was developed based on experimentally gathered data. The total primary-referred leakage of 32 μH is split across the two primary windings and the secondary winding. Based on the small dip in the secondary voltage, there is 14 μH placed in series with each transformer primary and the remaining 4 μH is referred over to the secondary, evenly split into 7.8125 nH in series with each terminal of the secondary winding. The turns ratio is still 16 to 1 for each transformer, but the magnetizing inductance as seen from the primary is 925 μH. Each primary winding has a winding resistance of 88.5 mΩ and the secondary has a winding resistance of 0.346 mΩ based on conduction through 4 layers of 4 oz copper. The core loss is modeled by a resistor in parallel with the magnetizing inductance. Its value is based on the core loss equations of (5.2) and (5.3) which will also depend on the operating voltage. The equivalent resistance across each transformer primary is calculated as the applied voltage squared divided by half of the total core power from (5.3), i.e.,

$$R_{core} = \frac{\left(\frac{V_{in}}{4}\right)^2}{\left(\frac{P_{core}}{2}\right)} \tag{5.6}$$

The switching devices for the GaN-based board are modeled based on EPC2012C and EPC2023 parameters. The on-state resistance of each inverter device is 105 mΩ and the off-state capacitance is 102.5 pF. The on-state resistance of each rectifier device is 2.6 mΩ and the off-state capacitance is 500 pF. Technically, these values should increase as the temperature increases and voltage decreases, but for simplicity, they are kept constant. Full details of the simulation are provided in Appendix C.

The simulated efficiencies when operated at full power as input voltage varies are shown in Figure 5-21. It can be seen that at lower input voltages, the efficiency drops. While a lower input voltage does correspond to a lower core loss (reduced by almost a factor of 4 between an input voltage of 410 V and 260 V), the sloping of the transformer current no longer allows for ZVS as shown in the simulated

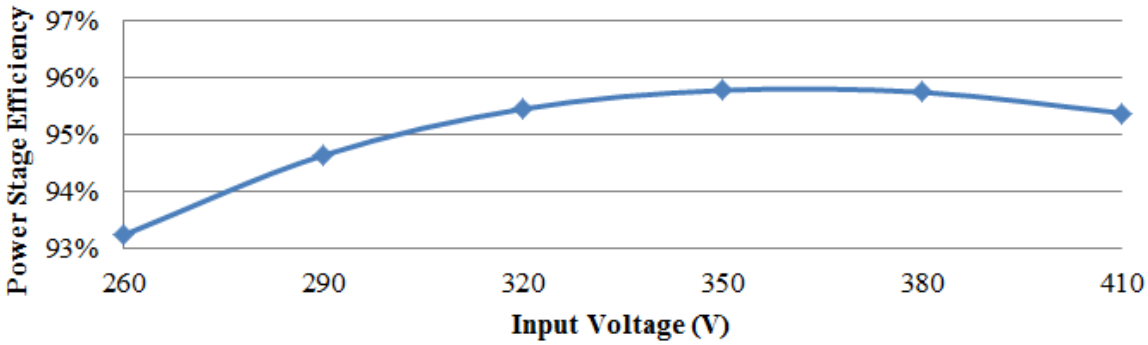
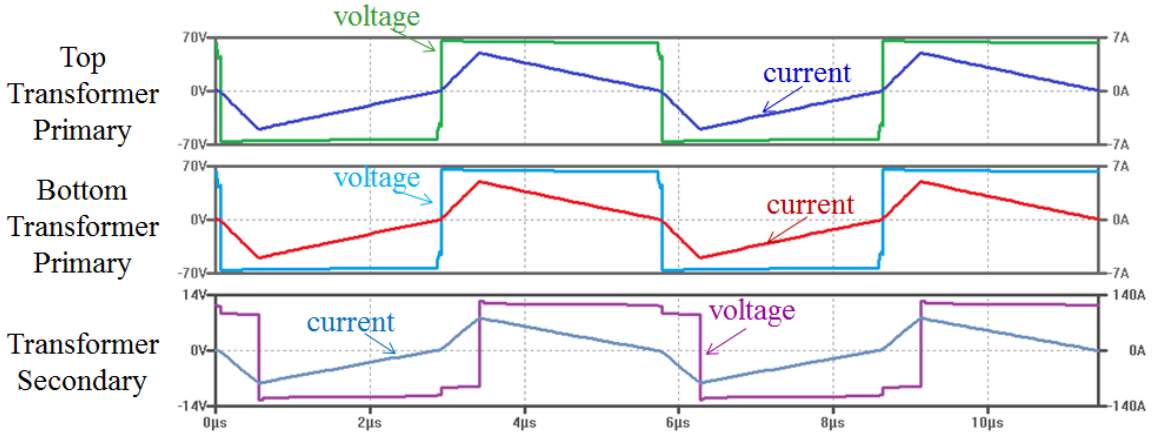


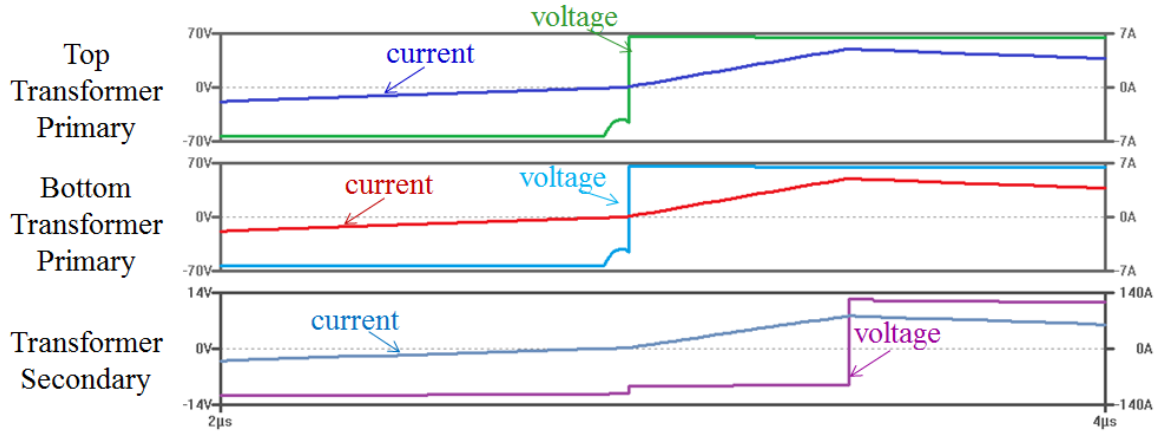
Figure 5-21: Simulated efficiency for the GaN-based reconfigurable double stacked active bridge converter across input voltage when operated in normal mode with V_{out} = 12 V, P_{out} = 300 W, N = 16, and switching dead-time = 130 ns.

waveforms of Figure 5-22. It is also seen that the RMS current through the switching devices almost doubles as shown in Figure 5-23. Based on datasheet parameters and paralleling of devices, the prototype should be able to handle the total current. It is possible that there is unequal sharing of current. Furthermore, the EPC2023 device has 30 solder bars and the high number of layers and thick copper used in the prototype present great difficulty in ensuring all connections are made.

This prototype was optimized to be extremely efficient at the nominal operating point where the input voltage is 380 V and the output voltage 12 V. The design and operating modes were intended to keep efficiency high across output power, not necessarily input voltage. The prototype can operate efficiently as the input voltage is varied by ±30 V (or almost 8%), but the construction of the prototype



(a)



(b)

Figure 5-22: Simulated waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 260 V, V_{out} = 12 V, P_{out} = 301 W, N = 16, ϕ = 0.3671 radians and switching dead-time = 130 ns. (a) Shows two periods and (b) zooms in on the switch transitions. For each figure, the top pane waveforms are the top transformer's primary voltage and current, the middle pane is the bottom transformer's primary voltage and current, and the bottom pane is the secondary's voltage and current.

does present issues at a greater voltage range (particularly at lower voltages). It's very possible a much wider range is possible with a slightly lower transformer turns ratio. For example, simulating the converter with a turns ratio of 14 (instead of 16) provides the simulated efficiency curve of Figure 5-24 and rectifier RMS current of Figure 5-25. It can be seen that the efficiency is high for the full input voltage of 260 V to 410 V and the RMS current is lower. Therefore, a wide-input voltage range design is possible although not implemented in this work.

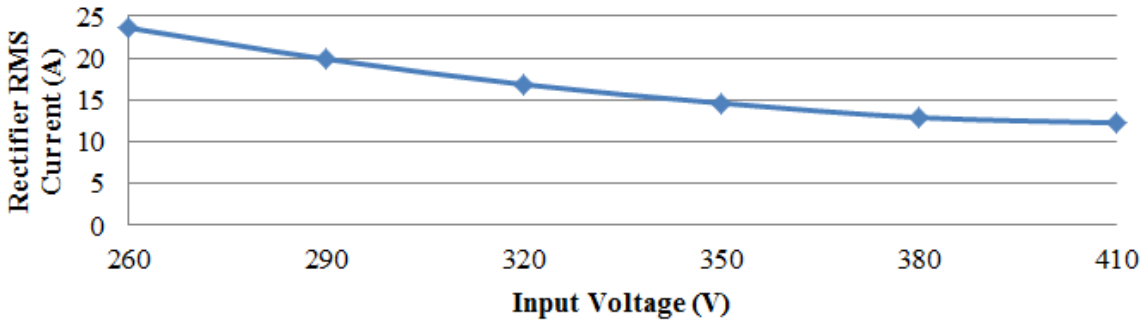


Figure 5-23: Simulated rectifier RMS current for the GaN-based reconfigurable double stacked active bridge converter across input voltage when operated in normal mode with V_{out} = 12 V, P_{out} = 300 W, N = 16, and switching dead-time = 130 ns.

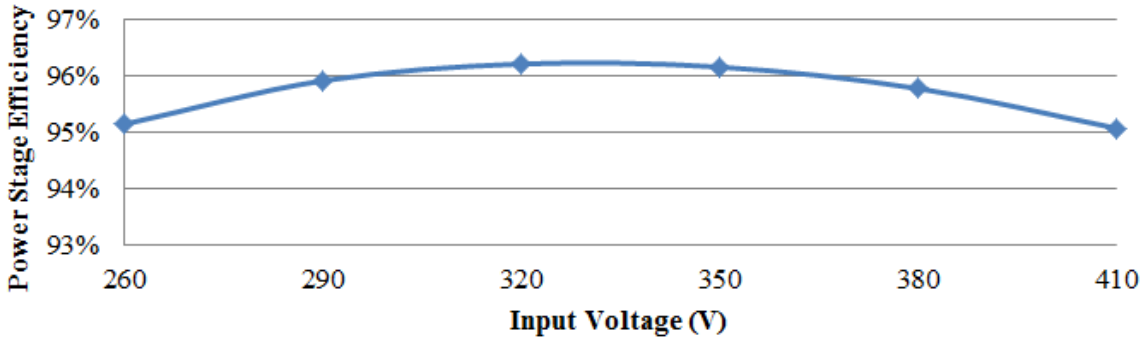


Figure 5-24: Simulated efficiency for the GaN-based reconfigurable double stacked active bridge converter across input voltage when operated in normal mode with V_{out} = 12 V, P_{out} = 300 W, N = 14, and switching dead-time = 130 ns.

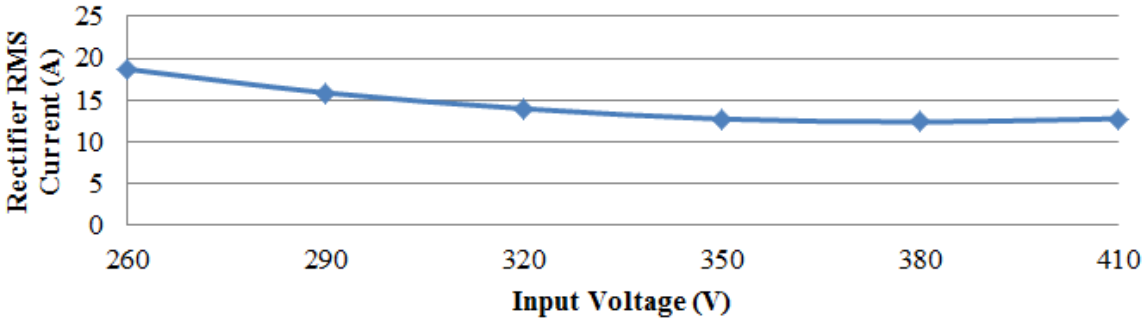
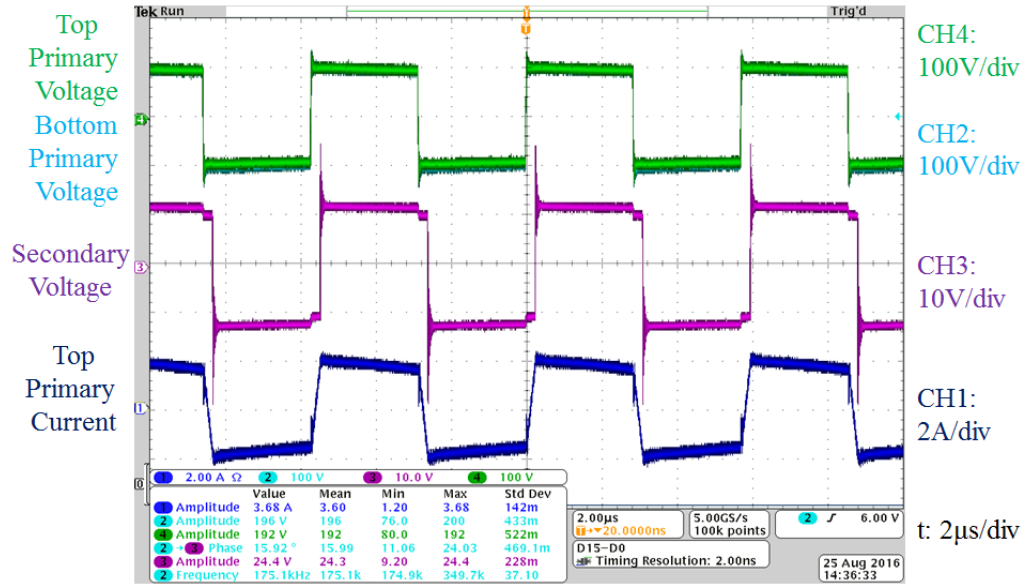


Figure 5-25: Simulated rectifier RMS current for the GaN-based reconfigurable double stacked active bridge converter across input voltage when operated in normal mode with V_{out} = 12 V, P_{out} = 300 W, N = 14, and switching dead-time = 130 ns.

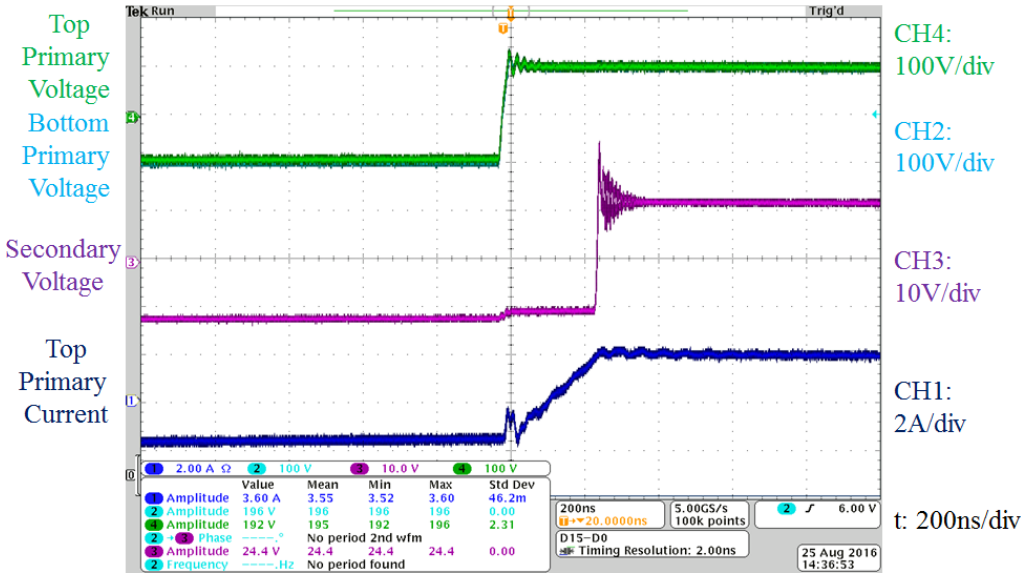
5.2.2 Converter Performance Across Output Power under Normal Operation

The reconfigurable double stacked active bridge converter can operate across some input voltage variance, but it was designed to operate very efficiently across a wide output power range. To vary power, phase-shift control between the inverter and the rectifier is used such that the rectifier voltage lags the two nominally identical inverter voltages with frequency kept constant. (It is noted that other means of control are possible, including phase shifting of the inverter legs and/or using variable operating frequency among other approaches.) The nominal operating point is an input voltage of 380 V and an output voltage of 12 V. The converter has been tested for delivery of power from a full load of 300 W down to 10 W (or 3.3% load). Each of the three prototype boards has different performance across this load range.

First we examine the operation of the GaN-based reconfigurable double stacked active bridge converter of Figure 5-13. Figure 5-26 shows the operating waveforms when the input voltage is 380 V, the output voltage is 12 V, and 300 W is delivered to the output. At full power, the secondary voltage is phase-shifted a significant amount behind the primary voltages and the current ramps up. When all voltages are high (or low), the current has a more level slope. It is not zero because the 190 V applied to the primaries divided by the 12 V applied to the secondary is lower than the physical turns ratio of the transformer (15.833 versus 16). The small dip in the secondary voltage before each switch transition indicates the presence of some leakage inductance distributed along the secondary winding. At this high power operating point, there is sufficient current to ensure ZVS of both the inverter and the rectifier. Alternatively, consider the operating point of Figure 5-27 when the converter delivers about 100 W to the output. Here, the secondary voltage is much closer to the primary voltages so that the current has a much lower amplitude. It can be seen that at the inverter switch transition, the primary voltage rises up slowly but starts to flatten out before reaching the full amplitude indicating that the inverter starts to lose ZVS. Increasing the dead-time beyond the existing 94 ns is not expected to improve performance. Some high frequency ringing is seen in the primary voltage waveforms and the primary current. These effects are abundantly clear at even lower operating points, such as that of Figure 5-28 when the converter delivers 30 W. At this power level, there is hardly any current available to ensure ZVS so the primary voltage barely rises up. The inverter switches hard switch and cause a high amount of ringing in the primary waveforms. The loss of ZVS at these lower power levels does affect the efficiency shown in Figure 5-29. Above 120 W, the converter can deliver power very efficiently but below this, the efficiency starts to degrade. It achieves a full load efficiency of 95.9%, a peak efficiency of 97.0%, an efficiency of 87.6% at 10% load, and an efficiency of 66.0% at 3.3% load. These efficiencies do include gating power loss. A brief description of the measurement method can be found in Appendix F and full details can be found in [78]. Full operating parameters and details can be found in Appendix F.

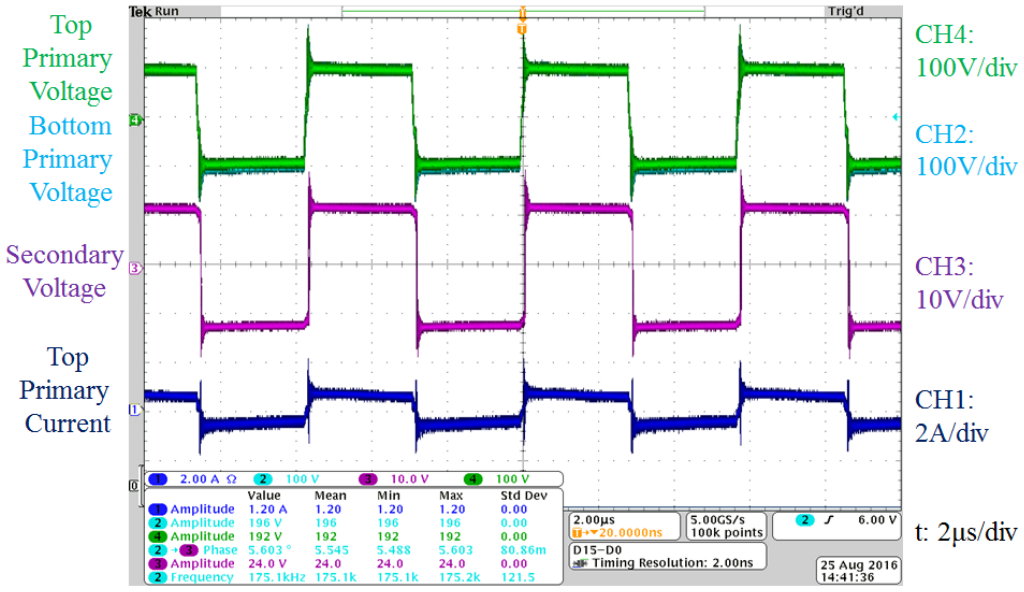


(a)

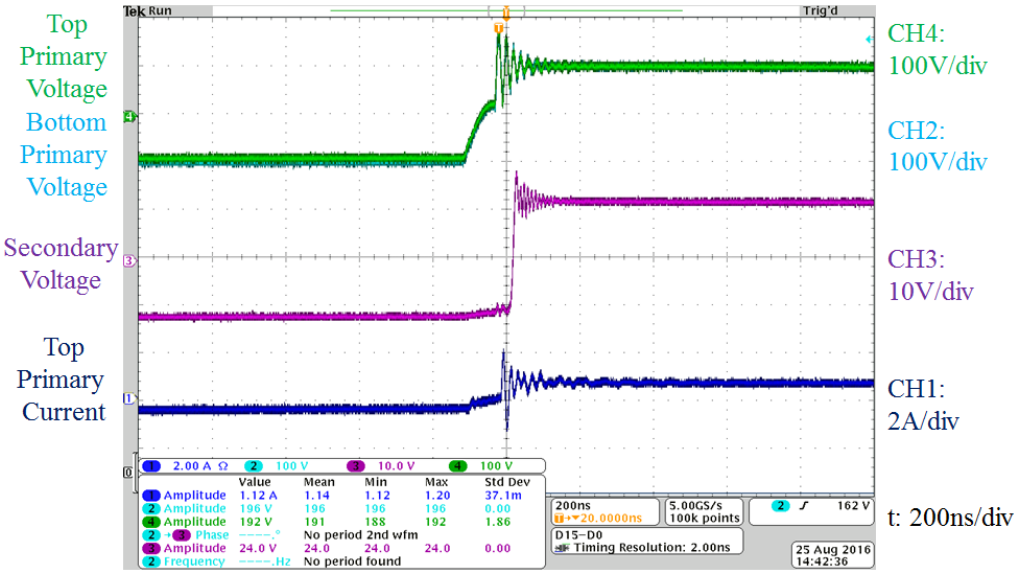


(b)

Figure 5-26: Operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, P_{out} = 300 W, and ϕ = 0.3007 radians. (a) Shows four periods and (b) zooms in on the switch transitions. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

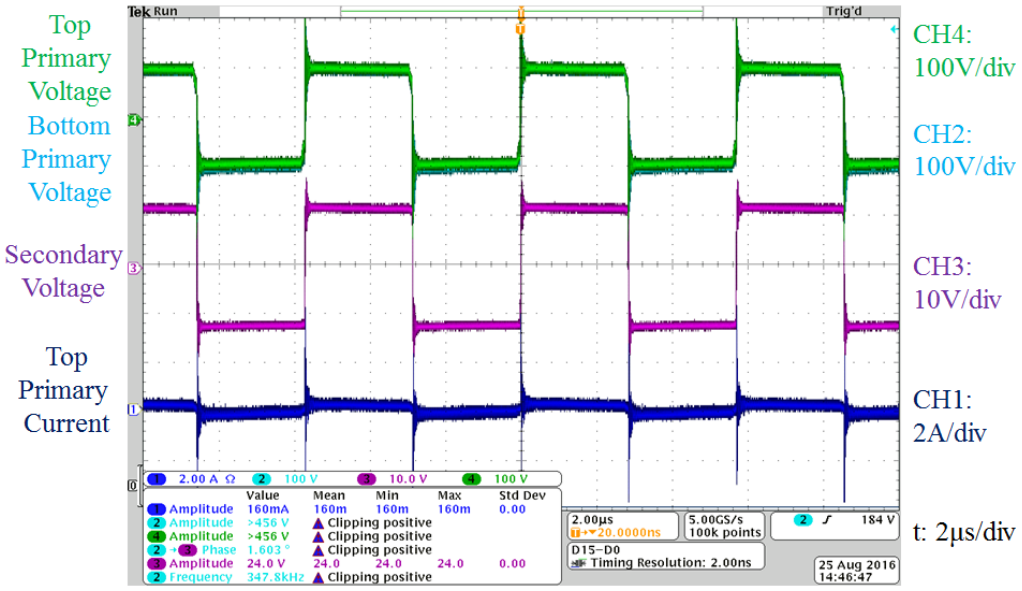


(a)

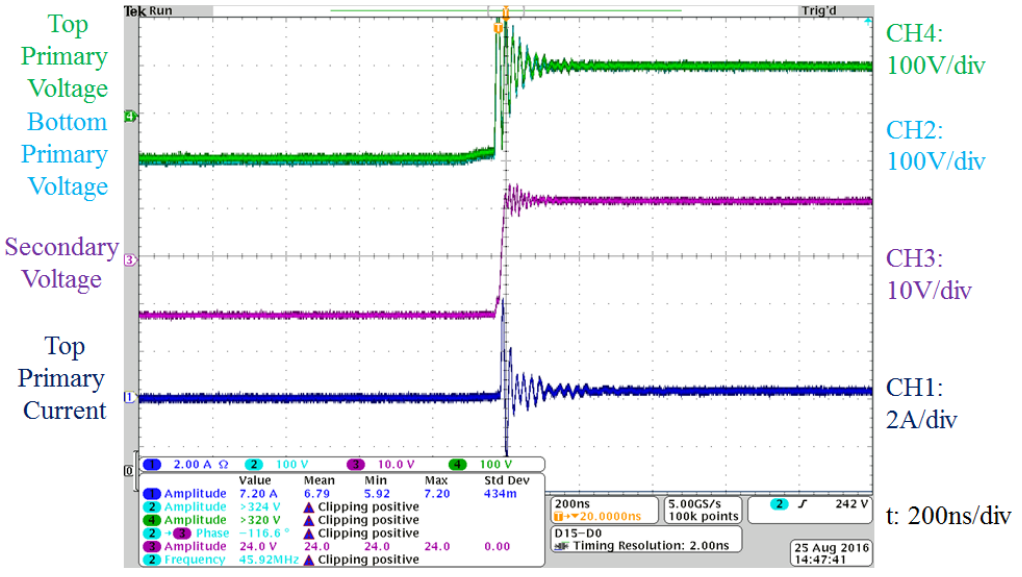


(b)

Figure 5-27: Operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, P_{out} = 104 W, and ϕ = 0.1544 radians. (a) Shows four periods and (b) zooms in on the switch transitions. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.



(a)



(b)

Figure 5-28: Operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, P_{out} = 30 W, and ϕ = 0.1178 radians. (a) Shows four periods and (b) zooms in on the switch transitions. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

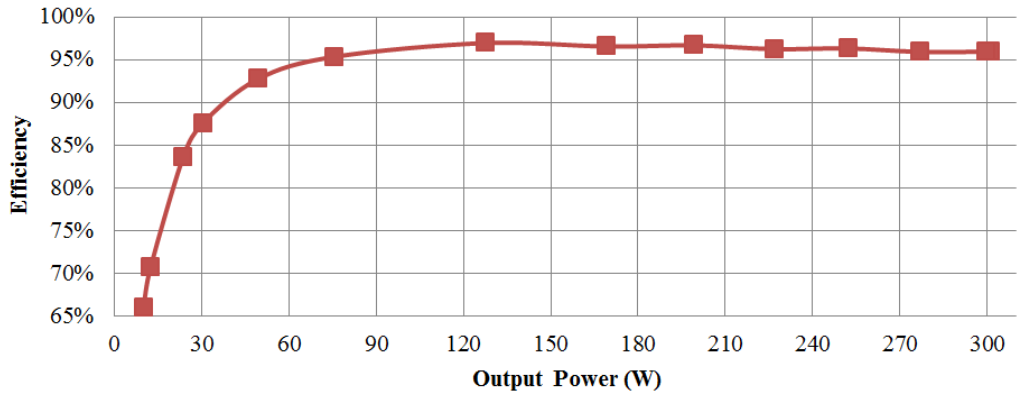


Figure 5-29: Efficiency curves for the GaN-based reconfigurable double stacked active bridge converter when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, and power from full load to 3.3% load.

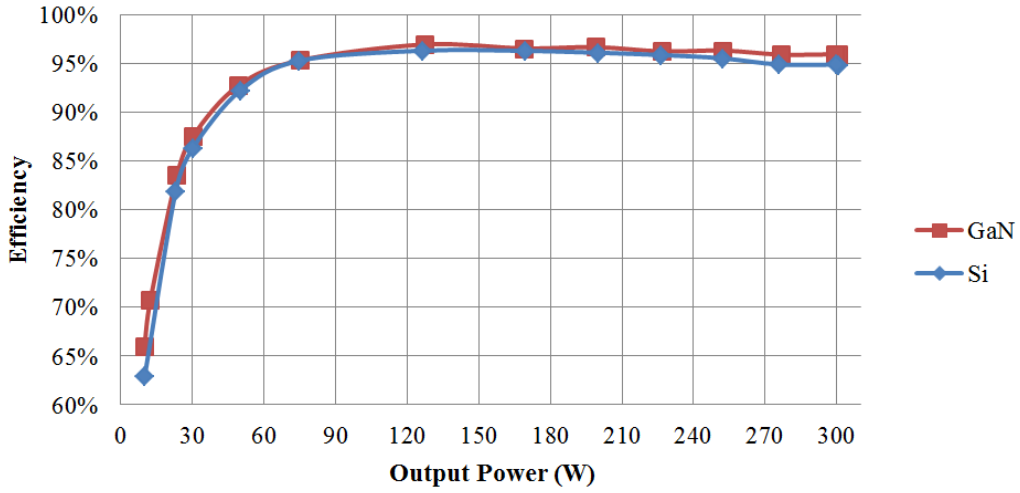


Figure 5-30: Efficiency curves comparing the GaN-based reconfigurable double stacked active bridge converter with the Si-based prototype when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, and power from full load to 3.3% load.

To highlight the advantages gained by using GaN power devices, now let us consider the performance of the Si-based reconfigurable double stacked active bridge converter of Figure 5-14. As seen in Figure 5-30, the two efficiencies have very similar trends where the efficiency starts to degrade below 120 W; this similarity is due to the devices having similar output capacitance. For the same voltage rating, the Si devices have a higher on-resistance than the GaN devices which results in the lower efficiency at high output powers where conduction loss is a dominant loss mechanism. The Si-based converter achieves a full load efficiency of 94.9%, a peak efficiency of 96.3%, an efficiency of 86.3% at 10% load, and an efficiency of 62.9% at 3.3% load. It is important to realize that the 1% reduction in efficiency at full load using Si devices represents approximately 25% higher loss than with the GaN devices at the same operating point – a significant difference for a high-efficiency converter.

To see the advantages gained by using a double stacked-bridge inverter instead of a single stacked-bridge inverter, let us consider the performance of the Si-based single stacked active bridge converter of Figure 5-15. The efficiency of this prototype along with the previous two efficiency curves is plotted in Figure 5-31. The performance is very similar at full power, where the single stack design actually has a higher efficiency than the Si-based double stacked design. However, below 200 W, the efficiency starts to degrade dramatically to values well below those of the double stacked designs. This decrease in performance was predicted in the simulations of Section 4.3 (see Figure 4-20, which shows curves that are qualitatively similar). Therefore, we have reason to believe that a full bridge DAB converter would have even worse performance than the single stacked inverter converter. The Si-based single stacked converter achieves a full load efficiency of 95.2%, a peak efficiency of 95.4%, an efficiency of 69.5% at 10% load, and efficiency of 41.4% at 3.3% load. The efficiencies for all three prototypes at various power levels are summarized in Table 5-6.

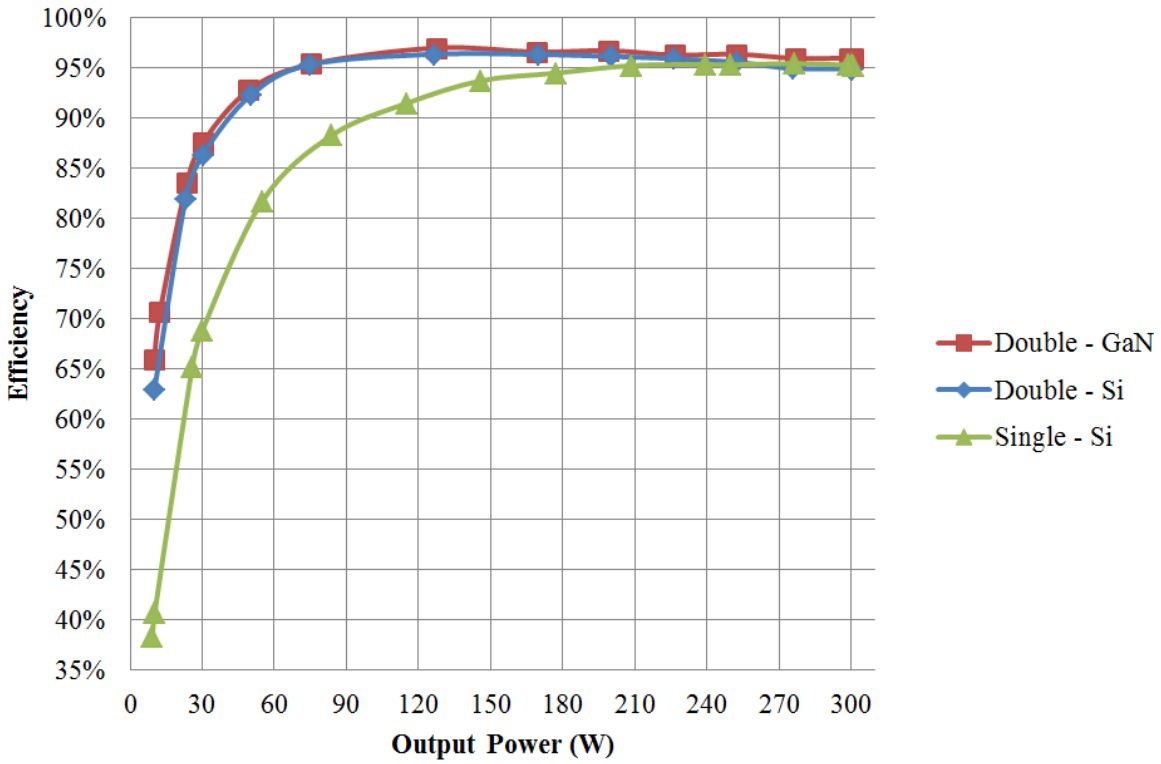


Figure 5-31: Efficiency curves comparing the GaN-based and Si-based reconfigurable double stacked active bridge converters with the Si-based single stacked active bridge converter when operated in normal mode with V_{in} = 380 V, V_{out} = 12 V, and power from full load to 3.3% load.

Table 5-6: Efficiencies for the three prototype converters when operated in normal mode

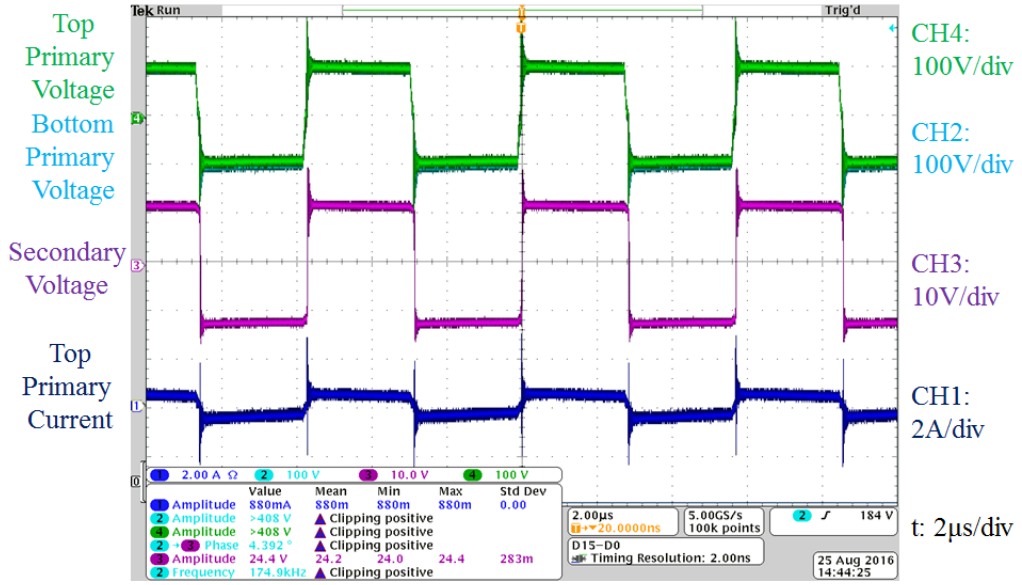
Prototype	3.3% Load	10% Load	100% Load
GaN-based Double Stacked Active Bridge	66.0%	87.6%	95.9%
Si-based Double Stacked Active Bridge	62.9%	86.3%	94.9%
Si-based Single Stacked Active Bridge	41.4%	69.5%	95.2%

5.2.3 Converter Performance Across Output Power in Low-Power Mode

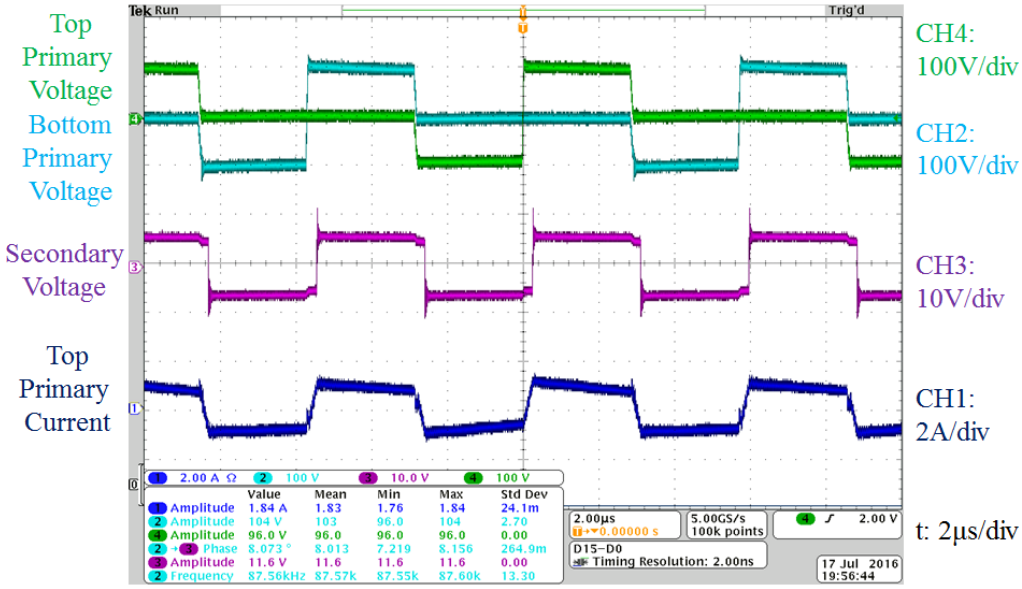
The efficiency can be improved by using a double stacked-bridge inverter, but that is not the extent of the potential for this reconfigurable double stacked active bridge converter. As seen in the previous subsection, there is a power level below which ZVS is lost and the efficiency begins to fall. It is at these lower power levels that we utilize a reconfiguration of the converter as described in Section 4.2. This reconfiguration will increase current available for ZVS. The operating waveforms for the GaN-based converter operating under normal and low-power mode to deliver 70 W are shown in Figure 5-32. It can be seen that the transformer primary waveforms are identical in normal mode but in low-power mode, one of the primary voltages is zero during a given switching cycle of the secondary. The effective frequency of the primary voltage is also halved (from 175 kHz to 87.5 kHz). It can also be seen that the secondary voltage is halved.

The primary current is much larger in the low-power mode for delivery of the same power in full power mode. Some variations in the slope are seen between cycles due to the addition of the magnetizing current in every other cycle. The current in the low-power mode does not exhibit the same high frequency oscillations seen in the current of the normal mode. By zooming into the switch transitions, it can be seen in Figure 5-33 that for the same power level, the converter is hard-switching in normal operation, but it can maintain soft-switching in low-power mode as seen in Figure 5-34. Even below 10% load (or 30 W) the inverters are not completely hard-switched like they were in Figure 5-28. Figure 5-35 shows the switch transitions for the low-power mode when delivering 27 W to the output. Because the inverter switches half as often when operated in low-power mode, any hard-switching loss will be reduced even further so efficiency does not degrade as much.

While conduction loss will increase in low-power mode as compared to normal mode due to the higher currents, the fact that soft-switching is maintained helps keep the efficiency high. Additionally, the core loss and any switching loss in the inverter are reduced by a factor of two. This leads to the efficiency curve shown in Figure 5-36. At power levels of 75 W (or ¼ power) and lower, the low-power mode results in a higher efficiency than the normal mode. When operated under low-power mode, the



(a)



(b)

Figure 5-32: Operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated with V_{in} = 380 V, V_{out} = 12 V in (a) normal mode, P_{out} = 76 W, and ϕ = 0.1407 radians and (b) low-power mode, P_{out} = 75 W, and ϕ = 0. 3145 radians. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

GaN-based double stacked-bridge converter achieves an efficiency of 93.2% at 10% load and an efficiency of 79.8% at 3.3% load. The Si-based double stacked converter can also achieve high efficiencies under low-power operation – an efficiency of 92.3% at 10% load and 77.6% at 3.3% load. Full operating parameters and details can be found in Appendix F. The single stacked converter is not capable of operating in this low-power mode. The efficiencies between normal and low-power modes are summarized in Table 5-7.

5.3 Summary of the Reconfigurable Double Stacked Active Bridge Converter

It has been shown that the GaN-based reconfigurable double stacked active bridge converter can achieve extremely high efficiencies across a wide range out output power levels. The high performance can be attributed to several factors in the topology and the component selection.

First, when compared to the single stacked-bridge inverter, the double stacked-bridge inverter can reduce loss by about 50% at power levels below 25% load as shown in Figure 5-37(a). This can be attributed to the improved performance of the inverter devices. The lower voltage rated devices offer improvements in on-state resistance and off-state capacitance.

Second, when compared to Si devices, GaN devices at the same voltage rating can reduce loss by about 20% at power levels close to full power as shown in Figure 5-37 (b). For the particular set of devices chosen, this is due to the lower on-state resistance for a similar off-state capacitance.

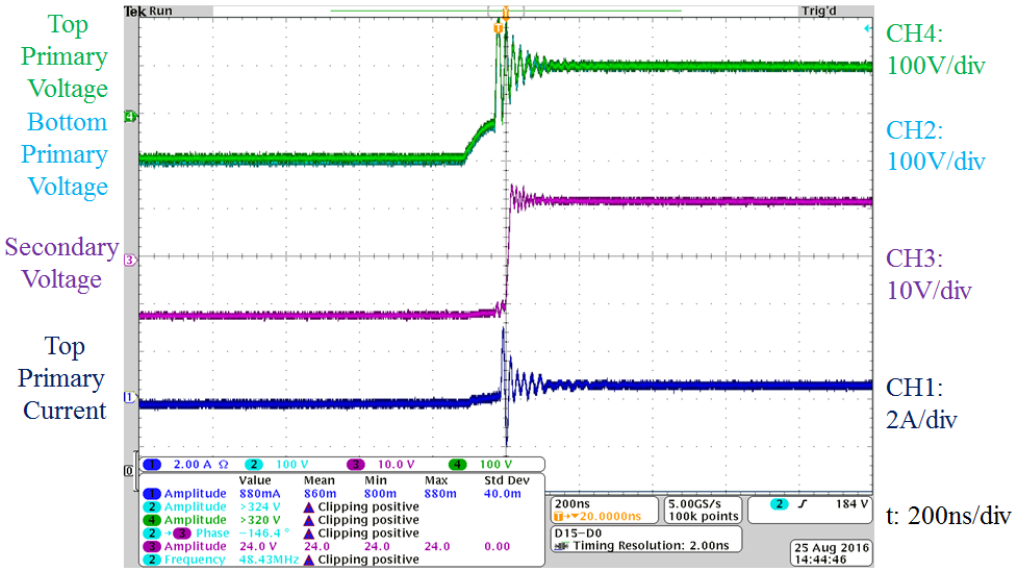
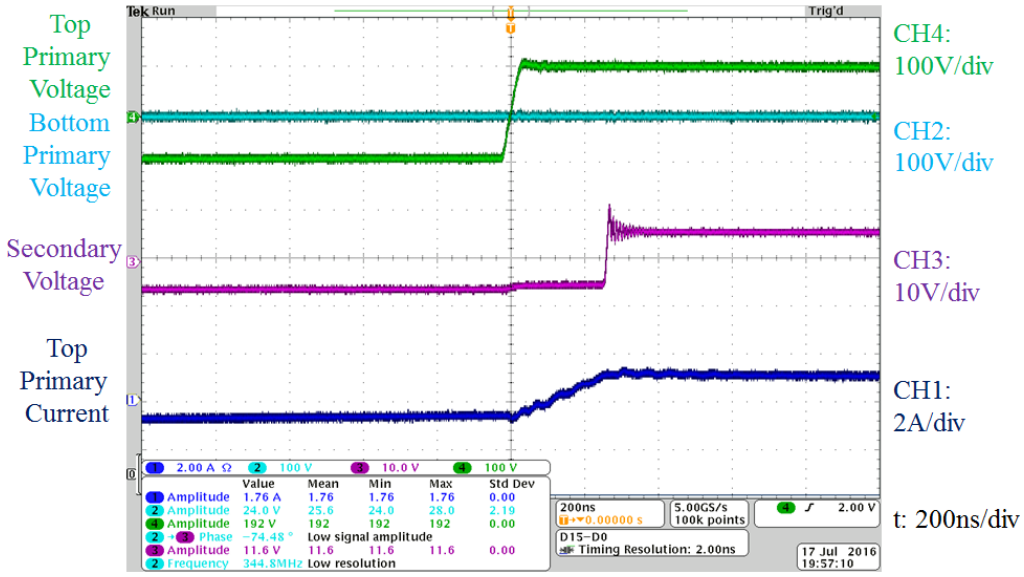
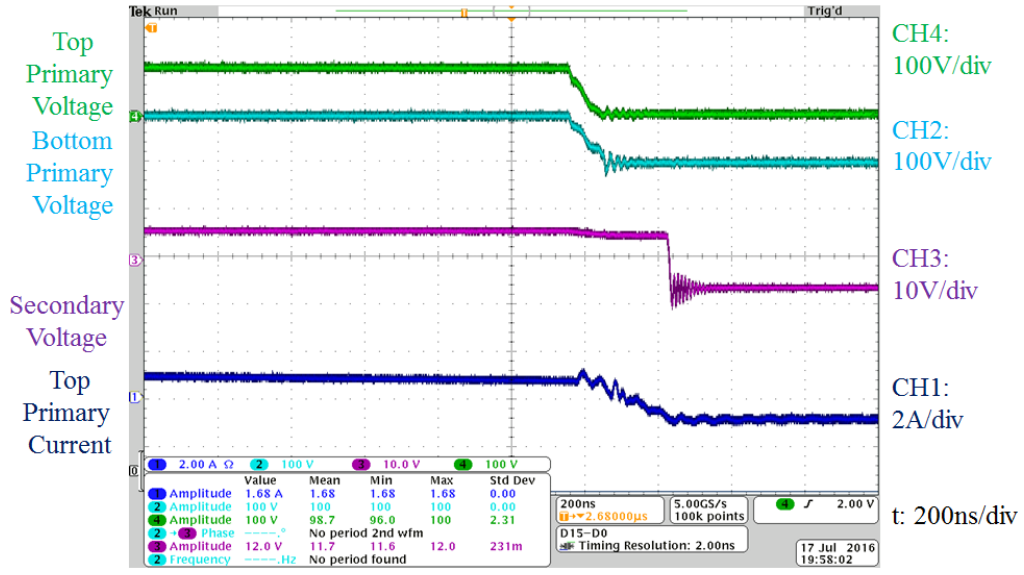


Figure 5-33: Zoomed in operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated with V_{in} = 380 V, V_{out} = 12 V in normal mode, P_{out} = 76 W, and ϕ = 0.1407 radians. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

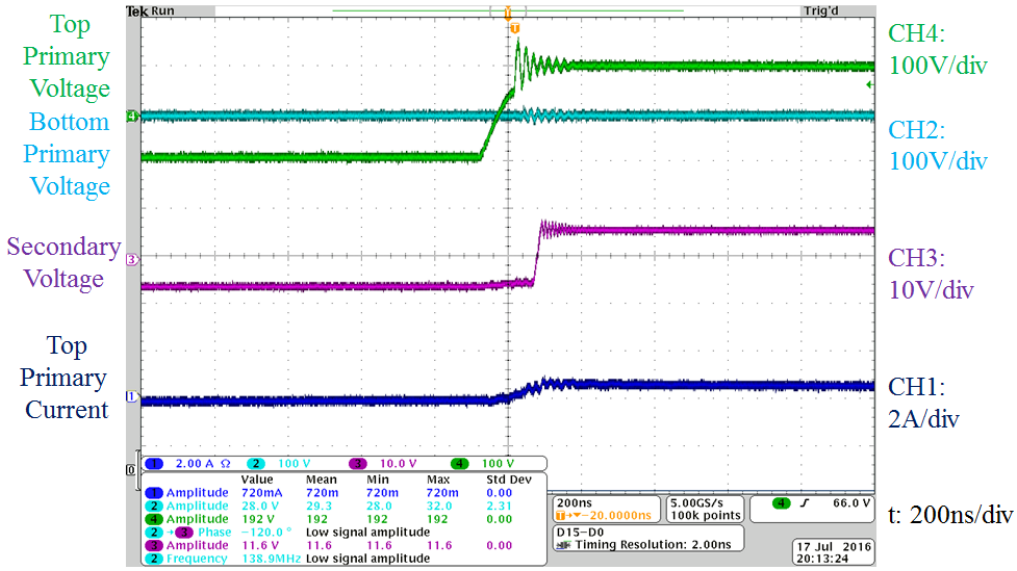


(a)

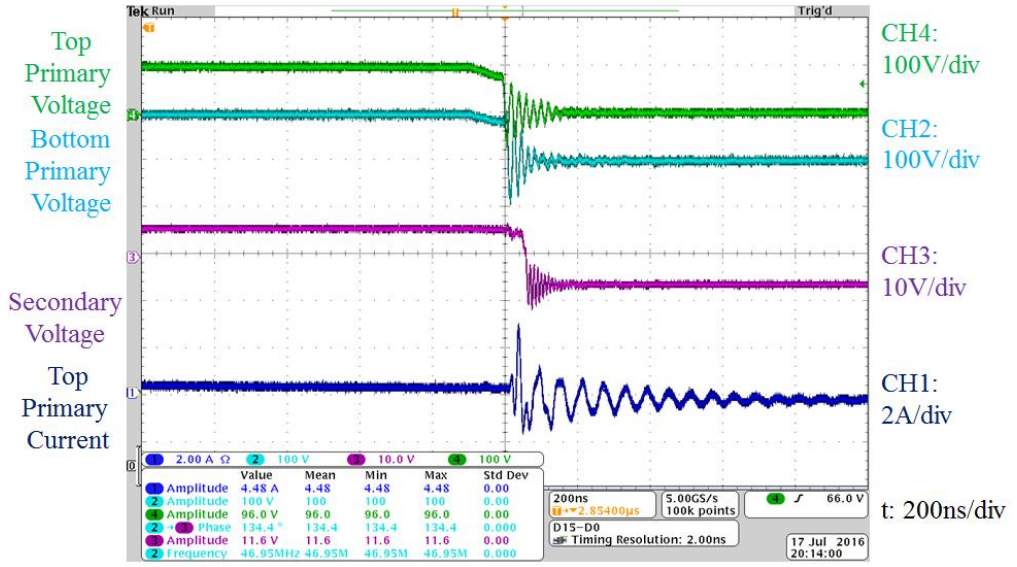


(b)

Figure 5-34: Zoomed in operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated with V_{in} = 380 V, V_{out} = 12 V in low-power mode, P_{out} = 75 W, and ϕ = 0. 3145 radians. There are two types of switch transitions: (a) when one transformer's primary voltage is kept at zero and the other transformer's primary voltage goes from $-V_{in}/4$ to $V_{in}/4$, and (b) when both transformer primary voltages fall by $V_{in}/4$. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.



(a)



(b)

Figure 5-35: Zoomed in operating waveforms for the GaN-based reconfigurable double stacked active bridge converter when operated with V_{in} = 380 V, V_{out} = 12 V in low-power mode, P_{out} = 27 W, and ϕ = 0. 1715 radians. There are two types of switch transitions: (a) when one transformer's primary voltage is kept at zero and the other transformer's primary voltage goes from $-V_{in}/4$ to $V_{in}/4$, and (b) when both transformer primary voltages fall by $V_{in}/4$. For each screenshot, the top two green and cyan waveforms are the two primary voltages, the middle magenta waveform is the secondary voltage, and the bottom blue waveform is the current into the top transformer primary.

Finally, the unique single core magnetic component and the reconfigurable rectifier working together with the double-stacked inverter in low-power mode can provide another 40% - 50% reduction in loss at ultra-low power levels as shown in Figure 5-37(c). This is because a higher amount of current is available to maintain ZVS transitions at the lower power levels. When ZVS is not achieved, the reduction in switching frequency and core loss also provide efficiency benefits.

Overall, the proposed converter can operate with the efficiency curve of Figure 5-38, which if evaluated using the 80 Plus specification [14] would earn the highest rating of 80 Plus Titanium.

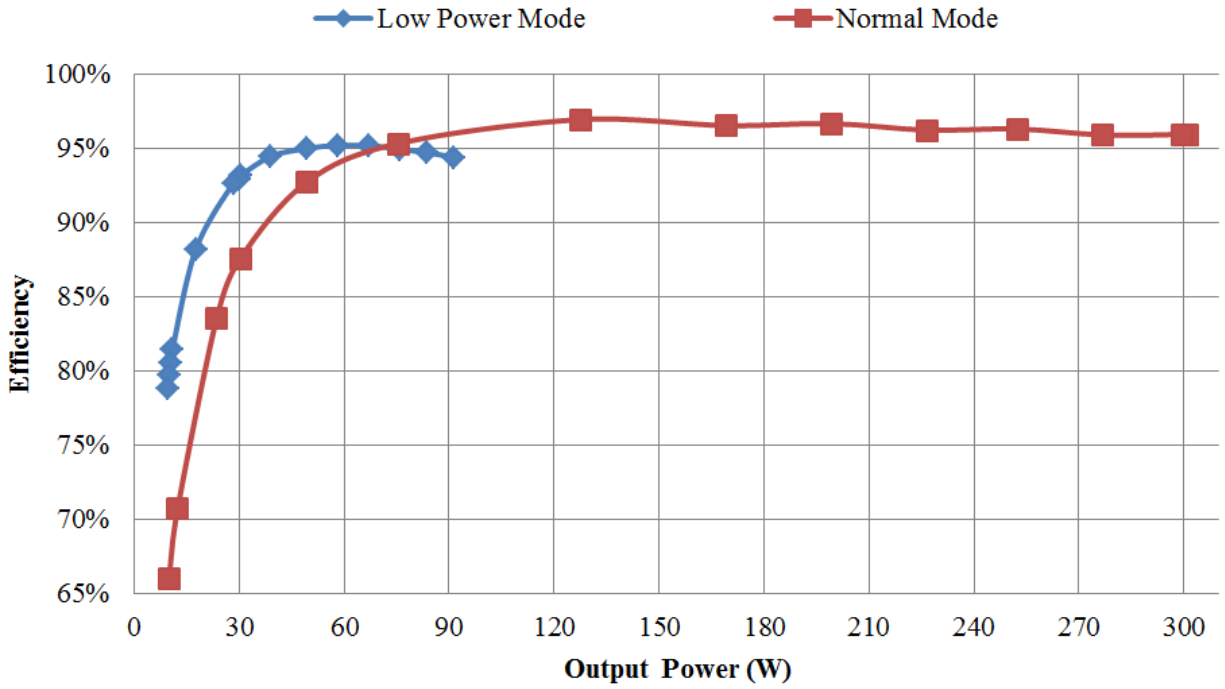
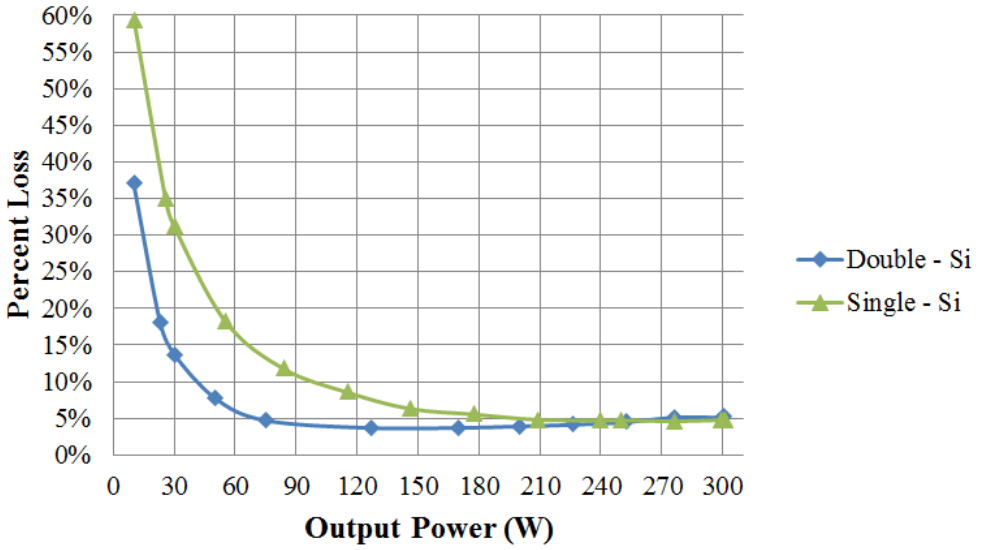


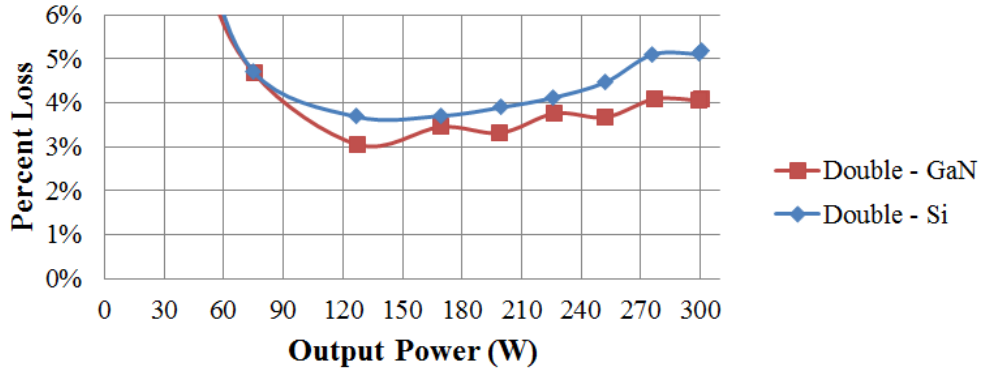
Figure 5-36: Efficiency curves for the GaN-based reconfigurable double stacked active bridge converter when operated with V_{in} = 380 V, V_{out} = 12 V in normal mode from full load to 3.3% load and low-power mode from 30% load to 3.3% load

Table 5-7: Efficiencies for the two reconfigurable double stacked active bridge converters when operated in normal mode and low-power mode at various power levels

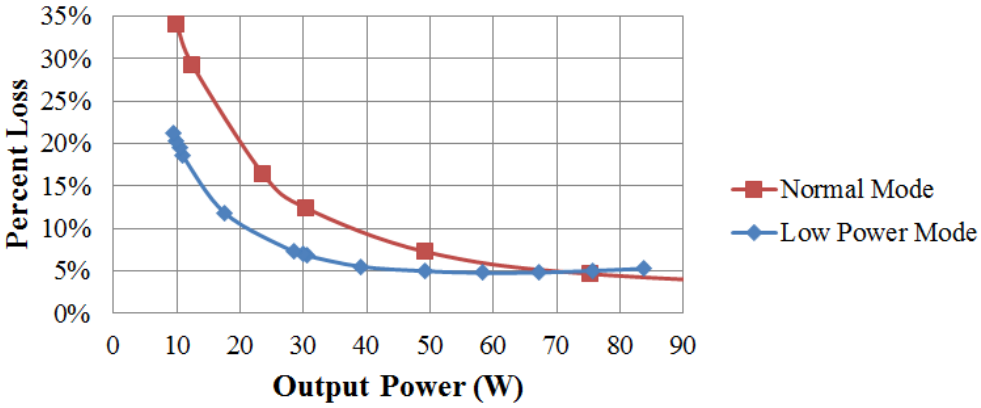
Prototype	3.3% Load	10% Load	25% Load
GaN-based Converter under Normal Mode	66.0%	87.6%	95.3%
GaN-based Converter under Low-Power Mode	79.8%	93.2%	95.0%
Si-based Converter under Normal Mode	62.9%	86.3%	95.3%
Si-based Converter under Low-Power Mode	77.6%	92.3%	93.9%



(a)



(b)



(c)

Figure 5-37: Percent loss curves comparing the improvement of performance from going from (a) a single stacked-bridge inverter design to a double stacked-bridge inverter design, (b) a Si-based double stacked-bridge inverter design to a GaN-based double stacked-bridge inverter design, and (c) normal mode to low-power mode.

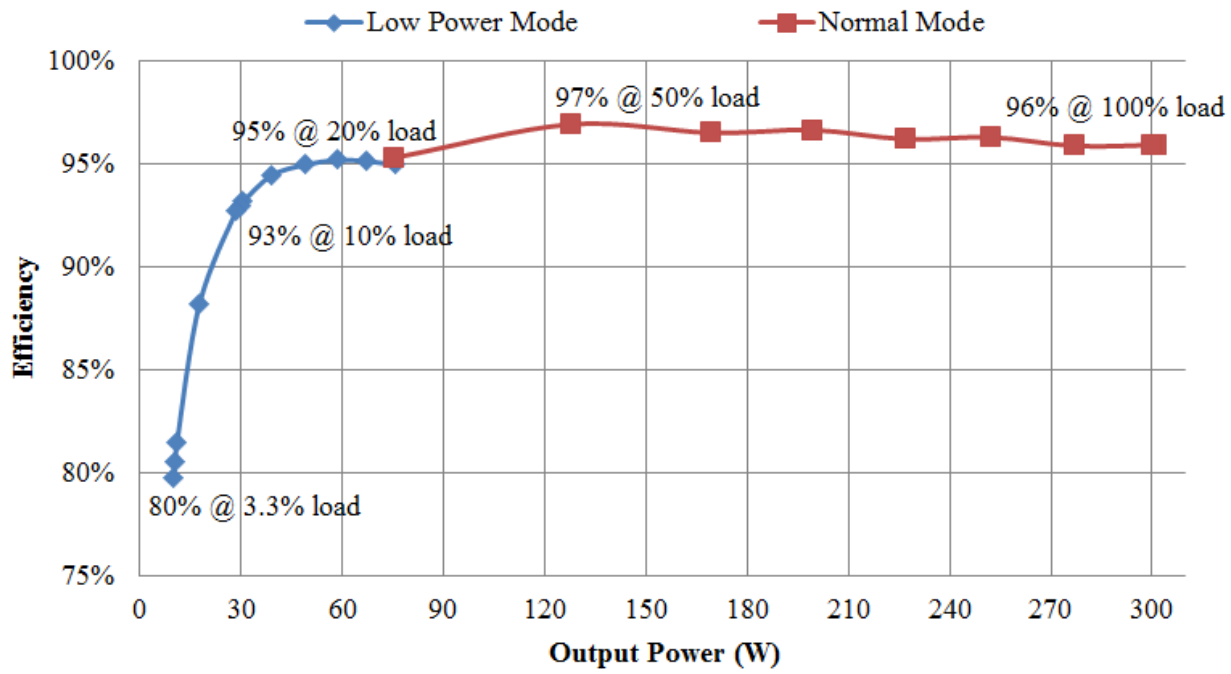


Figure 5-38: Efficiency curves for the GaN-based reconfigurable double stacked active bridge converter when operated with V_{in} = 380 V, V_{out} = 12 V in normal mode from full load to 25% load and low-power mode from 25% load to 3.3% load

Chapter 6

Summary and Future Work

With the emergence of many direct current (dc) sources and loads, there is an increased need for power electronic devices that can efficiently and effectively convert from one voltage domain to another. Of particular interest are converters that can take in hundreds of volts (dc) and transfer power to tens of volts (dc). This particular work focused on converters that can operate efficiently given a range of input voltages and output powers. To reduce size, high frequency converters are desirable but key to their efficient operation is soft-switching capability, in which switching devices are able to turn on or turn off with a low voltage across them or low current through them. If soft-switching is obtained, then high switching frequencies can be used, which can reduce the size of many components and improve power density.

This particular work expands upon two families of soft-switching converters – resonant converters and dual active bridge (DAB) converters. There are abundant applications for these converters, but this work focuses on converters one might find in a data center, where power is transmitted through the building at 380 V (dc) and must be converted down to 12 V (dc) for the server. The converters are expected to operate well across a wide input voltage range of 260 V to 410 V and output power range from full (100%) load down to very light loads (e.g., below 10% load).

6.1 Summary

This thesis presents the development, design, construction and application of two converter topologies. The first is a resonant converter and the second is an active bridge converter. Both are optimized to work efficiently at a nominal operating input voltage of 380 V and efficiently deliver between 300 W and 350 W to a 12 V depending on the converter topology. The topologies and design choices ensure that high efficiency operation can be maintained down to 10% load or below.

A new resonant converter is presented in Chapter 2. In traditional resonant converters, as the input voltage varies, the inverter current begins to look more reactive which can lead to increase conduction and potentially switching loss. The proposed converter uses a combination of phase-shift control as well as a specifically designed impedance network (termed an “Impedance Control Network”) to provide resistive loading of the inverters even as the input voltage varies. This allows for minimum conduction loss and the ability to maintain soft-switching for increased efficiency - between 89% and 92% at 365 W for a working prototype across the full input voltage range of 260 V to 410 V. The proposed design techniques provide minimal output power variation across the wide input voltage range –

between 365 W and 411 W. To lower the output power, burst mode (or on/off) control is used. This method allows the converter to maintain efficiency – falling by only 4.5% as power is reduced from 350 W to 35 W when the input voltage is 380 V.

Chapter 3 develops an additional control method that can be used to help vary the output power. The method shows the effect of applying Variable Frequency Multiplier (VFX) techniques to the inverter stage and/or rectifier stage. By varying the duty ratio and switching frequency of the inverter and/or rectifier half-bridges, the fundamental component of the voltage can be cancelled and the second harmonic component can be reinforced. When applied to the inverter, this has the effect of lowering the voltage as seen at the input to the transformers which reduces core loss without affecting the frequency through the remainder of the converter network so that components can be optimized to work well at a single frequency. Through this method, the converter would operate at a different portion of the power curve and naturally deliver a lower power. This technique can be combined with the burst mode to achieve high efficiencies at ultra-low power levels.

A second converter was developed in Chapter 4. This development takes in the strengths of the traditional full bridge inverter DAB converter – low component count and straightforward control mechanisms – and improves upon its weaknesses – poor performance outside of a fixed input voltage and output power. The proposed converter makes use of a GaN-based double stacked-bridge inverter stage, a single three-winding magnetic component which incorporates the necessary energy transfer inductance into one core, and a reconfigurable rectifier which can provide multiple operating modes for very high efficiency across a very wide output power range.

In Chapter 5, the proposed active bridge design techniques were experimentally compared with two benchmark prototypes – one that used Si devices on a double stacked inverter and one that used Si devices on a single stacked inverter. The GaN-based double stacked inverter prototype achieved the highest efficiencies of all three prototypes – an efficiency of 96% at 300 W, a peak efficiency of 97% at 150 W, an efficiency or 93% at 30 W, and an efficiency of 80% at 10 W.

6.2 Conclusions

A number of conclusions have been drawn from this thesis. These include:

1) The Impedance Control Network technique is an effective means to provide soft-switching of all devices in a resonant converter across wide input voltage variation.
2) Burst mode (on/off) control can provide a very efficient means of reducing the output power because soft-switching is preserved and core losses can be reduced.

3) Variable Frequency Multiplier techniques can be applied to provide multiple modes of operation by reducing the voltage as seen at the output of the inverter or the input to the rectifier.
4) Stacking of devices across a high voltage can greatly improve both individual device performance as well as overall converter performance. The proposed "double stacked-bridge" technique is a highly effective conversion strategy, including in the proposed double stacked active bridge converter.
5) A well-designed three-winding magnetic component can combine the features of two transformers and two energy leakage inductances into a single core. This structure is valuable for achieving high performance in the proposed double stacked active bridge converter.
6) The use of emerging GaN-based switch technology can provide increased performance when compared to traditional Si-based devices.

6.3 Directions for Future Work

The techniques used in this thesis have shown much promise and efforts have already been made to apply them to other converter topologies. The Impedance Control Network technique has already been applied to step-up converter topologies with very wide input and output voltages. The technique is most attractive when the input voltage is frequently changing. One interesting application of the technique would be in a power factor correction design where the 50/60 Hz line voltage sweeps from zero to some peak operating voltage.

The VFX technique was used as an operating mode when the output power needed to be reduced, but it would be very useful in applications where the input voltage increases by a factor of two, like a universal input power supply which must be able to operate when the ac input voltage is either 120 V_{RMS} or 240 V_{RMS}.

The reconfigurable double stacked active bridge design performed very well and its techniques could be applied to many other application spaces. Despite its high performance, there is always room for improvement. As was seen in the design of the ICN converter, the design of the magnetic component has a significant impact on the overall performance. More efforts can be made to model the special three-winding magnetic component to better understand how the windings outside the core affect the leakage. Future designs could potentially operate at a much higher frequency if the leakage can be well defined and controlled in the design stage.

The work performed for this thesis could very well provide the launch pad for many future endeavors.

Appendix A MATLAB Code

This Appendix contains the MATLAB code that was used to generate multiple plots and the code that was used to aide in designing the magnetic components presented in this thesis. There are a total of seven files. The first file is used to plot many of the theoretical and experimental plots of Chapter 2. The second file plots the transformer waveforms generated in simulation and from experiments (for length considerations the .txt input files are not included in the Appendix). The third and fourth file contain core geometry data for use in the fifth, sixth, and seventh files which sweep across frequency and core shapes to calculate the losses in the transformer and inductor designs. The fifth file is used for the transformer for the ICN converter and the sixth file is used for the coupled inductor and resonant inductor of the ICN. The seventh file is used for the transformer for the active bridge converter.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB Script used to generate many of the plots used in Chapter 2
% Plots that are generated include:
% Conductance and Susceptance vs. Phase Shift
% Output Power vs. a very wide Input Voltage
% Normalized Output Power vs. Normalized Operating Input Voltage
% Experimental Power and Efficiency vs. Input Voltage
% Experimental Power and Efficiency with 50% Burst Mode vs. Input Voltage
% Experimental Efficiency vs. Output Power for 380Vin, 12Vout
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all
clc
close all

% plot conductance and susceptance for key input voltages of interest

D = linspace(0,90);      % Phase Shift (degrees)
Vinmin = 260;            % Minimum input voltage
Vinmax = 410;            % Maximum input voltage
Vout = 12;               % Output voltage
Poutrated = 400;    % Rated output power divided by approx. efficiency
N = 4*Vout/sqrt(Vinmin^2+Vinmax^2);          % turns ratio 1:N
X = N*Vinmin*sqrt(16*Vout^2-N^2*Vinmin^2)/(pi^2*Poutrated);  % impedance

G260 = 4*Vout.*sin(D*pi/180)/(N*X*260);      % Conductance at 260Vin (min)
B260 = 4*Vout.*cos(D*pi/180)/(X*260*N)-1/X; % Susceptance at 260Vin (min)

G380 = 4*Vout.*sin(D*pi/180)/(N*X*380);      % Conductance at 380Vin (nom)
B380 = 4*Vout.*cos(D*pi/180)/(X*380*N)-1/X; % Susceptance at 380Vin (nom)

G410 = 4*Vout.*sin(D*pi/180)/(N*X*410);      % Conductance at 410Vin (max)
B410 = 4*Vout.*cos(D*pi/180)/(X*410*N)-1/X; % Susceptance at 410Vin (max)
```

```
FigHandle = figure('Position', [0, 550, 700, 400]);
plot(D,G260,'b-.')
hold on
plot(D,G380,'b-')
plot(D,G410,'b--')

plot(D,B260,'r-.')
plot(D,B380,'r-')
plot(D,B410,'r--')

plot(D,zeros(100),'k')

legend('Conductance(260V)','Conductance(380V)','Conductance(410V)',...
    'Susceptance (260V)','Susceptance (380V)','Susceptance (410V)',...
    'location','NorthWest')

xlabel('Phase Shift (degrees)')
ylabel('Conductance and Susceptance (S)')

% Another admittance plot for evenly spaces input voltages

G335 = 4*Vout.*sin(D*pi/180)/(N*X*335);     % Conductance at 335Vin (mid)
B335 = 4*Vout.*cos(D*pi/180)/(X*335*N)-1/X; % Susceptance at 335Vin (mid)

FigHandle = figure('Position', [0, 50, 700, 400]);
plot(D,G260,'b-.')
hold on
plot(D,G335,'b-')
plot(D,G410,'b--')

plot(D,B260,'r-.')
plot(D,B335,'r-')
plot(D,B410,'r--')

plot(D,zeros(100),'k')

legend('Conductance(low Vin)','Conductance(mid Vin)',...
    'Conductance(high Vin)','Susceptance (low Vin)',...
    'Susceptance (mid Vin)','Susceptance (high Vin)',...
    'location','NorthWest')

xlabel('Phase Shift (degrees)')
ylabel('Conductance and Susceptance (S)')

% Plot theoretical power curve across wide range of input voltages

Vin = linspace(00,500,151);     % Range of input voltage

P = N.*Vin.*sqrt(16*Vout^2-N^2.*Vin.*Vin)/(pi^2*X);     % Power

FigHandle = figure('Position', [650, 800, 700, 200]);

plot(Vin, P)
hold on
```

```
plot(Vin,Poutrated*ones(151),'--r')
plot([Vinmin Vinmin], [0 Poutrated], '--k')
plot([Vinmax Vinmax], [0 Poutrated], '--k')

xlabel('Input Voltage (V)')
ylabel('Output Power (W)')
set(gca, 'YTick', [], 'Xtick',[])
txt1 = '\color{red} P_{\itout,\rmrated}';
text(0,Poutrated*1.1,txt1)
txt2 = '\color{black} V_{in,min}\rightarrow ';
text(Vinmin,50,txt2,'HorizontalAlignment','right')
txt3 = '\color{black} \leftarrow V_{in,max}';
text(Vinmax,50,txt3)

% Plot theoretical power curve across operating range of input voltages,
% normalized

Vinop = linspace(260,410,151);  % Range of operating input voltage

Pop = N.*Vinop.*sqrt(16*Vout^2-N^2.*Vinop.*Vinop)/(pi^2*X); % Power

FigHandle = figure('Position', [650, 550, 700, 200]);

plot(Vinop/260, Pop/Poutrated)
xlabel('Input Voltage/V_{in,min}')
ylabel('Output Power/P{\itout,\rmrated}')
set(gca, 'YLim', [1 1.15], 'XLim',[1 1.6])

% Plot experimental power and efficiency

VinE = [260, 290, 320, 350, 380, 410];      % Experimental Input Voltage

% Data for ECCE Paper, gathered in 2015
% PinE = [389.62,  412.03, 426.29, 424.06, 407.89, 367.10];
% PoutE = [331.86, 354.34, 369.55, 371.10, 360.88, 329.20];
% nE = 100*[0.85175, 0.85999, 0.86689, 0.87512, 0.88473, 0.89676];

% Data for thesis, gathered July 2016
PinE = [412.03,  438.02, 453.82, 455.39, 439.44, 399.51];   % Input Power
PoutE = [364.89, 390.73, 407.36, 411.37, 400.25, 367.99];   % Output Power
nE = 100*[0.885605, 0.892017, 0.897612, 0.903337 0.91081, 0.921099];
    % Efficiency


FigHandle = figure('Position', [650, 300, 700, 200]);
[a,h1,h2] = plotyy(VinE,PoutE,VinE,nE);

set(h1,'color','green','LineWidth',3,'marker','d')
set(h2,'color','blue','LineWidth',3,'marker','o')

set(a,{'ycolor'},{'k';'k'})

ylabel(a(1),'Power (W)','FontSize',14,'Fontname','Times New Roman')
ylabel(a(2),'Efficiency (%)','FontSize',14,'Fontname','Times New Roman')
```

```
xlabel(a(1),'Input Voltage (V)','FontSize',14,'Fontname','Times New Roman')
% title(['\fontsize{20} \fontname{Times New Roman} Experimental Results'])

set(a(1),'YLim',[000,450],'ytick', linspace(000,420,8),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[88, 100],'ytick', linspace(88,100,4),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(1),'XLim',[260,410],'xtick', linspace(260,410,6),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'XLim',[260,410],'xtick', linspace(260,410,6),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'FontSize', 12, 'Fontname','Times New Roman');

axes(a(1))
hold on
h3 = plot(VinE,PoutE,'s-g','LineWidth',3);

axes(a(2))
grid on
l=legend([h3(1) h2(1)],'Output Power', 'Efficiency', ...
    'location','west');
set(l,'color','w')
v = get(gca,'Position');
set(gca,'Position',[v(1) v(2)*2 v(3) v(4)*0.9])

% Plot experimental power and efficiency for 50% burst mode
VinE = [260, 290, 320, 350, 380, 410];      % Experimental Input Voltage

% July 2016 set
PinE50 = [245.51,  262.79, 272.86, 274.37, 265.24, 241.66]; % Input Power
PoutE50 = [181.66, 196.42, 205.61, 208.28, 202.64, 185.81]; % Output Power
nE50 = 100*[0.882662, 0.888061, 0.893476, 0.897785, 0.903741, 0.910605];
    % Efficiency

FigHandle = figure('Position', [1300, 500, 800, 300]);
[a,h1,h2] = plotyy(VinE, PoutE,VinE,nE);

set(h1,'color','green','LineWidth',3,'marker','d')
set(h2,'color','blue','LineWidth',3,'marker','o')

set(a,{'ycolor'},{'k';'k'})

ylabel(a(1),'Power (W)','FontSize', 14, 'Fontname','Times New Roman')
ylabel(a(2),'Efficiency (%)','FontSize', 14, 'Fontname','Times New Roman')
xlabel(a(1),'Input Voltage (V)','FontSize', 14, 'Fontname','Times New Roman')

set(a(1),'YLim',[000,450],'ytick', linspace(000,420,8),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[88, 100],'ytick', linspace(88,100,4),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(1),'XLim',[260,410],'xtick', linspace(260,410,6),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'XLim',[260,410],'xtick', linspace(260,410,6),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'FontSize', 12, 'Fontname','Times New Roman');
```

```
axes(a(1))
hold on
h3 = plot(VinE,PoutE50,'d--g','LineWidth',3);

axes(a(2))
grid on
hold on
h4 = plot(VinE,nE50,'o--b','LineWidth',3);
l=legend([h1(1) h2(1) h3(1) h4(1)],'Output Power - 100%',...
    'Efficiency - 100%','Output Power - 50%', 'Efficiency - 50%', ...
    'location','NorthOutside','Orientation','horizontal');
set(l,'color','w')
v = get(gca,'Position');
set(gca,'Position',[v(1) v(2)*2 v(3) v(4)*0.9])

%Plot experimental power and efficiency for 380 Vin

%July 2016 set
Pin380 = [40.293891, 45.2795, 88.613792, 132.0646, 175.2445, 219.3732, ...
          263.1192, 306.9390, 350.7657, 382.4843];  % Input Power
Pout380 = [34.87294, 39.39173, 78.84997, 118.5155, 157.8898, 198.2565, ...
          238.3519, 278.4224, 318.5571, 347.4282];  % Output Power
n380 = 100*[0.865465, 0.869968, 0.889816, 0.897405, 0.900969, 0.903741, ...
            0.90587, 0.907094, 0.908176, 0.908346]; % Efficiency

FigHandle = figure('Position', [1300, 200, 600, 200]);

plot(Pout380, n380, 'bs-', 'LineWidth',3,'MarkerFaceColor','b')

xlabel('Output Power (W)')
ylabel('Efficiency (%)')
set(gca, 'YLim', [86.5 91.0],'Ytick',linspace (86.5, 91, 10),'XLim',...
    [0 351], 'Xtick',linspace (0, 350, 11))
grid on
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% MATLAB Script used to plot simulation and experimental data on one plot
% Each plot will have:
% Top Transformer Primary Voltage
% Top Transformer Primary Current
% Bottom Transformer Primary Voltage
% Bottom Transformer Primary Current
% from both experimental data and simulation
%
% The .txt files that contain the data are not contained within this script
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all
clc
close all

%% Import data from LTspice
% general format of data should be
% Column 1      2       3       4       5
%        time   Vtop    Vbottom Ibottom Itop

[t, Vtop, Vbottom, Ibottom, Itop] = textread(...
    'Fundamental Mode - Final Simulation 260 Vin 12 Vout MATLAB.txt');
%     'Fundamental Mode - Final Simulation 410 Vin 12 Vout MATLAB.txt');

FigHandle = figure('Position', [0, 500, 800, 500]);
%Plot top transformer output voltage and input current
subplot(2,1,1)
[a,h1,h2] = plotyy(t,Vtop,t,Itop);
legend('Voltage','Current')
ylabel(a(1),'Voltage (V)','FontSize', 16, 'Fontname','Times New Roman')
ylabel(a(2),'Current (A)','FontSize', 16, 'Fontname','Times New Roman')
xlabel(a(1),'Time (s)','FontSize', 16, 'Fontname','Times New Roman')
title([...
    '\fontsize{20}\fontname{Times New Roman}260Vin, 12Vout, Simulation',...
    '\newline \fontsize{16}            Top Transformer'])

set(a(1),'YLim',[-140, 140],'ytick',linspace(-140,140,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[-6 6],'ytick', linspace(-6,6,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'FontSize', 12, 'Fontname','Times New Roman');

set(h1,'color','blue','LineWidth',3)
set(h2,'color','magenta','LineWidth',3)
set(a,{'ycolor'},{'k';'k'})
grid on

%Plot bottom transformer output voltage and input current
subplot(2,1,2)
[a,h1,h2] = plotyy(t,Vbottom, t,Ibottom);
legend('Voltage','Current')
ylabel(a(1),'Voltage (V)','FontSize', 16, 'Fontname','Times New Roman')
ylabel(a(2),'Current (A)','FontSize', 16, 'Fontname','Times New Roman')
xlabel(a(1),'Time (s)','FontSize', 16, 'Fontname','Times New Roman')
```

```
title('Bottom Transformer','FontSize', 16, 'Fontname','Times New Roman')

set(a(1),'YLim',[-140, 140],'ytick', linspace(-140,140,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[-6, 6],'ytick', linspace(-6,6,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'XTick',0.1,'FontSize', 12, 'Fontname','Times New Roman');

set(h1,'color','cyan','LineWidth',3)
set(h2,'color','green','LineWidth',3)
set(a,{'ycolor'},{'k';'k'})
grid on


%% Import data from scope
% general format of data should be
% Column 1      2       3       4       5
%        time   Vtop    Vbottom Itop    Ibottom

[tE, VtopE, VbottomE, ItopE, IbottomE] = textread(...
    'Fundamental Mode - Final Experimental 260 Vin 12 Vout MATLAB.txt');
%     'Fundamental Mode - Final Experimental 410 Vin 12 Vout MATLAB.txt');

FigHandle = figure('Position', [900, 500, 800, 500]);
%Plot top transformer output voltage and input current
subplot(2,1,1)
[a,h1,h2] = plotyy(tE,VtopE,tE,ItopE);
legend('Voltage','Current')
ylabel(a(1),'Voltage (V)','FontSize', 16, 'Fontname','Times New Roman')
ylabel(a(2),'Current (A)','FontSize', 16, 'Fontname','Times New Roman')
xlabel(a(1),'Time (s)','FontSize', 16, 'Fontname','Times New Roman')
title([...
    '\fontsize{20}\fontname{Times New Roman}260Vin, 12Vout, Experimental',
...
    '\newline \fontsize{16}            Top Transformer'])

set(a(1),'YLim',[-140, 140],'ytick', linspace(-140,140,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[-6 6],'ytick', linspace(-6,6,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'FontSize', 12, 'Fontname','Times New Roman');

set(h1,'color','blue','LineWidth',3)
set(h2,'color','magenta','LineWidth',3)
set(a,{'ycolor'},{'k';'k'})
grid on

%Plot bottom transformer output voltage and input current
subplot(2,1,2)
[a,h1,h2] = plotyy(tE,VbottomE, tE,IbottomE);
legend('Voltage','Current')
ylabel(a(1),'Voltage (V)','FontSize', 16, 'Fontname','Times New Roman')
ylabel(a(2),'Current (A)','FontSize', 16, 'Fontname','Times New Roman')
xlabel(a(1),'Time (s)','FontSize', 16, 'Fontname','Times New Roman')
title('Bottom Transformer','FontSize', 16, 'Fontname','Times New Roman')
```

```
set(a(1),'YLim',[-140, 140],'ytick', linspace(-140,140,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[-6, 6],'ytick', linspace(-6,6,5),'FontSize', 12,...
    'Fontname','Times New Roman');
set(a(2),'XTick',0.1,'FontSize', 12, 'Fontname','Times New Roman');

set(h1,'color','cyan','LineWidth',3)
set(h2,'color','green','LineWidth',3)
set(a,{'ycolor'},{'k';'k'})
grid on

%% Compare the waveforms

FigHandle = figure('Position', [000, 100, 1900, 800]);
subplot(2,1,1)
[a,h1,h2] = plotyy(tE,VtopE,tE,ItopE);

set(h1,'color','blue','LineWidth',3)
set(h2,'color','magenta','LineWidth',3)

set(a,{'ycolor'},{'k';'k'})

ylabel(a(1),'Voltage (V)','FontSize', 24, 'Fontname','Times New Roman')
ylabel(a(2),'Current (A)','FontSize', 24, 'Fontname','Times New Roman')
xlabel(a(1),'Time (s)','FontSize', 24, 'Fontname','Times New Roman')
% title([...
%     '\fontsize{20}\fontname{Times New Roman}260Vin, 12Vout, Comparison',...
%     '\newline \fontsize{16}            Top Transformer'])
title('Top Transformer','FontSize', 24, 'Fontname','Times New Roman')

set(a(1),'YLim',[-140,140],'ytick', linspace(-140,140,5),'FontSize', 20,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[-6 6],'ytick', linspace(-6,6,5),'FontSize', 20,...
    'Fontname','Times New Roman');
set(a(2),'FontSize', 20, 'Fontname','Times New Roman');

axes(a(1))
hold on
plot(t,Vtop,'--b','LineWidth',3);

axes(a(2))
hold on
plot(t,Itop,'--m','LineWidth',3);

l=legend('Current-Experimental','Current-Simulated',...
    'Voltage-Experimental','Voltage-Simulated','location','EastOutside');
set(l,'color','w')
grid on

subplot(2,1,2)
[a,h1,h2] = plotyy(tE,VbottomE,tE,IbottomE);

set(h1,'color','cyan','LineWidth',3)
```

```
set(h2,'color','green','LineWidth',3)

set(a,{'ycolor'},{'k';'k'})

ylabel(a(1),'Voltage (V)','FontSize', 24, 'Fontname','Times New Roman')
ylabel(a(2),'Current (A)','FontSize', 24, 'Fontname','Times New Roman')
xlabel(a(1),'Time (s)','FontSize', 24, 'Fontname','Times New Roman')
title('Bottom Transformer','FontSize', 24, 'Fontname','Times New Roman')

set(a(1),'YLim',[-140, 140],'ytick',linspace(-140,140,5),'FontSize', 20,...
    'Fontname','Times New Roman');
set(a(2),'YLim',[-6 6],'ytick', linspace(-6,6,5),'FontSize', 20,...
    'Fontname','Times New Roman');
set(a(2),'FontSize', 20, 'Fontname','Times New Roman');

axes(a(1))
hold on
plot(t,Vbottom,'--c','LineWidth',3);

axes(a(2))
hold on
plot(t,Ibottom,'--g','LineWidth',3);

l=legend('Current-Experimental','Current-Simulated',...
    'Voltage-Experimental','Voltage-Simulated','location','EastOutside');
set(l,'color','w')
grid on
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Based heavily on David Perreault's PhD optimization file
% Defines variables containing data
% Params for EPCOS's Planar EILP Cores
% http://en.tdk.eu/tdk-en/1190522/products/product-catalog/
% ferrites-and-accessories/epcos-ferrites-and-accessories
% The data sets are as follows:
%   Quantity                Var name          units
%   Core name (Size-AL)     corename          text
%   Outer Diameter          OD                mm
%   Inner Diameter          ID                mm
%   Width                   W                 mm
%   Effective area          Ae                mm^2
%   Effective length        le                mm
%   Effective volume        Vc                mm^3
%   Permeability            ur                numerical
%   Height of core leg      h                 mm
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Core names
corename = {...
'EILP14/3.5/5'; 'EILP18/4/10'; 'EILP22/6/16'; 'EILP32/6/20'; 'EILP38/8/25';
'EILP43/10/28';  %'EILP64/10/50' ; removed because this core is extremely
                 % difficult to get
 };

numcores=length(corename);

% OD is the outer diameter of the core in m
OD = 1/1000*[...  % Conversion from mm to m
  11 ; 14 ; 16.8 ; 25.4 ; 30.8 ; 35.4 ; %53.6 ; ...
  ];

% ID is the inner diameter of the core in m
ID = 1/1000*[...    % Conversion from mm to m
  3 ; 4 ; 5 ; 6.35 ; 7.6 ; 8.1 ; %10.2 ; ...
  ];

% W is the width of the core in m
W = 1/1000*[...     % Conversion from mm to m
    5 ; 10 ; 15 ; 20 ; 25.4 ; 27.9 ; %50.8 ; ...
    ];

% Ae is the effective area in mm^2
Ae = 1/1000000*[... % Conversion from mm^2 to m^2
  14.5; 39.5 ; 78.5 ; 130 ; 194 ; 229 ; %519 ;
  ];

% Vc is the volume of the core in cm^3
Vc = 1/1000*[...    % Conversion from mm^3 to cm^3
   242  ; 802 ; 2050 ; 4560 ; 8440 ; 11500 ; %36200
   ];

% le is the effective length of magnetic material in mm
le = 1/1000*[...    % Conversion from mm to m
```

```
    16.7 ; 20.3 ; 26.1 ; 35.1 ; 52.4 ; 50.8 ; %??
    ];

% ur is the relative permeability of N49
% ur = [780 ; 860 ; 960 ; 950 ; 1040 ; 1030 ; %??
%     ];
ur = 1/1500.*40.*[780 ; 860 ; 960 ; 950 ; 1040 ; 1030 ; %??
    ];

% h is the height of the E core leg
h = 1/1000*[...     % Conversion from mm to m
    2 ; 2 ; 3.2 ; 3.2 ; 4.45 ; 5.4 ; %??
    ];
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Based heavily on David Perreault's PhD optimization file
% Defines variables containing data
% Params for EPCOS's Planar EILP Cores
% http://en.tdk.eu/tdk-en/1190522/products/product-catalog/
% ferrites-and-accessories/epcos-ferrites-and-accessories
% The data sets are as follows:
%   Quantity                Var name          units
%   Core name (Size-AL)     corename          text
%   Outer Diameter          OD                mm
%   Inner Diameter          ID                mm
%   Width                   W                 mm
%   Permeability            u                 numerical
%   AL                      AL                nH/Turns^2
%   Effective area          Ae                mm^2
%   Effective length        le                mm
%   Effective volume        Ve                mm^3
%   Core loss coefficient   a
%   Core loss B exponent    b                 numerical
%   Core loss f exponent    c                 numerical
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Core names
corename = {...
'RM 4' ; 'RM 4LP' ; ...
'RM12' ; 'RM12LP' ; ...
'RM14' ; 'RM14LP' ; ...
'EFD10/5/3' ; 'EFD15/8/5' ; 'EFD20/10/7' ; %'EFD25/13/9' ; 'EFD30/15/9' ;
                                            % not in N49 material

'EIQ13/3' ; 'EIQ20/6' ; 'EIQ25/6' ; 'EIQ30/8' ; ...
'ER11/5' ; 'ER14.5/6' ; 'ER18/3/10' ; 'ER23/5/13' ; 'ER25/6/15' ; ...
'ER32/5/21' ;
'EIR23' ; 'EIR25' ;
 };

numcores=length(corename);

% OD is the outer diameter of the core in m
OD = 1/1000*[...  % Conversion from mm to m
   8 ;  8 ; ...
  25 ; 25 ; ...
  29 ; 29 ; ...
  7.65 ; 11 ; 15.4 ; %18.7 ; 22.4 ; ...
  11.2 ; 18 ; 22 ; 26 ; ...
  8.7 ; 11.8 ; 15.6 ; 20.2 ; 21.7 ; 29.7 ;
  20.2; 21.7 ;
  ];

% ID is the inner diameter of the core in m
ID = 1/1000*[...    % Conversion from mm to m
  3.9  ; 3.9  ; ...
  12.8 ; 12.8 ; ...
  15   ; 15   ; ...
  4.55 ; 5.3 ; 8.9 ; %11.4 ; 14.6 ; ...
  9.05 ; 12.86 ; 14.5 ; 19.45 ; ...
```

```
  4.25 ; 4.7 ; 6.2 ; 8 ; 9.4 ; 11.2 ;
  8 ; 9.4 ;
  ];

% Ae is the effective area in mm^2
Ae = 1/1000000*[... % Conversion from mm^2 to m^2
   13 ;  14.5 ; ...
  146 ; 147.5 ; ...
  200 ; 201   ; ...
  7.2 ; 15 ; 31 ; %58 ; 69 ; ...
  19.8; 59.8 ; 89.7 ; 108 ; ...
  12.4; 17.6 ; 30.2 ; 50.3 ; 70.8 ; 100.5 ;
  50.3; 70.4 ;
  ];

% Vc is the volume of the core in cm^3
Vc = 1/1000*[...    % Conversion from mm^3 to cm^3
    286 ;  251 ; ...
   8320 ; 6195 ; ...
   14000; 10230; ...
   166  ; 510 ; 1460 ; %3310 ; 4690 ; ...
   315 ; 1550 ; 2370 ; 3400 ; ...
   174 ; 333 ; 667 ; 1640 ; 2414 ; 3847 ;
   1335; 1978;
   ];

% le is the effective length of magnetic material in mm
le = 1/1000*[...    % Conversion from mm to m
    22 ; 17.3 ; ...
    57 ; 42 ; ...
    70 ; 50.9 ; ...
    23.1 ; 34 ; 47 ; %57 ; 68 ; ...
    15.9 ; 33.2 ; 32.95 ; 46 ; ...
    14.1 ; 19 ; 22.1 ; 32.6 ; 34.1 ; 38.3 ; ...
    26.6 ; 28.1 ;
    ];

% ur is the relative permeability of N49
ur = [
     750 ;  900 ;  ...
    1150 ; 1020 ; ...
    1090 ; 1030 ; ...
     940 ; 1080 ; 1100 ; %?? ; ?? ; ...
    1020 ; 1070 ; 1010 ; 1130 ; ...
     715 ;  800 ; 1050 ; 1140 ; 1150 ; 1050 ; ...
    1100 ; 1080 ;
    ];

% h is the height of the core set
h = 1/1000*[...     % Conversion from mm to m
       7 ; 4.3 ; ...
    16.8 ; 9.0 ; ...
    20.8 ; 11.1 ; ...
    3.75 ; 5.5 ; 7.7 ; %9.3 ; 11.2 ; ...
    1.75 ; 4.1 ; 3.2 ; 5.3 ; ...
    3    ; 3.3 ; 3.1 ; 6.2 ; 6.2 ; 5.4 ; ...
```

```
3.1 ; 3.1 ;
];
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calculate planar core losses and winding losses for the planar
% transformer of the proposed ICN converter
% Based heavily on David Perreault's PhD optimization files
% Calculates magnetic flux density, current density, core loss, winding
% loss, and total power loss across a range of frequencies from 100 kHz to
% 1 MHz and across a selection of core geometries available in N49
% material.
% Several plots are generated and the minimum loss design across frequency
% is shown.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all
clc
close all

% load core data
EILPCoredat;
Coretype = 2;       % Let 1 be for RM and 2 be for E

%% design specifications
F=401;           % How many frequencies to check
f = linspace(100000,1000000,F);             % frequency in Hz
d = sqrt(2./(4*pi*10^-7*2*pi.*f*10^8/2.3)); % skin depth in m
% Current values are pulled from simulation and depend on operating
% conditions.  Usually, 260Vin, 12Vout, 400Wout. Values will vary depending
% on the input voltage.  Minimum RMS current possible for this power and
% voltage would be 33 Arms (400/12)

I = 63;          % Max Current
Irms1 = 37.144; % 260V current top transformer
Irms2 = 31.384; % 260V current bottom transformer
Bmax = 1;        % maximum flux density in T
Jmax = 10000;    % A/cm^2
mu=4*pi*10^-7;   % Permeability of free space
p = 2.3e-8;      % Resistivity of copper (Ohm-m)

%% save core data
Bpk1 = zeros(numcores,F);
Bpk2 = zeros(numcores,F);
Jwire1 = zeros(numcores,F);
Jwire2 = zeros(numcores,F);
Pcore1 = zeros(numcores,F);
Pcore2 = zeros(numcores,F);
Pwind = zeros(numcores,F);
Ptot = zeros(numcores,F);
designok = zeros(numcores,F);

%% Loop through available cores and synthesize inductor designs

for i=1:F
    f(i)
    for core = 1:numcores
        designok(core,i) = 1; % assume this core design works
            % Calc B at peak current in Tesla
```

```
% Input voltage of 260 V, 55 comes from simulation and incorporates
% imbalance
Bpk1(core,i) = (55/2)/(10*f(i)*Ae(core));
if Bpk1(core,i) > Bmax
    designok(core,i) = 0;   % design is not ok
    disp([corename{core,:},' @ ',num2str(f(i)),...
        ' rejected: Bpk1 = ',num2str(Bpk1(core,i)),' gauss']);
end
% Input voltage of 260 V, 55 comes from simulation and incorporates
% imbalance
Bpk2(core,i) = (73/2)/(10*f(i)*Ae(core));

% If design is still ok, check to make sure that current in wire
% is at an acceptable level.  Reject the design if not.  We require
% the rms current density to be less than 6000 A/in^2 or 930 A/cm^2
 Jwire1(core,i) = Irms1/((d(i)*100*(OD(core)-ID(core))*100/2));
 if designok(core,i) == 1;
     if Jwire1(core,i) > Jmax
         designok(core,i) = 0;
         disp([corename{core,:},' @ ',num2str(f(i)),...
             ' rejected: Jwire1 = ',num2str(Jwire1(core,i)),...
             ' A/cm^2']);
     end
 end
 Jwire2(core,i) = Irms2/((d(i)*100*(OD(core)-ID(core))*100/2));

% Calculate losses - both core and winding losses
% Core loss parameters are based on Steinmetz values from EPCOS'
% Magnetic Design Tool:
% 25 kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 50        2.46            1.3539      2.9043
% 100       18.18           1.3813      2.9043
% 200       141.92          1.5009      2.9043
% 300       439.21          1.141       2.9043
%
% 50 kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 50        4.92            1.3539      2.9574
% 100       39.56           1.3813      2.9574
% 200       313.59          1.5009      2.9574
% 300       968.59          1.141       2.9574
%
% 100 kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        1.53            1.7289      2.9889
% 50        10.29           1.3539      2.9889
% 100       87.82           1.3813      2.9889
% 200       747.23          1.5009      2.9889
%
% 200kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        3.29            1.7289      3.0995
% 50        22.69           1.3539      3.0995
% 100       196.24          1.3813      3.0995
% 200       2065.65         1.5009      3.0995
```

```
%
% 300kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        5.823           1.7289      3.386
% 50        37.2            1.3539      3.386
% 100       329.57          1.3813      3.386
% 200       7026            1.5009      3.386
%
% 500kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 13        2.52            3.0084      2.7746
% 25        13.45           1.7289      2.7746
% 50        82.19           1.3539      2.7746
% 100       749.56          1.3813      2.7746

    if f(i)<100000
        Cm = 87.82;         % Coefficient of power for N49
        x = 1.3813;         % exponent of f for N49
        y = 2.9889;         % exponent of Bpk for N49
        Pcore(core,i)=...
            Cm*(f(i)/100000)^x*(((Bpk1(core,i)/100e-3)^y)+...
            (Bpk2(core,i)/100e-3)^y)*Vc(core)/1000;
    elseif f(i)<250000
        Cm = 196.24;        % Coefficient of power for N49
        x = 1.3539;         % exponent of f for N49
        y = 3.0995;         % exponent of Bpk for N49
        Pcore(core,i)=...
            Cm*(f(i)/200000)^x*(((Bpk1(core,i)/100e-3)^y)+...
            (Bpk2(core,i)/100e-3)^y)*Vc(core)/1000;
%     elseif f(i)<300000 % alternative parameters based on f, Bpk
%         Cm = 329.57;        % Coefficient of power for N49
%         x = 1.3813;         % exponent of f for N49
%         y = 3.386;          % exponent of Bpk for N49
%         Pcore(core,i)=...
%             Cm*(f(i)/300000)^x*(((Bpk1(core,i)/100e-3)^y)+...
%             (Bpk2(core,i)/100e-3)^y)*Vc(core)/1000;
%     elseif f(i)<350000 % alternative parameters based on f, Bpk
%         Cm = 37.2;          % Coefficient of power for N49
%         x = 1.3539;         % exponent of f for N49
%         y = 3.386;          % exponent of Bpk for N49
%         Pcore(core,i)=...
%             Cm*(f(i)/300000)^x*(((Bpk1(core,i)/50e-3)^y)+...
%             (Bpk2(core,i)/50e-3)^y)*Vc(core)/1000;
    elseif f(i)<1050000
        Cm = 82.19;         % Coefficient of power for N49
        x = 1.3539;         % exponent of f for N49
        y = 2.7746;         % exponent of Bpk for N49
        Pcore(core,i)=...
            Cm*(f(i)/500000)^x*(((Bpk1(core,i)/50e-3)^y)+...
            (Bpk2(core,i)/50e-3)^y)*Vc(core)/1000;
    end

     % Calculate winding losses. We assume we will use foil/PCB and
     % current will only travel through copper that is one skin
     % depth thick. Current paths are calculated as the average
     % turn.
```

```
            if Coretype == 1;
                R(core,i) = ...
                    p*pi*(OD(core)+ID(core))/(d(i)*(OD(core)-ID(core)));
            elseif Coretype == 2;
                R(core,i) = ...
                    p*(2*ID(core)+2*W(core)+pi*(OD(core)-ID(core))/2)...
                    /(d(i)*(OD(core)-ID(core))/2);
            end

            % Calculate total winding loss.  There are two transformers
            % and we assume that the winding loss is split evenly between
            % the primary winding and the secondary winding. We anticipate
            % using 8 layers, so there will be 4 layers to spread the
            % current over but it may not spread evenly, so a conservative
            % design will assume the winding area is increased by only a
            % factor of 2 (rather than a most optimistic estimate of 4)
            % due to the parallel nature of the primary windings
            Pwind(core,i) = 2*(Irms1^2+Irms2^2)*R(core,i)/2;

            Ptot(core,i) = Pcore(core,i)+Pwind(core,i);

           % If design is ok, display the data
           if designok(core,i) == 1
               disp('              ');
               disp([corename{core,:},' :']);
               disp(['Bpk = ',num2str(Bpk1(core,i))]);
               disp(['Jwire = ',num2str(Jwire1(core,i)),' A/cm^2']);
               disp(['Pcore = ',num2str(Pcore(core,i)),' Watts']);
               disp(['Pwind = ',num2str(Pwind(core,i)),' Watts']);
               disp(['Ptot = ',num2str(Pcore(core,i)+Pwind(core,i)),...
                   ' Watts']);
               disp(['              ']);
           end
    end
    disp('%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%')
end

%Plot the core loss across core volume
figure
for i =1:F
    for core = 1:numcores
        if designok(core,i)==1
            plot(Vc(core),Ptot(core,i),'*')
            hold on
        end
    end
    hold all
end
grid on
xlabel('Core Volume (mm^3)')
ylabel('Total Power Loss Loss (W)')

% Filter out all invalid designs
for i = 1:F
    j(i)=0;
```

```
    for core = 1:numcores
        if (designok(core,i) == 1)
            j(i)=j(i)+1;
            corenamevalid{j(i),i} = corename{core,:};
            Bpkvalid(j(i),i) = Bpk1(core,i);
            Jwirevalid(j(i),i) = Jwire1(core,i);
            Pcorevalid(j(i),i) = Pcore(core,i);
            Pwindvalid(j(i),i) = Pwind(core,i);
            Ptotvalid(j(i),i) = Ptot(core,i);
        end
    end
end

%Plot the core loss across core
figure
for i =1:F
    plot(1:j(i),Pcorevalid(1:j(i),i))
    title('Core Loss vs core')
    hold all
end
grid on
xlabel('Core')
ylabel('Core Loss (W)')

figure
for i =1:F
    plot(1:j(i),Ptotvalid(1:j(i),i))
    hold all
end
title('Total Power Loss vs core')
xlabel('Core')
ylabel('Total Power Loss (W)')

% Find the minimum loss design for each frequency and then display the
% minimum loss design out of all options.
for g =1:F
    [Y(g),i(g)] = min(Ptotvalid(1:j(g),g));
end
   [X,k] = min(Y);

    disp('********************************');
    disp(['f = ',num2str(f(k)),' Hz']);
    disp([corenamevalid{i(k),k},' :']);
    disp(['Bpk = ',num2str(Bpkvalid(i(k),k))]);
    disp(['Jwire = ',num2str(Jwirevalid(i(k),k)),' A/cm^2']);
    disp(['Pcore = ',num2str(Pcorevalid(i(k),k)),' Watts']);
    disp(['Pwind = ',num2str(Pwindvalid(i(k),k)),' Watts']);
    disp(['Ptot = ',num2str(Ptotvalid(i(k),k)),' Watts']);
    disp(['********************************']);

%Plot the minimum loss for each frequency
figure
plot(f/1000,Y)
title('Total Power Loss vs Frequency')
xlabel('Frequency (kHz)')
ylabel('Minimum Total Power Loss (W)')
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calculate planar core losses and winding losses for the planar
% inductors of the proposed ICN converter
% Based heavily on David Perreault's PhD optimization files
% Calculates magnetic flux density, current density, core loss, winding
% loss, and total power loss across a range of frequencies from 100 kHz to
% 1 MHz and across a selection of core geometries available in N49
% material.
% Several plots are generated and the minimum loss design across frequency
% is shown.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all
clc
close all

% load core data
EILPCoredat;
Coretype = 1;       % Let 1 be for E and 2 be for ER

%% design specifications
F=401;           % How many frequencies to check
f = linspace(100000,1000000,F);              % frequency in Hz
d = sqrt(2./(4*pi*10^-7*2*pi.*f*10^8/2.3)); % skin depth in m
% Current values are pulled from simulation and depend on operating
% conditions.  Values will vary depending on the input voltage.

Ipk = 50;           % coupled inductor 260V max current
Irms1 = 31.384;     % coupled inductor 260V currents
Irms2 = 32.109;     % coupled inductor 260V currents
% Irms1 = 19;         % coupled inductor 410V currents
% Irms2 = 32;         % coupled inductor 410V currents
% Ipk = 59;           % resonant inductor 260V max current
% Irms1 = 41.656;       % resonant inductor 260V current
% Ipk = 35;           % resonant inductor 410V max current
% Irms1 = 26.082;   % resonant inductor 410V current
% Irms2 = 0;          % resonant inductor current

Bmax = 1;       % maximum flux density in T
Jmax = 10000;   % A/cm^2
Tmax = 150;     % maximum temperature rise in deg Celcius
% L = 0.3037./(2*pi.*f)/2;           % resonant inductance in H
L = 0.2827./(2*pi.*f)/2;         % coupled inductor inductance in H
Lmin = 0.98*L;  % Minimum allowable inductance
Lmax = 2*L;     % Maximum allowable inductance
mu=4*pi*10^-7;  % Permeability of free space
p = 1.68e-8;    % Resistivity of copper (Ohm-m)

%% save core data
lg = zeros(numcores,F);
ue = zeros(numcores,F);
Bpk = zeros(numcores,F);
Jwire = zeros(numcores,F);
Pcore = zeros(numcores,F);
```

```
R = zeros(numcores,F);
Pwind = zeros(numcores,F);
Lc = zeros(numcores,F);
designok = zeros(numcores,F);

%% Loop through available cores and synthesize inductor designs

for i=1:F;
    f(i)
    for core = 1:numcores
        designok(core,i) = 1; % assume this core design works

        N = 1;  % Assumption due to high current

        % Calc the length of the gap to get desired inductance
        lg(core,i) = mu*Ae(core)/L(i)-le(core)/ur(core);
        if lg(core,i) > h(core)/2
            designok(core,i) = 0;     % design is not ok
            disp([corename{core,:},' @ ',num2str(f(i)),...
                ' rejected: lg = ',num2str(lg(core,i)),' m']);
        elseif lg(core,i) < 0;
            designok(core,i) = 0;     % design is not ok
            disp([corename{core,:},' @ ',num2str(f(i)),...
                ' rejected: lg = ',num2str(lg(core,i)),' m']);
        end

        % Calc the effective permeability (coefficient)
        ue(core,i) = ur(core)/(1+ur(core)*lg(core,i)/le(core));
        if ue(core,i) < 0
            designok(core,i) = 0;     % design is not ok
        end

        Bpk(core,i) = ue(core,i)*mu*N*Ipk/le(core);
        if Bpk(core,i) > Bmax
            designok(core,i) = 0;     % design is not ok
            disp([corename{core,:},' @ ',num2str(f(i)),...
                ' rejected: Bpk = ',num2str(Bpk(core,i)),' gauss']);
        end
        % If design is still ok, check to make sure that current in wire
        % is at an acceptable level.  Reject the design if not.
         Jwire(core,i) = Irms1/(4*d(i)*100*(OD(core)-ID(core))/2*100);
         if designok(core,i) == 1;
             if Jwire(core,i) > Jmax
                 designok(core,i) = 0;
                 disp([corename{core,:},' @ ',num2str(f(i)),...
                     ' rejected: Jwire = ',num2str(Jwire(core,i)),...
                     ' A/cm^2']);
             end
         end
        % Calculate losses - both core and winding losses
        % Core loss parameters are based on Steinmetz values from EPCOS'
        % Magnetic Design Tool:
        % 25 kHz at 100 C
        % B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
        % 50        2.46            1.3539      2.9043
        % 100       18.18           1.3813      2.9043
```

```
% 200       141.92          1.5009      2.9043
% 300       439.21          1.141       2.9043
%
% 50 kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 50        4.92            1.3539      2.9574
% 100       39.56           1.3813      2.9574
% 200       313.59          1.5009      2.9574
% 300       968.59          1.141       2.9574
%
% 100 kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        1.53            1.7289      2.9889
% 50        10.29           1.3539      2.9889
% 100       87.82           1.3813      2.9889
% 200       747.23          1.5009      2.9889
%
% 200kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        3.29            1.7289      3.0995
% 50        22.69           1.3539      3.0995
% 100       196.24          1.3813      3.0995
% 200       2065.65         1.5009      3.0995
%
% 300kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        5.823           1.7289      3.386
% 50        37.2            1.3539      3.386
% 100       329.57          1.3813      3.386
% 200       7026            1.5009      3.386
%
% 500kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 13        2.52            3.0084      2.7746
% 25        13.45           1.7289      2.7746
% 50        82.19           1.3539      2.7746
% 100       749.56          1.3813      2.7746

    if f(i)<100000
        Cm = 87.82;         % Coefficient of power for N49
        x = 1.3813;         % exponent of f for N49
        y = 2.9889;         % exponent of Bpk for N49
        Pcore(core,i)=...
           Cm*(f(i)/100000)^x*(Bpk(core,i)/100e-3)^y*Vc(core)/1000;
    elseif f(i)<250000
        Cm = 22.69;         % Coefficient of power for N49
        x = 1.3539;         % exponent of f for N49
        y = 3.0995;         % exponent of Bpk for N49
        Pcore(core,i)=...
           Cm*(f(i)/200000)^x*(Bpk(core,i)/50e-3)^y*Vc(core)/1000;
%     elseif f(i)<250000  % alternative parameters based on f, Bpk
%         Cm = 196.24;      % Coefficient of power for N49
%         x = 1.3813;         % exponent of f for N49
%         y = 3.0995;         % exponent of Bpk for N49
%         Pcore(core,i)=...
%            Cm*(f(i)/200000)^x*(Bpk(core,i)/100e-3)^y*Vc(core)/1000;
    elseif f(i)<300000      % remove this for EI64 and RM cores
```

```
    Cm = 329.57;          % Coefficient of power for N49
    x = 1.3813;           % exponent of f for N49
    y = 3.386;            % exponent of Bpk for N49
    Pcore(core,i)=...
       Cm*(f(i)/300000)^x*(Bpk(core,i)/100e-3)^y*Vc(core)/1000;
elseif f(i)<350000        % remove this for EI64 and RM cores
    Cm = 37.2;            % Coefficient of power for N49
    x = 1.3539;           % exponent of f for N49
    y = 3.386;            % exponent of Bpk for N49
    Pcore(core,i)=...
       Cm*(f(i)/300000)^x*(Bpk(core,i)/50e-3)^y*Vc(core)/1000;
elseif (f(i)<1050000) || (Bpk(core,i)<60e-3)
    Cm = 82.19;           % Coefficient of power for N49
    x = 1.3539;           % exponent of f for N49
    y = 2.7746;           % exponent of Bpk for N49
    Pcore(core,i)=...
        Cm*(f(i)/500000)^x*(Bpk(core,i)/50e-3)^y*Vc(core)/1000;
elseif (f(i)<1050000) || (Bpk(core,i)>=60e-3)
    Cm = 749.56;          % Coefficient of power for N49
    x = 1.3813;           % exponent of f for N49
    y = 2.7746;           % exponent of Bpk for N49
    Pcore(core,i)=...
        Cm*(f(i)/500000)^x*(Bpk(core)/100e-3)^y*Vc(core)/1000;
end


 % Calculate winding losses. We assume we will use foil/PCB and
 % current will only travel through copper that is one skin
 % depth thick or 4 oz. copper. Current paths are calculated as
 % the average turn.

 if Coretype == 1;
     if d(i) < 140e-6;
        R(core,i) = ...
            4*p*(W(core)+OD(core))/...
            (d(i)*(OD(core)-ID(core)));
     else
        R(core,i) = ...
            4*p*(W(core)+OD(core))/...
            (140e-6*(OD(core)-ID(core)));
     end
 elseif Coretype == 2;
     if d(i) < 140e-6;
        R(core,i) = ...
            p*pi*(OD(core)+ID(core))/...
            (d(i)*(OD(core)-ID(core)));
     else
        R(core,i) = ...
            p*pi*(OD(core)+ID(core))/...
            (140e-6*(OD(core)-ID(core)));
     end
 end

 Pwind(core,i) = (Irms1^2+Irms2^2)*R(core,i);

 % Calculate total winding loss.
```

```
             Ptot(core,i) = Pcore(core,i)+Pwind(core,i);

            % If design is ok, check inductance
            % Calc L based on integer N
            Lc(core,i) = 1^2/(le(core)/ur(core)+lg(core,i))*(mu*Ae(core));

            % If design is ok, display the data
            if designok(core,i) == 1
                disp('              ');
                disp([corename{core,:},' :']);
                disp(['L = ',num2str(Lc(core,i)), ' nH']);
                disp(['lg = ',num2str(lg(core,i)), ' m']);
                disp(['Bpk = ',num2str(Bpk(core,i))]);
                disp(['Jwire = ',num2str(Jwire(core,i)),' A/cm^2']);
                disp(['Pcore = ',num2str(Pcore(core,i)),' Watts']);
                disp(['Pwind = ',num2str(Pwind(core,i)),' Watts']);
                disp(['Ptot = ',num2str(Pcore(core,i)+Pwind(core,i)),'
Watts']);
                disp(['              ']);
            end
    end
end

%Plot the core loss across core volume
figure
for i =1:F
    for core = 1:numcores
        if designok(core,i)==1
            plot(Vc(core),Ptot(core,i),'*')
            hold all
        end
    end
    hold all
end
grid on
xlabel('Core Volume (mm^3)')
ylabel('Total Power Loss Loss (W)')

% Filter out all invalid designs
for i = 1:F
    j(i)= 0;
    for core = 1:numcores
        if (designok(core,i) == 1)
            j(i)=j(i)+1;
            corenamevalid{j(i),i} = corename{core,:};
            Lcvalid(j(i),i) = Lc(core,i);
            lgvalid(j(i),i) = lg(core,i);
            Bpkvalid(j(i),i) = Bpk(core,i);
            Jwirevalid(j(i),i) = Jwire(core,i);
            Pcorevalid(j(i),i) = Pcore(core,i);
            Rvalid(j(i),i) = R(core,i);
            Pwindvalid(j(i),i) = Pwind(core,i);
            Ptotvalid(j(i),i) = Ptot(core,i);
            fvalid(i) = f(i);
        end
    end
```

```
end

%Plot the core loss across core
figure
for i =1:F
    if j(i) >0
        plot(1:j(i),Pcorevalid(1:j(i),i))
        hold all
    end
end
title('Core Loss vs core')
xlabel('Core')
ylabel('Core Loss (W)')

figure
for i =1:length(Ptotvalid)
    if j(i) >0
        plot(1:j(i),Ptotvalid(1:j(i),i))
        hold all
    end
end
title('Total Power Loss vs core')
xlabel('Core')
ylabel('Total Power Loss (W)')

% Find the minimum loss design for each frequency and then display the
% minimum loss design out of all options.
for g=1:length(Ptotvalid)
    j(g);
    if j(g) > 0
        [Y(g),i(g)] = min(Ptotvalid(1:j(g),g));
    else
        Y(g) = NaN;
        i(g) = g;
    end
end
   [X,k] = min(Y);

    disp('********************************');
    disp(['f = ',num2str(fvalid(k)),' Hz']);
    disp([corenamevalid{i(k),k},' :']);
    disp(['L = ',num2str(Lcvalid(i(k),k)), ' nH']);
    disp(['lg = ',num2str(lgvalid(i(k),k)), ' m']);
    disp(['Bpk = ',num2str(Bpkvalid(i(k),k))]);
    disp(['Jwire = ',num2str(Jwirevalid(i(k),k)),' A/cm^2']);
    disp(['Pcore = ',num2str(Pcorevalid(i(k),k)),' Watts']);
    disp(['Pwind = ',num2str(Pwindvalid(i(k),k)),' Watts']);
    disp(['Ptot = ',num2str(Ptotvalid(i(k),k)),' Watts']);
    disp(['********************************']);

%Plot the minimum loss for each frequency
figure
plot(fvalid/1000,Y)
title('Total Power Loss vs frequency')
xlabel('frequency (kHz)')
ylabel('Minimum Total Power Loss (W)')
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calculate planar core losses and winding losses for the two primary, one
% secondary transformer design of the proposed reconfigurable double
% stacked active bridge converter
% Based heavily on David Perreault's PhD optimization files
% Calculates magnetic flux density, current density, core loss, winding
% loss, and total power loss across a range of frequencies from 100 kHz to
% 1 MHz and across a selection of core geometries available in N49
% material.
% Several plots are generated and the minimum loss design across frequency
% is shown.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Operating paramters
clear all
clc
close all

% load core data
EILPCoredat;
Coretype = 2;       % Let 1 be for RM and 2 be for E

%% design specifications
F=401;          % How many frequencies to check
f = linspace(100000,1000000,F);             % frequency in Hz
d = sqrt(2./(4*pi*10^-7*2*pi.*f*10^8/2.3)); % skin depth in m
for i=1:F
    if d(i)>140e-6;
        d(i) = 140e-6;     %cap copper thickness to that of 4 oz
    end
end
% Current values are pulled from simulation under operating condition of
% 380Vin, 12Vout, 400W out, total inductance of 4uH, phase shift of 4.95%,
% dead-time of 20uS, 500 kHz, 256uH for primary winding, and 1uH for the
% secondary winding, using EPC2012C devices.  Values will vary depending on
% the frequency, phase-shift, and dead-time.  Minimum RMS current possible
% for this power and voltage would be 33 Arms (400/12)
Irms1 = 37.169; % secondary current top transformer
Irms2 = 37.169; % secondary current bottom transformer
Bmax = 1;       % maximum flux density in T
Jmax = 10000;   % maximum rms current density in A/cm^2
mu=4*pi*10^-7;  % Permeability of free space
p = 2.3e-8;     % Resistivity of copper (Ohm-m) at 100 C

%% save core data
Bpk1 = zeros(numcores,F);
Bpk2 = zeros(numcores,F);
Jwire1 = zeros(numcores,F);
Jwire2 = zeros(numcores,F);
Pcore1 = zeros(numcores,F);
Pcore2 = zeros(numcores,F);
R = zeros(numcores,F);
Pwind = zeros(numcores,F);
Ptot = zeros(numcores,F);
designok = zeros(numcores,F);
```

```
%% Loop through available cores and synthesize transformer designs

for i=1:F
    f(i)
    for core = 1:numcores
        designok(core,i) = 1;   % to start, assume this core design works
        % Nominal operating point of 380
        Bpk1(core,i) = (190/2)/(16*f(i)*Ae(core));  % Calc B in Tesla
        if Bpk1(core,i) > Bmax
            designok(core,i) = 0;   % design is not ok
            disp([corename{core,:},' @ ',num2str(f(i)),...
                ' rejected: Bpk1 = ',num2str(Bpk1(core,i)),' gauss']);
        end
        Bpk2(core,i) = (190/2)/(16*f(i)*Ae(core));  % Calc B in Tesla

        % If design is still ok, check to make sure that current in wire
        % is at an acceptable level.  Reject the design if not.
         Jwire1(core,i) = Irms1/((d(i)*100*(OD(core)-ID(core))*100/2));
         if designok(core,i) == 1;
             if Jwire1(core,i) > Jmax
                 designok(core,i) = 0;  % design is not ok
                 disp([corename{core,:},' @ ',num2str(f(i)),...
                     ' rejected: Jwire1 = ',num2str(Jwire1(core,i)),...
                     ' A/cm^2']);
             end
         end
         Jwire2(core,i) = Irms2/((d(i)*100*(OD(core)-ID(core))*100/2));

        % Calculate losses - both core and winding losses
        % Core loss parameters are based on Steinmetz values from EPCOS'
        % Magnetic Design Tool:
        % 25 kHz at 100 C
        % B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
        % 50        2.46            1.3539      2.9043
        % 100       18.18           1.3813      2.9043
        % 200       141.92          1.5009      2.9043
        % 300       439.21          1.141       2.9043
        %
        % 50 kHz at 100 C
        % B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
        % 50        4.92            1.3539      2.9574
        % 100       39.56           1.3813      2.9574
        % 200       313.59          1.5009      2.9574
        % 300       968.59          1.141       2.9574
        %
        % 100 kHz at 100 C
        % B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
        % 25        1.53            1.7289      2.9889
        % 50        10.29           1.3539      2.9889
        % 100       87.82           1.3813      2.9889
        % 200       747.23          1.5009      2.9889
        %
        % 200kHz at 100 C
        % B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
        % 25        3.29            1.7289      3.0995
        % 50        22.69           1.3539      3.0995
```

```
% 100       196.24          1.3813      3.0995
% 200       2065.65         1.5009      3.0995
%
% 300kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 25        5.823           1.7289      3.386
% 50        37.2            1.3539      3.386
% 100       329.57          1.3813      3.386
% 200       7026            1.5009      3.386
%
% 500kHz at 100 C
% B [mT]    Pvsin [kW/m3]   alpha [-]   beta [-]
% 13        2.52            3.0084      2.7746
% 25        13.45           1.7289      2.7746
% 50        82.19           1.3539      2.7746
% 100       749.56          1.3813      2.7746

    if f(i)<150000
        Cm = 87.82;         % Coefficient of power for N49
        x = 1.3813;         % exponent of f for N49
        y = 2.9889;         % exponent of Bpk for N49
        Pcore(core,i)=...
            Cm*(f(i)/100000)^x*(((Bpk1(core,i)/100e-3)^y)+...
            (Bpk2(core,i)/100e-3)^y)*Vc(core)/2/1000;
%     elseif f(i)<200000 % alternative parameters based on f, Bpk
%         Cm = 196.24;        % Coefficient of power for N49
%         x = 1.3539;         % exponent of f for N49
%         y = 3.0995;         % exponent of Bpk for N49
%         Pcore(core,i)=...
%             Cm*(f(i)/200000)^x*(((Bpk1(core,i)/100e-3)^y)+...
%             (Bpk2(core,i)/100e-3)^y)*Vc(core)/2/1000;
%     elseif f(i)<250000 % alternative parameters based on f, Bpk
%         Cm = 37.2;          % Coefficient of power for N49
%         x = 1.3539;         % exponent of f for N49
%         y = 3.386;          % exponent of Bpk for N49
%         Pcore(core,i)=...
%             Cm*(f(i)/300000)^x*(((Bpk1(core,i)/50e-3)^y)+...
%             (Bpk2(core,i)/50e-3)^y)*Vc(core)/2/1000;
    elseif f(i)<350000
        Cm = 329.57;        % Coefficient of power for N49
        x = 1.3813;         % exponent of f for N49
        y = 3.386;          % exponent of Bpk for N49
        Pcore(core,i)=...
            Cm*(f(i)/300000)^x*(((Bpk1(core,i)/100e-3)^y)+...
            (Bpk2(core,i)/100e-3)^y)*Vc(core)/2/1000;
%     elseif f(i)<750000 % alternative parameters based on f, Bpk
%         Cm = 13.45;         % Coefficient of power for N49
%         x = 1.7289;         % exponent of f for N49
%         y = 2.7746;         % exponent of Bpk for N49
%         Pcore(core,i)=...
%             Cm*(f(i)/500000)^x*(((Bpk1(core,i)/25e-3)^y)+...
%             (Bpk2(core,i)/25e-3)^y)*Vc(core)/2/1000;
    elseif f(i)<1050000
        Cm = 13.45;         % Coefficient of power for N49
        x = 1.7289;         % exponent of f for N49
        y = 2.7746;         % exponent of Bpk for N49
        Pcore(core,i)=...
```

```
                    Cm*(f(i)/500000)^x*((Bpk1(core,i)/25e-3)^y+...
                    (Bpk2(core,i)/25e-3)^y)*Vc(core)/2/1000;
%               elseif f(i)<1050000 % alternative parameters based on f, Bpk
%                   Cm = 2.52;          % Coefficient of power for N49
%                   x = 3.0084;         % exponent of f for N49
%                   y = 2.7746;         % exponent of Bpk for N49
%                   Pcore(core,i)=...
%                       Cm*(f(i)/500000)^x*(((Bpk1(core,i)/13e-3)^y)+...
%                       (Bpk2(core,i)/13e-3)^y)*Vc(core)/2/1000;
                end


                % Calculate winding losses. We assume we will use foil/PCB and
                % current will only travel through copper that is one skin
                % depth thick. Current paths are calculated as the average
                % turn.

                % Calculate resistance for one turn
                if Coretype == 1;
                    R(core,i) = ...
                        p*pi*(OD(core)+ID(core))/(d(i)*(OD(core)-ID(core)));
                elseif Coretype == 2;
                    R(core,i) = ...
                        p*(2*ID(core)+2*W(core)+pi*(OD(core)-ID(core))/2)...
                        /(d(i)*(OD(core)-ID(core))/2);
                end

                % Calculate total winding loss.  There are three windings and
                % we assume that the winding loss in all three are equal.
                % Each winding is split evenly across 4 layers.
                Pwind(core,i) = 3/4*(Irms1^2)*R(core,i);

                Ptot(core,i) = Pcore(core,i)+Pwind(core,i);

               % If design is ok, display the data
               if designok(core,i) == 1
                   disp('              ');
                   disp([corename{core,:},' :']);
                   disp(['Bpk = ',num2str(Bpk1(core,i))]);
                   disp(['Jwire = ',num2str(Jwire1(core,i)),' A/cm^2']);
                   disp(['Pcore = ',num2str(Pcore(core,i)),' Watts']);
                   disp(['Pwind = ',num2str(Pwind(core,i)),' Watts']);
                   disp(['Ptot = ',num2str(Pcore(core,i)+Pwind(core,i)),...
                       ' Watts']);
                   disp(['              ']);
               end
    end
    disp('%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%')
end

%Plot the core loss across core volume
FigHandle = figure('Position', [0, 200, 800, 300]);
for i =1:F
    for core = 1:numcores
        if designok(core,i)==1
```

```
            %logY so that low power loss is more easily seen
            semilogy(Vc(core),Ptot(core,i),'*')
            hold on
        end
    end
    hold all
end
grid on
xlabel('Core Volume (mm^3)')
ylabel('Total Power Loss Loss (W)')
set(gca, 'XTick', [0.242;0.802;2.050;4.560;8.440;11.500],...
    'XTickLabel', [242;802;2050;4560;8440;11500])

%Plot the core loss across core
FigHandle = figure('Position', [0, 600, 800, 300]);
for i =1:F
    for core = 1:numcores
        %logY so that low power loss is more easily seen
        semilogy(1:core,Pcore(1:core,i))
        hold all
    end
end
grid on
xlabel('Core')
ylabel('Core Loss (W)')
set(gca, 'XTick', 1:6,...
    'XTickLabel', ['EILP14';'EILP18';'EILP22';'EILP32';'EILP38';'EILP43'])

%Plot the total loss for across core
FigHandle = figure('Position', [800, 600, 800, 300]);
for i =1:F
    for core = 1:numcores
        %logY so that low power loss is more easily seen
        semilogy(1:core,Ptot(1:core,i))
        hold all
    end
end
grid on
xlabel('Core')
ylabel('Total Power Loss (W)')
set(gca, 'XTick', 1:6,...
    'XTickLabel', ['EILP14';'EILP18';'EILP22';'EILP32';'EILP38';'EILP43'])

%Plot the winding loss for across core
FigHandle = figure('Position', [800, 800, 800, 300]);
for i =1:F
    for core = 1:numcores
        %logY so that low power loss is more easily seen
        plot(1:core,Pwind(1:core,i))
        hold all
    end
end
grid on
xlabel('Core')
ylabel('Total Winding Loss (W)')
set(gca, 'XTick', 1:6,...
```

```
    'XTickLabel', ['EILP14';'EILP18';'EILP22';'EILP32';'EILP38';'EILP43'])

% Filter out all invalid designs
for i = 1:F
    j(i)=0;
    for core = 1:numcores
        if (designok(core,i) == 1)
            j(i)=j(i)+1;
            corenamevalid{j(i),i} = corename{core,:};
            Bpkvalid(j(i),i) = Bpk1(core,i);
            Jwirevalid(j(i),i) = Jwire1(core,i);
            Pcorevalid(j(i),i) = Pcore(core,i);
            Rvalid(j(i),i) = R(core,i);
            Pwindvalid(j(i),i) = Pwind(core,i);
            Ptotvalid(j(i),i) = Ptot(core,i);
        end
    end
end

% Find the minimum loss design for each frequency and then display the
% minimum loss design out of all options.
for g =1:F
    [Y(g),i(g)] = min(Ptotvalid(1:j(g),g));
end
   [X,k] = min(Y);

    disp('********************************');
    disp(['f = ',num2str(f(k)),' Hz']);
    disp([corenamevalid{i(k),k},' :']);
    disp(['Bpk = ',num2str(Bpkvalid(i(k),k))]);
    disp(['Jwire = ',num2str(Jwirevalid(i(k),k)),' A/cm^2']);
    disp(['Pcore = ',num2str(Pcorevalid(i(k),k)),' Watts']);
    disp(['Pwind = ',num2str(Pwindvalid(i(k),k)),' Watts']);
    disp(['Ptot = ',num2str(Ptotvalid(i(k),k)),' Watts']);
    disp(['********************************']);

%Plot the minimum loss for each frequency
FigHandle = figure('Position', [800, 200, 800, 300]);
plot(f/1000,Y,'LineWidth',3)
xlabel('Frequency (kHz)')
ylabel('Minimum Total Power Loss (W)')
```

Appendix B *M2Spice* Geometry Files

This Appendix contains the *M2Spice* geometry files that were used as an input to the *M2Spice* software tool. It was used to determine the best planar winding layer stackup for the transformers, coupled inductor and resonant inductor of the ICN converter. *M2Spice* is open-sourced and available at: http://www.rle.mit.edu/per/m2spice/

B.1 Transformer

EILP43 4 layer PSPS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,2,1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [5.2661e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = bot
nlayer = 4
d = 82.5e-3

EILP43 4 layer PPSS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,1,2,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [5.2661e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = bot
nlayer = 4
d = 82.5e-3

EILP43 4 layer PSSP geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,2,2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [5.2661e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = bot
nlayer = 4
d = 82.5e-3

EILP43 4 layer SPSP geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [2,1,2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [5.2661e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = bot
nlayer = 4
d = 82.5e-3

EILP43 4 layer SSPP geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [2,2, 1,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [5.2661e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = bot
nlayer = 4
d = 82.5e-3

EILP43 4 layer SPPS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [2,1,1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [5.2661e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = bot
nlayer = 4
d = 82.5e-3

EILP43 8 layer PSPSPSPS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,3,1,3,2,3,2,3]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,5,1,1,5,5,1,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [4.50406e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,11.65e-3,9.65e-3,9.65e-3,11.65e-3,11.65e-3]
x = top
nlayer = 8
d = 82.5e-3

EILP43 8 layer PPSSPPSS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,1,3,3,2,2,3,3]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,5,1,1,5,5,1,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [4.50406e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,11.65e-3,9.65e-3,9.65e-3,11.65e-3,11.65e-3]
x = top
nlayer = 8
d = 82.5e-3

EILP43 8 layer PSSPPSSP geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,3,3,1,2,3,3,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,5,1,1,5,5,1,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [4.50406e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,11.65e-3,9.65e-3,9.65e-3,11.65e-3,11.65e-3]
x = top
nlayer = 8
d = 82.5e-3

EILP43 8 layer SPSPSPSP geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [3,1,3,1,3,2,3,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,5,1,1,5,5,1,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [4.50406e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,11.65e-3,9.65e-3,9.65e-3,11.65e-3,11.65e-3]
x = top
nlayer = 8
d = 82.5e-3

EILP43 8 layer SSPPSSPP geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [3,3, 1,1,3,3,2,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,5,1,1,5,5,1,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [4.50406e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,11.65e-3,9.65e-3,9.65e-3,11.65e-3,11.65e-3]
x = top
nlayer = 8
d = 82.5e-3

EILP43 8 layer SPPSSPPS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [3,1,1,3,3,2,2,3]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,5,1,1,5,5,1,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [4.50406e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,11.65e-3,9.65e-3,9.65e-3,11.65e-3,11.65e-3]
x = top
nlayer = 8
d = 82.5e-3

EILP43 9 layer SPSPSPSPS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [3,1,3,1,3,2,3,2,3]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 3
h = [127e-6, 140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,5,1,5,1,5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [3.50406e-3,1e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,1]
gb = 0
w = [9.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = top
nlayer = 9
d = 82.5e-3

EILP43 12 layer PSPSPSPSPSPS geometry
Ac = 229e-6
gt = 6.2806e-4
lindex = [1,5,1,5,2,5,2,5,3,5,3,5,4,5,4,5]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 5
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [5,1,5,1,5,1,5,1,5,1,5,1,5,1,5,1]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.98006e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [0,0,0,0,1]
gb = 0
w = [9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3]
x = top
nlayer = 16
d = 82.5e-3

EILP43 12 layer SPSPSPSPSPSP geometry

Ac = 229e-6
gt = 6.2806e-4
lindex = [5,1,5,1,5,2,5,2,5,3,5,3,5,4,5,4]
mus = [1.2566e-6,1.2566e-6]
mur = 1030
nwinding = 5
h = [140e-6,140e-6]
f = 500000
m = [1,5,1,5,1,5,1,5,1,5,1,5,1,5,1,5]
c = 4.1e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.98006e-3,50.5e-6]
wstyle = [0,0,0,0,1]
gb = 0
w = [11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3,11.65e-3,9.65e-3]
x = top
nlayer = 16
d = 82.5e-3

B.2 Coupled Inductor

EILP18 2 layer PS geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6]
f = 500000
m = [1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7]
s = [2.719e-3,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3]
x =
nlayer = 2
d = 38e-3

EILP18 2 layer SP geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6]
f = 500000
m = [1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7]
s = [2.719e-3,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3]
x =
nlayer = 2
d = 38e-3

EILP18 4 layer PSPS geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [1,2,1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.338e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3]
x =
nlayer = 4
d = 38e-3

EILP18 4 layer PPSS geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [1,1,2,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.338e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3]
x =
nlayer = 4
d = 38e-3

EILP18 4 layer PSSP geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [1,2,2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.338e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3]
x =
nlayer = 4
d = 38e-3

EILP18 4 layer SPSP geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [2,1,2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.338e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3]
x =
nlayer = 4
d = 38e-3

EILP18 4 layer SSPP geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [2,2,1,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.338e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3]
x =
nlayer = 4
d = 38e-3

EILP18 4 layer SPPS geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [2,1,1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 860
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [2.338e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3]
x =
nlayer = 4
d = 38e-3

EILP18 6 layer PSPSPS geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [1,2,1,2,1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 2100
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [1.9176e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3,5e-3,5e-3]
nlayer = 6
d = 38e-3

EILP18 6 layer SPSPSP geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [2,1,2,1,2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 2100
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [1.9176e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3,5e-3,5e-3]
nlayer = 6
d = 38e-3

EILP18 8 layer PSPSPSPS geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [1,2,1,2,1,2,1,2]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 2100
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1,1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [1.5757e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3,5e-3,5e-3,5e-3,5e-3,5e-3]
nlayer = 8
d = 38e-3

EILP18 8 layer SPSPSPSP geometry
Ac = 39.5e-6
gt = 1.1e-3
lindex = [2,1,2,1,2,1,2,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 2100
nwinding = 2
h = [140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1,1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [1.5757e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1,1]
gb = 0
w = [5e-3,5e-3,5e-3,5e-3,5e-3,5e-3,5e-3,5e-3,5e-3]
nlayer = 8
d = 38e-3

B.3 Resonant Inductor

ER23 1 layer geometry
Ac = 50.3e-6
gt = 5.3881e-4
lindex = [1]
mus = [1.2566e-6,1.2566e-6]
mur = 1100
nwinding = 1
h = [140e-6]
f = 500000
m = [1]
c = 2e-3
sigmac = [3.5714e7]
s = [1.8634e-3,50.5e-6]
wstyle = [1]
gb = 0
w = [6e-3]
x =
nlayer = 1
d = 44.2965e-3

ER23 2 layer geometry
Ac = 50.3e-6
gt = 5.3881e-4
lindex = [1,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1100
nwinding = 1
h = [140e-6,140e-6]
f = 500000
m = [1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7]
s = [1.6729e-3,50.5e-6,50.5e-6]
wstyle = [1]
gb = 0
w = [6e-3,6e-6]
x =
nlayer = 2
d = 44.2965e-3

ER23 3 layer geometry
Ac = 50.3e-6
gt = 5.3881e-4
lindex = [1,1,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1100
nwinding = 1
h = [140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7]
s = [1.4824e-3,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1]
gb = 0
w = [6e-3,6e-3,6e-3]
x =
nlayer = 3
d = 44.2965e-3

ER23 4 layer geometry
Ac = 50.3e-6
gt = 5.3881e-4
lindex = [1,1,1,1]
mus = [1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6,1.2566e-6]
mur = 1100
nwinding = 1
h = [140e-6,140e-6,140e-6,140e-6]
f = 500000
m = [1,1,1,1]
c = 2e-3
sigmac = [3.5714e7,3.5714e7,3.5714e7,3.5714e7]
s = [1.2919e-3,50.5e-6,50.5e-6,50.5e-6,50.5e-6]
wstyle = [1]
gb = 0
w = [6e-3,6e-3,6e-3,6e-3]
x =
nlayer = 4
d = 44.2965e-3

Appendix C LTSpice Simulation Files

This Appendix contains multiple simulation files used to simulate the theory and practical converter designs. For each simulation, there will be an image of the schematic as captured by LTSpice as well as a netlist for full details since some information may not be visible in the schematic. This Appendix will also contain supporting material for some of the parasitic and operating values used in the simulations. There are a total of nine simulation files. The first simulates the ICN converter when operated under ideal conditions in fundamental mode. The second simulates the ICN converter in fundamental mode as it was implemented (e.g., with more practical components and parasitic elements). The third simulates the ICN converter when operated under ideal conditions in variable frequency multiplier (VFX) mode. The fourth simulates the ICN converter in VFX mode as it was implemented. The next four simulations compare various active bridge converter topologies when operated at 500 kHz to get a general understanding of their behaviors across power. The fifth simulation is for a regular DAB converter which uses a full bridge inverter. The sixth simulation is for a single stacked active bridge converter which uses a stacked full bridge inverter. The seventh simulation is for the proposed double stacked active bridge converter in normal mode and the eighth simulation is for low-power mode. The ninth simulation is for the proposed double stacked active bridge converter modeling the final prototype where the switching frequency is at 175 kHz, the total primary-referred energy transfer inductance is 32 μH but distributed across the two primaries and single secondary.

C.1 ICN Converter Simulations in Fundamental Mode

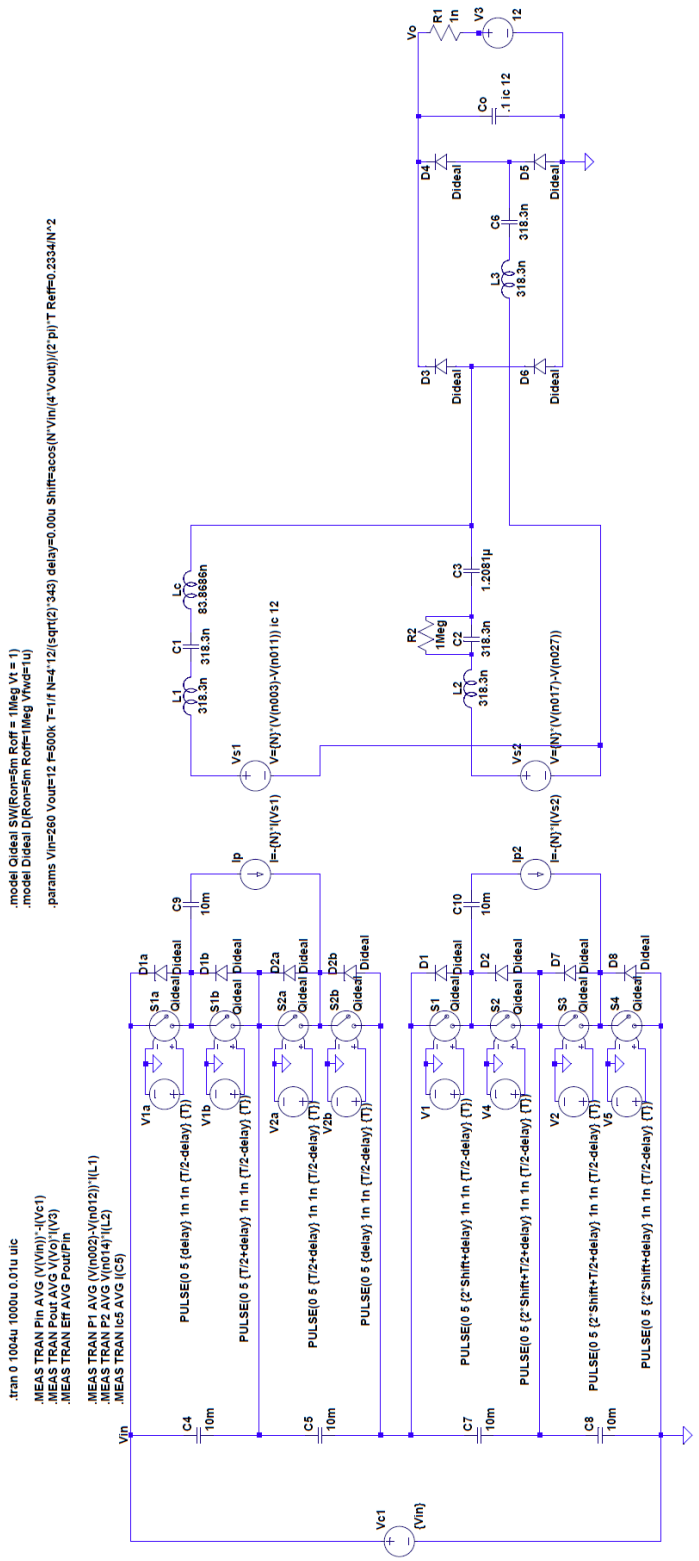


Figure C-1: Simulation schematic of the ICN converter when operated under ideal conditions in fundamental mode.

Netlist for Figure C-1

```
S1a Vin N002 N001 0 Qideal
S1b N002 N009 N008 0 Qideal
S2a N009 N011 N010 0 Qideal
S2b N011 N014 N013 0 Qideal
V1a N001 0 PULSE(0 5 {delay} 1n 1n {T/2-delay} {T})
V2a N010 0 PULSE(0 5 {T/2+delay} 1n 1n {T/2-delay} {T})
V1b N008 0 PULSE(0 5 {T/2+delay} 1n 1n {T/2-delay} {T})
V2b N013 0 PULSE(0 5 {delay} 1n 1n {T/2-delay} {T})
L1 N004 N005 318.3n Rser=0
L2 N018 N019 318.3n Rser=0
C1 N005 N006 318.3n Rser=0
C2 N019 N020 318.3n Rser=0
Lc N006 N007 83.8686n Rser=0
D3 N007 Vo Dideal
D4 N023 Vo Dideal
D5 0 N023 Dideal
D6 0 N007 Dideal
Co Vo 0 .1 ic 12
V3 N021 0 12
Vc1 Vin 0 {Vin}
D1a N002 Vin Dideal
D1b N009 N002 Dideal
D2a N011 N009 Dideal
D2b N014 N011 Dideal
B§Ip N003 N011 I=-{N}*I(Vs1)
R1 Vo N021 1n
C3 N007 N020 1.2081µ
R2 N020 N019 1Meg
C4 Vin N009 10m
C5 N009 N014 10m
S1 N014 N016 N015 0 Qideal
S2 N016 N025 N024 0 Qideal
S3 N025 N027 N026 0 Qideal
S4 N027 0 N028 0 Qideal
V1 N015 0 PULSE(0 5 {2*Shift+delay} 1n 1n {T/2-delay} {T})
V2 N026 0 PULSE(0 5 {2*Shift+T/2+delay} 1n 1n {T/2-delay} {T})
V4 N024 0 PULSE(0 5 {2*Shift+T/2+delay} 1n 1n {T/2-delay} {T})
V5 N028 0 PULSE(0 5 {2*Shift+delay} 1n 1n {T/2-delay} {T})
D1 N016 N014 Dideal
D2 N025 N016 Dideal
D7 N027 N025 Dideal
D8 0 N027 Dideal
C7 N014 N025 10m
C8 N025 0 10m
C9 N003 N002 10m
C10 N017 N016 10m
B§Ip2 N017 N027 I=-{N}*I(Vs2)
B§Vs1 N004 N012 V={N}*(V(n003)-V(n011)) ic 12
B§Vs2 N018 N012 V={N}*(V(n017)-V(n027))
C6 N023 N022 318.3n
L3 N012 N022 318.3n
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
```

```
.model Qideal SW(Ron=5m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.tran 0 1004u 1000u 0.01u uic
.params Vin=260 Vout=12 f=500k T=1/f N=4*12/(sqrt(2)*343) delay=0.00u
Shift=acos(N*Vin/(4*Vout))/(2*pi)*T Reff=0.2334/N^2
.MEAS TRAN Pin AVG (V(Vin))*-I(Vc1)
.MEAS TRAN Pout AVG V(Vo)*I(V3)
.MEAS TRAN Eff AVG Pout/Pin

.MEAS TRAN P1 AVG (V(n002)-V(n012))*I(L1)
.MEAS TRAN P2 AVG V(n014)*I(L2)
.MEAS TRAN Ic5 AVG I(C5)
.backanno
.end
```

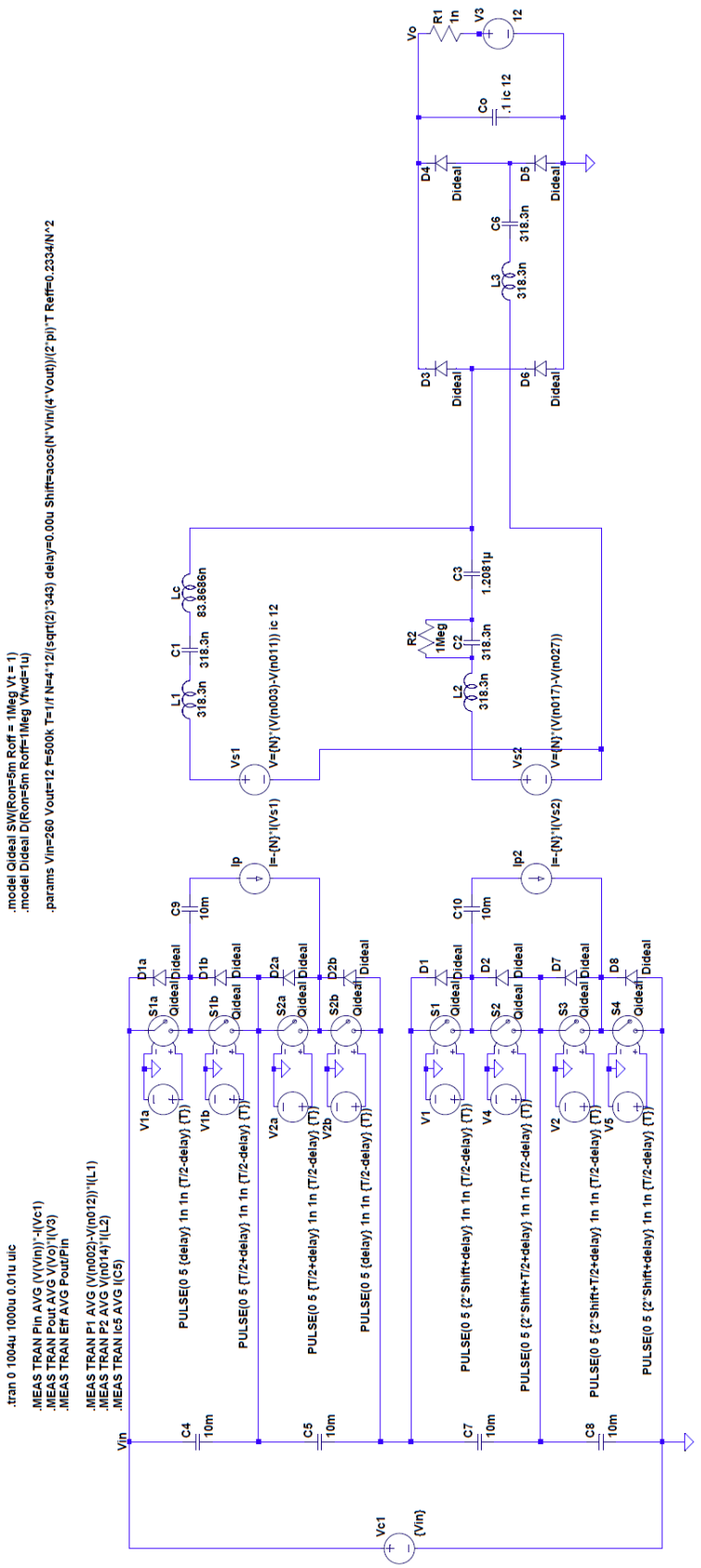


Figure C-2: Simulation schematic of the ICN converter modeling the final prototype in fundamental mode.

Netlist for Figure C-2

```
Cc N020 N007 .630µ Rser=0.128m
L2 N019 N020 130n Rser=2m
C2 N016 N015 3.3µ ic {-Vin/4} Rser=3.4m
R1 N015 N016 1Meg
D1 Vdiode Vo EPC2023
D2 Vref Vo EPC2023
D3 0 Vdiode EPC2023
D4 0 Vref EPC2023
CB3 Vo 0 340µ ic 12
R2 Vo N013 1n
V3 N013 0 {Vout}
S1 N002 Vin1 N001 0 Qideal
S2 Vin2 N002 N005 0 Qideal
V4 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V5 N005 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
DS1 N002 Vin1 Dideal
DS2 Vin2 N002 Dideal
S3 N009 Vin2 N008 0 Qideal
V1 N008 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
DS3 N009 Vin2 Dideal
DS4 Vin3 N009 Dideal
S5 N015 Vin3 N014 0 Qideal
S6 Vin4 N015 N018 0 Qideal
V8 N014 0 PULSE(0 5 {2*Shift+delay} 5n 5n {T/2-delay} {T})
V9 N018 0 PULSE(0 5 {2*Shift+T/2+delay} 5n 5n {T/2-delay} {T})
DS5 N015 Vin3 Dideal
DS6 Vin4 N015 Dideal
S7 N021 Vin4 N022 0 Qideal
S8 0 N021 N023 0 Qideal
V10 N022 0 PULSE(0 5 {2*Shift+T/2+delay} 5n 5n {T/2-delay} {T})
V11 N023 0 PULSE(0 5 {2*Shift+delay} 5n 5n {T/2-delay} {T})
DS7 N021 Vin4 Dideal
DS8 0 N021 Dideal
S4 Vin3 N009 N010 0 Qideal
V2 N010 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
Vin Vin1 0 {Vin}
CB1 N003 N002 3.3µ ic {-Vin/4} Rser=3.4m
R5 N003 N002 1Meg
Cin1 Vin1 Vin2 200µ ic {Vin/4} Rser=3.4m
Cin2 Vin2 Vin3 200µ ic {Vin/4} Rser=3.4m
Cin3 Vin3 Vin4 200µ ic {Vin/4} Rser=3.4m
Cin4 Vin4 0 200µ ic {Vin/4} Rser=3.4m
R6 Vin1 Vin2 1Meg
R7 Vin2 Vin3 1Meg
R8 Vin3 Vin4 1Meg
R9 Vin4 0 1Meg
L6 N009 N004 42µ Rser=187.5m
L7 Vref Vtop 420n Rser=1.875m
L4 N021 N017 42µ Rser=187.5m
L5 Vref Vbot 420n Rser=1.875m
L1 N007 N006 46n Rser=2m
L3 N011 N007 46n Rser=3m
C3 N012 N011 1.13µ Rser=0.148m
R10 N011 N012 1Meg
CS1 Vin1 N002 400p
```

```
CS2 N002 Vin2 400p
CS3 Vin2 N009 400p
CS4 N009 Vin3 400p
CS5 Vin3 N015 500p
CS6 N015 Vin4 500p
CS7 Vin4 N021 500p
CS8 N021 0 500p
Rtop N006 Vtop 2m
Rbottom N019 Vbot 1m
Rcommon Vdiode N012 10.25m
Rinvbottom N017 N016 6m
Rinvtop N004 N003 5m
R3 N004 N009 18123.18
R4 N017 N021 15278.5
R11 N020 N019 254.0534
R12 N007 N006 500
R13 N011 N007 500
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.tran 0 10505.5033206u 10501.5232211u 0.01u uic
.params Vin=260 Vout=12 f=502.5k T=1/f N=4*12/(sqrt(2)*338) delay=0.09u
Shift=acos(N*Vin/(4*Vout))*T/(2*pi)
.model Qideal SW(Ron=40m Roff=1Meg Vt=1)
.model Dideal D(Ron=1n Roff=1Meg Vfwd=2)
.model EPC2023 D(Ron = 1.3m Roff = 1Meg Vfwd = 1n)
.MEAS TRAN Pin AVG -(V(Vin1)*I(Vin))
.MEAS TRAN Pout AVG V(Vo)*I(V3)
.MEAS TRAN Eff AVG Pout/Pin
K1 L6 L7 0.998
K2 L4 L5 0.998
K3 L1 L3 0.988
.backanno
.end
```

Figure C-2 incorporates multiple loss mechanisms. This section briefly describes how the loss parameters were determined. The inverter switches used were EPC2010. The datasheet lists the typical on-resistance as 18 mΩ and the maximum on-resistance as 25 mΩ. The temperature normalization factor for 100 °C is estimated to be around 1.6 so the total on-resistance used in the simulation is 40 mΩ. The capacitance was determined from the averaged integral of the output capacitance up to the applied voltage level. A similar process was done for the rectifier switches. The EPC2023 datasheet lists the typical on-resistance as 1 mΩ, max on-resistance as 1.3 mΩ, and the temperature normalization factor for 100 °C is around 2.0. The estimated on-resistance for each device is 2.6 mΩ but because we are paralleling 2 devices, the resistance goes down to 1.3 mΩ.

There are multiple capacitors in the network. The main capacitors used and their parasitic values are shown in Table C-1. From this, the input capacitors and blocking capacitors are estimated to have a series resistance of 3.4 mΩ (each is a parallel combination of two 250V capacitors). The capacitors at the output of the bottom transformer are estimated to have a combined resistance of 0.128 mΩ (parallel combination of five 0.22 μF capacitors and two 0.015 μF capacitors). The output resonant tank capacitors (parallel combination of four 0.15 μF and two 0.015 μF capacitors) have a combined resistance of 0.146 mΩ.

There are several sources of trace resistances. A bare PCB was taken with appropriate terminals shorted and impedance measurements were made at various ports. The trace paths and their measured values are shown in Figure C-3. In the final prototype, some foil connections were made in place of the PCB traces to shorten the paths. R_{top} and R_{bottom} of Figure C-3 were reduced to 2 mΩ and 1 mΩ, respectively to account for this shortened connection.

The last major source of loss was the magnetic components. Each of the three components has two sources of loss – winding resistance and core loss. For the transformer windings, the secondary

Table C-1: ICN Converter Capacitor List and Parameter Values at 500 kHz

Description	Part Number	ESR (Ω)	Impedance (Ω)	Capacitance (nF)
CAP CER 1UF 50V 10% X7R 1812	C4532X7R1H105K160KA	8.16E-03	3.16E-01	1.00E+03
CAP CER 3.3UF 250V 20% X7T SMD	CKG57NX7T2E335M500JH	6.80E-03	9.06E-02	3.50E+03
CAP CER 0.22UF 50V 5% NP0 1812	C4532NP01H224J320KA	1.17E-03	1.42E+00	2.24E+02
CAP CER 0.015UF 630V 5% NP0 1210	C3225C0G2J153J160AA	5.66E-04	2.07E+01	1.51E+01
CAP CER 0.15UF 50V 5% C0G 1812	C4532C0G1H154J250KA	1.24E-03	2.09E+00	1.52E+02

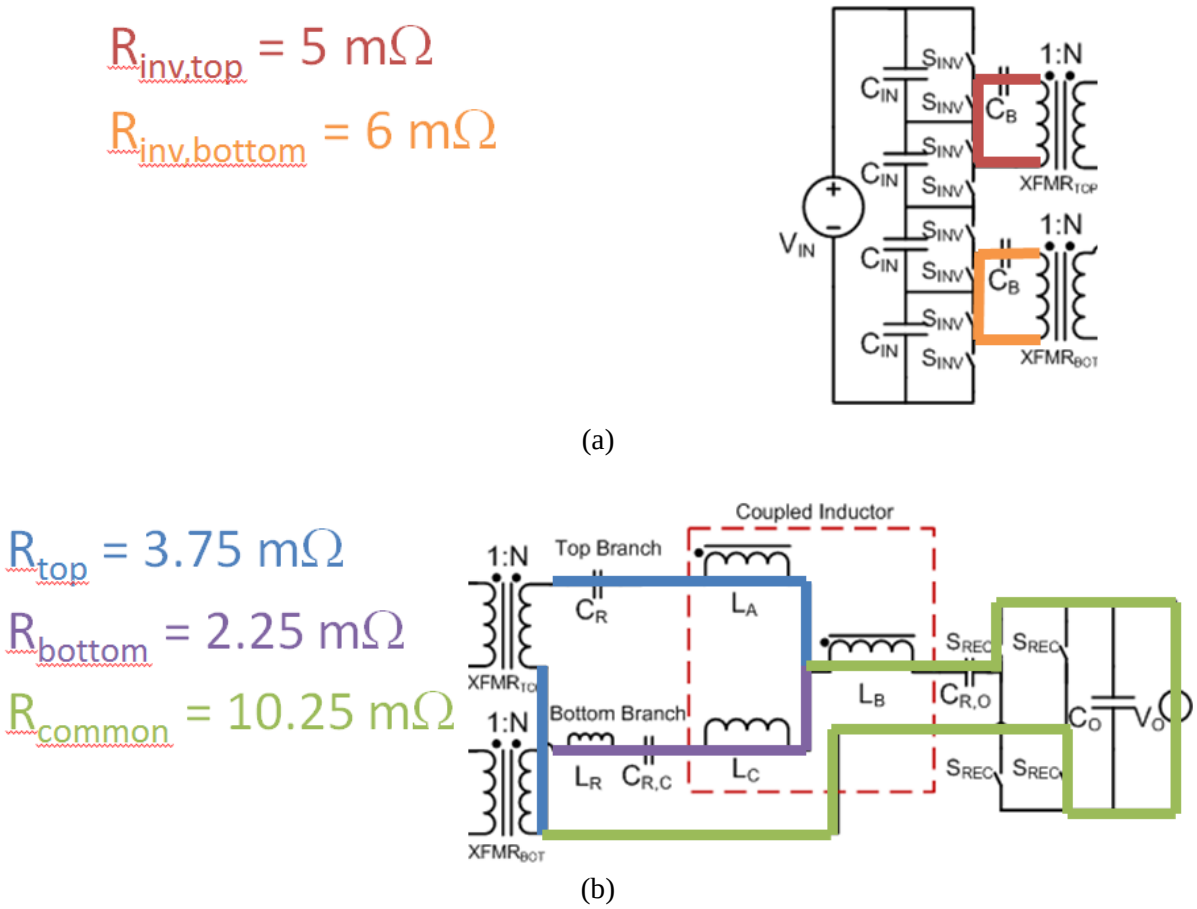


Figure C-3: Trace resistances for the (a) inverter and (b) output stage and the paths that were considered in the measurements.

winding was shorted and the primary winding resistance was measured to be 187.5 mΩ. (Note this was done without the core so proximity effect may not be accounted for.) The low resistance of the secondary was difficult to measure, but it is approximated to be the same as the primary resistance divided by the turns squared which is 1.875 mΩ. For the coupled inductor and the resonant inductor, their ports were measured, this time with a core. In the case of the coupled inductor, the other winding would be open circuited. This resistance was also on the order of 2-3 mΩ for each winding. The core loss is approximated by a parallel resistor in the schematic. The resistance value is calculated based on the expected voltage across the component squared divided by the expected core loss (determined through the MATLAB script of Appendix A).

C.2 ICN Converter Simulations in VFX Mode

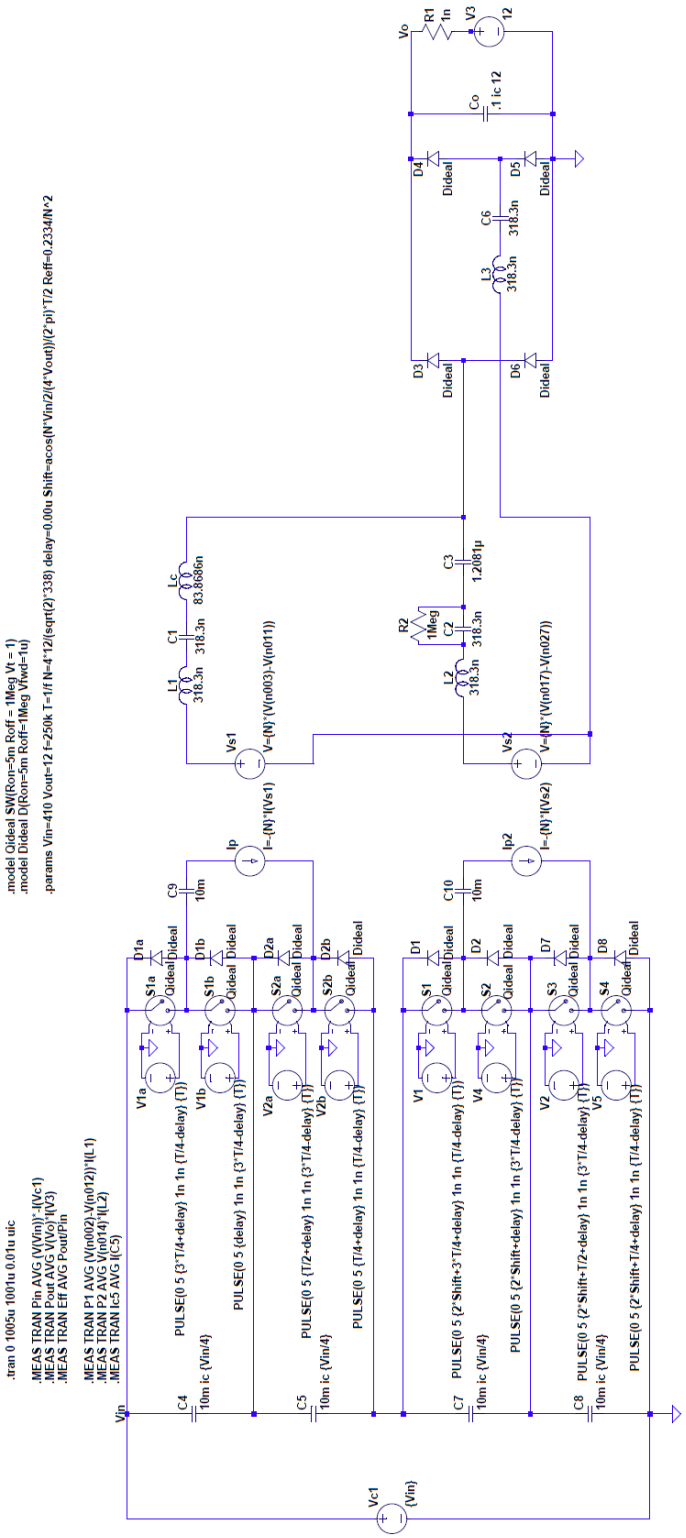


Figure C-4: Simulation schematic of the ICN converter when operated under ideal conditions in VFX mode.

Netlist for Figure C-4

```
S1a Vin N002 N001 0 Qideal
S1b N002 N009 N008 0 Qideal
S2a N009 N011 N010 0 Qideal
S2b N011 N014 N013 0 Qideal
V1a N001 0 PULSE(0 5 {3*T/4+delay} 1n 1n {T/4-delay} {T})
V2a N010 0 PULSE(0 5 {T/2+delay} 1n 1n {3*T/4-delay} {T})
V1b N008 0 PULSE(0 5 {delay} 1n 1n {3*T/4-delay} {T})
V2b N013 0 PULSE(0 5 {T/4+delay} 1n 1n {T/4-delay} {T})
L1 N004 N005 318.3n Rser=0
L2 N018 N019 318.3n Rser=0
C1 N005 N006 318.3n Rser=0
C2 N019 N020 318.3n Rser=0
Lc N006 N007 83.8686n Rser=0
D3 N007 Vo Dideal
D4 N023 Vo Dideal
D5 0 N023 Dideal
D6 0 N007 Dideal
Co Vo 0 .1 ic 12
V3 N021 0 12
Vc1 Vin 0 {Vin}
D1a N002 Vin Dideal
D1b N009 N002 Dideal
D2a N011 N009 Dideal
D2b N014 N011 Dideal
B§Ip N003 N011 I=-{N}*I(Vs1)
R1 Vo N021 1n
C3 N007 N020 1.2081µ
R2 N020 N019 1Meg
C4 Vin N009 10m ic {Vin/4}
C5 N009 N014 10m ic {Vin/4}
S1 N014 N016 N015 0 Qideal
S2 N016 N025 N024 0 Qideal
S3 N025 N027 N026 0 Qideal
S4 N027 0 N028 0 Qideal
V1 N015 0 PULSE(0 5 {2*Shift+3*T/4+delay} 1n 1n {T/4-delay} {T})
V2 N026 0 PULSE(0 5 {2*Shift+T/2+delay} 1n 1n {3*T/4-delay} {T})
V4 N024 0 PULSE(0 5 {2*Shift+delay} 1n 1n {3*T/4-delay} {T})
V5 N028 0 PULSE(0 5 {2*Shift+T/4+delay} 1n 1n {T/4-delay} {T})
D1 N016 N014 Dideal
D2 N025 N016 Dideal
D7 N027 N025 Dideal
D8 0 N027 Dideal
C7 N014 N025 10m ic {Vin/4}
C8 N025 0 10m ic {Vin/4}
C9 N003 N002 10m
C10 N017 N016 10m
B§Ip2 N017 N027 I=-{N}*I(Vs2)
B§Vs1 N004 N012 V={N}*(V(n003)-V(n011))
B§Vs2 N018 N012 V={N}*(V(n017)-V(n027))
C6 N023 N022 318.3n
L3 N012 N022 318.3n
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.model Qideal SW(Ron=5m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
```

```
.tran 0 1005u 1001u 0.01u uic
.params Vin=410 Vout=12 f=250k T=1/f N=4*12/(sqrt(2)*338) delay=0.00u
Shift=acos(N*Vin/2/(4*Vout))/(2*pi)*T/2 Reff=0.2334/N^2
.MEAS TRAN Pin AVG (V(Vin))*-I(Vc1)
.MEAS TRAN Pout AVG V(Vo)*I(V3)
.MEAS TRAN Eff AVG Pout/Pin

.MEAS TRAN P1 AVG (V(n002)-V(n012))*I(L1)
.MEAS TRAN P2 AVG V(n014)*I(L2)
.MEAS TRAN Ic5 AVG I(C5)
.backanno
.end
```

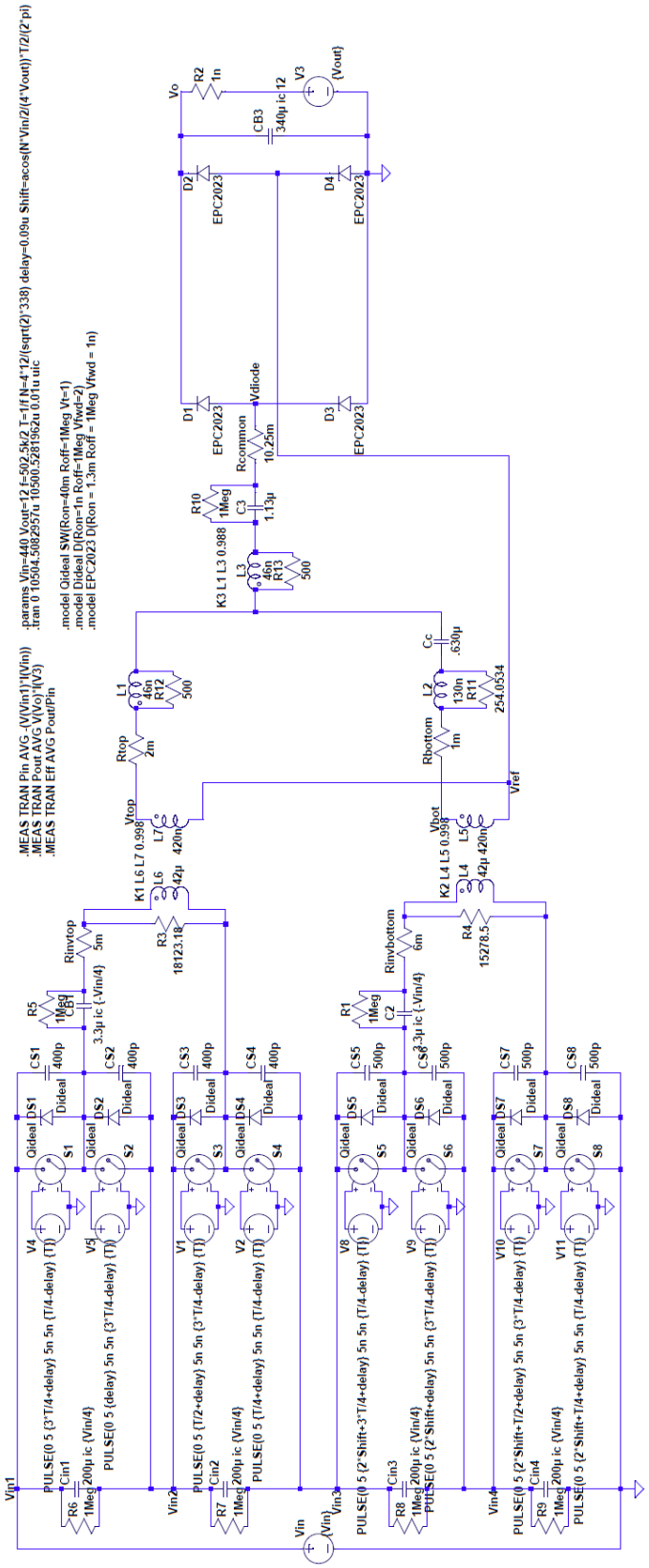


Figure C-5: Simulation schematic of the ICN converter modeling the final prototype in VFX mode.

Netlist for Figure C-5

```
Cc N020 N007 .630µ Rser=0.128m
L2 N019 N020 130n Rser=2m
C2 N016 N015 3.3µ ic {-Vin/4} Rser=3.4m
R1 N015 N016 1Meg
D1 Vdiode Vo EPC2023
D2 Vref Vo EPC2023
D3 0 Vdiode EPC2023
D4 0 Vref EPC2023
CB3 Vo 0 340µ ic 12
R2 Vo N013 1n
V3 N013 0 {Vout}
S1 N002 Vin1 N001 0 Qideal
S2 Vin2 N002 N005 0 Qideal
V4 N001 0 PULSE(0 5 {3*T/4+delay} 5n 5n {T/4-delay} {T})
V5 N005 0 PULSE(0 5 {delay} 5n 5n {3*T/4-delay} {T})
DS1 N002 Vin1 Dideal
DS2 Vin2 N002 Dideal
S3 N009 Vin2 N008 0 Qideal
V1 N008 0 PULSE(0 5 {T/2+delay} 5n 5n {3*T/4-delay} {T})
DS3 N009 Vin2 Dideal
DS4 Vin3 N009 Dideal
S5 N015 Vin3 N014 0 Qideal
S6 Vin4 N015 N018 0 Qideal
V8 N014 0 PULSE(0 5 {2*Shift+3*T/4+delay} 5n 5n {T/4-delay} {T})
V9 N018 0 PULSE(0 5 {2*Shift+delay} 5n 5n {3*T/4-delay} {T})
DS5 N015 Vin3 Dideal
DS6 Vin4 N015 Dideal
S7 N021 Vin4 N022 0 Qideal
S8 0 N021 N023 0 Qideal
V10 N022 0 PULSE(0 5 {2*Shift+T/2+delay} 5n 5n {3*T/4-delay} {T})
V11 N023 0 PULSE(0 5 {2*Shift+T/4+delay} 5n 5n {T/4-delay} {T})
DS7 N021 Vin4 Dideal
DS8 0 N021 Dideal
S4 Vin3 N009 N010 0 Qideal
V2 N010 0 PULSE(0 5 {T/4+delay} 5n 5n {T/4-delay} {T})
Vin Vin1 0 {Vin}
CB1 N003 N002 3.3µ ic {-Vin/4} Rser=3.4m
R5 N003 N002 1Meg
Cin1 Vin1 Vin2 200µ ic {Vin/4} Rser=3.4m
Cin2 Vin2 Vin3 200µ ic {Vin/4} Rser=3.4m
Cin3 Vin3 Vin4 200µ ic {Vin/4} Rser=3.4m
Cin4 Vin4 0 200µ ic {Vin/4} Rser=3.4m
R6 Vin1 Vin2 1Meg
R7 Vin2 Vin3 1Meg
R8 Vin3 Vin4 1Meg
R9 Vin4 0 1Meg
L6 N009 N004 42µ Rser=187.5m
L7 Vref Vtop 420n Rser=1.875m
L4 N021 N017 42µ Rser=187.5m
L5 Vref Vbot 420n Rser=1.875m
L1 N007 N006 46n Rser=2m
L3 N011 N007 46n Rser=3m
C3 N012 N011 1.13µ Rser=0.148m
R10 N011 N012 1Meg
CS1 Vin1 N002 400p
CS2 N002 Vin2 400p
```

```
CS3 Vin2 N009 400p
CS4 N009 Vin3 400p
CS5 Vin3 N015 500p
CS6 N015 Vin4 500p
CS7 Vin4 N021 500p
CS8 N021 0 500p
Rtop N006 Vtop 2m
Rbottom N019 Vbot 1m
Rcommon Vdiode N012 10.25m
Rinvbottom N017 N016 6m
Rinvtop N004 N003 5m
R3 N004 N009 18123.18
R4 N017 N021 15278.5
R11 N020 N019 254.0534
R12 N007 N006 500
R13 N011 N007 500
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.tran 0 10504.5082957u 10500.5281962u 0.01u uic
.params Vin=440 Vout=12 f=502.5k/2 T=1/f N=4*12/(sqrt(2)*338) delay=0.09u
Shift=acos(N*Vin/2/(4*Vout))*T/2/(2*pi)
.model Qideal SW(Ron=40m Roff=1Meg Vt=1)
.model Dideal D(Ron=1n Roff=1Meg Vfwd=2)
.model EPC2023 D(Ron = 1.3m Roff = 1Meg Vfwd = 1n)
.MEAS TRAN Pin AVG -(V(Vin1)*I(Vin))
.MEAS TRAN Pout AVG V(Vo)*I(V3)
.MEAS TRAN Eff AVG Pout/Pin
K1 L6 L7 0.998
K2 L4 L5 0.998
K3 L1 L3 0.988
.backanno
.end
```

C.3 Active Bridge Converter Simulations

This section contains several simulation files to understand the behavior of the various active bridge topologies discussed in Chapter 4 and Chapter 5. For the first four simulations, the nominal operating point was an input voltage of 380 V, an output voltage of 12 V, and an output power of 400 W. The operating frequency is 500 kHz and the primary-referred energy transfer inductance was chosen so that 400 W would be delivered at a phase shift that is 5% of the switching period. The transformer turns ratio was chosen so that the current into the primary would be a flattop trapezoidal waveform. For the full bridge DAB converter, this was an inductance of 32.832 μH and a transformer turns ratio of 32:1. For the single stacked active bridge converter, this was an inductance of 8.208 μH and a transformer turns ratio of 16:1. For the double stacked active bridge converter, this was an inductance of 4.104 μH on each primary and a transformer turns ratio of 16:1 for each transformer. There is a resistor in parallel with the transformer primary to model core losses. The total core loss should be constant across all designs because the secondary voltage is the same. At 500 kHz, the core loss was initially calculated as 1.29 W based on (5.2) and (5.3) using the parameters listed in the MATLAB code of Appendix A. The value of the core resistance is calculated based on the voltage across the primary squared divided by the core loss. For the full bridge DAB converter, the resistance is 111,832 Ω, for the single stacked design, it is 27,958 Ω and for the double stacked design, each transformer has a resistance of 14,000 Ω.

The devices used were GaN devices that were commercially available at the time and had sufficient safety margin on their rating. Therefore, the full bridge DAB converter used parameters for the GaNSystems GS66516T 650 V device with an on-state resistance of 70 mΩ and an off-state capacitance of 134 pF. The single stacked active bridge converter used parameters for EPC's only 300V device, the EPC2025 with an on-state resistance of 140 mΩ and an off-state capacitance of 106.25 pF. Both the EPC 2012C (with an on-state resistance of 105 mΩ and an off-state capacitance of 102.5 pF) and the EPC 2019 (with an on-state resistance of 55 mΩ and an off-state capacitance of 185 pF) were simulated for the double stacked active bridge converter. The EPC 2012C is EPC's lowest capacitance 200V device with the EPC2019 having the second lowest capacitance. All rectifier devices used EPC's lowest voltage device, the 30V EPC2023, with on-state resistance of 2.6 mΩ and off-state capacitance of 500 pF.

For the first four simulations, the phase shift was adjusted to modulate the output power. Dead-time was roughly minimized to reduce body diode conduction but increased at low powers to help achieve ZVS. The values for the simulations can be found in Table C-2 through Table C-6.

The last simulation is of the experimental prototype where the 32 μH of energy transfer inductance is distributed across the primary and secondary windings. EPC2012C and EPC2023 are used. The input voltage is varied from 260V to 410V. Core loss is calculated for each operating point. Simulations were run for a turns ratio of 16 and 14. Parameters can be found in Table C-7 and Table C-8.

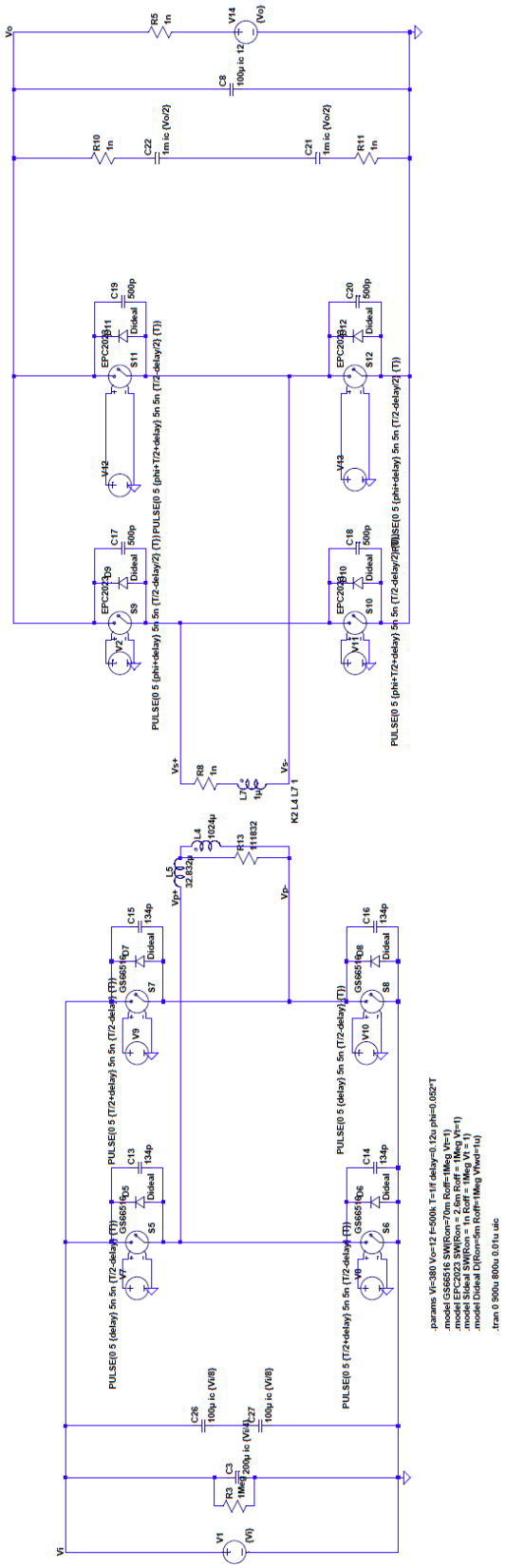


Figure C-6: Simulation schematic of a regular DAB operated at 500 kHz.

Netlist for Figure C-6

```
V1 Vi 0 {Vi}
V7 N003 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N015 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 Vp+ Vi N003 0 GS66516
S6 0 Vp+ N015 0 GS66516
S7 Vp- Vi N004 0 GS66516
S8 0 Vp- N013 0 GS66516
V9 N004 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N013 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 Vi 0 200µ ic {Vi/4}
L4 Vp- N006 1024µ Rser=114.6m
V2 N001 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
V11 N011 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
S9 Vs+ Vo N001 0 EPC2023
S10 0 Vs+ N011 0 EPC2023
V12 N002 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
V13 N012 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
S11 Vs- Vo N002 0 EPC2023
S12 0 Vs- N012 0 EPC2023
C8 Vo 0 100µ ic 12
D5 Vp+ Vi Dideal
C13 Vi Vp+ 134p
D6 0 Vp+ Dideal
C14 Vp+ 0 134p
D7 Vp- Vi Dideal
C15 Vi Vp- 134p
D8 0 Vp- Dideal
C16 Vp- 0 134p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 500p
D10 0 Vs+ Dideal
C18 Vs+ 0 500p
D11 Vs- Vo Dideal
C19 Vo Vs- 500p
D12 0 Vs- Dideal
C20 Vs- 0 500p
R3 Vi 0 1Meg
R5 Vo N007 1n
L5 Vp+ N006 32.832µ
L7 Vs- N008 1µ
R8 Vs+ N008 1n
V14 N007 0 {Vo}
C22 N005 N010 1m ic {Vo/2}
C21 N010 N014 1m ic {Vo/2}
R10 Vo N005 1n
R11 N014 0 1n
C26 Vi N009 100µ ic {Vi/8}
C27 N009 0 100µ ic {Vi/8}
R13 N006 Vp- 111832
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=500k T=1/f delay=0.12u phi=0.052*T
.model GS66516 SW(Ron=70m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 2.6m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
```

```
.tran 0 900u 800u 0.01u uic
K2 L4 L7 1
.backanno
.end
```

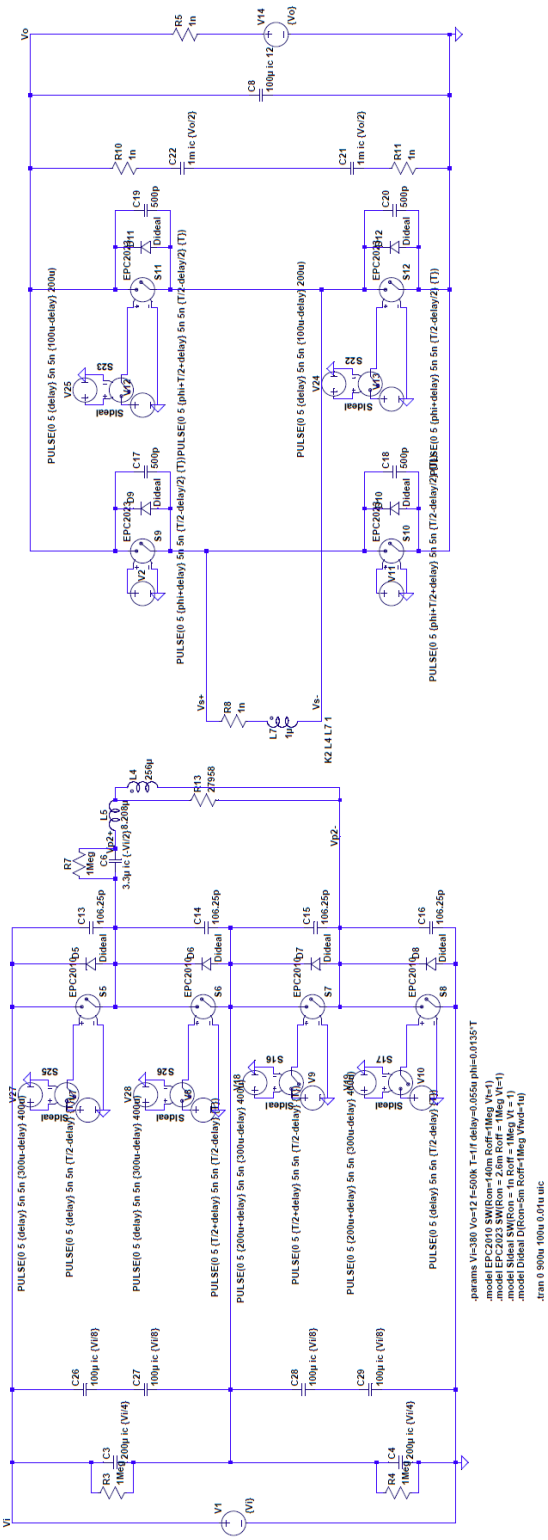


Figure C-7: Simulation schematic of a single stacked active bridge converter operated at 500 kHz.

Netlist for Figure C-7

```
V1 Vi 0 {Vi}
V7 N002 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N014 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N005 Vi N003 0 EPC2010
S6 N010 N005 N015 0 EPC2010
S7 Vp2- N010 N020 0 EPC2010
S8 0 Vp2- N030 0 EPC2010
V9 N019 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N029 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 Vi N010 200µ ic {Vi/4}
C4 N010 0 200µ ic {Vi/4}
C6 Vp2+ N005 3.3µ ic {-Vi/2}
L4 Vp2- N006 256µ Rser=114.6m
V2 N007 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
V11 N024 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N024 0 EPC2023
V12 N008 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
V13 N025 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
S11 Vs- Vo N009 0 EPC2023
S12 0 Vs- N026 0 EPC2023
C8 Vo 0 100µ ic 12
D5 N005 Vi Dideal
C13 Vi N005 106.25p
D6 N010 N005 Dideal
C14 N005 N010 106.25p
D7 Vp2- N010 Dideal
C15 N010 Vp2- 106.25p
D8 0 Vp2- Dideal
C16 Vp2- 0 106.25p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 500p
D10 0 Vs+ Dideal
C18 Vs+ 0 500p
D11 Vs- Vo Dideal
C19 Vo Vs- 500p
D12 0 Vs- Dideal
C20 Vs- 0 500p
R3 Vi N010 1Meg
R4 N010 0 1Meg
R5 Vo N016 1n
L5 Vp2+ N006 8.208µ
L7 Vs- N017 1µ
R7 N005 Vp2+ 1Meg
R8 Vs+ N017 1n
V14 N016 0 {Vo}
C22 N013 N021 1m ic {Vo/2}
C21 N021 N028 1m ic {Vo/2}
R10 Vo N013 1n
R11 N028 0 1n
C26 Vi N011 100µ ic {Vi/8}
C27 N011 N010 100µ ic {Vi/8}
C28 N010 N023 100µ ic {Vi/8}
C29 N023 0 100µ ic {Vi/8}
V18 N018 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
```

```
S16 N020 N019 N018 0 SIdeal
V19 N027 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S17 N030 N029 N027 0 SIdeal
V24 N022 0 PULSE(0 5 {delay} 5n 5n {100u-delay} 200u)
S22 N026 N025 N022 0 SIdeal
V25 N004 0 PULSE(0 5 {delay} 5n 5n {100u-delay} 200u)
S23 N009 N008 N004 0 SIdeal
V27 N001 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S25 N003 N002 N001 0 SIdeal
V28 N012 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S26 N015 N014 N012 0 SIdeal
R13 N006 Vp2- 27958
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=500k T=1/f delay=0.055u phi=0.0135*T
.model EPC2010 SW(Ron=140m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 2.6m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.tran 0 900u 100u 0.01u uic
K2 L4 L7 1
.backanno
.end
```

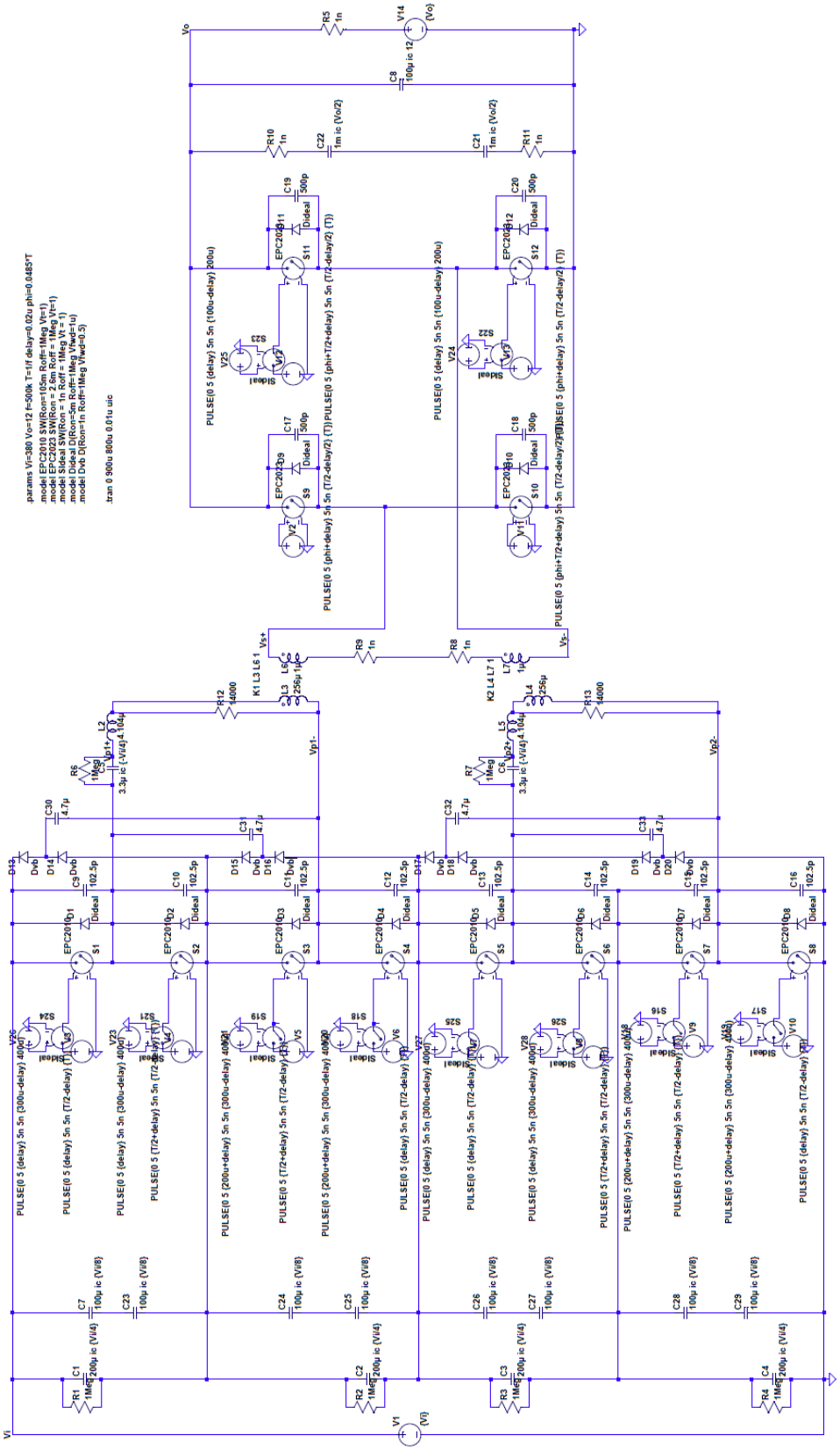


Figure C-8: Simulation schematic of the proposed double stacked active bridge converter operated at 500 kHz.

Netlist for Figure C-8

```
V1 Vi 0 {Vi}
V3 N003 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N010 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N006 Vi N004 0 EPC2010
S2 N005 N006 N011 0 EPC2010
S3 Vp1- N005 N015 0 EPC2010
S4 N026 Vp1- N024 0 EPC2010
V5 N016 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V6 N025 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C1 Vi N005 200µ ic {Vi/4}
C2 N005 N026 200µ ic {Vi/4}
V7 N031 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N045 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N039 N026 N032 0 EPC2010
S6 N042 N039 N046 0 EPC2010
S7 Vp2- N042 N051 0 EPC2010
S8 0 Vp2- N055 0 EPC2010
V9 N050 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N054 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 N026 N042 200µ ic {Vi/4}
C4 N042 0 200µ ic {Vi/4}
C5 Vp1+ N006 3.3µ ic {-Vi/4}
C6 Vp2+ N039 3.3µ ic {-Vi/4}
L3 Vp1- N007 256µ Rser=114.6m
L4 Vp2- N040 256µ Rser=114.6m
V2 N017 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
V11 N036 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
S9 Vs+ Vo N017 0 EPC2023
S10 0 Vs+ N036 0 EPC2023
V12 N018 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
V13 N037 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
S11 Vs- Vo N019 0 EPC2023
S12 0 Vs- N038 0 EPC2023
C8 Vo 0 100µ ic 12
D1 N006 Vi Dideal
C9 Vi N006 102.5p
D2 N005 N006 Dideal
C10 N006 N005 102.5p
D3 Vp1- N005 Dideal
C11 N005 Vp1- 102.5p
D4 N026 Vp1- Dideal
C12 Vp1- N026 102.5p
D5 N039 N026 Dideal
C13 N026 N039 102.5p
D6 N042 N039 Dideal
C14 N039 N042 102.5p
D7 Vp2- N042 Dideal
C15 N042 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 500p
D10 0 Vs+ Dideal
C18 Vs+ 0 500p
D11 Vs- Vo Dideal
C19 Vo Vs- 500p
```

```
D12 0 Vs- Dideal
C20 Vs- 0 500p
R1 Vi N005 1Meg
R2 N005 N026 1Meg
R3 N026 N042 1Meg
R4 N042 0 1Meg
R5 Vo N027 1n
L2 Vp1+ N007 4.104µ
L5 Vp2+ N040 4.104µ
L6 N022 Vs+ 1µ Rser=0.448m
L7 Vs- N035 1µ
R6 N006 Vp1+ 1Meg
R7 N039 Vp2+ 1Meg
R8 N029 N035 1n
R9 N022 N029 1n
V14 N027 0 {Vo}
C22 N020 N033 1m ic {Vo/2}
C21 N033 N041 1m ic {Vo/2}
R10 Vo N020 1n
R11 N041 0 1n
C7 Vi N008 100µ ic {Vi/8}
C23 N008 N005 100µ ic {Vi/8}
C24 N005 N021 100µ ic {Vi/8}
C25 N021 N026 100µ ic {Vi/8}
C26 N026 N043 100µ ic {Vi/8}
C27 N043 N042 100µ ic {Vi/8}
C28 N042 N052 100µ ic {Vi/8}
C29 N052 0 100µ ic {Vi/8}
V18 N048 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S16 N051 N050 N048 0 SIdeal
V19 N053 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S17 N055 N054 N053 0 SIdeal
V20 N023 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S18 N024 N025 N023 0 SIdeal
V21 N012 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S19 N015 N016 N012 0 SIdeal
V24 N034 0 PULSE(0 5 {delay} 5n 5n {100u-delay} 200u)
S22 N038 N037 N034 0 SIdeal
V25 N013 0 PULSE(0 5 {delay} 5n 5n {100u-delay} 200u)
S23 N019 N018 N013 0 SIdeal
V23 N009 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S21 N011 N010 N009 0 SIdeal
V26 N001 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S24 N004 N003 N001 0 SIdeal
V27 N030 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S25 N032 N031 N030 0 SIdeal
V28 N044 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S26 N046 N045 N044 0 SIdeal
R12 N007 Vp1- 14000
R13 N040 Vp2- 14000
D13 N002 Vi Dvb
D14 N005 N002 Dvb
C30 N002 Vp1- 4.7µ
D15 N014 N005 Dvb
D16 N026 N014 Dvb
C31 N006 N014 4.7µ
D17 N028 N026 Dvb
```

```
D18 N047 N028 Dvb
C32 N028 Vp2- 4.7µ
D19 N049 N047 Dvb
D20 0 N049 Dvb
C33 N039 N049 4.7µ
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=500k T=1/f delay=0.02u phi=0.0485*T
.model EPC2010 SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 2.6m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=0.5)
.tran 0 900u 800u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.backanno
.end
```

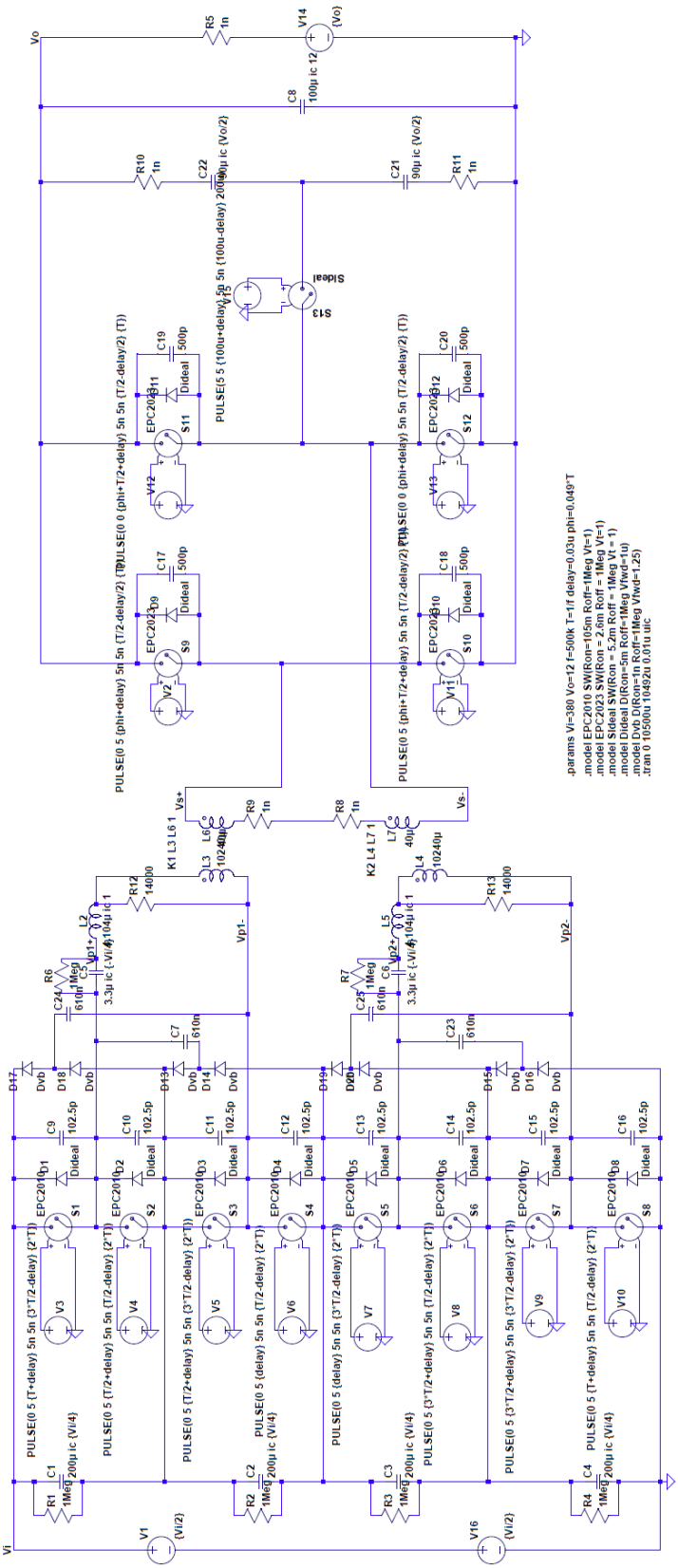


Figure C-9: Simulation schematic of the proposed double stacked active bridge converter operated in low-power mode at 500 kHz.

Netlist for Figure C-9

```
V1 Vi N029 {Vi/2}
V3 N001 0 PULSE(0 5 {T+delay} 5n 5n {3*T/2-delay} {2*T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {2*T})
S1 N004 Vi N001 0 EPC2010
S2 N003 N004 N006 0 EPC2010
S3 Vp1- N003 N009 0 EPC2010
S4 N014 Vp1- N013 0 EPC2010
V5 N009 0 PULSE(0 5 {T/2+delay} 5n 5n {3*T/2-delay} {2*T})
V6 N013 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {2*T})
C1 Vi N003 200µ ic {Vi/4}
C2 N003 N014 200µ ic {Vi/4}
V7 N019 0 PULSE(0 5 {delay} 5n 5n {3*T/2-delay} {2*T})
V8 N027 0 PULSE(0 5 {3*T/2+delay} 5n 5n {T/2-delay} {2*T})
S5 N022 N014 N019 0 EPC2010
S6 N024 N022 N027 0 EPC2010
S7 Vp2- N024 N030 0 EPC2010
S8 0 Vp2- N032 0 EPC2010
V9 N030 0 PULSE(0 5 {3*T/2+delay} 5n 5n {3*T/2-delay} {2*T})
V10 N032 0 PULSE(0 5 {T+delay} 5n 5n {T/2-delay} {2*T})
C3 N014 N024 200µ ic {Vi/4}
C4 N024 0 200µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N022 3.3µ ic {-Vi/4}
L3 Vp1- N005 10240µ Rser=114.6m
L4 Vp2- N023 10240µ Rser=114.6m
V2 N007 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay/2} {T})
V11 N025 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N025 0 EPC2023
V12 N008 0 PULSE(0 0 {phi+T/2+delay} 5n 5n {T/2-delay/2} {T})
V13 N026 0 PULSE(0 0 {phi+delay} 5n 5n {T/2-delay/2} {T})
S11 Vs- Vo N008 0 EPC2023
S12 0 Vs- N026 0 EPC2023
C8 Vo 0 100µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 102.5p
D2 N003 N004 Dideal
C10 N004 N003 102.5p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 102.5p
D4 N014 Vp1- Dideal
C12 Vp1- N014 102.5p
D5 N022 N014 Dideal
C13 N014 N022 102.5p
D6 N024 N022 Dideal
C14 N022 N024 102.5p
D7 Vp2- N024 Dideal
C15 N024 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 500p
D10 0 Vs+ Dideal
C18 Vs+ 0 500p
D11 Vs- Vo Dideal
C19 Vo Vs- 500p
```

```
D12 0 Vs- Dideal
C20 Vs- 0 500p
R1 Vi N003 1Meg
R2 N003 N014 1Meg
R3 N014 N024 1Meg
R4 N024 0 1Meg
R5 Vo N017 1n
L2 Vp1+ N005 4.104µ ic 1
L5 Vp2+ N023 4.104µ ic 1
L6 N012 Vs+ 40µ Rser=0.224m
L7 Vs- N021 40µ Rser=0.224m
R6 N004 Vp1+ 1Meg
R7 N022 Vp2+ 1Meg
R8 N018 N021 1n
R9 N012 N018 1n
V14 N017 0 {Vo}
C22 N011 N016 90µ ic {Vo/2} Rser=3.93m
C21 N016 N028 90µ ic {Vo/2} Rser=3.93m
R10 Vo N011 1n
R11 N028 0 1n
V15 N015 0 PULSE(5 5 {100u+delay} 5n 5n {100u-delay} 200u)
S13 Vs- N016 N015 0 SIdeal
R12 N005 Vp1- 14000
R13 N023 Vp2- 14000
D13 N010 N003 Dvb
D14 N014 N010 Dvb
C7 N004 N010 610n Rser=10.15m Lser=1.87n
D15 N031 N024 Dvb
D16 0 N031 Dvb
C23 N022 N031 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N020 N014 Dvb
D20 N024 N020 Dvb
C25 N020 Vp2- 610n Rser=10.15m Lser=1.87n
V16 N029 0 {Vi/2}
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=500k T=1/f delay=0.03u phi=0.049*T
.model EPC2010 SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 2.6m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 10500u 10492u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.backanno
.end
```

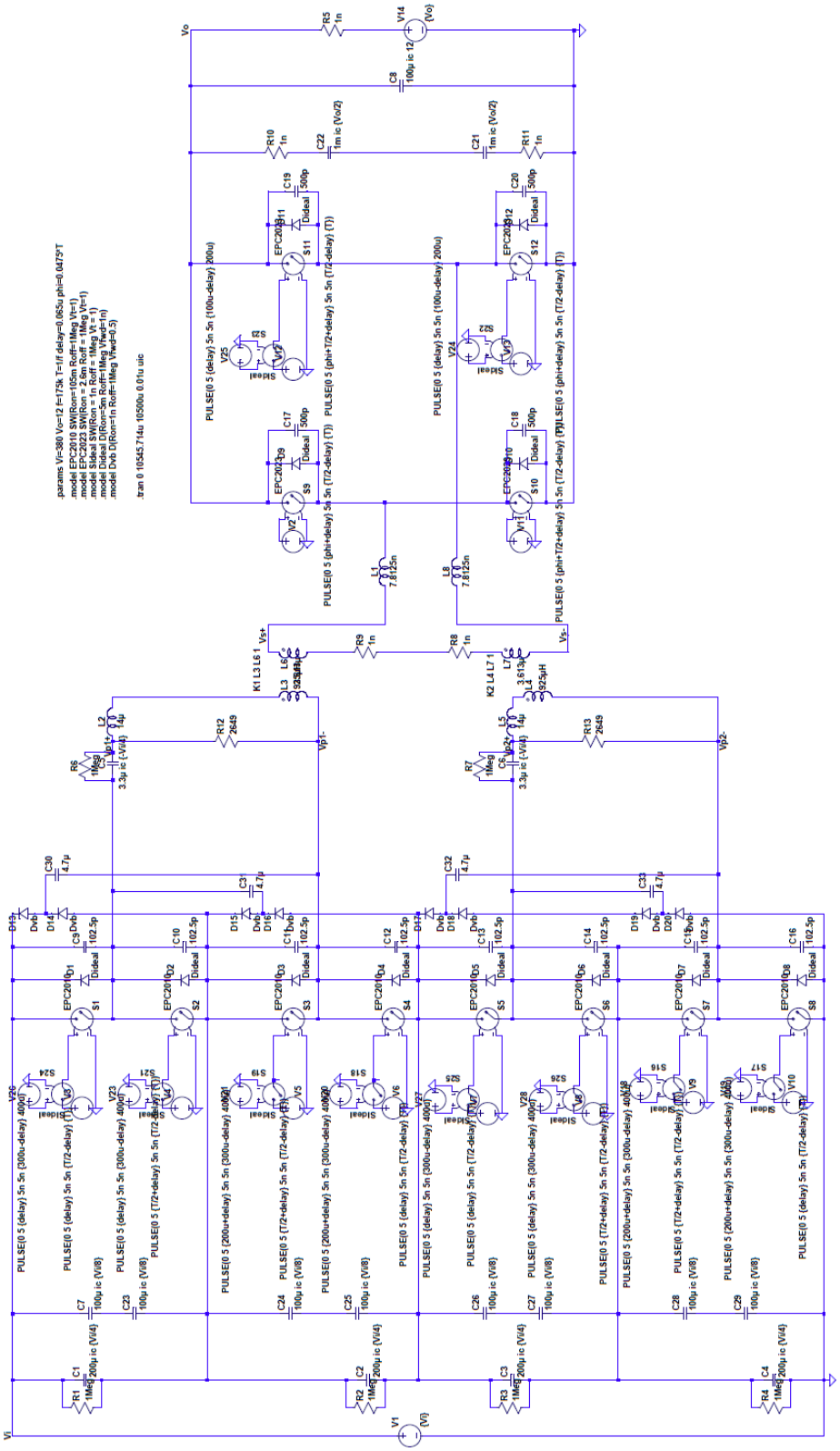


Figure C-10: Simulation schematic of the experimental prototype of the proposed double stacked active bridge converter operated at 175 kHz.

Netlist for Figure C-10

```
V1 Vi 0 {Vi}
V3 N003 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N010 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N006 Vi N004 0 EPC2010
S2 N005 N006 N011 0 EPC2010
S3 Vp1- N005 N015 0 EPC2010
S4 N028 Vp1- N026 0 EPC2010
V5 N016 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V6 N027 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C1 Vi N005 200µ ic {Vi/4}
C2 N005 N028 200µ ic {Vi/4}
V7 N033 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N047 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N041 N028 N034 0 EPC2010
S6 N044 N041 N048 0 EPC2010
S7 Vp2- N044 N053 0 EPC2010
S8 0 Vp2- N057 0 EPC2010
V9 N052 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N056 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 N028 N044 200µ ic {Vi/4}
C4 N044 0 200µ ic {Vi/4}
C5 Vp1+ N006 3.3µ ic {-Vi/4}
C6 Vp2+ N041 3.3µ ic {-Vi/4}
L3 Vp1- N007 925µH Rser=88.5m
L4 Vp2- N042 925µH Rser=88.5m
V2 N017 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay} {T})
V11 N038 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay} {T})
S9 N020 Vo N017 0 EPC2023
S10 0 N020 N038 0 EPC2023
V12 N018 0 PULSE(0 5 {phi+T/2+delay} 5n 5n {T/2-delay} {T})
V13 N039 0 PULSE(0 5 {phi+delay} 5n 5n {T/2-delay} {T})
S11 N021 Vo N019 0 EPC2023
S12 0 N021 N040 0 EPC2023
C8 Vo 0 100µ ic 12
D1 N006 Vi Dideal
C9 Vi N006 102.5p
D2 N005 N006 Dideal
C10 N006 N005 102.5p
D3 Vp1- N005 Dideal
C11 N005 Vp1- 102.5p
D4 N028 Vp1- Dideal
C12 Vp1- N028 102.5p
D5 N041 N028 Dideal
C13 N028 N041 102.5p
D6 N044 N041 Dideal
C14 N041 N044 102.5p
D7 Vp2- N044 Dideal
C15 N044 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 N020 Vo Dideal
C17 Vo N020 500p
D10 0 N020 Dideal
C18 N020 0 500p
D11 N021 Vo Dideal
```

```
C19 Vo N021 500p
D12 0 N021 Dideal
C20 N021 0 500p
R1 Vi N005 1Meg
R2 N005 N028 1Meg
R3 N028 N044 1Meg
R4 N044 0 1Meg
R5 Vo N029 1n
L2 Vp1+ N007 14µ
L5 Vp2+ N042 14µ
L6 N024 Vs+ 3.613µ Rser=0.346m
L7 Vs- N037 3.613µ
R6 N006 Vp1+ 1Meg
R7 N041 Vp2+ 1Meg
R8 N031 N037 1n
R9 N024 N031 1n
V14 N029 0 {Vo}
C22 N022 N035 1m ic {Vo/2}
C21 N035 N043 1m ic {Vo/2}
R10 Vo N022 1n
R11 N043 0 1n
C7 Vi N008 100µ ic {Vi/8}
C23 N008 N005 100µ ic {Vi/8}
C24 N005 N023 100µ ic {Vi/8}
C25 N023 N028 100µ ic {Vi/8}
C26 N028 N045 100µ ic {Vi/8}
C27 N045 N044 100µ ic {Vi/8}
C28 N044 N054 100µ ic {Vi/8}
C29 N054 0 100µ ic {Vi/8}
V18 N050 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S16 N053 N052 N050 0 SIdeal
V19 N055 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S17 N057 N056 N055 0 SIdeal
V20 N025 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S18 N026 N027 N025 0 SIdeal
V21 N012 0 PULSE(0 5 {200u+delay} 5n 5n {300u-delay} 400u)
S19 N015 N016 N012 0 SIdeal
V24 N036 0 PULSE(0 5 {delay} 5n 5n {100u-delay} 200u)
S22 N040 N039 N036 0 SIdeal
V25 N013 0 PULSE(0 5 {delay} 5n 5n {100u-delay} 200u)
S23 N019 N018 N013 0 SIdeal
V23 N009 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S21 N011 N010 N009 0 SIdeal
V26 N001 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S24 N004 N003 N001 0 SIdeal
V27 N032 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S25 N034 N033 N032 0 SIdeal
V28 N046 0 PULSE(0 5 {delay} 5n 5n {300u-delay} 400u)
S26 N048 N047 N046 0 SIdeal
R12 Vp1+ Vp1- 2649
R13 Vp2+ Vp2- 2649
D13 N002 Vi Dvb
D14 N005 N002 Dvb
C30 N002 Vp1- 4.7µ
D15 N014 N005 Dvb
D16 N028 N014 Dvb
C31 N006 N014 4.7µ
```

```
D17 N030 N028 Dvb
D18 N049 N030 Dvb
C32 N030 Vp2- 4.7µ
D19 N051 N049 Dvb
D20 0 N051 Dvb
C33 N041 N051 4.7µ
L1 Vs+ N020 7.8125n
L8 Vs- N021 7.8125n
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=0.065u phi=0.0475*T
.model EPC2010 SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 2.6m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1n)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=0.5)
.tran 0 10545.714u 10500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.backanno
.end
```

Table C-2: Simulation Operating Parameters and Power Data for the Regular DAB converter of Figure C-6 when operated with an input voltage of 380 V, an output voltage of 12 V, and an operating frequency of 500 kHz. Inverter devices are modeled off of GaNSystems GS66516T with 70 mΩ of resistance and 134 pF of capacitance

Theoretical		Simulation				
Power (W)	**Phase Shift (%)**	**Phase Shift (%)**	**Dead-time (µs)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
40	0.454	2.95	0.12	97.89	40.11	40.97
80	0.917	3.19	0.12	140.54	80.76	57.46
100	1.151	3.30	0.12	154.19	99.35	64.44
120	1.389	3.42	0.12	173.60	119.42	68.79
160	1.870	3.67	0.12	207.53	161.00	77.58
200	2.362	3.95	0.12	242.83	201.90	83.14
240	2.864	4.15	0.12	273.59	239.04	87.37
280	3.378	4.40	0.12	310.75	278.41	89.59
320	3.905	4.70	0.12	352.54	324.95	92.17
360	4.445	4.95	0.12	384.77	363.03	94.35
400	5	5.20	0.12	420.21	400.29	95.26

Table C-3: Simulation Operating Parameters and Power Data for the single stacked active bridge converter of Figure C-7 when operated with an input voltage of 380 V, an output voltage of 12 V, and an operating frequency of 500 kHz. Inverter devices are modeled off of EPC2025 with 140 mΩ of resistance and 106.25 pF of capacitance

Theoretical		Simulation				
Power (W)	**Phase Shift (%)**	**Phase Shift (%)**	**Dead-time (µs)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
40	0.454	1.35	0.055	51.92	40.61	78.21
80	0.917	1.60	0.055	90.50	79.83	88.20
100	1.151	1.73	0.055	109.54	100.20	91.47
120	1.389	1.86	0.055	128.69	120.39	93.55
160	1.870	2.12	0.055	166.77	160.23	96.08
200	2.362	2.39	0.055	206.39	200.94	97.36
240	2.864	2.65	0.055	244.66	239.54	97.91
280	3.378	2.92	0.055	284.35	279.01	98.12
320	3.905	3.55	0.045	326.43	320.14	98.07
360	4.445	4.12	0.040	367.43	359.97	97.97
400	5	4.60	0.040	407.73	398.88	97.83

Table C-4: Simulation Operating Parameters and Power Data for the double stacked active bridge converter of Figure C-8 when operated with an input voltage of 380 V, an output voltage of 12 V, and an operating frequency of 500 kHz. Inverter devices are modeled off of EPC2019 with 55 mΩ of resistance and 185 pF of capacitance

Theoretical		Simulation				
Power (W)	**Phase Shift (%)**	**Phase Shift (%)**	**Dead-time (µs)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
40	0.454	1.375	0.0575	49.37	40.06	81.14
80	0.917	1.59	0.0575	88.53	79.30	89.57
100	1.151	1.70	0.0575	107.75	99.47	92.31
120	1.389	1.81	0.0575	127.00	119.57	94.15
160	1.870	2.04	0.0575	167.55	161.48	96.38
200	2.362	2.25	0.0575	205.11	199.53	97.28
240	2.864	2.475	0.0575	244.93	239.73	97.88
280	3.378	3.04	0.045	285.58	280.04	98.06
320	3.905	3.69	0.035	326.77	320.09	97.96
360	4.445	4.15	0.035	367.74	359.85	97.85
400	5	4.85	0.027	409.58	400.00	97.66

Table C-5: Simulation Operating Parameters and Power Data for the double stacked active bridge converter of Figure C-8 when operated with an input voltage of 380 V, an output voltage of 12 V, and an operating frequency of 500 kHz. Inverter devices are modeled off of EPC2012C with 105 mΩ of resistance and 102.5 pF of capacitance

Theoretical		Simulation				
Power (W)	**Phase Shift (%)**	**Phase Shift (%)**	**Dead-time (µs)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
40	0.454	1.07	0.045	46.73	40.471	86.61
80	0.917	1.285	0.045	84.982	79.759	93.85
100	1.151	1.4	0.045	105.48	100.79	95.55
120	1.389	1.51	0.045	125.09	120.81	96.58
160	1.870	1.73	0.045	164.65	160.67	97.58
200	2.362	1.95	0.045	204.97	200.81	97.97
240	2.864	2.4	0.04	245.74	240.89	98.03
280	3.378	3.2	0.025	286.49	280.51	97.91
320	3.905	3.75	0.022	327.78	320.49	97.78
360	4.445	4.3	0.020	368.65	359.84	97.61
400	5	4.85	0.020	411.55	400.92	97.42

Table C-6: Simulation Operating Parameters and Power Data for the double stacked active bridge converter of Figure C-9 when operated in low-power mode with an input voltage of 380 V, an output voltage of 12 V, and an operating frequency of 500 kHz. Inverter devices are modeled off of EPC2012C with 105 mΩ of resistance and 102.5 pF of capacitance

Theoretical		Simulation				
Power (W)	**Phase Shift (%)**	**Phase Shift (%)**	**Dead-time (µs)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
40	1.870	2.00	0.040	41.94	39.22	93.52
80	3.905	3.75	0.040	85.30	81.85	95.95
100	5.000	4.90	0.030	104.74	100.10	95.57
120	6.159	6.10	0.025	125.48	119.23	95.02
160	8.721	9.70	0.025	184.58	171.43	92.88
200	11.771	13.00	0.025	227.95	206.68	90.67
240	15.781	19.00	0.025	282.34	243.19	86.13

Table C-7: Simulation Operating Parameters and Power Data for the experimental prototype of the double stacked active bridge converter of Figure C-10 when operated with an output voltage of 12 V, an output power of 300 W, a turns ratio of 16 and an operating frequency of 175 kHz. Inverter devices are modeled off of EPC2012C with 105 mΩ of resistance and 102.5 pF of capacitance

	Theoretical		Simulation					
Power (W)	**Phase Shift (%)**	**Pcore (W)**	**Phase Shift (%)**	**Dead-time (µs)**	**Rcore (Ω)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
260	8.02	1.885	9.70	0.065	4482	322.56	300.77	93.24
290	7.02	2.729	8.05	0.065	3853	316.04	299.13	94.65
320	6.25	3.808	6.75	0.065	3361	312.62	298.44	95.46
350	5.64	5.158	5.95	0.065	2969	313.82	300.61	95.79
380	5.13	6.814	5.25	0.065	2649	311.39	298.18	95.76
410	4.71	8.813	4.75	0.065	2384	314.12	299.65	95.39

Table C-8: Simulation Operating Parameters and Power Data for the experimental prototype of the double stacked active bridge converter of Figure C-10 when operated with an output voltage of 12 V, an output power of 300 W, a turns ratio of 14 and an operating frequency of 175 kHz. Inverter devices are modeled off of EPC2012C with 105 mΩ of resistance and 102.5 pF of capacitance

	Theoretical		Simulation					
Power (W)	**Phase Shift (%)**	**Pcore (W)**	**Phase Shift (%)**	**Dead-time (µs)**	**Rcore (Ω)**	**Pin (W)**	**Pout (W)**	**Efficiency (%)**
260	9.50	1.885	9.70	0.065	4482	314.69	299.44	95.15
290	8.26	2.729	8.25	0.065	3853	310.99	298.32	95.93
320	7.32	3.808	7.25	0.065	3361	312.04	300.26	96.22
350	6.58	5.158	6.40	0.065	2969	311.47	299.54	96.17
380	5.98	6.814	5.75	0.065	2649	313.55	300.35	95.79
410	5.48	8.813	5.20	0.065	2384	316.32	300.77	95.08

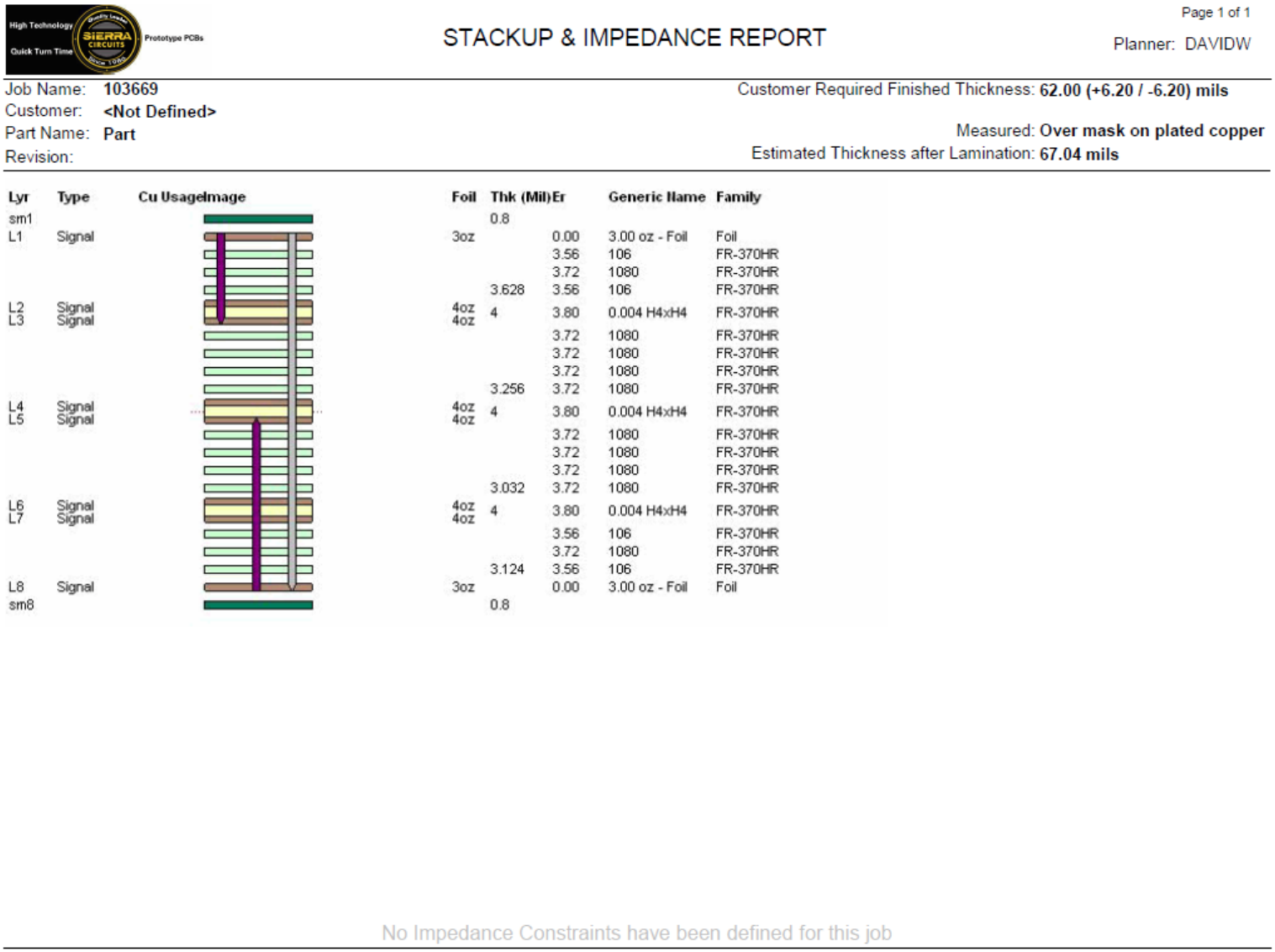
Appendix D EAGLE Layout Files

This Appendix contains layout details for each of the prototype boards. The layout for all boards was done in EAGLE V6. There are a total of four layouts of varying layer counts. The first set of layout files contains multiple variants of the transformers and a version of the coupled magnetic structure. The second set of layout files contains the inverter stage of the ICN as well as a diode bridge rectifier used in the initial testing stage. The third set of layout files contains the fully integrated ICN board that was developed but could never reach the targeted input voltage range due to the reduction in parasitics and adverse effects on the inverter stage. The fourth set contains the GaN-based and Si-based reconfigurable active bridge boards.

D.1 Planar Magnetic PCB Windings

This set of layout files contains the planar PCB winding for the transformer used for the ICN converter. A planar magnetic structure is also shown, but the inductance of this design was too high because of the large core size. There are other variants of the transformer and coupled inductor stackup, which were used in the analysis performed in [60]. The board was ordered from Sierra Circuits using an 8 layer design with 4 oz. copper on all layers and HASL surface finish. The board material is FR4 with green soldermask and white silkscreen. There are blind vias connecting layers 1 - 3 and another set connecting layers 5 – 8 for the transformer primary windings. The manufacturer stackup report can be found in Figure D-1. The layout for each of the 8 layers can be found in Figure D-2 through Figure D-9.

Figure D-1: Stackup and Impedance Report for the board containing the ICN transformer PCB winding.



High Technology Quick Turn Time SIERRA CIRCUITS Prototype PCBs

STACKUP & IMPEDANCE REPORT

Planner: DAVIDW

Job Name: **103669**
Customer: **<Not Defined>**
Part Name: **Part**
Revision:

Customer Required Finished Thickness: **62.00 (+6.20 / -6.20) mils**

Measured: **Over mask on plated copper**

Estimated Thickness after Lamination: **67.04 mils**

Lyr	Type	Cu Usage	Image	Foil	Thk (Mil)	Er	Generic Name	Family
sm1					0.8			
L1	Signal			3oz		0.00	3.00 oz - Foil	Foil
						3.56	106	FR-370HR
						3.72	1080	FR-370HR
					3.628	3.56	106	FR-370HR
L2	Signal			4oz	4	3.80	0.004 H4xH4	FR-370HR
L3	Signal			4oz				
						3.72	1080	FR-370HR
						3.72	1080	FR-370HR
						3.72	1080	FR-370HR
					3.256	3.72	1080	FR-370HR
L4	Signal			4oz	4	3.80	0.004 H4xH4	FR-370HR
L5	Signal			4oz				
						3.72	1080	FR-370HR
						3.72	1080	FR-370HR
						3.72	1080	FR-370HR
					3.032	3.72	1080	FR-370HR
L6	Signal			4oz	4	3.80	0.004 H4xH4	FR-370HR
L7	Signal			4oz				
						3.56	106	FR-370HR
						3.72	1080	FR-370HR
					3.124	3.56	106	FR-370HR
L8	Signal			3oz		0.00	3.00 oz - Foil	Foil
sm8					0.8			

No Impedance Constraints have been defined for this job

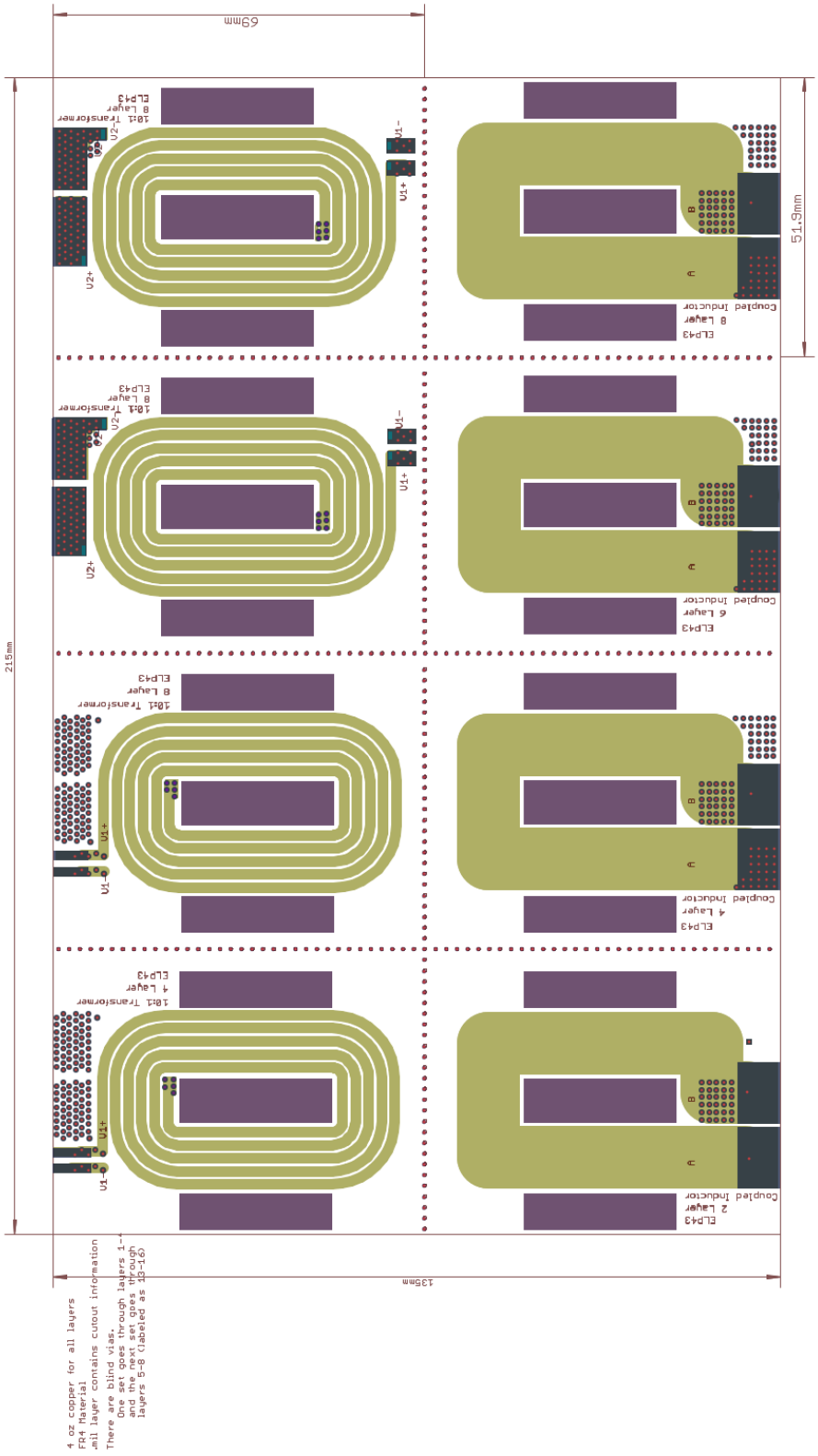


Figure D-2: Layer 1 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

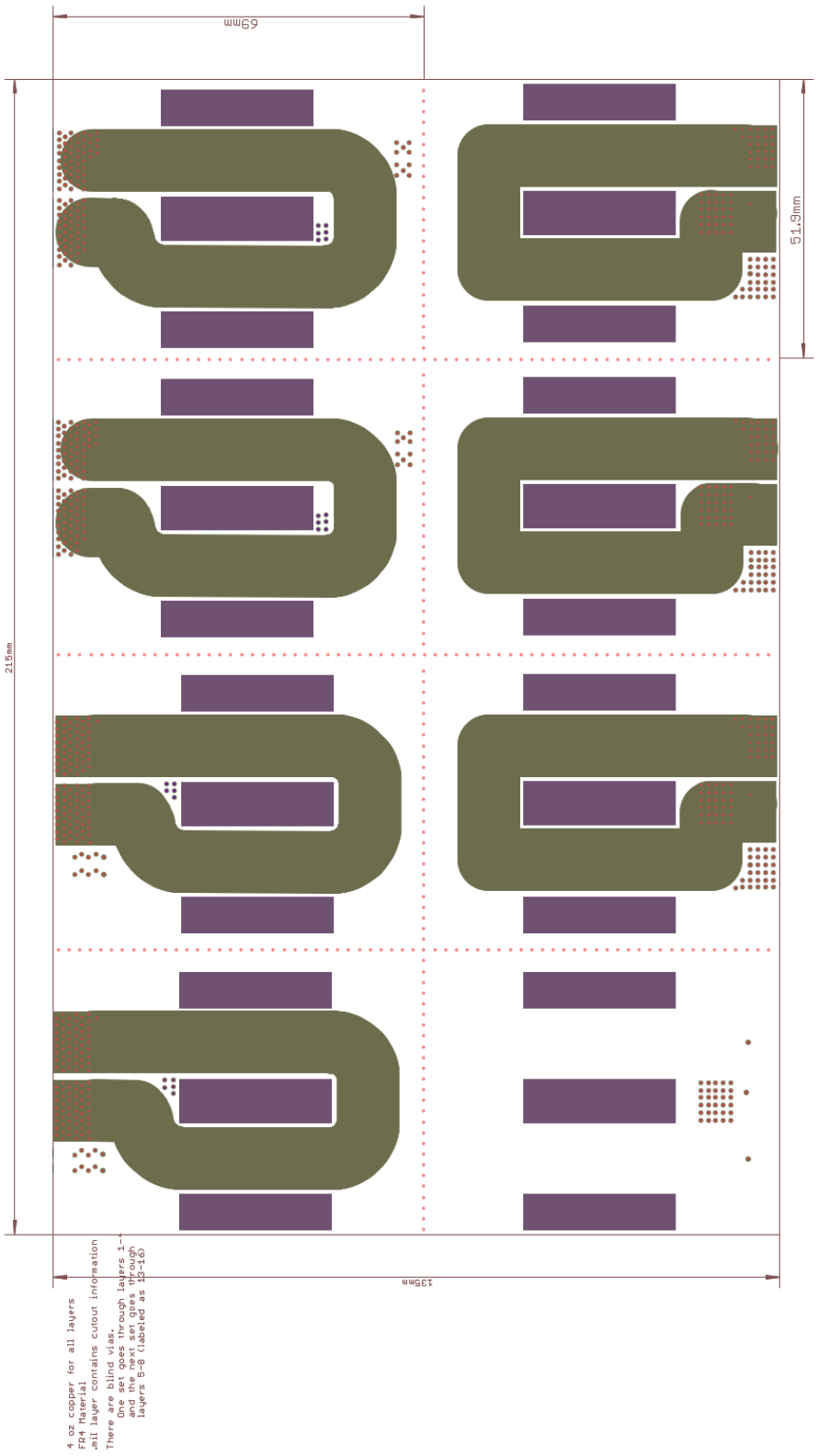


Figure D-3: Layer 2 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

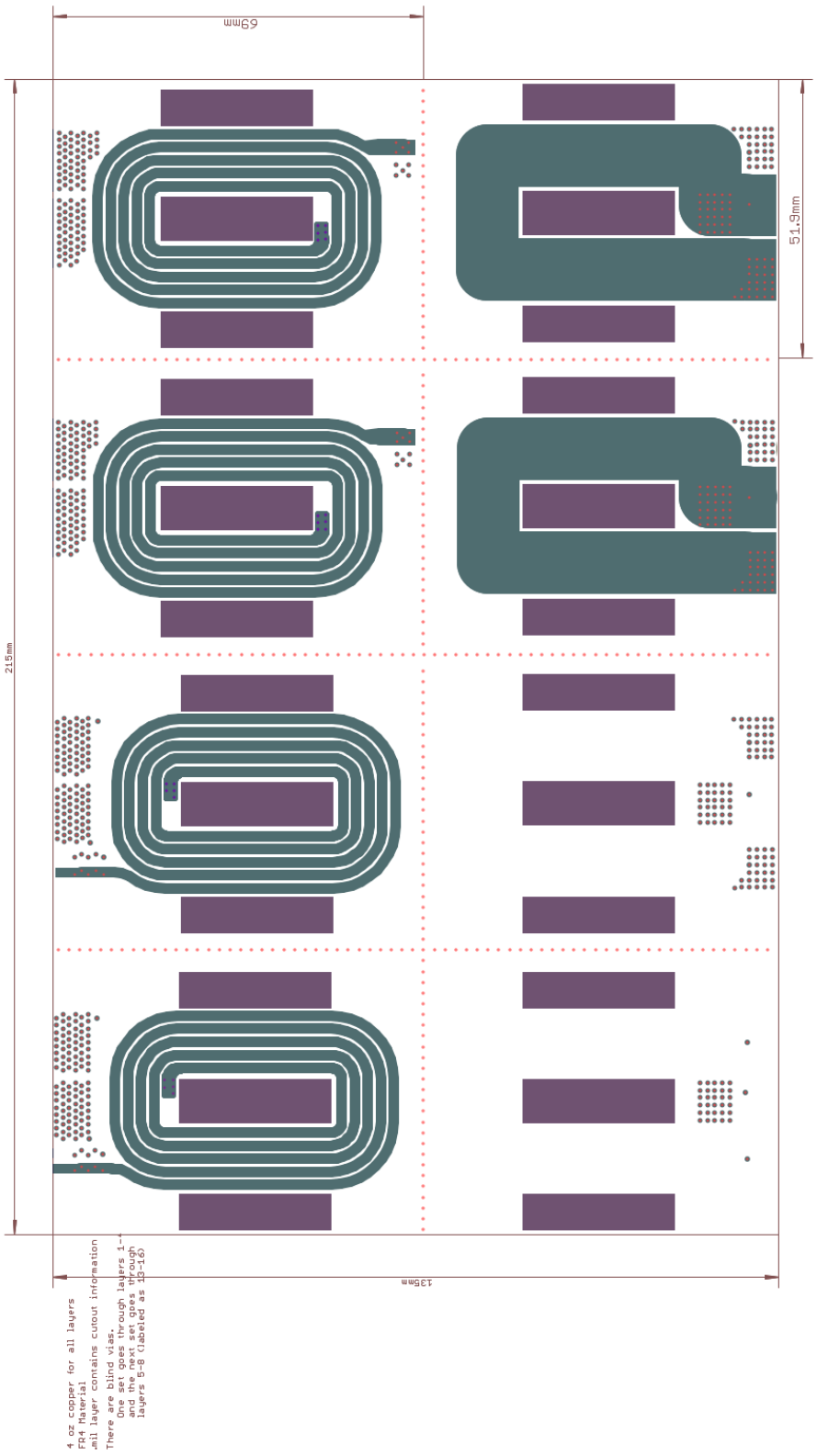


Figure D-4: Layer 3 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

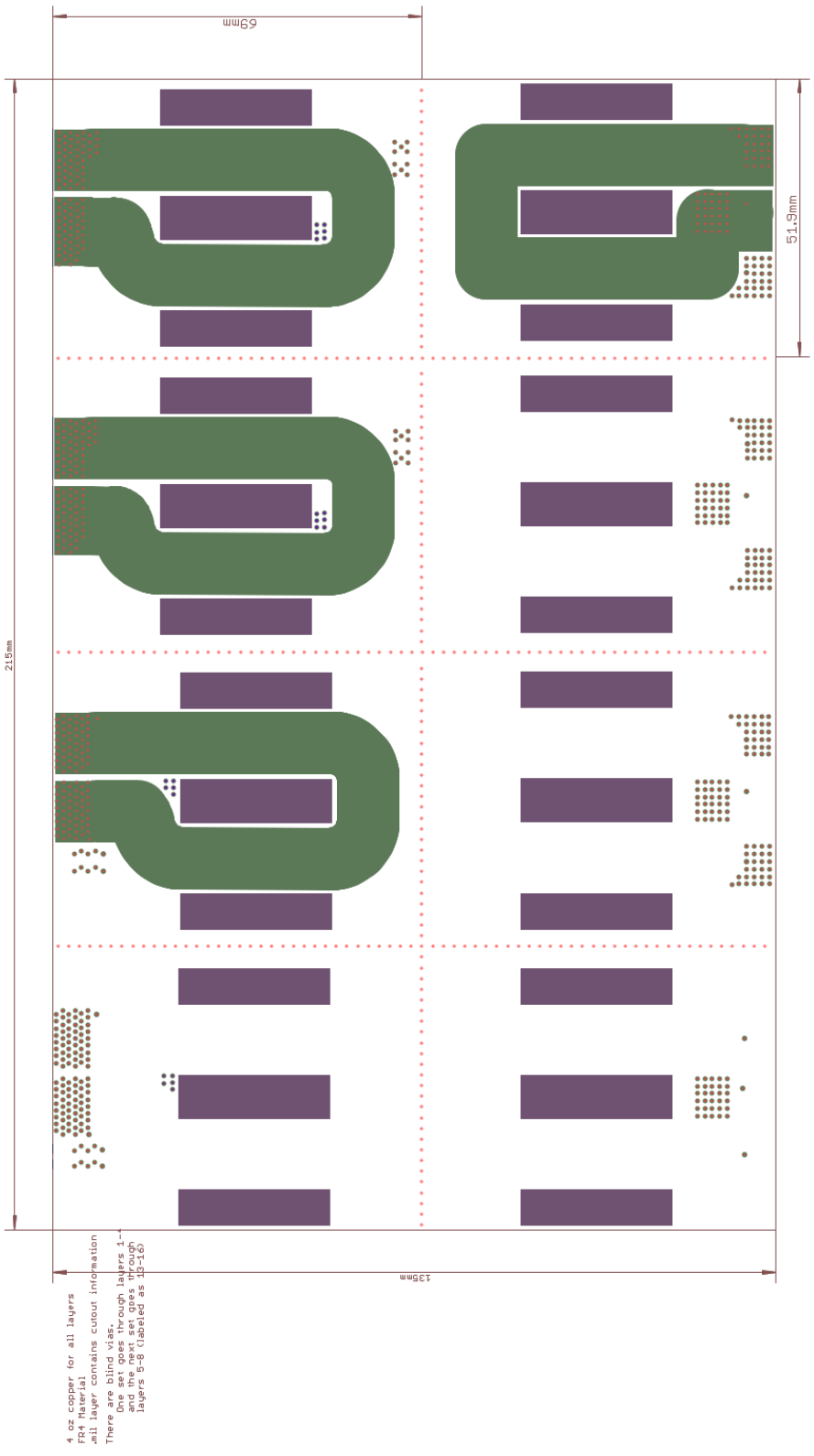


Figure D-5: Layer 4 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

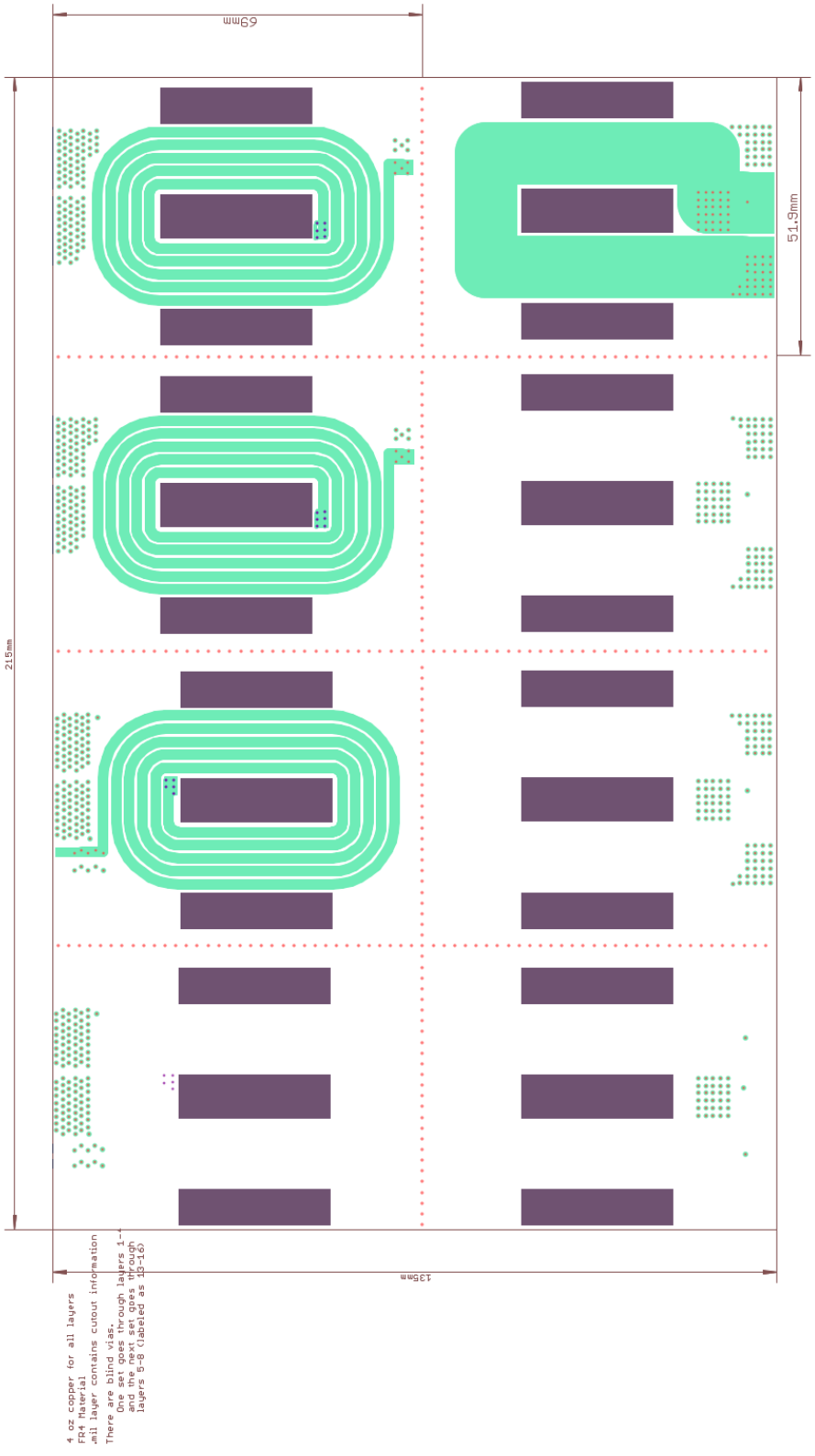


Figure D-6: Layer 5 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

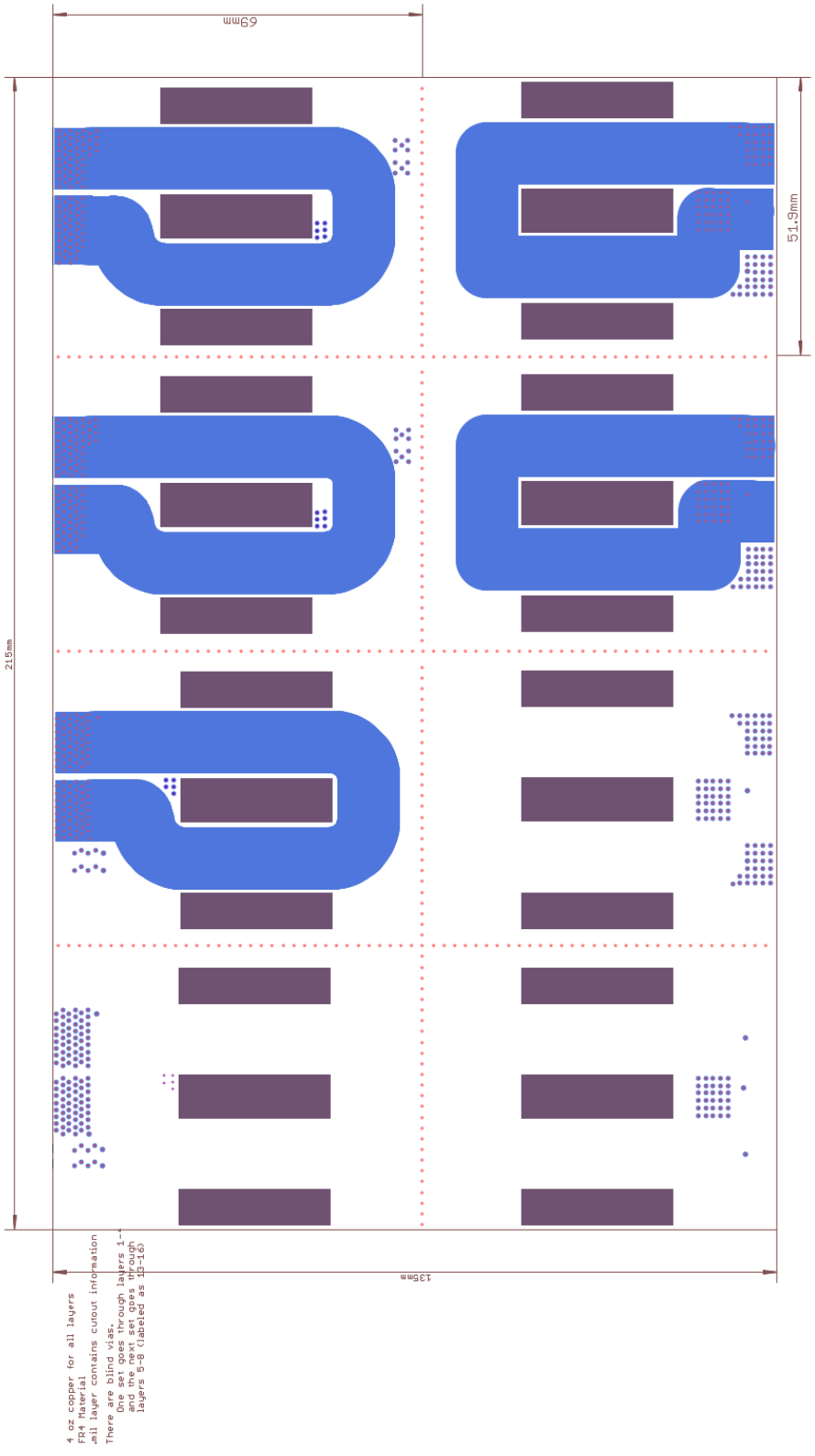


Figure D-7: Layer 6 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

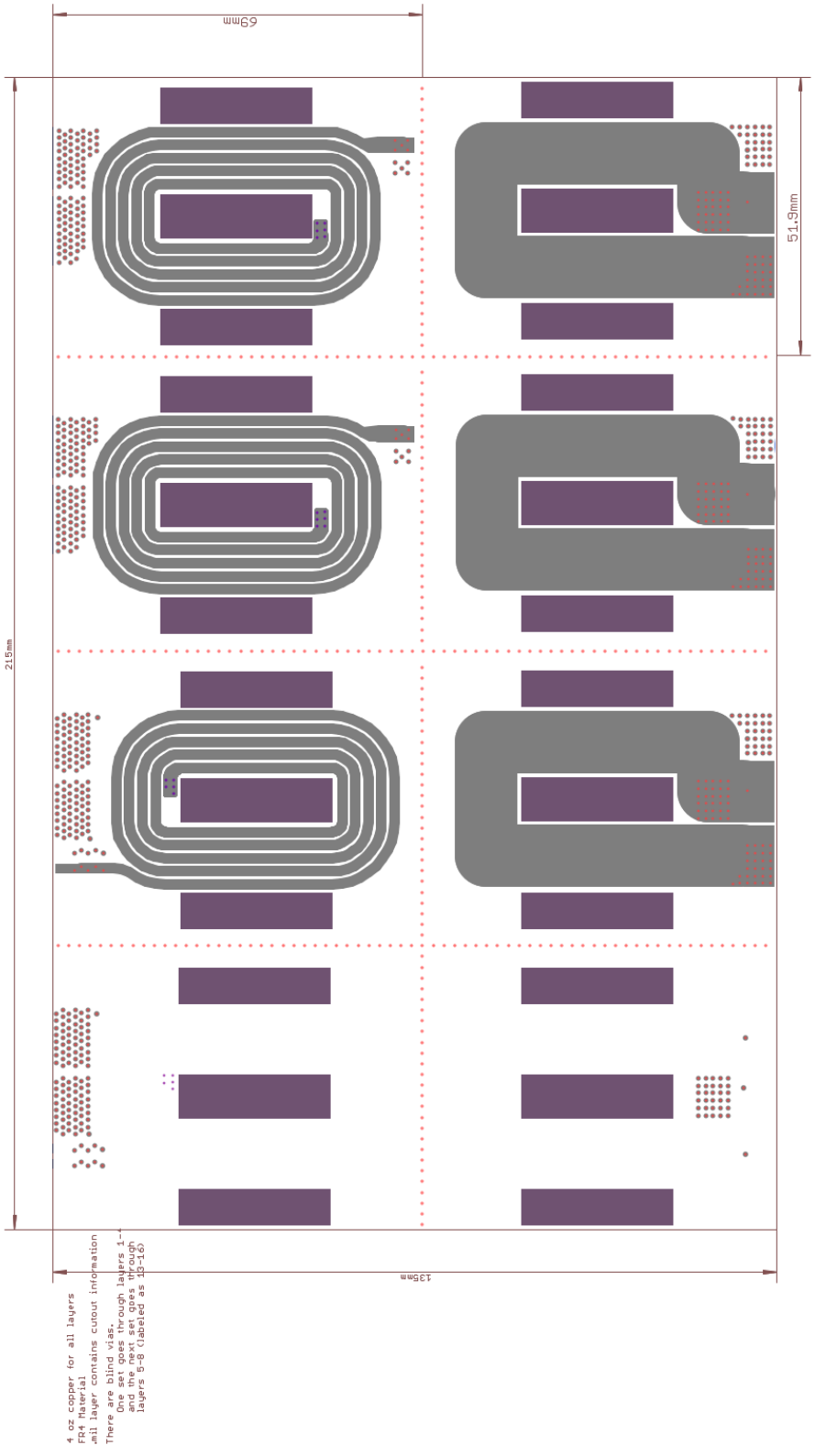


Figure D-8: Layer 7 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

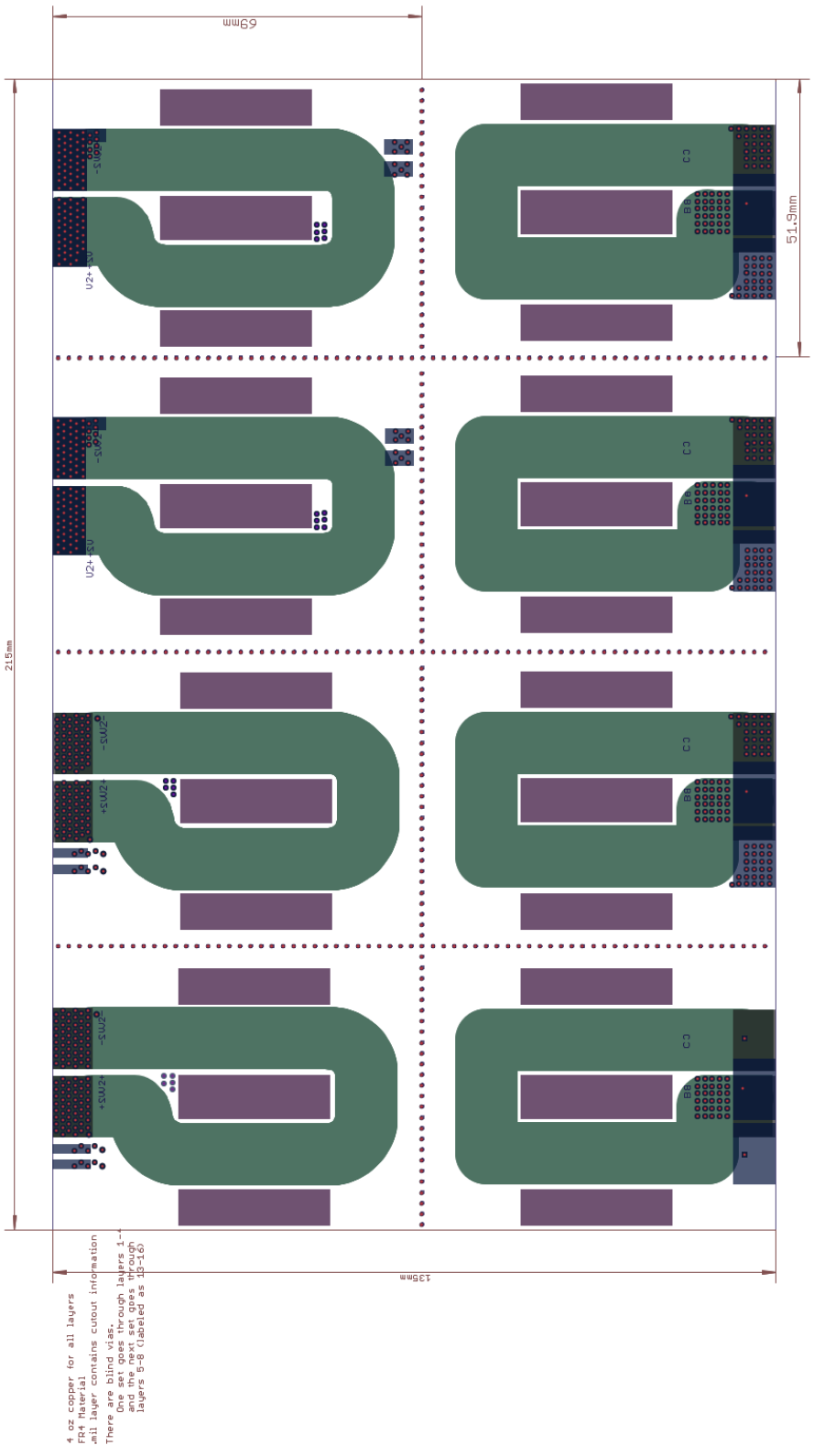


Figure D-9: Layer 8 of the ICN transformer PCB winding (located in the top left) and other magnetic component variants. The purple rectangles indicate cutouts in the board.

D.2 First Generation ICN Converter

This set of layout files contains the first generation board used for initial testing of the ICN converter. The inverter stage of this board is also used in the final prototype shown in Figure 2-25. The rectifier stage is a full bridge diode rectifier for ease of control but due to efficiency concerns, this was replaced with the synchronous full bridge rectifier of the next subsection. The board was ordered from Advanced Circuits using a 4 layer design with 1 oz. copper on the outer layers, 2 oz copper on the inner layers and HASL surface finish. The board material is FR4 with green soldermask and white silkscreen. The layout for each of the 4 layers can be found in Figure D-10 through Figure D-13.

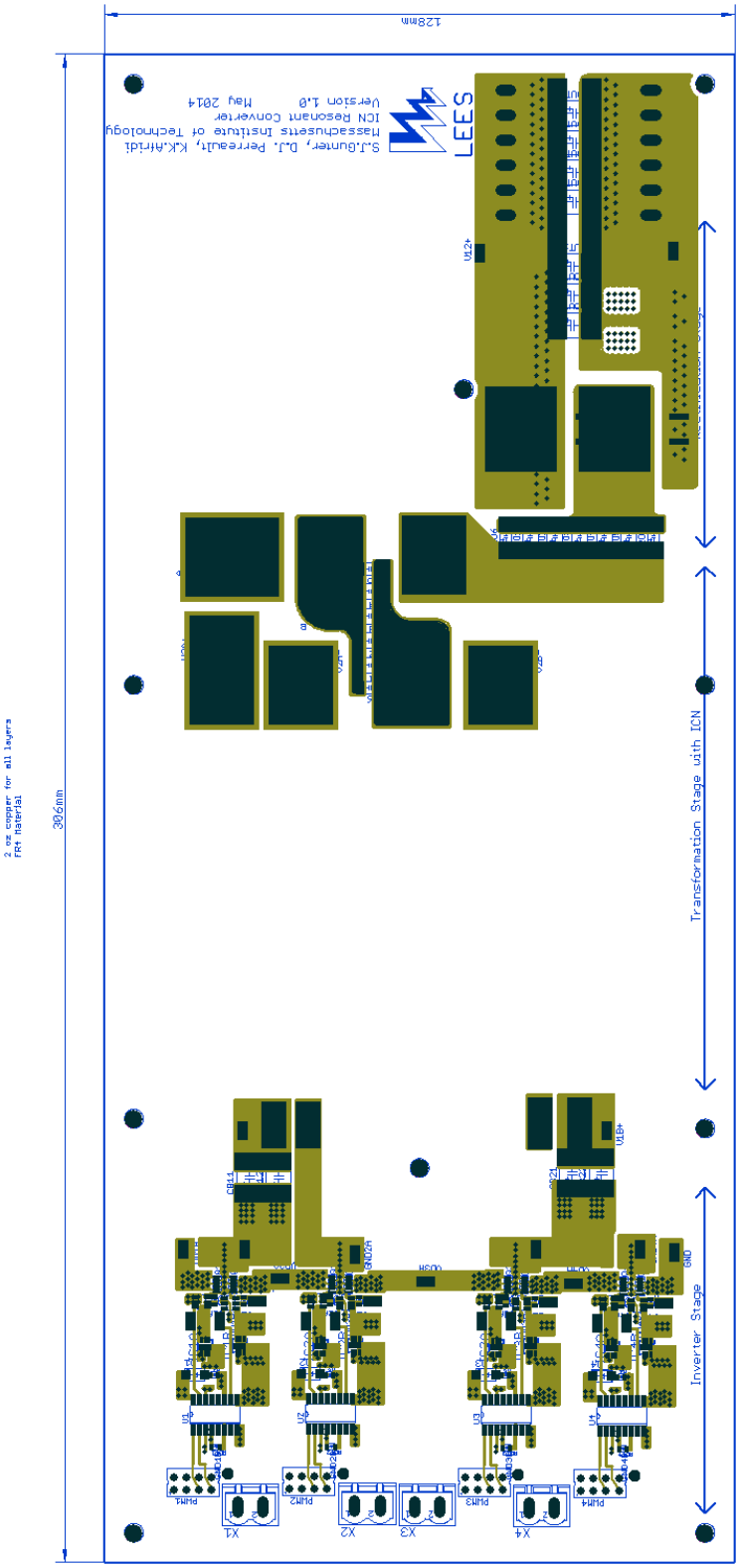


Figure D-10: Layer 1 of the first generation ICN converter board.

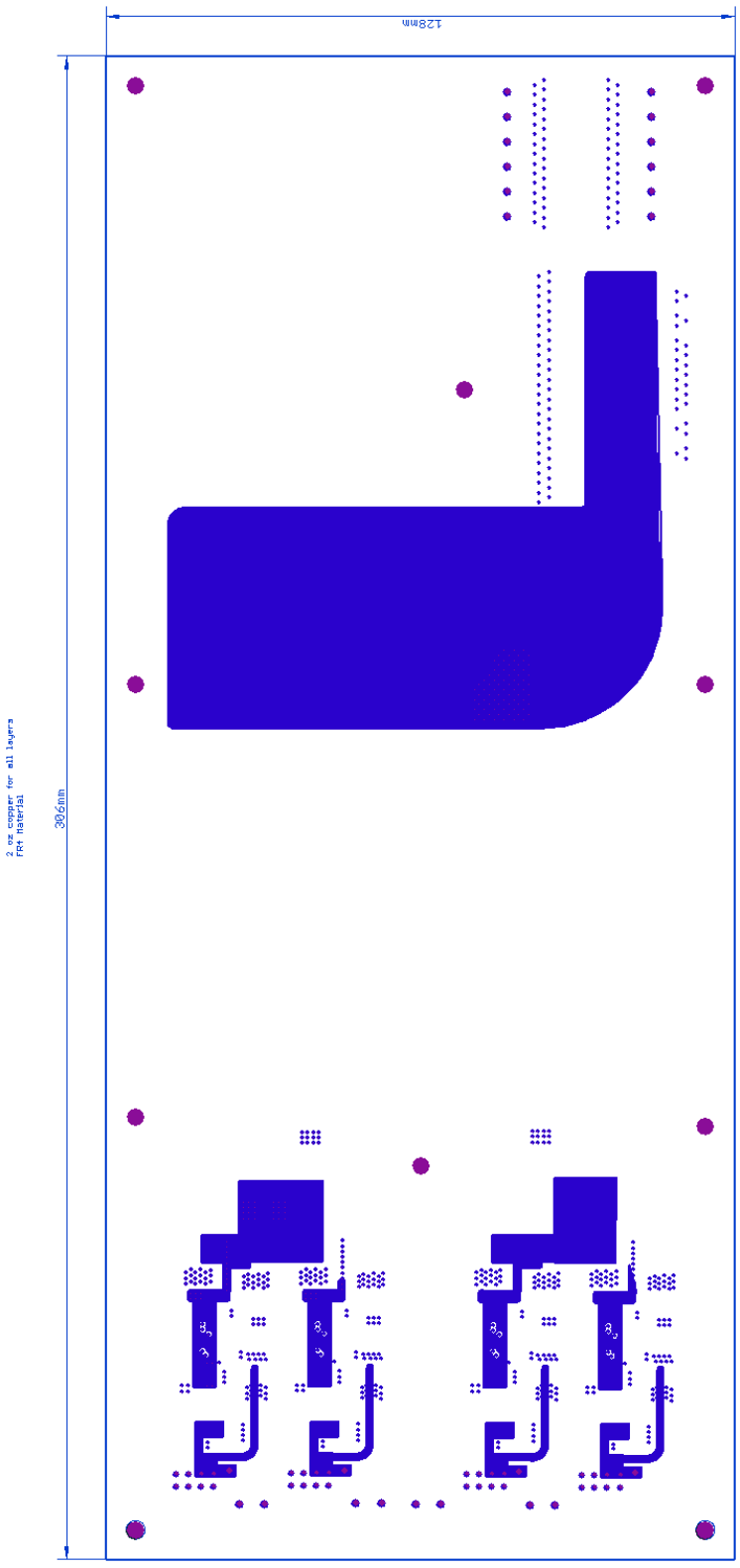


Figure D-11: Layer 2 of the first generation ICN converter board.

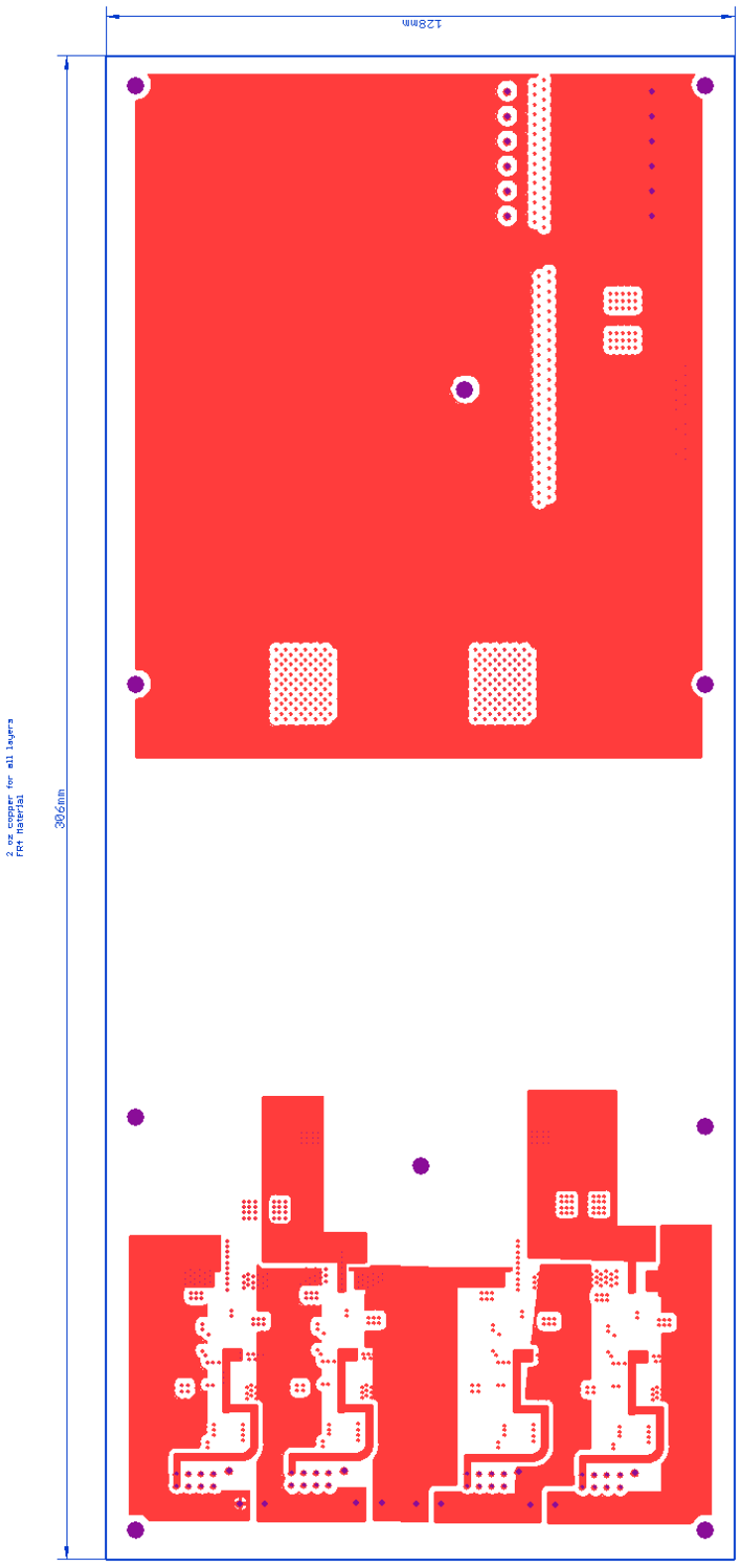


Figure D-12: Layer 3 of the first generation ICN converter board.

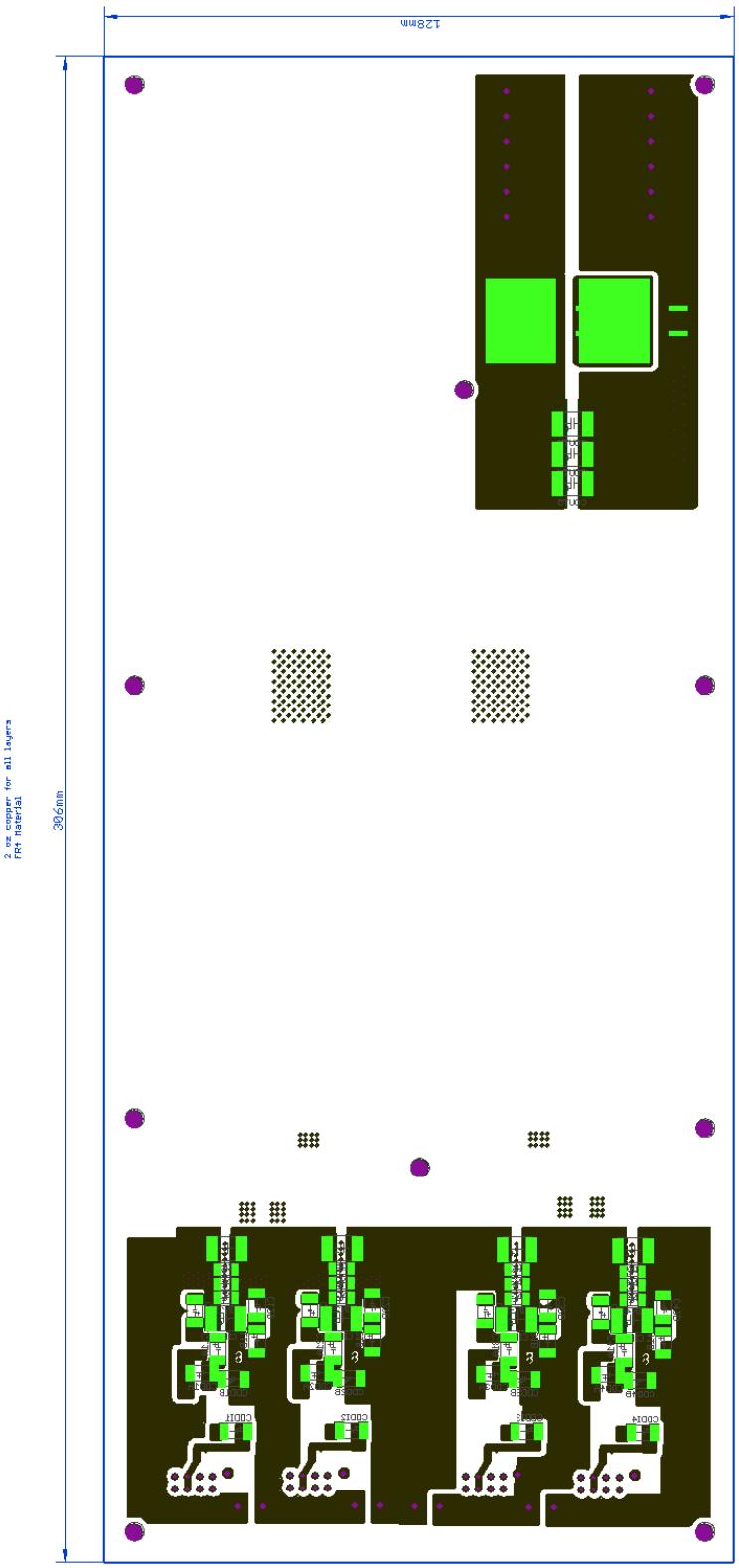


Figure D-13: Layer 4 of the first generation ICN converter board.

D.3 Synchronous Full Bridge Rectifier for the ICN Converter

This set of layout files contains the synchronous full bridge rectifier used for the ICN converter of Figure 2-25. The board was ordered from Advanced Circuits using a 4 layer design with 1 oz. copper on the outer layers, 2 oz copper on the inner layers and HASL surface finish. The board material is FR4 with green soldermask and white silkscreen. The layout for each of the 4 layers can be found in Figure D-14 through Figure D-17.

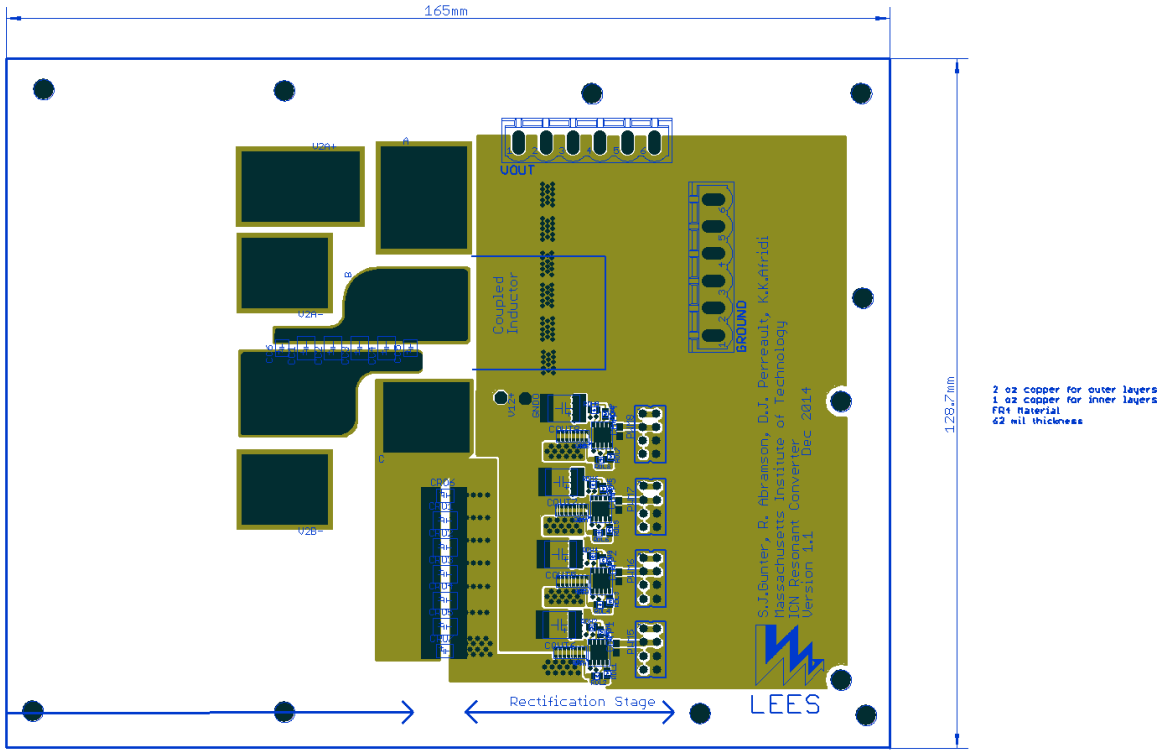


Figure D-14: Layer 1 of the synchronous full bridge rectifier for the ICN converter.

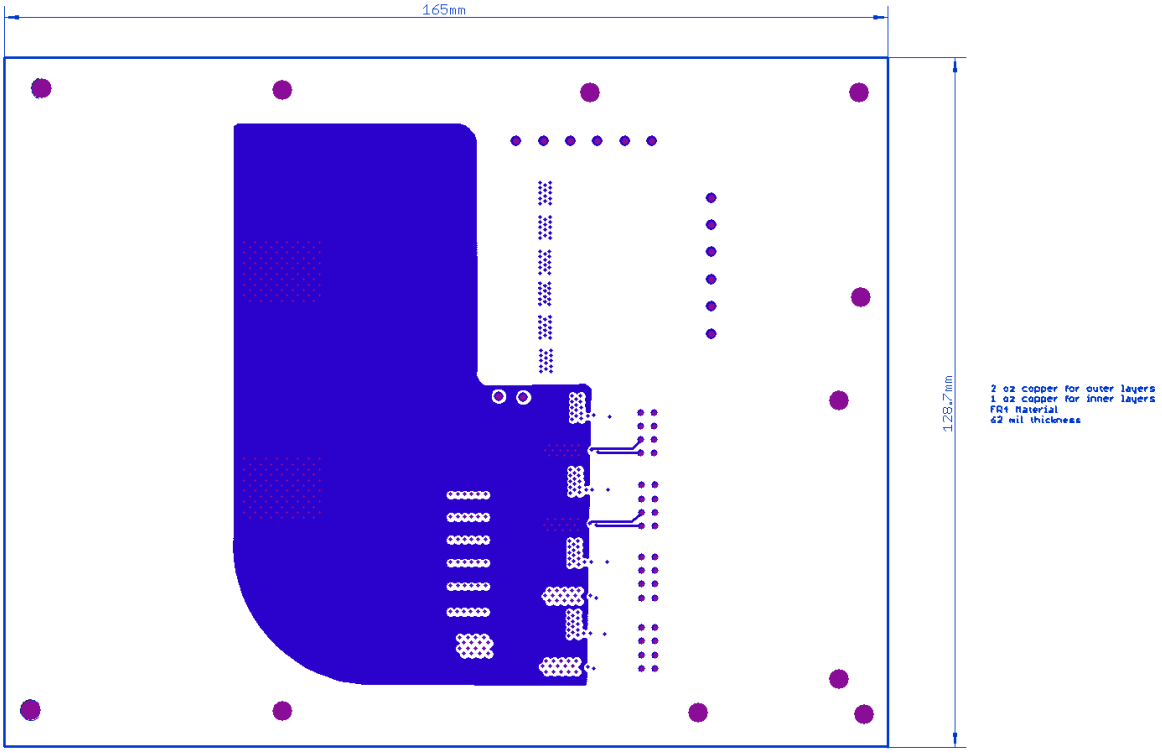


Figure D-15: Layer 2 of the synchronous full bridge rectifier for the ICN converter.

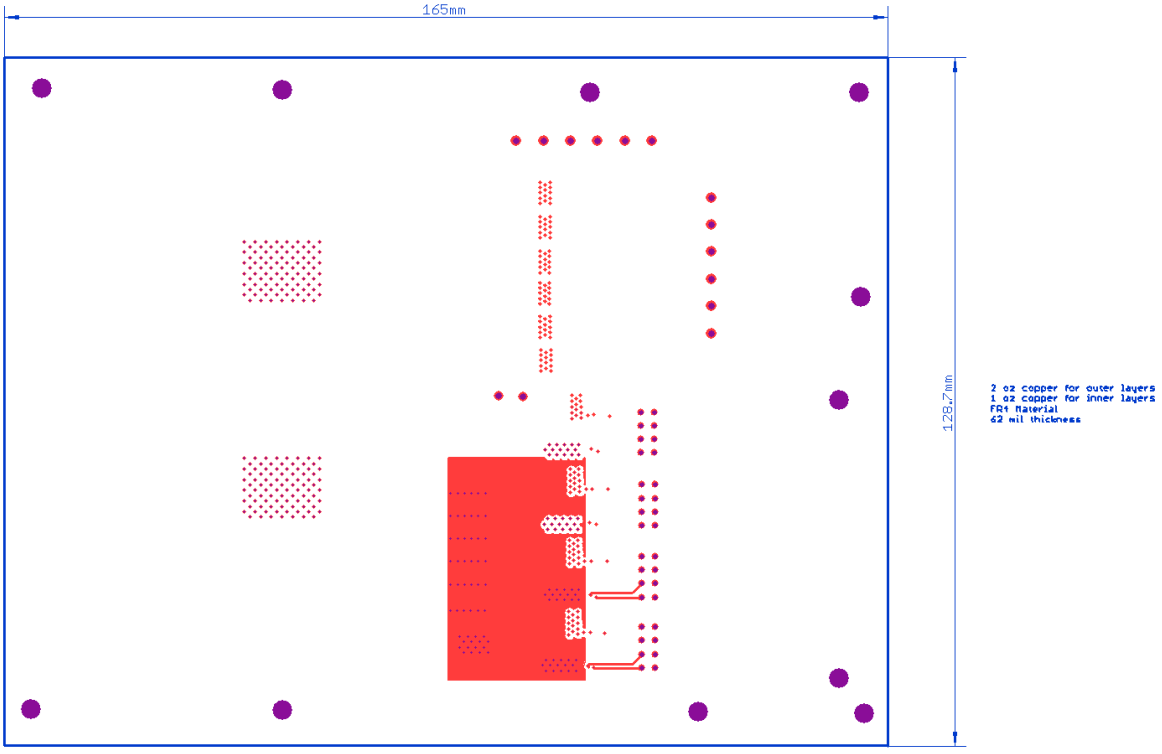


Figure D-16: Layer 3 of the synchronous full bridge rectifier for the ICN converter.

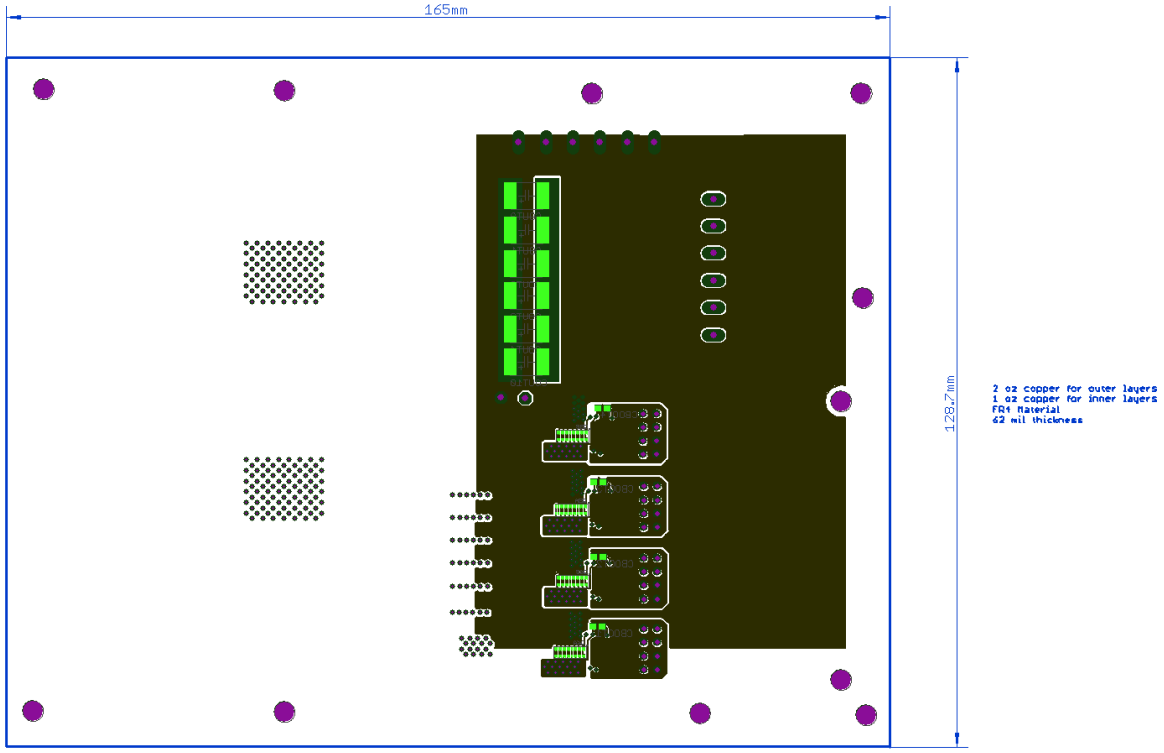


Figure D-17: Layer 4 of the synchronous full bridge rectifier for the ICN converter.

D.4 Fully Integrated ICN Converter Prototype

This set of layout files contains the fully integrated prototype of the ICN converter of Figure 2-27. The board was ordered from Imagineering using an 8 layer design with 2 oz. copper on the outer layers, 4 oz copper on the inner layers and ENIG surface finish. The board material is FR4 with red soldermask and white silkscreen. The layout for each of the 8 layers can be found in Figure D-18 through Figure D-25. The coupled inductor and resonant inductor from this board were used in the final prototype of Figure 2-25.

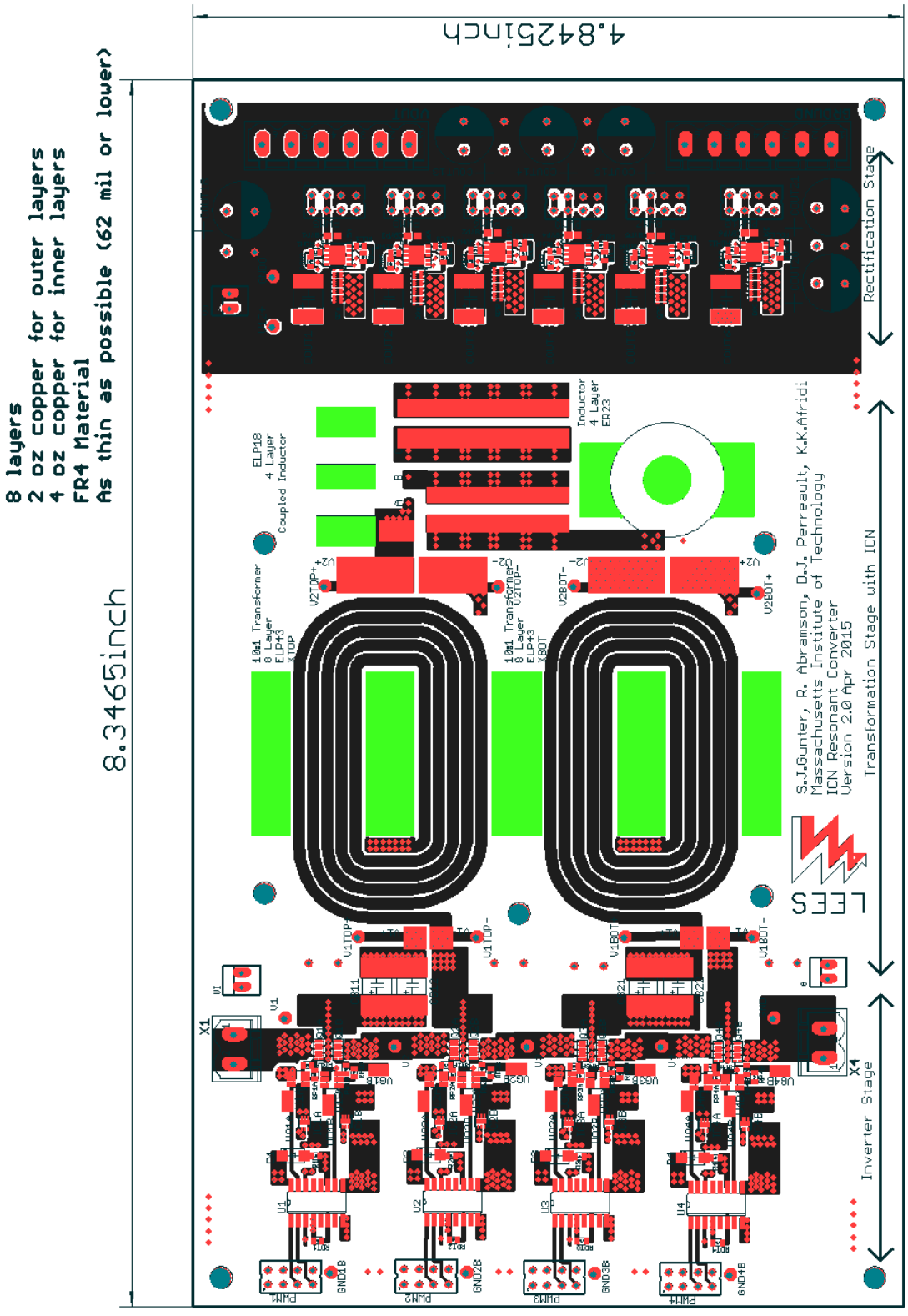


Figure D-18: Layer 1 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

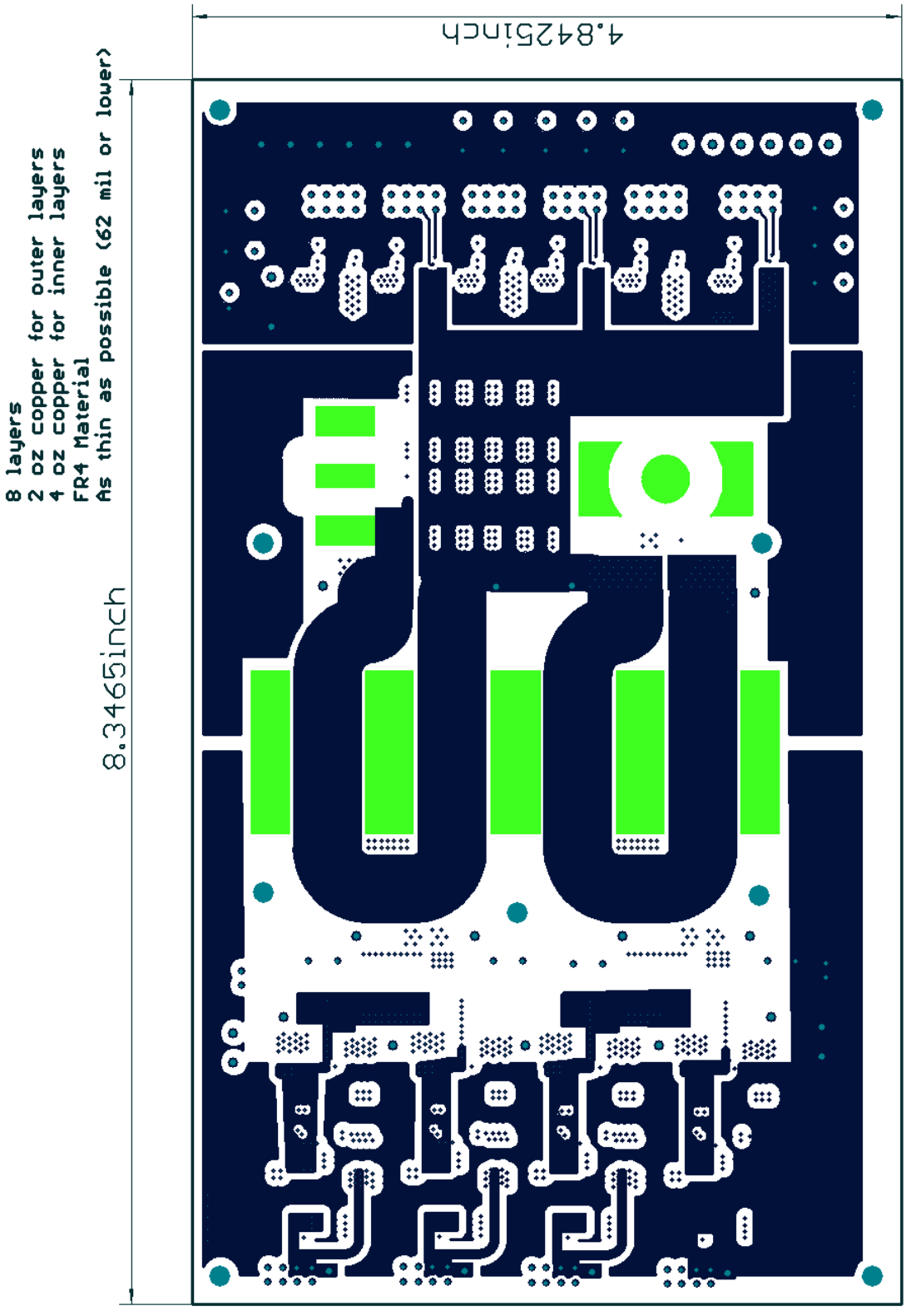


Figure D-19: Layer 2 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

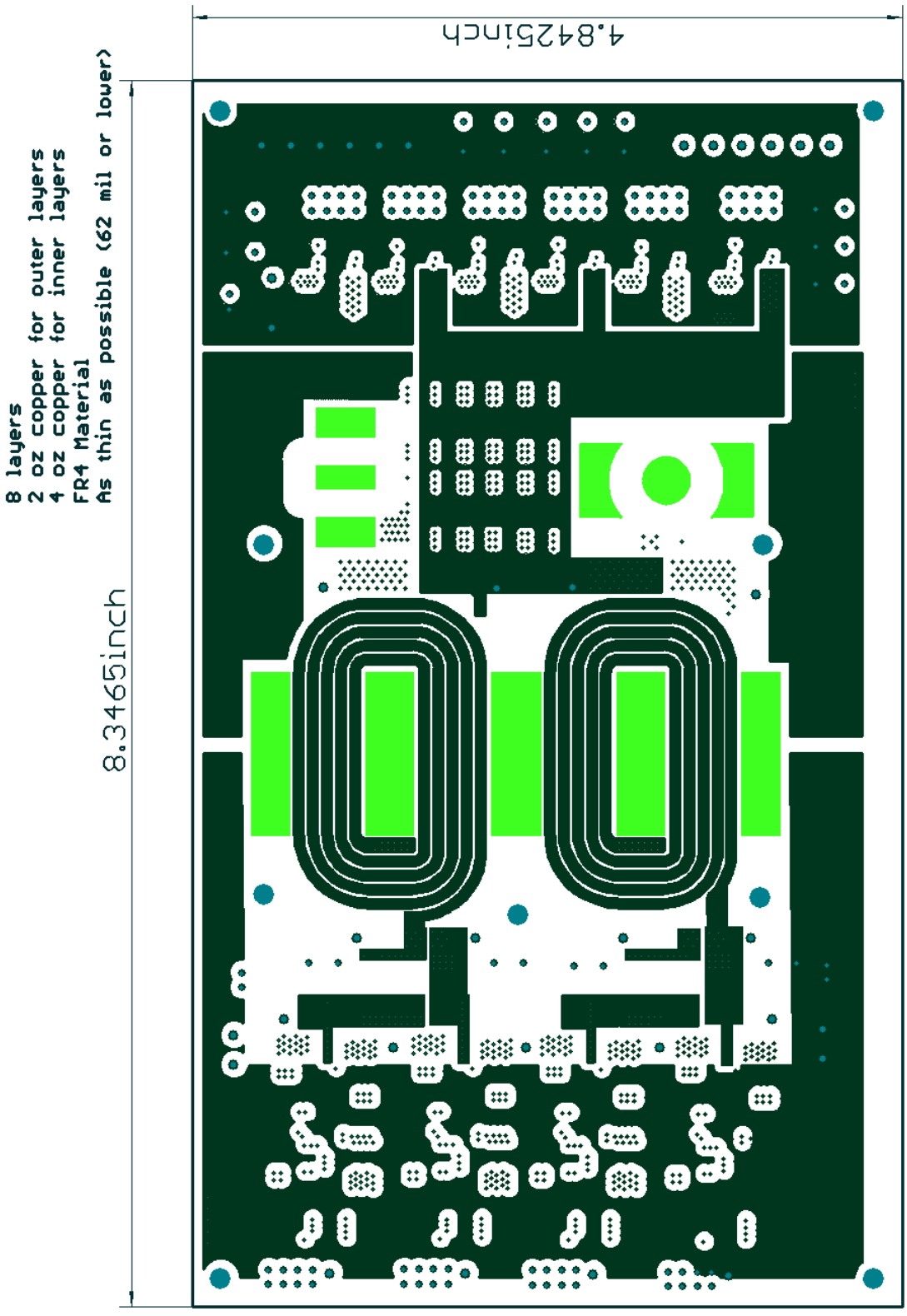


Figure D-20: Layer 3 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

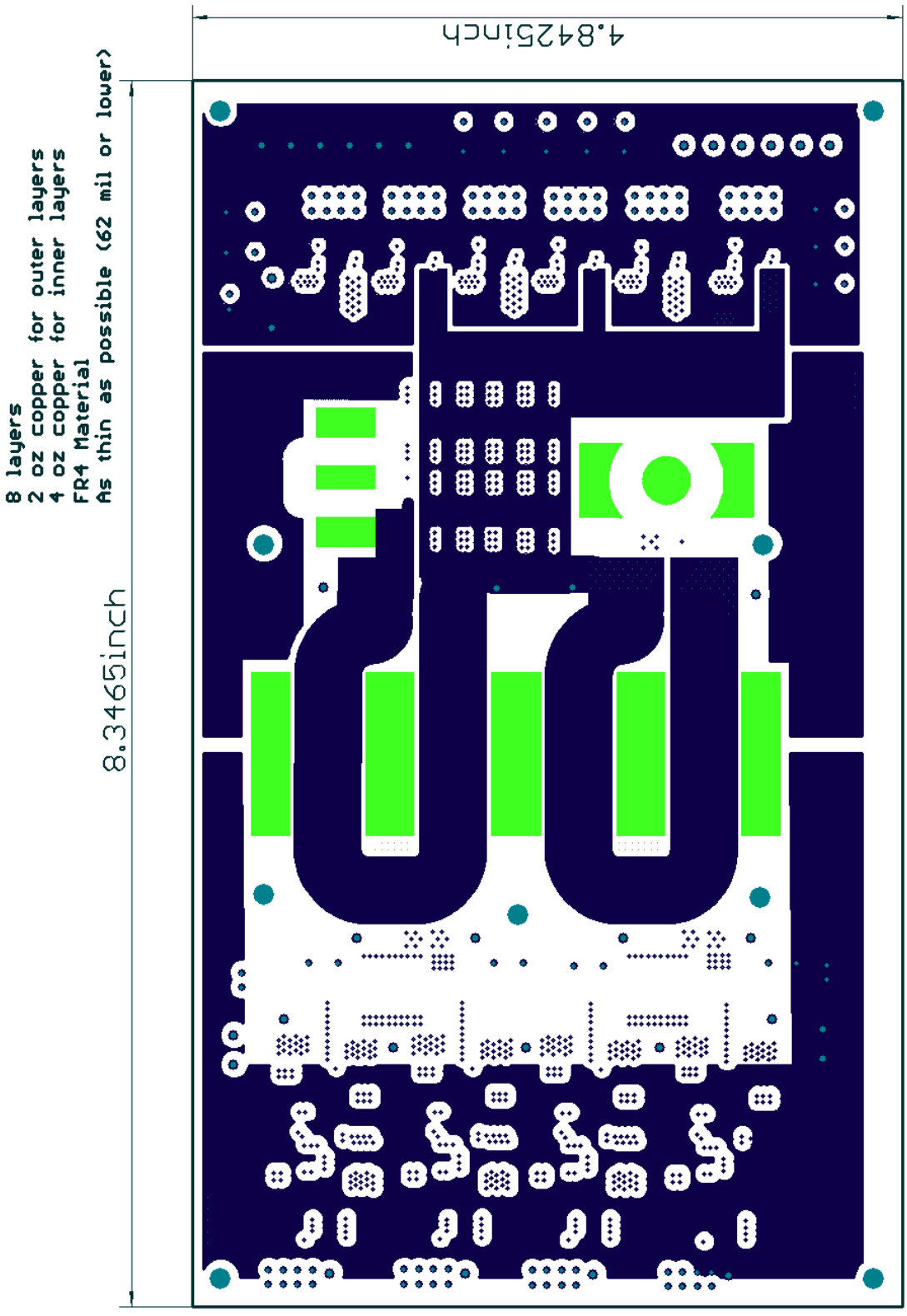


Figure D-21: Layer 4 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

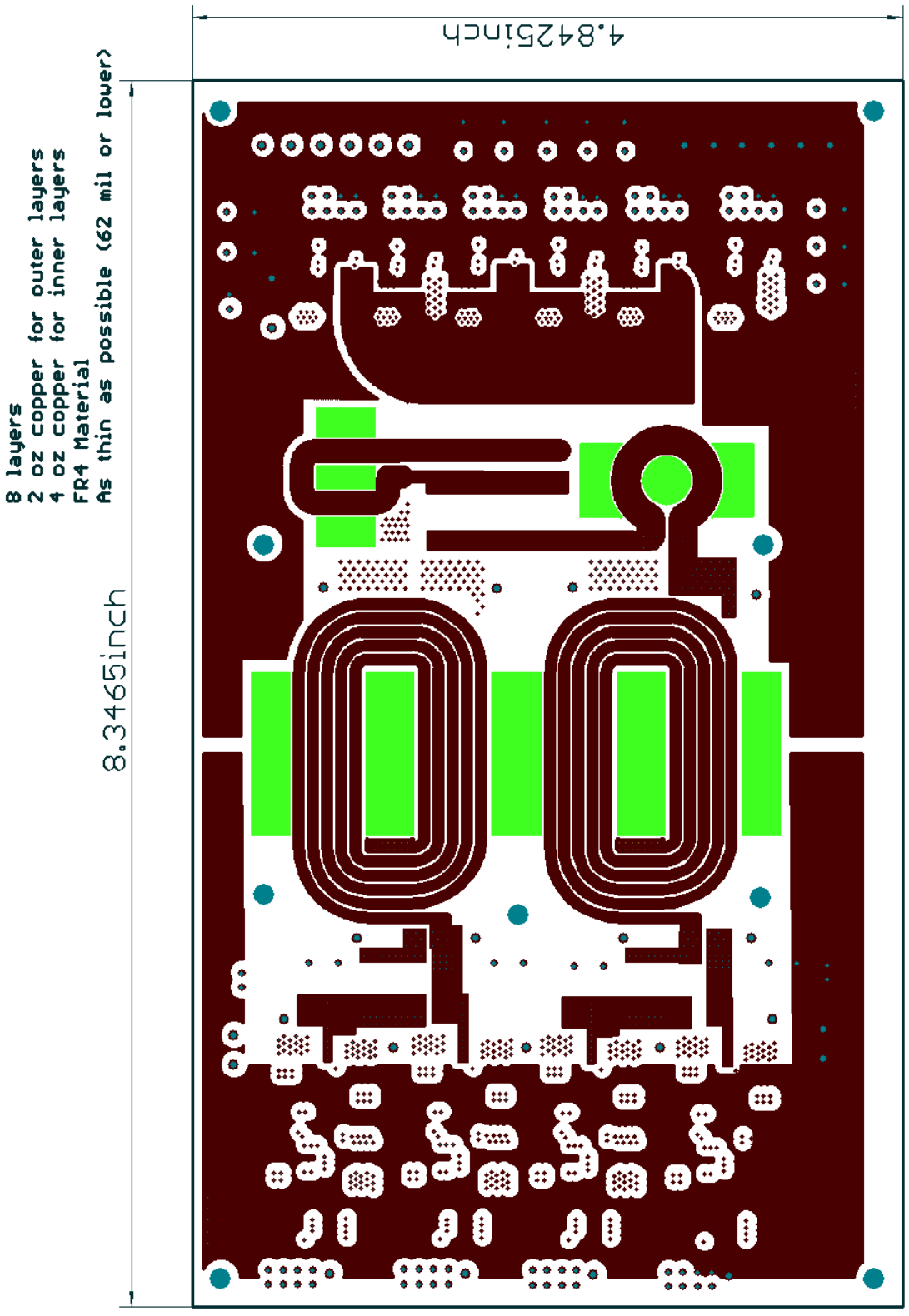


Figure D-22: Layer 5 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

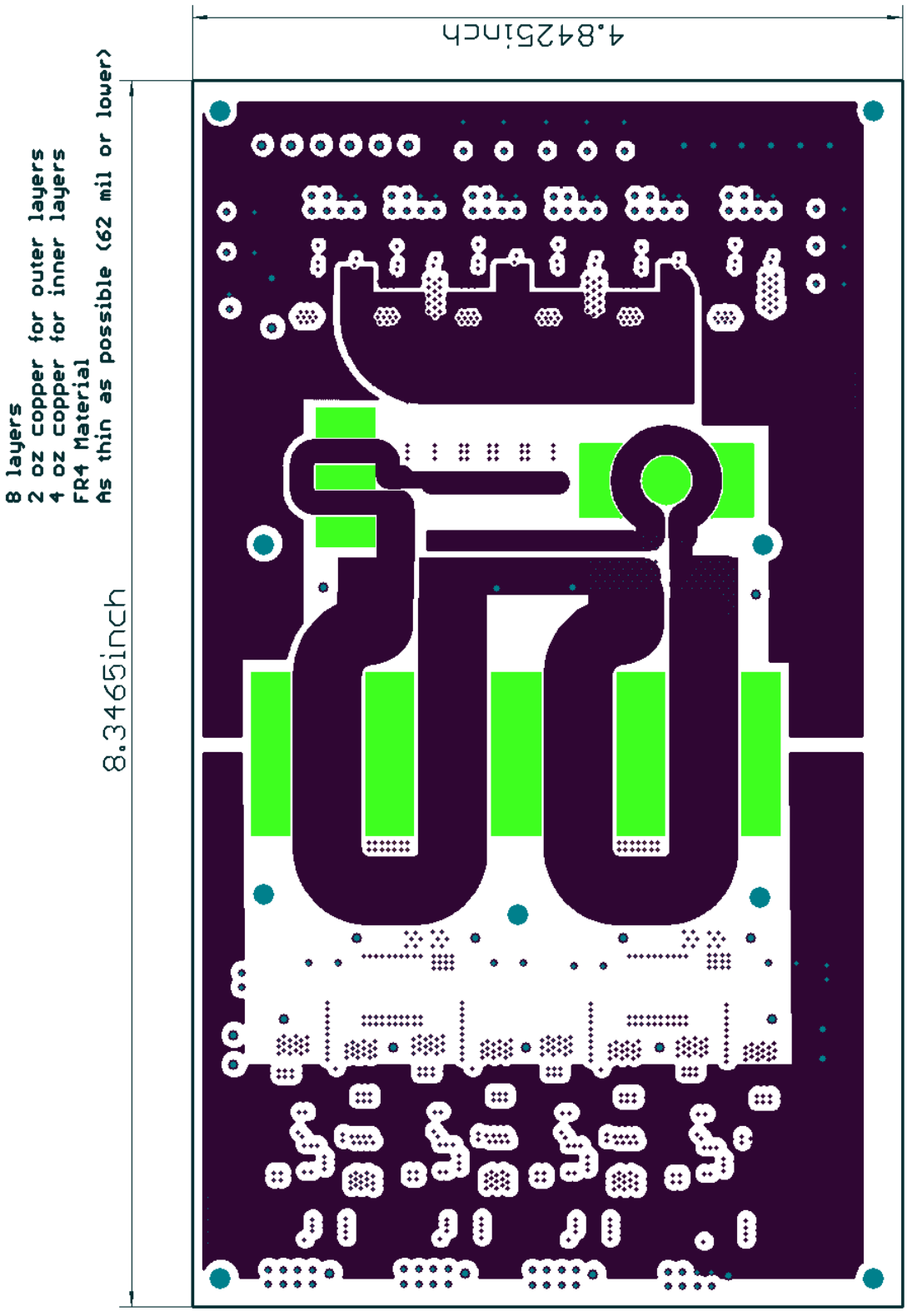


Figure D-23: Layer 6 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

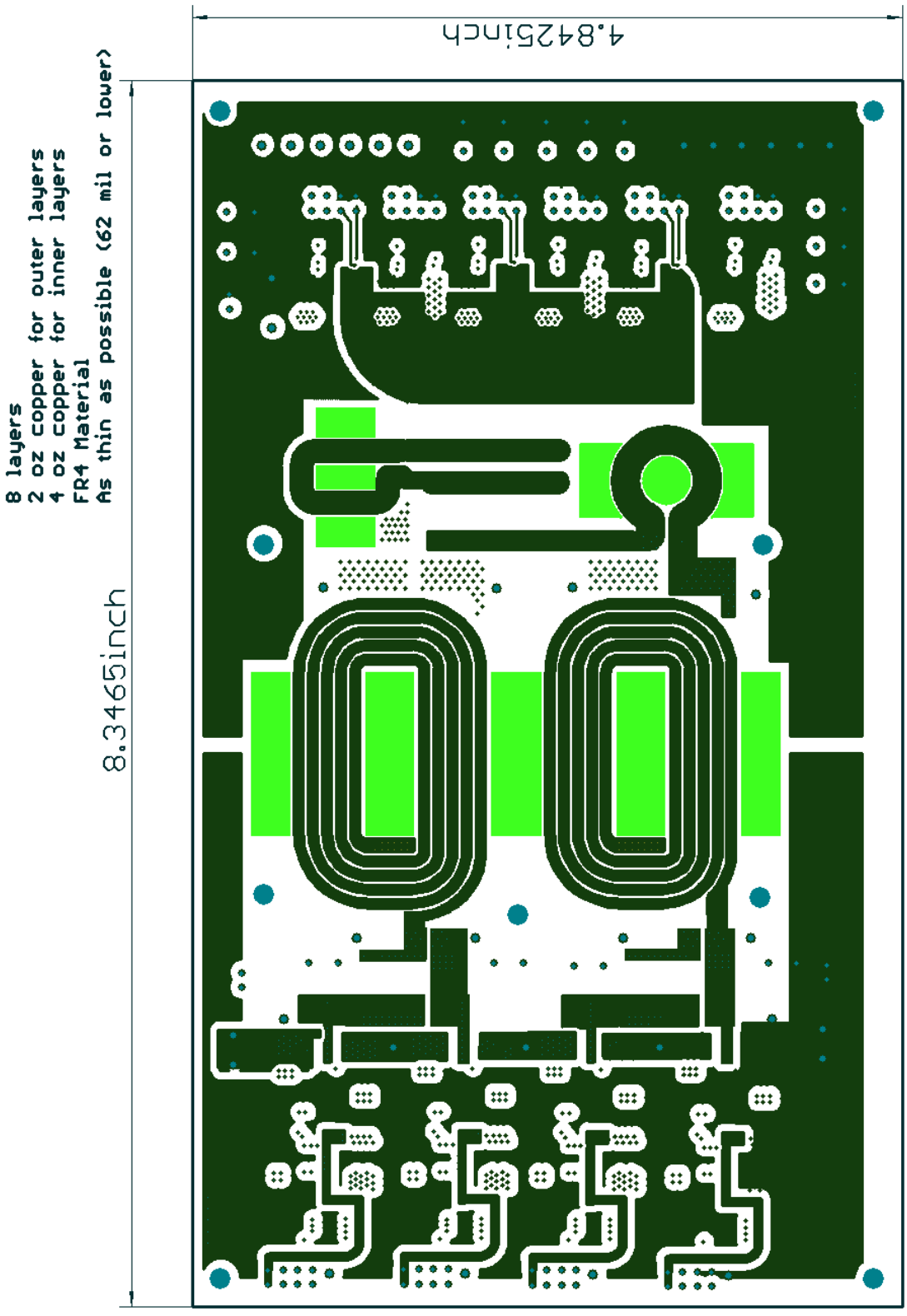


Figure D-24: Layer 7 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

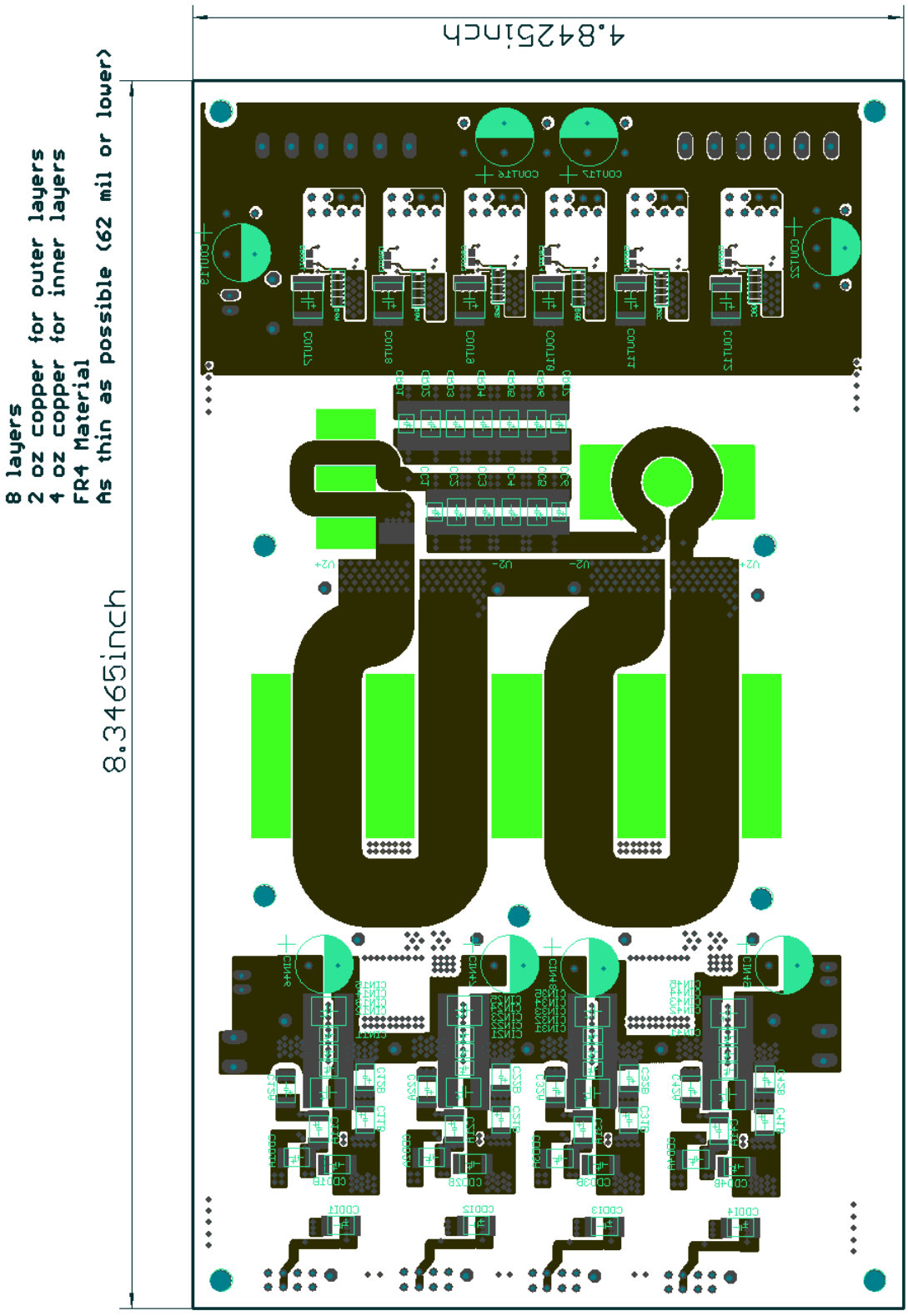


Figure D-25: Layer 8 of the fully integrated ICN converter board. The bright green indicates the locations of the cutouts for the magnetic cores.

D.5 GaN-based and Si-based Reconfigurable Double Stacked Active Bridge Prototypes

This set of layout files contains the fully integrated prototypes for the GaN-based and the Si-based reconfigurable double stacked active bridge converters of Figure 5-13 and Figure 5-14. The boards were ordered from Gold Phoenix Printed Circuit Board Co., Ltd using an 8 layer design with 2 oz. copper on the outer layers, 4 oz copper on the inner layers and ENIG surface finish. The board material is FR4 with blue soldermask and white silkscreen. The layout for each of the 8 layers can be found in Figure D-26 through Figure D-33 for the GaN-based prototype and Figure D-34 through Figure D-41 for the Si-based prototype.

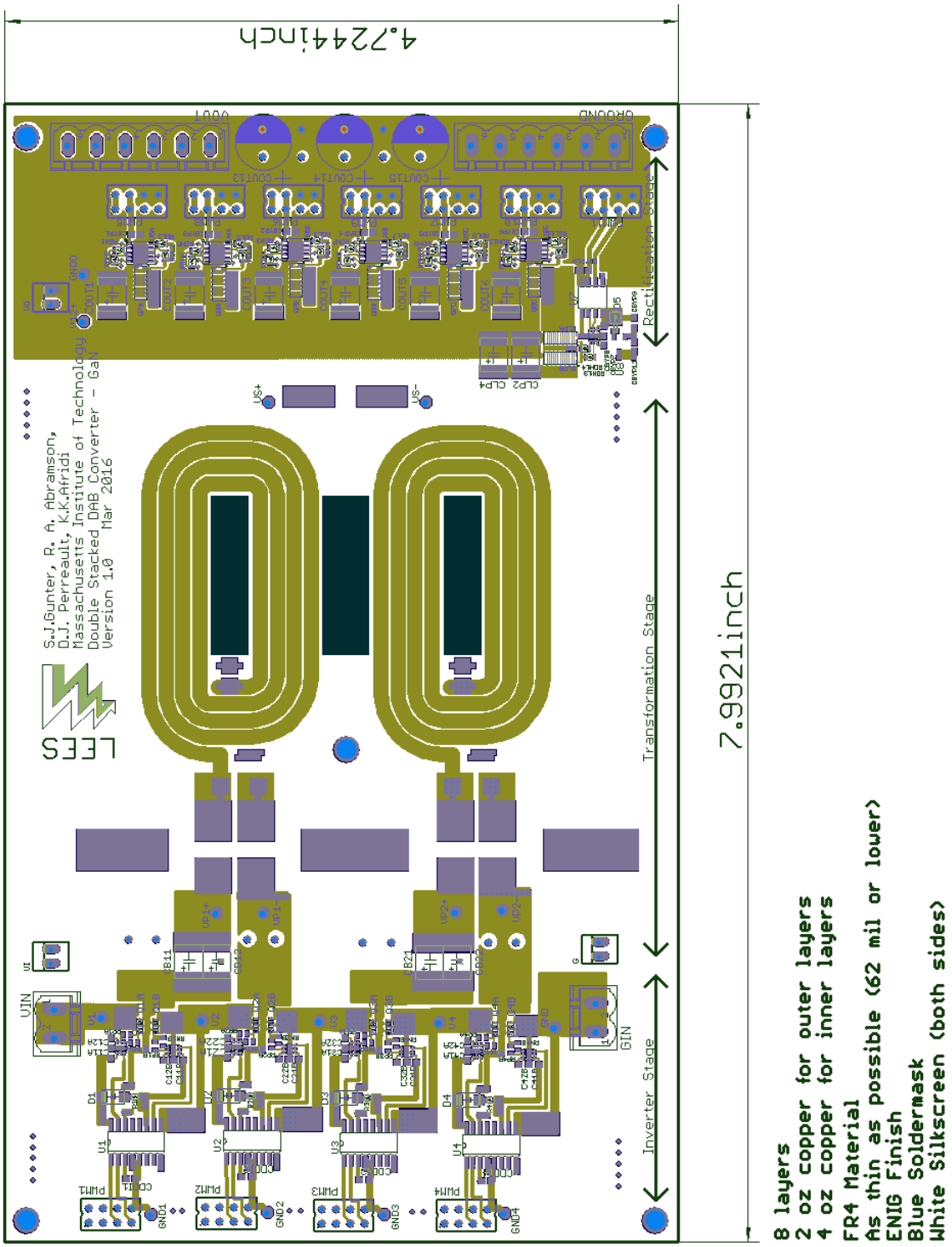


Figure D-26: Layer 1 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

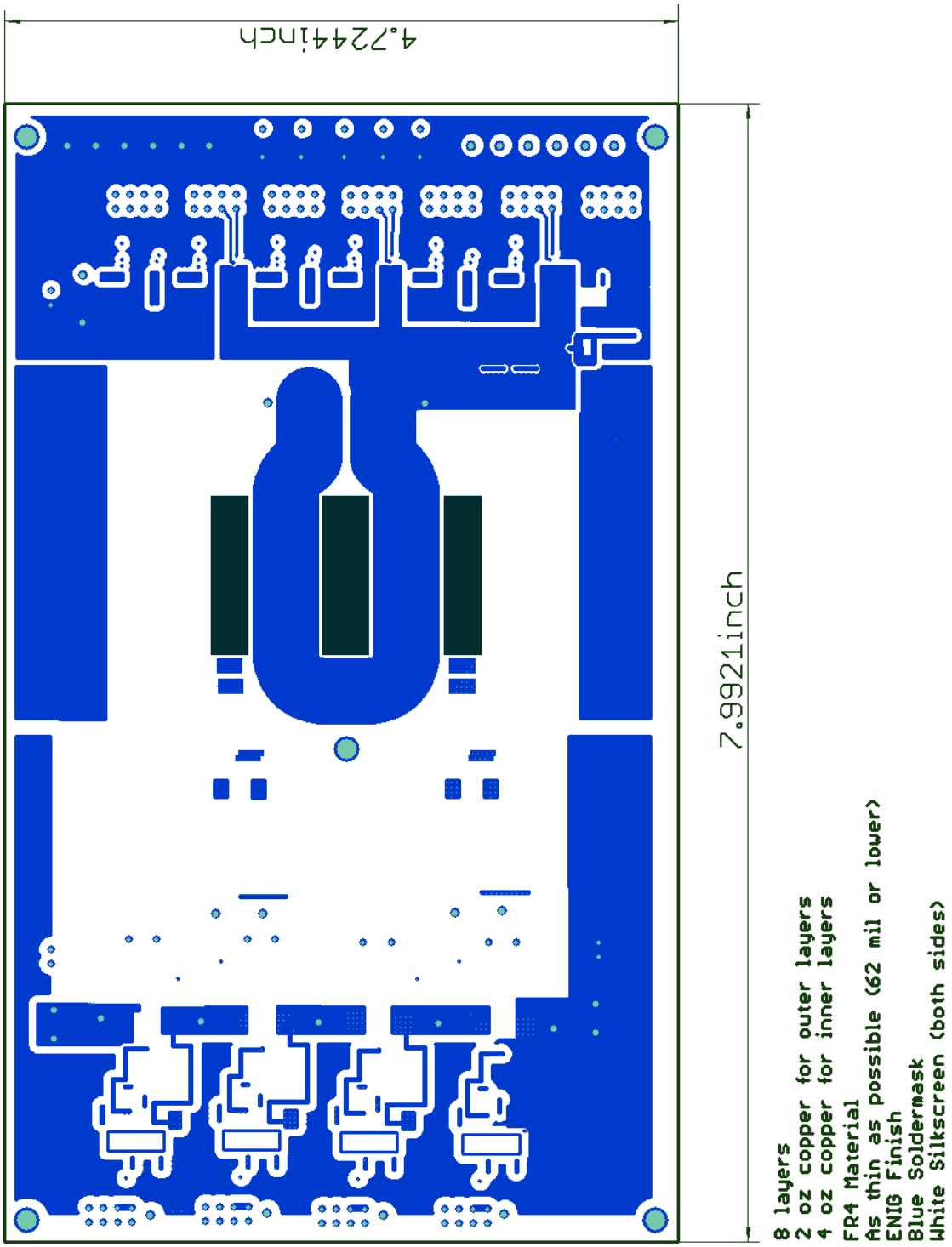


Figure D-27: Layer 2 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

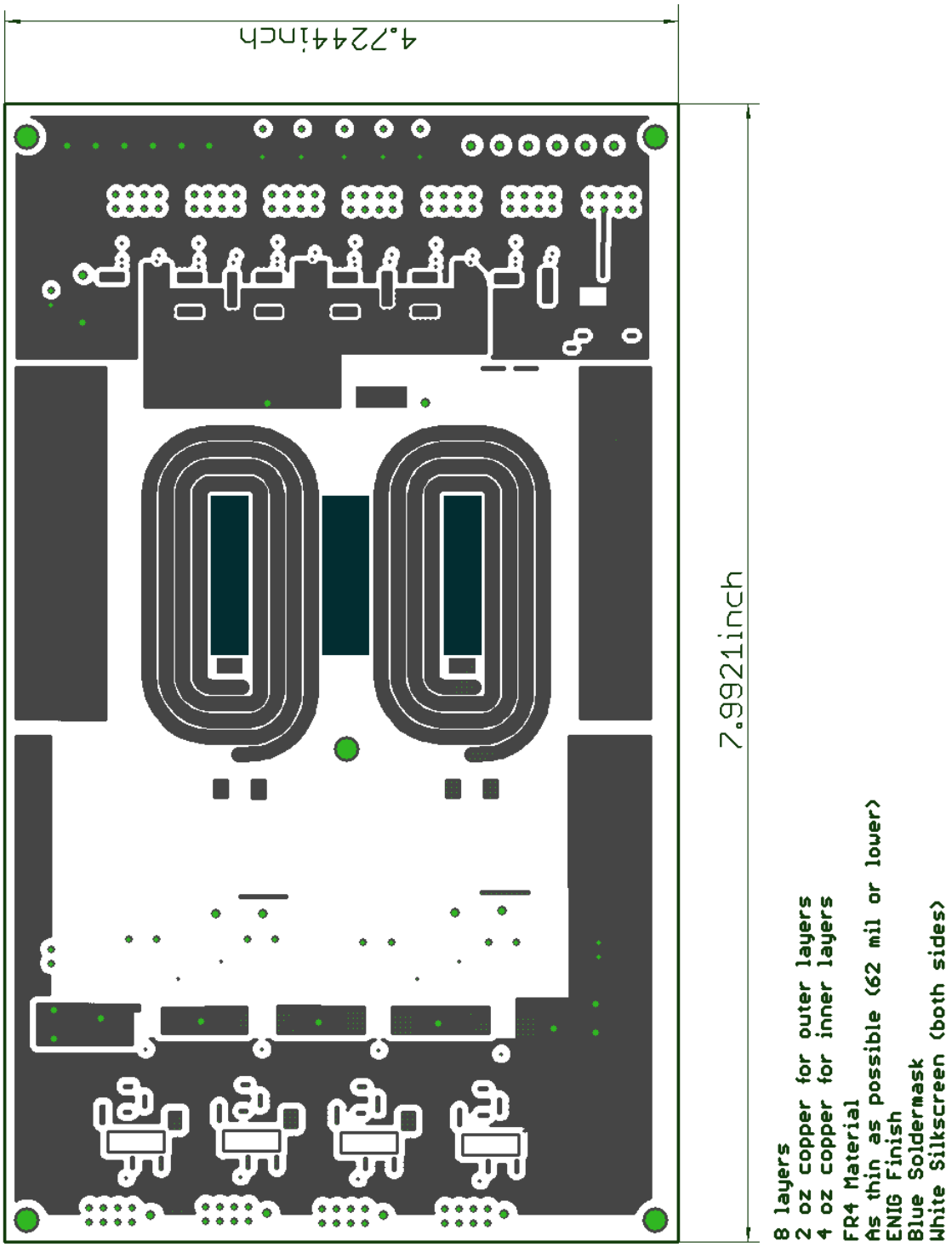


Figure D-28: Layer 3 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

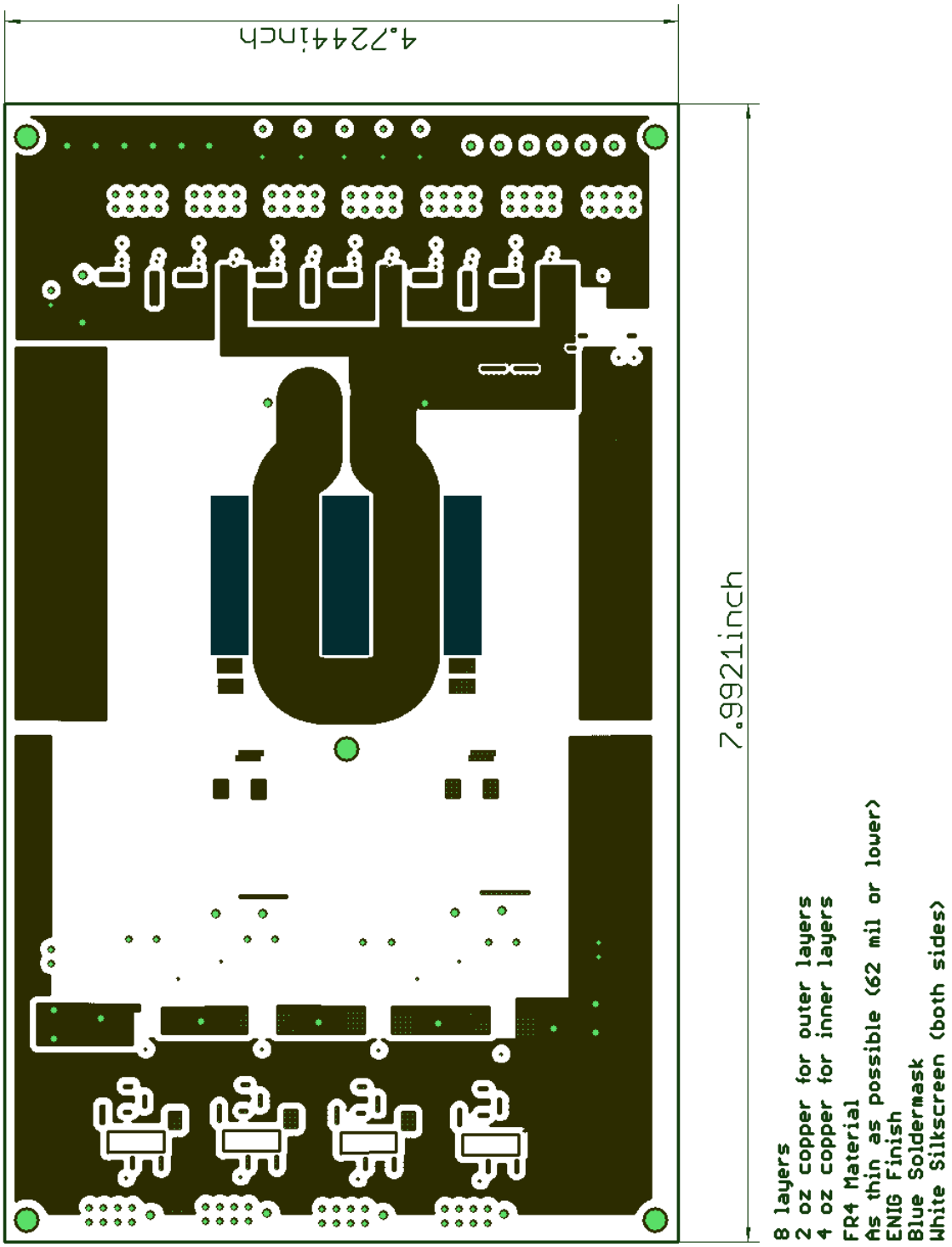


Figure D-29: Layer 4 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

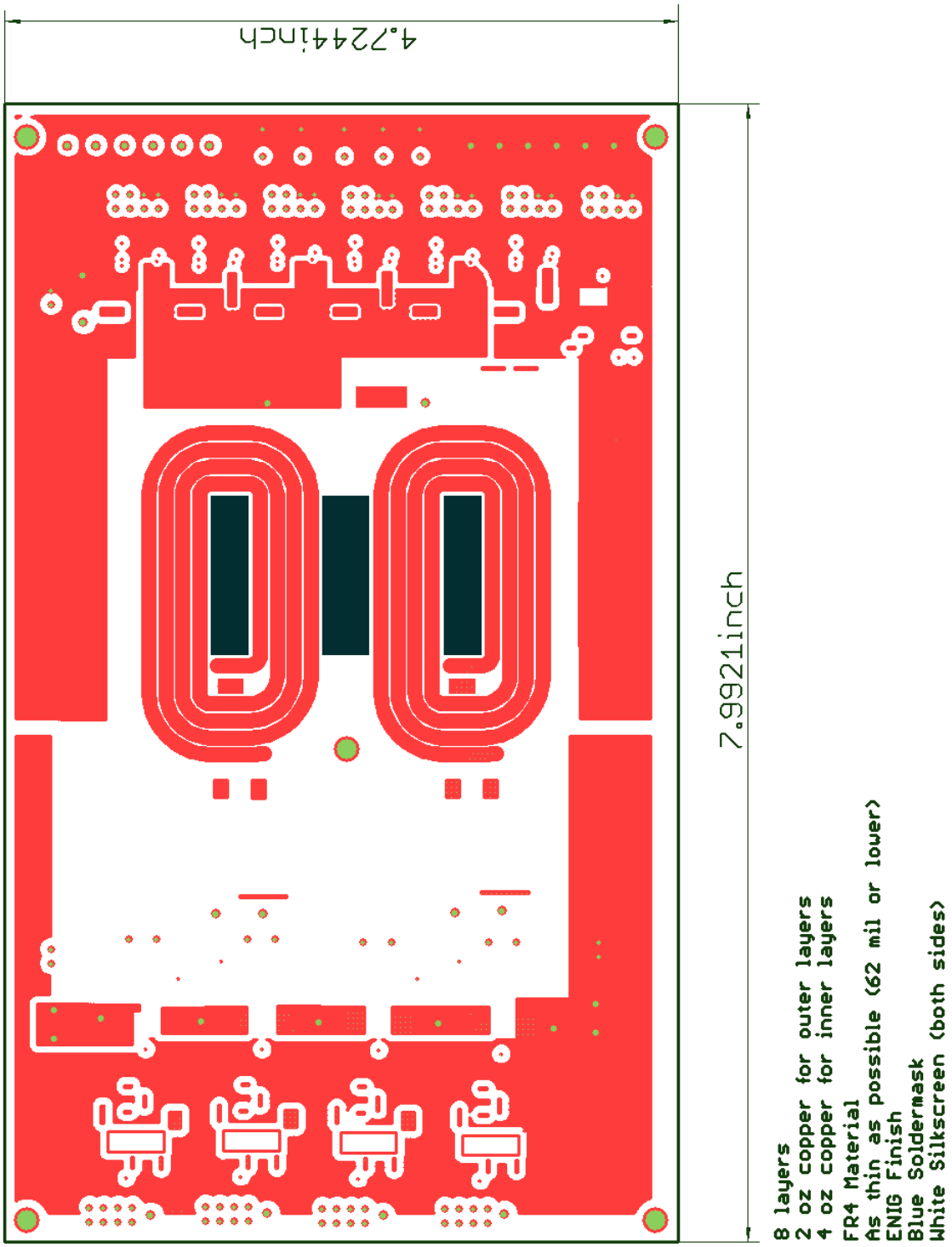


Figure D-30: Layer 5 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

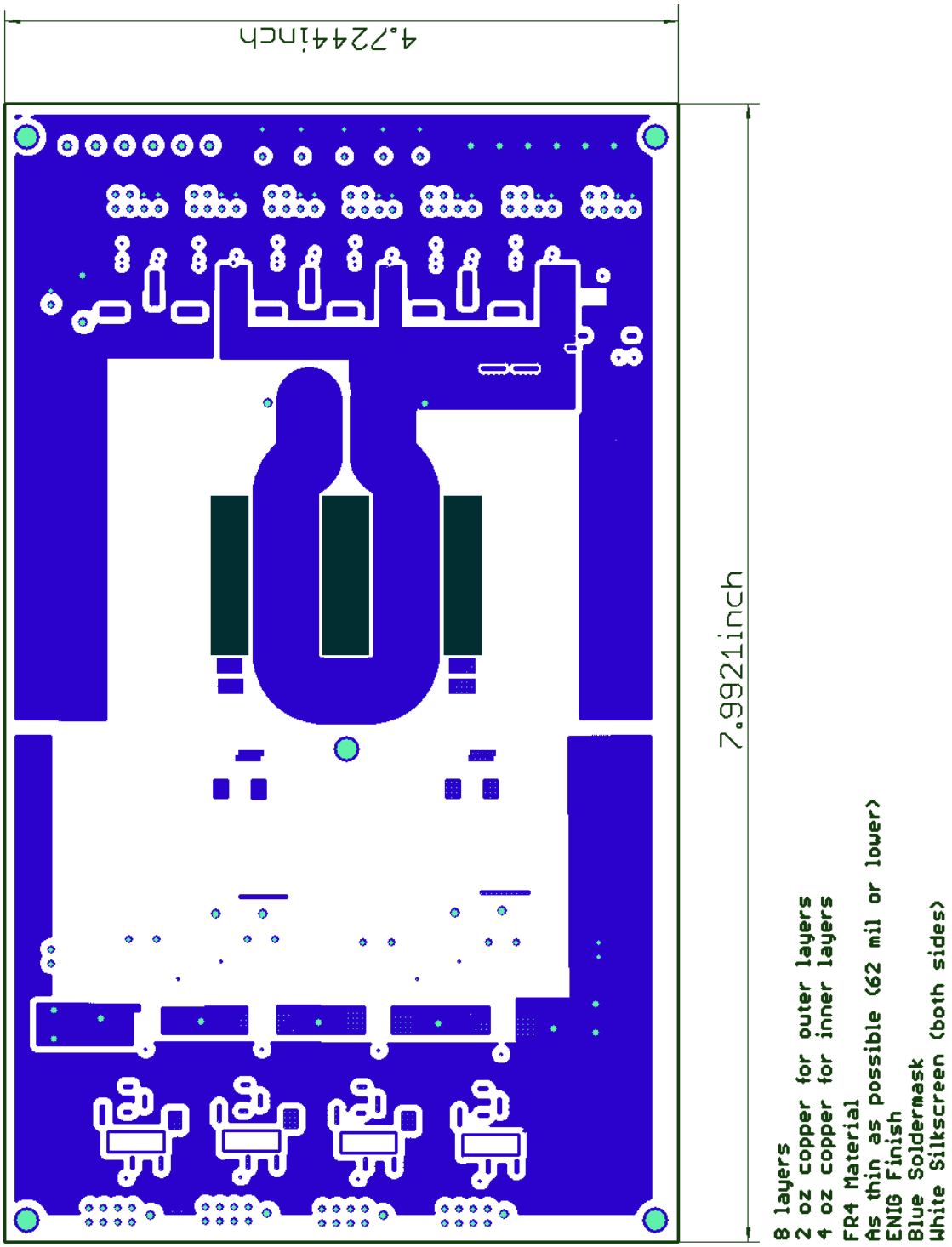


Figure D-31: Layer 6 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

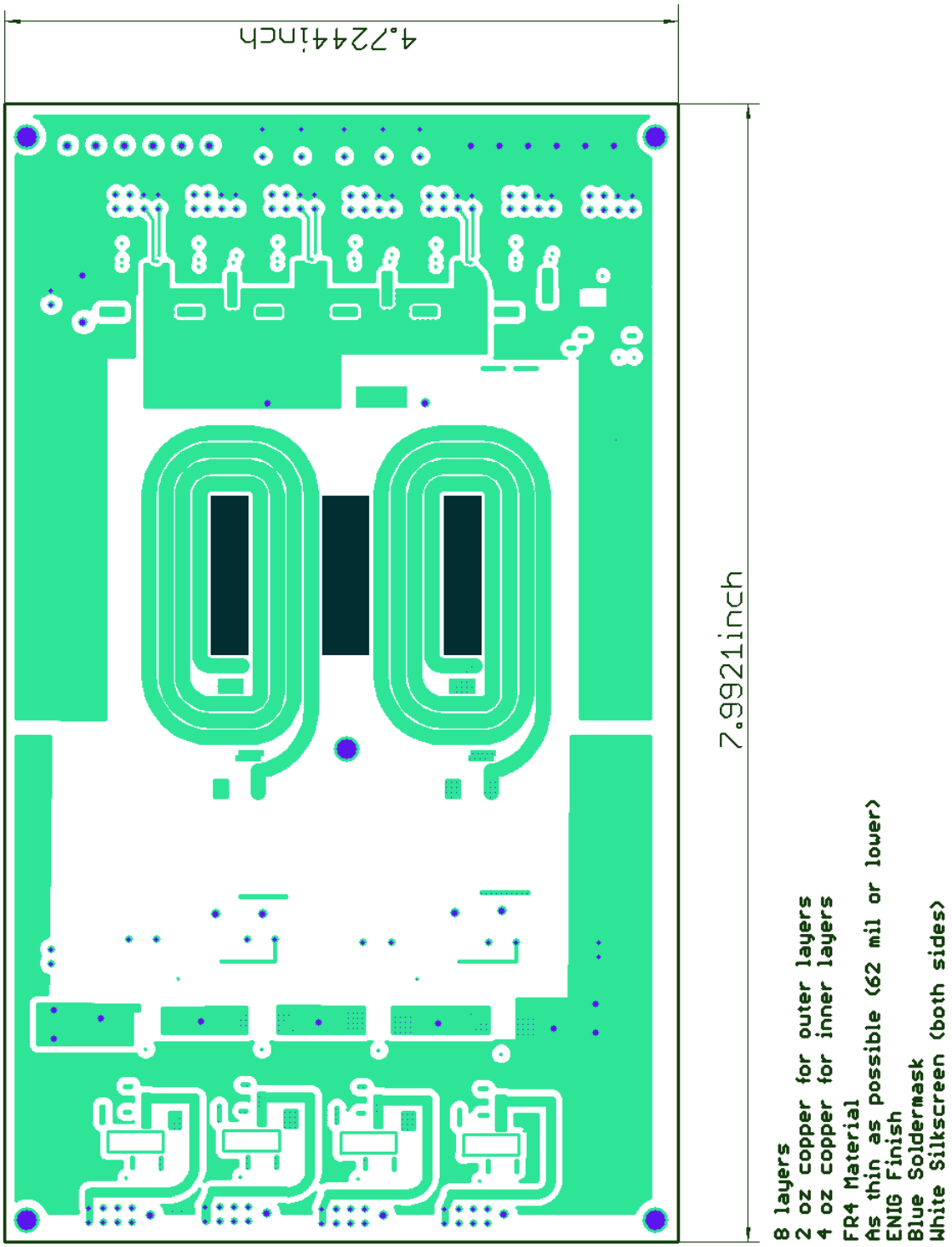


Figure D-32: Layer 7 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

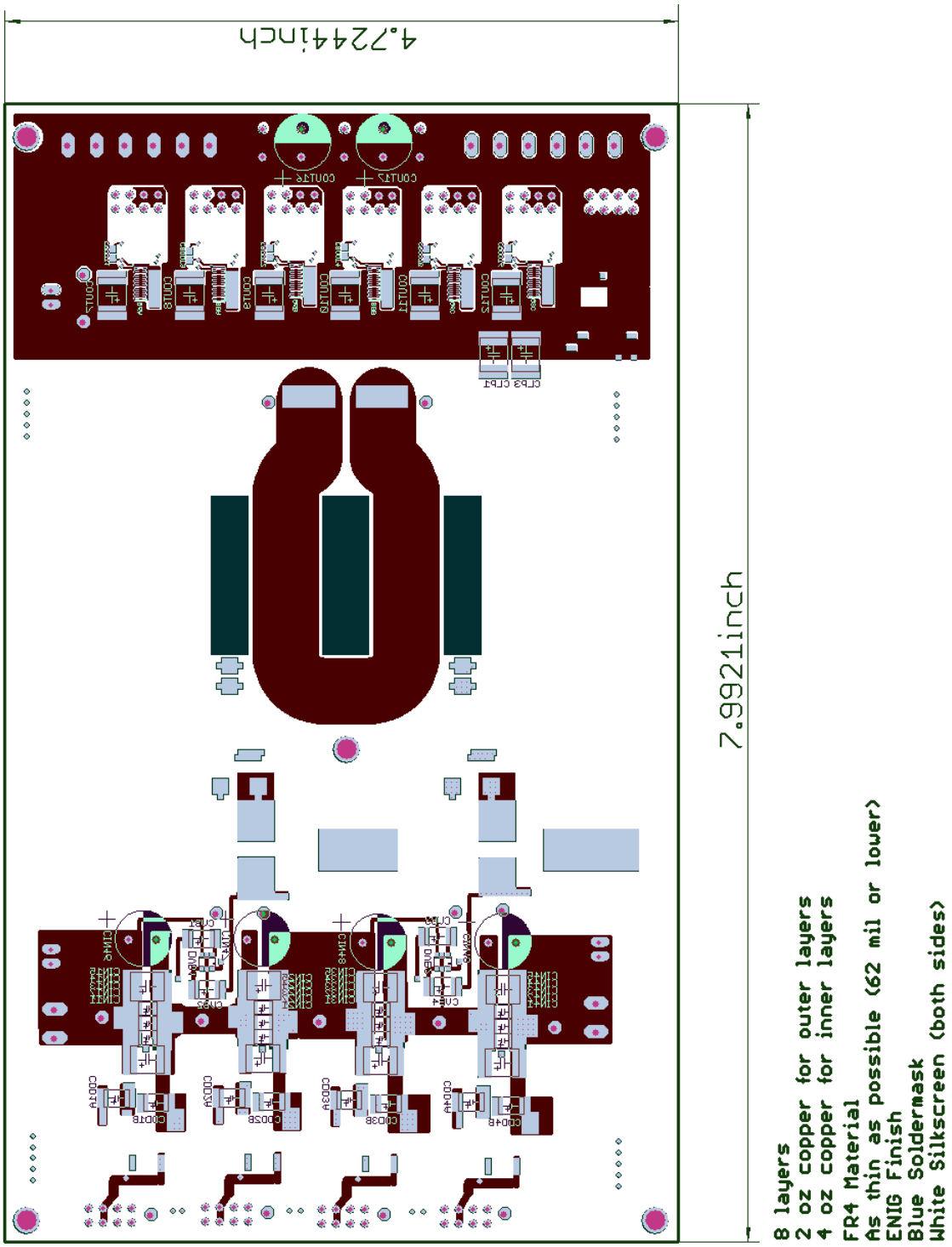


Figure D-33: Layer 8 of the GaN-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

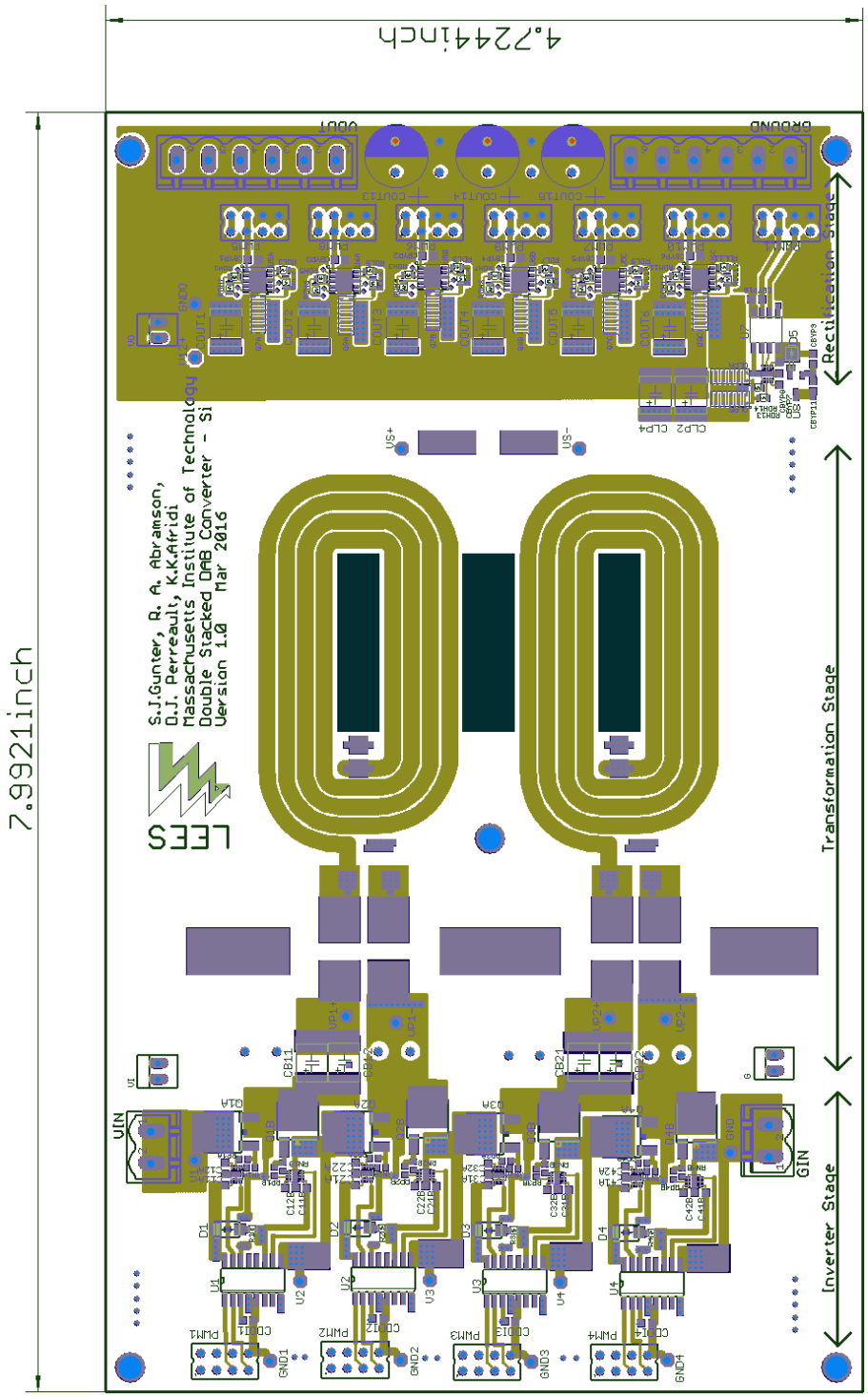


Figure D-34: Layer 1 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

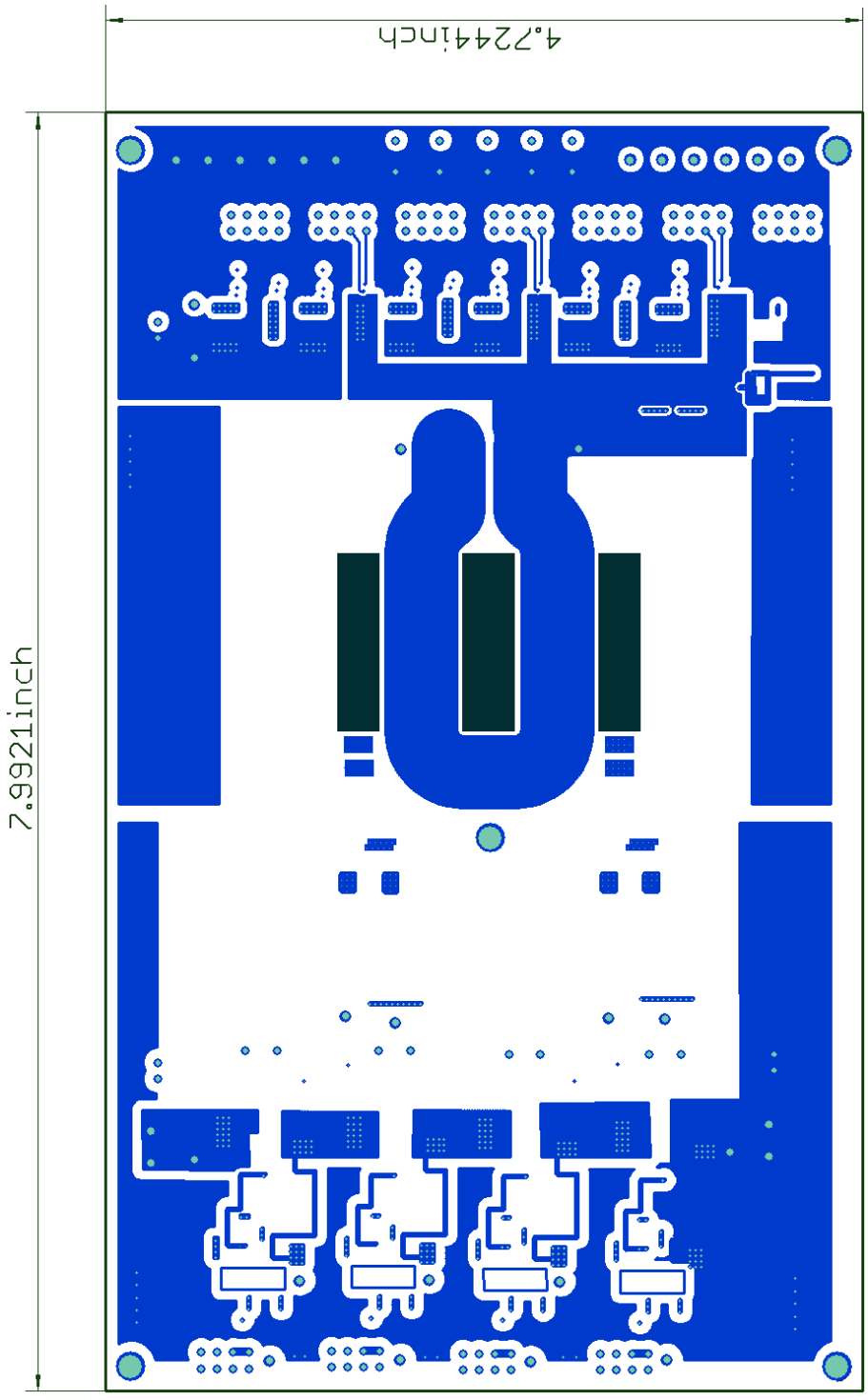


Figure D-35: Layer 2 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

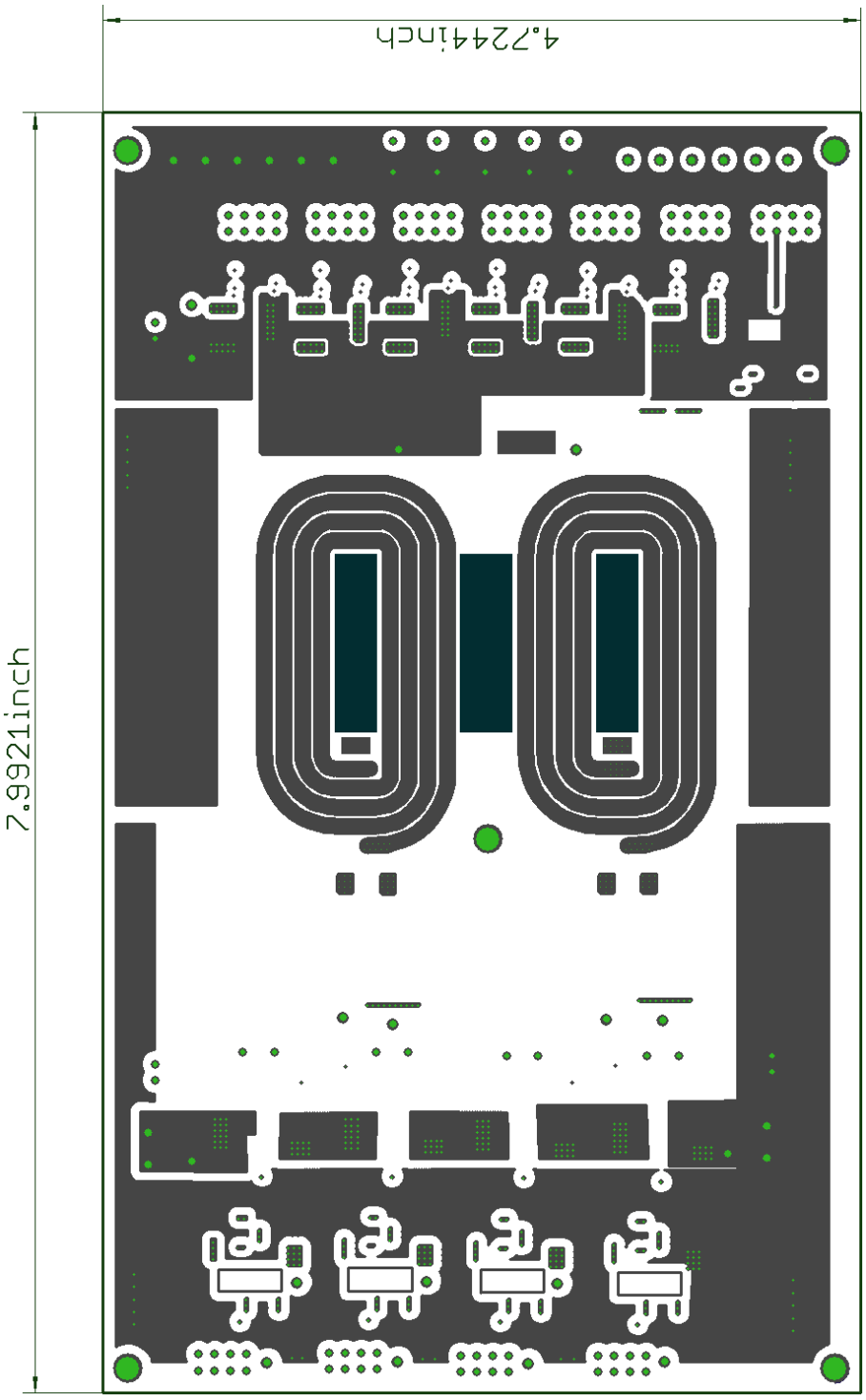


Figure D-36: Layer 3 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

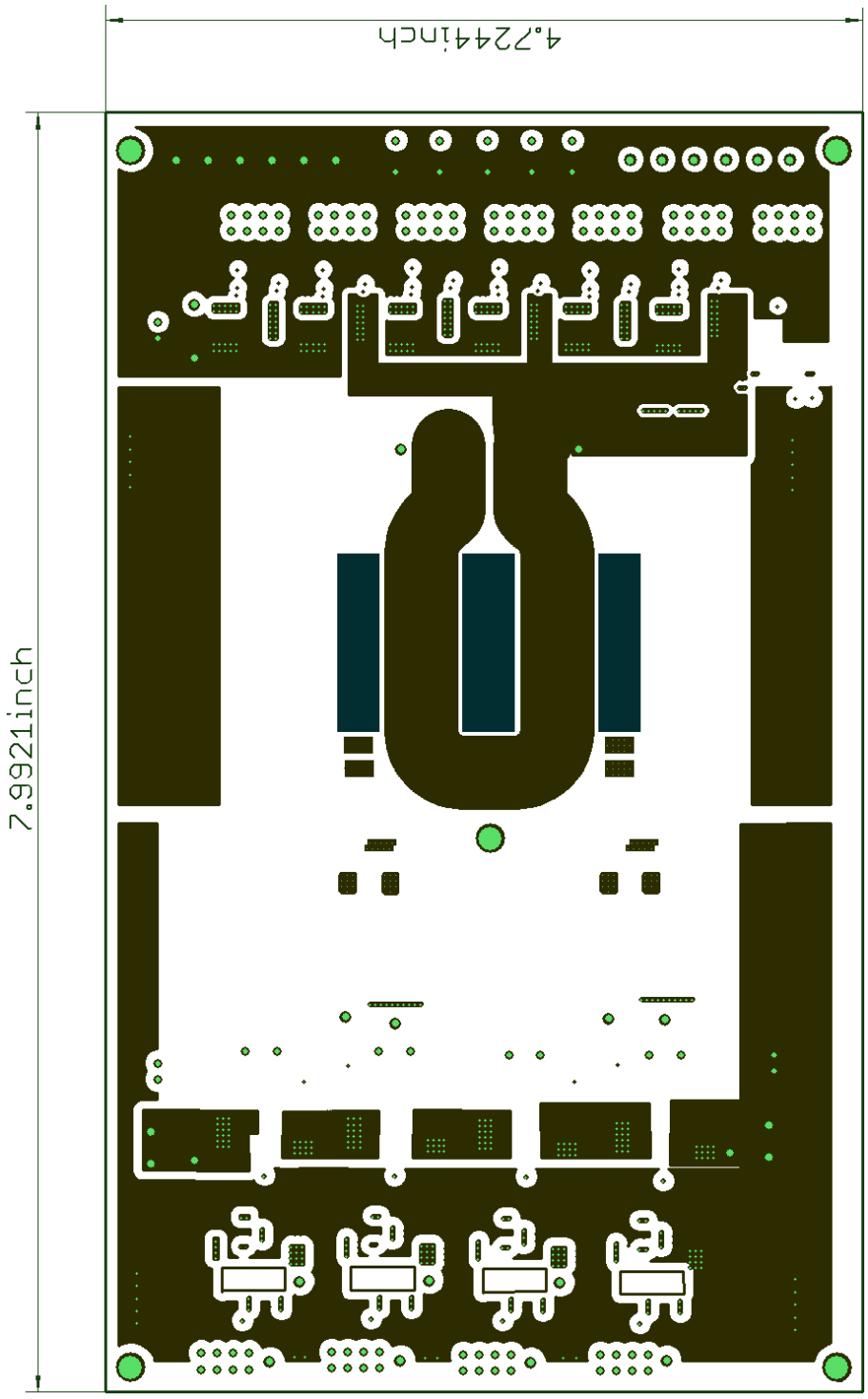


Figure D-37: Layer 4 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

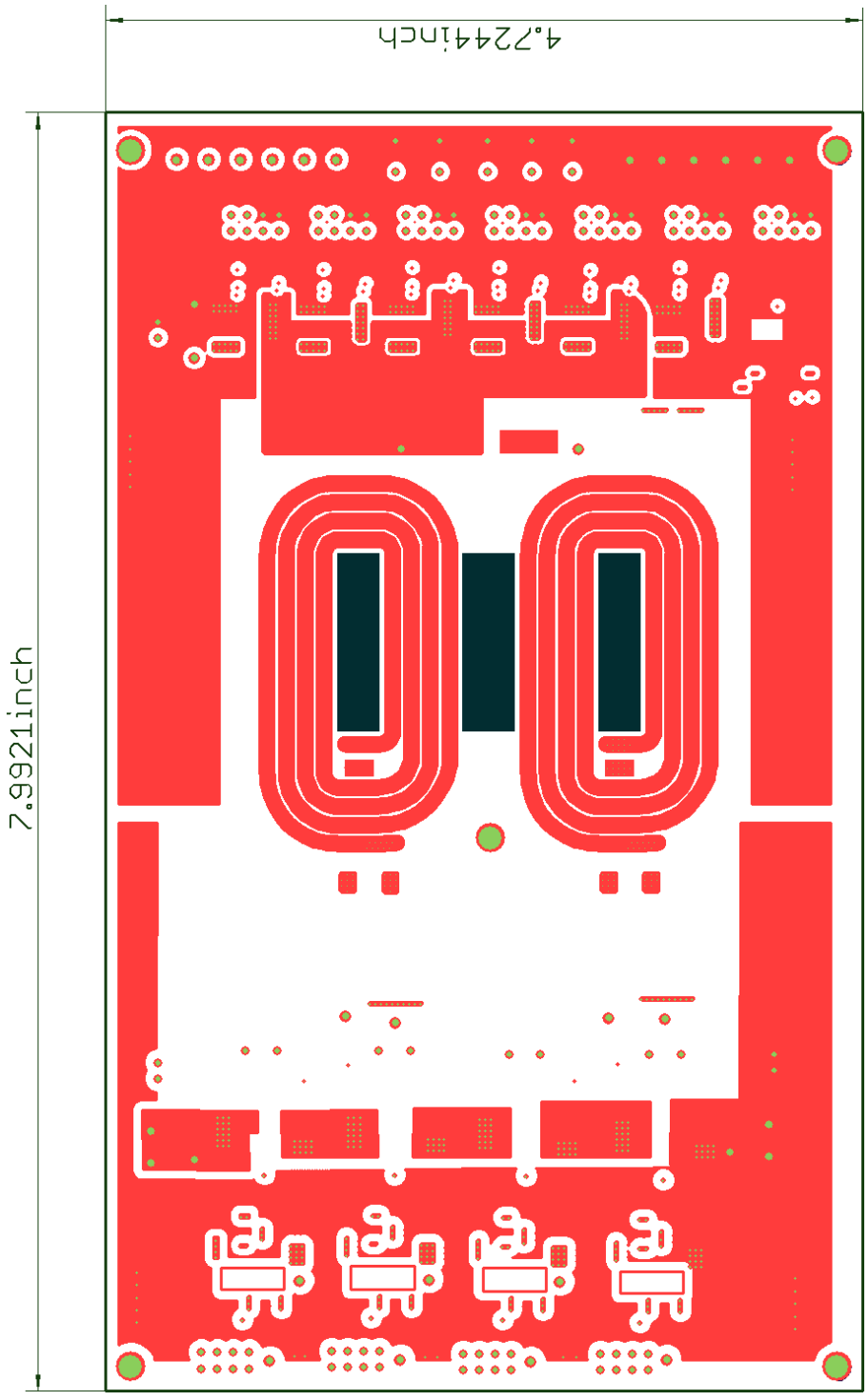


Figure D-38: Layer 5 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

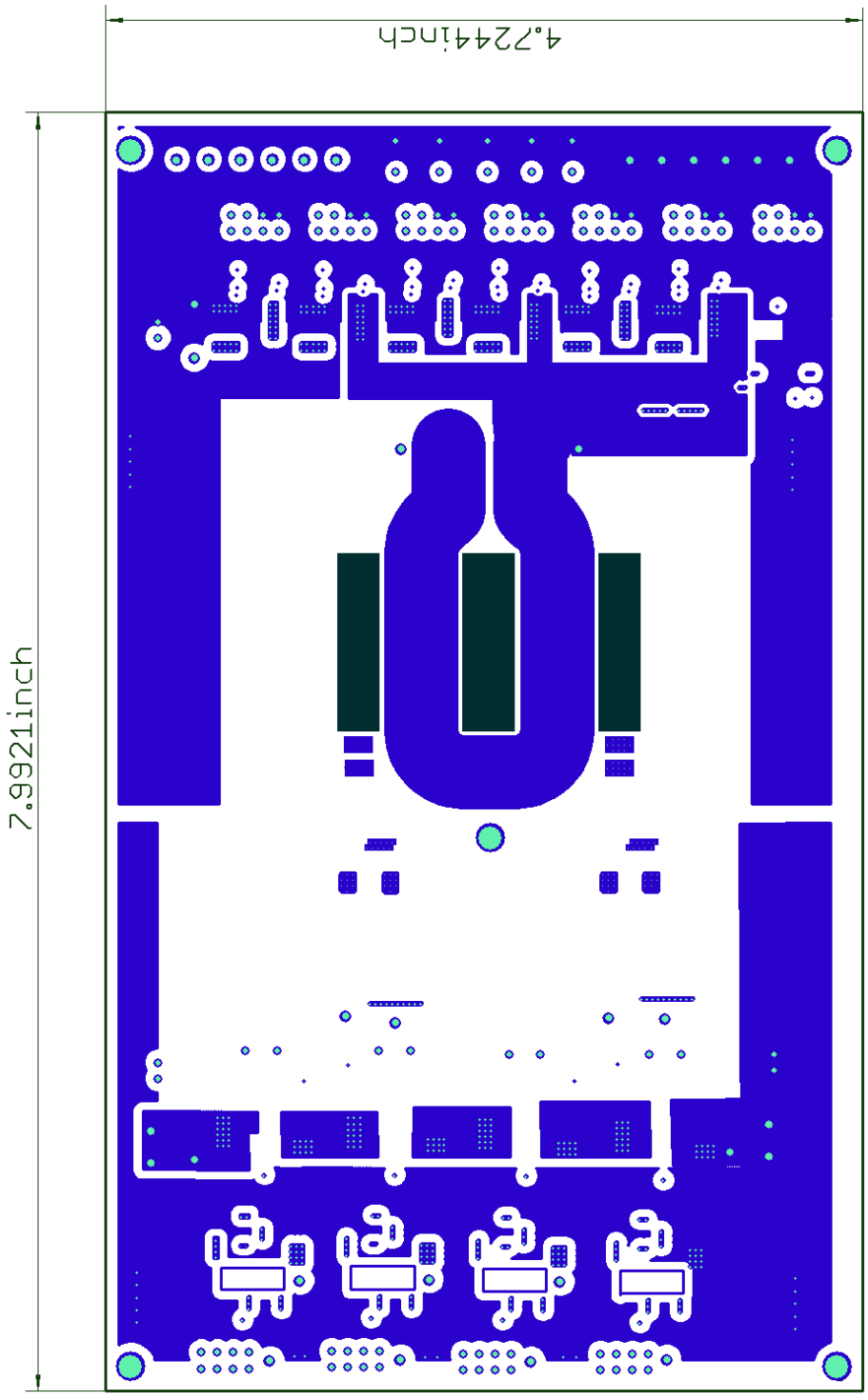


Figure D-39: Layer 6 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

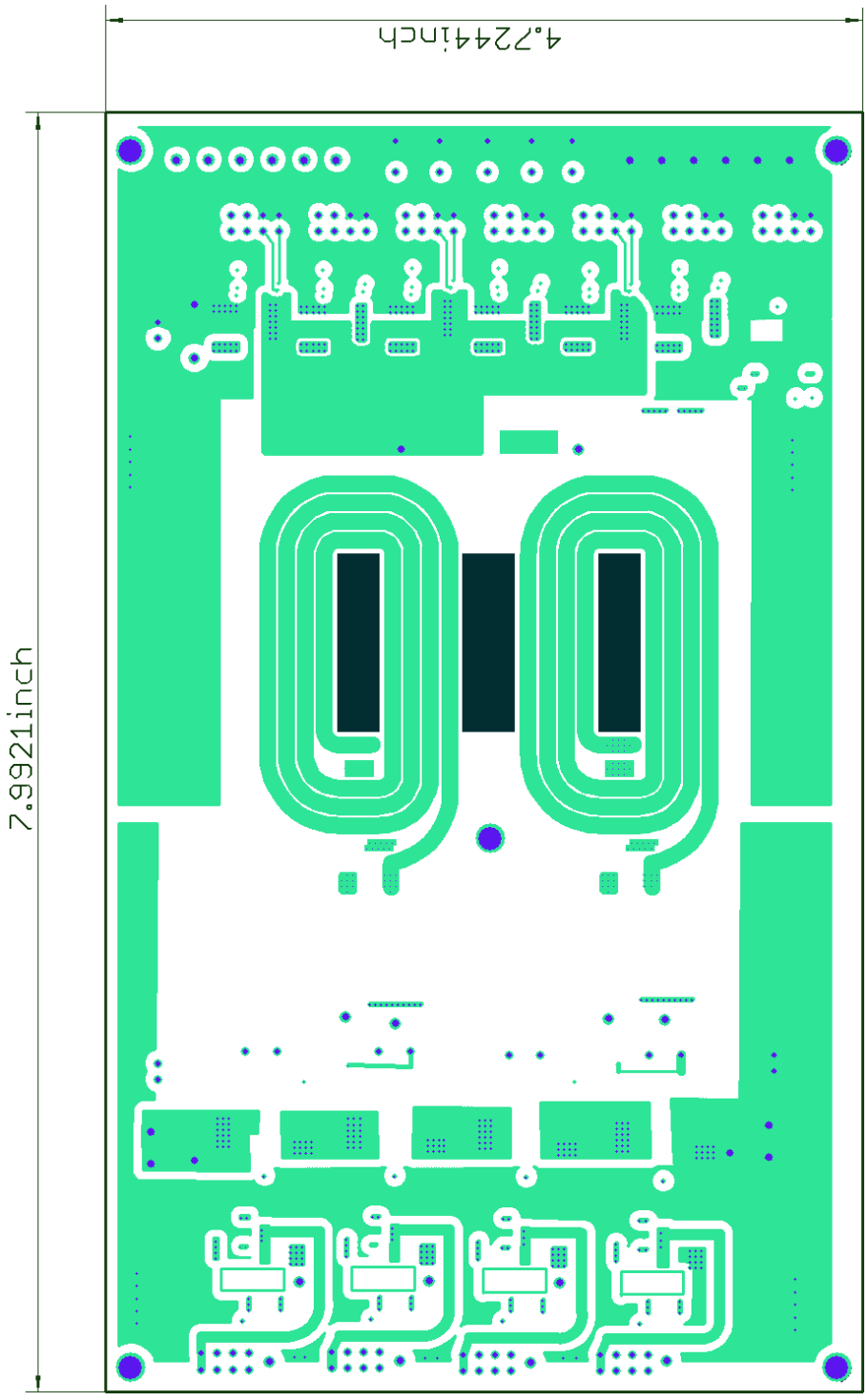


Figure D-40: Layer 7 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

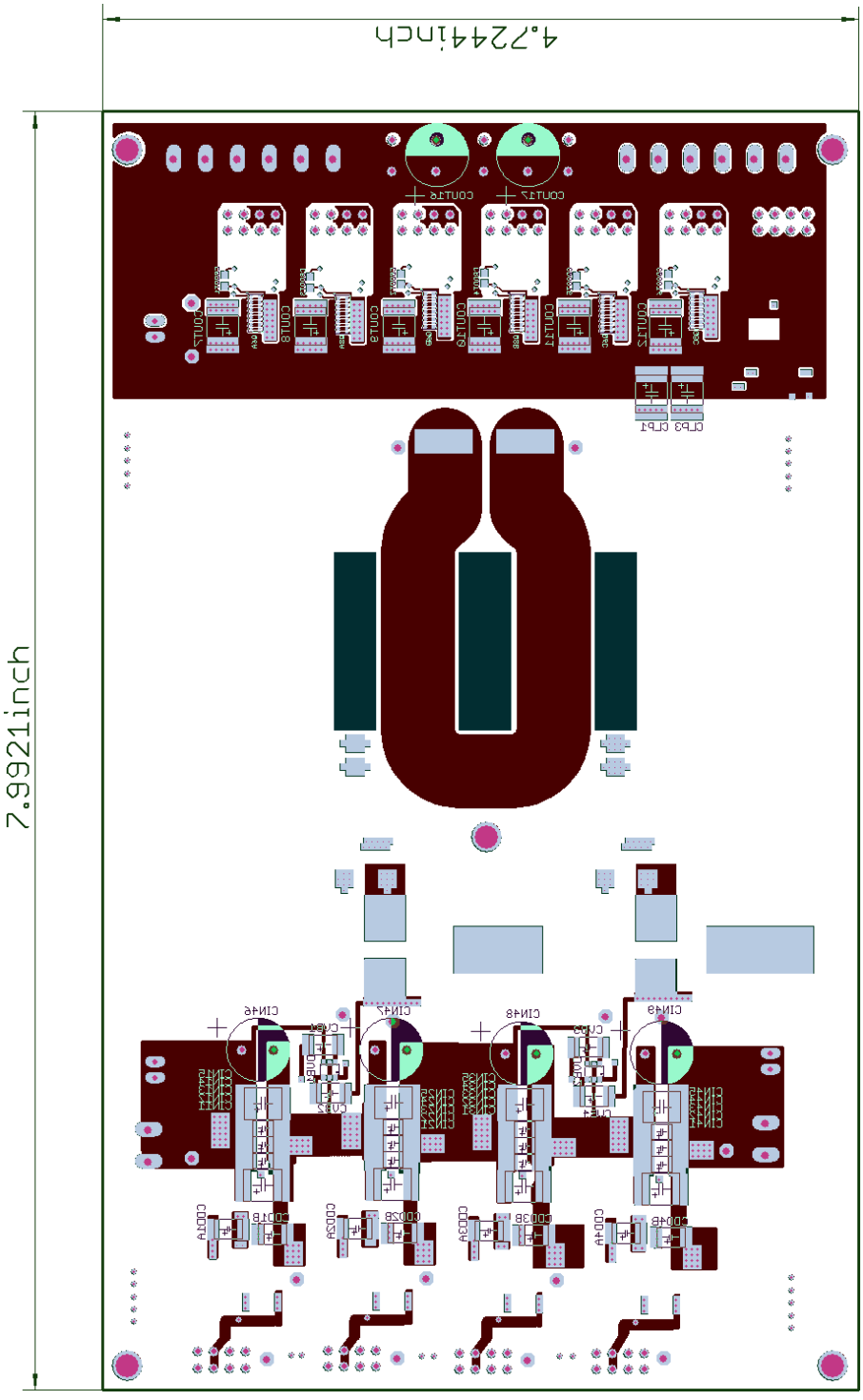


Figure D-41: Layer 8 of the Si-based reconfigurable double stacked active bridge converter board. The dark green indicates the locations of the cutouts for the magnetic core.

Appendix E EAGLE Schematic and Bill of Materials (BOM)

This Appendix contains schematic and Bill of Materials (BOM) details for each of the prototype boards. The schematics for all boards were done in EAGLE V6. There are a total of five schematics. The first schematic is for the first generation prototype of the ICN converter. The second schematic is for the synchronous full bridge rectifier for the ICN converter. The third schematic is for the fully integrated ICN board. The fourth schematic is for the GaN-based prototype for the reconfigurable double stacked active bridge converter. The fifth schematic is only for the inverter stage of the Si-based prototype for the active bridge converter because the transformation and rectification stages are identical to the GaN-based prototype.

There are two main BOMs. One is for the ICN converter prototypes and the other is for the reconfigurable active bridge converter prototypes.

E.1 First Generation ICN Converter

This schematic contains the inverter stage used in the initial prototype of the ICN converter and it is the same inverter used in the final prototype of Figure 2-25. The schematic also contains the full bridge diode rectifier output stage. Between the inverter stage and the rectifier stage are the planer transformers of section D.1, two handmade inductors, as well as the capacitors used on the bottom branch to form the –jX impedance (included in this set of schematic files).

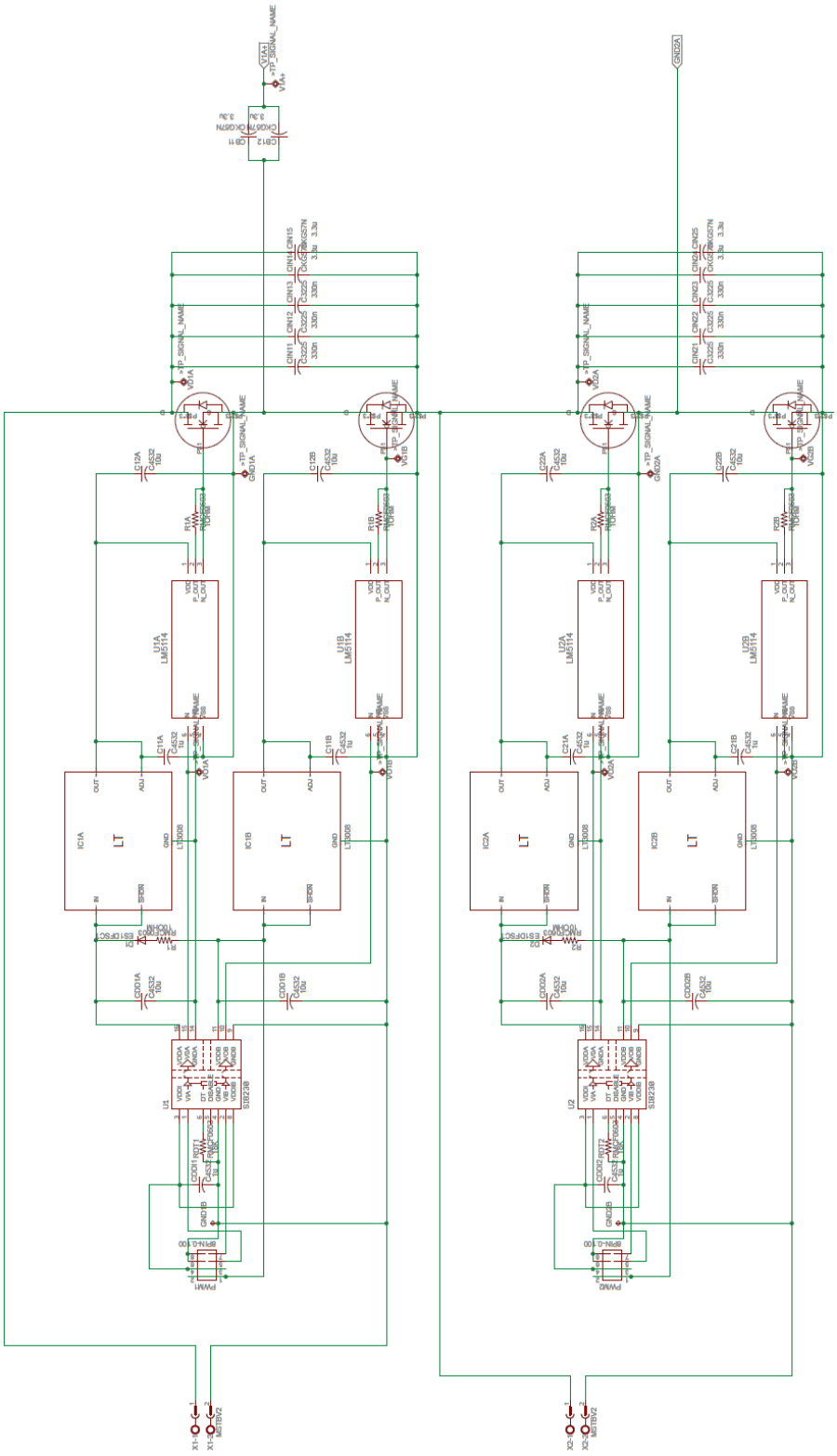


Figure E-1: Schematic of the top inverter of the ICN converter.

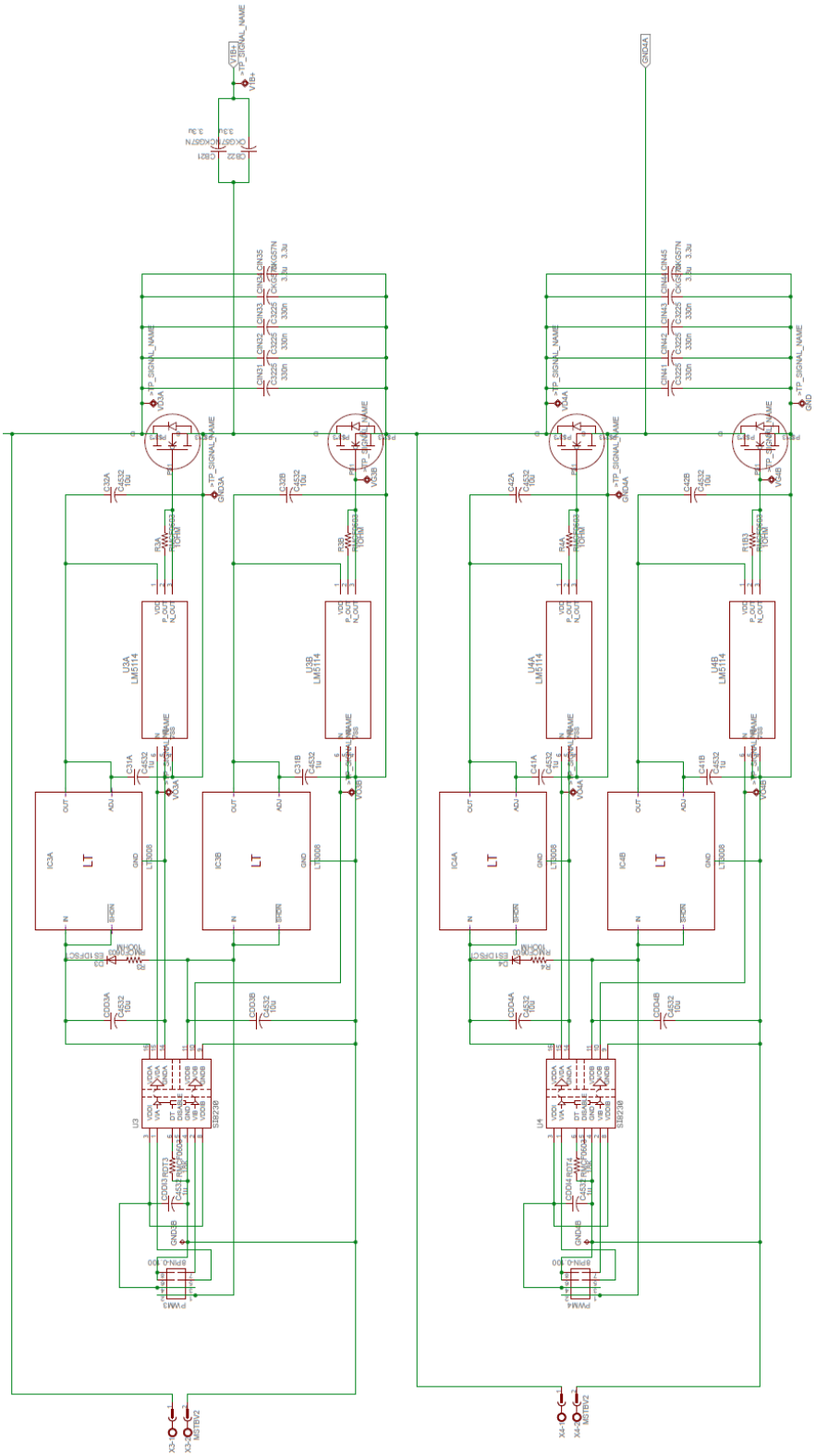


Figure E-2: Schematic of the bottom inverter of the ICN converter.

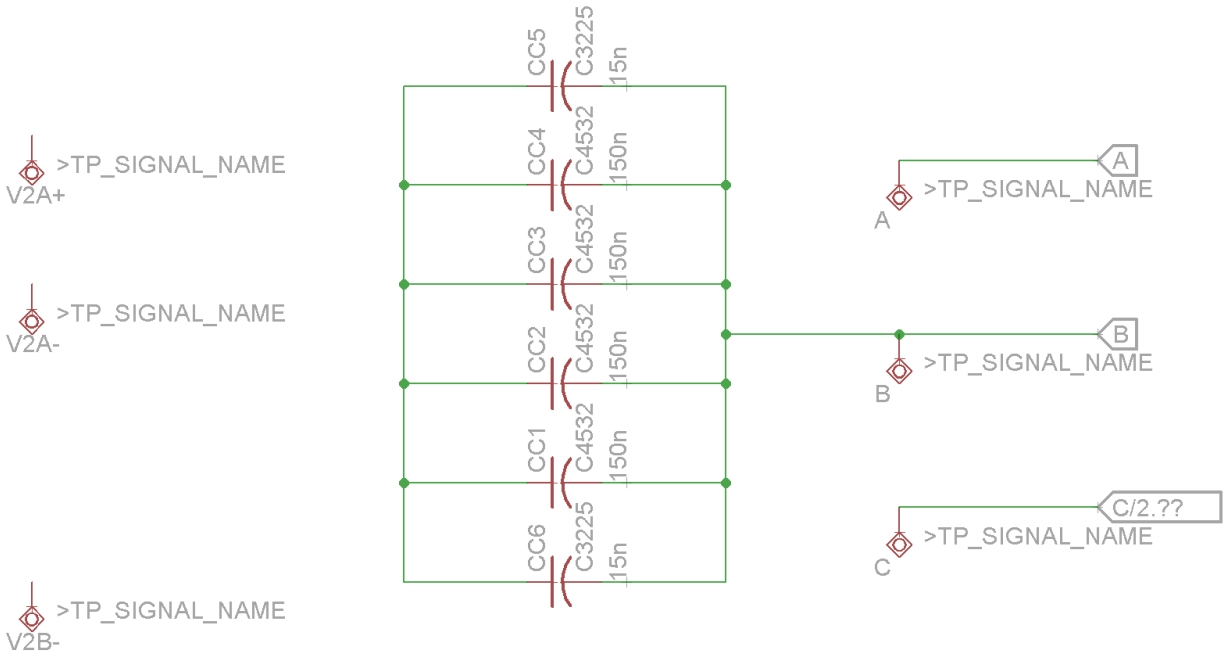


Figure E-3: Schematic of the capacitors comprising the –jX impedance of the ICN converter.

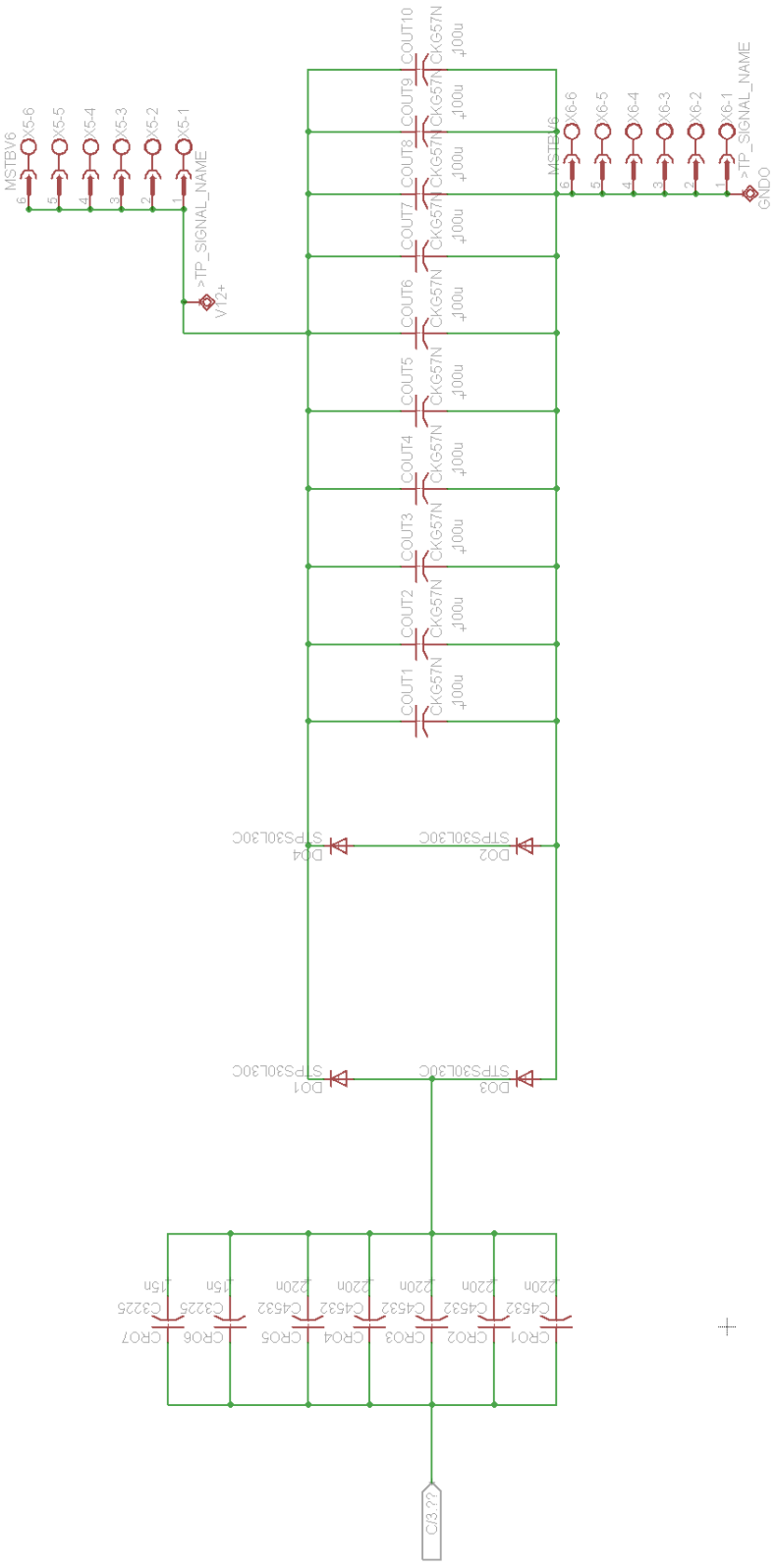


Figure E-4: Schematic of the output diode bridge rectifier of the first generation ICN converter.

E.2 Synchronous Rectifier for the ICN Converter

This schematic contains the output stage beyond the secondary of the transformer. It includes the synchronous rectifier used in the final prototype of Figure 2-25.

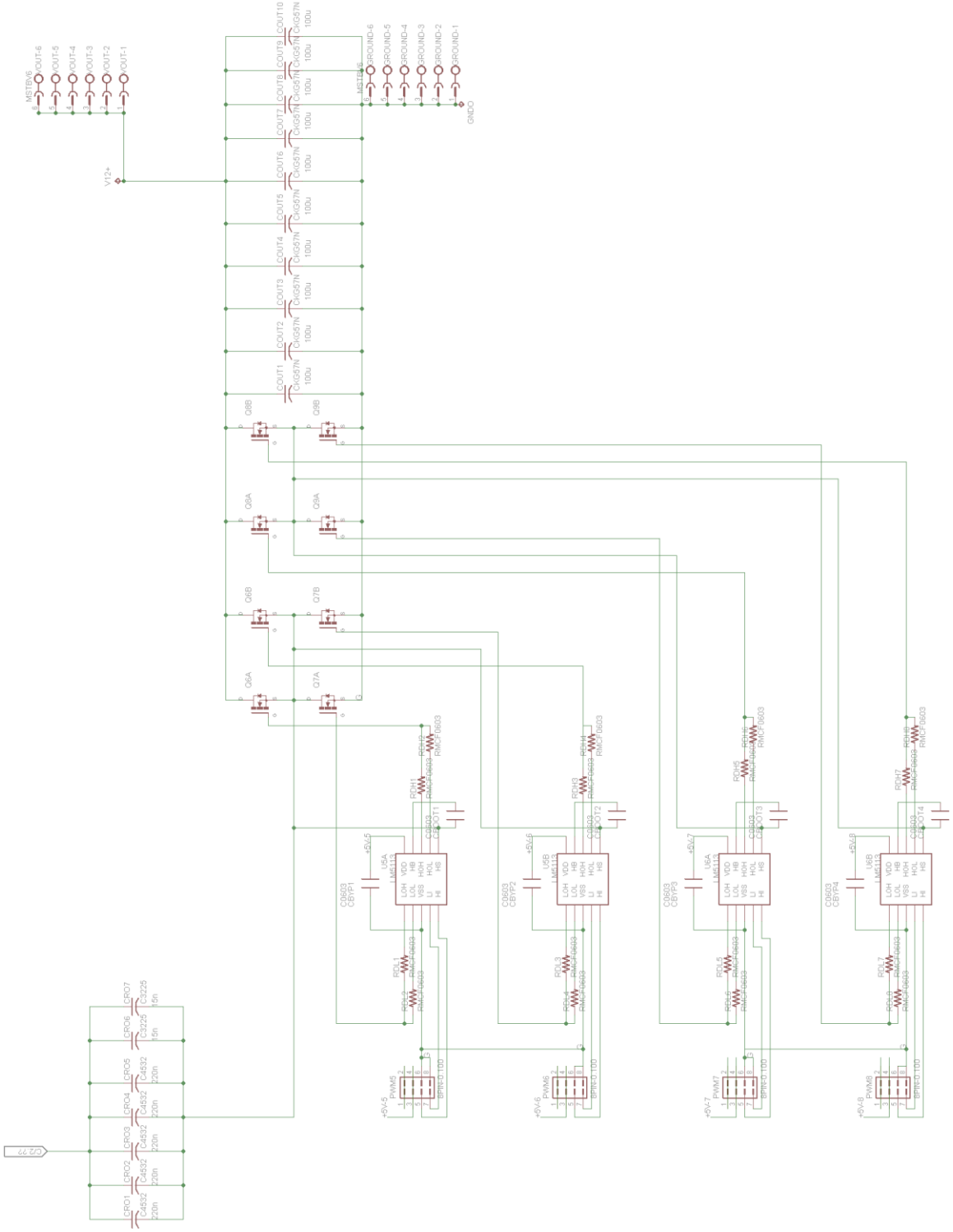


Figure E-5: Schematic of the synchronous full bridge rectifier of the final ICN converter.

E.3 Fully integrated ICN Converter

This schematic contains the various stages used in the final prototype of Figure 2-27. Compared to the original prototype, it includes a very similar inverter stage, but now has integrated magnetic components and a synchronous rectifier stage that has three sets of parallel FETs.

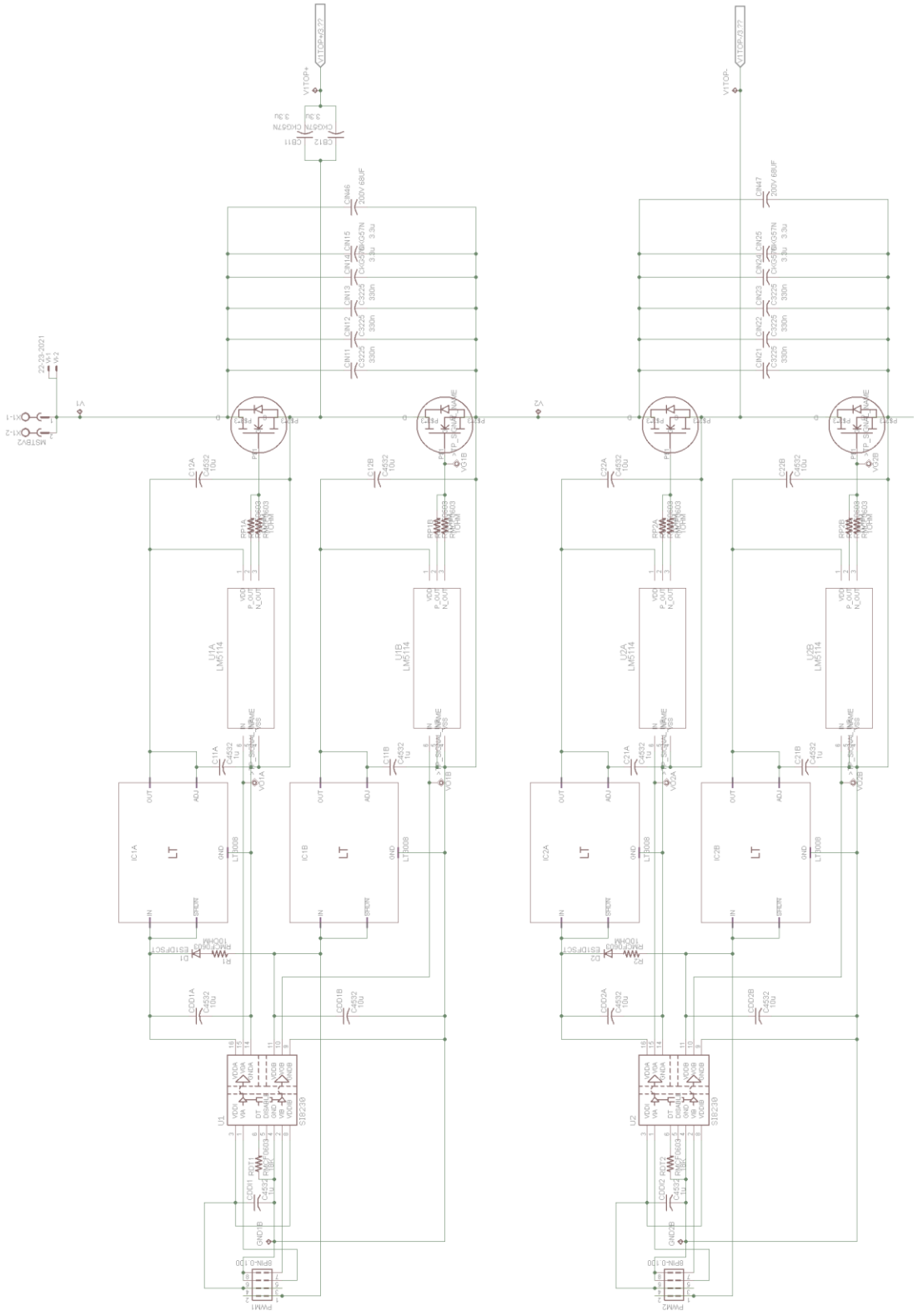


Figure E-6: Schematic of the top inverter of the fully integrated ICN converter.

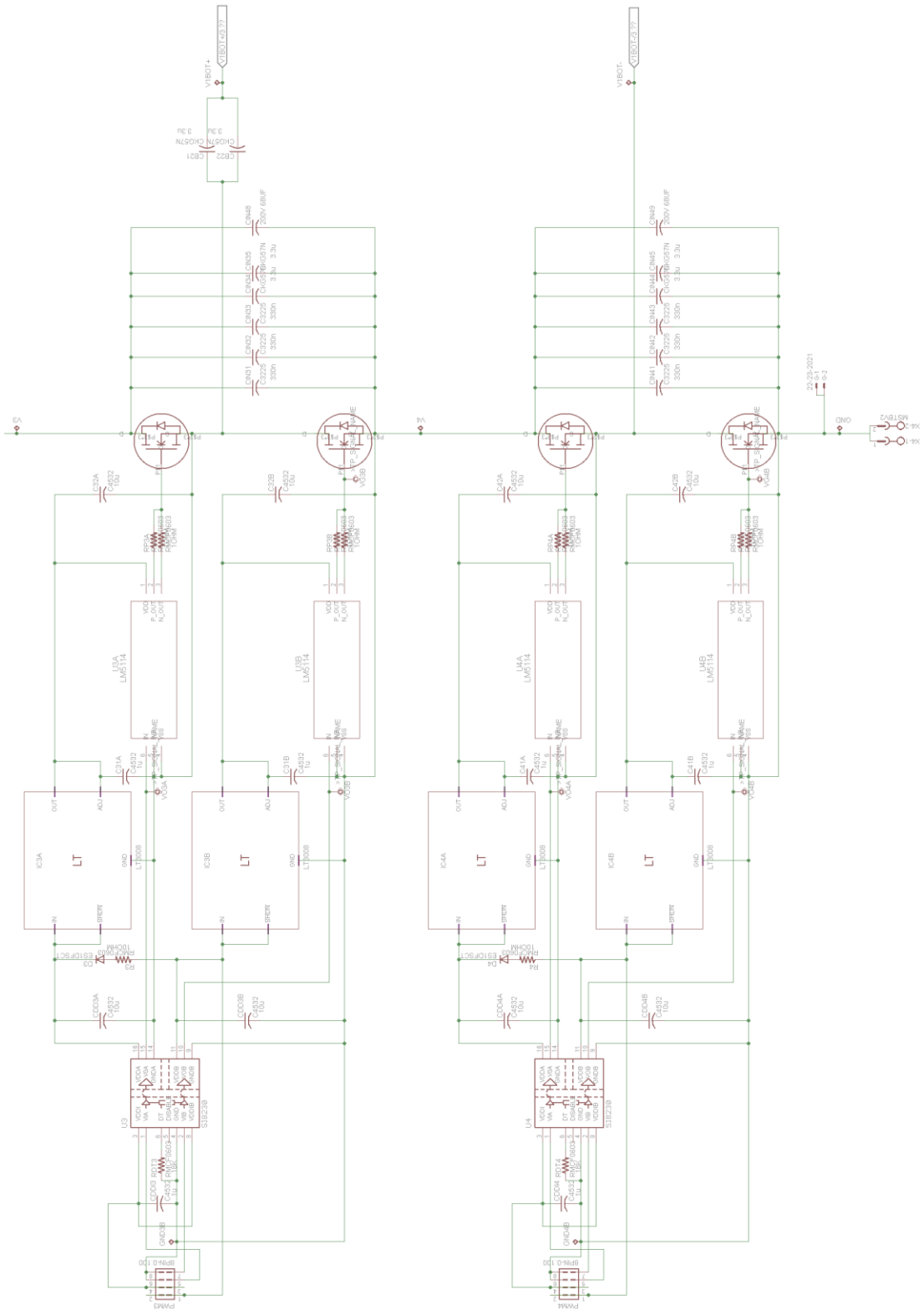


Figure E-7: Schematic of the bottom inverter of the fully integrated ICN converter.

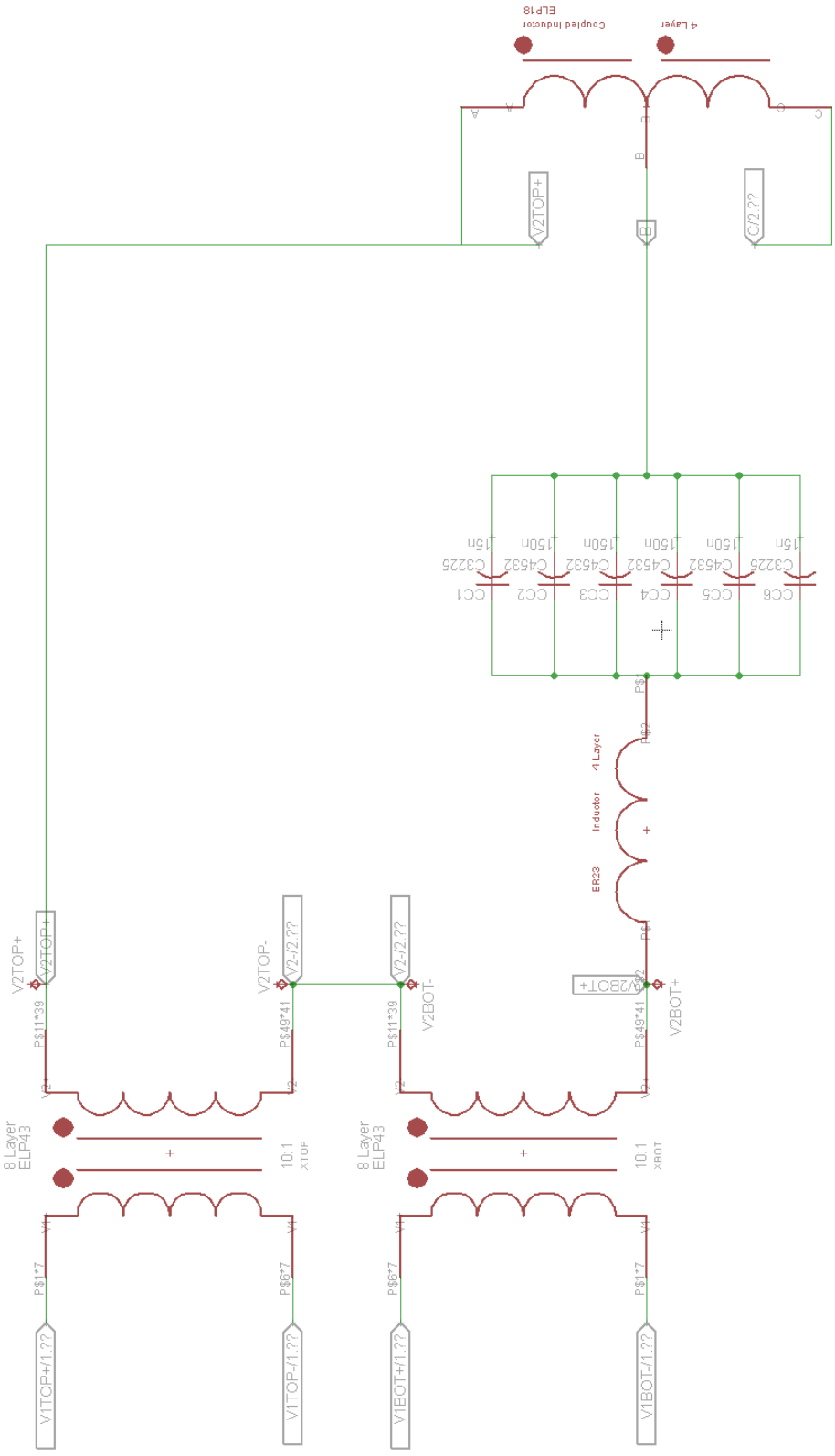


Figure E-8: Schematic of the transformers, the resonant inductor, the –jX capacitors, and the coupled inductor for the fully integrated ICN converter.

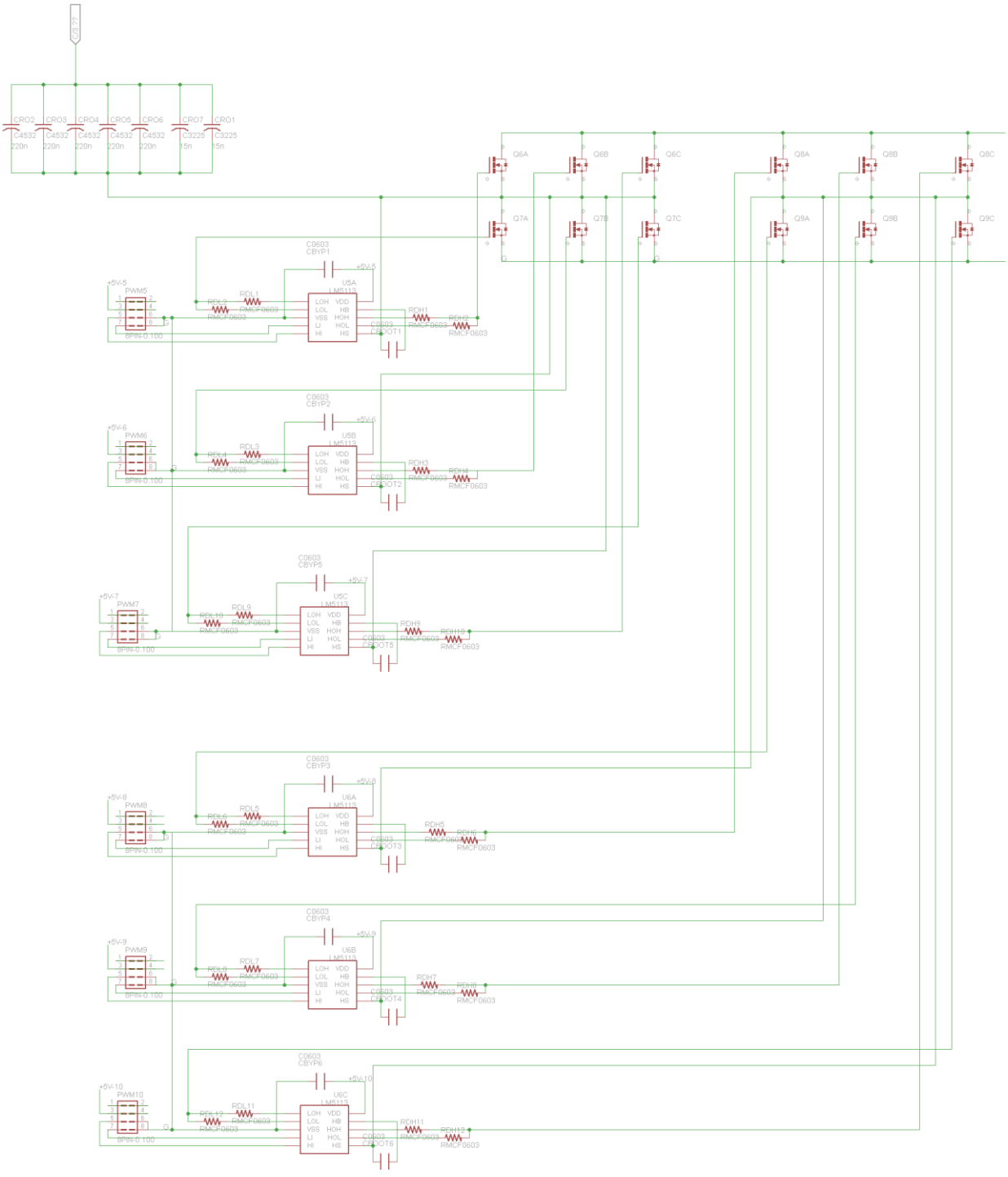


Figure E-9: Schematic of the output rectifier for the fully integrated ICN converter.

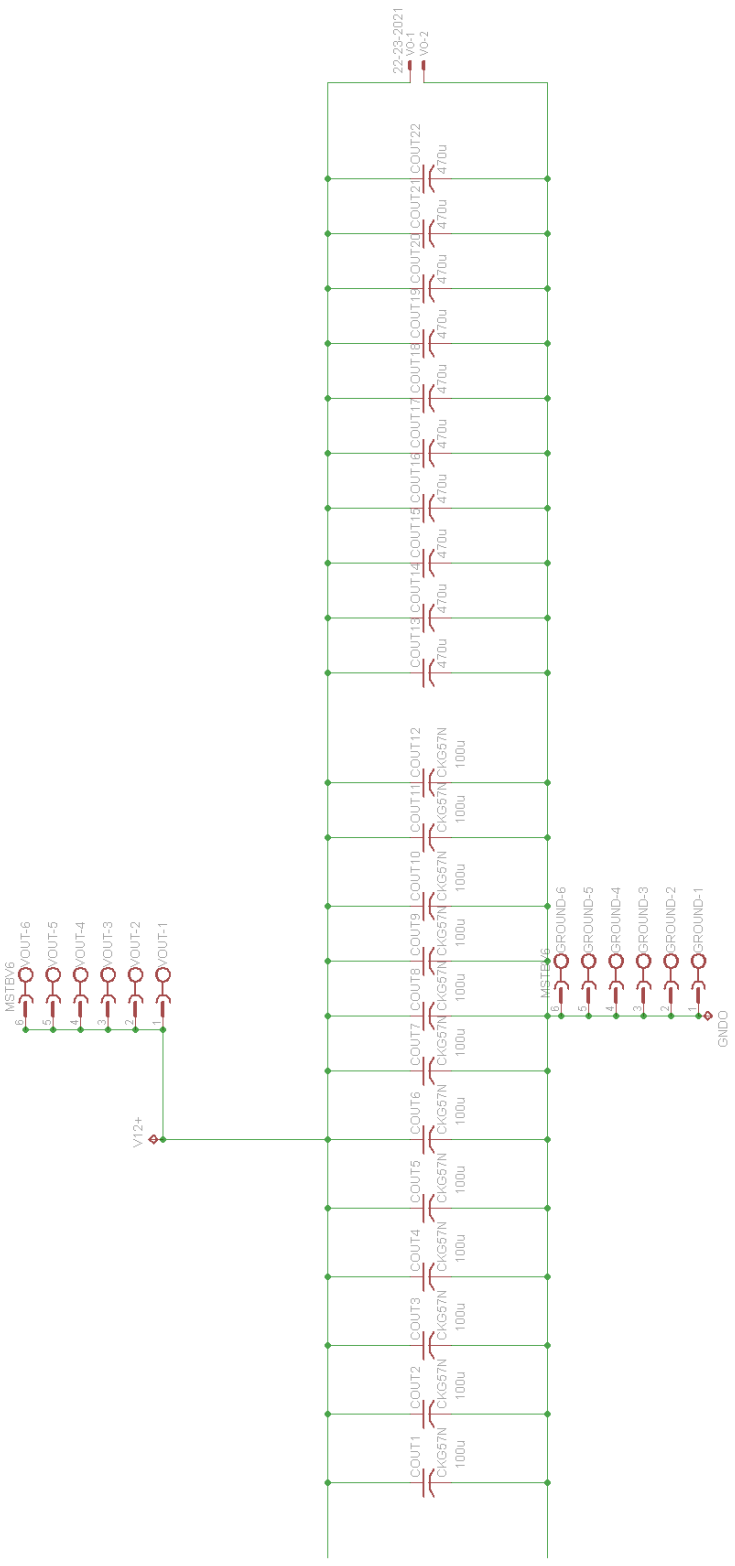


Figure E-10: Schematic of the output capacitors for the fully integrated ICN converter.

E.4 ICN Converter Bill of Materials

Table E-1 shows the list of materials used across the different prototypes for the ICN resonant converter.

Table E-1: Bill of Materials for the ICN Converter

Description	Part Number	Notes
CONN HEADER 8POS .100 STR 30AU	68602-108HLF	Ribbon connector from control
TERM BLOCK HDR 2POS VERT 5.08MM	1755736	Solder to board power connectors
TERM BLOCK PLUG 2POS 5.08MM	1792757	Plugin power connectors
RES 18K OHM 1/10W 1% 0603	RMCF0603FT18K0	Dead time delay resistor (RDT), DT[nS] = 10*RDT[kOhm]
CAP CER 1UF 50V 10% X7R 1812	C4532X7R1H105K160KA	Maintain voltage - input to Si8230, output of LT3008
IC HIGH/LOW SIDE DRIVER 16NSOIC	SI8230AB-B-IS1	Isolator and H-Bridge Driver, Dual input, 5V UVLO, Narrow
DIODE ULTRA FAST 200V 1A SMA	ES1D	Bootstrap Diode
RES 10 OHM 1/10W 1% 0603	RMCF0603FT10R0	Bootstrap Resistor to limit current
CAP CER 10UF 25V 10% X7R 1812	C4532X7R1E106K250KA	Maintain - VDDA, VDDB of isolator/driver, output of LT3008
IC REG LDO 5V 20MA 6DFN	LT3008EDC-5#TRMPBF	Voltage Regulator, fixed 5V for GaN FETs
IC MOSFET GATE DVR 7.6A SOT23-6	LM5114BMF/NOPB	LM5114 GaN FET Driver
KIT RES 1% 22 VALUES 50 EA 0603	PHH1-KIT-ND	Resistor kit for pull up and pull down gate resistors
TRANS GAN 200V 12A BUMPED DIE	EPC2010	Inverter GaN FETs
PC TEST POINT MINIATURE SMT TEST POINT PC MINI .040"D	5000, 5001, 5003, 5015, 5118	Test Points
CAP CER 0.33UF 250V 10% X7T 1210	C3225X7T2E334K200AA	Small caps across GaN FETs
CAP CER 3.3UF 250V 20% X7T SMD	CKG57NX7T2E335M500JH	Medium caps across GaN FETs, Blocking caps before transformers
CAP ALUM 56UF 200V 20% RADIAL	UCY2D560MPD1TD	Electrolytic input caps
CAP CER 0.15UF 50V 5% C0G 1812	C4532C0G1H154J250KA	-jX caps
CAP CER 0.22UF 50V 5% NP0 1812	C4532NP01H224J320KA	+ output resonant tank caps
CAP CER 0.015UF 630V 5% NP0 1210	C3225C0G2J153J160AA	-jX and output resonant tank caps
CAP CER 100UF 16V 20% X7S SMD	CKG57NX7S1C107M500JH	Output caps
CAP POLYMER 1000UF 20% 16V T/H	APSG160ELL102MJB5S	Electrolytic output caps
FERRITE CORE	B66291GX149	E core for transformers
Ferrite Cores & Accessories I 43/4/28 N49 5900 +25%-25%	B66291KX149	I core for transformers
Plain Core, 0.750" OD, 1.5" L, -2 Mix	P4848-102	Bottom branch resonant inductor
FERRITE CORE EIR23	B66482GX149, B66482KX149	ER, I core for resonant inductor
FERRITE CORE EILP18	B66283GX149, B66283KX149	E, I core for coupled inductor
DIODE SCHOTTKY 30V 15A D2PAK	STPS30L30CG-TR	Full-bridge rectifier diodes
HEATSINK FOR TO-263	DA-T263-201E-TR	Heat Sinks for diodes
TRANS GAN 30V 60A BUMPED DIE	EPC2023ENG	Synchronous rectifier GaNFETs
IC GATE DVR HALF BRIDGE 4A 10LLP	LM5113SD/NOPB	Half-bridge driver for rectifier
CAP CER 6.8UF 10V 10% JB 0603	C1608JB1A685K080AC	Capacitors for LM5113 driver
TERM BLOCK HDR 6POS VERT 5.08MM	1755778	Solder to board output power connectors
TERM BLOCK PLUG 6POS 5.08MM	1792799	Plugin output power connectors
TERM BLOCK PLUG 6POS 5.08MM	1792281	Plugin output power connectors
HEX STANDOFF 6-32 NYLON 1-1/4"	4822	Standoffs
HEX NUT 5/16" NYLON 6-32	9606	Nuts for standoffs

E.5 Reconfigurable Double Stacked Active Bridge Converter

This schematic contains the various stages used in the prototype of Figure 5-13 as well as the inverter stage of Figure 5-14.

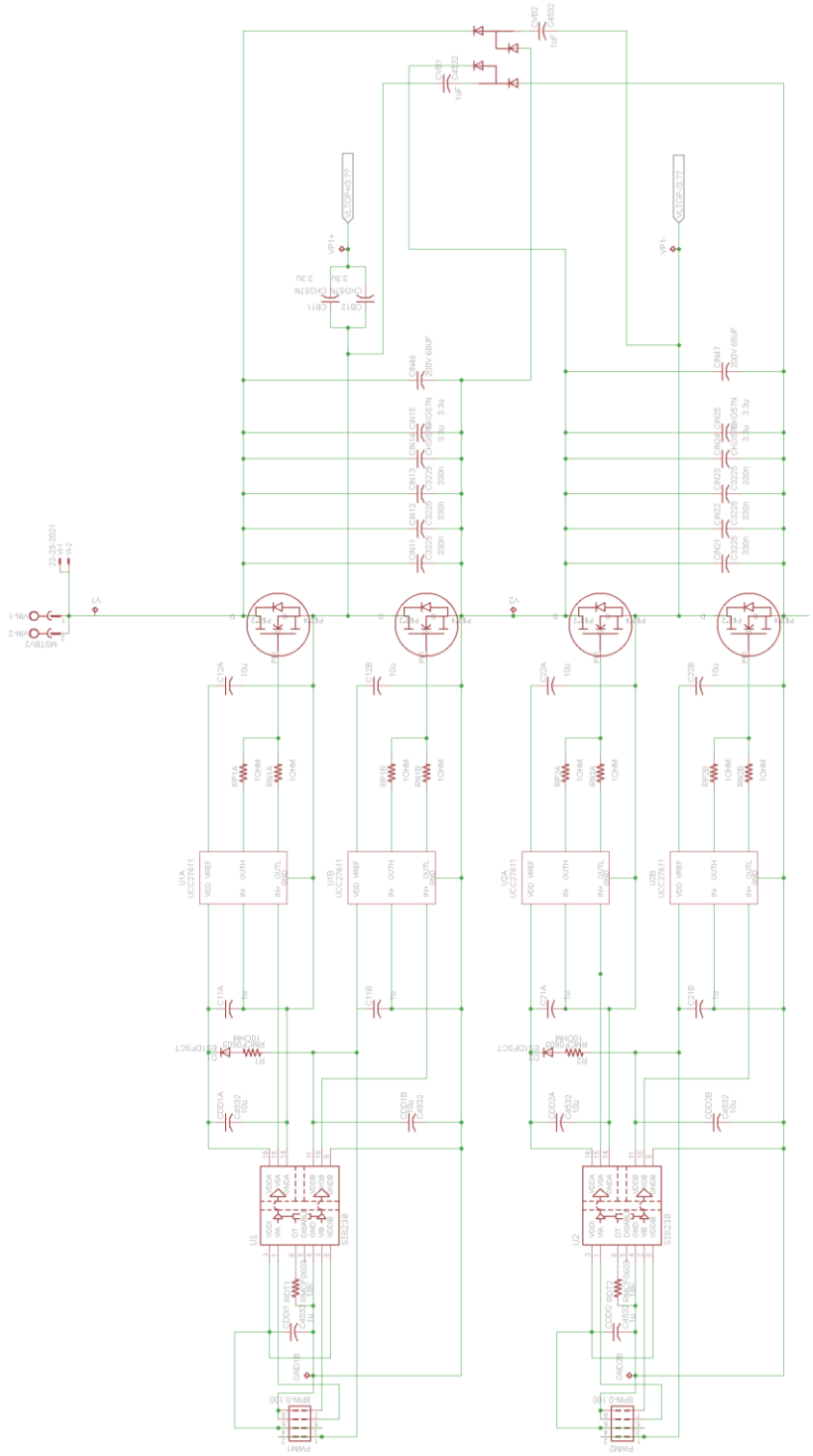


Figure E-11: Schematic of the top inverter of the GaN-based double stacked active bridge converter.

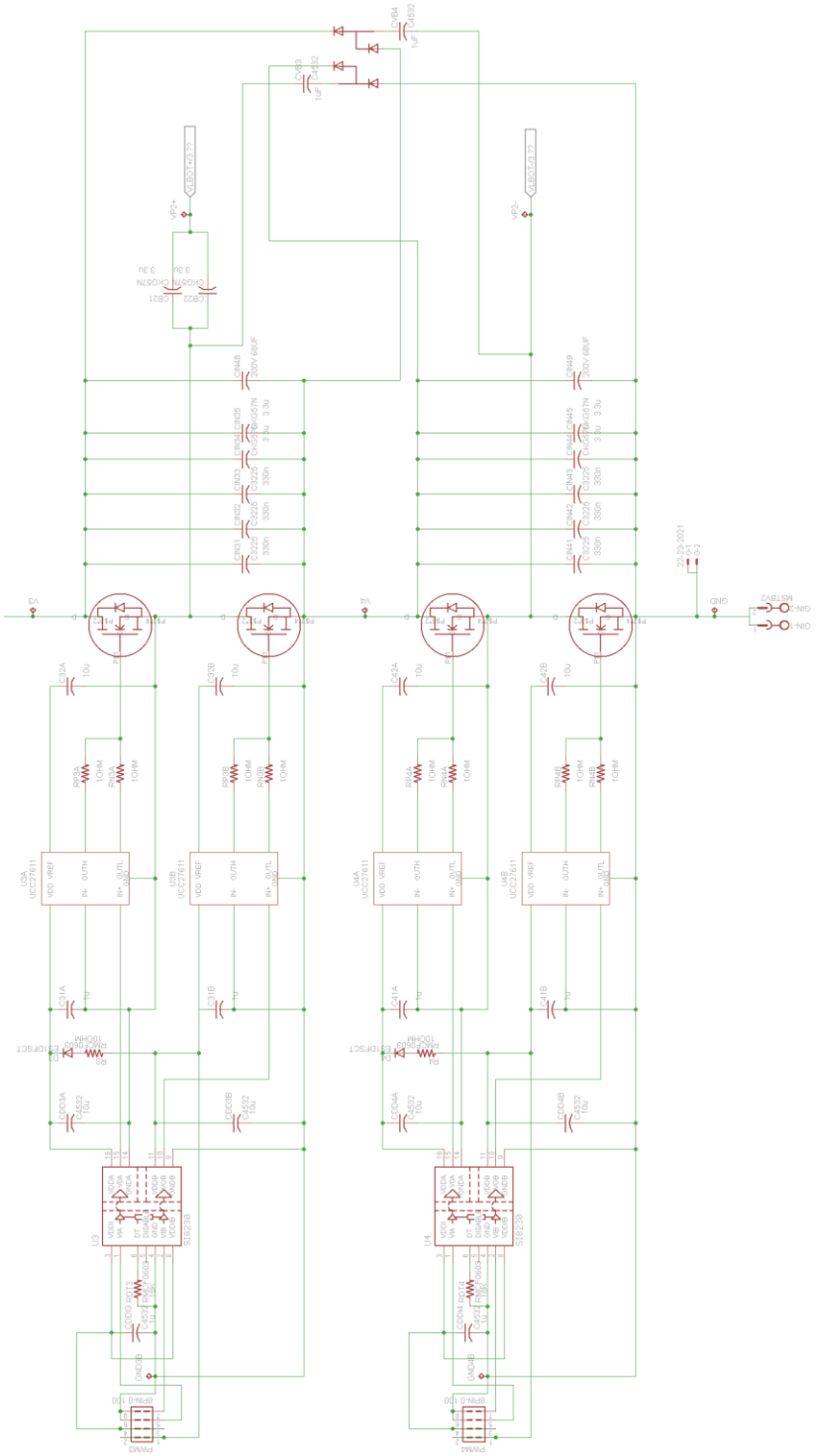


Figure E-12: Schematic of the bottom inverter of the GaN-based double stacked active bridge converter.

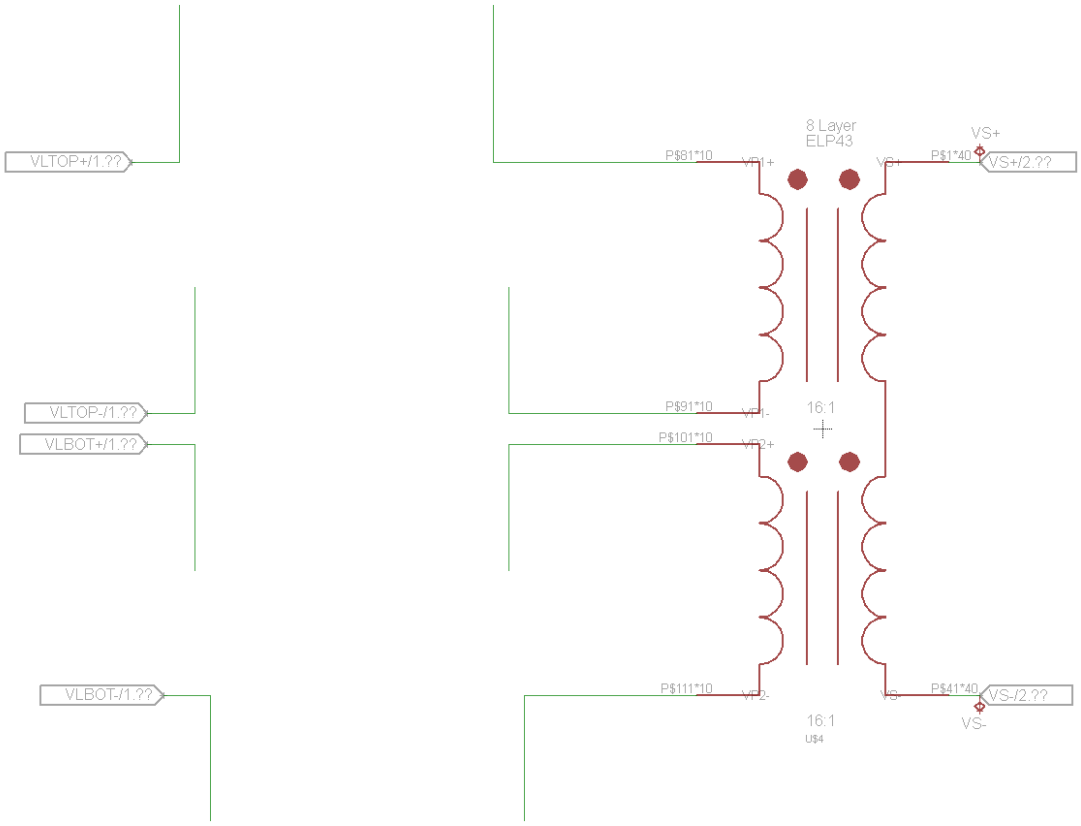


Figure E-13: Schematic of the transformer of the reconfigurable double stacked active bridge converter with provision for two discrete inductors in series with each primary winding.

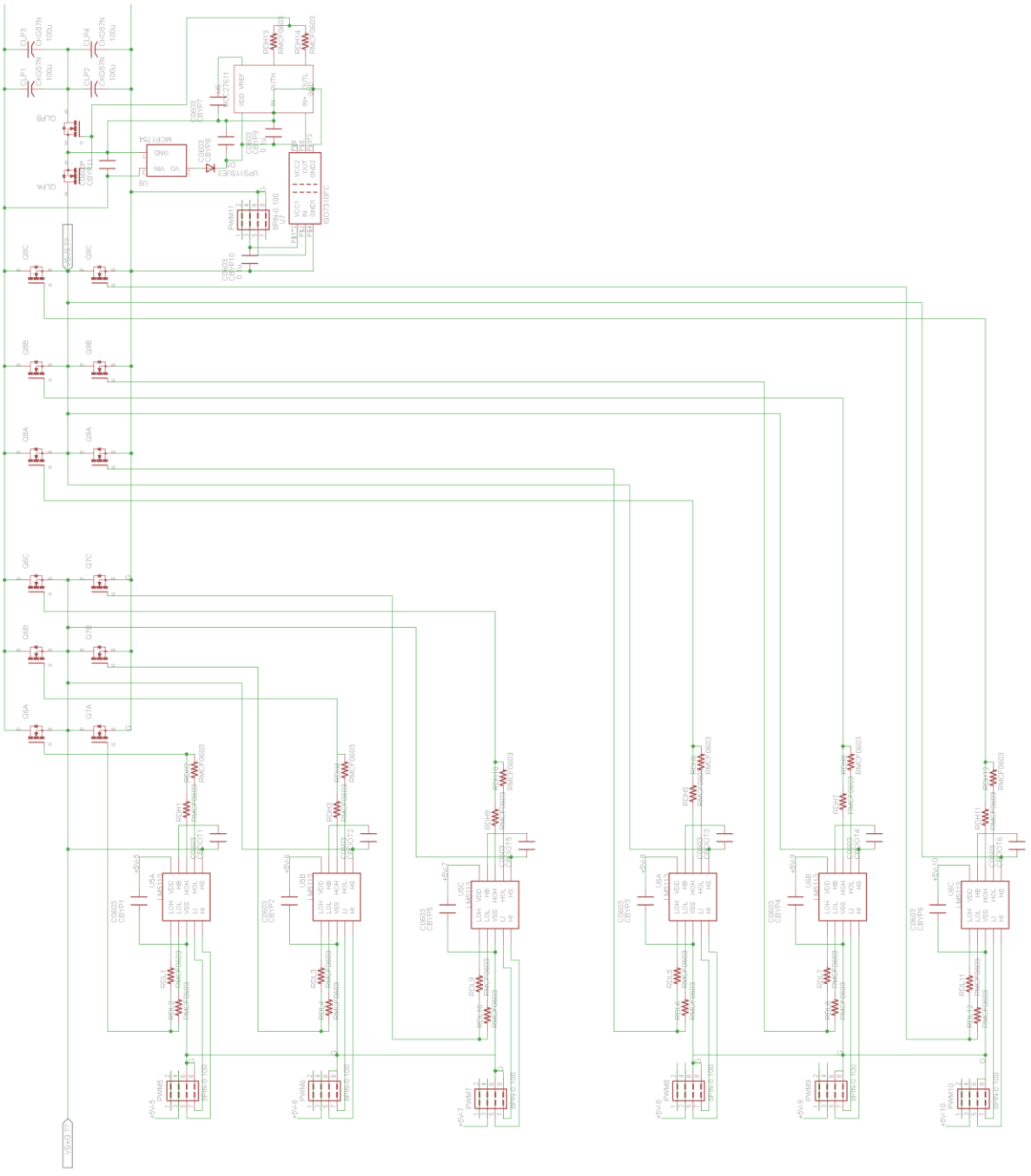


Figure E-14: Schematic of the rectifier of the reconfigurable double stacked active bridge converter, which contains three paralleled sets of half-bridges. Also shown is the low-power auxiliary switch.

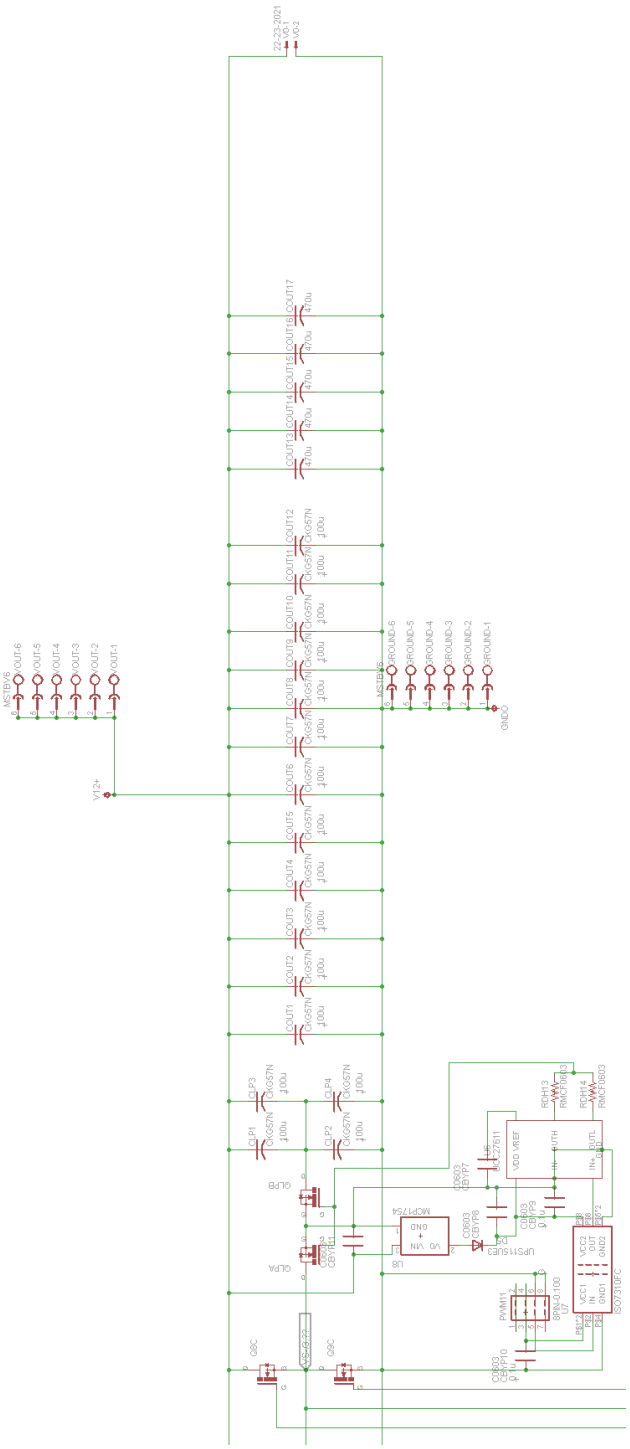


Figure E-15: Schematic of the low-power auxiliary switch and output capacitors of the reconfigurable double stacked active bridge converter.

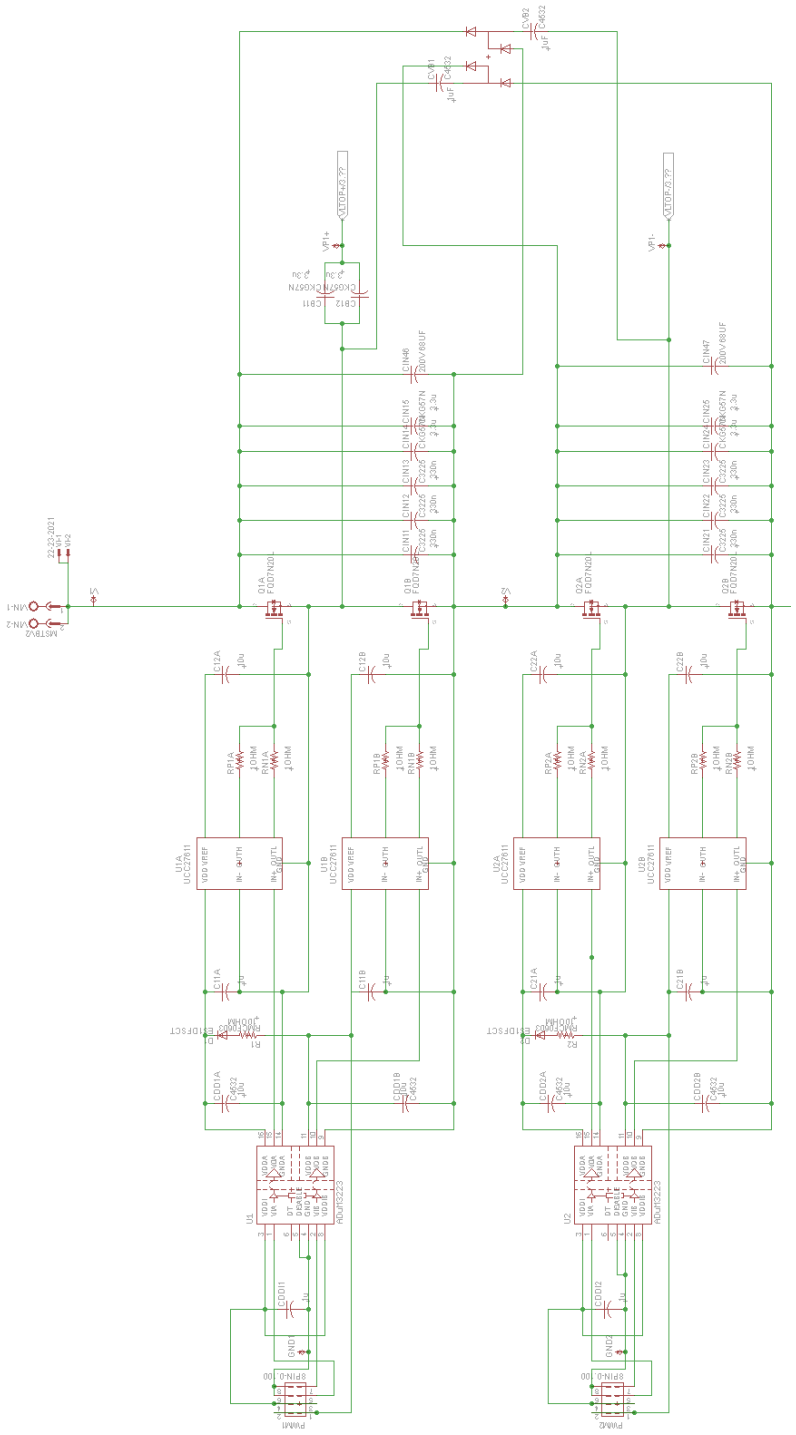


Figure E-16: Schematic of the top inverter of the Si-based double stacked active bridge converter.

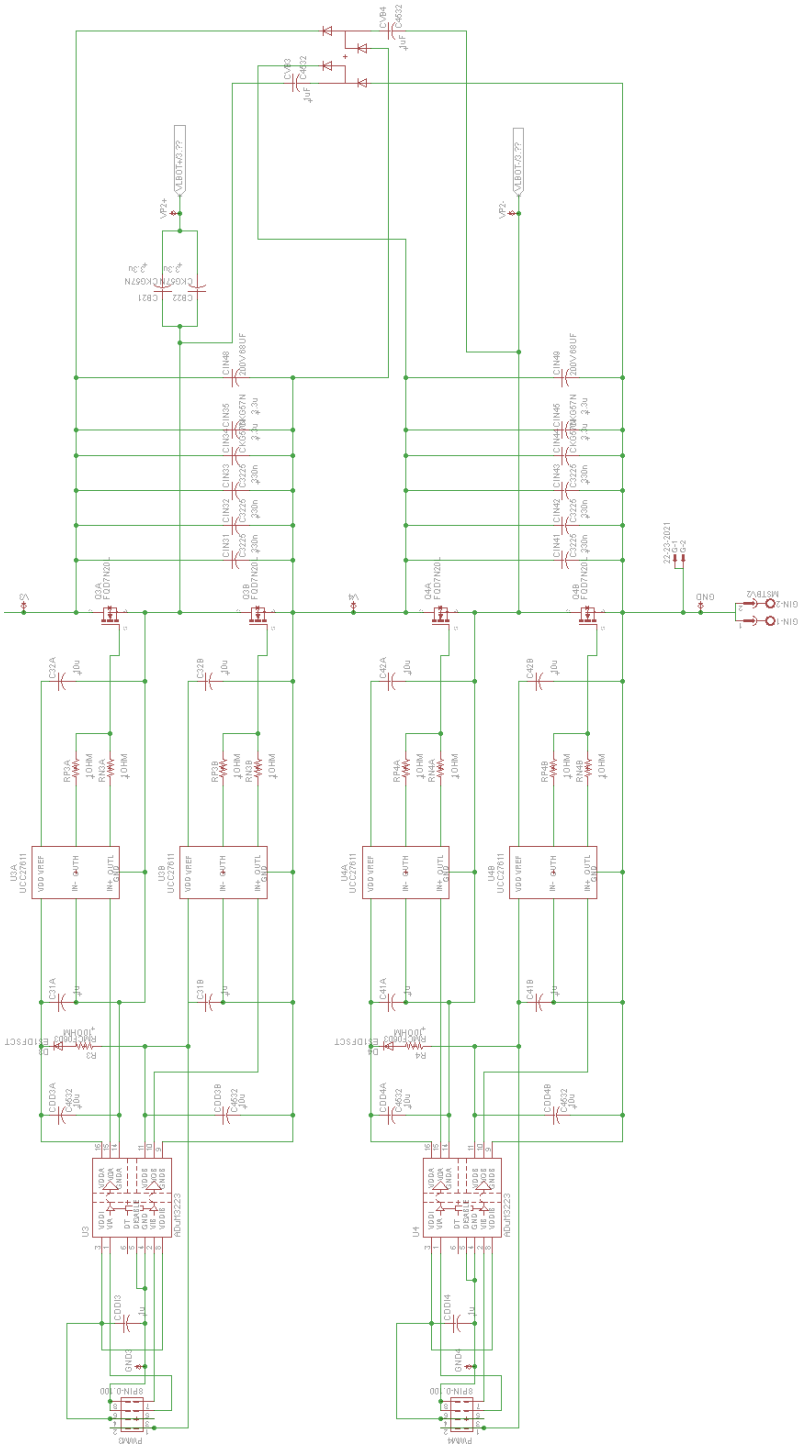


Figure E-17: Schematic of the bottom inverter of the Si-based double stacked active bridge converter.

E.6 Active Bridge Converter Bill of Materials

Table E-2 shows the list of materials used for the GaN-based reconfigurable double stacked active bridge converter. Table E-3 shows the materials used for the Si-based reconfigurable double stacked active bridge converter that differ from those listed in Table E-2. Table E-4 shows the materials used for the Si-based reconfigurable single stacked active bridge converter that differ from those used in Table E-2 or Table E-3.

Table E-2: Bill of Materials for the GaN-Based Double Stacked Active Bridge Converter

Description	Part Number	Notes
CONN HEADER .100" DUAL STR 8POS	PRPC004DABN-RC	Ribbon connector from control
TERM BLOCK HDR 2POS VERT 5.08MM	1755736	Solder to board power connectors
TERM BLOCK PLUG 2POS 5.08MM	1792757	Plugin power connectors
CAP CER 1UF 50V X6S 0603	C1608X6S1H105K080AC	Maintain voltage - input to ISO
DGTL ISO 3KV 2CH GATE DVR 16SOIC	ADUM3223ARZ	Isolator and H-Bridge Driver, Dual input, 5V UVLO, Narrow
DIODE ULTRA FAST 200V 1A SMA	ES1D	Bootstrap Diode
RES 10 OHM 1/10W 1% 0603	RMCF0603FT10R0	Bootstrap Resistor to limit current
CAP CER 10UF 25V X5R 0603	C1608X5R1E106M080AC	Maintain voltages of driver
CAP CER 10UF 25V 10% X7R 1812	C4532X7R1E106K250KA	Maintain voltage - VDDA, VDDB of isolator/driver
IC GATE DRIVER 6SON	UCC27611DRVT	Single GaN FET Driver with voltage regulator, for inv. and LP switch
RES SMD 10 OHM 5% 1/10W 0402	ERJ-2GEJ100X	Resistor for pull up and pull down gate resistors
DIODE ARRAY GP 300V 225MA SOT26	MMBD3004BRM-7-F	Diodes for voltage balancing circuits
CAP CER 1UF 250V X7T SMD	CKG45KX7T2E105K290JH	Caps for voltage balancing circuits
TRANS GAN 200V 5A BUMPED DIE	EPC2012C	Inverter GaN FETs
TEST POINT PC MINI .040"D	5000, 5001, 5003, 5118	Test Points
CAP CER 0.33UF 250V 10% X7T 1210	C3225X7T2E334K200AA	Small caps across GaN FETs
CAP CER 3.3UF 250V 20% X7T SMD	CKG57NX7T2E335M500JH	Medium caps across GaN FETs, Blocking caps before transformers
CAP ALUM 56UF 200V 20% RADIAL	UCY2D560MPD1TD	Electrolytic input caps
CAP CER 100UF 16V 20% X7S SMD	CKG57NX7S1C107M500JH	Output caps
CAP POLYMER 1000UF 20% 16V T/H	APSG160ELL102MJB5S	Electrolytic output caps
FERRITE CORE	B66291GX149	E core for transformer
Ferrite Cores & Accessories I 43/4/28 N49 5900 +25%-25%	B66291KX149	I core for transformer
TRANS GAN 30V 60A BUMPED DIE	EPC2023ENG	Synchronous rectifier GaNFETs
IC GATE DVR HALF BRIDGE 4A 10LLP	LM5113SD/NOPB	Half-bridge driver for rectifier
CAP CER 6.8UF 10V 10% JB 0603	C1608JB1A685K080AC	Capacitors for LM5113 driver
KIT RES 1% 22 VALUES 50 EA 0603	PHH1-KIT	0603 resistor kit for P_out and N_out resistors of LM5113 (50x 1-7.5 Ohm)
DIODE SCHOTTKY 15V 1A POWERMITE	UPS115UE3/TR7	Bootstrap Diode for LP switch
IC REG LDO 5V 0.15A SOT23A-3	MCP1754ST-5002E/CB	On-board Regulator for LP switch
IC REG ISOLATED 5V 0.2A 7SOP	DCP010505BP-U	External regulator for LP switch
DGTL ISO 3KV 1CH GEN PURP 8SOIC	ISO7310FCQDRQ1	Isolator for LP switch
TERM BLOCK HDR 6POS VERT 5.08MM	1755778	Solder to board output power connectors
TERM BLOCK PLUG 6POS 5.08MM	1792799	Plugin output power connectors
HEX STANDOFF 6-32 NYLON 1-1/4"	4822	Standoffs
HEX NUT 5/16" NYLON 6-32	9606	Nuts for standoffs
WIRE JUMPER FEM-FEM 15CM 10PCS	MIKROE-511	Jumper cables for rectifier signals

Table E-3: Bill of Materials for the Si-Based Double Stacked Active Bridge Converter that were not included in Table E-2

Description	Part Number	Notes
RES SMD 0.47 OHM 5% 1/10W 0402	73L1R47J	Resistor for pull up and pull down gate resistors
MOSFET N-CH 200V 7.6A DPAK	FQD10N20LTM	Inverter MOSFETs

Table E-4: Bill of Materials for the Si-Based Single Stacked Active Bridge Converter that were not included in Table E-2

Description	Part Number	Notes
RES SMD 0.47 OHM 5% 1/10W 0402	73L1R47J	Resistor for pull up and pull down gate resistors
DIODE GEN PURP 300V 1A SMA	ES1FCT-ND	Bootstrap Diode
CAP CER 2.2UF 450V X7T SMD	CKG57NX7T2W225M500JH	Medium caps across GaN FETs, Blocking caps before transformers
MOSFET N-CH 500V 13A PG-TO252	IPD50R280CE	Inverter MOSFETs

Appendix F Converter Operating Parameters and Data

This Appendix contains details on the control of the converter as well as the operating data that was gathered. All gate drive signals are from the control board developed by David Otten of MIT. It has a number of control functions as shown in operating terminal of Figure F-1, which is run using PuTTY. The period, duty cycle, dead time, and inverter and rectifier phase shift can be individually adjusted in increments of 1.04 ns. There is a preprogrammed table for inverter and rectifier phase shifts based on input voltage. This Appendix is written in the style of a tutorial of how we use the controller and power up the prototypes. The parameters and operation for each converter and operating mode is detailed in the following subsections.

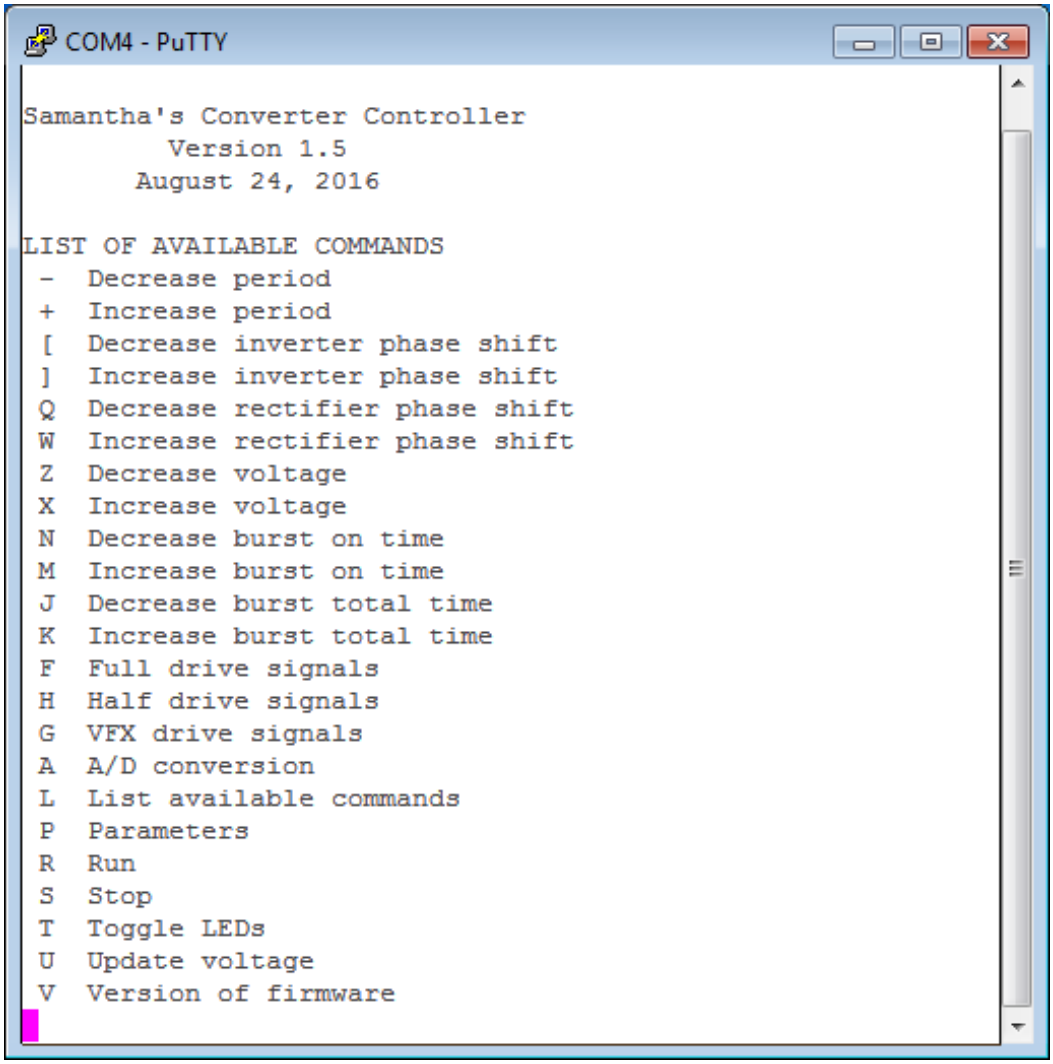


Figure F-1: Command terminal for the control board

F.1 ICN Converter Operated in Normal Mode

The ICN resonant converter of Chapter 2 in fundamental mode is designed to operate at 500 kHz with a 50% duty ratio. In actuality, the control board generates waveforms that are around 502.5 kHz. The dead-time between when one half-bridge device turns off and before the other turns on is set to 20 increments (or 20.8 ns) for the inverter and 70 increments (or 72.8 ns) for the rectifier. There was no optimization made in this setting. The parameters are therefore set as:

```
Master Period 01880
Master Duty Cycle 00940

     Duty  Phase Dead
Unit Cycle Shift Time
PWM1 00940 00000 00020
PWM2 00940 00000 00020
PWM3 00940 00000 00020
PWM4 00940 00000 00020
PWM5 00940 00000 00070
PWM6 00940 00000 00070
PWM7 00940 00000 00070
PWM8 00940 00000 00070
```

PWM1 and PWM2 are the half-bridge gate signals for the top inverter. PWM3 and PWM4 are the half-bridge gate signals for the bottom inverter. PWM5 and PWM 6 are identical and are used to drive the rectifier half-bridges connected to the output resonant tank. PWM7 and PWM8 are identical and are used to drive the rectifier half-bridges connected to the negative terminal of both transformers.

To aide in the operation, there is a preprogrammed set of phase shifts for the inverters and rectifier based on input voltage. The theoretical phase shift (in radians) of one inverter (from zero) is given in (2.20) but must be adjusted for use with the controller. The following equation is used to calculate the phase shift that the controller uses:

$$Inverter\ Phase\ Shift = round\left(\frac{\text{acos}\left(\frac{NV_{in}}{4V_{out}}\right)}{f \times 2pi} \times 1.04 \times 10^{-9} \times 2\right) \tag{F.1}$$

where the function round(X) will round X to the nearest integer, N is the turns ratio which is set to 0.10041753, f is the frequency of 502500 Hz, V_{out} is the output voltage, which is set to 12 V, and V_{in} is the input voltage. The phase shift value used by the controller is double the theoretical phase shift because it is the total phase shift between the two inverters. The rectifier phase shift is approximately half of the inverter phase shift, but does depend on how the transformer output currents combine. The actual values used are based on the rectifier phase shift seen in simulation with a diode bridge rectifier. The phase shifts used can be seen in Table F-1.

Table F-1: Phase Shifts used by the Control Board for Normal Mode

V_{in}	Inverter Phase	Rectifier Phase	V_{in}	Inverter Phase	Rectifier Phase	V_{in}	Inverter Phase	Rectifier Phase
240	636	358	301	542	306	362	433	255
241	635	355	302	540	305	363	431	254
242	633	353	303	539	305	364	430	253
243	632	352	304	537	304	365	428	252
244	630	351	305	535	303	366	426	251
245	629	351	306	534	302	367	424	249
246	627	351	307	532	301	368	422	248
247	626	351	308	530	300	369	420	247
248	625	351	309	529	299	370	418	246
249	623	351	310	527	298	371	416	244
250	622	351	311	525	297	372	414	243
251	620	349	312	524	296	373	412	242
252	619	347	313	522	295	374	409	240
253	617	345	314	520	295	375	407	239
254	616	345	315	519	294	376	405	238
255	614	344	316	517	293	377	403	236
256	613	344	317	515	292	378	401	235
257	611	343	318	513	291	379	399	233
258	609	343	319	512	290	380	397	232
259	608	342	320	510	289	381	395	231
260	606	341	321	508	289	382	393	230
261	605	340	322	507	288	383	391	228
262	603	339	323	505	288	384	389	227
263	602	339	324	503	287	385	386	226
264	600	338	325	501	287	386	384	225
265	599	337	326	500	286	387	382	223
266	597	336	327	498	285	388	380	222
267	596	335	328	496	285	389	378	221
268	594	335	329	494	284	390	376	220
269	593	334	330	493	284	391	373	218
270	591	333	331	491	283	392	371	217
271	590	332	332	489	282	393	369	216
272	588	331	333	487	282	394	367	215
273	587	330	334	486	281	395	364	213
274	585	330	335	484	280	396	362	212
275	583	329	336	482	280	397	360	211
276	582	328	337	480	279	398	358	209
277	580	327	338	478	278	399	355	208
278	579	326	339	477	277	400	353	207
279	577	325	340	475	277	401	351	206
280	576	325	341	473	276	402	348	204
281	574	324	342	471	275	403	346	203
282	572	323	343	469	274	404	343	202
283	571	322	344	467	273	405	341	200
284	569	321	345	466	273	406	339	199
285	568	320	346	464	272	407	336	198
286	566	319	347	462	271	408	334	197
287	564	319	348	460	270	409	331	195
288	563	318	349	458	269	410	329	194
289	561	317	350	456	268	411	326	193
290	560	316	351	454	267	412	324	191
291	558	315	352	453	266	413	321	190
292	556	314	353	451	265	414	319	189
293	555	313	354	449	264	415	316	187
294	553	313	355	447	263	416	314	186
295	552	312	356	445	262	417	311	185
296	550	311	357	443	261	418	308	184
297	548	310	358	441	260	419	306	182
298	547	309	359	439	259	420	303	181
299	545	308	360	437	258	421	301	180
300	544	307	361	435	257	422	298	178

Because the phase shift is dependent on the ratio of input to output voltage, the same phase shift can be used for multiple combinations of input and output voltages as long as the ratio is maintained. Typically, the control board and gate drive signals are powered up at an initial phase shift of 636 increments for the inverters and 358 increments for the rectifier. The terminal should display:

```
Converter Running in Full Drive Mode
Burst on time = 100
Burst total time = 00100
Voltage = 00240, Inverter phase = 00636, Rectifier phase = 00358
```

But instead of using 240 V initially, we typically start with 20 V on the input and 1 V on the output (a 20 to 1 ratio). First the electronic load is set to voltage mode and then the voltage is set to 1 V. Then the power supply is set to 20 V. With the control stage already running, power is applied to the converter. The Kepco 600 V power supply that is used has a course voltage increment of 8 V but fine-tuned increments of 0.1 V can be done to get the exact desired voltage. As the input voltage is increased, the load voltage is also increased to maintain the 20 to 1 ratio. It is important to note that the output voltage we use is measured on the board and will vary slightly from the actually voltage setting on the electronic load. Once the input voltage is equal to 240 V and the output voltage is equal to 12 V, only the input voltage is increased with the output voltage (as measured on the board, not the electronic load) kept constant at 12 V. The control board voltage is increased with the power supply voltage as demonstrated below:

```
Converter Running in Full Drive Mode
Burst on time = 100
Burst total time = 00100
Voltage = 00240, Inverter phase = 00636, Rectifier phase = 00358
Voltage = 00241, Inverter phase = 00635, Rectifier phase = 00355
Voltage = 00242, Inverter phase = 00633, Rectifier phase = 00353
Voltage = 00243, Inverter phase = 00632, Rectifier phase = 00352
Voltage = 00244, Inverter phase = 00630, Rectifier phase = 00351
Voltage = 00245, Inverter phase = 00629, Rectifier phase = 00351
Voltage = 00246, Inverter phase = 00627, Rectifier phase = 00351
Voltage = 00247, Inverter phase = 00626, Rectifier phase = 00351
Voltage = 00248, Inverter phase = 00625, Rectifier phase = 00351
```

It should be noted that all changes are made manually and all control is open loop. Input voltage, input current, output voltage, and output current are measured by a Yokogawa WT1800 power meter, which also calculates the efficiency. Table F-2 shows the experimental data used to generate Figure 2-33. It also shows the parameters normally recorded when running the ICN converter. It includes the normal startup points as well as key operating points. Table F-3 shows the data used to generate Figure 2-28

Table F-2: Experimental Data for Non-Burst Mode Operation of the ICN Converter

Operating Point		Power Supply		Power Meter		Load		Power Meter		Inv. Phase	Rec. Phase	Calculated			Power Meter
Vin	Vout	Vin	Iin	Vin	Iin	Vout	Iout	Vout	Iout			Pin	Pout	Eff.	Eff.
20	1	20.1	0.139	20.004	0.1331	0.98	2.35	1.005	2.3331	636	358	2.663	2.345	0.88065	0.88097
40	2	39.2	0.27	39.212	0.2654	1.94	4.7	2.0076	4.5995	636	358	10.407	9.234	0.88729	0.88749
80	4	79.3	0.541	79.36	0.5364	3.87	9.4	4.0006	9.449	636	358	42.569	37.802	0.88802	0.88821
120	6	119.5	0.812	119.67	0.8081	5.74	14.35	6.0076	14.271	636	358	96.705	85.734	0.88655	0.88636
160	8	159.8	1.083	160.03	1.0789	7.78	19.2	8	19.064	636	358	172.656	152.512	0.88333	0.88314
200	10	199.9	1.353	200.36	1.35	9.54	23.9	10.007	23.914	636	358	270.486	239.307	0.88473	0.8847
260	12	259.6	1.589	260.07	1.5843	11.52	30.15	12.013	30.375	606	341	412.029	364.895	0.88561	0.88567
290	12	289.5	1.514	290.14	1.5097	11.52	32.55	12.002	32.555	560	316	438.024	390.725	0.89202	0.89204
320	12	319.3	1.423	320.09	1.4178	11.47	33.85	12.009	33.921	510	289	453.824	407.357	0.89761	0.89766
350	12	349.2	1.307	350.03	1.301	11.52	34.1	12.015	34.238	456	268	455.389	411.370	0.90334	0.90329
380	12	379	1.164	380.14	1.156	11.5	33.3	12	33.354	397	232	439.442	400.248	0.91081	0.91082
410	12	409.1	0.983	410.09	0.9742	11.52	30.6	12.003	30.658	329	194	399.510	367.988	0.92110	0.91925

Table F-3: Experimental Data for the Fully Integrated Version of the ICN Converter

Operating Point		Power Supply		Power Meter		Load		Power Meter		Inv. Phase	Rec. Phase	Calculated		
Vin	Vout	Vin	Iin	Vin	Iin	Vout	Iout	Vout	Iout			Pin	Pout	Eff.
20	1	20.1	0.131	19.944	0.12866	1.01	2.3	1.032	2.177	636	358	2.57	2.25	0.87555
40	2	40	0.253	39.812	0.25353	2.01	4.5	2.0597	4.401	636	358	10.09	9.06	0.89807
80	4	80.1	0.498	79.843	0.4979	3.9	9	4.0072	8.991	636	358	39.75	36.03	0.90630
120	6	100	0.621	99.575	0.62156	4.86	11.1	5.0023	11.221	636	358	61.89	56.13	0.90692
160	8	120.1	0.746	119.576	0.74568	5.74	13.6	5.9994	13.474	636	358	89.17	80.84	0.90658
200	10	160.1	0.994	159.45	0.99545	7.82	18.1	8.0088	17.996	636	358	158.72	144.13	0.90803

For Table F-2 and Table F-3, the calculated input and output power is based on the data collected from the meters, not the power supply or the load. The calculated efficiency is the ratio of output power to input power.

F.2 ICN Converter Operated in Burst Mode

To modulate power, we propose operating the converter using on/off control. After the input voltage and phase shift are set, the controller is used to set the number of cycles the converter is on and indirectly, the total number of cycles it is off. (By cycle, we mean one switching period as defined by the Master Period parameter.) The burst mode parameters can be changed while the converter is running. To operate in burst mode, the electronic load is set to resistive mode and the resistance is set to keep the output voltage (still measured on the board with the power meter) at a constant 12 V while still delivering the desired amount of power as displayed on the power meter. An oscilloscope is used to monitor that the voltage ripple is within ±2% of the nominal output voltage. The number of cycles on and total burst time are manually set such that the output voltage stays within two horizontal bands located at ±240 mV.

For a given input voltage and desired output power, there a total of three parameters that are adjusted to maintain the desired output power, voltage, and voltage ripple. They are the resistance of the load, the number of cycles the converter is on, and the total number of cycles that are considered for each burst period. Because this is done manually in an open loop fashion, it can be an iterative process to make sure all operating values are obtained. It should be noted that the electronic load that was used has a minimum resistance of 0.5 Ω. To achieve higher power levels (above 300W at an output voltage of 12 V), external power resistors must be connected in parallel with the load.

The command terminal for adjusting the power will look something like the following:

```
Voltage = 00380, Inverter phase = 00397, Rectifier phase = 00232

Converter Running in Full Drive Mode
Burst on time = 00100
Burst total time = 00100
Burst on time = 00100
Burst total time = 00101
Burst on time = 00100
Burst total time = 00102
Burst on time = 00100
Burst total time = 00103
Burst on time = 00100
Burst total time = 00104
Burst on time = 00100
Burst total time = 00105
```

In the above example, the converter goes from being on for 100 cycles and off for zero cycles to being on for 100 cycles and off for 5 cycles. At first, the converter will deliver the full (natural) power given by Figure 2-8, but it is then set to deliver roughly 100/105 or 95.2% of the full power.

To achieve a similar effect, the on time can be modulated as shown below:

```
Voltage = 00380, Inverter phase = 00397, Rectifier phase = 00232

Converter Running in Full Drive Mode
Burst on time = 00100
Burst total time = 00100
Burst on time = 00099
Burst total time = 00100
Burst on time = 00098
Burst total time = 00100
Burst on time = 00097
Burst total time = 00100
Burst on time = 00096
Burst total time = 00100
Burst on time = 00095
Burst total time = 00100
```

To maintain high efficiency, usually a large number of cycles on is desirable because the cycles which experience transient hard switching is only a small fraction of the total number of cycles on. This usually means that the burst total time needs to be increased in order to back down in power. It should be noted that the burst frequency is set by the burst total time so if the converter bursts at a frequency that is between 20 Hz and 20 kHz, it is possible that the converter will emit audible sound. Therefore, there is a tradeoff between efficiency and aesthetics. In our experience, when the converter is operated in the audible spectrum, it is greatly overshadowed by the noise from the various fans within the power supply, load, and meter.

To get a full understanding of how we operated the converter, Table F-4 shows the operating parameters and data used to generate Figure 2-36. Table F-5 and Table F-6 show the operating parameters and data used to generate Figure 2-40. For space reasons, only the actively set parameters are shown. These are the voltage of the power supply and the resistance of the load. The other readings from the power supply (i.e., current) and load (i.e., voltage and current) are not included. The output power of the operating point is based on the data of Table F-2 and multiplied by some operating percentage (e.g., 10%, 50%).

Table F-4: Experimental Data for Burst Mode Operation of the ICN Converter to deliver about 50% power

Operating Point			Burst			Power Supply	Power Meter		Load	Power Meter		Inv. Phase	Rec. Phase	Calculated			Power Meter
Vin	Vout	Pout	R	on	total	Vin	Vin	Iin	R	Vout	Iout			Pin	Pout	Eff.	Eff.
20	1	1.21	0.83	100	200	20.1	19.983	0.0632	0.8	0.956	1.1608	636	358	1.263	1.110	0.8787	0.8786
40	2	4.90	0.82	100	200	40	40.001	0.1274	0.8	1.919	2.3415	636	358	5.096	4.493	0.8817	0.8826
80	4	19.88	0.81	100	200	80.2	80.35	0.26	0.8	3.881	4.7475	636	358	20.891	18.425	0.8820	0.8820
120	6	44.80	0.80	100	200	120	120.24	0.3905	0.8	5.815	7.119	636	358	46.954	41.397	0.8817	0.8821
160	8	79.69	0.80	100	200	160.1	160.5	0.5222	0.8	7.764	9.508	636	358	83.813	73.820	0.8808	0.8815
200	10	124.48	0.80	100	200	200.4	200.84	0.6538	0.8	9.711	11.897	636	358	131.309	115.532	0.8798	0.8805
260	12	183.16	0.79	100	200	259.6	260.11	0.7861	0.7831	12.004	15.035	606	341	204.472	180.480	0.8827	0.8829
290	12	196.48	0.73	100	200	289.5	290.19	0.7507	0.7294	12.002	16.119	560	316	217.846	193.460	0.8881	0.8881
320	12	205.17	0.70	100	200	319.3	320.13	0.7048	0.6991	12.001	16.798	510	289	225.628	201.593	0.8935	0.8932
350	12	206.95	0.70	100	200	349.4	350.21	0.6476	0.6921	12.002	16.965	456	268	226.796	203.614	0.8978	0.8980
380	12	201.33	0.72	100	200	379.6	380.46	0.5766	0.743	12.001	16.52	397	232	219.373	198.257	0.9037	0.9045
410	12	184.43	0.78	100	200	409.4	410.55	0.4872	0.7756	12.001	15.177	329	194	200.020	182.139	0.9106	0.9106

Table F-5: Experimental Data for Burst Mode Operation of the ICN Converter to deliver between 10% and 80% of rated power with a fixed input voltage of 380 V and an output voltage of 12 V.

Operating Point		Burst		Power Supply	Power Meter		Load	Power Meter		Inv. Shift	Rec. Shift	Calculated			Power Meter
Pout	R	on	total	Vin	Vin	Iin	R	Vout	Iout			Pin	Pout	Eff.	Eff.
281.58	0.51	140	200	379.4	380.44	0.8066	0.50208	12.003	23.191	397	232	306.863	278.362	0.9071	0.90725
241.11	0.60	120	200	379.4	380.45	0.6915	0.58903	12.001	19.854	397	232	263.081	238.268	0.9057	0.90551
201.33	0.72	100	200	379.4	380.46	0.5766	0.743	12.001	16.52	397	232	219.373	198.257	0.9037	0.9045
161.06	0.89	85	213	379.4	380.47	0.4606	0.8978	12.005	13.152	397	232	175.244	157.890	0.9010	0.90128
120.92	1.19	75	250	379.4	380.48	0.3471	1.2015	12.004	9.873	397	232	132.065	118.515	0.8974	0.89807
80.53	1.79	65	325	379.4	380.48	0.2329	1.8155	12.007	6.567	397	232	88.614	78.850	0.8898	0.89053
40.27	3.58	60	600	379.4	380.5	0.119	3.659	12.017	3.278	397	232	45.280	39.392	0.8700	0.87076
35.01	4.11	57	643	379.4	380.49	0.1059	4.1357	12.009	2.9039	397	232	40.294	34.873	0.8655	0.86759

Table F-6: Experimental Data for Burst Mode Operation of the ICN Converter to deliver between 60% and 100% of rated power with a fixed input voltage of 380 V and an output voltage of 12 V. A 2 Ω resistor is connected in parallel with the electronic load so that higher power levels could be reached.

Operating Point		Burst		Power Supply	Power Meter		Load	Power Meter		Inv. Shift	Rec. Shift	Calculated			Power Meter
Pout	R	on	total	Vin	Vin	Iin	R	Vout	Iout			Pin	Pout	Eff.	Eff.
362.75	0.4	178	204	379.4	380.43	1.0054	0.50005	11.996	28.962	397	232	382.484	347.428	0.9083	0.90877
322.13	0.45	160	200	379.4	380.44	0.922	0.56104	12.002	26.542	397	232	350.766	318.557	0.9082	0.90837
281.58	0.51	140	200	379.4	380.44	0.8068	0.673	12.002	23.198	397	232	306.939	278.422	0.9071	0.90672
241.11	0.60	120	213	379.4	380.45	0.6916	0.8382	12.001	19.861	397	232	263.119	238.352	0.9059	0.90578
201.33	0.72	100	643	379.6	380.46	0.5766	1.108	12.001	16.525	397	232	219.373	198.317	0.9040	0.90393

F.3 ICN Converter Operated in VFX Mode

An additional mode of operation was proposed for the ICN converter that delivers a lower power. This Variable Frequency Multiplier (VFX) technique requires the adjustment of the duty ratios and a new phase shift table. Similar to the previous operation (or fundamental mode operation), the parameters are set as follows:

```
Master Period 01880
Master Duty Cycle 00940

     Duty  Phase Dead
Unit Cycle Shift Time
PWM1 00940 00000 00090
PWM2 00940 00000 00090
PWM3 00940 00000 00090
PWM4 00940 00000 00090
PWM5 00940 00000 00090
PWM6 00940 00000 00090
PWM7 00940 00000 00090
PWM8 00940 00000 00090
```

PWM1 and PWM2 are the half-bridge gate signals for the top inverter. PWM3 and PWM4 are the half-bridge gate signals for the bottom inverter. PWM5 and PWM 6 are identical and are used to drive the rectifier half-bridges connected to the output resonant tank. PWM7 and PWM8 are identical and are used to drive the rectifier half-bridges connected to the negative terminal of both transformers.

To aide in the operation, there is a preprogrammed set of phase shifts for the inverters and rectifier based on input voltage. The theoretical phase shift (in radians) of one inverter (from zero) is given in (2.20) but must be adjusted for use with the controller. The following equation is used to calculate the phase shift that the controller uses:

$$Inverter\ VFX\ Phase\ Shift = round\left(\frac{\text{acos}\left(N\frac{V_{in}}{4V_{out}}\right)}{f \times 2pi} \times 1.04 \times 10^{-9} \times 2\right) \tag{F.2}$$

as before, the function round(X) will round X to the nearest integer, N is the turns ratio which is set to 0.10041753, f is the frequency of 502500 Hz, V_{out} is the output voltage, which is set to 12 V, and V_{in} is the input voltage. The phase shift value used by the controller is double the theoretical phase shift because it is the total phase shift between the two inverters. The rectifier phase shift is approximately half of the inverter phase shift, but does depend on how the transformer output currents combine. The actual values

used are based on the rectifier phase shift seen in the simulation of Figure C-5 with a diode bridge rectifier. The phase shifts used can be seen in Table F-7.

The converter underwent the normal startup routine with the input voltage starting at 20 V and the electronic load set to voltage mode with the output voltage at 1 V. The phase shift used was the same as what would be used for an input voltage of 240 V and an output voltage of 1 V. The command terminal then looks like

```
VFX Drive Mode Enabled

Converter Running in VFX Drive Mode
Voltage = 00240, Inverter phase = 00636, Rectifier phase = 00358
```

The data gathered when attempting to operate the converter using VFX mode are listed in Table F-8. The voltage was not increased beyond 160 V due to the nature of the waveforms and the efficiency.

Table F-7: Phase Shifts used by the Control Board for VFX Mode

Vin	Inverter Phase	Rectifier Phase	Vin	Inverter Phase	Rectifier Phase	Vin	Inverter Phase	Rectifier Phase
240	802	450	301	762	423	362	720	400
241	802	449	302	761	423	363	720	399
242	801	448	303	760	423	364	719	399
243	800	447	304	760	422	365	718	398
244	800	446	305	759	422	366	717	397
245	799	445	306	758	421	367	717	397
246	798	445	307	758	421	368	716	396
247	798	444	308	757	421	369	715	396
248	797	443	309	756	420	370	715	395
249	796	442	310	756	420	371	714	394
250	796	441	311	755	420	372	713	394
251	795	440	312	754	419	373	713	393
252	794	439	313	754	419	374	712	392
253	794	438	314	753	418	375	711	392
254	793	438	315	752	418	376	711	391
255	792	437	316	752	418	377	710	390
256	792	437	317	751	417	378	709	390
257	791	436	318	750	417	379	708	389
258	790	436	319	750	416	380	708	388
259	790	435	320	749	416	381	707	388
260	789	435	321	748	416	382	706	388
261	788	435	322	748	416	383	706	387
262	788	435	323	747	415	384	705	387
263	787	434	324	746	415	385	704	387
264	786	434	325	745	415	386	704	387
265	786	434	326	745	415	387	703	386
266	785	434	327	744	414	388	702	386
267	784	433	328	743	414	389	702	386
268	784	433	329	743	414	390	701	386
269	783	433	330	742	414	391	700	385
270	782	433	331	741	413	392	699	385
271	782	432	332	741	413	393	699	385
272	781	432	333	740	413	394	698	385
273	780	432	334	739	412	395	697	384
274	780	432	335	739	412	396	697	384
275	779	431	336	738	412	397	696	384
276	778	431	337	737	411	398	695	383
277	778	431	338	737	411	399	695	383
278	777	431	339	736	411	400	694	383
279	776	430	340	735	410	401	693	383
280	776	430	341	735	410	402	692	382
281	775	430	342	734	410	403	692	382
282	774	429	343	733	409	404	691	382
283	774	429	344	733	409	405	690	381
284	773	429	345	732	408	406	690	381
285	772	429	346	731	408	407	689	381
286	772	428	347	731	407	408	688	381
287	771	428	348	730	407	409	687	380
288	770	428	349	729	407	410	687	380
289	770	427	350	728	406	411	686	380
290	769	427	351	728	406	412	685	379
291	768	427	352	727	405	413	685	379
292	768	426	353	726	405	414	684	379
293	767	426	354	726	404	415	683	378
294	766	426	355	725	404	416	683	378
295	766	425	356	724	403	417	682	378
296	765	425	357	724	403	418	681	378
297	764	425	358	723	402	419	680	377
298	764	424	359	722	401	420	680	377
299	763	424	360	722	401	421	679	377
300	762	424	361	721	400	422	678	376

Table F-8: Experimental Data for VFX Mode Operation of the ICN Converter

Operating Point		Power Supply		Power Meter		Load		Power Meter		Inv. Phase	Rec. Phase	Calculated			Power Meter
Vin	Vout	Vin	Iin	Vin	Iin	Vout	Iout	Vout	Iout			Pin	Pout	Eff.	Eff.
20	1	20.1	0.08	20.13	0.0732	1.01	1.2	1.02	1.1456	802	450	1.474	1.169	0.79301	0.79224
40	2	39.8	0.15	39.89	0.1453	2.02	2.3	2.034	2.272	802	450	5.796	4.621	0.79731	0.79712
80	4	80.2	0.295	80.25	0.2906	4.03	4.7	4.081	4.5708	802	450	23.321	18.653	0.79987	0.79975
120	6	120.5	0.442	120.74	0.4387	5.92	7.3	6.109	6.682	802	450	52.969	40.820	0.77065	0.77053
160	8	160.6	0.588	161.01	0.5831	8.02	9	8.139	8.855	802	450	93.885	72.071	0.76765	0.76750

F.4 Reconfigurable Double Stacked Active Bridge Converter Operation

The reconfigurable double stacked active bridge converter of Chapter 5 in normal mode is designed to operate at 175 kHz with a 50% duty ratio. The dead-time between when one half-bridge device turns off and before the other turns on is set to 90 increments (or 93.6 ns) for the inverter and 15 increments (or 15.6 ns) for the rectifier. The inverter dead-time was adjusted to ensure that the voltage across the switch is able to approach ZVS as close as it can. This is signified by the slope of the voltage approaching zero during the transition. The rectifier dead-time is lowered to reduce the amount of time the "body diode" of the GaNFET is conducting while still ensuring shoot-through does not occur. The parameters are therefore set as:

```
Master Period 05412
Master Duty Cycle 002706

     Duty  Phase Dead
Unit Cycle Shift Time
PWM1 00940 00000 00090
PWM2 00940 00000 00090
PWM3 00940 00000 00090
PWM4 00940 00000 00090
PWM5 00940 00000 00015
PWM6 00940 00000 00015
PWM7 00940 00000 00015
PWM8 00940 00000 00015
```

PWM1 and PWM2 are the half-bridge gate signals for the top inverter. PWM3 and PWM4 are the half-bridge gate signals for the bottom inverter. PWM5 and PWM 6 are identical and are used to drive the rectifier half-bridges connected to the output resonant tank. PWM7 and PWM8 are identical and are used to drive the rectifier half-bridges connected to the negative terminal of both transformers. Because there are three paralleled half-bridges for each rectifier half-bridge but only enough channels for 4 gate drive signals, jumper cables are used on the board to connect the remaining two half-bridges.

The two inverters are operated together, so no phase shift is necessary between inverters. The rectifier is phase shifted to control power. To increase power, the phase shift is increased. For the initial startup routine, we choose to set the rectifier phase shift at 200 increments (208 ns or about 3.65% of the total 175 kHz period). This allows enough power so that the current is high enough for ZVS but not at the rated power to reduce stress on the devices. The command terminal will look like the following:

```
Full Drive Mode Enabled

Converter Running in Full Drive Mode
Burst on time = 00025
```

```
Burst total time = 00025
Rectifier phase = 00001
Rectifier phase = 00002
Rectifier phase = 00003
...
Rectifier phase = 00198
Rectifier phase = 00199
Rectifier phase = 00200
```

The input voltage from the dc power supply is first set to 20 V and the electronic load is set to voltage mode. For the startup routine, the output voltage is always the input voltage from the power supply divided by 32. This comes from the fact that each primary winding sees a quarter of the input voltage and steps down the voltage by the turns ratio, which is 16 for this prototype. So for an initial input voltage of 20 V, the output voltage is set to 0.625 V and this ratio is maintained. When operated in this way, the current will have a flattop trapezoidal waveform. An example set of startup operating points can be found in Table F-9.

Once 380 V is reached for the input voltage, the output voltage can be set to 12 V and the power can be modulated by incrementing and decrementing the rectifier phase shift. Across this power range, the output voltage should be maintained at 12 V. For this, we rely on the reading of the Yokogawa WT1800 power meter instead of the load voltage. For this board, Rose Abramson set up multimeters to measure the power that comes from the control board to run the gate drivers. This method uses the fact that ribbon cables come from the control board. Each ribbon cable has two pins with a regulated 5 V rail, two pins with an unregulated 9 V rail, a pin for the high-side device drive signal, a pin for the low-side device drive signal, and two pins for ground. To measure the power from the 5 V and 9 V rails, the ribbon cable was cut to measure the current through a multimeter and the voltage. This was done for one PWM channel for the inverter and another PWM channel for the rectifier. It would be too cumbersome to measure all 8 channels simultaneously. We assume there is very little variance in the power between the 4 inverter channels and 4 rectifier channels given the balanced nature of the waveforms. A full detailed explanation of the setup can be found in Rose's thesis [78].

The operating parameters and efficiency measurements for the GaN-based reconfigurable double stacked active bridge converter of Figure 5-13 to create the graph of Figure 5-29 can be found in Table F-10. The operating parameters and efficiency measurements for the Si-based reconfigurable double stacked active bridge converter of Figure 5-14 to create the graph of Figure 5-30 can be found in Table F-11. The operating parameters and efficiency measurements for the Si-based single stacked active bridge converter of Figure 5-15 to create the graph of Figure 5-31 can be found in Table F-12. It should be noted that all of these operating parameters and data were gathered by Rose Abramson.

Table F-9: Experimental Data for Normal Operation of the Reconfigurable Double Stacked Active Bridge Converter During Startup

Operating Point		Power Supply	Power Meter		Load	Power Meter		Inv. Phase	Rec. Phase	Phase (%)	Calculated			Power Meter
Vin	**Vout**	**Vin**	**Vin**	**Iin**	**Vout**	**Vout**	**Iout**				**Pin**	**Pout**	**Eff.**	**Eff.**
20	0.625	19.9	19.982	0.0277	0.630	0.628	0.854	0	200	3.64	0.55	0.54	0.9697	0.9737
40	1.25	40.2	40.248	0.0581	1.240	1.254	1.821	0	200	3.64	2.34	2.28	0.9768	0.9774
80	2.5	80.2	80.290	0.1197	2.450	2.507	3.746	0	200	3.64	9.61	9.39	0.9770	0.9768
120	3.75	120.5	120.610	0.1837	3.670	3.745	5.774	0	200	3.64	22.16	21.62	0.9760	0.9757
160	5	160.6	160.670	0.2454	4.880	5.014	7.665	0	200	3.64	39.43	38.43	0.9747	0.9747
200	6.25	200.1	200.540	0.3079	6.090	6.249	9.617	0	200	3.64	61.75	60.10	0.9733	0.9732
260	8.125	260.3	260.690	0.4018	7.900	8.130	12.495	0	200	3.64	104.75	101.58	0.9698	0.9698
290	9.0625	290	290.910	0.4499	8.820	9.054	13.994	0	200	3.64	130.88	126.70	0.9681	0.9680
320	10	320	320.720	0.4964	9.740	10.009	15.366	0	200	3.64	159.21	153.80	0.9660	0.9661
350	10.9375	350	350.930	0.5453	10.640	10.917	16.909	0	200	3.64	191.36	184.60	0.9646	0.9647
380	11.875	380.1	381.000	0.5933	11.570	11.857	18.370	0	200	3.64	226.05	217.81	0.9636	0.9636
410	12.8125	410.1	411.210	0.6404	12.460	12.812	19.782	0	200	3.64	263.34	253.45	0.9624	0.9625

Table F-10: Experimental Data for Normal Operation of the GaN-based Reconfigurable Double Stacked Active Bridge Converter with a Fixed Input Voltage of 380 V and a Fixed Output Voltage of 12 V. The inverter phase shift is kept at 0.

Power Meter		Inverter 9V Gate Power		Inverter 5V Gate Power		Rectifier Gate Power		Power Meter		Rec. Phase	Phase (%)	Calculated		
Vin	Iin	V	I (mA)	V	I (mA)	V	I (mA)	Vout	Iout			Pin	Pout	Eff.
380.62	0.3122	9.3987	5.566	5.0032	1.4406	4.9829	7.91	11.998	9.299	400	7.28	118.83	111.57	0.9352
380.63	0.2929	9.3987	5.5645	5.0032	1.4406	4.9829	7.828	12.005	8.747	375	6.83	111.49	105.01	0.9379
380.64	0.2734	9.3988	5.564	5.0032	1.44075	4.9829	7.737	11.998	8.201	350	6.37	104.07	98.40	0.9413
380.62	0.2528	9.3988	5.564	5.0032	1.4409	4.9829	7.68	12.004	7.605	325	5.92	96.22	91.29	0.9442
380.63	0.2312	9.3988	5.565	5.0032	1.4411	4.9828	7.647	11.996	6.985	300	5.46	88.00	83.79	0.9471
380.63	0.2083	9.3988	5.563	5.0032	1.44125	4.9828	7.598	12.001	6.311	275	5.01	79.29	75.74	0.9497
380.64	0.1844	9.3986	5.571	5.0032	1.4413	4.9827	7.488	12.007	5.6	250	4.55	70.19	67.24	0.9517
380.64	0.1598	9.3986	5.571	5.0032	1.4412	4.9827	7.343	11.996	4.864	225	4.10	60.83	58.35	0.9521
380.64	0.1348	9.3988	5.568	5.0031	1.4412	4.9826	7.251	12	4.098	200	3.64	51.31	49.18	0.9500
380.65	0.1075	9.3988	5.5645	5.0031	1.4419	4.9826	7.107	12.004	3.256	175	3.19	40.92	39.09	0.9448
380.65	0.0851	9.3987	5.573	5.0031	1.4429	4.9826	6.995	11.995	2.5516	155	2.82	32.39	30.61	0.9320
380.66	0.0833	9.3987	5.5725	5.0031	1.44305	4.9826	6.986	12.01	2.4889	154	2.80	31.71	29.89	0.9296
380.66	0.0794	9.3987	5.574	5.0031	1.4433	4.9826	6.979	12.007	2.3681	150	2.73	30.22	28.43	0.9270
380.66	0.0514	9.3988	5.5715	5.0031	1.4443	4.9828	6.828	11.994	1.4716	125	2.28	19.57	17.65	0.8821
380.66	0.0342	9.3988	5.5775	5.0031	1.4472	4.9828	6.765	12.002	0.9134	110	2.00	13.02	10.96	0.8145
380.66	0.0331	9.3987	5.578	5.0031	1.4472	4.9828	6.757	12.003	0.8749	109	1.98	12.60	10.50	0.8053
380.66	0.0318	9.3988	5.5794	5.0031	1.44705	4.9829	6.749	12.001	0.8339	108	1.97	12.10	10.01	0.7977
380.66	0.0307	9.3988	5.5794	5.0031	1.447	4.9829	6.744	12.002	0.7963	107	1.95	11.69	9.56	0.7881

Table F-11: Experimental Data for Normal Operation of the Si-based Reconfigurable Double Stacked Active Bridge Converter with a Fixed Input Voltage of 380 V and a Fixed Output Voltage of 12 V. The inverter phase shift is kept at 0.

Power Meter		Inverter 9V Gate Power		Inverter 5V Gate Power		Rectifier Gate Power		Power Meter		Rec. Phase	Phase (%)	Calculated		
Vin	Iin	V	I (mA)	V	I (mA)	V	I (mA)	Vout	Iout			Pin	Pout	Eff.
380.59	0.3175	9.3766	6.937	5.0031	1.4063	4.9794	7.032	11.997	9.255	422	7.68	120.84	111.03	0.9151
380.59	0.3008	9.3766	6.9375	5.0031	1.4062	4.9794	7.005	12.006	8.801	400	7.28	114.48	105.67	0.9190
380.59	0.2807	9.3765	6.94	5.0031	1.4065	4.9794	6.943	11.999	8.262	375	6.83	106.83	99.136	0.9237
380.6	0.274	9.3765	6.9415	5.0031	1.4068	4.9794	6.918	11.995	8.078	366	6.66	104.28	96.896	0.9248
380.59	0.2477	9.3768	6.93	5.0031	1.407	4.9793	6.884	12.001	7.348	335	6.10	94.272	88.183	0.9305
380.6	0.221	9.3755	7.0145	5.0031	1.4072	4.9793	6.838	12.005	6.591	305	5.55	84.113	79.125	0.9352
380.61	0.1958	9.3737	7.134	5.0031	1.4072	4.9791	6.855	11.994	5.874	277	5.04	74.523	70.453	0.9391
380.61	0.1685	9.3734	7.152	5.0031	1.4074	4.979	6.816	11.999	5.068	249	4.53	64.133	60.811	0.9409
380.61	0.1423	9.3731	7.1688	5.0031	1.4074	4.9788	6.873	12.005	4.288	222	4.04	54.161	51.477	0.9417
380.62	0.113	9.3696	7.3995	5.0031	1.4081	4.9786	6.911	12.007	3.394	194	3.53	43.010	40.752	0.9363
380.63	0.0853	9.3695	7.4095	5.0031	1.409	4.9786	6.886	11.995	2.5376	167	3.04	32.468	30.439	0.9230
380.64	0.0848	9.3694	7.4135	5.0031	1.4091	4.9786	6.885	12.009	2.5146	167	3.04	32.278	30.198	0.9209
380.64	0.0567	9.3673	7.54	5.003	1.4099	4.9788	6.81	11.998	1.6258	139	2.53	21.582	19.506	0.8828
380.64	0.0402	9.3401	9.369	5.0029	1.4102	4.979	6.65	12.006	1.0871	123	2.24	15.302	13.052	0.8220
380.64	0.0331	9.3117	11.34	5.0028	1.4099	4.9791	6.59	12.002	0.8603	116	2.11	12.599	10.325	0.7795
380.49	0.0328	9.3111	11.38	5.0028	1.4099	4.9791	6.61	12.002	0.8493	116	2.11	12.480	10.193	0.7764

Table F-12: Experimental Data for Normal Operation of the Si-based Single Stacked Active Bridge Converter with a Fixed Input Voltage of 380 V and a Fixed Output Voltage of 12 V. The inverter phase shift is kept at 0.

Power Meter		Inverter 9V Gate Power		Inverter 5V Gate Power		Rectifier Gate Power		Power Meter		Rec. Phase	Phase (%)	Calculated		
Vin	Iin	V	I (mA)	V	I (mA)	V	I (mA)	Vout	Iout			Pin	Pout	Eff.
380.43	0.8283	9.3088	11.962	5.00325	1.44425	4.9829	7.632	11.994	25.055	322	5.8604	315.11	300.51	0.9523
380.58	0.8232	9.3088	11.976	5.00325	1.4442	4.983	7.584	12.01	24.876	321	5.8422	313.29	298.76	0.9522
380.58	0.8291	9.309	11.959	5.0032	1.44415	4.983	7.631	11.996	25.079	322	5.8604	315.54	300.85	0.9520
380.58	0.8239	9.3089	11.968	5.0032	1.4441	4.9831	7.588	11.995	24.932	321	5.8422	313.56	299.06	0.9523
380.59	0.7594	9.3078	12.057	5.0032	1.4435	4.9832	7.44	11.999	23.012	305	5.551	289.02	276.12	0.9538
380.6	0.6876	9.3068	12.123	5.0032	1.4424	4.9832	7.312	12	20.813	287	5.2234	261.70	249.76	0.9527
380.6	0.6591	9.3059	12.15	5.0033	1.4418	4.9829	6.579	12	19.953	280	5.096	250.85	239.44	0.9528
380.6	0.575	9.3046	12.249	5.0033	1.4426	4.983	6.503	11.995	17.402	260	4.732	218.85	208.74	0.9519
380.6	0.4922	9.3034	12.338	5.0032	1.4419	4.983	6.47	12.006	14.771	240	4.368	187.33	177.34	0.9445
380.6	0.4079	9.3025	12.399	5.0033	1.44105	4.9831	6.49	12.002	12.152	220	4.004	155.25	145.85	0.9368
380.62	0.3295	9.3022	12.461	5.0032	1.4395	4.9833	6.611	11.999	9.591	200	3.64	125.41	115.08	0.9144
380.63	0.2486	9.3015	12.511	5.0032	1.439	4.9832	6.617	12.009	6.986	180	3.276	94.62	83.8949	0.8825
380.63	0.1756	9.301	12.546	5.0032	1.4383	4.983	6.69	12.006	4.579	160	2.912	66.84	54.9755	0.8170
380.64	0.1131	9.3005	12.583	5.0032	1.4372	4.983	6.733	12.008	2.4908	143	2.6026	43.05	29.9095	0.6876
380.64	0.1028	9.3005	12.585	5.0032	1.4371	4.983	6.725	12.004	2.1472	140	2.548	39.13	25.7750	0.6512
380.5	0.0647	9.3004	12.602	5.0032	1.435	4.9831	6.67	12.001	0.8495	130	2.366	24.62	10.195	0.4067
380.63	0.062	9.3003	12.601	5.0032	1.4352	4.9831	6.69	12	0.7678	129	2.3478	23.60	9.214	0.3831

To operate the converter in low-power mode, it must be enabled from the control interface. Once enabled, the converter can be operated in a very similar fashion as the normal mode. The inverters have no phase shift between them, and the rectifier phase shift is set high enough to ensure ZVS but not too high to keep switch stress low. For the low-power mode, the rectifier shift is set to 300 increments as the converter goes through the same voltage startup routine. The command terminal will look like the following:

```
Half Drive Mode Enabled

Converter Running in Half Drive Mode
Rectifier phase = 00001
Rectifier phase = 00002
Rectifier phase = 00003
...
Rectifier phase = 00298
Rectifier phase = 00299
Rectifier phase = 00300
```

Once 380 V is reached for the input voltage, the output voltage can be set to 12 V and the power can be modulated by incrementing and decrementing the rectifier phase shift. Across this power range, the output voltage should be maintained at 12 V. The operating parameters and efficiency measurements for the GaN-based reconfigurable double stacked active bridge converter of Figure 5-13 to create the graph of Figure 5-29 can be found in Table F-10. Again, it should be noted that this data was collected by Rose Abramson.

Table F-13: Experimental Data for Normal Operation of the GaN-based Reconfigurable Double Stacked Active Bridge Converter Operated in Low-Power Mode with a Fixed Input Voltage of 380 V and a Fixed Output Voltage of 12 V. The inverter phase shift is kept at 0.

Power Meter		Inverter 9V Gate Power		Inverter 5V Gate Power		Rectifier Gate Power		Power Meter		Rec. Phase	Phase (%)	Calculated		
Vin	**Iin**	**V**	**I (mA)**	**V**	**I (mA)**	**V**	**I (mA)**	**Vout**	**Iout**			**Pin**	**Pout**	**Eff.**
380.62	0.3122	9.3987	5.566	5.0032	1.4406	4.9829	7.91	11.998	9.299	400	7.28	118.83	111.57	0.9352
380.63	0.2929	9.3987	5.5645	5.0032	1.4406	4.9829	7.828	12.005	8.747	375	6.83	111.49	105.01	0.9379
380.64	0.2734	9.3988	5.564	5.0032	1.44075	4.9829	7.737	11.998	8.201	350	6.37	104.07	98.40	0.9413
380.62	0.2528	9.3988	5.564	5.0032	1.4409	4.9829	7.68	12.004	7.605	325	5.92	96.22	91.29	0.9442
380.63	0.2312	9.3988	5.565	5.0032	1.4411	4.9828	7.647	11.996	6.985	300	5.46	88.00	83.79	0.9471
380.63	0.2083	9.3988	5.563	5.0032	1.44125	4.9828	7.598	12.001	6.311	275	5.01	79.29	75.74	0.9497
380.64	0.1844	9.3986	5.571	5.0032	1.4413	4.9827	7.488	12.007	5.6	250	4.55	70.19	67.24	0.9517
380.64	0.1598	9.3986	5.571	5.0032	1.4412	4.9827	7.343	11.996	4.864	225	4.10	60.83	58.35	0.9521
380.64	0.1348	9.3988	5.568	5.0031	1.4412	4.9826	7.251	12	4.098	200	3.64	51.31	49.18	0.9500
380.65	0.1075	9.3988	5.5645	5.0031	1.4419	4.9826	7.107	12.004	3.256	175	3.19	40.92	39.09	0.9448
380.65	0.0851	9.3987	5.573	5.0031	1.4429	4.9826	6.995	11.995	2.5516	155	2.82	32.39	30.61	0.9320
380.66	0.0833	9.3987	5.5725	5.0031	1.44305	4.9826	6.986	12.01	2.4889	154	2.80	31.71	29.89	0.9296
380.66	0.0794	9.3987	5.574	5.0031	1.4433	4.9826	6.979	12.007	2.3681	150	2.73	30.22	28.43	0.9270
380.66	0.0514	9.3988	5.5715	5.0031	1.4443	4.9828	6.828	11.994	1.4716	125	2.28	19.57	17.65	0.8821
380.66	0.0342	9.3988	5.5775	5.0031	1.4472	4.9828	6.765	12.002	0.9134	110	2.00	13.02	10.96	0.8145
380.66	0.0331	9.3987	5.578	5.0031	1.4472	4.9828	6.757	12.003	0.8749	109	1.98	12.60	10.50	0.8053
380.66	0.0318	9.3988	5.5794	5.0031	1.44705	4.9829	6.749	12.001	0.8339	108	1.97	12.10	10.01	0.7977

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