Prospects of Germanium-based MOSFETs and Tunnel Transistors for Low Power Digital Logic

by

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Abstract

Moore's law has driven technological improvements for decades by halving the areal footprint of the transistor every two years and increasing the performance of making integrated circuits while reducing their cost. The ability to reduce the footprint of the device was enabled by advances in processing technology, novel materials and device design. As ever-smaller footprints are desired, power density limitations and performance degradation require more innovations on all fronts. Recently introduced improvements to integrated circuits are high-κ and metal gate for MOSFETs (45-nm node onward), the FinFET (22-nm node onward) and air gaps between copper interconnects (14-nm node) illustrating that at every new technology node there needs to be a materials or process-related improvement to reduce power and maintain performance. Other approaches are also being explored or taken to further improve the MOSFET performance in future technology nodes, namely use of channel materials with higher carrier mobility such as SiGe and Ge for p-MOSFETs, III-V compound semiconductors for n-MOSFETs and steep subthreshold swing devices such as tunnel field effect transistors (TFETs).

This work evaluates both approaches utilizing germanium (Ge) and strained-Ge as a material to understand the benefits and drawbacks to both approaches. Hypothetically, high

carrier mobility and velocity channel materials can lower the overall power consumption because lower power supply voltage is required to obtain the same amount of current. Germanium and strained-Ge are candidates for the channel material of p-MOSFETs. MOSFETs made using Ge and strained-Ge as the channel material are evaluated based upon the ITRS roadmap requirements using experimental results in this work and data from literature. The approach for using TFETs was evaluated in this work also using germanium as a channel material. TFETs can have a steep subthreshold swing (SS), better than the minimum of 60 mV/decade at room temperature for a MOSFET, which also reduces the total power and supply voltage required for operation. The reduced SS is hypothetically achieved through the band-to-band tunneling which allows for the filtering of the Fermi-tail distribution of carriers. Experimentally, TFETs have not generally shown the steeper than Fermi-tail SS promised by the theory and this work uses both results from fabricated strained-Si/strained-Ge TFETs as well as modeling to explain why this has been the case. The challenges for both technologies are outlined in this thesis and suggestions are made on approaches to tackling their respective intrinsic problems from the point of view of Ge-based devices.

Acknowledgements

The adventure along the way and the experiences that it provides are the important lessons from the beginning to the end of the time covered in this thesis. First, I would like to express my gratitude to those have contributed directly to my work at MIT beginning with my advisors Judy Hoyt and Dimitri Antoniadis who have given me a large amount of guidance while also showing a large amount of patience and gave leniency to allow me to explore all sorts of different topics. Judy taught me the basics of doing research and communicating the things that I learned from step-by-step experimental design all the way to presentations. She generously gave me lots of attention and dedicated much time to advancing my professional prospects. Dimitri took me on as a student in lieu of Judy part-way through my time here and reinforced all of the principle that Judy had taught me, but also drove home characteristics that I lacked, preciseness and discipline. The generosity of both Judy and Dimitri has contributed greatly to the quality of my experience here at MIT. Other professors within MTL have also been very open to discussions with special mentions for my committee members, Gene Fitzgerald and Tayo Akinwande, which have been helpful for all sorts of questions

The facilities and staff at the Microsystems Technology Laboratories (MTL) which this work relied on have also been excellent. The specialists have been very prompt in training, assisting and reacting when anything went wrong and the speed at which things were fixed enabled the progress made in fabrication at the facilities. Leniency and exceptions to procedures also expedited the work done in the labs and I am grateful to those who afforded me such luxuries. I would like to especially thank Gary Riggott for his processing and epitaxial growth assistance as well as Vicky Diaduk, Mark Mondol, Paul Tierney, Paul McGrath, Eric Lim, Bob Bicchieri, Bernard Alamariu, Kurt Broderick, Donal Jamieson, Kristofor Payer and Scott Poesse,

in no particular order, for their expertise and helpfulness. Judy and Dimitri's administrators, Whitney Rokui, Loriann McCormick, Janna Atcheson and Steven O'Hearn, and MTL administrators with special mention for Valerie DiNardo, Debroah Hodge-Pabon and Joseph Baylon have also been very helpful in making everything run smoothly; they have fulfilled my seemingly random requests with a smile.

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This was made possible by the sponsors to the project, MSD/FCRP, IBM and the NSF energy efficient electronics (E3S) programs, as well as my previous advisor, Xiuling Li, who

gave me the opportunity to come to MIT through her guidance which contributed to the fact that I eventually chose Judy as an advisor.

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The time I spent with people while at MTL only tells part of the story, and would not have been complete without a mention of the time that I spent with friends both inside and outside of Boston. While the company inside MTL was great, I am glad that I was able to spend time with different people outside of the lab, playing video/board games and for meals with people here at MIT. My friends that I have made during my time at the University of Illinois have also contributed to my experience here but from afar through conversations over the internet, video games or the occasional visit.

Last but not least, my friends who have been with me through high school have been some of my strongest influences. They congregated in Houston from Cincinnati while I was here in Boston which has offered me somewhere to reside when I wanted somewhere to relax, a home away from home. They have taught me so much that graduate school that could not by offering a different viewpoint relative to the like-minded people around me. Most importantly of all though, they inspire my conviction to maintain my beliefs and speculations, despite the fact that many people oppose them, until the theories can be proven right or wrong.

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Chapter 1: Introduction

Silicon integrated circuits have driven technological advancements such as the modern computer, the internet, laptops and smartphones. Significant progress in the cost, functionality and performance of silicon (Si) integrated circuits (ICs) has been made since one was first fabricated [1]. The all-around improvement in Si ICs have been driven by Moore's law [2-4] which states that the number of transistors on the chip increases by a factor of 2 every 2 years. The increase in the number of transistors was possible because engineers were able to decrease the areal footprint of transistors by 50% every 2 years. While Moore's law is not a fundamental law of nature, it has continued since the early days of Si integrated circuits and will likely continue for the next few years [3, 4].

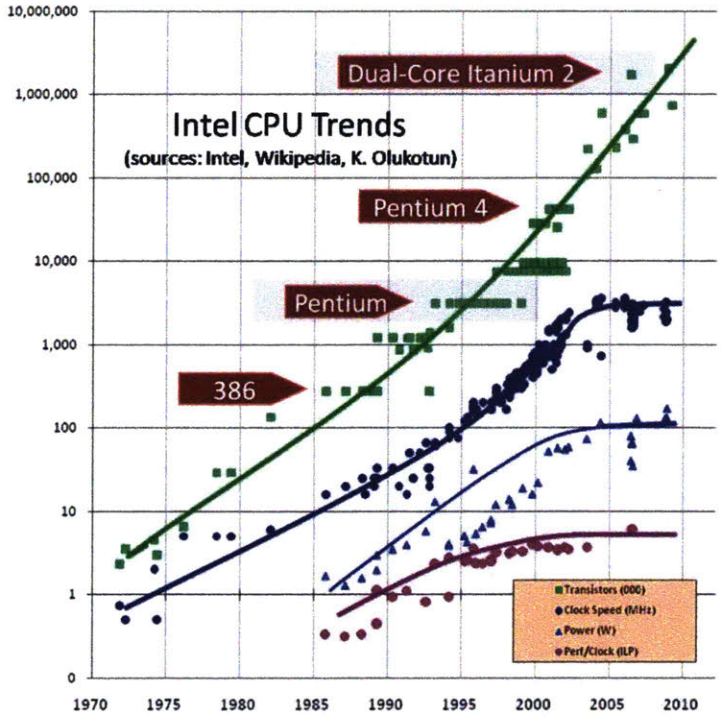


Figure 1.1. Transistors (green), Clock speed (dark blue), Power (blue), Performance per clock (purple) as a function of time for Intel CPUs [5]. The number of transistors per CPU has increased exponentially over time while other metrics have saturated around 2002.

The benefits of a few figures of merits (FOMs) can be visualized in Figure 1.1. The graph shows the improvement in integrated circuits for central processing units (CPUs) over time based upon several metrics, number of transistors, clock speed, power and performance per clock [5]. The figures of merit can be broken into two categories, functionality and performance. The functionality of the integrated circuit is proportional to the number of transistors in CPUs which has been increasing exponentially over time. The other figures of merit such as power, frequency and performance per clock are performance metrics and have two regimes: 1.) Pre-2002 where the performance metrics were increasing in an exponential fashion and 2.) Post-2002 where all the figures of merits became constant.

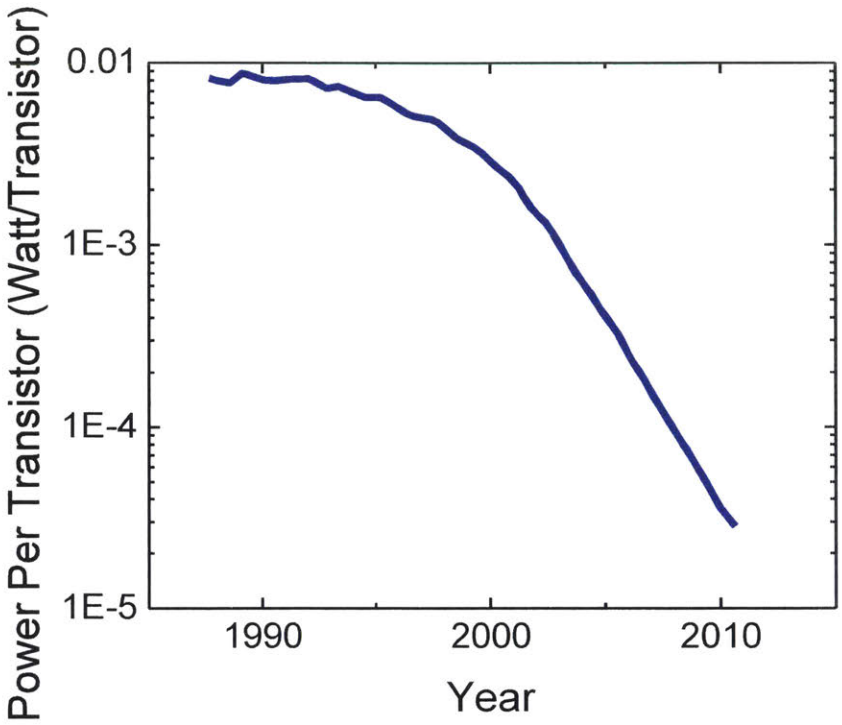


Figure 1.2. Power per transistor extracted from figure 1.1 vs. year. Power per transistor was fairly constant as a function of time until exponential scaling of the power per transistor began around 2002.

The cause of the difference in the two time periods is the change in the figures of merit for scaling. In the time period before 2002, improvements in the clock speed were the important driver for improvements in performance and total power increased with the total number of transistors. One can clearly see that the power per transistor during this time was held constant in figure 1.2. This worked well until one looks at the areal power density for CPUs, figure 1.3. The power density of CPUs approached the power density of 100 W/cm^2 or the power density of 100 suns which made cooling the CPU challenging. This resulted in the need for a change in the figure of merit to maintaining power density or by exponentially reducing power per transistor.

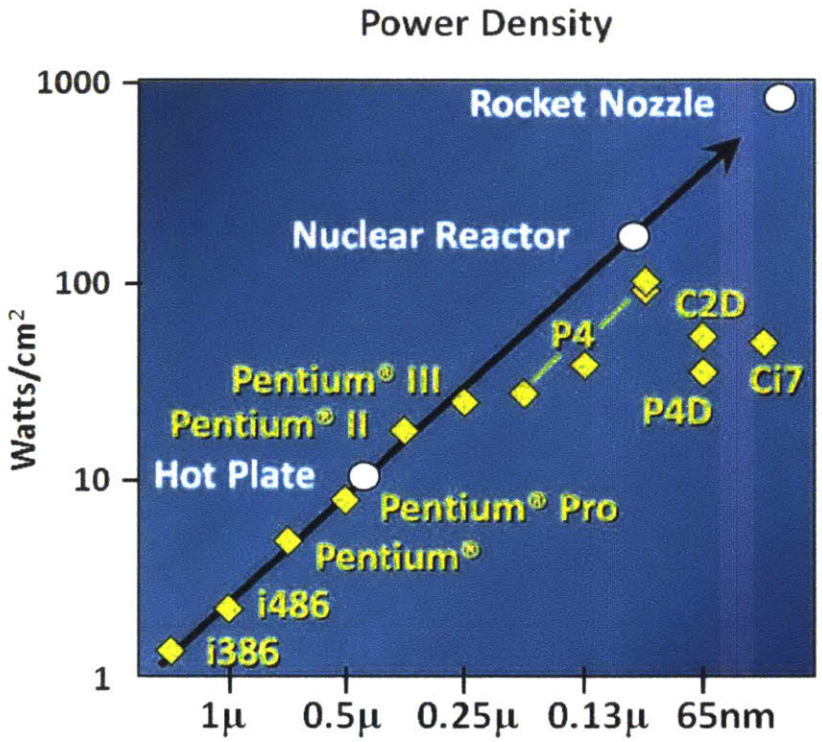


Figure 1.3. Power density (Watts/cm^2) versus the Intel generation for different Intel CPUs (yellow) [6]. Several different power densities are also included such as that of a hot plate, nuclear reactor and rocket nozzle.

Overview

This thesis covers work on future possibilities for further scaling of power per transistor to extend Moore's law. Chapter 2 will cover the technical background on power scaling for digital logic applications and talk about some history behind it. There are a few approaches to reducing the power relative to standard Si MOSFET scaling, and this thesis covers two different approaches to reduce power by allowing reduced power supply voltage with no sacrifice is speed: 1.) Improving carrier mobility and carrier velocity in order to improve drive current or 2.) Improving the switching characteristics of the device. The concepts of using a high mobility and

velocity channel material and tunnel field effect transistors (TFETs) as a steep switching device are introduced and the progress made in both of these categories is discussed.

The first approach will be covered in Chapter 3 which describes in detail the efforts made to develop and assess compressively strained-Ge as a viable candidate for a high hole mobility channel material. This chapter talks about the requirements and approaches made to assess the viability of channel material.

The second approach will be covered in the remainder of the thesis Chapters 4 and 5. TFETs have been previously simulated and fabricated, but experimental TFETs have not shown the steep SS and the high currents that were promised by simulations. Chapter 4 details design considerations for TFETs that were used to explain why the simulations and experiments are so different. It also introduces strained-Si/strained-Ge TFETs used in the experiments as well as the fabrication and basic electrical characteristics of the TFETs. Chapter 5 covers the electrical device characteristics which include temperature-dependent I-V and C-V and characteristics and the electrical results are analyzed and discussed based on an electric-field-enhanced Shockley-Read-Hall model. Chapter 6 concludes this thesis with suggestions for future work.

Chapter 2: Technical Introduction to Power Scaling

The previous chapter established that the power density is the most important figure of merit for scaling digital logic technologies because the power density in CPUs has already reached its limit of ~ 100 W/cm^2.

The power consumption of each transistor in a digital logic circuit is well established and is given by Eq. 2.1.

$$P = \alpha f C V_{DD}^2 + I_{off} V_{DD} \quad \textbf{(2.1)}$$

Where P is the power consumption of one transistor, α is the activity factor or the fraction of clock cycles that the device is switching, f is the clock frequency, C is the load capacitance, V_{DD} is the supply voltage, and I_{off} is the off-state current of the device. The first term of the power equation is the switching power, and the second term is the off-state or static power of the device. Because this is the power per transistor, the power must be divided by the area of the transistor to get the power density. Every future technology node has transistors that have approximately half of the area of the previous node meaning that the power per transistor must be reduced a factor of 2 by each generation in order to have constant power density. The reduction in the power can come from a combination of any of the parameters in Eq. 2.1, but can be conveniently achieved by reducing V_{DD} since it decreases both switching and static power dissipation.

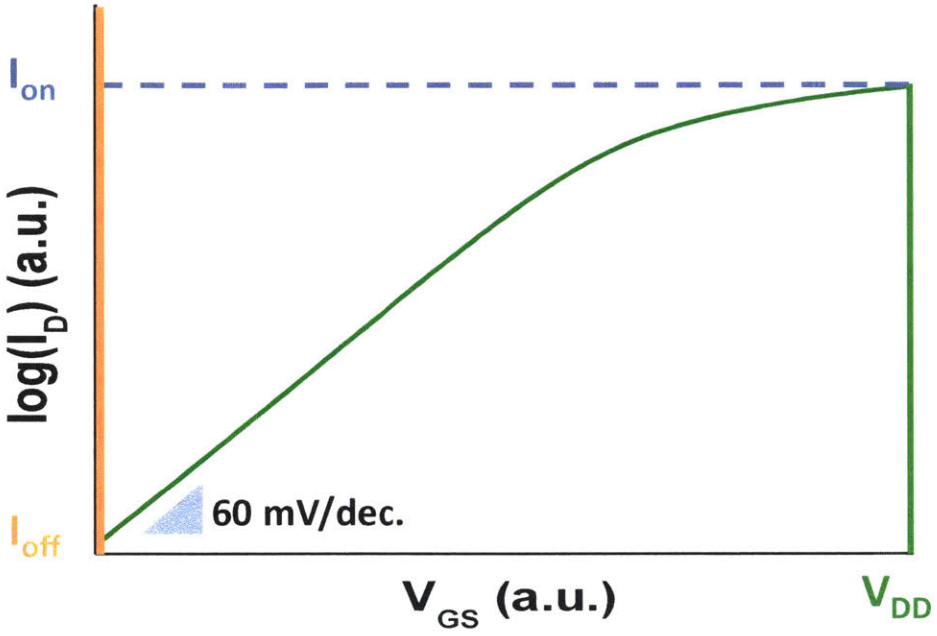


Figure 2.1. Schematic of I_D-V_G or transfer characteristics for an n-MOSFET. The on-state current is defined as the current at a certain supply voltage where $V_{DS} = V_{GS} = V_{DD}$. The off-state current or I_{off} is defined as the point where the transfer characteristics meet the origin or the current when $V_{DS} = V_{DD}$ and $V_G = 0$ V.

The basic transfer characteristics of a MOSFET are shown in Fig. 2.1. The V_{DD} in this figure is defined as the gate voltage, V_{GS}, required to obtain a certain current. The reason why constant current is used as the metric for choosing V_{DD} is due to the fact that the intrinsic delay, defined by equation 2.2, of the transistor is inversely proportional to the on-state current of the device, and it could be analogous to constant performance.

$$\tau_i = \frac{C_G V_{DD}}{I_{on}} \tag{2.2}$$

Where τ_i is the intrinsic transistor delay, C_G is the gate capacitance, V_{DD} is the supply voltage and I_{on} is the on-state current. While the constant on-state current metric is not completely

accurate for predicting constant performance since both capacitance and supply voltage will also change, it is a simple way to show how the trend for V_{DD} would likely change. Many parameters such as the total power, variation and power delay product go into the decision of selecting the V_{DD}. The process of selecting a proper V_{DD} for a specific application is not the focus of this work, and detailed analysis of the design considerations for selecting the V_{DD} has already been done and can be found elsewhere [7].

This chapter gives a technical overview of the strategies employed to scale V_{DD}. The three common approaches considered in order to maintain the power density while scaling the transistor area are discussed; the approaches are: 1.) Varying the threshold voltage of MOSFETs to reduce the active switching power, 2.) Increasing the mobility which is related to the carrier velocity using strain or higher mobility channel materials, and 3.) Using a new device concepts, steep subthreshold swing transistors.

2.1 Threshold voltage scaling for reduced power density

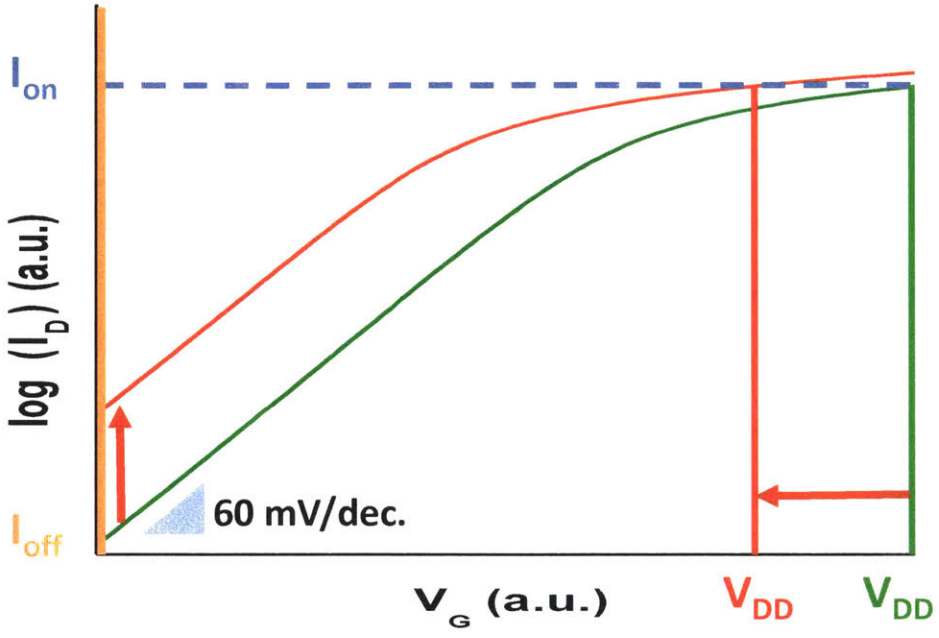


Figure 2.2. Schematic of I_D-V_G or transfer characteristics for two n-MOSFETs. The green curve is the original curve from Fig. 2.1, and the red curve is the transfer characteristic with a less positive threshold voltage. At a constant I_{on}, the V_{DD} is reduced for the device with less positive threshold voltage, but the I_{off} is increased as a result.

The simplest and first methodology that was used to reduce the V_{DD} was varying the threshold voltage of the device by changing the work-function of the gate metal or polysilicon [8, 9]. For an n-MOSFET and p-MOSFET, the threshold voltages would be shifted to less positive and negative values respectively. Figure 2.2 shows the change in transfer characteristics of an n-MOSFET with only the threshold voltage shifted. The V_{DD} is reduced by shifting the threshold voltage to a less positive value which shifts the curve to the left while I_{off} is increased. Looking back at equation 2.1, the reduction in V_{DD} will decrease the switching power, first term, of the

transistor. The second term or the static power is higher which means that this method trades off the switching power for the static power. The reason why the second term is higher is because the off-state current increases exponentially when the threshold voltage is decreased as shown by equation 2.3 [7, 10].

$$I_{off} = I_{threshold} * \exp(-\frac{|V_T|}{SS}) \quad \textbf{(2.3)}$$

Where I_{off} is the off-state current, $I_{threshold}$ is the current at the threshold voltage, V_T is the threshold voltage of the device and SS is the subthreshold swing of the device.

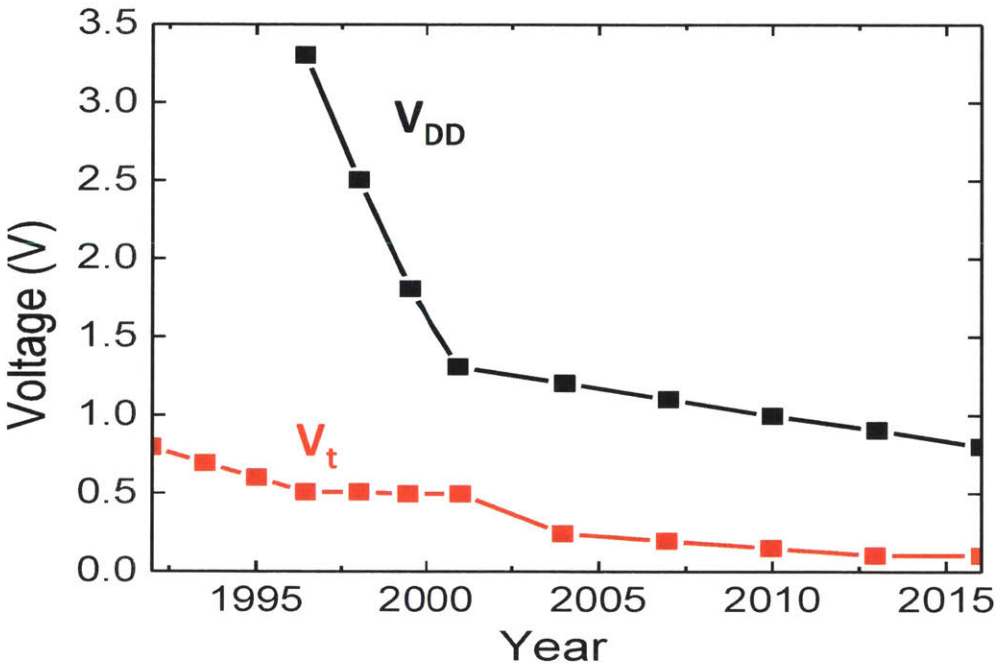


Figure 2.3. The supply voltage and threshold voltage for high performance MOSFETs. The supply voltage has been consistently reduced while the reduction in threshold voltage has slowed over time particularly in the most recent technology node. The data is public information for Intel CPUs and replotted from [11].

The threshold voltage has been reduced as a function of time during the time period shown in the figure, ~1990 to 2016. In the past decade, The V_{DD} has decreased with at a similar rate as the reductions in V_T as seen in Fig. 2.3. However, the ability to continue to reduce V_T is nearing its limit as V_T approaches 0 V [12, 13]. This is evident in the most recent technology node where no V_T shift occurred [13]. There are two ramifications for a V_T of 0 V. First, the reduction in V_T to 0 V is significant because it means that the device ON to OFF current ratio is reduced leading to poor logic noise margins [14]. Second, the higher off-state current results in higher amounts of static power dissipation which is already significant relative to the switching power, as seen in Fig. 2.4. This means that the reduction in the active power may not warrant an increase in the static power [12, 14].

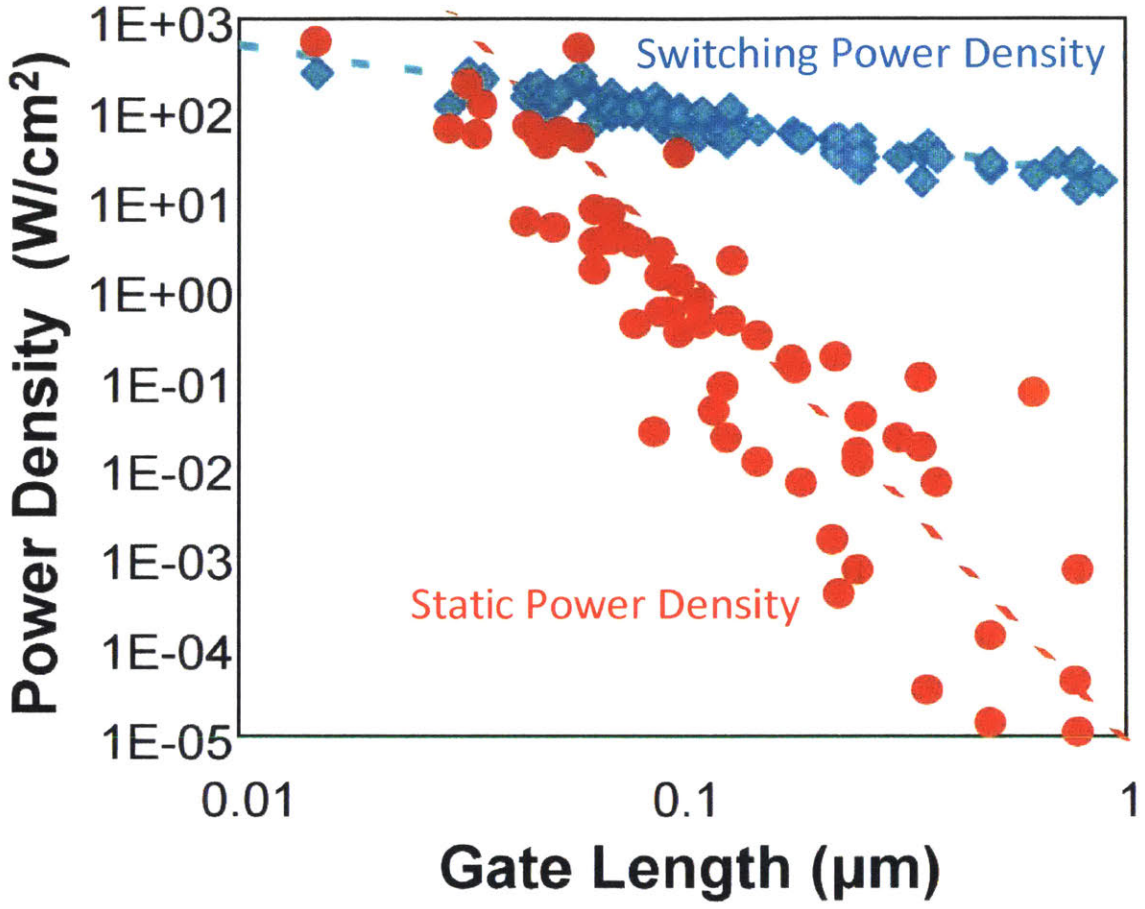


Figure 2.4. The power density of switching and static components as a function of the gate length for planar transistors. Both static and switching power density have a power law relationship with decreasing gate length, but with a different slope. This figure shows that for small gate length MOSFETs, the static power density becomes comparable to the switching power density. This figure is reproduced from [15], but the original data comes from [16].

2.2 Strain and high mobility channel materials

Alternatives to shifting the V_T were investigated for reducing power and/or increasing performance because of the known drawbacks of increasing I_{off}. One alternative is to improve the

drive current of the transistor for a given channel charge, i.e. at constant $V_{GS}=V_{DD}$. The improvement in drive current can be accomplished by reducing the carrier effective mass of the material; this strategy, in principle, does not have the drawback of increasing I_{off}. The impact of reducing the effective mass increases both the mobility and thermal velocity of carriers based upon the relationships given in Eqs. 2.4 and 2.5 respectively:

$$\mu = \frac{q\tau}{m^*} \tag{2.4}$$

$$v_\theta = \sqrt{\frac{2kT}{\pi m^*}} \tag{2.5}$$

Where μ is the carrier mobility, q is the elementary charge, τ is the scattering time, m^* is the conductivity effective mass of the carrier, v_θ is the ballistic mobility, k is Boltzmann's constant and T is the temperature.

The increase in mobility and velocity matter for short-channel devices because it increases the overall drive current for a given channel charge. The drive current is given by Eq. 2.6 where the virtual-source velocity is proportional to the ballistic velocity given by Eq. 2.5 [7, 10, 17, 18],

$$\frac{I_D}{W} = Q_{inv} v_{xo} \tag{2.6}$$

Where I_D is the drain current, W is the width of the device, Q_{inv} is the areal charge density and v_{xo} is the virtual source velocity. The impact of decreasing the effective mass on the transfer characteristics can be visualized by Fig. 2.5 where the on-current can be achieved at a lower V_{DD} without sacrificing I_{off}. Based upon this approach both the switching and static power can be decreased because of the decrease in V_{DD}.

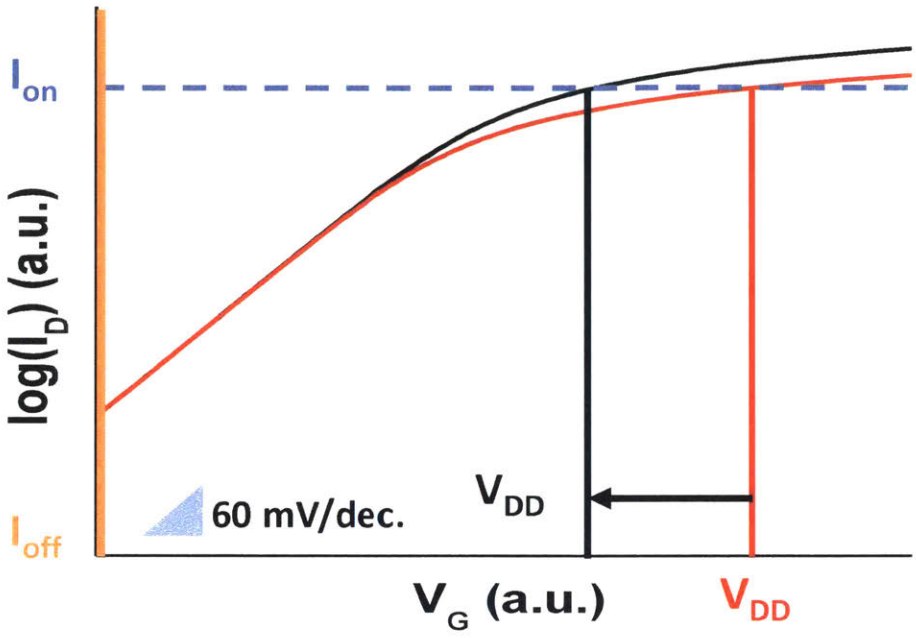


Figure 2.5. Schematic of transfer characteristics for two different n-MOSFETs. The red curve is the red curve from Fig. 2.2, and the black curve is the transfer characteristic with the same threshold voltage but higher field effect electron mobility and velocity or lower effective mass. As defined by a constant I_{on}, the V_{DD} is reduced for the device with a higher field effect mobility and carrier velocity.

The methods that one would go about reducing the carrier effective mass in the channel would be to apply strain to the channel or to replace the channel material with a material with a lower effective mass and hence higher mobility, or both. Strain, given it is the correct orientation i.e. tensile strain for electrons and compressive strain for holes in the direction of transport, is applied in current state-of-the-art transistors in order to boost the device performance [7, 12, 19, 20]. The strain modifies the band structure of the semiconductor resulting in changes in the bandgap and effective mass [21, 22]. If the strain is applied properly, the effective mass in the

transport direction is reduced, but the density of states effective mass in the non-transport directions is increased; this will result in approximately a constant density of states effective mass. As a result, the channel material will have a higher mobility and approximately constant charge and the MOSFET made with the material will have an increased drive current. Band structure calculations can be done to predict the reduction in the transport effective mass and the increase in the carrier velocity for different orientations and magnitude of strain [21, 22].

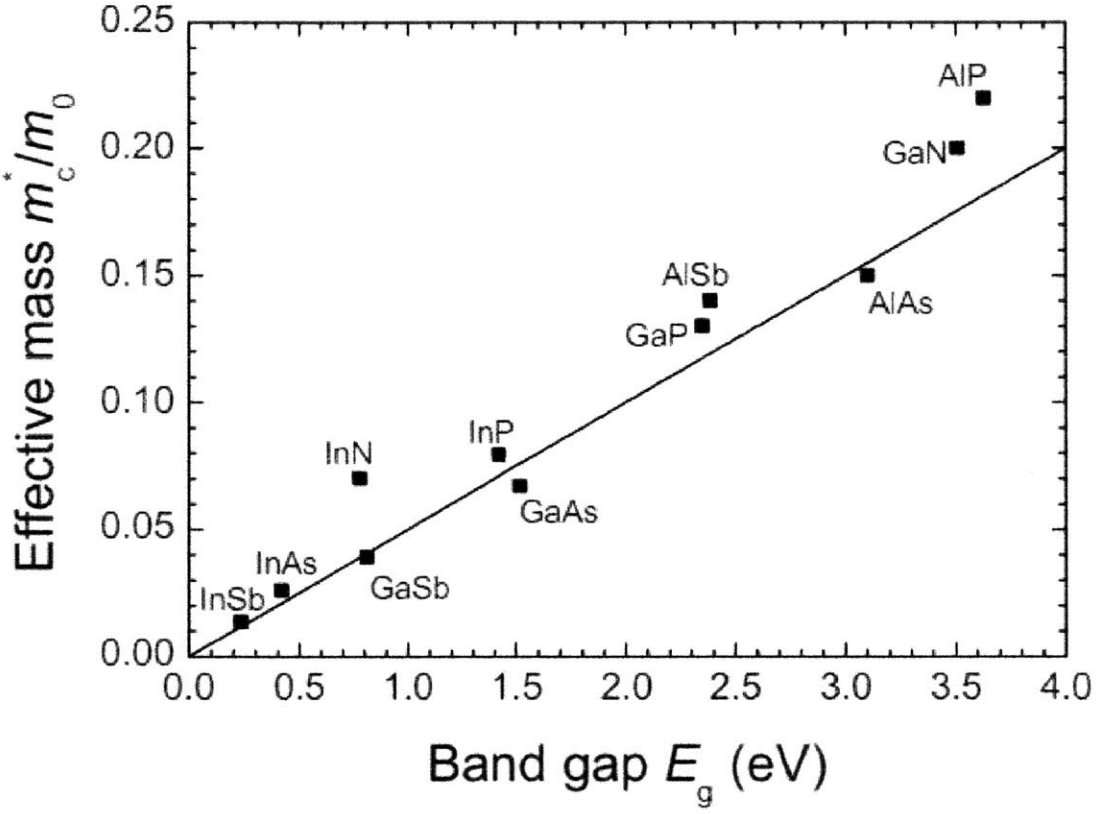


Figure 2.6. Conduction band effective mass versus the bandgap of the material for III-V binary materials. The solid line is the effective mass as predicted by k.p theory. This shows the trend that the effective mass tends to decrease with decreasing bandgap. This figure is directly reproduced from [23].

The other methodology of improving the current is switching materials to a high channel mobility material or a material with a lower effective mass. Instead of applying strain to change the band structure of the material, a different material with a different band structure can be used. If the correct material is selected, the effective mass will be reduced and the carrier mobility and velocity will be increased relative to the incumbent channel material. However, there can be drawbacks to using a different channel material arising from the accompanying bandgap energy, aside from the obvious technological challenge of integrating a different material on the Si platform. The conduction band effective mass versus the bandgap of the material for a few select materials, Fig. 2.6, shows a distinct trend where the effective mass is directly correlated to the bandgap of the material. When the effective mass drops, the bandgap of the material also tends to drop, and the reduction in the bandgap could cause an increase in I_{off} due to the increase in the minimum attainable current [23].

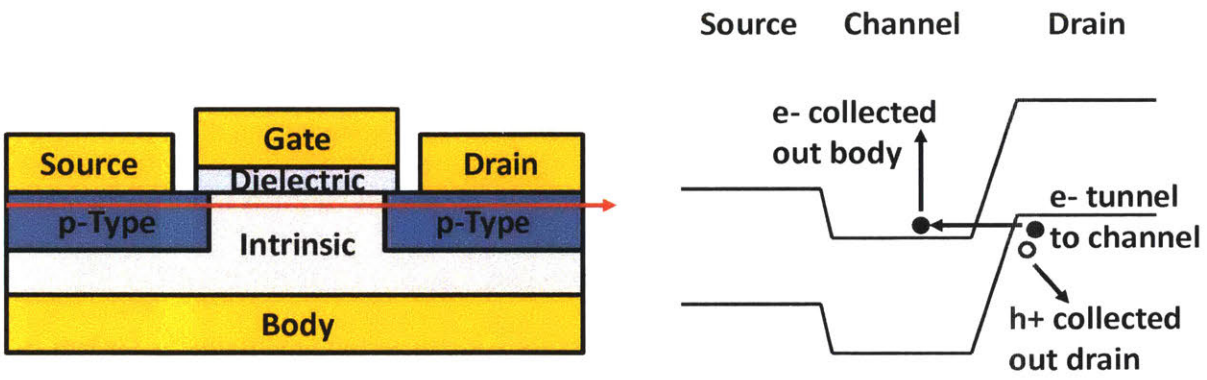


Figure 2.7. Schematic of a p-MOSFET (left) with the red arrow indicating the direction of the band diagram on the right which shows the device under bias when the device is off. With positive gate bias and negative drain bias, characteristic of a device that is off, the band bending can be large enough to cause band to band tunneling between the intrinsic body and the p-type drain. For a p-MOSFET, an electron from the valence band tunnels from the drain to the channel which is collected out of the body. During this process a hole is formed which is subsequently collected out of the drain.

The minimum attainable current of a material arises from the limitation imposed by the so-called gate induced drain leakage (GIDL) current [24-26]. The origin of the current comes from band-to-band tunneling (BTBT) between the drain and the channel when the device is off; the schematic in Fig. 2.7 illustrates GIDL current for a p-MOSFET. In the example shown in Fig. 2.7, electrons from the valence band of the p-type drain tunnel to the conduction band of the intrinsic channel. The tunneling generates an electron-hole pair where an electron is generated in the channel and a hole is generated in the drain. The Keldysh and Kane BTBT rate equation [27-30] is an empirical rate equation that is defined in Eq. 2.7 and can be used to show the trend for tunneling current based upon the bandgap and electric field.

$$I_{BTBT} = A\exp(-\frac{B\sqrt{E_g^3}}{|E|}) \quad (2.7)$$

where I_{BTBT} is the band-to-band tunneling current, A and B are two empirically derived parameters for a given material, E_g is the effective bandgap of the material and |E| is the magnitude of the electric field. When the applied gate bias for a p-MOSFET is more positive or the drain bias is more negative the GIDL current increases; Fig. 2.8 shows the impact of the GIDL current in the transfer characteristics of a p-MOSFET. The minimum attainable current is marked as I_{min} in the figure and is different from I_{off} which is normally considered the current at V_{GS} = 0 V and $V_{DS} = V_{DD}$. Based upon the Eq. 2.7, the GIDL current also greatly increases with decreasing bandgap and as a result obtaining the desired I_{off} for high mobility channel materials is a challenge which will be discussed in the subsequent chapter.

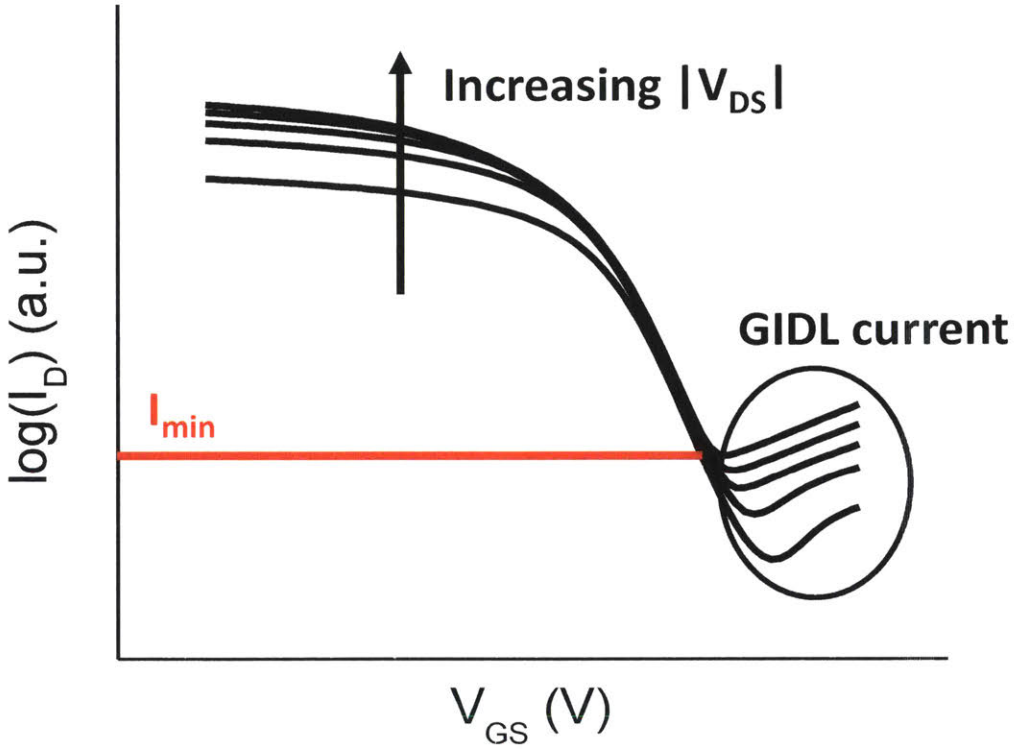


Figure 2.8. Transfer characteristics for a p-MOSFET with different V_{DS}. The GIDL current causes the drain current to increase with a more positive gate bias. When the magnitude of V_{DS} is increased, the GIDL current also increases resulting in an increase in the minimum attainable current for a given V_{DS} or I_{min}.

2.3 Steep subthreshold swing transistors

The third and final approach to reducing the V_{DD} is to use a new transistor design with a steeper subthreshold slope than a MOSFET. There are two types of transistors which qualify for this category of transistor: 1.) transistors that have internal gain or amplification of the gate voltage, and 2.) transistors which switch via a different mechanism than conventional MOSFETs. The first category of transistors still operate under the normal mechanisms of a

MOSFET, but the electric field at the dielectric-semiconductor interface is applied as in the case of the negative capacitance (ferroelectric/normal gate dielectric stack) field effect transistor [31]; this type of steep SS transistor is not covered in this work. The tunnel field effect transistor (TFET) falls in the second category which utilizes the interband tunneling mechanism for carrier injection into the channel, as opposed to thermionic injection in a MOSFET..

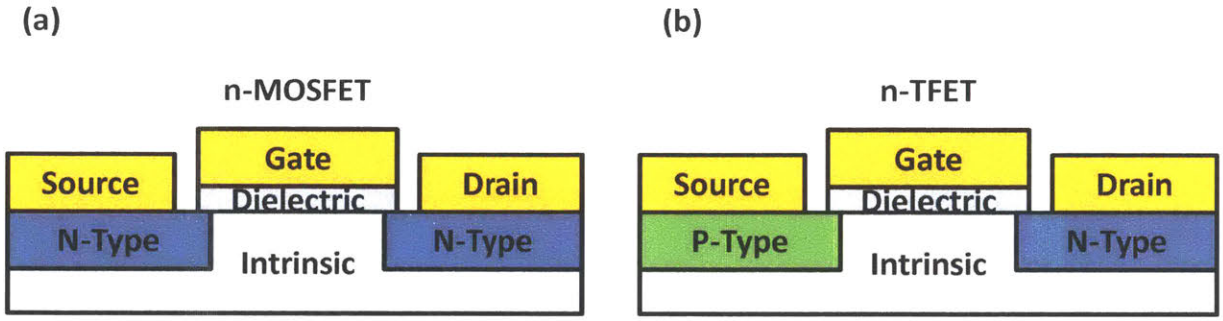


Figure 2.9. Schematic for an n- (a) MOSFET and (b) TFET. An n-MOSFET has an n-type source and drain while an n-TFET has a p-type source and an n-type drain making it a gated diode.

The tunnel field effect transistors (TFET) is a device that has been hypothesized in the 1980s [32] that has gained more attention recently because of its potential as a steep subthreshold swing device. In principle, the only physical difference between a TFET and a MOSFET is the doping profiles in the device; this is schematically shown in Fig. 2.9. The difference in the doping greatly changes the nature of the devices and two types of current injection are discussed briefly first: 1.) thermionic current and 2.) tunneling current. The thermionic current originates from the energy distribution of carriers given by Eq. 2.8.

$$N(E) = g(E)f(E) = g(E)\frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)} \tag{2.8}$$

Where N is the areal density of charge carriers at a given energy, g(E) is the density of states as a function of energy, E is energy, f is the Fermi function, E_F is the Fermi energy, k is Boltzmann's

constant, T is the temperature. The current from thermionic emission is current based upon the areal charge density larger than the potential barrier between the source and the channel multiplied by the velocity of the carriers, Eq. 2.9 [10, 17, 18].

$$\frac{I_D}{W} = qN(E > E_c^{chan})v \tag{2.9}$$

Where I_D is the drain current, W is the width, q is the elementary charge, $N(E > E_c^{chan})$ is the areal density of carriers in the source that have an energy larger than the minimum energy on the channel's conduction band and v is the carrier velocity.

The tunneling current has a few formalisms, but the requirements for tunneling are that the energy and momentum must be conserved and that there must be states to tunnel into. This is captured through a general transition rate given by Fermi's golden rule, Eq. 2.10.

$$I = q\Gamma = \frac{2\pi}{\hbar}|< f|H'|i >|^2\rho \tag{2.10}$$

Where I is the current, q is the elementary charge, Γ is the transition rate, $\hbar$ is Planck's constant divided by 2π, <f| is the final state, H' is the Hamiltonian, i|> is the initial state and ρ is the density of the final states. While Fermi's golden rule is not a commonly applied equation to calculate the tunneling current, it highlights the requirements for tunneling listed above which are useful for explaining why no current theoretically exists for an ideal TFET before band overlap; there are no final states, ρ.

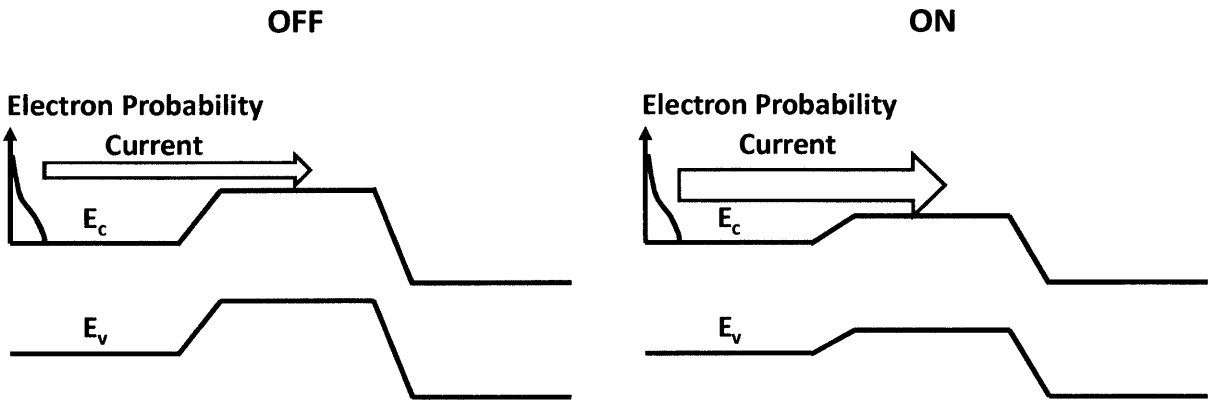


Figure 2.10. Band-diagram of an n-MOSFET in the "off" and "on" state with the majority carrier (electron) probability within the source plotted alongside it. The amount of current that flows is based upon the number of electrons that have enough energy to overcome the potential barrier. When the device is off, the potential barrier is high, and few carriers have enough energy to overcome the potential barrier. When the device is on, many more electrons have enough energy to overcome the barrier allowing for significantly more current to flow.

The band-diagram for the n-MOSFET is shown in Fig. 2.10 for the on- and off- state case with arrows qualitatively showing the magnitude of the thermionic current over the barrier. The current, based off of Eq. 2.9, is defined by the areal density of carriers in the source with energy larger than the E_c of the channel multiplied by the carrier velocity [10, 17, 18]. When a gate voltage is applied turning the device towards the on-state, the E_c of the channel is reduced and an exponentially larger areal density of carriers from the source has enough energy to overcome the barrier based upon the thermal distribution of carriers, Eq. 2.8. Based upon the thermal energy at room temperature, there will be an order of magnitude increase in the areal density of carriers for a 60 mV difference in the barrier height giving the 60 mV/dec. rule for MOSFETs. When the

MOSFET is off, there is no interband tunneling current in the device because there is no point where the valence band and the conduction bands overlap.

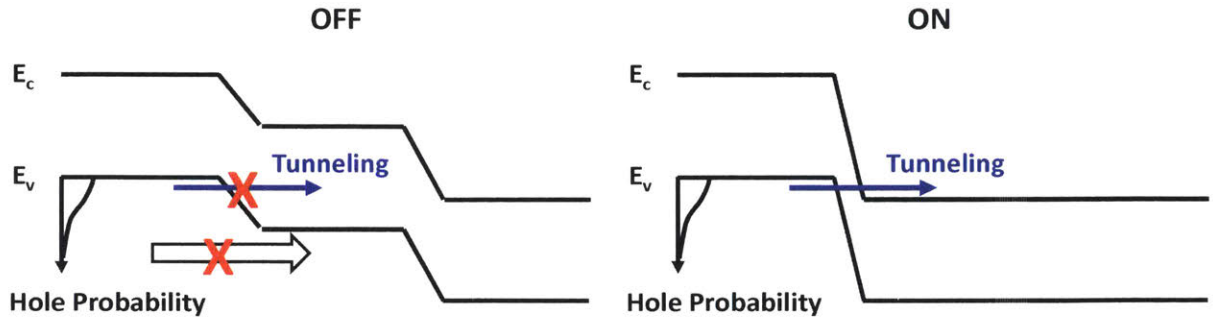


Figure 2.11. Band-diagram of an n-TFET in the "off" and "on" state with the majority carrier (hole) probability within the source plotted alongside it. When the device is off a very large potential barrier blocks injection of holes from the source to the channel, and channel states exist for electrons from the valence band to tunnel to, while the drain states are too far. When the device is turned on, the potential barrier is still large preventing thermionic current from flowing but the conduction band of the channel is overlapped with the valence band of the source resulting in a tunneling path for carriers. This allows current to flow, and in principle the switching can be abrupt because of the energy abruptness of the band edges.

The band-diagram for an n-TFET is quite different relative to an n-MOSFET, as seen in Fig. 2.11. The majority carrier in the source is now holes instead of electrons since the source is p-type. When the device is "off" there is a very large electrostatic barrier blocking the Fermi tail from conducting holes to the drain so thermionic current is not present. Furthermore, there are no states in the bandgap of the channel which means that there will be no conduction from tunneling. The result in an ideal TFET is that no current flows then the device is "off". When the device is turned "on", a positive applied gate voltage pushes the band of the channel down. Still no holes from the Fermi tail can be conducted because of the electrostatic barrier, but electrons

from the valence band of the source can tunnel into the conduction of the channel because now there is a finite density of states to tunnel into. The tunneling of an electron results in a hole being generated in the source and an electron being generated in the channel. The hole and electron are collected out of the source and drain respectively resulting in the measured current of the device. The fact that both a hole and electron is collected is the key difference between a MOSFET and a TFET. Because there is neither thermionic nor tunneling current when the device is off, the TFET can theoretically switch at a rate steeper than 60 mV/decade when the bands align. In fact, the switching should be very steep (from no current to some current) assuming the density of states cut-off for the valence and conduction bands are infinitely sharp.

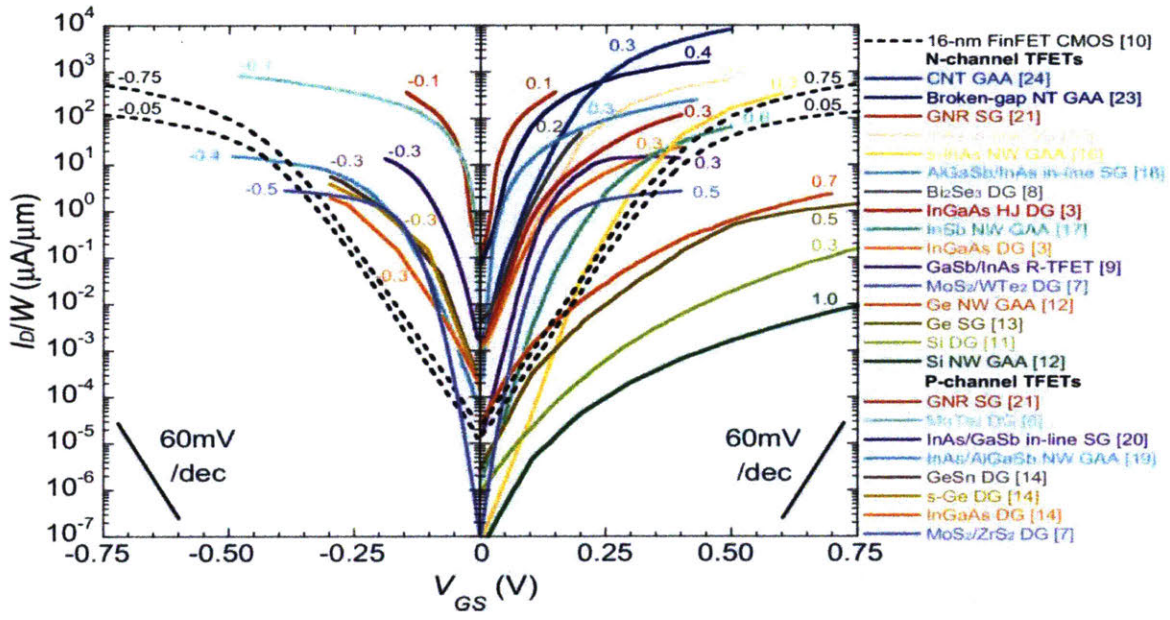


Figure 2.12. Simulated transfer characteristics from TCAD simulations for both p- and n-TFETs are plotted alongside those of the 16-nm FinFET technology from [33]. The V_{DS} of the simulations are marked next to their respective curves. The majority of the simulated curves have steeper SS and reasonable drive currents resulting in the curves falling to the right and left of the FinFETs for p- and n- TFETs respectively. This figure is reproduced directly from [34] and the references refer to those in [34].

When researchers identified TFETs as a potential candidate for low-power digital devices, they used Technology Computer-Aided Design or TCAD to simulate I-V curves in order to evaluate the performance of TFETs. TCAD simulators can include complex quantum effects, OMEN™, but majority of the simulated curves have been done with classic drift-diffusion simulations with minor quantum corrections such as Sentaurus Device™, Silvaco Atlas™ and Medici™; the majority of simulations have been done with drift-diffusion simulators and the references to TCAD simulations in this chapter will refer to simulations done

by them. The simulated curves which are shown in Fig. 2.12 have been summarized in [34], and cover both n- and p- TFETs. The figure includes 16-nm MOSFET characteristics from [33] to illustrate the performance of the TFETs relative to that of a state-of-the-art MOSFET. If one looks at the simulations, the majority of the graphs have similar or higher on-state currents relative to the MOSFET and significantly steeper SS suggesting that TFETs could be better logic switches than MOSFETs for both p- and n- TFETs.

Following the TCAD simulations experimental results began to get published. The first demonstrations of TFETs were on Si [35], but other TFETs fabricated with other materials followed the Si work. Early devices showed steep SS at very low currents near the minimum current values for TFETs giving promise to the field although at unusable current levels. These devices tended to have good SS, and low on-state currents, single digit μA/μm range, due to the fact that they were based upon Si. The later work that was done utilized smaller bandgap materials and heterojunctions [36-39] in order to reduce the effective mass and bandgap so as to increase the on-state current. The work from [34] benchmarked experimental devices relative to the same 16-nm MOSFETs, as seen in Fig. 2.13. The experimental curves tell a drastically different story relative to the simulation work: TFETs in general are not better than MOSFETs in either on-state current or SS. In fact, at no point did any experimental TFET benchmarked in these curves show improved performance: higher on-state current for a given off-state current. While experimental TFETs have not shown SS < 60 mV/dec. at 300K at practical currents, there have been a few demonstrations of TFETs of lower SS at very low current levels, I_D < 1 nA/μm [34, 35, 39-42]. The reasons why the SS may be steep at very low currents for these devices is not clear, and experimental errors cannot be excluded unequivocally, but for devices to be practical, the steep SS needs to be achieved at higher current levels, 1 nA/μm and above [13].

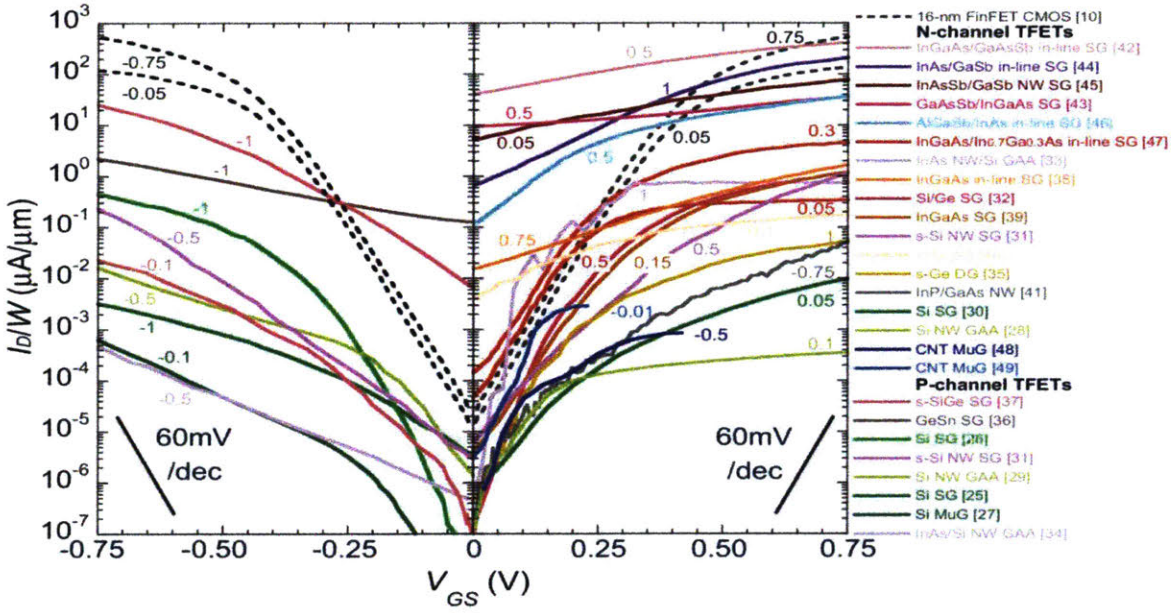


Figure 2.13. Experimental transfer characteristics of various p- and n- TFETs are plotted alongside those of the 16-nm FinFET technology from [33]. The V_{DS} values for the transfer characteristics are marked next to their respective curves, and the material of the TFET is marked in the legend. The majority of the experimental transfer curves have high SS and low on-currents resulting in the curves falling to the left and right of the FinFETs for p- and n- TFETs respectively. This figure is reproduced directly from [34] and the references refer to those in [34].

There are many reasons why experiment and the simulation for TFETs can differ greatly. Some of these problems are technological and might be solved by improvements in technology, while others are fundamental or caused by incorrect capture of the physics between experiment and simulation. The technological issues are related to the inherent assumptions made in the simulations of the TFET. Some technological assumptions for TFETs are 1.) the semiconductor has no states in the bandgap, 2.) the materials are spatially homogenous, 3.) the source/channel

junction is too abrupt, and 4.) the realized electrostatics and the simulation electrostatics are the same.

The assumption that the semiconductor has no states in the bandgap is inherently poor due to the fact that defect states have always been observed experimentally in semiconductors. There are both intentional and unintentional defects present. Interface and bulk defects are unintentional dopants and dopants are intentional dopants. The unintentional defects are physically located everywhere in the device and energetically located throughout the bandgap. The interface states are located at the interfaces between different materials, and the highest density of interface states tends to occur between the semiconductor and oxide [43]. The density of the interface states (D_{it}) between the oxide and semiconductor has been previously characterized to be large [37] and can cause problems in the TFETs because they are available at all energies. The bulk defects are located within the bulk of the semiconductor and tend to occur at specific energies depending upon the type of the defect [43]. Finally, the dopant atoms have states near the band edges and also are known to modify the intrinsic band-edge state spectrum. The standard simulation approaches are based upon the empty bandgap, but this is clearly not the case so inconsistencies can be expected.

Another assumption is that the materials are spatially homogenous over the entire area. It is very likely that the material or certain properties of the material like strain is not exactly the same as a function of position in the channel. Some examples of variations that become particularly important in miniaturized MOSFETs are random dopant density fluctuations and grain boundaries in the gate metal [44]. It would also be sensible that material inhomogeneity will also hurt TFETs, but it has been proposed that it would harm it in a different way [15, 45]. The tunneling interface is sensitive to local changes in material thicknesses, strain, doping, etc.

which could cause local electric fields resulting in turn-on of tunneling at different gate voltages [15, 45]. It is relatively uncertain how one should quantify this problem, but researchers have proposed making the devices small in order to increase to reduce the effects of local material differences [15, 45]. The problem with making the device smaller is that the surface area of the device begins to be more significant thus complicating the problem of surface related defects and the variation has been shown to increase [46, 47].

The doping profile is also important for achieving good TFET characteristics according to previous TCAD studies [48]. Realistic doping profiles have finite rate of change in the doping concentration. The rate of change depends on process conditions such as the ion implant, diffusion during high temperature steps and the silicidation processes [35, 41, 49]. It has been hypothesized and shown using TCAD simulations that the doping profile should be steep and near the gate edge in order to get the proper band-bending characteristics for steep SS [35, 41, 49]. Obtaining a steep enough profile is a technological issue that might be solved by good control of the process conditions and simulations can be used to design devices more immune to doping profile.

The final problem listed as a technological issue is that the TFET electrostatic design may reflect the realities of experiments. The TCAD simulations take into account the ideal characteristics of a TFET. They do not take into consideration some technological factors such as defects states which may contribute to differences in the electrostatics between experiment and simulations.

The reason why TCAD software is unable to capture the fundamental physics is that it is based upon the lumping of many parameters. Typically, the tunneling current is calculated from the Keldysh and Kane rate equation, Eq. 2.8, which significantly simplifies the tunneling rates

that should be derived from Fermi's golden rule, Eq. 2.9, into two parameters: bandgap and electric field. The tunneling rate in Fermi's golden rule considers many things such as momentum matching from one state to another, the energy states of the initial and end states and the density of carriers present at both the initial and final states. The oversimplification of the physics can explain why the TCAD simulations are not predictive of TFET device characteristics.

One of the effects that would be observed in experimental device or in calculations utilizing Fermi's golden rule but not TCAD is the effect of phonons. Phonons are required for the indirect bandgap transition between the valence band and conduction bands of silicon, but also could provide the energy necessary for BTBT before the bands overlap. This would result in a less abrupt turn-on of the BTBT current. Similarly, the intrinsic property of semiconductors whereby the band edges are not infinitely steep but they taper off at a finite rate ~20 mV/dec. the so- called Urbach tails [50], is often not captured. These are two examples of more fundamental physics that could change the results of the simulations if they were considered, and more reasons why experimentally TFETs do not match simulations.

In summary, while TFETs are a promising solution to making steep SS transistors, previous experiments have corroborated this claim. There are a lot of possibilities why the experimental TFETs do not show steep SS characteristics, and this work will present experimental results of Si/Ge TFETs and will discuss which of these problems are potentially limiting.

Chapter 3: Strained Germanium as a p-MOSFET Channel Material

The previous chapter outlined strategies that are being investigated in order to reduce the power consumption per transistor of CMOS circuits by reducing the V_{DD}. This chapter looks at the approach of reducing the effective mass in order to boost the drive current of the transistor. This approach can be done for p-MOSFETs by switching channel materials and using strain; this chapter presents work and analysis on germanium and strained germanium. The chapter first details the requirements that a MOSFET must fulfill and it analyzes, based upon experiments from this work and literature, whether or not the performance metrics for a future MOSFET can be met using germanium as a channel material.

3.1 Technological requirements for future MOSFETs

There are many technological requirements that a MOSFET must meet in order to be useful for a future technology node. Although optimistic, the ITRS roadmap is a good indicator of those requirements; the key ones are shown in table 3.1 for the so-called "high performance (HP) and low power (LP) MOSFETs, [13] and include the gate length and on-current. The first of the two requirements is that the MOSFET needs to have a certain physical gate-length meaning the chosen materials need to be able to be integrated at a tight pitch

The second criterion, the MOSFET must have a certain on-state current ($V_{DS} = V_{GS} = V_{DD}$) for a given off-state current ($V_{DS} = V_{DD}$ and $V_{GS} = 0$ V) at a given V_{DD}, can be split into several smaller requirements: 1.) the channel material should have a high enough carrier velocity or mobility, 2.) the gate oxide is scalable to achieve good electrostatic integrity and have a low interface trap density, 3.) the desired threshold voltage can be obtained, and 4.) the MOSFET can meet the off-state current level (100 nA/μm for high performance and 100 pA/μm for low power).

Germanium (Ge) has been identified as one of the leading candidates behind Si and SiGe as a channel material for p-MOSFETs in future nodes because of its ease of integration with Si and the fact it has one of the highest hole mobilities of all semiconductors; a comparison of different diffusive hole mobilities is shown in Fig. 3.1. Other high hole mobility candidates are antimonide based materials which are challenging to integrate or grow on silicon due to the binary or ternary nature of the materials [51, 52]. As a testament to its ease of integration, Ge is the only high hole mobility material to be integrated on Si thus far [53-57]. Ge FinFETs on Si with scaled gate length have been demonstrated with high currents and good electrostatics, and important characteristics can be seen in Fig. 3.2 [53]. The hole mobility in the published Ge FinFETs is significantly higher than in Si and therefore higher on-currents were observed in the devices for a given off-current (100 nA/μm) [53, 57].

Table I: Targeted MOSFET Device Characteristics Based Upon the ITRS 2015 Roadmap [13]

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Physical Gate Length for HP Logic (nm)	24	18	14	10	10	10	10
Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12
$V_{t,sat}$ (mV) at I_{off} = 100 nA/μm - HP Logic	129	129	133	136	84	52	52
$V_{t,sat}$ (mV) at I_{off} = 100 pA/μm - LP Logic [5][6]	351	336	333	326	201	125	125
I_{on} (uA/μm) at I_{off} = 100 nA/μm - HP logic	1177	1287	1397	1476	1546	1456	1391
I_{on} (uA/μm) at I_{off} =100 pA/um - LP logic	596	637	637	629	890	956	821

White = Manufacturable solutions exist, Yellow =Manufacturable solutions are known, Red =Manufacturable solutions are not known

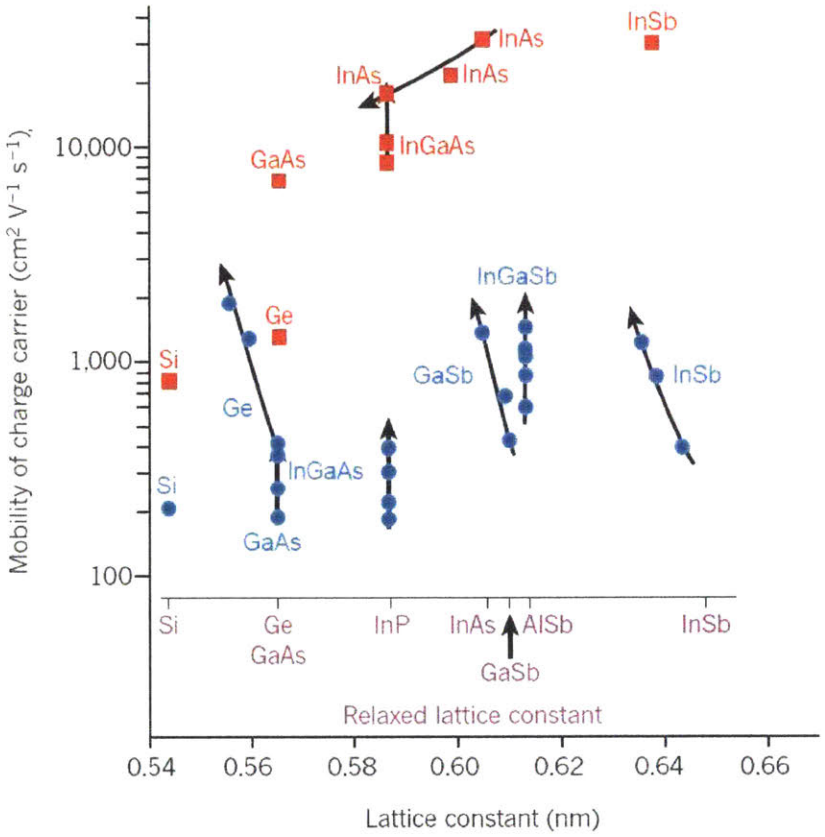


Figure 3.1. Diffusive electron (red) and hole (blue) bulk mobility for different materials and lattice constants. Arrows denote changes in mobility due to increasing compressive strain. For high levels of biaxial, compressive strain, Ge shows the highest hole mobility out of all materials that have been benchmarked. The figure comes directly from [52].

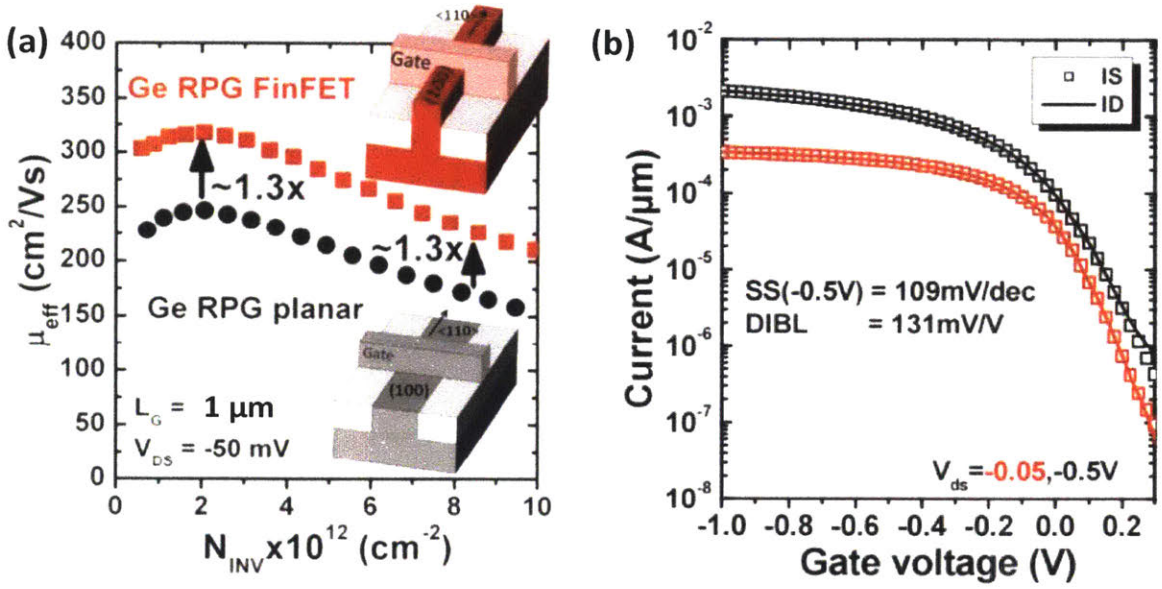


Figure 3.2. (a) Effective mobility of a Ge FinFET and relaxed planar Ge p-MOSFET on Si for CET = 15 Å and L_G = 1 μm. The schematic for the respective structures is in the inset where the channel is in the <110> direction. The enhancement in the hole mobility is due to improvement in transport in the [110] sidewalls. The transfer characteristics (b) for a L_G = 20 nm Ge FinFET show reasonable electrostatics despite the scaled gate length, and good drive currents ~500 μA/μm for an off current of 100 nA/μm and a V_{DS} = -0.5 V. These figures were taken directly from [53] to illustrate that the Ge FinFET can be integrated with good results on Si.

3.2 Germanium and strained germanium for high drive current MOSFETs

The main argument behind using Ge is its high channel mobility. This section examines mobility enhancement through strain. Applying compressive strain to germanium can improve the hole mobility hence the hole velocity. Biaxial compressive strain, i.e. equal magnitude of strain for both in-plane directions, can be used to greatly improve the hole mobility for s-Ge; the improvement of the mobility with strain is well documented in literature, and a good example is

shown in Fig. 3.3 from Intel [25]. The work showed that relaxed Ge has higher hole mobility than strained Si and that compressive strain increased the mobility in Ge even further. While biaxial strain can improve the mobility, it has been shown in both Si and Ge that uniaxial compressive strain is more ideal for hole mobility for p-MOSFETs with a [110] channel orientation [12, 21, 58, 59]. The effect of various degrees of strain is well known, but it had not been well quantified for s-Ge.

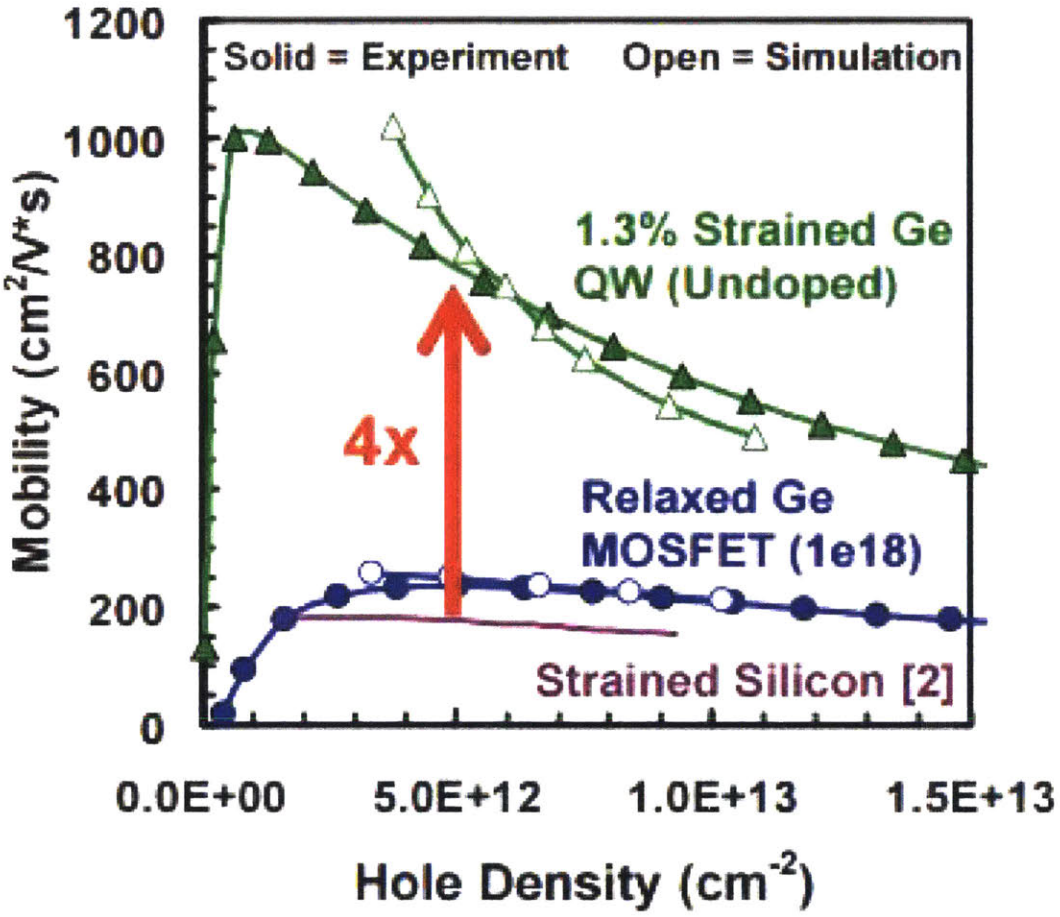


Figure 3.3. Hole mobility for strained silicon (purple), relaxed (blue), and biaxially compressively strained Ge quantum well with a Si cap (green) versus hole density. The relaxed Ge has higher mobility than strained Si to begin with and the compressive biaxial strain of the Ge quantum well greatly improves the mobility on top of that. The figure comes directly from [60].

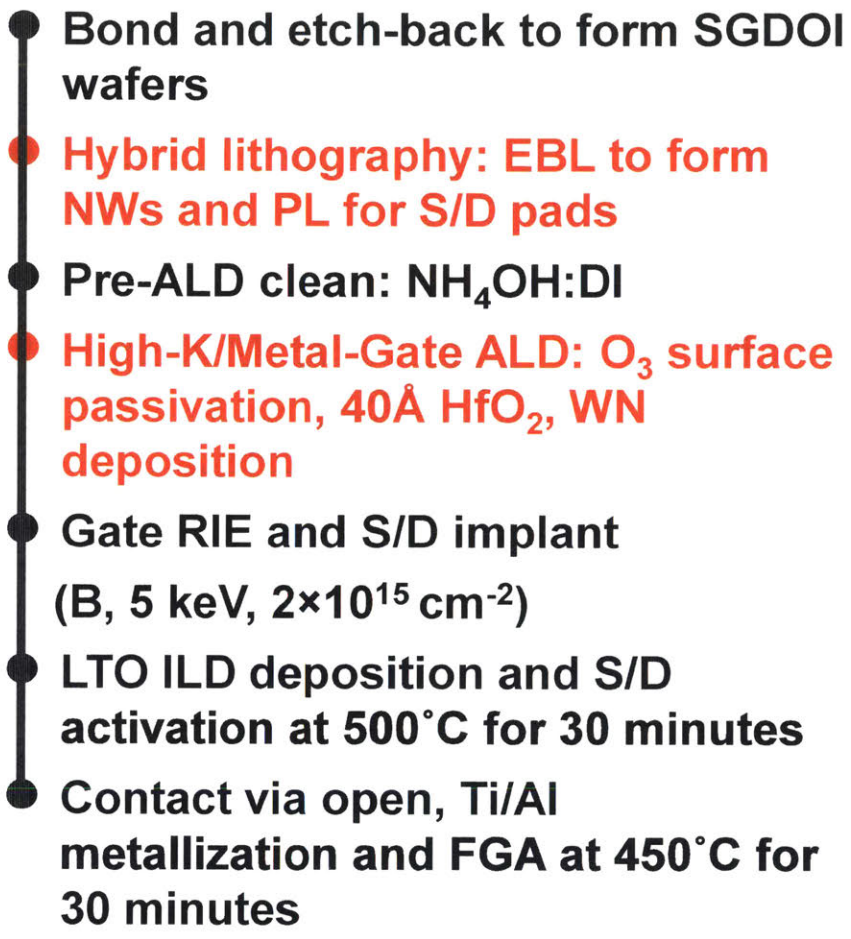


Figure 3.4. Abbreviated process flow for both narrow width and s-Ge trigate nanowire p-MOSFETs [61, 62].

An experiment to investigate the impact of differing degrees of strain, specifically biaxial, asymmetric – differing magnitudes of strain in the two in-plane axes – and nearly uniaxial strain was performed and was partially published in [62] and [61]. Previous work examined nanowires ranging in width from 18 to 49 nm and biaxially strained Ge. The work in this thesis expands on the previously published work by investigating the impact of different strain configurations and channel directions, <110> and <100>, in narrow width devices ranging from 425 nm to 2 μm with different channel orientations. These devices were processed on the

same wafer as the previously published nanowire and biaxially strained s-Ge devices in [61, 62]; the abbreviated process flow and schematic of the device can be found in Fig. 3.4 and 3.5 respectively and the full process flow can be found in Appendix A. The top-down schematic of the fabricated device is in Fig. 3.5a, and the cross-section TEM (XTEM) in Fig. 3.5c shows the channel configuration with the 3.5 nm s-Si cap on top of the s-Ge. The XTEM was used to calibrate the exact mesa widths of the devices so that current could be normalized.

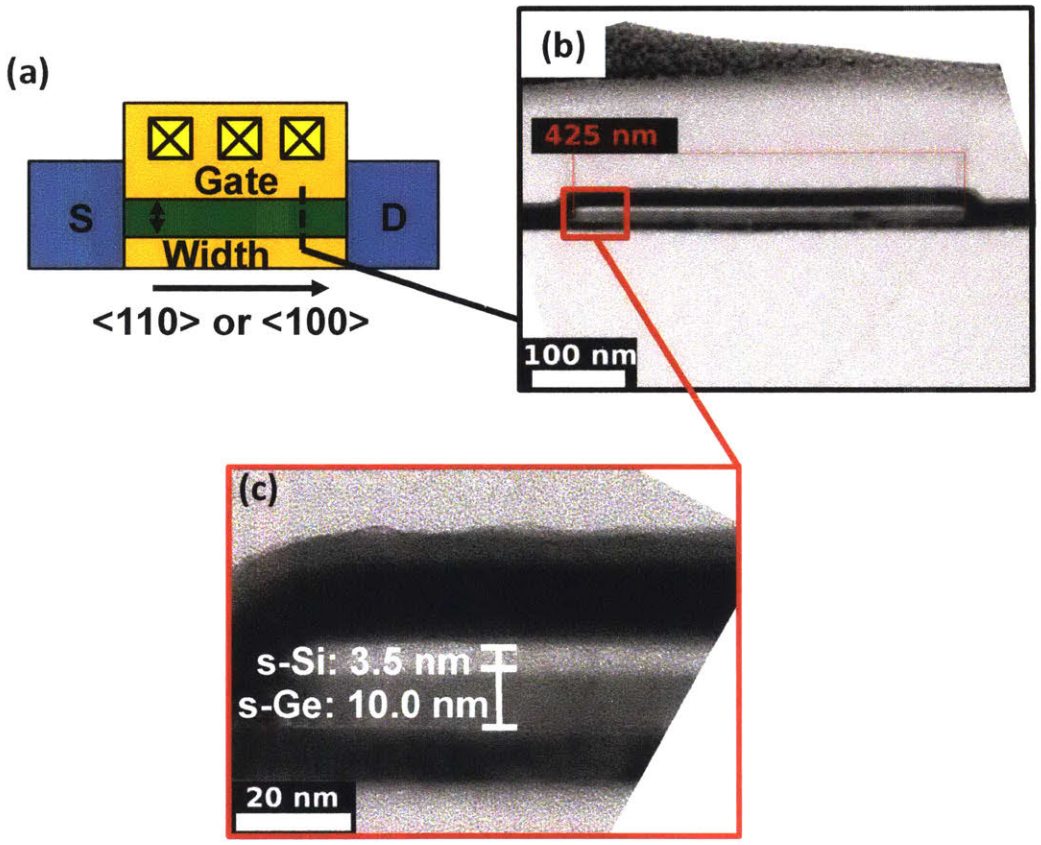


Figure 3.5. (a) Top-down schematic of s-Ge narrow width p-MOSFETs. (b) XTEM of the channel of a 425 nm wide mesa. (c) High resolution XTEM shows the channel heterostructure consists of 3.5 nm s-Si/10 nm s-Ge.

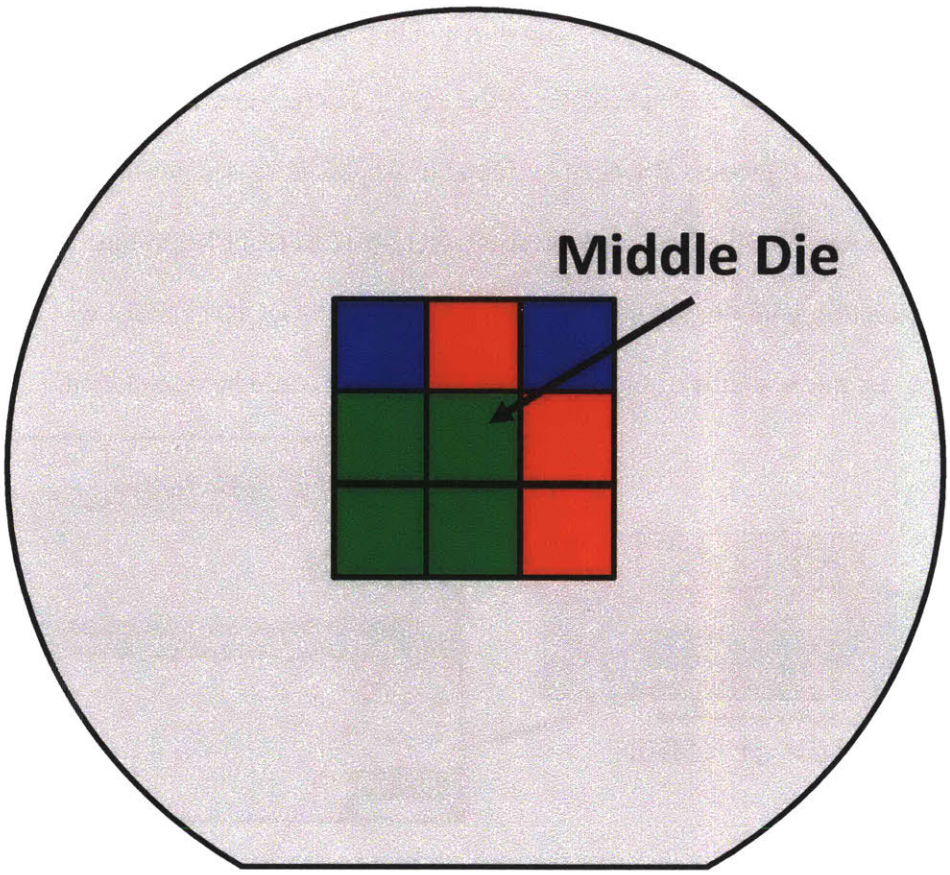


Figure 3.6. Die map of measured devices where: red indicates dies with a bonding defect, blue designates dies used to show the mobility trend, and green are other measured dies.

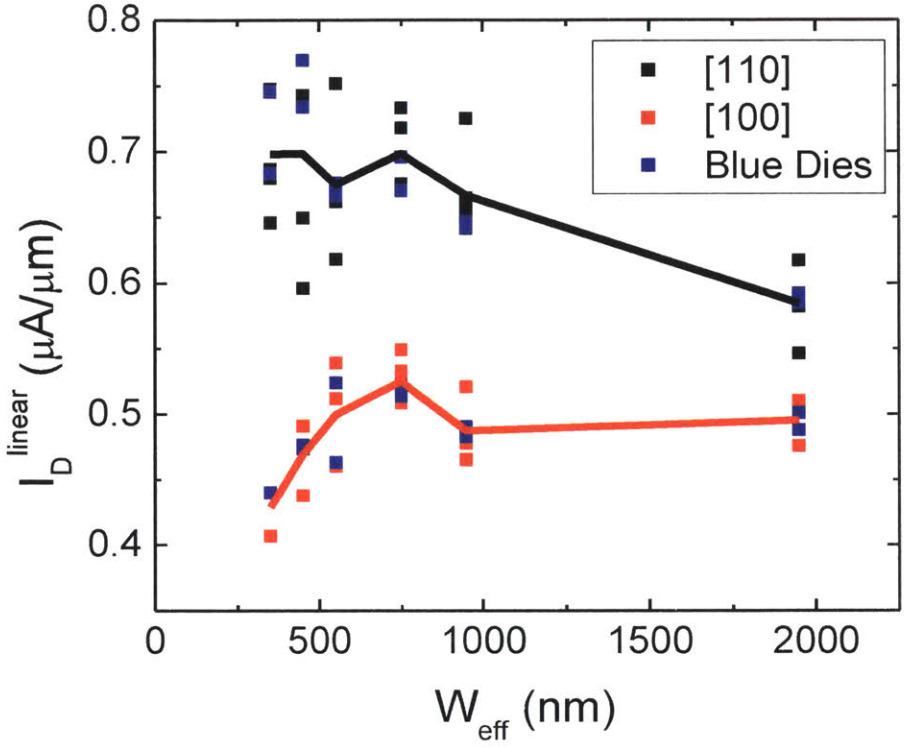


Figure 3.7. I_D^{linear} (I_D @ V_{DS} = -50 mV, V_G = -0.5 V) versus the effective width (W_{eff}) for different crystal orientations. The line is average for all of the data points as a function of the width. The widths are calibrated based on the cross-section TEM in Fig. 3.5b; the widths were adjusted by the difference in physical and nominal mesa widths for all mesa widths. The data points in blue correspond to the blue dies in Fig. 3.6.

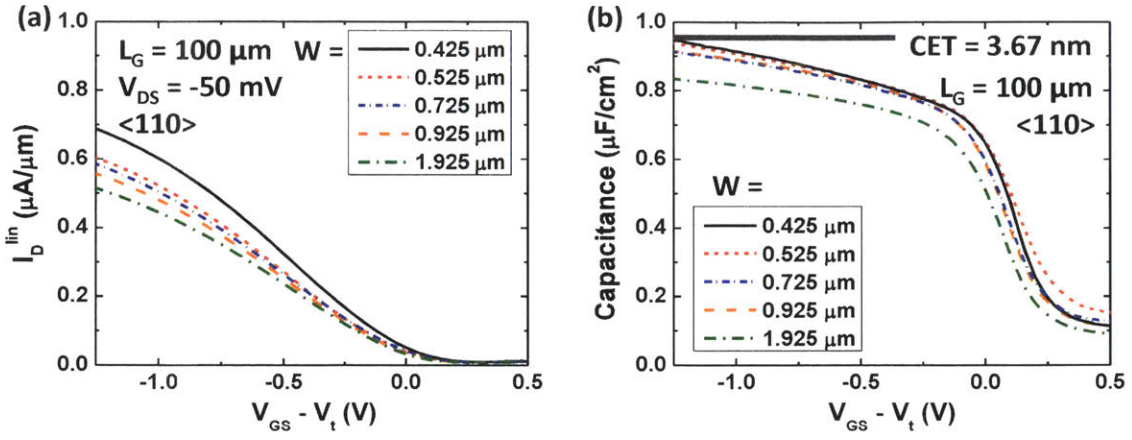


Figure 3.8. Normalized (a) V_{DS}=-50 mV transfer and (b) C-V characteristics for <110> oriented narrow width devices. The normalization was done using $W_{eff} = W + 2H_{mesa}$ where W is the adjusted width based on the XTEM and H_{mesa} is the height of the mesa.

Only certain dies were measured in this experiment, and the die map of the middle 9 dies is shown in Figure 3.6. Because the process uniformity near the center wafer is better, devices from the 6 dies without bonding defects were measured. The scatter plot, Fig. 3.7, of the measured I_D^{linear}, i.e. the I_D at V_{DS} = -50 mV, shows large variation in the current across the measured dies. Despite this, the average of data from the points still showed a trend of increasing and decreasing current with decreasing mesa width for the <110> and <100> channel directions respectively. This effect of strain on the current can be more cleanly evaluated if the data is converted into hole mobility using I_D-V_G and split C-V. These characteristics are shown for several <110> devices on one of the blue dies from Fig. 3.8. The I-V characteristics for these devices show a clear increase in the I_D/W with decreasing mesa width. The C-V characteristics show that the capacitance increases with decreasing mesa width which is indicative of the additional contribution of charge from the sidewalls. Nevertheless, because of the large increase in the current, the calculated mobility for the <110> direction increases with decreasing mesa

width as shown in figure 3.9 and 3.10. The trend is opposite for the <100> direction with the mobility decreasing with decreasing mesa width. The explanation for this is that the effective mass decreases for increasingly asymmetric strain, caused by strain relaxation from the sidewalls, in the <110> direction but increases in the <100> direction; simulations done in nextnano^{TM} [63] showing this are documented in [58, 59]. The improvement in mobility by ~4-16x translates to between a 2-4x enhancement in the ballistic velocity relative to Si [59]; this is because mobility is inversely proportional to the effective mass while velocity is inversely proportional to the square root of the effective mass as described in Eqs. 2.5 and 2.6. The significance of these results is that even a small amount of strain asymmetry can be used to achieve a significant reduction in the effective mass, and that strain and Ge can be used to boost the p-MOSFET drive current allowing for V_{DD} reduction [58, 59].

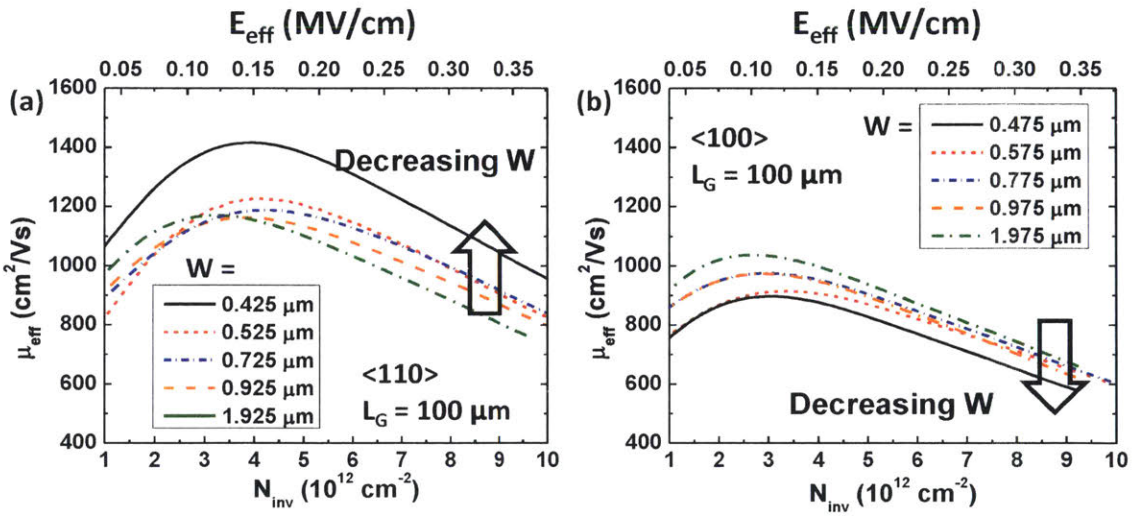


Figure 3.9. Extracted μ_{eff} vs. N_{inv} for (a) <110> and (b) <100> oriented devices for nominally W = 425 nm to ~2 µm; N_{inv} was derived using W_{eff}. The general trend is that mobility increases for <110> and decreases for <100> for decreasing mesa width.

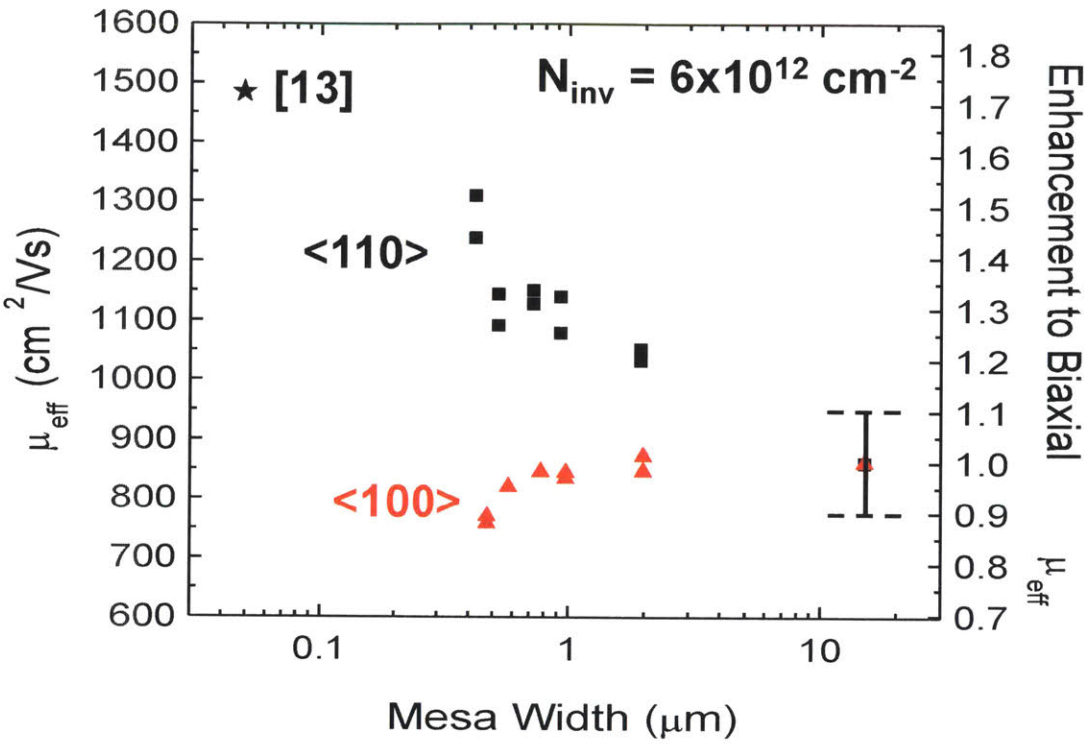


Figure. 3.10. μ_{eff} vs. mesa width by split-CV method for <110> and <100> channel orientations for $N_{inv} = 6x10^{12}$ cm^{-2}. The μ_{eff} for biaxially strained s-Ge is estimated for W = 15 μm using $Q_{inv} = qC_{ox}(V_{GS}-V_T)$. The error bar represents a +/-10% μ_{eff} error due to that estimate. Also shown is the W_{NW} = 49 nm trigate p-MOSFET in [13] to show the effect of further lateral strain relaxation.

3.3 Gate Oxide development for s-Ge electrostatics

Developing a high quality and thin gate oxide stack is important for maintaining good electrostatics at the short channel lengths required of future CMOS nodes. High channel mobility materials tend to have worse semiconductor-oxide interfaces than Si which poses a challenge to maintaining good electrostatics in short channel MOSFETs for high channel mobility materials [25, 52, 64]. Not only are the electrostatics a challenge, the main benefit of the high mobility is

degraded due to higher densities of interface states and the remote dipole and phonon scattering for thin high-κ dielectrics [9]; the degradation with decreasing CET is shown in Fig. 3.11. In order to reduce the impact of interface states, it is important to develop a process with low interface state densities for the channel material, in this case biaxially strained Ge.

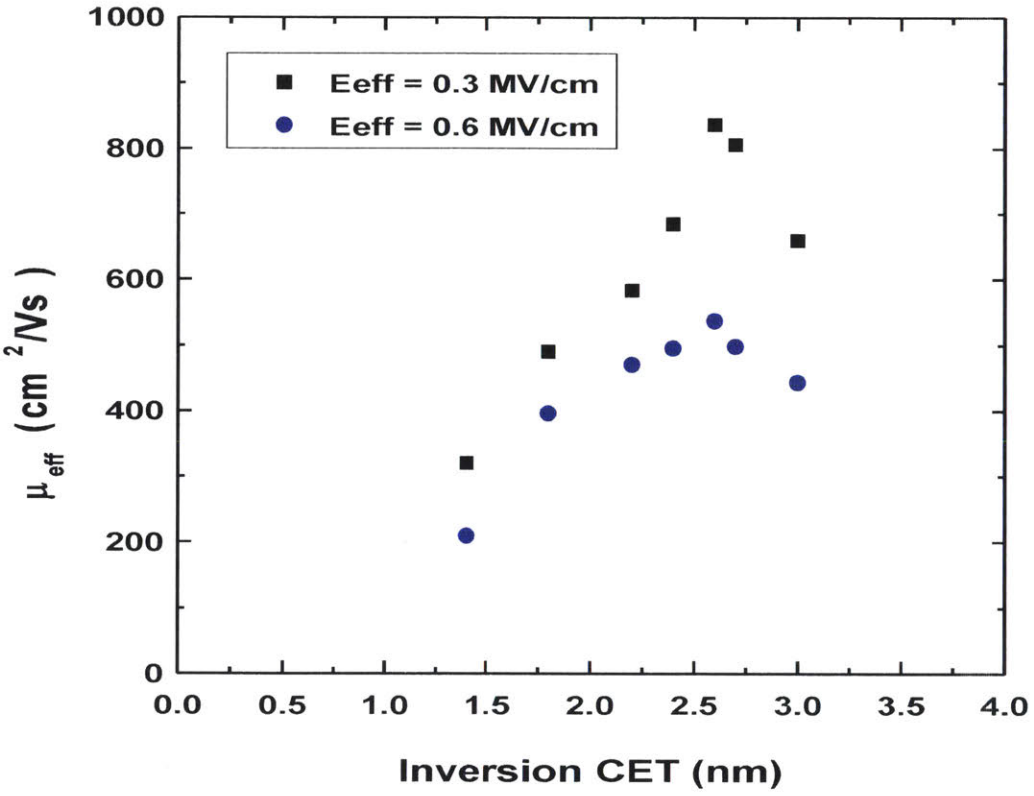


Figure 3.11. Effective hole mobility versus inversion CET for different biaxially strained-Ge devices at different inversion CETs for different effective vertical fields (Eeff) [65, 66]. When the inversion CET decreases below 2.5 nm there is degradation in mobility due to the increase in hole scattering rate caused by the increased remote dipole scattering [65]. When the CET is larger than 2.5 nm there is degradation in the mobility due to defects from relaxation of the s-Si cap [60, 67].

The state-of-art results of subthreshold swing (SS) versus capacitance effective thickness (CET) for high-κ on strained-Ge channels are benchmarked in Fig. 3.12; CET is the equivalent to the following abbreviations used in the literature, TOXE (Intel) and T_{inv} (IBM) [40, 65, 67-70]. The figure shows that researchers have tried several different methods of forming an interfacial oxide: 1.) Si cap, 2.) ozone, 3.) surface nitridation and 4.) plasma post-oxidation. The first mentioned approach is to use a strained Si cap on top of a strained Ge channel in order to improve the interfacial oxide (SiO_2 instead of GeO_x). This approach limits the minimum CET that can be achieved; CET = 1.4 nm is the minimum thickness reported for a gate stack with a Si-cap [60, 67-69]. This means that other approaches should be taken if one wishes to scale the CET beyond this value for short-channel devices. Other approaches such as ozone, and plasma post-oxidation are different methods of forming the interfacial GeO_x [40, 71, 72]. In an ozone process the bare s-Ge is exposed to ozone before high-k deposition to form GeO_x. For a plasma post-oxidation process, oxygen plasma is diffused through the already deposited high-k dielectric resulting in a GeO_x interface. A schematic showing the two techniques can be found in Fig. 3.13. Nitridation instead forms $GeON_x$ as the interfacial oxide [70]. Despite all of the different methods in forming the gate stack, there are no reports of ideal SS = 60 mV/dec. at room temperature due to the high interface trap density (D_{it}) of any dielectric on s-Ge relative to that of Si.

In order to address the issue of high-k gate dielectric scaling on strained Ge channel hole mobility, the previous work was followed-up by developing a gate stack on biaxially strained-Ge using plasma post-oxidation technology first introduced in [72]. Annular FETs were fabricated using both facilities at MIT and IBM T.J. Watson.

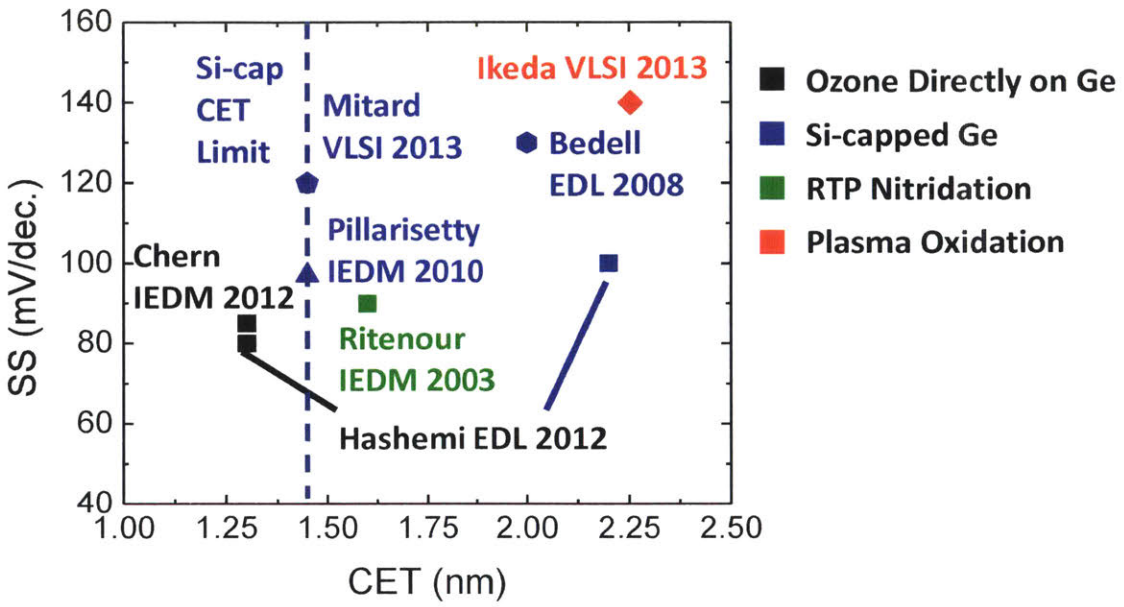


Figure 3.12. SS vs. CET for different technologies on s-Ge [61, 65, 67-70]. The CET is compared at $V_{GS} - V_T = -0.7$ V when possible. The color denotes the type of technology of the gate dielectric and the symbol denotes different institutions. Square, pentagonal, hexagonal and diamond symbols represent work from MIT, IMEC, IBM T.J. Watson and the National Institute of Advanced Industrial Science and Technology (AIST).

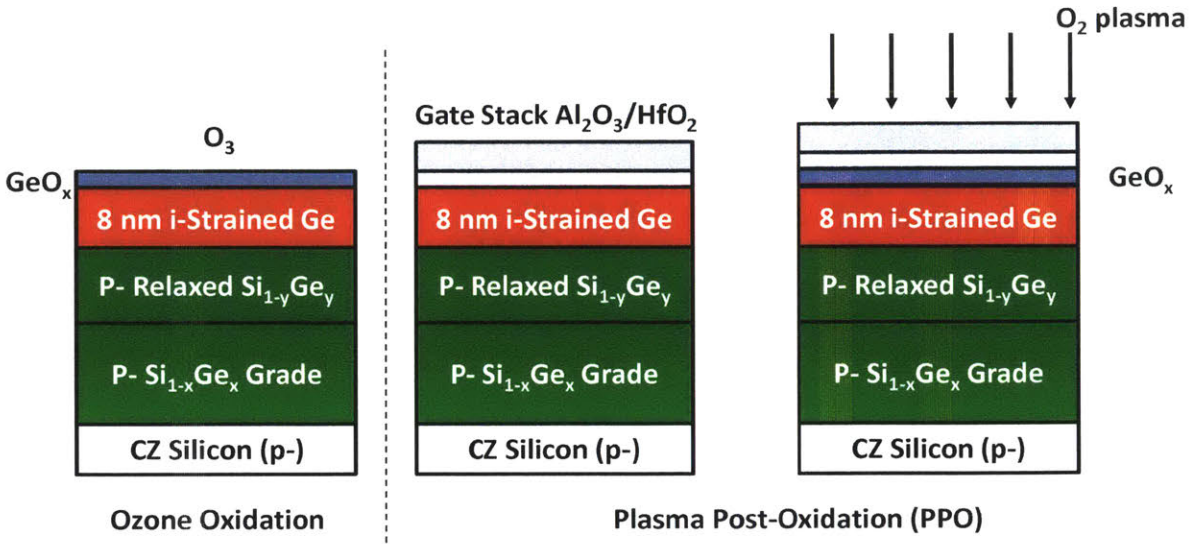


Figure 3.13. Schematic showing formation of the native GeO_x for ozone and plasma post-oxidation (PPO). In ozone oxidation, the strained germanium is directly exposed to the ozone in order to form GeO_x. In plasma post-oxidation or PPO, the gate stack of Al_2O_3 and HfO_2 is deposited first and then O_2 plasma is diffused through the gate stack to form GeO_x.

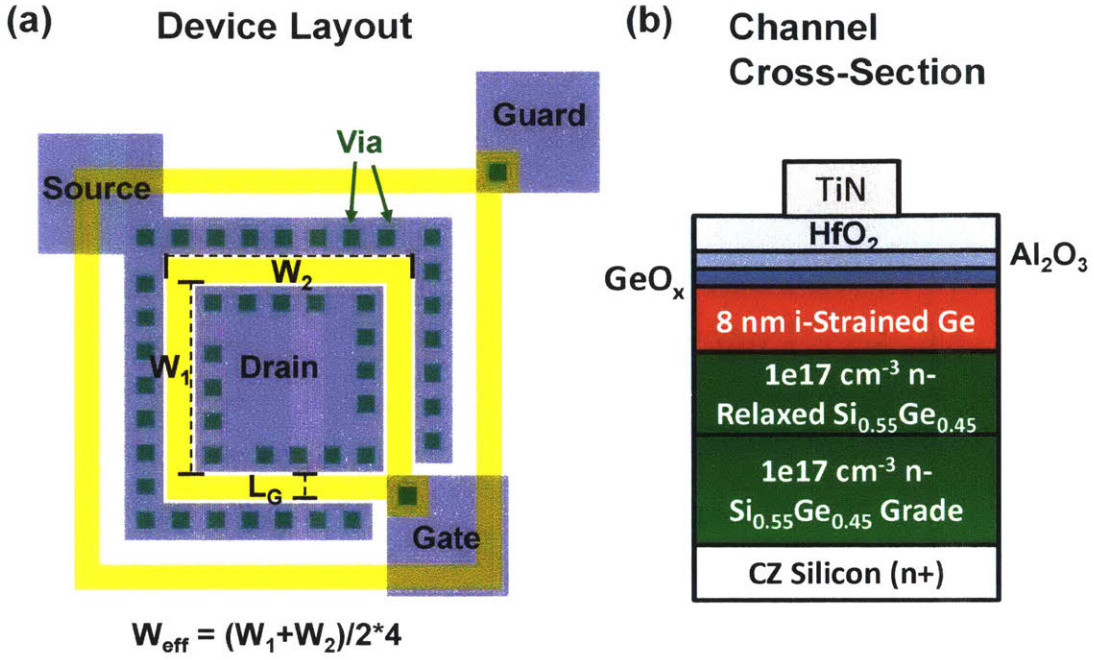


Figure 3.14. (a) The top-down schematic for the fabricated s-Ge p-MOSFETs. W_{eff} is approximated as the average of outer and inner width of the gates. (b) The gate dielectric and epitaxy structure of the device. The gate dielectric consists of $GeO_x/Al_2O_3/HfO_2$ and has a TiN electrode.

Annular strained-Ge p-MOSFETs with the schematic shown in figure 3.13a were fabricated on the epitaxial structure shown in Fig. 3.13b. The epitaxial structure was grown in an Applied Materials Epi-Centura LPCVD reactor. After epitaxial growth, a protective SiO_2 layer was deposited via PECVD on top of the s-Ge and removed using buffered HF. After BHF, 10:1 HCl was used to pre-treat the s-Ge surface before ALD. The gate stack consisted of 5 Å Al_2O_3/25 Å HfO_2. Plasma post-oxidation was performed after high-κ deposition using an O_2/Ar plasma. The gate, 30 nm TiN, was deposited via sputtering and patterned by wet etching. The photoresist that was used to mask the gate wet etch was used for the source/drain ion

implantation of boron with an energy of 15 keV and a dose of $4x10^{15}$ cm^{-2}. After ion implantation, the interlayer dielectric of SiO_2 was deposited and the samples were annealed at 625°C for 10s in N_2 to activate the ion implant. The fabrication was completed using a standard via and metallization process with Ti/Al contacts.

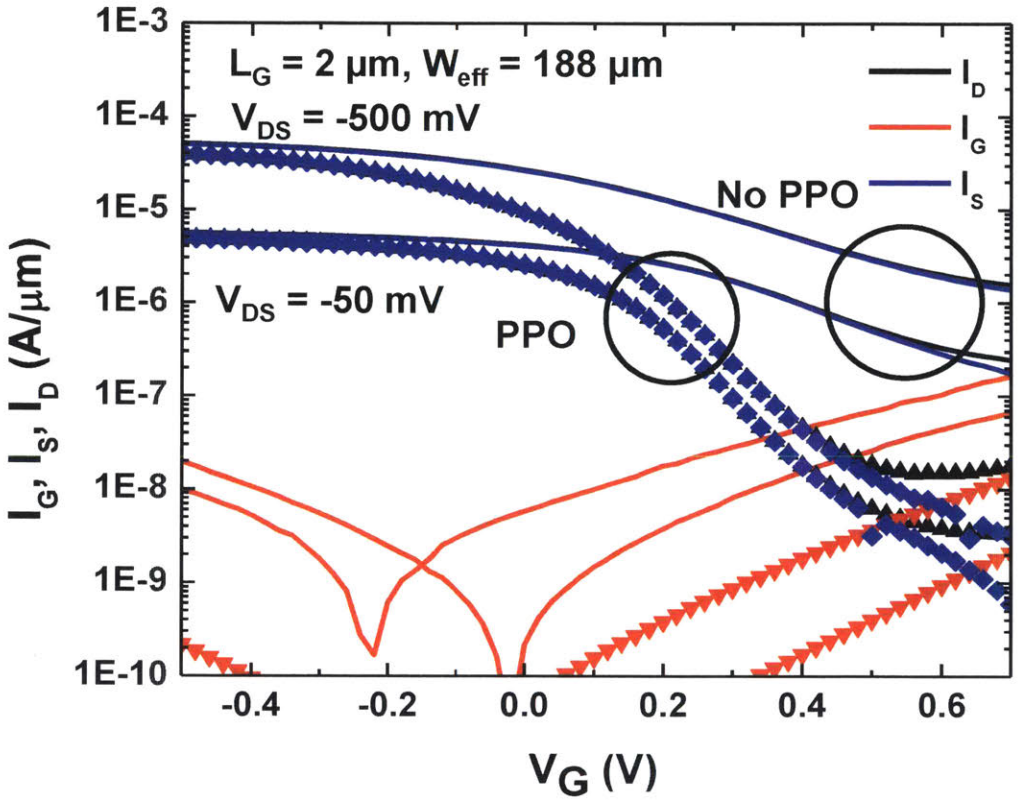


Figure 3.15. Transfer and gate leakage characteristics for a L_G = 2 μm annular p-MOSFET with (symbols) and without plasma post oxidation, PPO (solid lines). Improved sub-threshold swing is evident for the devices with the PPO process.

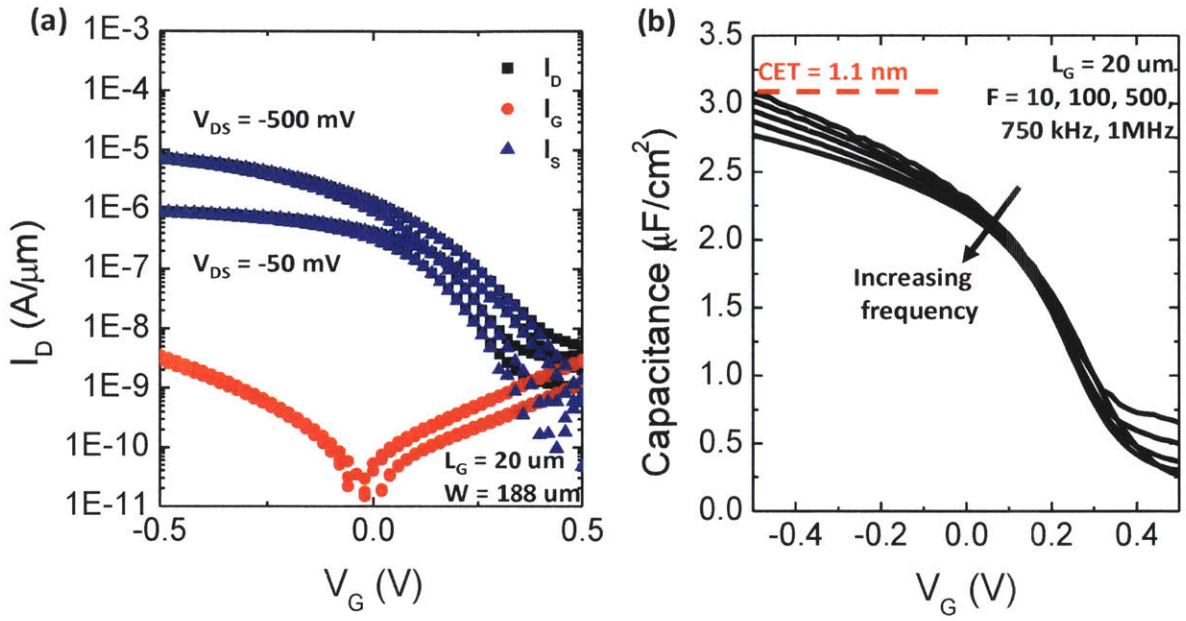


Figure 3.16. (a) I-V and (b) frequency dependent C-V characteristics for L_G = 20 μm p-MOSFET used for mobility extraction. A significant frequency dependence for C-V shows that the capacitance in the inversion and the depletion regime decreases with increasing frequency. The 10 kHz curve was used to extract the CET because it is the curve with the maximum capacitance. The 100 kHz curve was used to extract mobility to balance the reduction in the inversion and the depletion capacitance associated with interface traps.

The transfer characteristics for devices with and without PPO can be seen in Fig. 3.15. The device characteristics show that PPO improves: 1.) I_{max}/I_{min} (I_{max} and I_{min} refer to the maximum and minimum drain current shown for a given V_{DD} respectively), 2.) SS and apparent DIBL, 3.) the threshold voltage (more negative), and 4.) reduces the gate leakage due to the increase in the physical thickness of the gate oxide; apparent DIBL refers to a phenomenon which has causes a drain voltage dependent shift in the subthreshold current such as drain-dependent direct source to drain leakage. The improvement in the transfer characteristics, namely

the reduction in the SS, is clear and the origin of it is the reduction in the density of interface trap states (D_{it}). The threshold voltage also shifted to a more negative voltage which suggests that the interface traps tend to be acceptor states; this corroborates previous observations [73, 74]. The C-V characteristics of the device used for mobility extraction, Fig. 3.16b, shows the thin CET, ~1.1 nm, as extracted from the 10 kHz curve; this CET is below the lowest attainable CET obtained from using a Si cap for passivation. The reduction in the capacitance in the on-state, $V_G < -0.2$ V, is associated with the series resistance of the gate metal due to the large spreading resistance of the gate metal due to the large width of the device. The decreased capacitance in the weak-inversion to depletion regime, $V_G > 0.2$ V, is caused by the diminished response from interface traps. As a trade-off between the influence of the interface traps and the gate capacitance, a frequency of 100 kHz was chosen for mobility extraction. The extracted mobility for this device is compared to previously fabricated devices using ozone passivation in Fig. 3.17. The device with PPO has a reduced mobility which is expected because of the reduced CET. The reduction in the mobility as a function of CET is shown for biaxially strained-Ge with interfacial layers prepared with both PPO and ozone in Fig. 3.18. The trend for biaxially strained-Ge shows an approximately linear decline in the mobility with decreasing CET which is an expected trend as reported in Si and Ge [9, 53]. The mobility of the biaxially strained Ge with a scaled CET ~1.1 nm has a higher mobility than the s-Si device reported in [60] and shown in Fig. 3.4, 200 vs. 140 cm^2/Vs.

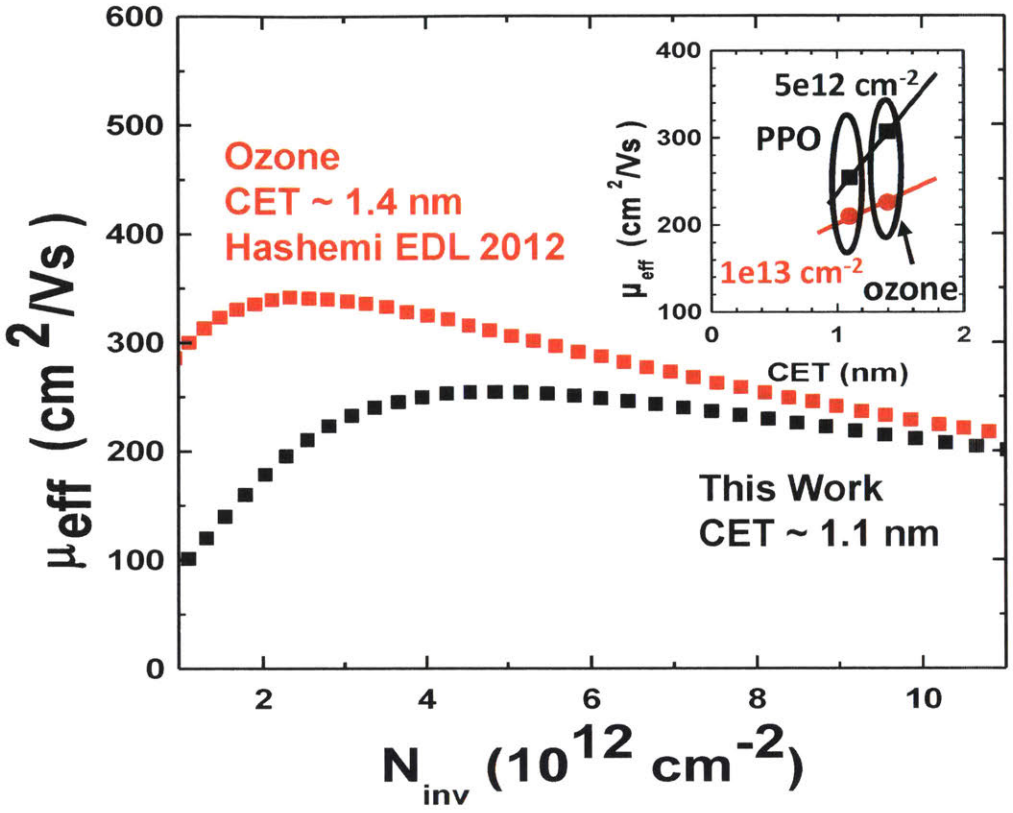


Figure 3.17. Effective mobility vs. N_{inv} for long channel (L_G = 20 μm) strained-Ge devices using ozone (11) compared to PPO (this work). PPO offers 3 Å CET reduction (~1.27X capacitance increase) over ozone while only ~7% mobility reduction penalty is measured at 10^{13} cm^{-2}.

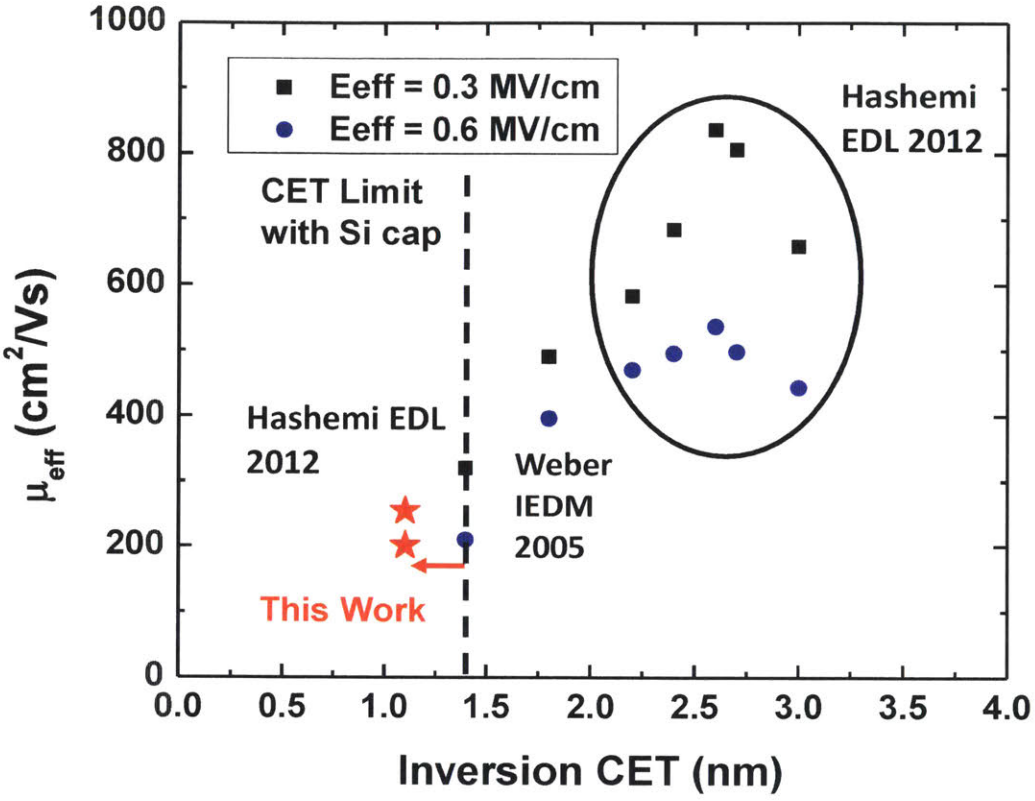


Figure 3.18. Effective mobility vs. inversion CET for published s-Ge devices with and without a Si cap and a gate-first process using ion implanted source/drains (8, 11, 18). Despite their significantly scaled inversion CET, the present devices exhibit comparable mobility (E_{eff}=0.6 MV/cm) or low mobility degradation compared to the rest of the devices [64, 66, 67].

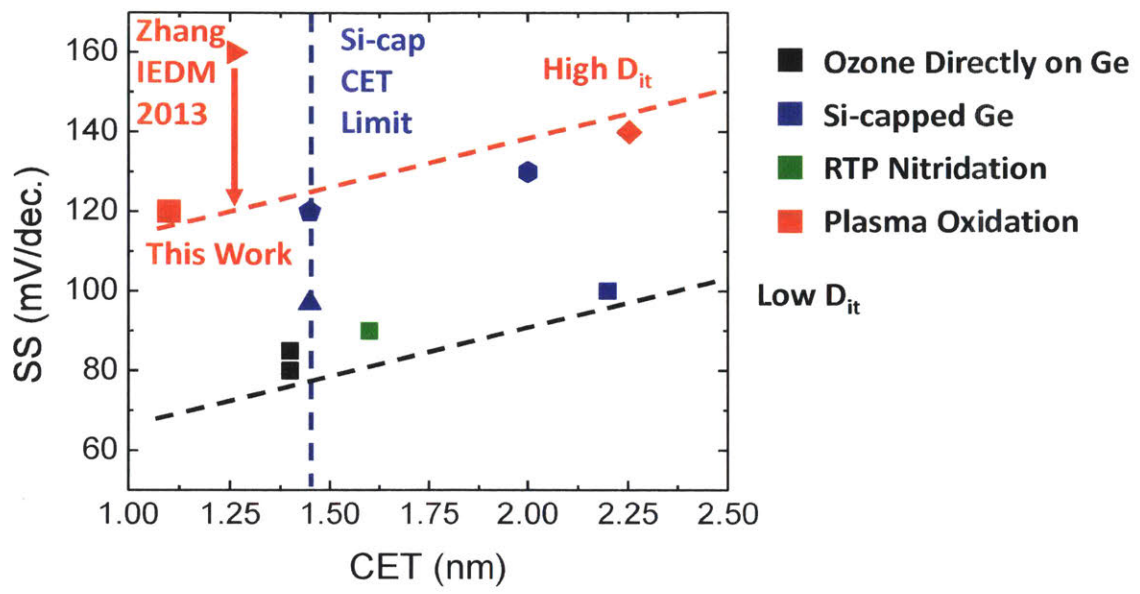


Figure 3.19. SS vs. CET for different technologies on s-Ge [65, 67-71, 75]. The CET is compared at V_{GS} - V_T = -0.7 V when possible. The figure is the same as figure 3.11 except for additional data points from Zhang et al. [71] and the SS from this work. Plasma post-oxidation is capable of scaling below the minimum CET with a s-Si cap of ~1.4 nm. Plasma post-oxidation is potentially a viable high-k technology except it tends to have higher interface trap densities (red dashed line) where other technologies such as ozone or Si-capped Ge tend to have lower densities of interface traps nearer to the black dashed line.

Interface traps have an effect on both the mobility and the subthreshold swing. To quantify the amount of D_{it} at the semiconductor-oxide interface, the SS is plotted against the CET which is seen in Fig. 3.19. The reason why this technique is used is because it is the easiest way to compare the apparent D_{it} between different works. The data points of SS vs. CET falls in a range and linear lines of high and low D_{it} are plotted to indicate the upper and lower bound of the range. The motivation of plotting a linear relationship between SS and CET for constant D_{it}

is because the correlation between SS and decreasing CET is based upon a capacitance divider, Eq. 3.1.

$$SS = 60\frac{mV}{decade}(1 + \frac{C_{it}}{C_{ox}}) \quad (3.1)$$

Where SS is the subthreshold swing, C_{it} is the capacitance associated with the interface traps, and C_{ox} is the capacitance of the oxide. C_{ox} is inversely proportional to the effective oxide thickness hence the SS is directly proportional to the EOT with a slope depending upon the amount of D_{it}. For the p-MOSFETs with PPO treatment done in this work, the extracted D_{it} is on the upper trend line suggesting that the PPO treatment still needs to be further optimized. With further improvement to the D_{it}, the mobility could increase [71, 72, 76] and the SS will be reduced.

The fabricated s-Ge p-MOSFETs showed that PPO and GeO_x could be used to scale the CET to a low value of ~1.1 nm which is desired for electrostatic integrity of the MOSFETs in future generation nodes. The higher mobility of Ge was maintained relative to that of Si despite the scaled oxide thickness and higher D_{it}. However, both of these improvements came at a cost of increased D_{it} and SS for PPO, and further improvements in the gate oxide technology would be required for Ge to be competitive as a p-MOSFET channel material.

3.4 Threshold voltage for Ge p-MOSFETs

The threshold voltage is another design consideration that needs to be met for a MOSFET to be technologically relevant, and some materials have a harder time than others to meet this requirement; this work does not specifically address this problem for Ge. Ideally, it should be simple to achieve a negative threshold voltage for Ge p-MOSFETs because the electron affinity is very close to Si, 4.0 eV (Ge) versus 4.05 eV (Si). However, experimentally it has not been easy to obtain a negative threshold voltage for Ge for scaled devices. The low power and high

performance threshold voltages of ~-330 and ~-130 mV respectively must be met. To investigate whether or not Ge p-MOSFETs have been able to achieve these values, the threshold voltages for different Ge p-MOSFETs are plotted versus the gate length in Fig. 3.20. There are only a few demonstrations of short-channel Ge devices near the future expected gate lengths, but for gate lengths below 100 nm there are no demonstrations of negative threshold voltages. Most of the demonstrations of negative threshold voltages have occurred on bulk n-Ge substrates and at long gate lengths. There are two reasons why Ge MOSFETs have a difficult time meeting the threshold voltage requirements. First, defects in Ge tend to be acceptor states which shift the threshold voltage to more positive values; this is also observed in SiGe p-MOSFETs [55, 73, 76]. The second is that Ge devices also tend to have worse short-channel effects due to the higher permittivity constant and a higher number of interface states [17, 53]. Because neither of these parameters are intrinsically limiting, with more technological improvements in both the gate oxide technology and stronger scaling of other electrostatic parameters, such as the gate oxide thickness, the threshold voltage could meet the required specifications.

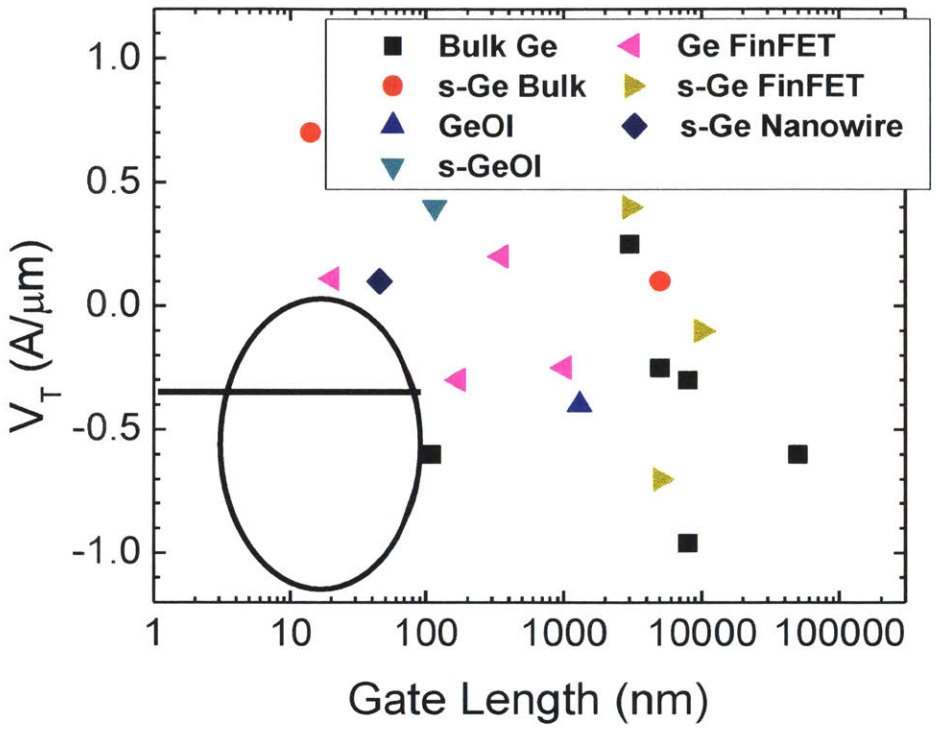


Figure 3.20. Threshold voltage (V_T) in saturation (V_{DS} = -0.5 V when possible) versus the gate length for most published Ge p-MOSFETs [40, 53, 54, 57, 61, 65, 69, 71, 74, 77-87]. Different symbols represent different technologies which are shown in the legend. An abbreviation that was not previously used is GeOI which stands for germanium on insulator. The plot shows that no demonstrations with negative threshold voltages for devices under L_G = 100 nm are available. There are few demonstrations of devices with a threshold voltage near the desired saturation threshold voltage for low power (V_T = 0.351 V from the ITRS roadmap Table 3.1) but most of them are on bulk Ge.

3.5 Limitations of I_{off} in Ge p-MOSFETs

The main challenge for high mobility channel materials as described from the previous chapter is the off-state current because of the tendency to have a reduced bandgap relative to Si.

Ge is a channel material which also faces the challenge of having a smaller bandgap, 0.66 eV, relative to Si, 1.1 eV, and may have higher I_{min}, the minimum attainable current for a given V_{DS} schematically shown in Fig. 2.8 from the previous chapter; the work in this thesis did not attempt to attain the desired I_{min} but rather to show the historical trends. To look at the extent of the problem, I_{min} can be plotted against L_G for different Ge technologies, Fig. 3.21. Practical implementations of Ge devices for future technology nodes are FinFETs and Ge nanowires, but there are not enough Ge nanowire devices to extrapolate a trend against gate length. The red dashed line is the trend in the minimum current for FinFETs which shows that for future gate lengths, Ge could potentially even have a difficult time meeting the high performance I_{off} current of 100 nA/μm. This means that while high currents and thin gate dielectrics can be achieved using Ge and s-Ge, the off-current needs to be reduced or else it will be the showstopper for Ge.

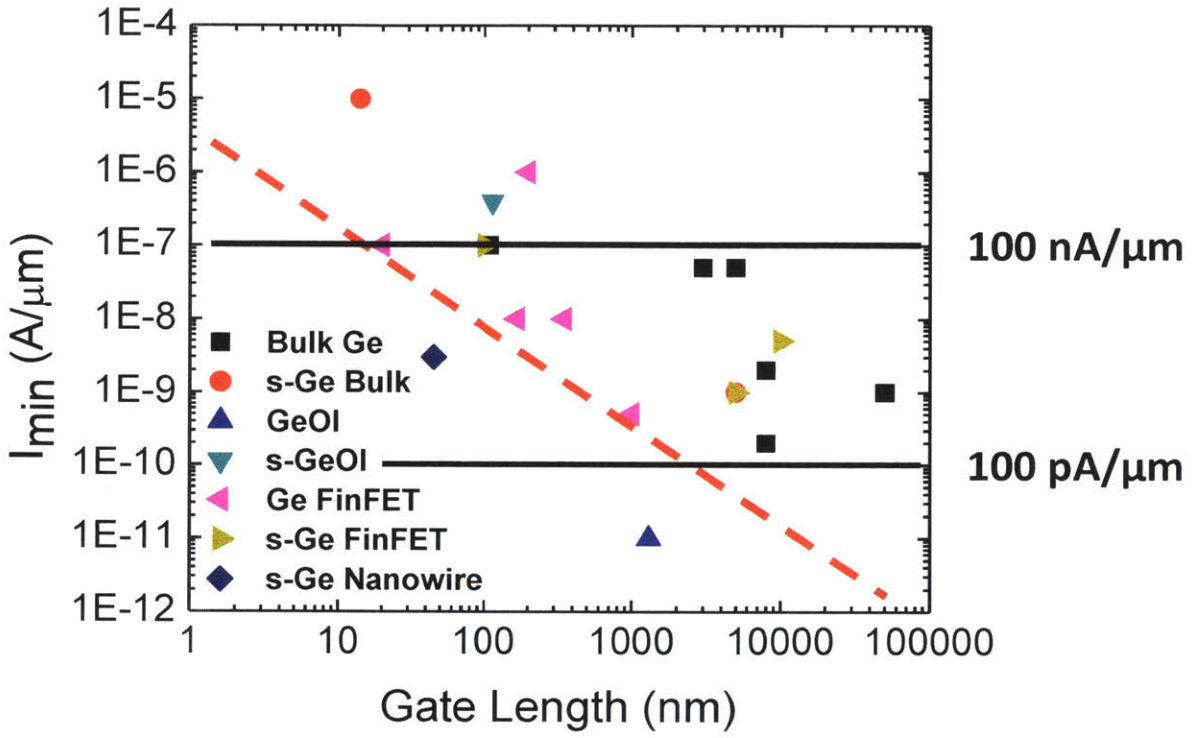


Figure 3.21. Minimum current (I_{min}) in saturation (V_{DS} = -0.5 V when possible) versus the gate length for most published Ge p-MOSFETs [40, 53, 54, 57, 61, 65, 69, 71, 74, 77-87]. I_{min} refers to the minimum current that can be obtained as a given V_{DS}. Different symbols represent different technologies which are shown in the legend. A dotted red trend line is shown for the minimum current obtained for relaxed Ge finFETs which are the lowest off-state current devices for Ge with multiple data points. The trend line illustrates that the off-state current is too high for low power devices which require the off-state current to be 100 pA/μm and may be borderline for future scaled devices requiring an off-state current of 100 nA/μm.

3.5 Summary and Conclusion

This chapter has explored the feasibility of Ge and s-Ge as a channel material. Experimentally, the chapter experimentally explores whether Ge and s-Ge could potentially outperform Si and s-Si in terms of on-current and its potential for short-channel scaling. Based upon the experimental work presented in this thesis and previous experiments, Ge channel p-MOSFETs appear to be scalable to short physical gate lengths and have the ability to achieve higher on-currents than Si for a given V_{DD}.

The ability to achieve other requirements such as the desired threshold voltage and off-current have not been demonstrated in any work thus far. The origin of the positive threshold voltage likely comes from the nature of defects in Ge which tend to act like acceptor states, and this challenge will dissipate as the quality of the gate oxide on Ge improves. The off-current is a more significant challenge that is intrinsic to the small bandgap of Ge. Based upon extrapolation of the current trends for Ge, device designers could potentially struggle to achieve even the high-performance off-state leakage of 100 nA/μm benchmark for future nodes, and engineering will need to be done in order to reach this and lower current levels. This is the likely showstopper for the practicality of Ge p-MOSFETs in future technology nodes. A more practical approach may be to trade-off the high mobility of Ge and to use $Si_{1-x}Ge_x$ channel devices instead which have a higher mobility than Si and but also a larger bandgap than Ge.

Chapter 4: Introduction and Motivation for s-Si/s-Ge Tunnel Field Effect Transistors (TFETs)

The work in this thesis on TFETs attempts to understand the reason or reasons why TFETs have not experimentally shown a combination of high drive currents, similar to MOSFETs, and a subthreshold swing (SS) steeper than 60 mV/decade at room temperature. This chapter explains the design of the experimental s-Si/s-Ge heterostructure TFETs fabricated in this work, describes the fabrication of said TFETs, and presents the associated electrical characteristics.

4.1 TFET Design Considerations

There are several ways an experimental TFET can be designed but it should utilize both geometry and process technology to attempt to isolate the fundamental tunneling physics or identify what technological factors if any limit the TFET performance and result in low drive currents or higher SS than MOSFET. The most basic design consideration when making a TFET is the device geometry. TFET designs can all be generalized into two types of designs, transverse and in-line, depending on the alignment of the electric field profile of the gate relative to the tunneling direction and the TFET schematics can be seen in Fig. 4.1.

The transverse n-TFET gets its name because the gate electric field is transverse or perpendicular to the tunneling direction. In this schematic the gate electric field is in the vertical direction and the tunneling is in the horizontal direction. The way that this TFET turns from "off" to "on" is that the gate controls the energy level of the conduction band at the interface between the gate oxide in the intrinsic channel referenced to the source. When the conduction band-edge of the channel aligns with the valence band-edge of the source, tunneling results and

electrons are generated in the channel corresponding with holes being generated in the source. The electrons in the channel are collected out of the drain which is n-type while the holes in the source are collected out of the source.

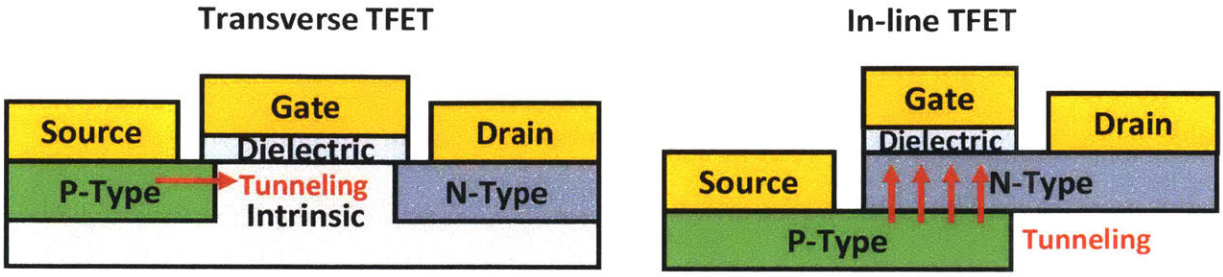


Figure 4.1. Schematic of the two types of TFETs, transverse and in-line. In the transverse n-TFET, electron tunneling occurs transverse to the gate electric field from the valence band of the p-type source to the conduction band of the intrinsic channel when the gate aligns the bands. The gate electric field is parallel to the tunneling in an in-line TFET. An electron from the valence band of the p-type source tunnels to the conduction band of the n-type channel when the gate aligns or overlaps the band-edges.

For the in-line TFET, the gate electric field and tunneling are in the same direction, in this case the vertical direction. The way the in-line n-TFET works is that semiconductor layer, the n-type layer in Fig. 4.1, underneath the gate is depleted by the higher doped p-type region underneath it. A positive bias is applied to the gate to accumulate electrons at the top of the channel underneath the gate oxide thereby aligning the conduction band of the n-type semiconductor at the top of the channel to the valence band at the top of the p-type layer. The approximate tunneling distance is the thickness of the n-type layer. In this structure, there is an inherent trade-off between the tunneling current and the gate control. The thickness of the n-type layer determines the width of the tunneling barrier and therefore the thicker the n-type later, the lower the tunneling current. However, the thickness of the n-type layer also dictates how much

capacitance exists for the p-n junction, between the p-type layer and the electron gas at the interface between the gate and the semiconductor. The capacitive divider between the gate oxide capacitance and the p-n junction capacitance determines the efficiency of the gate; if the n-type layer thickness is reduced the gate efficiency drops.

Both TFET architectures do different things well. The transverse TFET has some distinct advantages, it has: 1.) better gate control, 2.) better device footprint scalability, and 3.) simpler fabrication. The in-line TFET has benefits due to: 1.) 1D electrostatics, 2.) ease of heterojunction integration. The transverse TFET shines when it comes to electrostatics because of the geometrical layout. The transverse TFET's p-n junction is at the gate edge and that capacitance is small relative to the gate capacitance (gate area tends to be much larger than the source to channel junction area). An in-line TFET's p-n junction has the same area as the gate area, and this causes the capacitance of the p-n junction to be quite large. What this means is that the gate efficiency for in-line TFETs is intrinsically poorer due to the capacitive divider. The other benefit for making a transverse TFET is that it has better footprint scalability. The transverse TFET's current theoretically should not change as a function of gate length assuming the tunneling current dominates the device resistance. When the device is scaled the overall gate capacitance drops while the parasitic fringing capacitances stay the same suggesting that this device could maintain its performance, defined as dQ_g/dI_D, as the device is scaled down. The in-line TFET has areal scaling for both current and capacitance. If and when the device is scaled, the tunnel current and capacitance scale with area. If the parasitic capacitance is constant then reduced performance will be realized which means that the in-line TFET will be a bad choice for footprint scaling. Finally, the device structure for an in-line TFET requires that there be an undercut between the channel and drain. This makes the fabrication for the in-line difficult

relative to the transverse TFET and is another reason why the transverse TFET is a more practical structure. Nevertheless, while the in-line TFET is the poorer choice in terms of technology, it is the preferable structure in terms of studying TFET behavior due to a number of other factors as explained next.

The transverse TFET is a more complicated structure for analysis due to the fact that calculating the electrostatics requires 2D simulations. The channel electrostatics for a MOSFET are not known exactly, and therefore the electrostatics for a TFET with a similar layout are also difficult to analyze. By fabricating an in-line TFET, one can simplify the electrostatics to 1D because the gate electric field and tunneling occurs in the same direction simplifying the analysis. The other benefit for the in-line TFET is that heterostructures can be more easily integrated. The reason behind this is that the structure is vertical and the heterostructure, with or without strain, can be conveniently grown by epitaxy. For a transverse TFET, it is not so simple to investigate heterostructures although it has been done before [42, 47, 49, 88-92]. In order to integrate a heterostructure, one either needs to do a source replacement or to make a vertical-sidewall, fin or nanowire, TFET. For both of these reasons, the in-line TFET tend to be the structure of choice to study the device and tunneling physics for homo- and hetero- junction devices. This work has both transverse and in-line TFETs built into the mask set allowing for the choice of studying either TFET design.

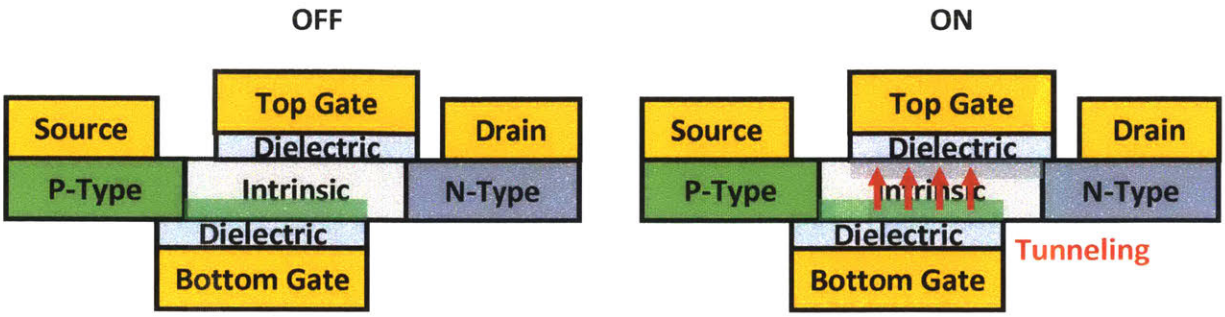


Figure 4.2. A schematic of a 2-gate bilayer TFET in the ON and OFF states. In the OFF state, a hole 2D gas is accumulated at the semiconductor surface with the bottom gate oxide because of a constant negative bias on the bottom gate. The device is turned to its ON state when a large positive bias is applied to cause an electron 2D gas at the surface of the semiconductor beneath the top gate oxide. At this point, electrons from the valence band at the bottom interface can tunnel to the conduction band of the top.

Transverse and in-line are two general TFET geometries and each TFET class requires different methods of fabricating the device. The in-line TFET has two layouts, the conventional in-line TFET, Fig. 4.1, and the bilayer TFET, Fig. 4.2. The reason that it is called a bilayer TFET is because of the presence of both an 2D electron and hole gas that results in tunneling [15, 93-95]. The way the electron and hole gases are formed is from electrostatic doping by the two gate electric fields. The top gate is in contact with an n-well and a positive bias is applied to cause a 2D electron gas. The bottom gate is in contact with the p-well and a negative bias is applied to populate the bottom of the channel with holes from the source resulting in the tunneling current between the two charge gases in the ON state. The only reason to make this structure is to study the impact of doping on the characteristics of tunneling without chemical doping. By using

electrostatic doping, one can form electron and hole wells without any intentional dopants thereby reducing the number of states in the bandgap.

In a practical sense here are many difficulties in making the bilayer TFET compared to a conventional in-line TFET. The bilayer device requires top- and bottom-gates that are underlapped relative to each other. This requires an isolated local bottom gate below the semiconductor layer which makes the fabrication of the device complex. The fact that there are two gates means that they will compete against each other resulting in poor gate efficiency for either gate, extremely high electric fields and potentially high gate leakage currents; the amount of electric field can be seen for various materials in Fig. 4.3. The amount of band bending in the semiconductor that is necessary is the entire bandgap of the semiconductor plus whatever ground-state eigenstates shifts that result from energy quantization that occurs due to the two triangular wells formed at the surfaces of the semiconductor [15, 96, 97]. This amount of voltage is extremely high and can lead to a high level of gate leakage which can mask the transition between the device turning OFF to ON. An analysis of gate leakage for Si and InAs is summarized in Fig. 4.4 [15].

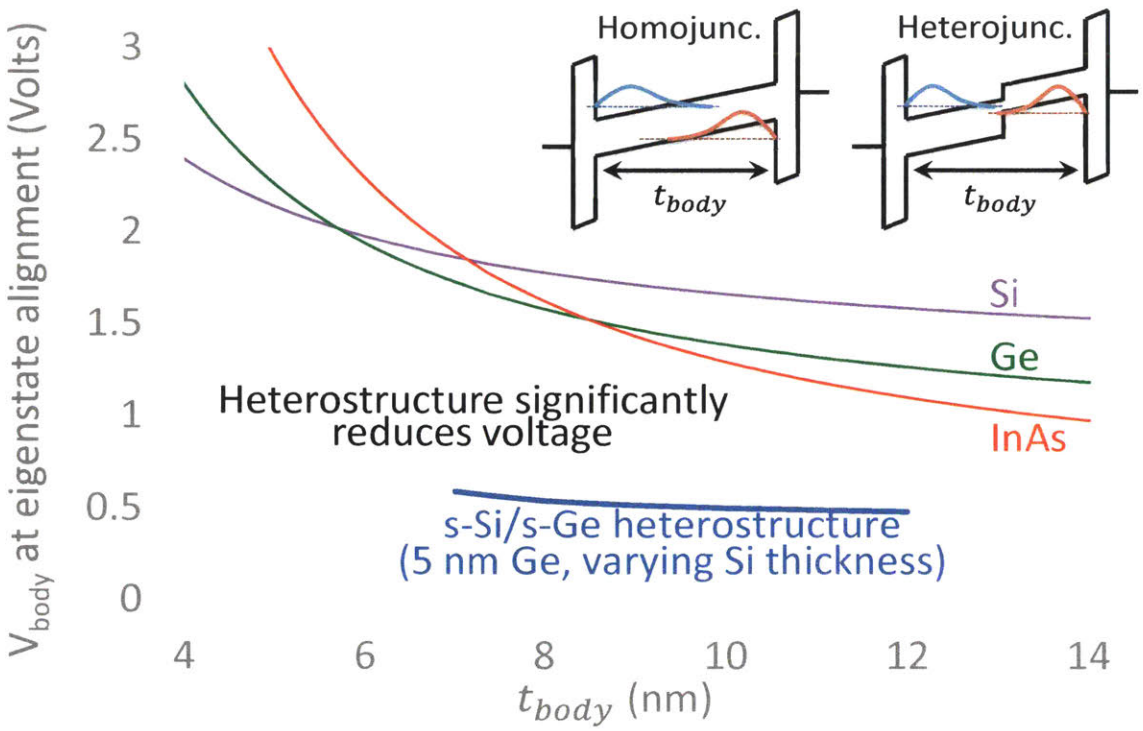


Figure 4.3. The voltage drop across the semiconductor for alignment of the first eigenstates of the conduction and valence bands in a bilayer TFET (V_{body} at eigenstate alignement) vs. semiconductor thickness, t_{body} is plotted for different hypothetical homojunction and heterojunction bilayer TFETs. The increase in the body voltage for decreasing t_{body} is caused by increased quantization energies. A significant reduction in the V_{body} at eigenstate alignment is achieved for a heterojunction bilayer TFET compared to a single material bilayer TFET. This can also be seen in the inset where a constant voltage is applied to both a homo- and hetero-junction bilayer TFET where only the heterojunction TFET has achieved eigenstate alignment. The figure was reproduced from [15].

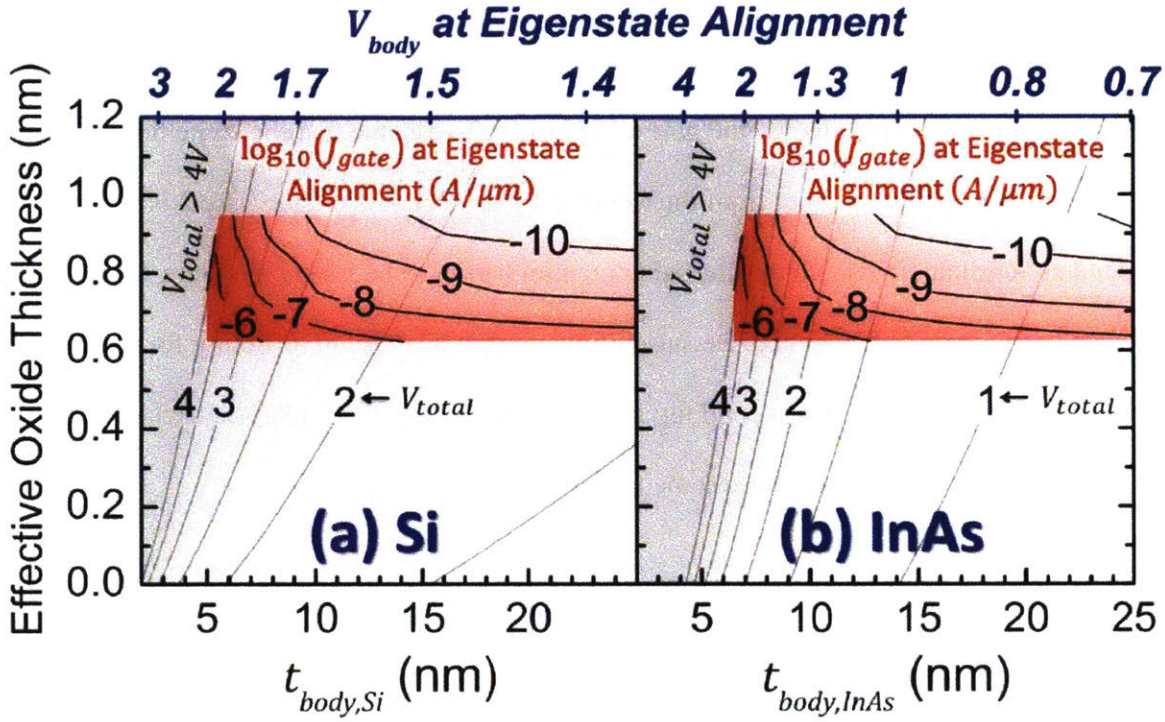


Figure 4.4. Gate leakage current (inset black contours with red shading) and total applied gate voltage, V_{total}, (gray contours) at eigenstate alignment as a function of effective oxide thickness and body thickness for (a) Si and (b) InAs. The leakage current is derived from high-κ on Si experimental data [98], and the top axis (V_{body} at eigenstate alignment) is derived from Fig. 4.3. The gate leakage (in A/μm of width) is calculated for a 50-nm gate length but can be scaled linearly with gate length. Decreasing t_{body} increases V_{body} and thus increases the electric field and gate leakage current. While InAs generally requires less voltage for eigenstate alignment compared to Si, the 30% larger relative permittivity of InAs causes a higher dielectric field resulting in similar gate leakage current contours. Figure and caption reproduced from [15].

While fabricating the bilayer TFET there is not much more effort required to add a gate making a 3-gate bilayer TFET, Fig 4.5. The method of operation is the same as the 2-gate bilayer TFET, but the top gate 2 acts as an independent gate which allows one to isolate the tunneling to

the electron gas beneath the top gate 1 and the hole gas at the surface of the semiconductor and the bottom gate; this mitigates the impact of the drain. By removing the influence of the drain, the tunneling is fully controlled by the gate allowing one to assume that the switching is only controlled by the band alignment from the top gate 1 bias. Because the top gate 2 is an independent terminal, it also allows the said potential barrier to be varied allowing for the influence of the drain to be studied. Because of the modest increase in difficulty for the extra fabrication, it is worth adding a second top gate although it makes the analysis trickier since the bias conditions of the top gate 2 need to be found empirically.

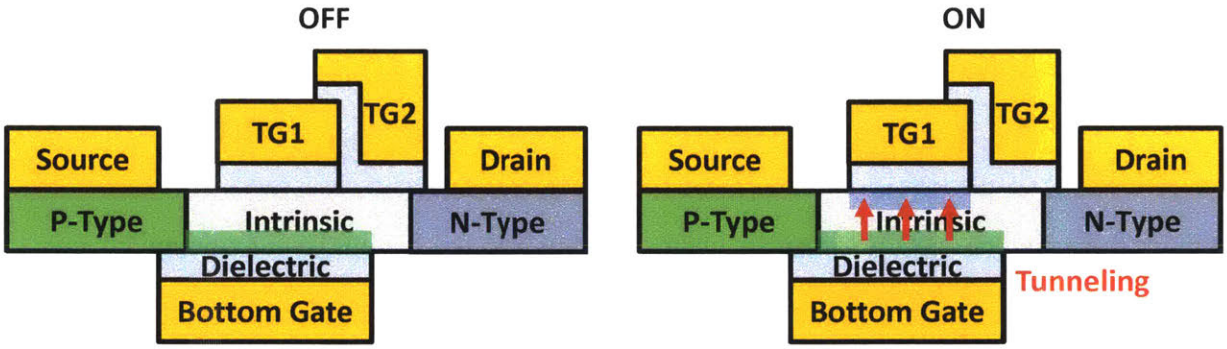


Figure 4.5. A schematic of a 3-gate bilayer TFET in the ON and OFF states. In the OFF state, a hole gas is accumulated at the semiconductor surface with the bottom gate oxide because of a negative constant bias on the bottom gate. The device is turned to its ON state when a large positive bias is applied to cause an electron gas to invert at the surface of the semiconductor beneath the top gate 1 oxide. At this point, electrons from the valence band of the hole gas can tunnel to the conduction band of the electron gas. Top gate 2 is biased so that no electron gas forms between the n-type drain and the electrons confining the tunneling to the areal overlap between top gate 1 and the bottom gate.

The design considerations of the experiment on TFETs in this thesis are built around the 3-gate bilayer TFET. This device has the most ideal structure to allow for studying the tunneling

physics, and the design considerations are made to mitigate the flaws in the structure. The structure of the s-Si/s-Ge 3-gate bilayer TFET was designed in order to mitigate the drawback of the high required voltage for operation. The s-Si/s-Ge heterostructure significantly reduces the gate voltage required because it has a type II band alignment, Fig. 4.6. In the type II heterostructure the effective bandgap is smaller than either of the bandgaps of the two materials because of the conduction and valence band offsets. For the s-Si/s-Ge heterostructure, the large valence and conduction bands favor the s-Ge and s-Si as the hole and electron wells respectively. When the heterostructure is biased to ON, significantly less voltage or band bending is required than for a homojunction bilayer TFET based upon the calculations illustrated in Fig. 4.4. The reason why this particular heterostructure vs. other type II heterostructures was used is because it has been well characterized in [99]. Another problem in the bilayer TFET is the poor gate efficiency which is an intrinsic and cannot be mitigated, but it would not prevent accurate extraction of the tunneling physics because it can be calculated using simulations [95, 97] or directly using experimental techniques, and therefore it should be possible to extract the intrinsic tunneling characteristics.

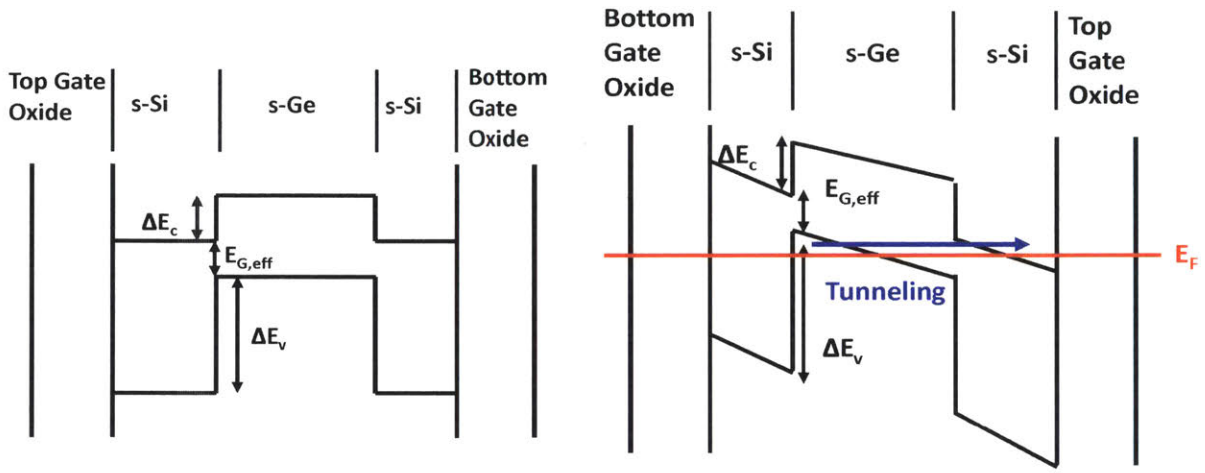


Figure 4.6. Band diagram of the s-Si/s-Ge/s-Si heterostructure depleted (left) and ON (right). The s-Si heterojunction has a type II band alignment with a $\Delta E_c \sim 250$ meV, $\Delta E_v \sim 770$ meV and $E_{G,eff} \sim 180$ meV. The band diagram in the ON state is drawn for a negative bottom gate voltage and a positive top gate voltage resulting in the formation of a hole and electron gas respectively. Tunneling of electrons from the valence band of the s-Ge to the conduction band of the s-Si allows current to conduct.

4.2 Fabrication of s-Si/s-Ge Bilayer TFETs

The fabrication of the device began with the fabrication the substrate or the s-Si/s-Ge/s-Si heterostructure on top of the embedded bottom gate; the detailed process flow can be found in Appendix B. Previous work [62, 100, 101] has been done fabricating different strained semiconductors on insulator, but did not have a patterned and embedded bottom gate which is an additional challenge.

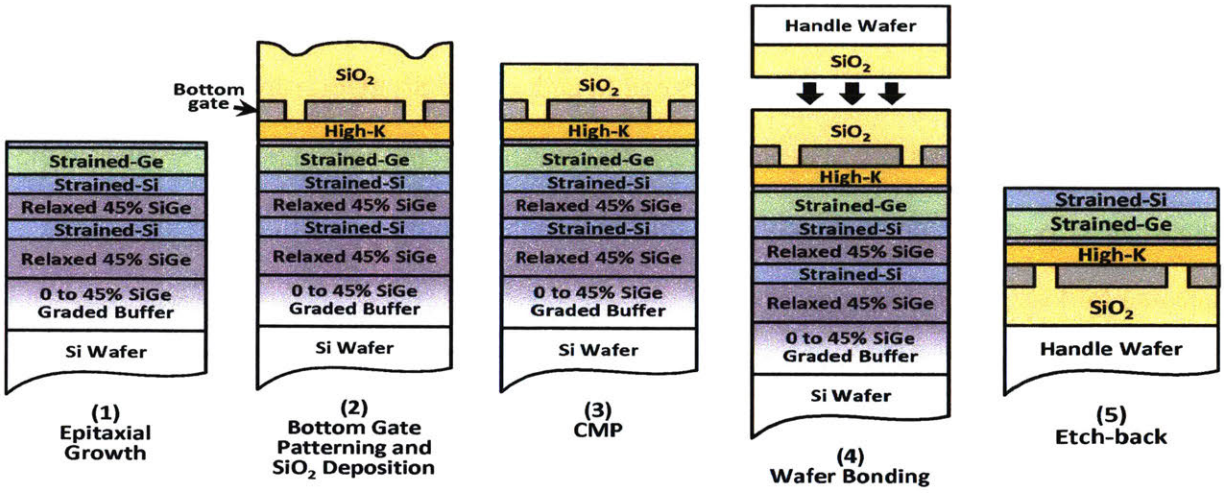


Figure 4.7. Schematic for the bond and etchback process for the starting wafers for the s-Si/s-Ge 3-gate bilayer TFET. The wafer fabrication first begins with (1) epitaxial growth on the sacrificial wafer; the unlabeled top layer is a thin s-Si layer used to improve the oxide interface of the bottom gate oxide. (2) After epitaxial growth of the sacrificial layer, the bottom gate high-κ, bottom gate metal are deposited and patterned. SiO_2 is subsequently deposited for bonding and planarization. (3) The SiO_2 is planarized using CMP to create a flat and low roughness surface for wafer bonding. (4) The sacrificial wafer is bonded to a thermally oxidized handle wafer. (5) The undesired layers are removed using mechanical and chemical processes resulting in the desired device layer on the bottom gate. Figure reproduced from [15].

The bond and etchback process used to fabricate the substrate in this process begins with the epitaxial growth of the heterostructure, Fig. 4.7, consisting of a virtual substrate, etchback layers and the device layer. The virtual substrate generates the desired lattice constant, in this case the lattice constant of $Si_{0.45}Ge_{0.45}$, while at the same time having minimizing the threading dislocation density caused by the relaxation of strain, by slowly varying the lattice constant [102]. The compositional rate of change is 10% increase in the Ge fraction for every 1 μm of growth. A 1 μm thick relaxed buffer layer, $Si_{0.45}Ge_{0.45}$, is grown on top of the virtual substrate to

reduce the defect density to approximately 10^6 dislocations/cm^2 as measured from the etch pit density test [62]. Chemical etch-stop layers of s-Si and relaxed $Si_{0.45}Ge_{0.45}$ are subsequently grown before the s-Si/s-Ge/s-Si device layers. The thickness of the bottom most s-Si layer in the device layer is grown approximately 4 nm thicker than the desired device thickness in order to account for loss of s-Si during processing.

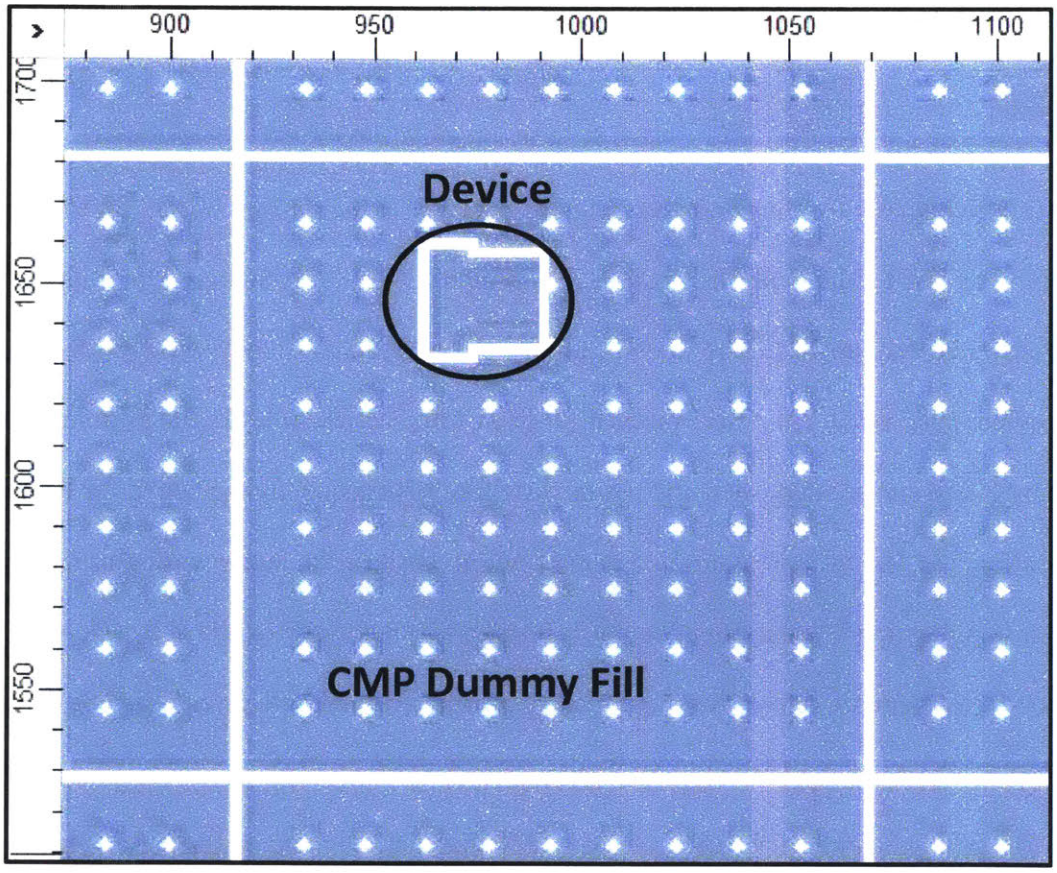


Figure 4.8. The mask layout of the bottom gate showing the pattern and the CMP dummy fill around it. The circled device indicates the local bottom gate of a device with CMP dummy fill around it covering the majority of the area. The purpose of the CMP dummy fill is to prevent pad deformation from a local protrusion. The figure is adapted from [15]

The steps after wafer growth consist of bottom gate oxide and metal deposition, patterning of the gate metal, oxide deposition, chemical and mechanical polishing (CMP), wafer

bonding, and mechanical followed by chemical removal of the sacrificial layers. The bottom gate oxide process consisted of flowing 1 minute ozone to form SiO_2, depositing the gate oxide (20 nm ALD Al_2O_3) and gate metal (50 nm plasma enhanced ALD, PEALD, TiN) at 300 °C. After, the gate stack was deposited, the gate metal was patterned using photoresist and dry etching; the pattern has many dummy metal structures surrounding the desired pattern as shown in Fig. 4.8 in order to make sure that the CMP is uniform. 500 nm SiO_2 is deposited using low pressure CVD (LPCVD) at 400 °C to encapsulate the entire pattern. CMP is used to planarize and reduce the surface roughness of the wafer to allow for wafer bonding. After CMP, the sacrificial wafer is bonded to thermally oxidized handle wafer. The stack is flipped over and mechanical polishing is used to thin the thickness of the sacrificial wafer down to 100 μm.

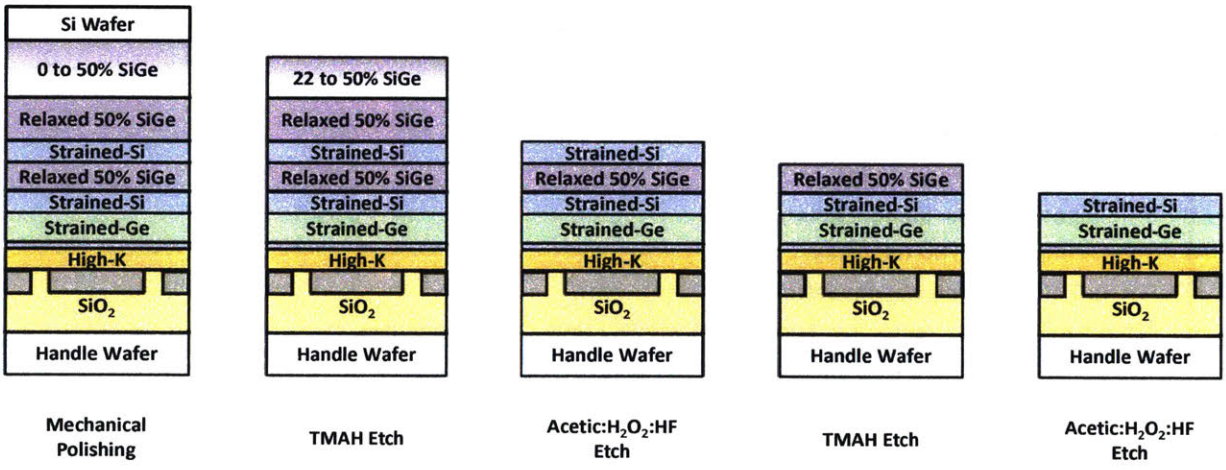


Figure 4.9. Mechanical and chemical etchback process with the etchant process step the schematic of the resulting heterostructure.

After mechanical thinning, oxide is deposited on the backside of the handle wafer to prevent scratches in the backside from being attacked by subsequent chemical etch steps; the wafer etch steps are shown in Fig. 4.9. 25% TMAH is used to remove the remainder of the sacrificial Si wafer and part of the graded buffer layer up to $Si_{0.78}Ge_{0.22}$. The remaining portion of

the graded buffer layer and relaxed buffer layer are removed in a solution containing acetic acid, hydrogen peroxide and hydrofluoric acid with a ratio of 9:6:1 respectively. The s-Si etch-stop layer is removed using 25% TMAH which stops on the final relaxed $Si_{0.45}Ge_{0.45}$ layer. This layer is removed in the same acetic acid, hydrogen peroxide and hydrofluoric acid solution leaving a blanket film of s-Si/s-Ge/s-Si heterostructure on the locally patterned bottom gates; the thickness of the s-Si/s-Ge/s-Si heterostructure at this point is 9 nm/7 nm/3 nm respectively.

- **Epitaxial growth of sacrificial wafer**
- **Deposit and pattern back-gate (1 minute O_3/245 cycles (200A) Al_2O_3 300C/ 50 nm TiN via plasma ALD)**
- **Bond and etch-back to form SGDOI wafers**
- **Mesa Patterning (CF_4/CHF_3 etch to stop on Al_2O_3)**
- **Pre-ALD clean: 10:1 H_2SO_4:DI, 10:1 HCl:DI, 15s 500:1 HF:DI**
- **Top gate 1 high-k/metal (1 minute O3/55 cycles (50A) Al2O3 300C/1400 cycles (500) WN via plasma ALD)**
- **Top gate 1 patterning and RIE**
- **Pre-ALD clean: 10 min. nanostrip**
- **Top gate 2 high-k/metal (1 minute O_3/55 cycles (50A) Al_2O_3 300C/1400 cycles (500) WN via plasma ALD)**
- **Top gate 2 patterning and RIE step 1 - n-type implant definition**
- **Self-aligned Drain implant (P, no tilt, 10 keV, 2e15 cm^{-2})**
- **Top gate 2 patterning and RIE step 2**
- **Non-aligned Source implant lithography**
- **Source implant (B, no tilt, 5 keV, 2e15 cm^{-2})**
- **Pre- ILD clean 10 minute nanostrip**
- **220 nm PECVD ILD deposition and S/D activation at 500°C for 30 minutes**
- **Contact via open, Ti/Al metallization and FGA at 450°C for 30 minutes**

Figure 4.10. The device process flow beginning after the wafer fabrication for all s-Si/s-Ge TFETs.

The abbreviated process flow can be seen in Fig. 4.10. Device fabrication begins with the patterning of the s-Si/s-Ge/s-Si heterostructure into mesas. The mesa is patterned using a fluorine chemistry dry etch (CF_4/CHF_3) in order to stop on the Al_2O_3 bottom gate and is lithographically aligned to the bottom gate; because the semiconductor heterostructure is so thin, the patterned metal layer can be clearly seen and aligned to. Problems with lithographic alignment were

observed because of the distortion in the pattern after the wafer bonding process; details about this fabrication problem and other problems can be seen in Appendix C. After mesa patterning, the substrates were cleaned in 10:1 H_2SO_4, 10:1 HCl and 500:1 HF before the deposition of the first top gate. The first top gate stack of 1 nm SiO_2 formed by ozone, 5.5 nm Al_2O_3 was deposited via ALD and the gate metal, 50 nm WN, was deposited using PEALD. The first gate metal was patterned using a SF_6 based dry etch, and the substrate was subsequently cleaned using nanostrip. The second top gate was deposited next which consisted of the same gate stack as the first gate, 1 minute ozone/5.5 nm Al_2O_3 and 50 nm WN. The second gate was partially patterned, and the phosphorus drain implant was self-aligned to the pattern. After ion implantation, the remainder of the second gate was patterned using a SF_6 dry etch. The boron source implant was masked by photoresist in a subsequent step and therefore not self-aligned to top gate 2. After ion implantation, the interlayer layer dielectric, SiO_2, is deposited using PECVD and the ion implants were activated at 500 °C for 30 minutes. A standard via, Ti/Al metallization process followed by a 400 °C forming gas anneal was used to complete the device fabrication.

Because of the flexibility of the fabrication process transverse, 2-gate bilayer and 3-gate bilayer TFETs can all be fabricated on the same wafer; figures 4.11 and 4.12 show the schematics of the transverse and 3-gate bilayer TFETs and the as-fabricated devices respectively. Cross-section TEM (XTEM) showing select cross-section areas of the 3-gate bilayer TFET can be seen in Fig. 4.13. The TEM shows that the final heterostructure and gate oxide thicknesses are similar to the as expected thicknesses in the process. It also shows that the morphology of the three gates is similar to what was expected from the fabrication.

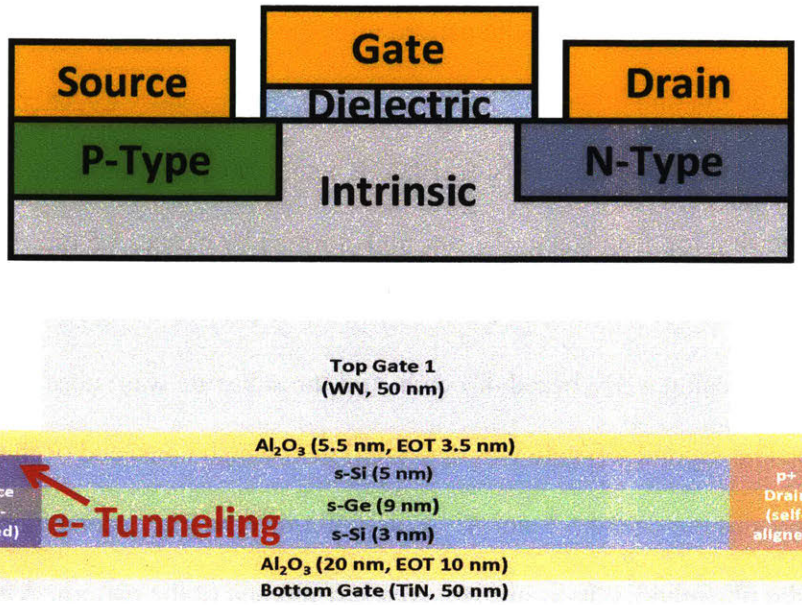


Figure 4.11. The schematic of a general transverse TFET, the actual fabricated version of the device, 2-gate s-Si/s-Ge transverse p-TFET, is shown from top to bottom. A significant difference between the schematic and fabricated TFETs exists due to the bottom gate and the s-Si/s-Ge heterostructure. The fabricated transverse TFET is a p-TFET and tunneling of electrons occurs between the valence band of the s-Ge in the channel to the s-Si of the n+ source.

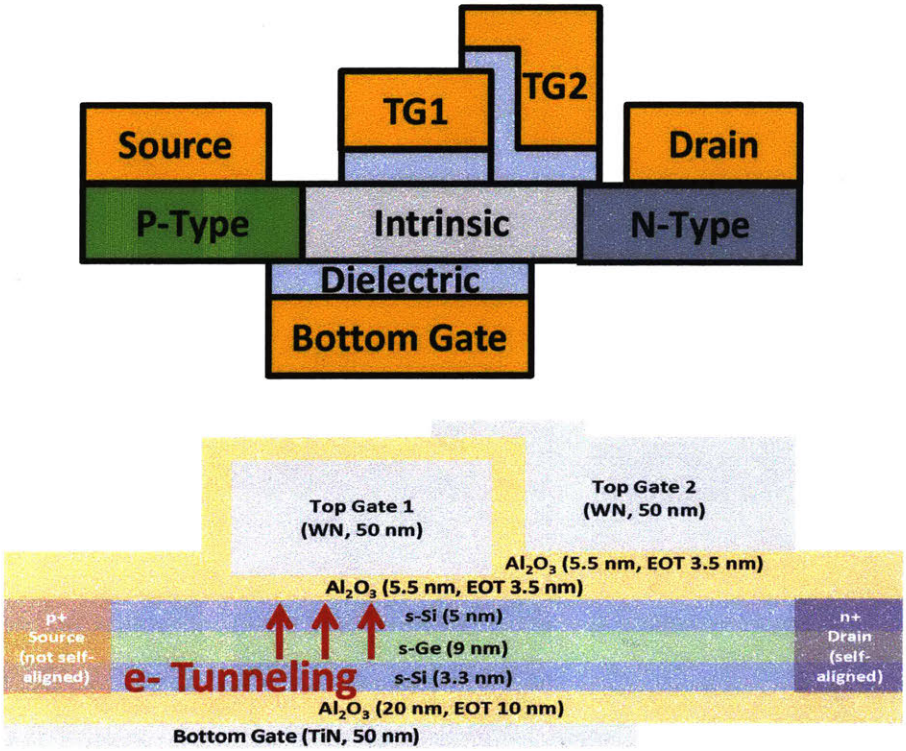


Figure 4.12. The schematic of a 3-gate bilayer TFET, the actual fabricated version of the device and a simplified circuit element is shown from top to bottom. The main difference between the schematic and fabricated TFETs exists because of the s-Si/s-Ge heterostructure that is the channel. The fabricated 3-gate TFET is a n-TFET and tunneling of electrons occurs between the valence band well of the s-Ge at the bottom surface of the s-Ge to the s-Si conduction band well underneath top gate 1.

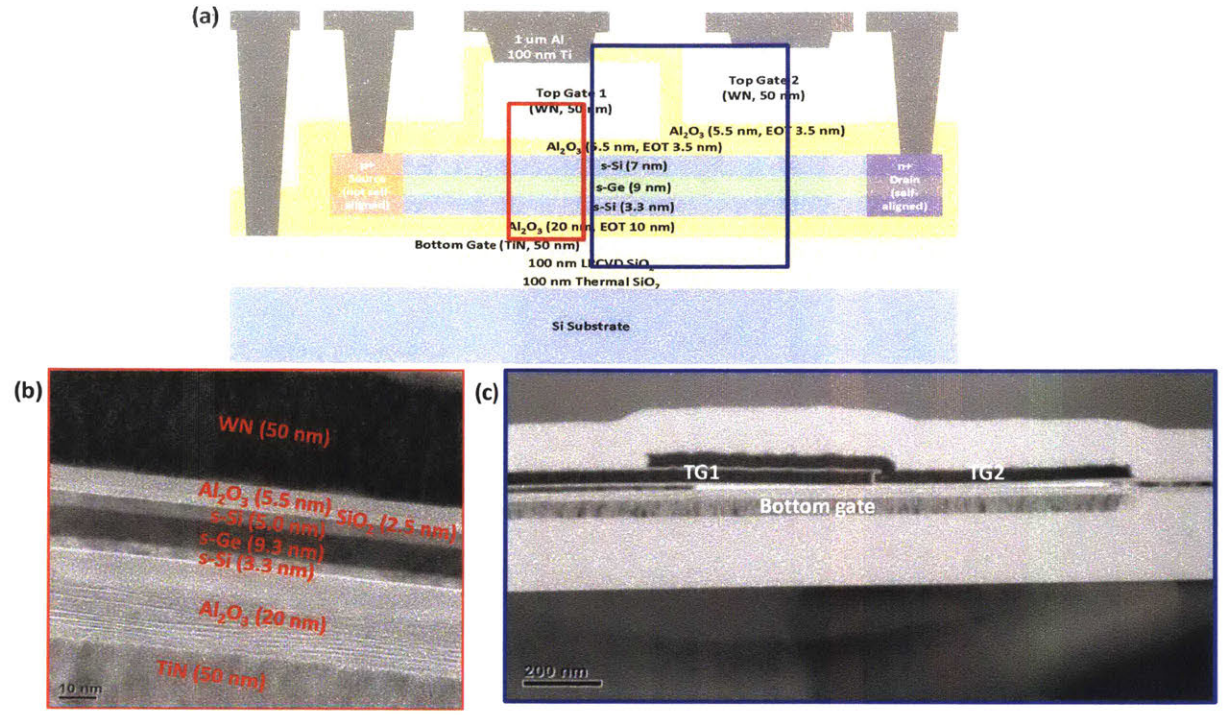


Figure 4.13. (a) Schematic of a 3-gate s-Si/s-Ge bilayer TFET indicating the location of XTEM cuts in (b) and (c). The XTEM in (b) shows that the layer thicknesses of the channel are approximately what was expected. (c) Shows that top gate 2 overlaps top gate 1 like expected and that all of the gates are present and reasonably well aligned. A void formed during etchback exists underneath TG1 and TG2 in c and is not indicative of the majority of the devices in this work.

4.3 TFET Device Characteristics

The 3-gate s-Si/s-Ge bilayer n-TFET is in-principle operated by adjusting the bias of top gate 1 (V_{TG1}). The device when in OFF-state already has a valence band well with accumulated holes at the interface of the s-Ge and the bottom s-Si from a negative bottom gate bias (V_{BG}). Ideally no current flows because the distance between this hole gas and the n-type drain is very large, and no band overlap exists. When the device is switched to ON-state, a positive bias is applied to top gate 1 causing a 2D electron gas to form at the top surface and resulting in a

tunneling conduction path between the electron well and the hole well; this was schematically shown in Fig. 4.5. Based upon the mode of operation, current should increase with increasing V_{TG1}.

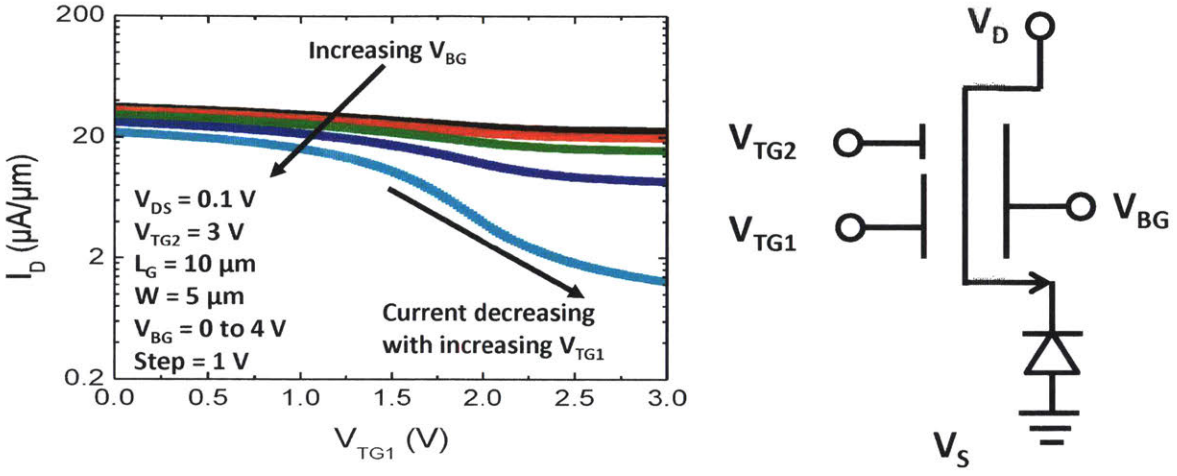
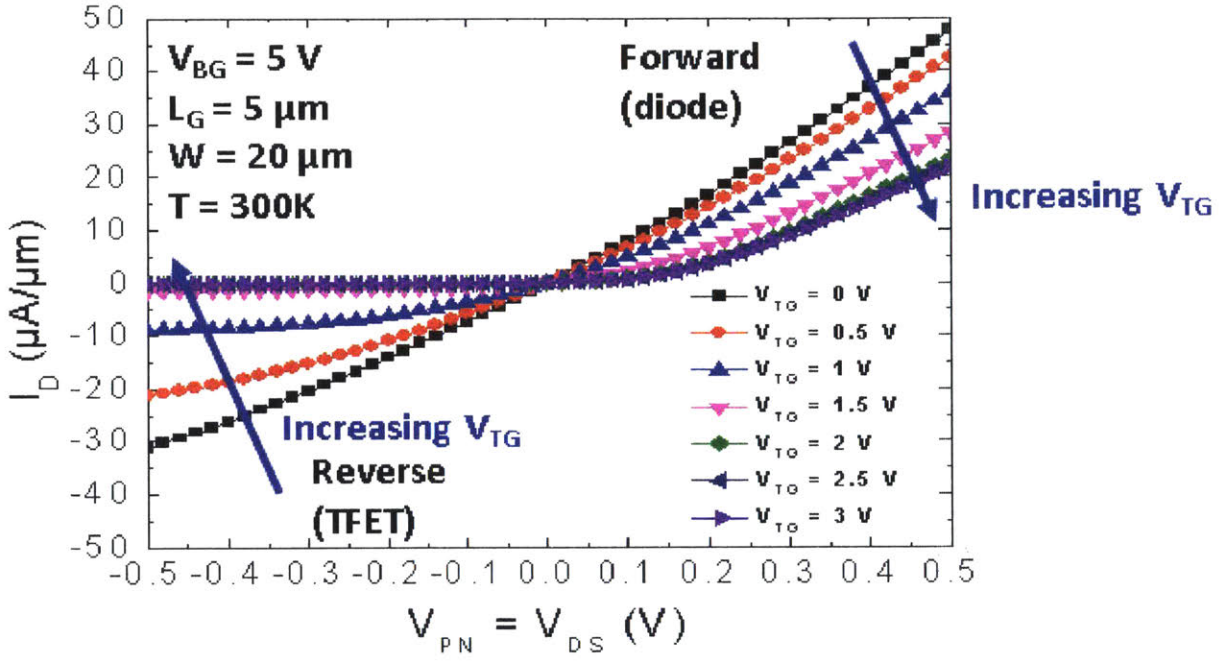


Figure 4.14. Transfer characteristics for a L_G = 10 μm and W = 5 μm 3-gate s-Si/s-Ge bilayer TFET. V_{DS}, and V_{TG2} are held at constant bias, and V_{BG} is varied in the different curves. The intended principle of the bilayer n-TFET operation is represented by the circuit diagram on the right, there are two n-MOSFETs in series with a reverse biased diode. When an electron gas is present in the channel of both n-MOSFETs, the drain voltage is split between the tunnel diode and the n-MOSFETs. When either the n-MOSFETs or tunnel diode are off, no current flows. In the transfer characteristics at V_{BG} = 0 V, little gate modulation exists indicating that the device is likely already on. When V_{BG} and V_{TG} are increased to more positive values, the device turns off indicating the presence of holes in the channel when the device is on and suggesting that the cooperation of two gates is required to deplete the channel of holes. When V_{BG} = 4V, the current decreases with increasing V_{TG1} suggesting that the bilayer tunneling mechanism is not active.

The transfer characteristics are plotted for the 3-gate bilayer n-TFET, Fig. 4.14 for a constant V_{BG} and V_{TG2}; the device characteristics of this device are representative of other 3-gate bilayer TFETs. The output characteristics show: 1.) the top gate modulation is very poor except for large positive values of V_{BG}, and 2.) the current decreases with a more positive V_{TG1} suggesting p-type behavior. The fact that the device is ON and has very poor top gate 1 modulation when $V_{BG} = 0$ V suggests that there is a lot of hole charge in the bottom channel without gate bias, and that a single gate is insufficient to deplete the hole charge in the s-Ge. Hall-measurements found that a sheet charge density of $7x10^{12}$ cm^{-2} holes is present in the nominally undoped and ungated heterostructure and explain why significant positive gate bias is required to deplete the channel. Furthermore, the decrease of current with increasing V_{TG1} suggests that the current is carried by holes which are being depleted with increasing V_{TG1}. Both of these characteristics point to the fact that the bilayer tunneling is not active at room temperature, and instead the device is acting like a p-TFET instead. The 3-gate bilayer n-TFET is not an ideal structure to study this, and instead the 2-gate transverse p-TFET previously shown in Fig. 4.11 will be used to study the transverse p-TFET mechanism in this heterostructure.


V_{BG} = 5 V
L_G = 5 µm
W = 20 µm
T = 300K
Forward
(diode)
Increasing V_{TG}
Increasing V_{TG}
Reverse
(TFET)
V_{TG} = 0 V
V_{TG} = 0.5 V
V_{TG} = 1 V
V_{TG} = 1.5 V
V_{TG} = 2 V
V_{TG} = 2.5 V
V_{TG} = 3 V
I_D (µA/µm)
$V_{PN} = V_{DS}$ (V)

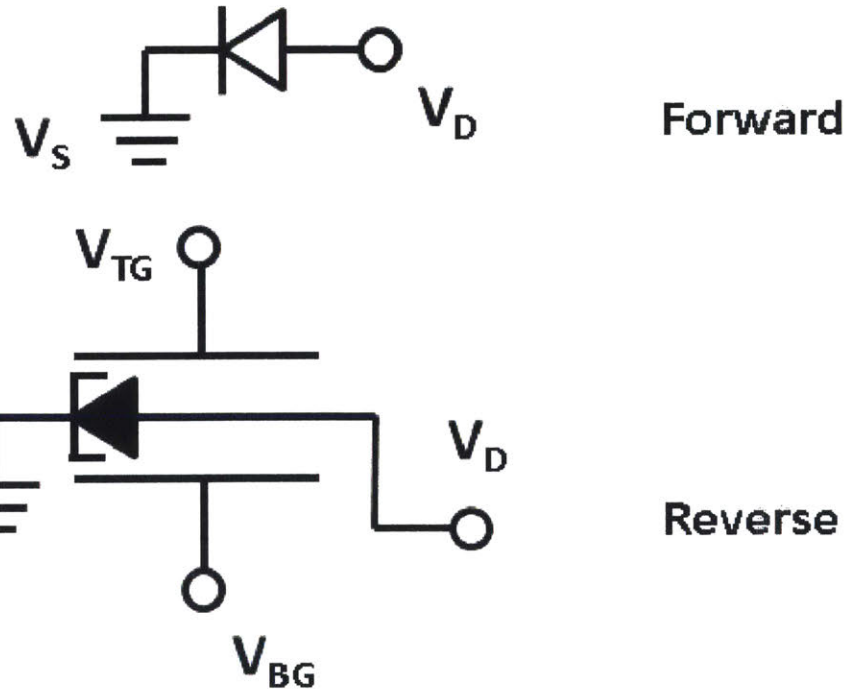

V_S
V_D
Forward
V_{TG}
V_S
V_D
Reverse
V_{BG}

Figure 4.15. Output characteristics for a s-Si/s-Ge transverse p-TFET with L_G = 5 μm and W = 20 μm. For $V_{DS} = V_{PN} > 0$, the device is in the forward diode regime, and super linear diode behavior is observed for all V_{TG}. For $V_{DS} = V_{PN} < 0$, or the reverse regime of the diode (TFET mode), the device can be approximated as a gate controlled tunnel diode in reverse bias in series with a p-MOSFET. When the MOSFET and tunnel diode are on, the characteristics of the MOSFET dominate resulting in velocity saturation and MOSFET-like output characteristics as shown.

The output characteristics of a 2-gate transverse p-TFET are shown in Fig. 4.15 and the tunnel path for the device is shown in Fig. 4.11; the characteristics of this device are representative of other devices with the same architecture. When the $V_{DS} = V_{PN} > 0$V, the TFET is in the forward diode regime, and the device simplifies down to a diode and super linear behavior is observed for all V_{TG}. The rationale is that the gate can only change the length of the depletion region when the diode is forward biased. The minimum current is achieved with increasing V_{TG} because it maximizes the depletion length; a low V_T for the diode is observed which is characteristic of a device with a small effective bandgap, ~180 meV for the s-Si/s-Ge heterostructure. When the $V_{DS} = V_{PN} < 0$ V, the TFET is in the reverse diode or tunneling regime and the circuit diagram is a diode and a p-MOSFET in series. When the p-MOSFET and diode are both on, the voltage is split between the two depending upon which resistance is limiting. The can result in the MOSFET-like behavior that is observed in the output characteristics which shows reasonable saturation similar to [36, 103].

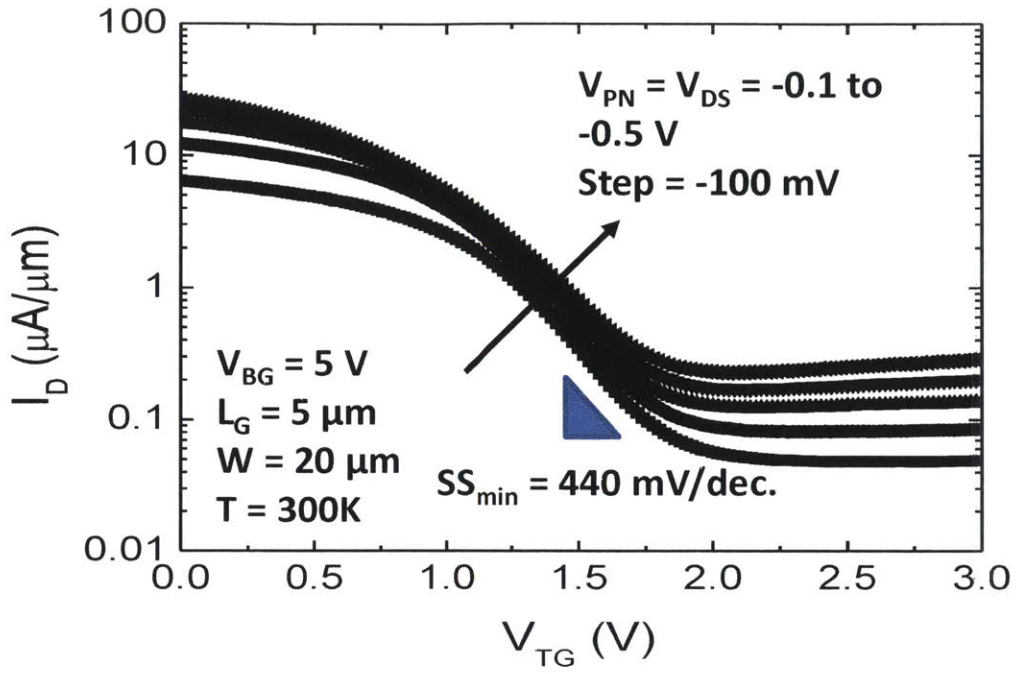


Figure 4.16. The transfer characteristics of a transverse s-Si/s-Ge p-TFET with L_G = 5 μm and W = 20 μm at a constant V_{BG} = 5 V. The minimum SS or SS_{min} = 440 mV/dec. and a DIBL of ~400 mV/V. I_{on} = 25.9 μA/μm as measured at V_{DS} = -0.5 V and V_{TG} = 0 V. Small hysteresis is observed in the transfer characteristics.

The transfer characteristics, Fig 4.16, show both positive and negative attributes. The transfer characteristics show: 1.) high drive currents (25.9 μA/μm at V_{BG} = 5 V, V_{TG} = 0 V, V_{DS} = -0.5 V) which is one of the highest reported among all p-TFETs [34, 49, 104], 2.) an I_{max}/I_{min} ~ 10^2, 3.) high SS ~440 mV/dec., and 4.) high apparent DIBL ~ 400 mV/V; the apparent DIBL in this case is likely caused by the drain dependence of generation in the SS regime which will be discussed later. The high drive current relative to other TFETs is due to the low effective mass of the s-Ge and the low effective bandgap of the s-Si/s-Ge heterojunction. The ratio of I_{max}/I_{min} ~ 10^2 is low, but is a product of the low effective bandgap, 180 meV; an empirical trend shows that lower effective bandgap TFETs have lower I_{max}/I_{min} [34]. The electrostatics parameters, SS and

DIBL are exceptionally high for a long-channel device; the DIBL here is likely influenced by the drain dependent leakage currents in the device and the low I_{max}/I_{min}. The high SS and DIBL are suggestive that the top gate has poor gate efficiency; poor gate efficiency has been observed in previous TFETs [103].

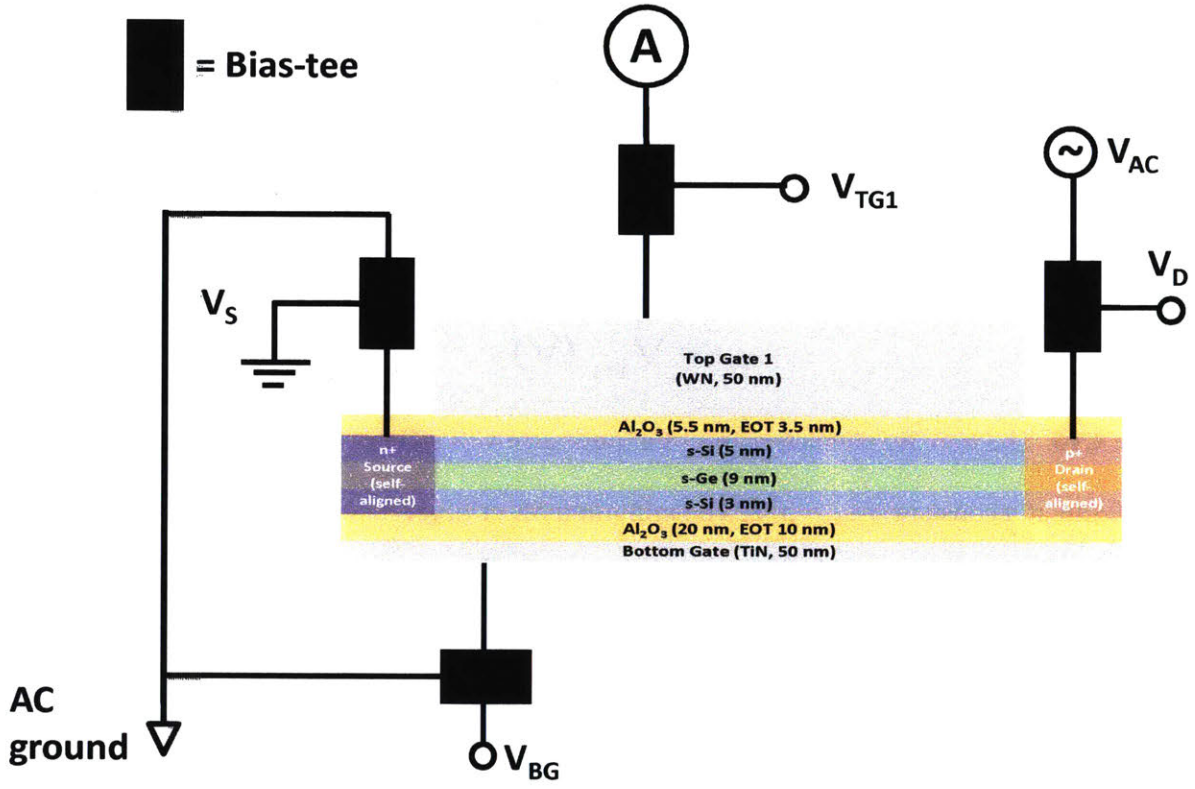


Figure 4.17. C-V measurement setup for C_{GD} as measured from the top gate for a 2-gate transverse p-TFET. A bias-tee consists of an inductor and capacitor which are connected to the DC and AC bias respectively. For the C_{GD} measurement, AC current is applied through the drain, and the resulting AC current is measured out of the top gate. To measure C_{GS}, the AC current is instead applied through the source, and the drain is connected to the AC guard.

The C-V characteristics for the TFETs can be used in order to understand the reasons behind the high current and poor gate control, but require a more complex setup than in a

MOSFET. In a TFET, the total capacitance, C_{GG}, can be measured by applying a DC and AC bias to the gate and grounding the source and drain terminals while measuring the AC current from these terminals. However, unlike a MOSFET the capacitance for different charges cannot be easily differentiated by split C-V. TFET C-V curves require a different setup [103], Fig. 4.17, which require bias-tees. The more complex setup allows for C_{GD} and C_{GS}, or the capacitance associated with the p- and n- wells respectively, to be separately measured. These capacitances are measured at the same time as the current and shifts between the I-V and C-V characteristics are intrinsic to the measurement. The C_{GD} and C_{GS} is measured for the device in saturation and the current for the measurement is overlaid on top of the capacitances, Fig. 4.18.

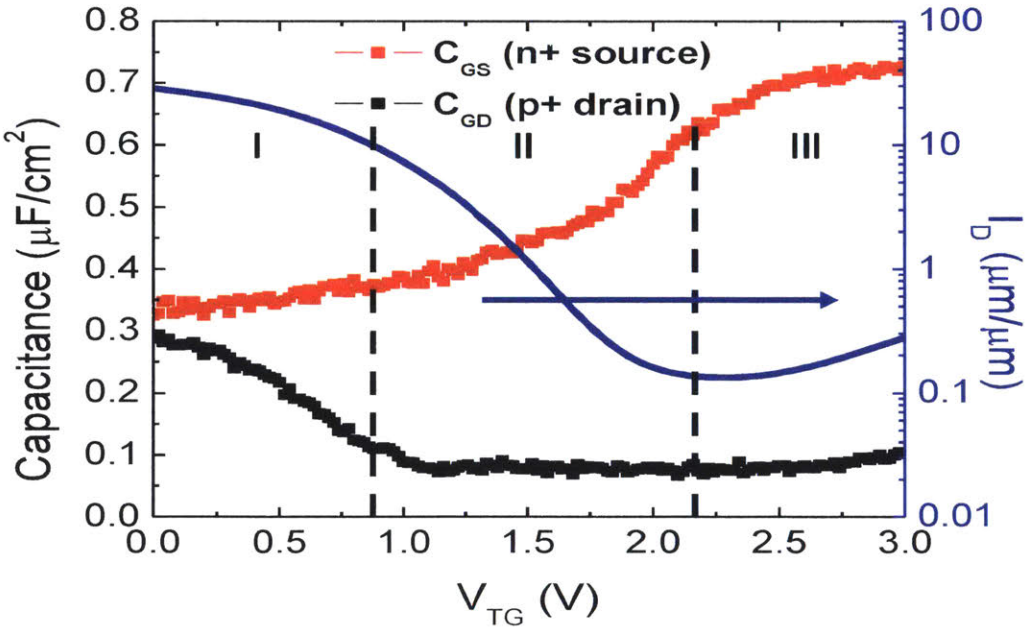


Figure 4.18. C_{GD} (black), C_{GS} (red), and I_D (blue) as a function of V_{TG} for V_{DS} = 0.5 V. Three regimes are marked indicating different charge regimes: ON (I) hole accumulation in the s-Ge, subthreshold (II) depletion of both electrons and holes and OFF (III) electron inversion of the s-Si underneath the top gate.

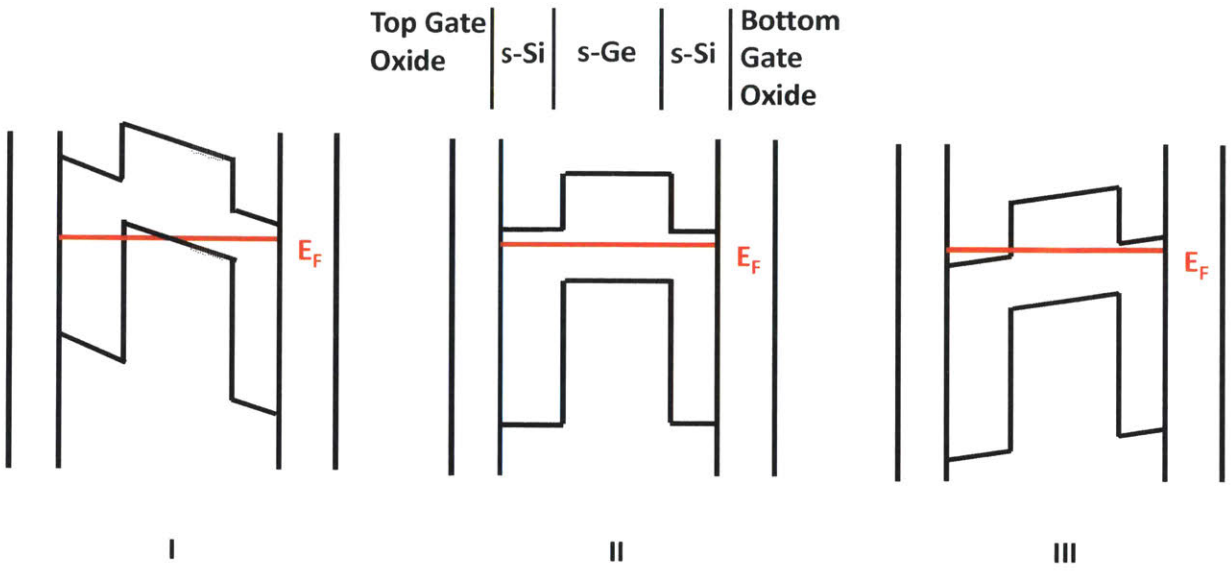


Figure 4.19. Band diagrams for regimes associated with the Fig. 4.17. In regime: (I) the s-Ge is accumulated with holes at the interface between the s-Si and the s-Ge beneath the top gate oxide, (2) the heterojunction is in depletion, and (3) the s-Si beneath the top gate oxide is inverted with electrons.

The capacitances show clearly three different regimes as marked in Fig. 4.18 and the corresponding band diagrams for each regime are shown in Fig. 4.19. Regime I shows hole accumulation, C_{GD} increases with a less positive gate bias, suggesting that the device is on when holes are accumulated in the s-Ge. In regime II, the device is in the subthreshold regime which coincides with little capacitance for C_{GD} and C_{GS} suggesting that the channel is depleted of charge. In regime III or when the device is completely off, there is significant increase in C_{GS}, but not C_{GD} suggesting that the charge in the channel is electrons, most likely in the s-Si cap due to the magnitude of the capacitance. The most important regime to study is the subthreshold regime which happens when the channel is depleted. The observation that the subthreshold regime occurs when the channel is in depletion suggests that some form of generation dominates

the current; the generation mechanism is not known without measuring the temperature dependent I-V characteristics.

This chapter has given an introduction on the different TFET device architectures. S-Si/s-Ge heterostructure TFETs were successfully fabricated in this work and the characteristics of 3-gate bilayer n-TFETs and 2-gate transverse p-TFETs were shown. The 3-gate bilayer n-TFETs were shown to not be operating as intended and the bilayer TFET mechanism is assumed to be the non-dominant current at room temperature. The I-V characteristics of the 2-gate transverse p-TFETs have demonstrated that the device performs as one would expect: as a diode under forward bias, and as a tunnel diode in series with a MOSFET in reverse bias. The capacitance measurements were also taken for these devices showing that in the on-state the s-Ge channel was populated with holes while in the subthreshold regime the channel was in depletion; understanding of the generation mechanisms while the channel is in depletion will take place in the next chapter.

Chapter 5: Analysis of TFET Electrical Characteristics

This chapter analyzes C-V and temperature-dependent I-V characteristics in order to experimentally obtain an understanding of the physics dictating TFET switching. Calculations are compared to the experimental results in order to draw conclusions on the limiting physics for TFETs.

5.1 Gate Efficiency Extraction

Before interpreting the results of the temperature-dependent I-V characteristics, the gate efficiency should be known in order to extract the intrinsic SS. This can be done one of two ways: 1.) by experimentally analyzing C_{GD}-V_{TG} as a function of V_{DS} for the 2-gate transverse s-Si/s-Ge p-TFET structure that was measured in the previous chapter or 2.) by calculating the gate efficiency using a quantum simulator such as nextnano^{TM} [63]. Experimental extraction of the gate efficiency is the preferred method because it does not run into the problem of having to know the correct material parameters or simulations not matching the realities of the experiment.

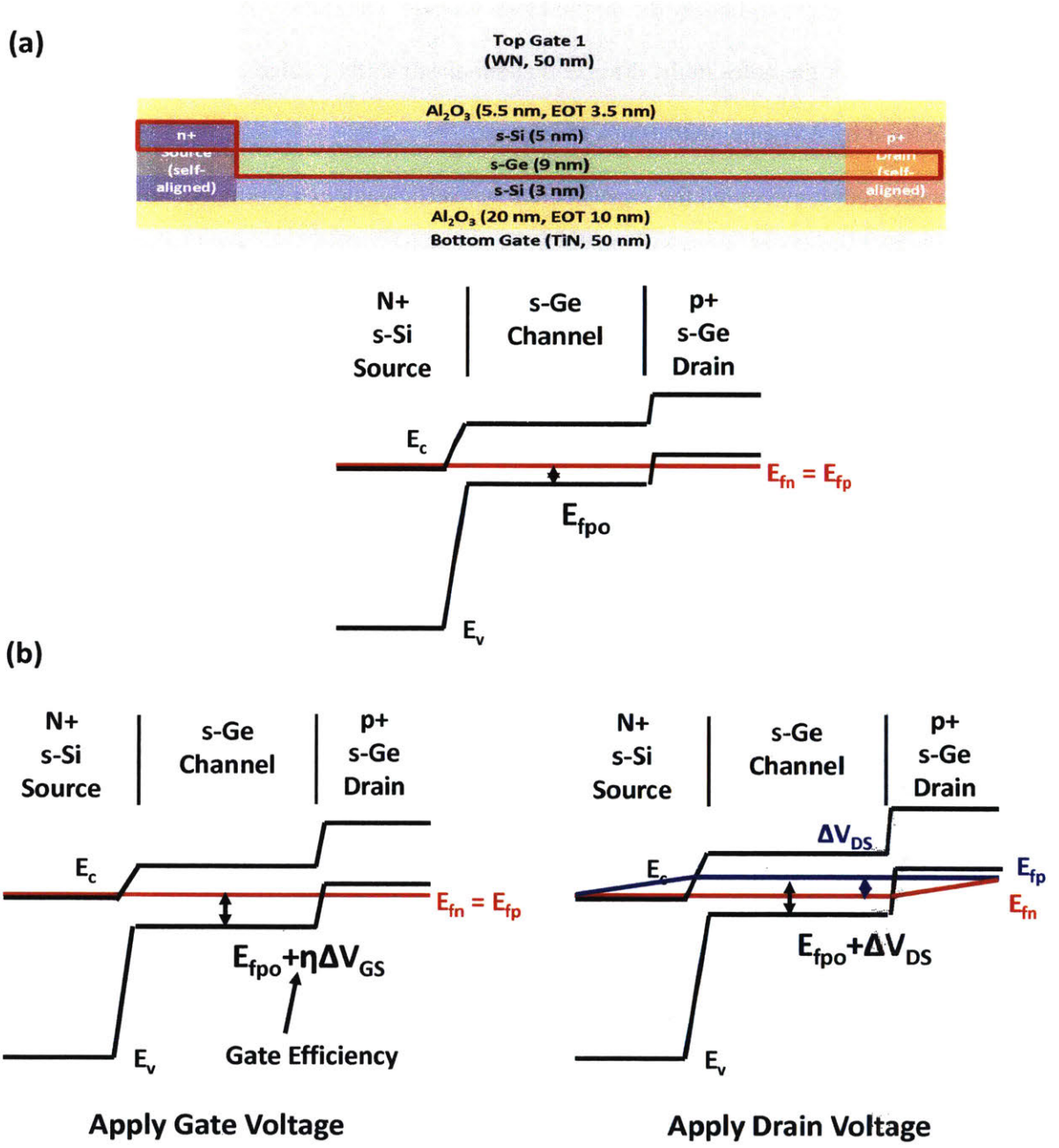


Figure 5.1. (a) Schematic of s-Si/s-Ge transverse p-TFET with the key material regions bordered in red; the band diagram of the key regions when the channel is depleted next to the schematic. (b) The band diagram is varied by changing a gate voltage and a drain voltage. The gate voltage

shifts the conduction and valence band of the channel relative to the drain and source by $\eta\Delta V_{GS}$ or the gate efficiency multiplied by the applied gate voltage. The drain voltage controls the quasi-Fermi level for the holes in the drain and channel and shifts it relative to the conduction and valence band by ΔV_{DS} i.e. with 100% efficiency.

The methodology behind the experimental gate efficiency extraction technique is based upon the fact that the carrier density in the channel, in this case holes, can be controlled by both the drain and the gate voltages, Fig. 5.1. The gate can vary the conduction and valence bands of the channel relative to the quasi-Fermi levels of the source and drain for their respective majority carriers; the amount the conduction and valence bands move is the gate efficiency multiplied by the change in the applied gate bias. The drain causes separation of the quasi-Fermi levels for the different carriers in the channel based upon the amount of applied V_{DS}. In the case of the transverse p-TFET, the drain controls the hole charge in the channel. The efficiency of the drain's control over quasi-Fermi level in the channel is 100% given that the device is a diode and a few assumptions hold: 1.) the current in the channel is low (i.e. the MOS channel is in the subthreshold regime), 2.) the V_{DS} is low so the channel charge is uniform. A constant hole quasi-Fermi level is the same thing as a constant hole charge in the channel which can be observed as a constant gate to drain capacitance, C_{GD}, with the assumption that the shape of the C_{GD}-V_{TG} curve doesn't change with different V_{DS}. When V_{DS} changes by ΔV_{DS}, the C_{GD}-V_{TG} curve is shifted by ΔV_{GS} which yields the gate efficiency, η, defined in Eq. 5.1 and illustrated in Fig. 5.2,:

$$\eta = \frac{\Delta V_{DS}}{\Delta V_{GS}} \tag{5.1}$$

Based upon these measurements, the gate efficiency for the device in the subthreshold regime is approximately 25%. This may seem like a very low number, but the presence of two gates, a thick gate oxide, and the s-Si cap between the top gate oxide and s-Ge serve to reduce the gate

efficiency relative to previously reported values of ~50% [15, 97]. Based upon this analysis, it is clear that the gate efficiency would have to be improved significantly. If the intrinsic SS is ~ 20 mV/decade as people have speculated it to be based upon the Urbach tail, the extrinsic SS would be ~80 mV/decade based upon the extracted gate efficiency which is too high for TFETs to be of interest in digital logic applications.

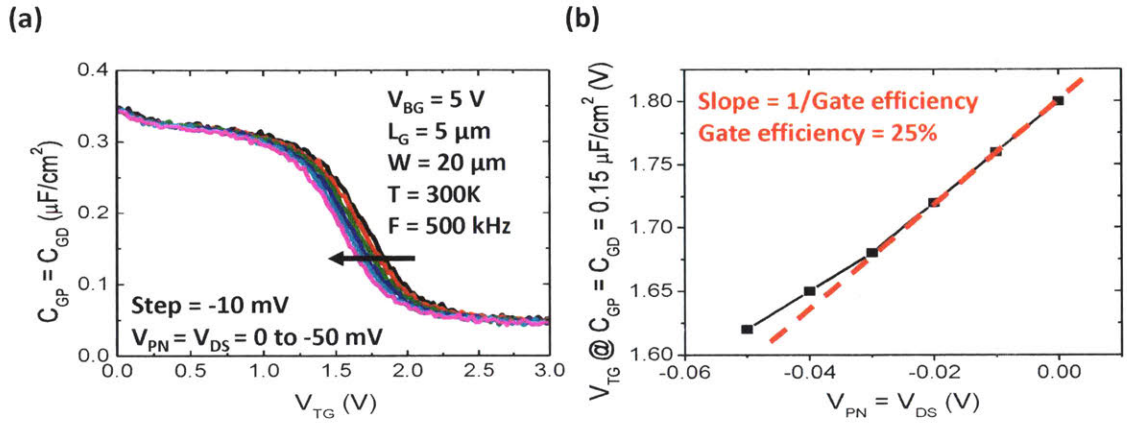


Figure 5.2. (a) C_{GD} vs. V_{TG} for V_{BG} = 5 V for different V_{DS}. (b) The top gate voltage for a constant capacitance, C_{GD} = 0.15 µF/cm^2, in the subthreshold regime is plotted against V_{DS}. The slope of the line is the gate efficiency.

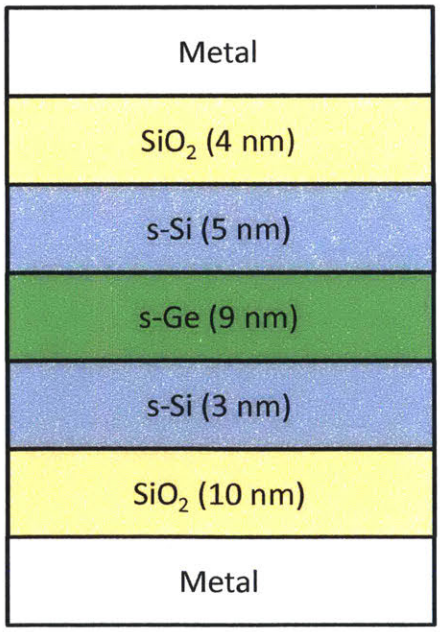


Figure 5.3. The heterostructure used for 1D nextnano^{TM} simulations to extract the gate efficiency of the device.

Quantum simulations were also performed using nextnano^{TM} to corroborate the experimentally extracted gate efficiency using experimentally extracted material parameters from [15, 99]. The methodology is to fit the experimentally measured C-V characteristics of the structure by simulating a 1D device structure based upon the known physical thicknesses of the heterostructure while fitting the gate dielectric thickness; the simulated structure is seen in Fig 5.3. Doping was added in either the s-Si or the s-Ge in order to compensate for the fact that there is approximately $7x10^{12}$ cm^{-2} holes in the channel; this was the density of holes in the channel that was measured through Hall effect measurements. The simulated $C_{electrons}$ and C_{holes}, Fig. 5.4, curves show that the simulated C-V curves are relatively insensitive to where the doping is introduced, in s-Si or s-Ge. C_{GG} or the total top gate capacitance can be created by adding C_{holes} and $C_{electrons}$ together, Fig. 5.5, and both simulated C-V characteristics are fairly similar to the experimentally measured C-V characteristics.

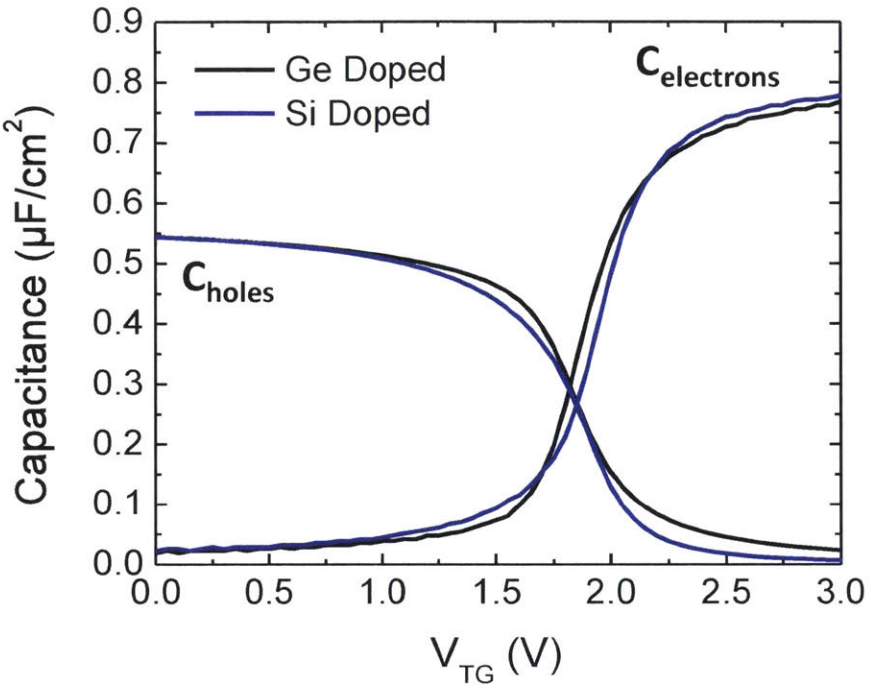


Figure 5.4. Capacitance of holes and electrons for p-type dopants in the s-Si or s-Ge for N_A = $1x10^{19}$ cm^{-3}. The voltage of the curves have been shifted so that they overlay on top of each other and show that the overall shape of the curves are very similar suggesting that this is not a particularly good way of differentiating where dopants are present.

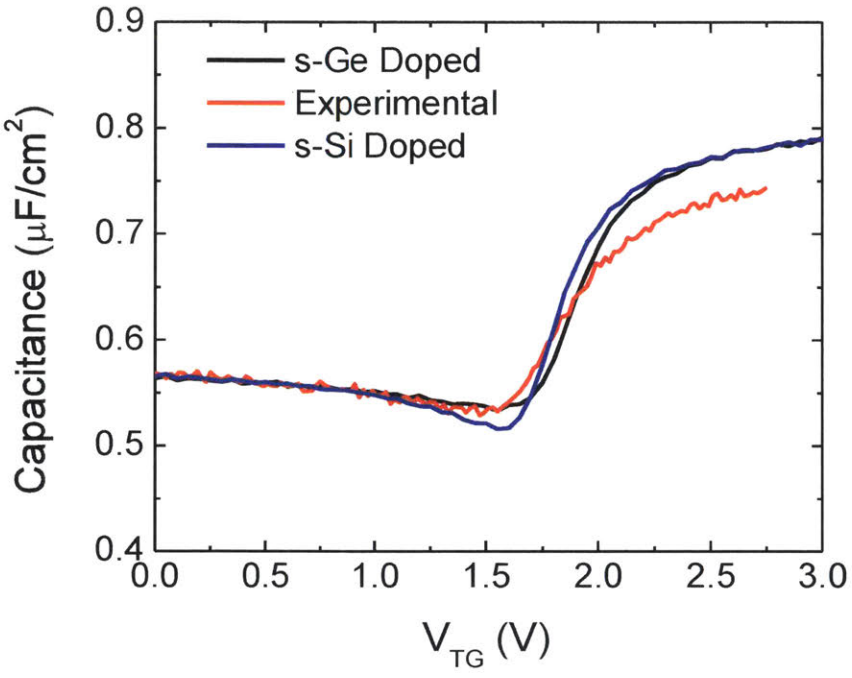


Figure 5.5. Capacitance (C_{GG}) vs. V_{TG} for an experimental TFET compared to simulations with $N_A = 1x10^{19}$ cm^{-3} doping in either the s-Si or the s-Ge. Both match the experimental curve reasonably well although the simulation with doping in the s-Si shows a deeper depletion capacitance dip near $V_{TG} \sim 1.5$ V, than the s-Ge.

The gate efficiency can be extracted based upon the simulations by measuring the change in the surface potential of the s-Ge at the interface of the s-Si directly beneath the top gate oxide relative to the applied top gate voltage. The reasoning behind this figure of merit is that tunneling of holes occurs between the conduction band of the s-Si in the source and the valence band of the s-Ge in the channel where the energy minimum of the s-Ge in the channel is at the interface between the s-Ge and s-Si directly beneath the top gate oxide. The maximum gate efficiencies for the dopant in s-Si and s-Ge, Fig. 5.6, are ~25% and 16% respectively which shows that the gate efficiencies vary dramatically depending upon where the dopants are; the experimentally extracted gate efficiency is in line with the simulated gate efficiency suggesting that the dopants

in the s-Si cap, similar to previous results [67]. One would expect the gate efficiency to be lower if the doping is in the s-Ge because the charge is farther away from the gate which should result in lower gate efficiency. The extracted gate efficiency of 25% will be used to extract the intrinsic SS.

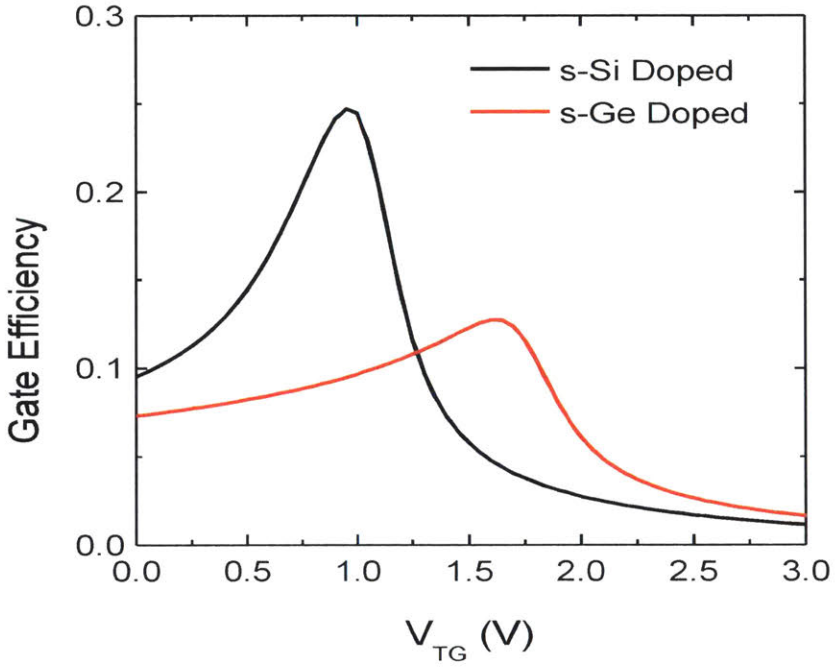


Figure 5.6. Gate efficiency vs. V_{TG} for doping in the s-Si or s-Ge. Gate efficiency is defined by the change in the surface potential of the s-Ge at the point closest to the top gate to the applied gate bias. Despite the small differences in the C-V curves, drastic differences in gate efficiency are calculated.

5.2 Temperature Dependent I-V Characteristics

The temperature dependent I-V characteristics are important to determine the origin of the carrier generation occurring in the subthreshold regime and also the mechanism dominating the transport. The temperature dependent I-V characteristics and the corresponding SS vs. I_D,

Fig. 5.7, show two regimes separated approximately by the threshold voltage. Regime I is when the device is ON and the temperature dependent trend shows increasing current with decreasing temperature. This observation suggests that carrier transport, i.e. the hole mobility, is limiting the ON state current. Because the current is mobility dependent, if the gate length of the device is scaled, higher currents could be obtained and shows promise for higher current TFETs indicating that the low-current problem could have a solution.

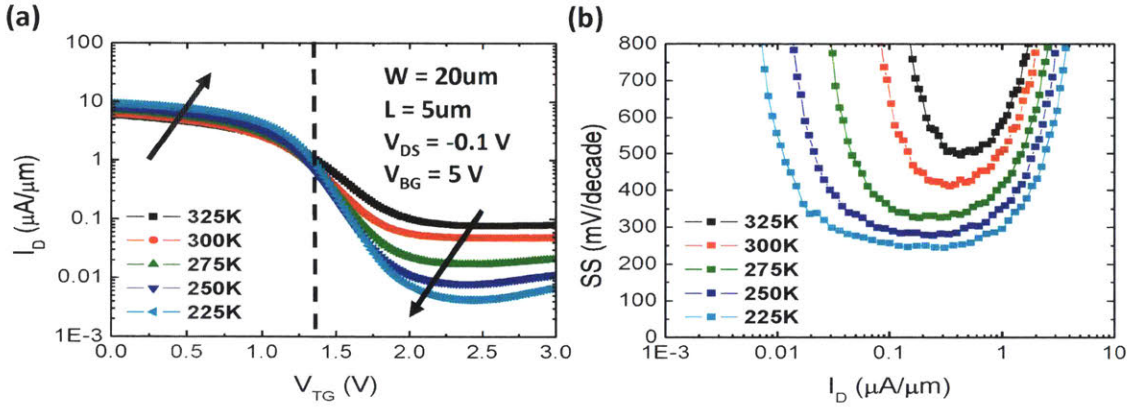


Figure 5.7. (a) Transfer characteristics for V_{DS} = -0.1 V and V_{BG} = 5 V as a function of temperature. Two regimes with different trends are present as differentiated by the dashed line: 1.) The on-state regime where the current increases with decreasing temperature and 2.) the subthreshold and off-state regime where the current decreases with decreasing temperature. (b) SS vs. I_D showing the SS drastically reduces as a function of temperature.

Regime II includes both the subthreshold regime and the OFF state of the device and shows decreasing current and SS for decreasing temperature. The trend of the current and SS with temperature is supportive of a thermally activated current dominating the switching behavior and the minimum attainable current. The SS vs. temperature, Fig 5.8, shows relatively consistent device to device behavior, and a non-linear trend between the minimum value of SS and temperature; this non-linear trend suggests that multiple mechanisms are active.

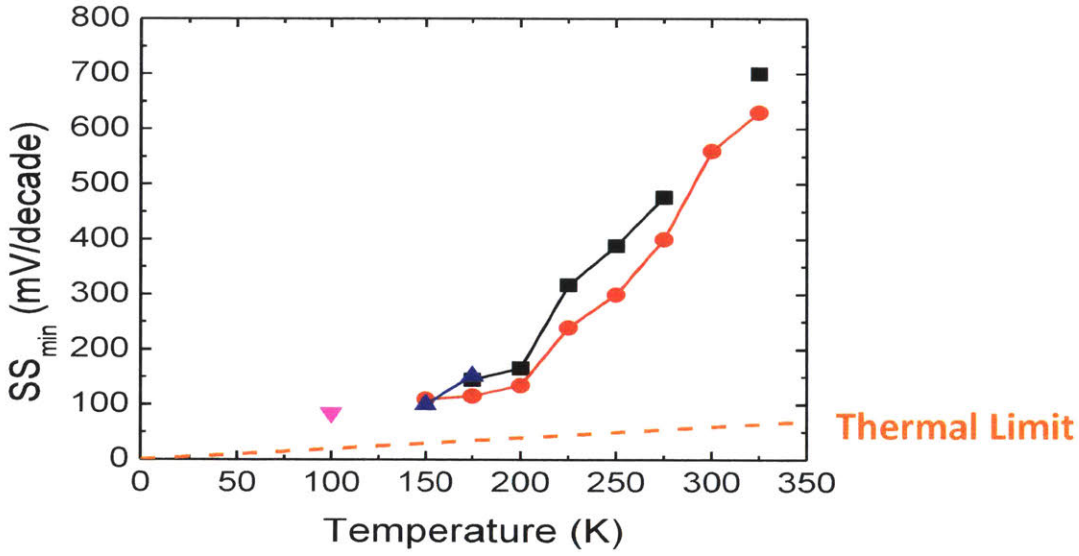


Figure 5.8. SS_{min} vs. temperature for multiple s-Si/s-Ge p-TFETs devices; different symbols indicate different devices. The SS_{min} is higher than the thermal limit at all temperatures and is non-linear as a function of temperature.

The intrinsic SS, Fig. 5.9, is the measured SS divided by the gate efficiency factor and shows two clear regimes that change at T ~ 200 K. Below 200 K, the intrinsic SS vs. temperature follows the thermal limit, but it is not understood why; it could be related to the observation that the ON current is transport limited as well. For T > 200K, the relationship between the SS and temperature has a higher slope, suggesting that another thermally activated mechanism is being frozen out as the temperature is decreased. Examples of such mechanisms are Auger and Shockley-Read-Hall (SRH) generation-recombination. In reverse bias, net generation occurs so the mechanism, Auger or SRH, will be referred to as SRH generation. Auger generation is difficult to quantify [105] and requires high carrier densities with high energy. SRH generation is more easily quantified and also more likely because of the presence of interface traps at high density at the surface of the semiconductor-oxide s-Si/s-Ge TFETs. While both bulk and

semiconductor-semiconductor interface defects would also give current through the SRH mechanism, the semiconductor-oxide interface tends to have a higher density of defect states.

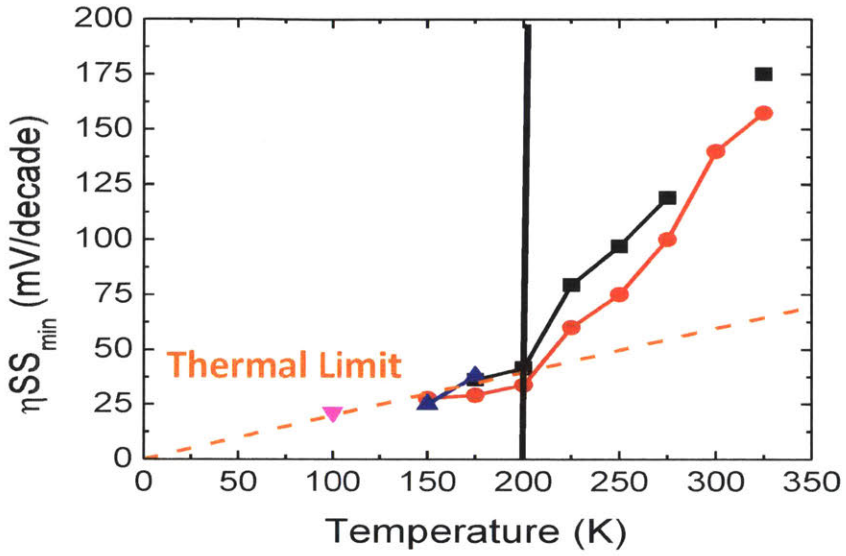


Figure 5.9. The gate efficiency corrected SS_{min} vs. temperature for different s-Si/s-Ge p-TFETs. After the SS_{min} is corrected for gate efficiency, a clear change in the temperature dependence occurs at 200 K. For T > 200 K, the slope of the SS_{min} dependence on temperature is higher than the thermal limit suggesting that a thermally activated mechanism is being frozen out near 200 K. For T < 200 K, the intrinsic SS can be seen; in the case of this p-TFET, the intrinsic SS follows the thermal limit.

5.3 Electric Field Enhanced Shockley-Read-Hall for TFETs

SRH generation is considered to be the dominant mechanism for the reverse bias current in conventional p-n diodes and solar cells [43]. In the basic SRH mechanism, Fig. 5.10, a midgap trap state assists the thermal emission of an electron from the valence band to the conduction band thereby generating an electron hole pair. While this mechanism works well for modeling devices with low electric fields such as p-i-n solar cells, devices with amorphous silicon,

polysilicon, highly doped p-n diodes have significant electric fields which enhances the SRH mechanism [106-108]. The basic difference between electric field enhanced SRH (EFESRH) and low-field SRH models is that tunneling is allowed because of the electric field. It is important to consider the tunneling and thermal emission rates as a single mechanism because they are parallel paths that an electron can take to being emitted into the conduction from the valence band; i.e. an electron can be thermally emitted into the trap state and then tunnel into the conduction band. This model takes into account both mechanisms in a single term.

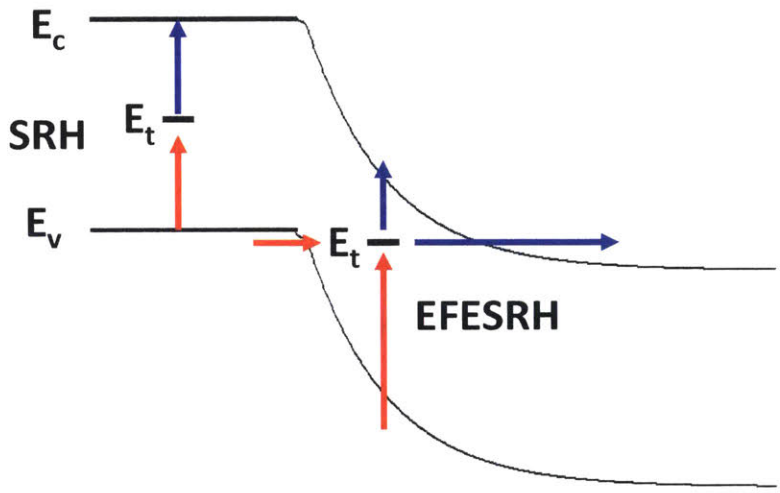


Figure 5.10. A band diagram showing the mechanisms for Shockley-Read-Hall (SRH) and electric field enhanced SRH (EFESRH). In the absence of an electric field, SRH is the active mechanism which consists of an electron being thermally emitted from the valence band to the conduction band with the assistance of a trap state. When an electric field is large, the EFESRH mechanism dominates which consists of an electron being emitted from the valence band to the conduction band assisted by a trap state through either tunneling or thermal emission. The path does not need to consist of only tunneling or thermal emission; for example, the electron can tunnel from the valence band to the trap state and be thermally emitted into the conduction band.

With both SRH and EFESRH a hole is generated when the electron from the valence band is emitted into the trap state.

Mathematically, the generation rate from SRH and EFESRH can be combined in a general formalism, Eq. 5.2 [107].

$$U = G - R = \int \frac{n_i^2 - np}{\frac{\tau_n(p+p_1)}{1+\Gamma_n} + \frac{\tau_p(n+n_1)}{1+\Gamma_p}} D_{it} dE \tag{5.2}$$

Where U is the net generation-recombination rate, G is the generation rate, R is the recombination rate, n_i is the intrinsic carrier concentration, n and p are the electron and hole concentrations at a specific position in the channel, τ_n and τ_p are the minority carrier lifetimes for electrons and holes, n_1 and p_1 are the electron and hole concentrations due to the thermal excitation of carriers from the trap states, $(1+\Gamma_n)$ and $(1+\Gamma_p)$ are the electric field enhancement factors for electrons and holes, D_{it} is the density of interface states and E is energy. If the electric field is non-existent, the electric enhancement factor terms, $1+\Gamma$, go to 1 and Eq. 5.2 converges with the standard SRH formalism.

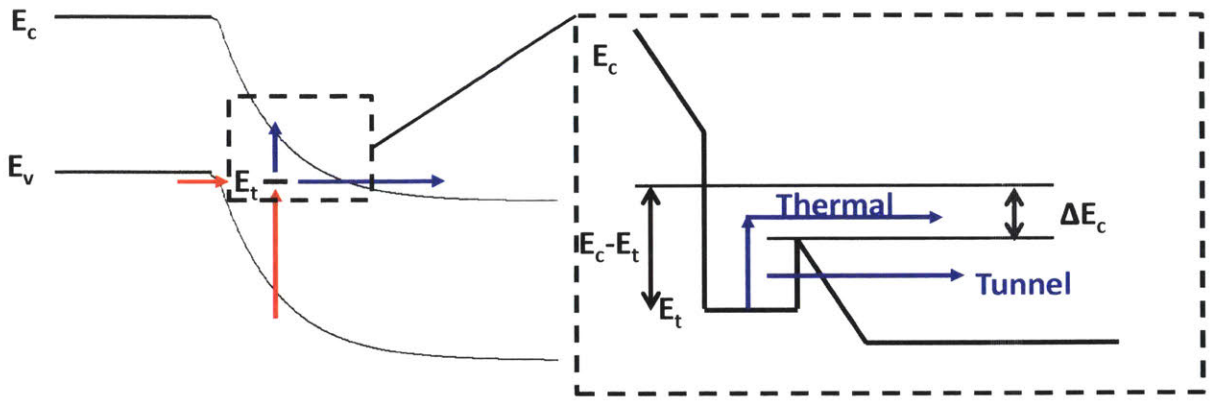


Figure 5.11. Schematic of the different mechanisms for EFESRH focusing on electron emission from the trap state. The difference between the trap energy and the conduction band, $E_c - E_t$, is modified by ΔE_c or the reduction in the barrier height due to the Poole-Frenkel effect. The reduced barrier height is now the barrier height for both tunneling and thermal emission. The same mechanisms are present for the generation of holes, but are done relative to the valence band instead of the conduction band.

The mechanisms present in the electric field enhancement terms are 1.) Poole-Frenkel effect and 2.) tunneling, and are illustrated in Fig. 5.11. The Poole-Frenkel effect is a phenomenon where the electric field causes a reduction in the potential barrier height of a trap-state [107, 109]; this reduction is due to the fact that the trap-state has a finite cross-section resulting in lower barrier on one side of the trap. Tunneling from the trap-state is also possible, and the tunneling barrier height and width is impacted by the presence of the electric field. The electric field enhancement for a given electric field considering both the Poole-Frenkel and tunneling effects is several orders of magnitude higher than if only the tunneling was considered, Fig 5.12. The impact of electric field enhancement is very significant on the generation rates, several orders of magnitude larger in the TFET operation regime, than calculated for plain SRH.

Generation due to EFESRH is the basis behind the calculations in [110] which give the direction for understanding how to reduce the parasitic currents in TFETs.

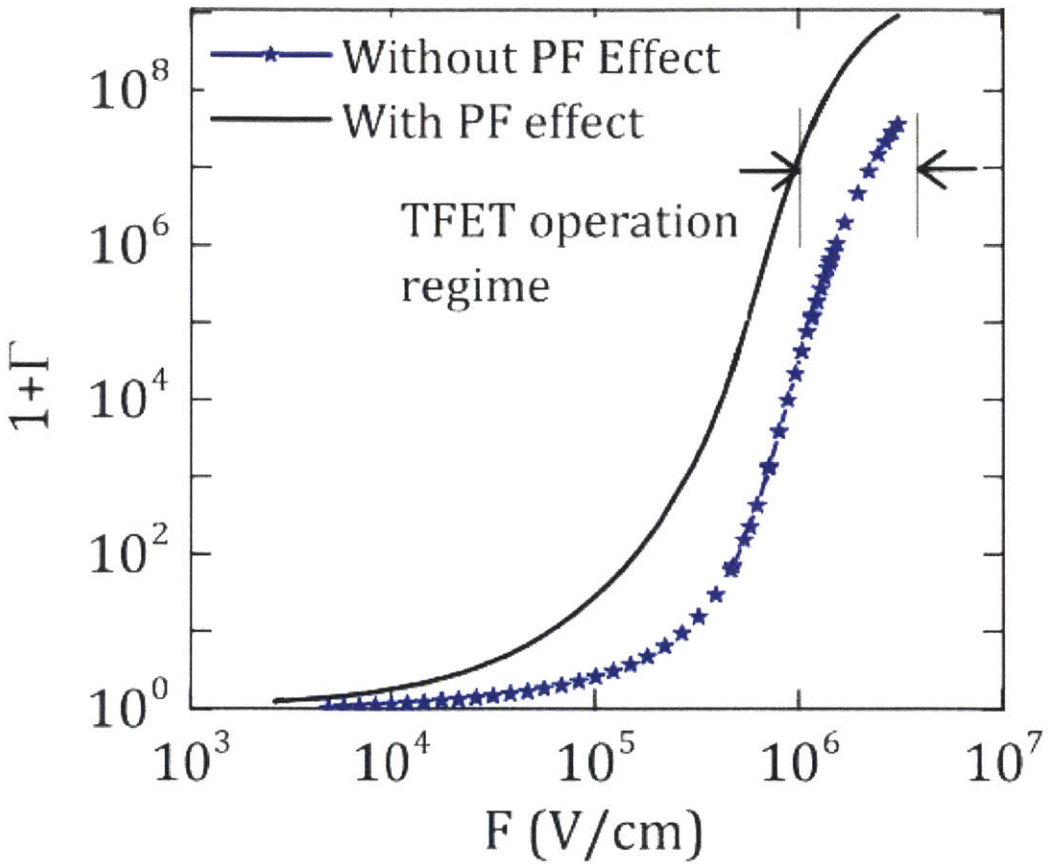


Figure 5.12. The electric field enhancement factor, 1+Γ, vs. electric field, F, with and without the Poole-Frenkel (PF) effect. The Poole-Frenkel effect greatly enhances 1+Γ by a few orders of magnitude, for a given electric field, within the operating range of the TFET. Figure reproduced from [110].

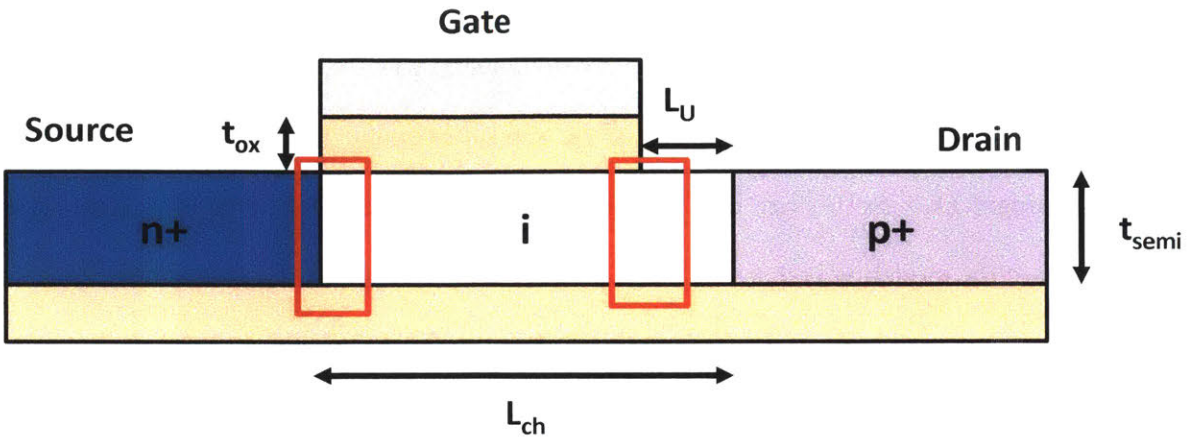


Figure 5.13. Schematic of a simplified homojunction p-TFET structure used for calculating the EFESRH and tunneling currents. The heterostructure is simplified into a homostructure with a bandgap of 0.22 eV for the sake of simplicity in calculations. The semiconductor thickness, t_{semi}, and oxide thickness are varied in this work, and the channel length, L_{ch}, and the gate-drain underlap, L_U, are fixed at 100 nm and 10 nm. The highlighted areas are spatially the important regions to control traps as these regions have high electric fields and large band-bending resulting in high EFESRH currents. Figure reproduced from [110].

Rather than use the complicated s-Si/s-Ge/s-Si heterostructure for modeling, a homojunction TFET, Fig. 5.13, with a bandgap of 0.22 eV was used to understand the basic trends for EFESRH; the material parameters for the homostructure are approximately those of the heterostructure but are capable of showing the physics behind the experimental results. The bandgap of 0.22 eV was used to approximately reproduce the trend in the experimentally measured minimum current as a function of temperature. An optimized mode can be found in [110] which shows similar trends on a different material system, $In_{0.53}Ga_{0.47}As$. The benefit of using a faux material with a bandgap of 0.22 eV is that the structure can be simplified for calculating the band diagram. The simulated structure is a p-TFET with an underlap between the

gate and drain to reduce the ambipolarity of the device; the ambipolarity is intrinsic for the heterostructure. The assumptions in the model are that the top gate oxide interface states dominate the EFESRH current and the effect of the trap states on the gate efficiency is not minimal; a midgap $D_{it} = 5x10^{10}$ $cm^{-2}eV^{-1}$ would have limited impact on the gate efficiency. The methodology of the modeling is that first the electrostatics are calculated for the device. The EFESRH generation rate and interband tunneling or band-to-band-tunneling (BTBT) current are then calculated as a function of position based upon the previously calculated electrostatics. To get the current from EFESRH generation rate, the generation rate is integrated over length of the channel to get the normalized current, Eq. 5.3.

$$\frac{I_D}{W} = q \int U(x)dx \tag{5.3}$$

Where I_D is the drain current, W is the width of the device, q is the elementary charge, U(x) is the net generation-recombination rate as a function of position. The current from EFESRH and the BTBT, Eq. 5.4, are added together and the result as a function of temperature can be found in Fig. 5.14.

$$J_{wkb} = aV_{TW}\left(\frac{F}{F_0}\right)^P \exp(-\frac{B}{F}) \tag{5.4}$$

Where a, F_0, P, and B are material parameters, F is the electric field and V_{TW} is the tunnel window, i.e., the energy difference between the valence band in the source and the conduction in the channel [110]. The off-state current is set by the EFESRH current, and depending upon the temperature the SS may or may not be impacted by the EFESRH current. For high temperatures, T > 300K, the subthreshold current is affected by EFESRH, and for the lower temperatures, T< 200K, the minimum SS is not impacted by the generation current from traps, showing the intrinsic SS. This is consistent with the temperature dependence that was found in s-Si/s-Ge heterostructure p-TFETs and this suggests that the model is a valid test-bed to vary certain

parameters that are possible to vary experimentally in a predictable way such as the interface trap density, the electrostatic scaling length and intrinsic SS.

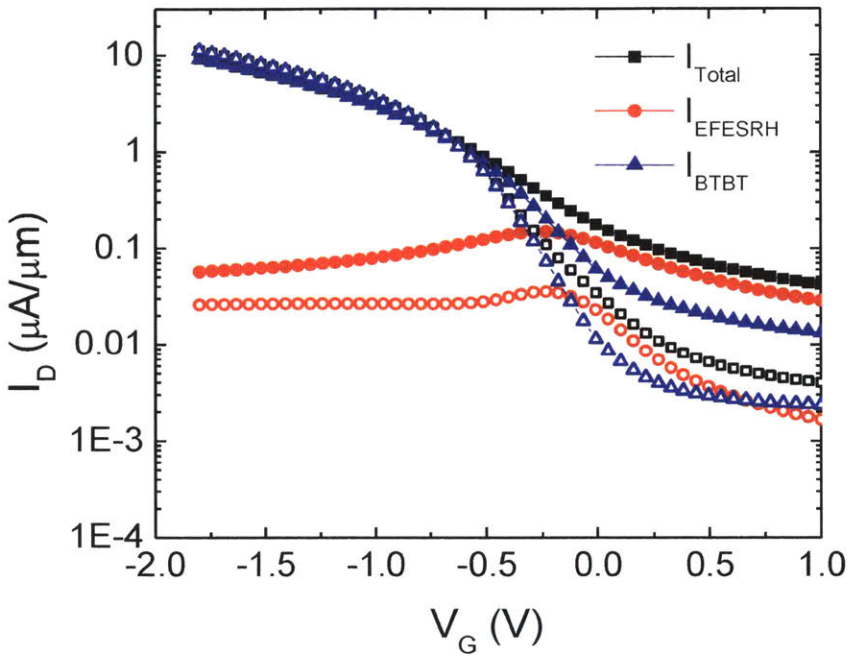


Figure 5.14. Total (EFESRH + BTBT) current in the simulated homojunction TFET for temperatures of 300 K (closed) and 200 K (open) with the device structure, as shown in Fig. 5.13 with a t_{ox} and t_{semi} of 4 and 105 nm respectively, and V_{DS} = -0.1 V. The gate efficiency penalty of 25% is included in these calculations. The BTBT current follows the WKB formalism above threshold (when the bands overlap), while below threshold, the BTBT has an exponentially decaying transmission. EFESRH is temperature-dependent and obscures the steepest part of the BTBT current in the subthreshold regime (~V_G < -0.3 V) for temperatures above 200 K. The energetic distribution of traps is a constant midgap $D_{it} \sim 1x10^{10} cm^{-2}eV^{-1}$. We find that the midgap traps dominate the net generation rate.

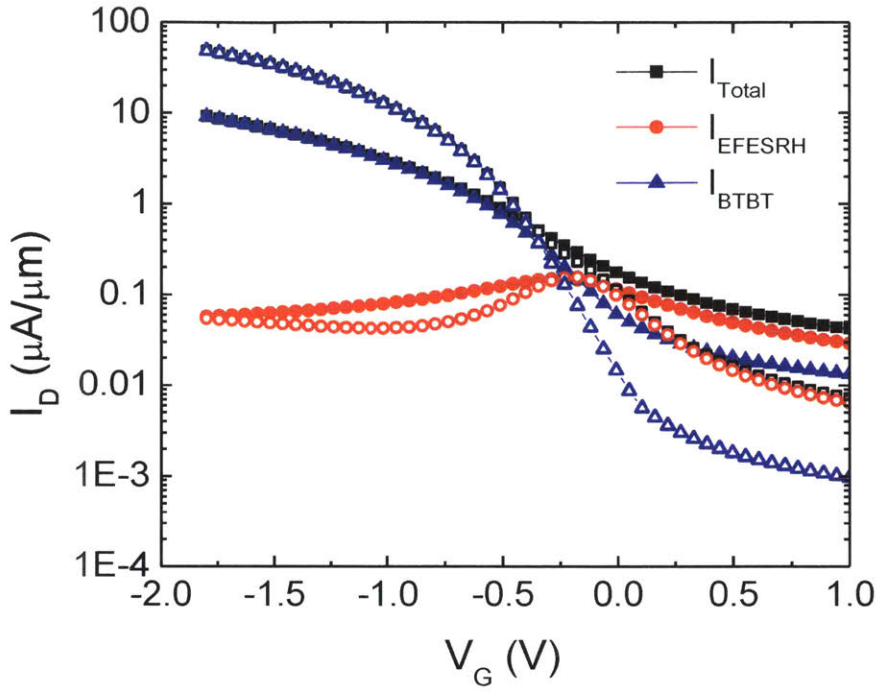


Figure 5.15. Since both EFESRH and BTBT are electric-field dependent the thickness of the oxide and semiconductor affect the current levels as well as the SS. In this calculation, the thicknesses of the semiconductor and oxide (from top to bottom) results in decreasing electrostatic scaling lengths which increases the electric field at the edges of the channel resulting in enhanced electric field dependent currents. t_{ox} is 4 (closed) and 1 (open) nm and t_{semi} is 10 (closed), and 5 (open) nm, respectively. Even for very thin oxide and body thicknesses, EFESRH is large enough to overshadow the steep change of BTBT current.

The most prevalent and convenient strategy to dealing with interface trap problems in CMOS [53, 64] is reducing the effective oxide thickness by reducing the physical oxide thickness. This strategy improves the gate efficiency through the capacitive divider between the capacitance of the interface traps and the gate oxide for MOSFETs. For a TFET, it improves the gate efficiency in the way that it would for a MOSFET (not captured in this model), but it also

affects both the tunneling and the EFESRH current because the electric field between the source and channel increases [111-113]. The figure of merit used to evaluate the gate control over the channel is the electrostatic scaling length, λ, which is the characteristic length at which a potential exponentially decays into the channel; the expression for λ for a thin body semiconductor on insulator can be seen in Eq. 5.5. If the λ is shorter, the potential decays faster and the electric field is higher resulting in increases in both the tunneling and EFESRH current.

$$\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} t_s} \tag{5.5}$$

Here ε_s and ε_{ox} is the dielectric constant for the semiconductor and gate oxide respectively, t_s and t_{ox} is the thickness of the semiconductor and gate oxide respectively. λ can be practically changed by decreasing the thicknesses of either the gate oxide or semiconductor and the impact of changing the electrostatic scaling length on the current is shown in Fig. 5.15. When the electrostatic scaling length is decreased by decreasing either the semiconductor body or gate oxide thicknesses, the current increases for all gate voltages. If λ is large to begin with, reducing λ shows a significant improvement in the transfer characteristics; the SS decreases and the overall I_{max}/I_{min} increases. However, when λ is already scaled, the SS and I_{max}/I_{min} do not improve because the increase in the EFESRH current is similar to that of the interband tunneling current and the EFESRH current still obscures the intrinsic SS resulting in SS larger than 60 mV/decade at room temperature. The results of this model is in line with the observation that many papers have shown reduction in the SS by decreasing the gate oxide and body thickness, but have rarely shown SS below 60 mV/dec. at room temperature for reasonable current densities [36].

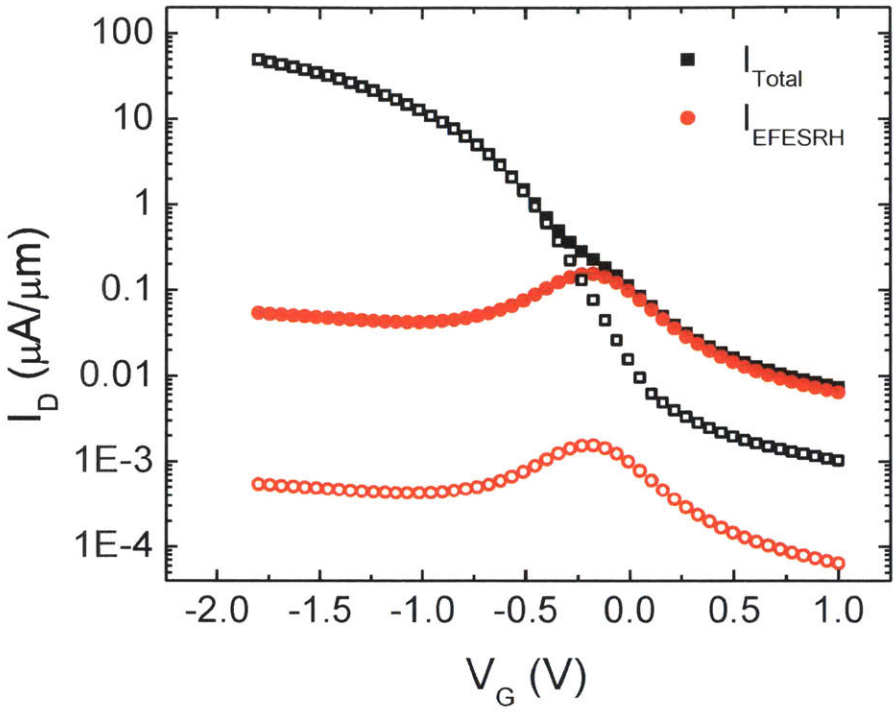


Figure 5.16. Impact of the magnitude of D_{it} on the transfer characteristics for t_{ox} = 1 nm and t_{semi} = 5 nm with two different levels of D_{it}, $1x10^{10}$ $cm^{-2}eV^{-1}$ (closed) and $1x10^{8}cm^{-2}eV^{-1}$ (open). For Dit = 10^{8} $cm^{-2}eV^{-1}$, the EFESRH current is low enough for the steep BTBT current to be manifested.

The more difficult method of reducing the EFESRH current is to simply reduce the D_{it} by improving the passivation technology for different materials; this will also improve the gate efficiency, not shown here. Based upon Eq. 5.2, the generation rate hence current is linearly proportional to the D_{it}. Figure 5.16 shows the impact of reducing the D_{it} on the transfer characteristics for the modeled TFET from the original value of $5x10^{12}$ $cm^{-2}eV^{-1}$ to $5x10^{10}$ $cm^{-2}eV^{-1}$ at the midgap. The effect of reducing the D_{it} is the reduction of the EFESRH current which determines how much of the intrinsic SS can be observed in the transfer characteristics. Based upon this calculation, a few orders of magnitude, at least 100x, reduction in the D_{it} is necessary

to observe around 2 orders of magnitude of the intrinsic SS at room temperature. If the off-state current requirements are lower to reduce the static power, the midgap trap density will need to be further lowered based upon those requirements.

The last methodology is to reduce the intrinsic SS in order to get a steeper external SS. It is obvious if the intrinsic SS of the device can be engineered, the overall SS will be improved. Regardless of the change in the intrinsic SS, the EFESRH current does not change and limits both the off-state current which will likely limit the steepness in the measured SS. A study on what limits the intrinsic SS will need to be performed in order to understand whether or not this is something that can be improved.

5.4 Summary of TFET Results

This chapter has looked at TFETs through the lens of both experiments and calculations and has three main conclusions: 1.) The on-current for s-Si/s-Ge TFETs could potentially be high because the current in the experimental TFETs was relatively high and transport limited, 2.) The gate efficiency for the experimental TFET was ~25% and will need to be improved for practical TFETs, and 3.) the EFESRH generation current dominates the off-state and covers-up the intrinsic SS at room temperature. The first conclusion is conditional upon the heterostructure used in the future depending upon the effective bandgap and mass or other reasons which would cause the on-current to be dominated by the tunneling current. However, the other two conclusions are reasons why TFETs have not been able to exhibit the goal of SS < 60 mV/dec. at room temperature. The gate efficiency must be good enough for the extrinsic SS to be steeper than the 60 mV/decade of a MOSFET. This challenge has been previous reported in [103]. Furthermore, the conclusion that EFESRH dominates TFETs explains why most researchers have not been able to observe SS < 60 mV/dec. at room temperature, namely that generally the

interface trap density is not specifically optimized. This conclusion unfortunately means that the arduous task of reducing interface trap density will need to be accomplished before TFETs can be a practical device for future CMOS applications.

Chapter 6: Conclusions and Future Work

This thesis has presented two different approaches in the quest to reduce the power dissipation for digital logic circuits and has evaluated the ability of these approaches to achieve the desired goal: 1.) use Ge or strained-Ge as a high mobility channel material for p-MOSFETs and 2.) change the MOSFET device architecture to a tunnel FET to reduce the SS. Both of these approaches have significant challenges to achieving the goal which were identified.

As with any channel material, Ge and strained-Ge p-MOSFET are required to meet a certain I_{on} for a given supply voltage, V_{DD}, and I_{off}, and with certain a device footprint. The first requirement can be split into four other requirements: 1.) to obtain a certain mobility or velocity for a certain amount of charge or a given CET, 2.) having a reasonable SS, 3.) being able to have the correct threshold voltage and 4.) being able to meet the I_{off} requirement. Ge and s-Ge was found to be able to have a higher hole mobility than Si for a given CET. While the SS for Ge and s-Ge was higher than Si, it was found that improvement in the density of interface traps would serve to improve this number. The threshold voltage for short gate length Ge devices is too positive, but improving the defect states could improve this. The main problem that was identified with even unstrained Ge, looking at previously published data, is its ability to achieve the desired I_{off} due to the reduced bandgap of Ge relative to Si.

Based upon the high I_{off}, Ge will be an unlikely candidate for future p-MOSFET logic devices. The geometry can be taken one step further to a gate-all-around geometry to increase the bandgap through quantum confinement. Another alternative is instead of using Ge or strained Ge as a channel material, SiGe could be used as a channel material instead. This would allow some of the benefits of Ge, having a higher hole mobility hence carrier velocity relative to Si, but also have a higher bandgap.

Tunnel FETs were explored using both experiments and calculations. The two main problems that TFETs face are the low on-state current and the inability to achieve steeper than 60 mV/decade SS at room temperature. S-Si/s-Ge heterostructure TFETs were used to experimentally look at the physics limiting the steep SS for TFETs. Originally, the experiment was planned around 3-gate bilayer s-Si/s-Ge n-TFETs, but it turned out that another mechanism was dominant over the bilayer tunneling mechanism at room temperature. As a result, transverse 2-gate s-Si/s-Ge p-TFETs were used to look at the tunneling behavior through I-V, C-V and temperature dependent I-V measurements. Calculations using a homostructure TFET with a faux material of a similar bandgap, $E_G = 0.22$ eV, were correlated to the experimental temperature dependent I-V measurements and used to extrapolate the results. The results of this experiment showed that 1.) the on-state current is temperature dependent hence transport limited, 2.) the current in the subthreshold regime is dominated by generation current, 3.) the gate efficiency is very poor ~25% and needs to be improved and 4.) the temperature dependence shows the SS can be intrinsic or extrinsic depending upon the temperature. Calculations corroborated the temperature dependent trend for the experiment and were used to identify that for $T > 200$ K electric field enhanced SRH generation dominates the minimum-current and influences the SS and for $T < 200$ K the SS is the intrinsic SS.

The main positive of this experiment was that the on current was temperature dependent meaning that the tunneling resistance was not dominating the on current. This suggests that higher current TFETs may be possible in this materials system, although it is uncertain what this high current is.

Several negatives for the TFET were found in the experiment which will need to be improved for practical use of TFETs as a MOSFET replacement. The first is that the gate

efficiency is poor at 25%. The low gate efficiency has been previously reported [103], but is also due to the presence of the bottom gate, the buried channel architecture of this device, and thick gate dielectric. TFETs need to be investigated without any of the abovementioned properties and with the gate efficiency taken into account in the TFET design.

The more intrinsic and important problem for TFETs is electric-field-enhanced SRH generation, more commonly referred to as trap-assisted-tunneling (TAT), at $T > 200$ K which increases the minimum attainable current and the SS. The cause of this mechanism is defect states at all of the interfaces between channel materials. The defect states at the interface between the channel material and the gate oxide is of key importance because that region has the highest electric field and the density of interface states is also highest. By using calculations, the impact of electrostatic scaling, interface trap density and the intrinsic SS on the EFESRH current was evaluated. It was found that electrostatic scaling will not be able to improve the SS to much less than 60 mV/decade at room temperature. The calculations found that the EFESRH current is linearly dependent upon the midgap density of interface traps (D_{it}), and that lowering the D_{it} by 100x to $5x10^{8}$ $cm^{-2}eV^{-1}$ would allow the intrinsic SS to be observed for approximately 2 orders of magnitude of current. Therefore, the only method of being able to practically obtain a SS < 60 mV/decade at room temperature would be to lower the D_{it} several orders of magnitude so that the intrinsic SS can be utilized assuming that EFESRH is the dominant mechanism at room temperature. Future work should also include understanding what determines the intrinsic SS to understand what the minimum obtainable SS would be assuming the D_{it} reductions could be achieved in the future.

Appendix A: Process Flow for s-Si/s-Ge TFETs

The process flow to make the s-Si/s-Ge heterostructure TFETs can be separated into two processes, one to fabricate the wafer and another to fabricate devices after wafer fabrication. All fabrication steps are done at MIT unless otherwise noted.

Epitaxial wafers:

Step #	Step	Details	Machine
1	Pre-Epi RCA	10 min. SC-1, 15s HF, 15min. SC-2, 15s HF	RCA/ICL
2	Epitaxial growth	SiGe, Si and Ge	Epi-Centura
3	Bottom gate deposition	300°C 1 minute O_3/243 cycles Al_2O_3/1400 cycles PEALD TiN (TiCl, NH_3 plasma)	Oxford-ALD/ICL
4	Spin PR	Recipe: T1HMDS	Coater6/ICL
5	Expose PR	Reticle: Bilayer TFET Mask 1 Dose: 140 ms, Focus: 0 um	i-stepper/ICL
6	Develop PR	Recipe: PUDDLE3	Coater6/ICL
7	Ash PR	Asher: 3 minutes	Asher/ICL
8	Pre-LTO clean	Nanostrip: 10 minutes	Greenflo/ICL
8	LTO deposition	Immediate transfer, using dedicated cage, ~500 nm **Note: HfO_2 will be buried after this step**	6C-LTO/ICL
9	LTO anneal	Immediate anneal (550C, 30min.) to densify oxide	A1/TRL
10	Ellipsometry	Thickness measurement	UV1280/ICL

11	LTO planarization	Outside vendor – To remove the cross-hatch	Entrepix
12	Post-CMP clean	Double Piranha – Check wafers after double piranha for pinholes (reject wafers if pinhole is present)	Premetal-Piranha/ICL
13	Ellipsometry	Thickness measurement	UV1280/ICL

Handle wafers and bonding:

Step #	Step	Details	Machine
1	RCA clean	Standard RCA	RCA/ICL
2	Oxidation	Tox=100nm after dry oxidation	5C/ICL
3	Dry surface activation (Both wafers)	Recipe: iaberg-O2, 20s, chamber A	AME5000/ICL
4	Wet surface activation	3 min. Piranha to prevent the piranha from attacking too much of the wafer in case of pinholes in the oxide.	Acidhood-2/TRL
5	Wafer bonding (SDB)	note: no bond chamber	EV620/TRL
6	Post-bond anneal	300C for 5 hours	A1/TRL
7	Wafer Grinding and CMP	Outside vendor	SQI
8	Wafer clean	Double Piranha	Premetal-

			Piranha/ICL
9	Backside protection	Oxide deposition – 2um of oxide deposited with 4 separate depositions of 0.5um at a time.	DCVD/ICL
10	TMAH etch	~10 hrs. until the cross-hatch of the graded buffer layer is visible by eye. It is important to rinse the cassette thoroughly after 50:1 HF removal of the native SiO_2 to prevent salt formation.	TMAH/ICL
11	SiGe etch	1:2:3 $HF:H_2O_2:CH_3COOH$ - 2hours after mixing should be waited for the etch rate to become stable. Etching should be ~15-20 minutes until the entire wafer color stabilizes. The etch rate of the s-Si is ~1nm/min.	Acidhood2/TRL
12	TMAH dip	Remove etch stop 10s. TMAH temperature should be 80C, and the wafer can be removed once the color stabilizes.	Acidhood2/TRL
13	SiGe etch	1:2:3 $HF:H_2O_2:CH_3COOH$ 15s. The wafer should be removed	Acidhood2/TRL

		immediately after the color stabilizes.	
14	Ellipsometry	Thickness measurement	UV1280/ICL

Device Fabrication:

Step #	Step	Details	Machine
1	Spin PR	Recipe: T1HMDS	Coater6/ICL
2	Expose PR	Pattern Alignment verniers to rotate wafer Dose: 140 ms, Focus: 0 um Orthoganlity: +70 urad, wafer rotation: -70 urad	i-stepper/ICL
3	Develop PR	Recipe: PUDDLE3	Coater6/ICL
4	Etch alignment marks	Recipe: Baseline-ox New, 5s O_2 descum	AME5000/ICL
5	Ash PR	Asher: 2 minutes	Asher/ICL
6	Spin PR	Recipe: T1HMDS	Coater6/ICL
7	Expose PR	Pattern Mesa Dose: 140 ms, Focus: 0 um	i-stepper/ICL
8	Develop PR	Recipe: PUDDLE3	Coater6/ICL
9	Etch alignment marks	Recipe: Baseline-ox New, 5s O_2 descum	AME5000/ICL

10	Ash PR	Asher: 2 minutes	Asher/ICL
11	Pre-ALD Clean	10 min. 10:1 H_2SO_4:DI, 10 min. 10:1 HCl:DI, 15s 500:1 HF:DI	Greenflo/TRL
12	Top gate 1 ALD	300°C 1 minute O_3/55 cycles Al_2O_3/1400 cycles PEALD WN (NH_3 plasma)	Oxford-ALD/ICL
13	Spin PR	Recipe: T1HMDS	Coater6/ICL
14	Expose PR	Pattern Top Gate 1 Dose: 140 ms, Focus: 0 um	i-stepper/ICL
15	Develop PR	Recipe: PUDDLE3	Coater6/ICL
16	Etch WN	Recipe: Pouya WN etch	Rainbow/ICL
17	Pre-ALD Clean	10 min. Nanostrip	Greenflo/TRL
18	Top gate 2 ALD	300°C 1 minute O_3/55 cycles Al_2O_3/1400 cycles PEALD WN (NH_3 plasma)	Oxford-ALD/ICL
19	Spin PR	Recipe: T1HMDS	Coater6/ICL
20	Expose PR	Pattern Top Gate 2 drain side Dose: 140 ms, Focus: 0 um	i-stepper/ICL
21	Develop PR	Recipe: PUDDLE3	Coater6/ICL
22	Etch WN	Recipe: Pouya WN etch	Rainbow/ICL
22	Phosphorus Implantation	Ion implant Phosphorus, Energy: 10 keV, Dose: $2x10^{15}$ cm^{-2}	Innovion

23	Ash PR	Asher: 4 min.	Asher/ICL
24	Spin PR	Recipe: T1HMDS	Coater6/ICL
25	Expose PR	Pattern Top Gate 2 remainder Dose: 140 ms, Focus: 0 um	i-stepper/ICL
26	Develop PR	Recipe: PUDDLE3	Coater6/ICL
27	Etch WN	Recipe: Pouya WN etch	Rainbow/ICL
28	Ash PR	Asher: 2 min.	Asher/ICL
29	Spin PR	Recipe: T1HMDS	Coater6/ICL
30	Expose PR	Pattern Source Implant Dose: 140 ms, Focus: 0 um	i-stepper/ICL
31	Develop PR	Recipe: PUDDLE3	Coater6/ICL
32	Boron Implantation	Ion implant Boron, Energy: 5 keV, Dose: $2x10^{15}$ cm^{-2}	Innovion
33	Ash PR	Asher: 4 min.	Asher/ICL
34	Pre-ALD Clean	10 min. Nanostrip	Greenflo/TRL
35	ILD Deposition	PECVD 220 nm SiO_2 Recipe: CH A: 2k SiO_2	DCVD/ICL
36	S/D Activation Anneal	30 minutes, 500 °C	A3-Sinter/TRL
37	Spin PR	Recipe: T1HMDS	Coater6/ICL
38	Expose PR	Pattern Vias Dose: 140 ms, Focus: 0 um	i-stepper/ICL

39	Develop PR	Recipe: PUDDLE3	Coater6/ICL
40	Etch Vias	Timed Etch leave 25 nm SiO_2 Recipe: Baseline-ox New, 5s O_2 descum	AME5000/ICL
41	Ash PR	Asher: 2 min.	Asher/ICL
42	Premetal Clean	10 minutes Green Piranha, 50:1 HF timed over-etch 20%	Premetal-piranha/ICL
43	Metal Deposition	100 nm Ti/1 μm Al Recipe: Cait Ti/Al	Endura/ICL
44	Spin PR	Recipe: T1HMDS	Coater6/ICL
45	Expose PR	Pattern Metal Pads Dose: 140 ms, Focus: 0 um	i-stepper/ICL
46	Develop PR	Recipe: PUDDLE3	Coater6/ICL
47	Etch Metal	Recipe: Pouya metal etch Ti Al Manual endpoint	Rainbow/ICL
48	Ash PR	Asher: 4 min.	Asher/ICL
49	Sinter Anneal	Forming gas 95% N_2/5% H_2 30 minutes, 400 °C	A3-Sinter/TRL

Appendix B: Fabrication Challenges for s-Si/s-Ge Bilayer TFETs

The fabrication of the s-Si/s-Ge Bilayer TFETs were not without its challenges which are documented in this section. The challenges that were seen in this work are: 1.) etchback voids, 2.) strain relaxation as measured by Raman spectroscopy in the s-Ge, 3.) pattern skew after the bond and etchback process and 4.) film delamination during the source drain activation anneal.

Etchback voids were previously observed in [62] and have also been observed in the current experiments. The etchback void is a void in the s-Ge layer caused by etching of the s-Ge in the Acetic:H_2O_2:HF etch step where the solution seeps through pinhole defects in the s-Si layer. The resulting defect is a crystal orientation dependent defect shown in Fig. C.1 which was shown previously in [62]. The method of avoiding pinhole defects relies on reducing the defect selective etching characteristics of the acetic:H_2O_2:HF etching solution which can be done by reducing the HF concentration [114]; this was done by diluting the HF solution by a factor of 3. The result is a longer etch time and a wafer without bonding defects.

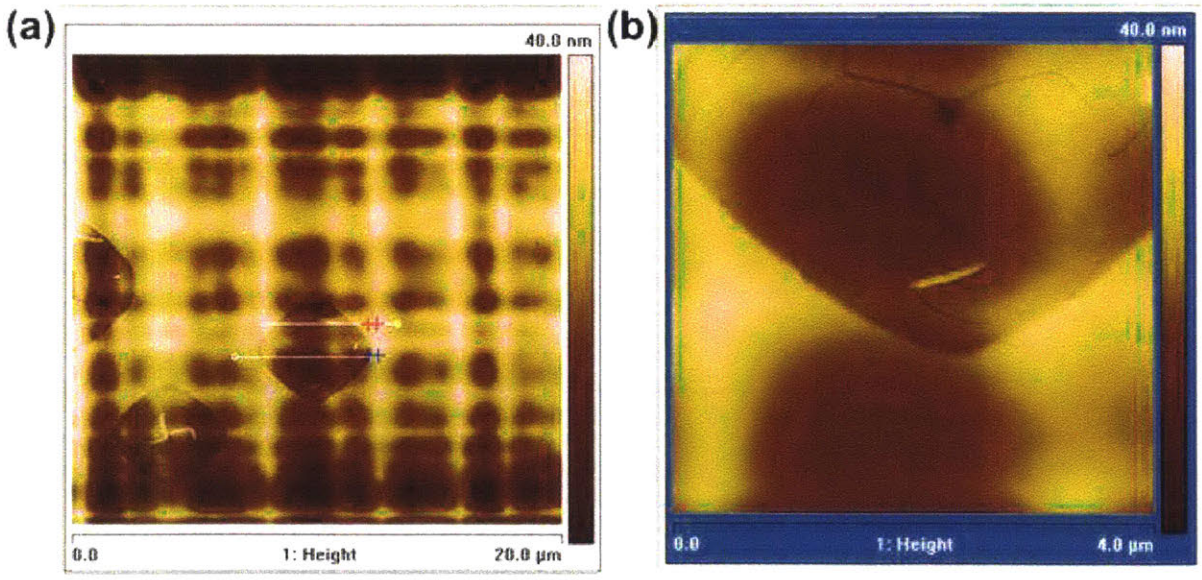


Figure C.1. (a), (b) AFM images of the microscopic (~5 μm) defects caused by the final Acetic:H_2O_2:HF etch step. The <110> cross-hatch is in the x and y directions of the image, and the defects are 45 degrees relative to the x-axis. This suggests that the defects propagate in the <100> directions from a pinhole defect in the s-Si film.

Another problem in the fabrication is related to the strain state in the s-Ge layer before and after the bond and etchback, Fig. C.2. The Raman spectra show that there is significant shift in the Ge-Ge Raman peak after the bond and etchback process; the implied biaxial compressive strain based upon the Ge-Ge Raman peak is 2.5% to 1.7% after wafer fabrication. The apparent strain relaxation is limited to the Ge-Ge peak. The Si-Si peak corresponds to a biaxial tensile strain of ~1.7% which is approximately what the strain should be as-grown. It is uncertain why there is strain relaxation only in the s-Ge layer, but it could be due to strain relaxation or inter-diffusion between the s-Si and s-Ge during the densification anneal after the LPCVD oxide deposition on the epitaxial, sacrificial wafer [101].

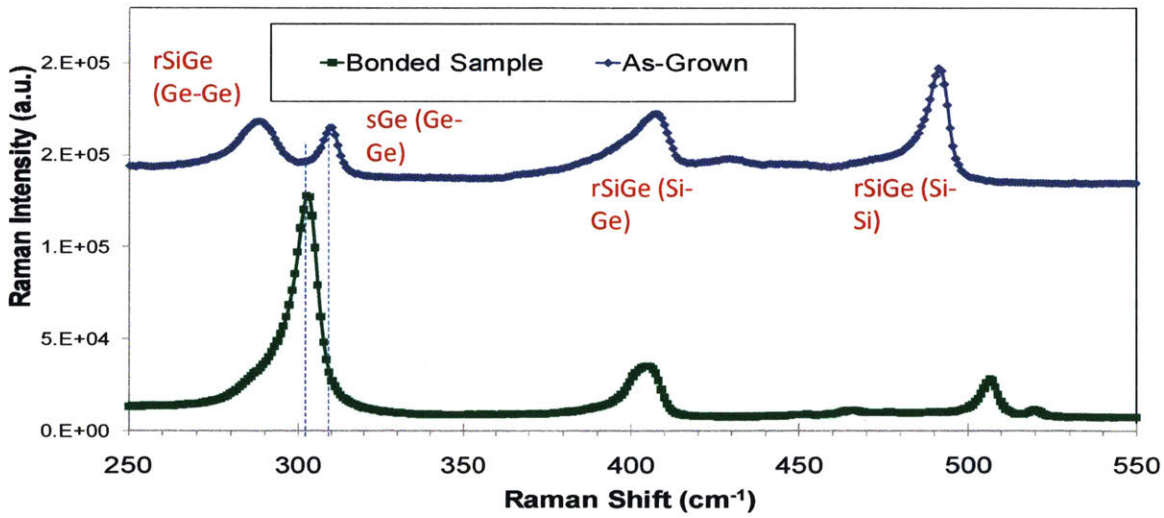


Figure C.2. Raman spectra of the s-Si/s-Ge/s-Si heterostructure as-grown (blue) and after bond and etchback (green). The Ge-Ge peak of the s-Ge shifts from 309.8 to 302 cm^{-1} after etchback. Raman spectroscopy was done by Pouya Hashemi.

Pattern skew after wafer bond and etchback was a major problem for the alignment of subsequent mask layers to the bottom gate. The meaning of pattern skew is that the die is not exactly rectangular, but instead a parallelogram, Fig. C.3; the spatial difference between the alignment at the top and bottom of the 1x1 cm die is 2.7 μm. The non-rectangular die means that there is no way that any subsequent mask levels can be overlaid to the bottom gate by any die rotation or wafer rotation meaning misalignment all subsequent layers will be present relative to the bottom gate. The alignment tolerance for the process was 1 μm in both the x and y directions, and the solution was to rotate the overlaid die putting misalignment in both the x and y directions. The 2.7 μm misalignment was spread out over both the x and y axes resulting in up to a 0.8 μm misalignment in both axes, within the designed tolerance of the mask.

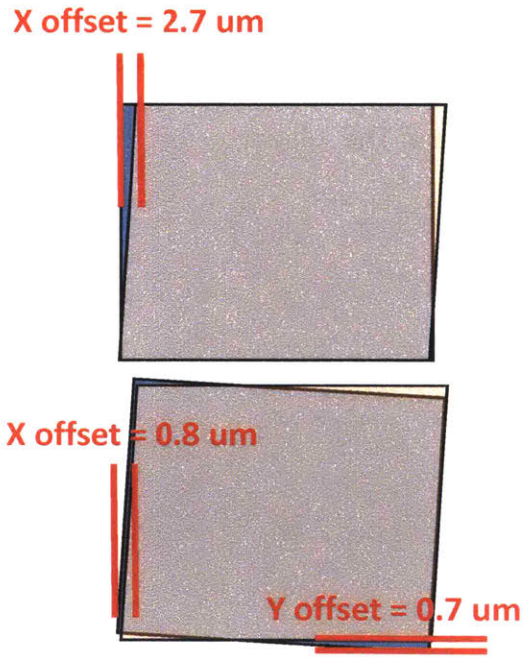


Figure C.3. Schematic of an expected square die (blue), and a parallelogram (orange) representative of the skewed die is overlaid on top of the square die showing the 2.7 μm of misalignment if the x axis is aligned properly. After the square pattern of the mask is rotated, the pattern misalignment is shared between the x and y axes resulting in a misalignment below the designed tolerance for both axes.

The origin of the pattern skew is unfortunately not known and the possibilities include the asymmetric strain relaxation of the semiconductor wafer after etchback or skew in the original mask writing. The asymmetric strain relaxation of the film could be due to the way the transfer of stress from the sacrificial wafer to the handle wafer. The modulus of elasticity is different for the <100> and <110> directions in Si resulting in different amounts of strain for each direction. If this is the problem, then the skew will be intrinsic to strained wafers and the lithographic tolerance should be increased in order to make the alignment easier. Another possible reason why the pattern skew could exist is based upon how the mask is written. It is possible that the mask originally is a parallelogram because of stage drift during the mask writing process. When the pattern is mirrored during the bond and etchback process this skew will also be mirrored resulting in a mirrored parallelogram. The solution to this reason is to write the mask in the reverse order in the future.

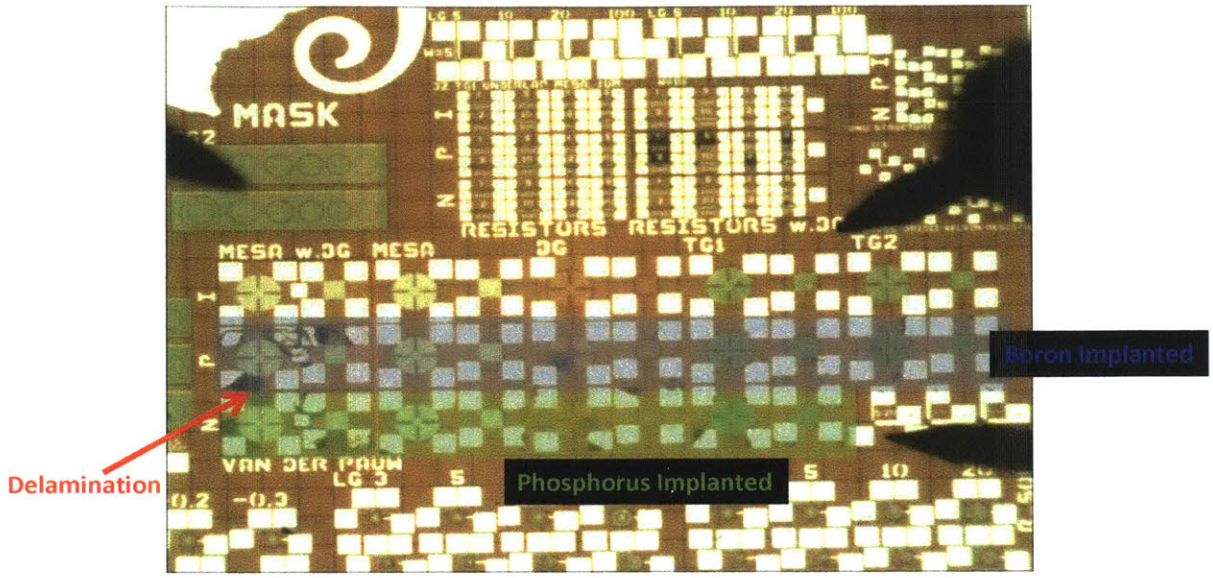


Figure C.4 Microscope image of the fully processed wafer with overlays of boron and phosphorus implanted regions. Film delamination appears under the microscope as a darker feature and, based upon this microscope image, instances of delamination are predominantly found where an ion implant has occurred.

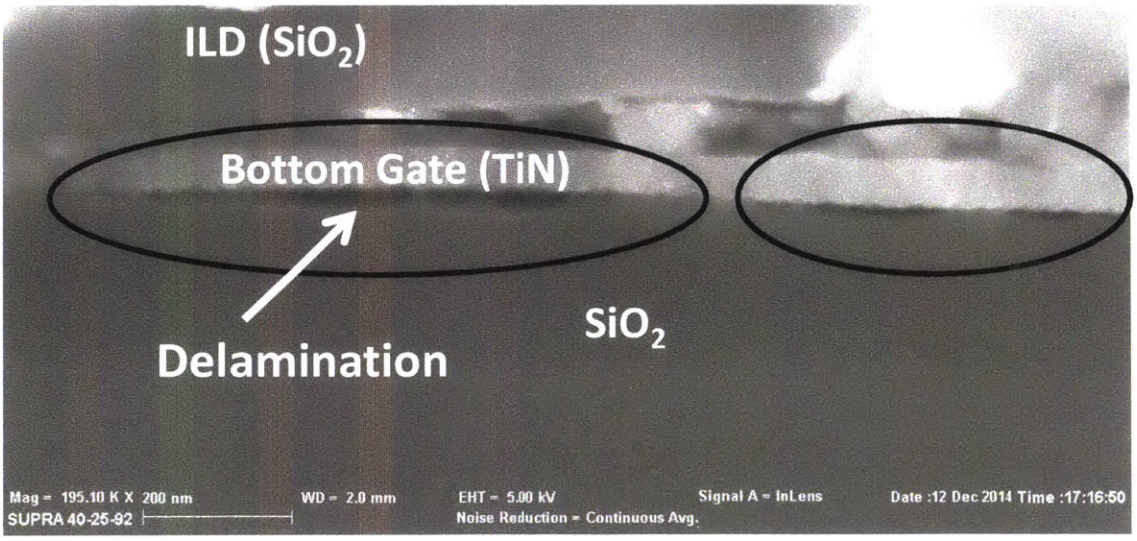


Figure C.5. Cross-section SEM of the bottom gate covered by the ILD showing delamination between the bottom gate, TiN, and the buried oxide layer SiO_2. Delamination of the TiN occurs at multiple points between the bottom gate and SiO_2 as indicated by the two circled regions.

Delamination of the film during the S/D activation anneal was the final major problem encountered in the process. While there were still measurable devices after fabrication, the delamination greatly reduced the yield in the process resulting in the need to look for working devices; the delamination is likely due to a combination of the thermal stresses from the many films that are present on the semiconductor and damage caused by the ion implantation, Fig. C.4. Based upon the cross-section SEM, Fig. C.5, of a previously fabricated s-Si/s-Ge bilayer TFET wafer, delamination occurs between at the Al_2O_3 interface below the semiconductor. Because of the complexity of the structure, it is difficult to identify methods of reducing the delamination in the future.

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