Low-Power Design Techniques for Pipelined Analog-to-Digital Converters

by

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Abstract

In a pipelined architecture, the growth of the hardware and power consumption with the number of bits the converter resolves is linear, while the concurrency of operation by the pipelined stages enables high throughput. These advantages make a pipelined architecture suitable for video-rate applications. Based on this architecture, a set of power minimization techniques is proposed for the pipelined architecture.

In the first technique, a commutated feedback-capacitor switching technique is used to improve the differential nonlinearity of an ADC beyond the capacitor matching accuracy. As a result, the size of the capacitors can be minimized down to the $kT/C$ noise limit. With a reduced capacitive load, the power of the op-amp can be significantly reduced without reducing its speed.

In the second technique, the second stage of the op-amp is shared between adjacent stages of the pipeline while maintaining the offset cancellation capability. As a result, the effective number of op-amps used in the entire pipeline can be reduced by as much as 40%, depending on the ratio of the first to second stage power of the op-amp.

In the third technique, the first stage of the op-amp is reused as the first stage of a comparator pre-amp. In addition, by the addition of two resistors, the common-mode feedback circuit for the first stage of the op-amp is turned into the second stage of the pre-amp. Hence, power is saved by the reuse of existing circuits.

In a two-stage op-amp, the bottom plate of the pole-splitting compensation capacitor is typically connected to the output of the op-amp. In the fourth technique, by inserting a well underneath this compensation capacitor, the bottom-plate parasitic capacitance that would otherwise load the op-amp output is exploited as a common-mode feedback capacitor, saving power for the same settling speed.

This set of power minimization techniques are implemented in a 12-b 5-MHz ADC, consuming 33 mW of power from a 2.5-V analog supply. Fabricated in a 1.2-$\mu$m double-metal double-poly process, the ADC achieves a DNL of $-0.78$ and $+0.63$ LSB with a peak SNR of 67.6 dB.

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Electrical Engineering and Computer Science
To My Family
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It has been a great privilege to be a student of Prof. Hae-Seung Lee in the last six years. Over this period of time, I worked on four different projects ranging from analog image processing circuits to the ADC project on which this thesis is based. In each of these projects, I have benefitted a great deal from his technical guidance and insight. I have also received many encouragement and practical assistance from him during the difficult times of the projects. The pursuit of technical excellence, the dedication to professional standard, and an optimistic outlook are perhaps some of the greatest asset I have learned from Prof. Lee.

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Biography

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Introduction

One of the fundamental attributes of electrical engineering is the ability to manipulate information so as to facilitate its transmission, recording, or some other useful utilities. One familiar example is the telephone. Here, the transducer converts the sound pressure into an electrical signal, representing the voice. This signal is transmitted to the receiving end where the signal is used to drive the speaker, which converts the electrical signal back to sound pressure. The ability of electronic systems to filter out the noise and select the desired signal during transmission is an example of signal processing. For historical reasons, the signal processing was mostly done in the analog domain. The prevalence of modern digital computers gave birth to digital signal processing (DSP). In the last twenty years, the growing trend has been to replace analog processing functions with digital processing functions. Despite this trend, a number of analog components remain critical in many electronic systems. One such component is the Analog-to-Digital Converter (ADC). As far as signal processing is concerned, the physical quantities of interest such as the sound pressure are analog in nature. It is therefore necessary to convert analog signals into digital signals before DSP can be used. After the signal is processed by DSP, a digital-to-analog converter (DAC) is sometimes used to convert the processed signal back to the analog domain as in the case of a compact disc player. In other times, the digital signal can be stored as bits in a computer for further processing or retrieval.

It is clear that without high-performance ADC's and DAC's, the performance of the DSP will be limited. In addition, in recent years, the demand for portable equipments is increasing steadily. In these systems, the size and weight of the equipment are important factors. Since these two factors are strongly influenced by the battery that powers the equipment, power reduction is an important goal.

In a typical mixed-signal system, the digital circuits constitute a large percentage of the transistor count. While power reduction techniques for digital circuits are of paramount importance, there are three factors that highlight the importance of power reduction for analog
circuits.

The first is that at the device level, the scaling of MOS transistors facilitate the digital circuit performance such as the propagation delay, but aggravates the analog performance such as the output resistance. To build a high-gain op-amp, for example, extra gain-enhancement circuits such as cascodes have to be added to overcome the low intrinsic gain of the devices. The extra circuits either consume more power or require additional power to bias it. More importantly, they often lead to a reduction of the op-amp output voltage swing, resulting in a corresponding decrease in the signal-to-noise ratio (SNR). To compensate, additional power has to be consumed to maintain the SNR.

The second factor is that as power supply is scaled down, analog circuits experience more severe degradation of performance compared to digital circuits. The reduced supply, for example, directly reduces the op-amp output voltage swing described previously. In a $kT/C$-noise limited system (to be described in Section 4.2), for a given amount of noise, for every factor of two reduction in the power supply, the SNR goes down by a factor of 6 dB. To maintain the same SNR, the rms noise needs to be reduced by 6 dB by increasing the capacitor size four times. As a result, the current and widths of the devices have to be increased four times to maintain the same settling speed. Hence, with a reduction of two in power supply, the analog circuits actually have to double their power consumption.

Another factor that highlights the difference between the analog and the digital circuits is the different modes of operation. In analog circuits, the devices tend to be large and operate with large quiescent power dissipation. On the other hand, in digital circuits, the devices tend to be small and operate with dynamic power dissipation.

The combination of these factors lead to an increasing fraction of the total power consumption by the analog circuits as the technology and supply are scaled [1]. In addition, since a wide range of power reduction techniques are available for digital circuits, these factors point to a growing need for power reduction techniques for analog circuits.

Because of the many design constraints between the various specifications in an analog circuit, a set of completely general power reduction techniques is difficult to implement. Since ADC's are a critical part of many signal processing systems, this thesis will demonstrate power reduction techniques and strategies for ADC's.

This thesis is organized as follows. In Chapter 2, after a description of some of the key specifications for ADC's and the target application, an overview of some commonly used ADC architectures is given. While each of these architectures has its strengths and weaknesses, for applications requiring high throughput rate (≥ 1MHz) and moderate resolution (10-14 bits), a pipelined architecture is selected for its low-power consumption.

In Chapter 3, a more detailed description of the pipelined architecture including implementation non-idealities is given. In Chapter 4, a set of power reduction techniques are presented as an example of the various levels at which power can be minimized. Chapter 5 describes the
design of an experimental chip in detail. In Chapter 6, some experimental procedures and cautions necessary to characterize an ADC are described along with experimental results obtained. Chapter 7 summaries the thesis and proposes some possible future research topics in this area.
Architecture Selection

2.1 Introduction

A number of ADC architectures are commonly in use for a wide array of different applications. In this chapter, a description of the performance metrics used to characterize an ADC is first given in Section 2.2. The video applications will be briefly described in Section 2.3. Finally, some of the commonly used ADC architectures will be described. As will be shown, the pipelined architecture is well suited for video applications.

2.2 Performance Metrics

A number of parameters are used to measure the performance of an ADC. In this section, the parameters relevant to this thesis will be described.

2.2.1 Conversion Rate

The conversion speed refers to the number of digital samples an ADC can convert from an analog input in a given time. It is typically measured in Msample/s. For a 5 Msample/s ADC, the ADC can produce a complete digital sample in 200 ns. For Nyquist rate ADC's such as a flash or a pipelined ADC, the conversion rate is equal to the clock frequency, which is twice the maximum allowed input frequency. For oversampling ADC's, the conversion rate is significantly lower than the clock frequency by a factor of the oversampling ratio.

2.2.2 Differential NonLinearity (DNL)

For an ideal ADC, the output digital codes can be plotted as a function of the input analog voltage as shown in Fig. 2-1. For simplicity, the ideal staircase transfer curve is replaced with a
straight line. For a digital output code \( D_{i+1} \), there exists a decision voltage \( V_{i+1} \) at the input. This decision voltage is defined as the voltage such that if it is decreased slightly, the output digital code will drop to \( D_{i} \). A similar decision voltage \( V_{i} \) exists for the code \( D_{i} \).

![Figure 2-1: An ideal ADC transfer curve.](image)

For an ideal ADC, the spacing between the adjacent decision points is equal to the voltage \( V_{LSB} \) corresponding to one Least Significant Bit (LSB). In other words, the difference between \( V_{i+1} \) and \( V_{i} \) is equal to \( V_{LSB} \), which is given by \( V_{FS}/2^n \), where \( V_{FS} \) is the full-scale analog input voltage, and \( n \) is the resolution of the ADC in bits. Non-idealities in the ADC, however, can cause the spacing to be either greater or less than 1 LSB. As a measure of the non-ideal decision spacings, the DNL for a particular digital output code is defined as

\[
dnl[i] = \frac{(V_{i+1} - V_{i})}{V_{LSB}} - 1,
\]

where, \( i \) is equal to the value of the digital output \( D_{i} \).

![Figure 2-2: A transfer curve with a missing code.](image)

Thus, in one extreme case when the digital output code \( D_{i} \) never appears at the output, the analog decision point \( V_{i+1} = V_{i} \). This is known as a missing code as shown in Fig. 2-2. In this case, the DNL = -1 for the code \( D_{i} \). From Equation (2.1), a DNL of -1 is the worse case negative DNL an ADC can have. In the other case, when \( V_{i+1} - V_{i} = 2 V_{LSB} \), DNL = +1.
This is known as a wide code. Since there is no limit to how far \( V_{i+1} \) can be from \( V_i \), the positive DNL can be larger than +1.

### 2.2.3 Integral NonLinearity (INL)

While the DNL measures the resolution of an ADC, the absolute accuracy is given by the INL. As an example, Fig. 2-3 shows a transfer plot of an ADC. The INL is defined as the difference between the actual output codes produced by the ADC and the ideal linear curve. The double-headed arrow in Fig. 2-3 shows that for this ADC, the worse case INL occurs at the code \( D_i \).

![Figure 2-3: A transfer curve with large INL.](image)

It is important to distinguish the difference between DNL and INL. Since the DNL is a measure of the variation in spacing of adjacent decision points, it is a measure of how small an input voltage the ADC can resolve. While an ADC can resolve a 1 LSB difference between two input voltages at a 12-b level, for example, it may not be accurate to the same resolution. In other words, the DNL of an ADC in LSB can be smaller than its INL in LSB. An example of this situation is shown in Fig. 2-3 where the ADC has no gross DNL errors and yet a maximum INL of approximately 10% of the full-scale voltage is clearly visible. This point will be expanded in Chapter 4.

### 2.2.4 Signal-to-Noise Ratio (SNR)

For an ideal ADC, > root-mean-square (rms) quantization noise is given by \[2\]:

\[
V_{noise, rms} = \sqrt{\frac{\int_{-\frac{1}{2}V_{LSB}}^{\frac{1}{2}V_{LSB}} V^2 dV}{V_{LSB}}} = \frac{1}{\sqrt{12}} V_{LSB}.
\] (2.2)

A full-scale analog sine wave input with a peak-to-peak voltage of \(2^n \cdot V_{LSB}\) has a rms value
given by

\[ V_{FS,rms} = \frac{1}{2 \sqrt{2}} \cdot 2^n \cdot V_{LSB}. \]  \hspace{1cm} (2.3)

Thus, for an ideal \( n \)-bit ADC, the SNR with a full-scale sine wave input is obtained by dividing Equation (2.3) by Equation (2.2):

\[
SNR_{FS} = 20 \log_{10} \left( \frac{V_{FS,rms}}{V_{noise,rms}} \right) \\
= 20 \log_{10} \left( \frac{1}{2 \sqrt{2}} \cdot 2^n \cdot V_{LSB} \right) \\
= 20 \log_{10} \left( \frac{1}{\sqrt{12}} V_{LSB} \right) \cdot \left( \frac{\sqrt{6}}{2} \right) \\
= 6 n + 1.76 \text{ in dB}. \hspace{1cm} (2.4)
\]

From Equation (2.4), for an ideal 12-b ADC, the peak SNR = 73.8 dB.

2.2.5 Signal-to-Noise-and-Distortion Ratio (SNDR)

While SNR is a measure of the noise level of an ADC relative to its peak input signal, SNDR is a measure of the noise plus the harmonic distortion energy relative to its peak input signal. The harmonic distortion is a result of the nonlinearity of the ADC. In the calculation for SNDR, typically the first five harmonics are used.

2.3 Target Application

Having defined the performance metrics, the target application will be described before the architectures are discussed in the next section.

One of the most challenging area of application is the video imaging applications. Since an imaging sensor such as the Charge-Coupled Device (CCD) produces an output in the form of an analog signal, an ADC is needed to convert this analog signal into digital codes that can be further processed by the DSP. The diagram shown in Fig. 2-4 illustrates the front-end of a typical imaging system [1]. Here, after light is converted into charge and subsequently voltage by the CCD chip, the signal is passed to a Correlated Double Sampling (CDS) circuit. The purpose of this block is mainly to remove the \( kT/C \) noise associated with the CCD output circuit. Subsequently, an automatic gain control (AGC) circuit is used to amplify the signal so that the entire dynamic range of the ADC can be utilized. This amplified signal is then digitized by the ADC for further processing in the digital domain.

In this type of application, the conversion rate is typically determined by the frame rate
2.4 Common ADC Architectures

and the number of pixels per frame. For a frame rate of 30 frames/s, and a frame size of 256 x 256, the required conversion rate is 1.97 Msample/s. As the linear dimension of the frame increases, the conversion rate required for the ADC increases quadratically. Thus, for the same frame rate of 30 frames/s, if the frame size increases to 512 x 512, the required conversion rate becomes 7.86 Msample/s. As a result, there is an increasing demand for increasingly faster ADC.

In addition to the speed requirement, there is a resolution requirement for the ADC’s. With a large resolution, the image intensities are quantized into a large number of levels, with a correspondingly higher SNR. In a large number of applications such as a medical and scientific imaging, 12-b resolution is often required. In the consumer electronics application such as a camera recording (camcorder) system, 10-b resolution is commonly in use. As the performance of DSP improves, higher resolution ADC’s will be desired in the near future [3].

2.4 Common ADC Architectures

Having described the video imaging application as the target application for the ADC, some of the common ADC architectures with video-rate capabilities are presented.

2.4.1 Flash Architecture

One of the most commonly used ADC architecture for video application is the flash architecture [4] as shown in Fig. 2-5. For an n-bit flash ADC, $2^n - 1$ comparators are used. The analog input $V_{IN}$ is presented to the negative inputs of the comparators in parallel. Each of these comparators compares $V_{IN}$ with a reference which is typically derived with a resistive string that divides the reference into $2^n$ equal segments. For a given $V_{IN}$, all the comparators whose reference inputs are less than $V_{IN}$ produce a '0'; all the comparators whose reference inputs are greater than $V_{IN}$ produce a '1'. The resulting digital output is known as a thermometer code. An encoder logic is used to convert the thermometer code into a binary code.

The conversion speed of a flash ADC is determined by the comparator time and the encoder time. Since the comparators work in parallel, by maximizing the comparator and encoder speed, a flash ADC usually achieves the highest conversion speed in a given technology. The drawback is that the resolution achievable using a flash architecture is typically limited to a maximum of 8 b. This limitation is predominantly due to the fact that the amount of hardware and power
consumption needed are exponentially dependent on the number of bits resolved. Beyond 8 b, the enormous amount of power and hardware become unmanageable.

![Diagram of a flash ADC architecture]

**Figure 2-5:** A flash ADC architecture.

### 2.4.2 Two-Step Architecture

The exponential increase in power consumption of the flash architecture can be minimized by using a multi-step architecture, of which a two-step architecture [4] as shown in Fig. 2-6 is a special case. As the name implies, the conversion is performed in two steps. A coarse quantization is first performed to arrive at the first \( m \) MSB's. This code is converted back to an analog voltage using a digital-to-analog converter (DAC) and subtracted from the input. The difference is digitized by a second ADC for the remaining \( k \) LSB's. Typically, the output codes of the two ADC's overlap by 1 b to perform error correction [5]. Therefore, the overall resolution is \( (m + k - 1) \) b.

The advantage of a two-step architecture is that the amount of hardware and power consumption are much less than a flash ADC. For a two-step 12-b ADC, assuming a coarse quantization of 7 b and a fine quantization of 6 b, the hardware and power requirement is proportional to \( 2^7 + 2^6 \), as opposed to \( 2^{12} \) for a flash ADC. Thus, although the conversion speed is less than a flash ADC by a theoretical factor of two, significant hardware and power saving can be achieved.

In practice, the two-step architecture has its drawbacks. First, the subtractor takes the analog input and the output of the DAC as its two inputs, the two paths have different delays. This difference in delay necessitates the use of a sample-and-hold amplifier (SHA) at the input
of the ADC. Since this SHA must be accurate to the full resolution of the ADC, a large amount of power is required. Second, the DAC must be accurate to the entire resolution of the ADC, not just that of the second stage ADC [5]. As a result, the DAC must take time to achieve the required precision, making the conversion speed more than a factor of two slower than a flash ADC.

2.4.3 Folding Architecture

The use of a SHA, a DAC and a subtractor in a two-step architecture described above can be eliminated by using analog pre-processing in the folding architecture [6] shown in Fig. 2-7. The analog input voltage $V_{IN}$ is applied to a coarse quantizer and an analog pre-processor in parallel. The coarse quantizer produces the first $m$ MSB's, while the analog pre-processor folds $V_{IN}$ into $2^m$ segments of the residue voltages $V_{RES}$. For Fig. 2-7, $m$ is equal to 3. The resulting voltage is digitized by the $k$-bit ADC to arrive at the remaining $k$ LSB's. In this manner, the number of comparators used is comparable to that in a two-step ADC.

By eliminating speed bottlenecks such as the SHA in a two-step architecture, the folding architecture can achieve a high conversion rate that is close to a flash ADC, while using much less hardware and power consumption than a flash ADC. Nonetheless, the folding architecture has several drawbacks. First, the analog input signal frequency is increased by a factor of $2^m$ by the folding operation. This limits the maximum number of times $V_{IN}$ can be folded. Consequently the power and area saving advantage compared with a flash ADC is limited. Second, the analog pre-processor ideally should produce the triangular waveform shown in Fig. 2-7. In practical implementation, the triangular waveform often resembles a sinusoidal waveform, producing nonlinearities in the ADC. Although interpolation schemes can be used to minimize this effect [7], most folding ADC’s have a maximum resolution of about 8 b.
2.4.4 Pipelined Architecture

In both the two-step architecture and the folding architecture, although the number of comparators and the power consumption is minimized compared with that of a flash ADC, they still grow exponentially with the number of bits resolved. This is contrasted with the pipelined architecture in which an $N$ number of pipelined stages are used as shown in Fig. 2-8. Each stage consists of a SHA, an Analog-to-Digital-SubConverter (ADSC), a Digital-to-Analog-SubConverter (DASC), a subtractor, and an interstage amplifier. For ease of discussion in Chapter 3, the $m$-bit ADC and DAC used in each pipelined stage are termed 'subconverters' to distinguish them from the overall pipelined converter [8]. By pipelining, the stages perform the operation concurrently. Therefore, the conversion speed of the overall ADC is equal to the speed of a single stage, allowing high throughout. The resulting latency due to the pipeline operation can be tolerated in a large number of applications [9]. In addition, the growth of hardware and power with the number of bits resolved is linear. This represents a tremendous saving in hardware and power as the resolution of the ADC increases.

As video applications increasingly demand resolution of greater than 8 b, the pipelined architecture becomes increasingly attractive. Although the necessity of a SHA for each stage of the pipeline does prevent a pipelined ADC from matching the speed of a flash ADC, recent advances in both circuit design techniques and process improvements have made video-rate pipelined ADC's with resolution of greater than 8-10 b feasible.
2.4.5 Cyclic Architecture

An architecture that is closely related to the pipelined architecture described in the previous section is the cyclic architecture shown in Fig. 2-9. Rather than using $N$ pipelined stage, a single stage is used. For the first clock cycle of every $N$-cycle period, switch $M1$ is connected to $V_{IN}$ which is applied as an input to the ADC. After performing a similar set of operation described previously for a pipelined stage, the analog output $V_{RES}$ is recycled as the analog input by connecting the switch $M1$ to $V_{RES}$. This is done for $N - 1$ clock cycles in an $N$-cycle period. At the end of the $N$-cycle period, one complete conversion is achieved. Thus, for the same clock rate, the conversion speed of a cyclic ADC is $N$ times slower than a pipelined ADC. However, since only one stage is used, the area and power are also $N$ times smaller than a pipelined ADC using $N$ identical stages.
sample is produced. It is possible to use, for example, two pipelined stages and the signal is recycled $N/2$ times. This is referred to as a pipelined cyclic ADC [10].

Although power efficient, cyclic or pipelined cyclic ADC's operate at a reduced conversion speed compared with the pipelined ADC. Therefore, the pipelined ADC is selected as a vehicle for the demonstration of power minimization techniques that do not compromise the speed and accuracy requirements for video applications.

2.4.6 Other Architectures

Some of the commonly used ADC architectures for video applications have been described above. A number of general architectures exist, including the successive approximation and the sigma-delta architectures. However, most of these architectures, although capable of high resolution, cannot achieve the high conversion rate needed for video applications due to the large number of clock cycles necessary to perform one conversion.

2.5 Summary

A set of performance metrics is presented to facilitate the selection of an ADC architecture in this chapter as well as specifying and characterizing an ADC in general. Video applications are identified as the area for which the ADC described in this thesis is intended. Driven by this application, a number of video-rate capable ADC architectures are presented, including a flash, a two-step, a folding, and a pipelined architecture. Because of its linear growth of the power and the area with the number of bits resolved, the pipelined architecture is selected as a design vehicle to demonstrate the low-power ADC design techniques to be described.
Conventional Pipelined ADC

3.1 Introduction

As described in Chapter 2, the power efficiency of a pipelined ADC makes it suitable for video applications. In this chapter, a more detailed description of a conventional pipelined ADC is given. The wide availability of CMOS technology makes switched-capacitor techniques feasible. As a result, the description of the pipeline implementation assumes the use of switched-capacitor circuits. In Section 3.2, the basic principle of operation of a pipelined ADC will be explained, assuming ideal components. In section 3.3, a description of non-idealities encountered in a typical switched-capacitor implementation is given. Finally, in Section 3.4, various design considerations related to the details of the pipelined architecture are described.

3.2 Basic Operation

3.2.1 General Description of a Pipeline

A typical pipelined architecture uses a number of similar pipelined stages labeled Stage 1, Stage 2, etc. as shown in Fig. 3-1. As indicated in Section 2.4.4, all of the pipelined stages are similar in construction, consisting of a sample-and-hold amplifier (SHA), a Digital-to-Analog-SubConverter (DASC), an Analog-to-Digital-SubConverter (ADSC), a subtractor, and a multiply by $2^{m_i}$ amplifier. The symbol $m_i$ denotes the number of bits the $i$th stage of the pipeline resolves.

The input $V_{IN}$ is first sampled-and-held, and then digitized by the ADSC to arrive at the first $m_0$ MSB's, represented by $d_0$. This digital code $d_0$ is applied to the DASC to produce an analog voltage which is subtracted from the sampled-and-held input. The difference represents the residue, or error in the coarse quantization of the ADSC, and is amplified by $2^{m_0}$ to scale
it back to the full scale. This amplified residue, $V_{RES1}$, is passed to Stage 2 as an input. After performing a similar set of operations as described for Stage 1, Stage 2 resolves the next $m_1$ MSB's.

In this manner, as the input signal is processed by Stage 1, Stage 2 concurrently processes the residue signal $V_{RES1}$ from the previous sample, while Stage 3 concurrently processes $V_{RES2}$ corresponding to still the sample before the previous sample and so on. After the signal has propagated through $N$ stages in $N$ clock cycles, one complete conversion is achieved. The total resolution is given by

$$Resolution = \sum_{i=0}^{N-1} m_i \text{ bits.} \quad (3.1)$$

The resolution of the converter can be increased by adding additional stages in the pipeline. While the latency is increased, the conversion rate, to first order, remains the same as before\(^1\). This feature enables the pipelined architecture to achieve a high throughput. In a typical implementation, the digital codes $d_0$, $d_1$, $d_2$, etc are overlapped by 1 b to perform digital error correction [11]. As will be seen in Section 3.3.4, when redundant digital codes are needed for digital error correction, the number of stages must be increased for a given resolution. In this case, the latency is increased, while the throughput is maintained.

### 3.2.2 A 1-b-per-stage Switched-Capacitor Example

A pipelined ADC consists of alternating odd and even stages of the pipeline. Each of the pipelined stages shown in Fig. 3-1 is typically implemented using a switched-capacitor circuit consisting of capacitors, MOS switches, and op-amps. A non-overlapping two-phase clocking scheme is commonly used to control the switches. The switched-capacitor implementation of a 1-b-per-stage example is shown in Fig. 3-2 for the odd stages of the pipeline. For clarity, only switches that are ON in a given phase are shown. The even stages operate by exchanging $\phi_1$

\(^1\)As the resolution increases, the op-amp open-loop DC gain has to increase, resulting in a slower operating speed.
with $\phi_2$ [12].

During the sampling phase, the analog input $V_{IN}$ is connected to the bottom plates of two capacitors $C_1$ and $C_2$ which are nominally equal in capacitance. Since the op-amp inverting input is at a virtual ground, the charge stored on capacitors $C_1$ and $C_2$ is equal to $V_{IN} \cdot (C_1 + C_2)$. At $t = t_2$, the falling edge of $\phi_1$ turns off the feedback sampling switch M1. At this point, since the MOS op-amp has an infinite input resistance, the charge on $C_1$ and $C_2$, which are proportional to $V_{IN}$, is trapped. This results in the input voltage $V_{IN}$ being held on capacitors $C_1$ and $C_2$. During the amplification phase, the bottom plate of $C_1$ is connected to the output of the op-amp, making $C_1$ a feedback capacitor. At the same time, the bottom plate of $C_2$ is connected to either $V_{REF}$ or Ground (GND), depending on the comparator decision $d_i$ on the analog input. At the end of $\phi_2$ at $t = t_4$, the op-amp settles and the amplified residue $V_{RES_i}$ is generated.

Assuming an ideal op-amp with $V_- = 0$, and equating the charge stored on the capacitors during the sampling and the amplifying phases:

$$
\frac{(0 - V_{IN})(C_1 + C_2)}{\text{Charge during sampling phase}} = \frac{(0 - d_i \cdot V_{REF}) \cdot C_2 + (0 - V_{RES}) \cdot C_1}{\text{Charge during amplifying phase}},
$$

(3.2)

where the subscripts in $d_i$ and $V_{RES_i}$ are omitted for simplicity. Rearranging Equation (3.2) yields:
\[ V_{RES} = \left( \frac{C_1 + C_2}{C_1} \right) \cdot \frac{V_{IN} - d \cdot V_{REF} \cdot \left( \frac{C_2}{C_1} \right)}{\text{gain of two}} \cdot \text{DASC} \] (3.3)

The first term in Equation (3.3) is the result of the multiply by \(2^{m_i}\) amplifier, while the second term is the output of the the DASC multiplied by \(2^{m_i}\). Here, \(m_i = 1\).

Assuming perfectly matched capacitors, Equation (3.3) simplifies to

\[ V_{RES} = 2 \cdot V_{IN} - d \cdot V_{REF}. \] (3.4)

Thus, after the input is sampled at the end of \(\phi_1\), a residue output voltage \(V_{RES}\) given by Equation (3.3) is produced at the end of \(\phi_2\). Compared with Fig. 3-1, this residue voltage equation embodies the coarse quantization by the ADSC, conversion back to the analog domain using the DASC, subtraction from the SHA output, and multiplication by two.

**Timing for the Odd and Even Stages of the Pipeline** The previous discussion focused on the operation of the odd stages of the pipeline. Since the pipeline consists of alternating odd and even pipelined stages, the even stages operate by exchanging \(\phi_1\) with \(\phi_2\). In other words, during clock phase \(\phi_1\), the odd stages operate in the sampling mode, while the even stages operate in the amplifying mode. When the clock phase changes to \(\phi_2\), the odd stages operate in the amplifying mode, while the even stages operate in the sampling mode. Thus, the analog input labeled \(V_{IN}\) in Fig. 3-2 is the analog output from the previous even stage of the pipeline. The analog output labeled \(V_{RES}\) is the input voltage for the following even stage of the pipeline. At the end of \(\phi_2\) at \(t = t_4\), the residue voltage generated by the odd stage is sampled by the even stages of the pipeline when the falling edge of \(\phi_2\) turns off the feedback sampling switches for the even stages. In this way, the analog signal propagates down the pipeline so that the following pipelined stage can resolve additional bits. When the signal reaches the end of the pipeline, one complete digital sample is obtained.

**Input Sample-and-Hold Stage** In a conventional pipeline, a dedicated sample-and-hold stage is needed at the input of the pipeline. This is because dynamic errors can be reduced by using the sampled-and-held signal as the input, instead of \(V_{IN}\), for the comparator. In addition, a comparator decision is necessary at the beginning of the amplifying phase in order to apply the appropriate reference voltage to the bottom plate of \(C_2\).

A typical implementation of this sample-and-hold circuit is shown in Fig. 3-3. During the sampling phase, the operation is the same as the circuit shown in Fig. 3-2 previously but with only one capacitor. During the amplification phase, the bottom plate of \(C_1\) is connected to the output of the op-amp to produce a sampled-and-held output in a gain-of-one configuration. This output is applied to the input of the next stage for sampling and to a comparator to
arrive at the MSB decision. Note that the analog input to the comparator is the sampled input voltage, instead of the dynamically changing $V_{IN}$.

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{pipeline_input_stage.png}
\caption{The input stage of a pipeline.}
\end{figure}

### 3.3 Non-Ideal Effects

When implemented using a switched-capacitor circuit, the residue voltage generated is only approximately equal to that given by Equation (3.4). Several sources of errors exist due to non-ideal components. Some of the common non-ideal effects and the typical solutions are discussed in this section.

#### 3.3.1 Finite Op-Amp DC Open-Loop Gain

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{finite_op_amp_gain.png}
\caption{The effect of a finite op-amp gain.}
\end{figure}
Using the circuit in Fig. 3-4, the effect of a finite op-amp open-loop gain can be analyzed by applying the charge conservation principle. A parasitic capacitance \( C_p \) at the inverting input of the op-amp has been added for completeness. During the amplification phase, the output of the op-amp, \( C_o \), which models the load capacitance of the op-amp such as the sampling capacitance of the following pipelined stage and the input capacitance of the comparator, is also added. The offset voltage of the op-amp, which is ignored for now, will be discussed in Section 3.3.5.

During the sampling phase, \( V_O = V_- \) as dictated by the direct feedback and \( V_O = -a \cdot V_- \) as dictated by the forward path of the op-amp. The symbol \( a \) denotes the DC open-loop gain of the op-amp. These two conditions given by the forward and the feedback paths force \( V_- = 0 \). During the amplifying phase, the charge sampled on capacitors \( C_1 \) and \( C_2 \) redistribute as follows:

\[
\frac{(0 - V_{IN}) \cdot (C_1 + C_2)}{C_1 + C_2} = \frac{(V_- - d \cdot V_{REF}) \cdot C_2 + (V_- - V_O) \cdot C_1 + V_- \cdot C_p}{C_1 + C_2}.
\]

Charge during sampling phase Charge during amplifying phase

Rearranging Equation (3.5) yields:

\[
V_O = V_{IN} \cdot \left( \frac{C_1 + C_2}{C_1} \right) - d \cdot V_{REF} \cdot \frac{C_2}{C_1} + \frac{V_- \cdot \left( C_1 + C_2 + C_p \right)}{C_1}.
\]

The feedback factor \( f \) is defined as the fraction of the op-amp output voltage that is fed back to the op-amp input. Therefore, from Fig. 3-4, the feedback factor \( f \) during the amplification phase is given by,

\[
f = \frac{C_1}{C_1 + C_2 + C_p}.
\]

(3.7)

Substituting Equation (3.7) into Equation (3.6) and making use of the fact that \( V_O = -a \cdot V_- \),

\[
V_O \approx V_{IN} \cdot \left( \frac{C_1 + C_2}{C_1} \right) \left( 1 - \frac{1}{a f} \right) - d \cdot V_{REF} \cdot \left( \frac{C_2}{C_1} \right) \left( 1 - \frac{1}{a f} \right),
\]

where the following approximation is made:

\[
\frac{1}{1 + \frac{1}{a f}} \approx 1 - \frac{1}{a f}
\]

(3.9)

Assuming that \( C_1 \) and \( C_2 \) are perfectly matched,

\[
V_O \approx 2 V_{IN} \cdot \left( 1 - \frac{1}{a f} \right) - d \cdot V_{REF} \left( 1 - \frac{1}{a f} \right).
\]

(3.10)

Comparing Equation (3.10) with the ideal case given by Equation (3.4), the fractional error is approximately \( 1/af \). As an example, for a 12-b ADC with a 1-b-per-stage architecture, \( V_O \)
constitutes the input of the following 11 stages. If the maximum tolerable DNL is 0.5 LSB at 11 b for the following 11 stages, then $1/a_f < 1/2 \cdot 1/2^{11}$ or equivalently

$$a > \frac{1}{f \cdot 2^{12}}.$$  \hspace{1cm} (3.11)

Assuming $C_1 = C_2 = C_p$, so that $f = 1/3$, the minimum op-amp DC open-loop gain $a = 3 \cdot 2^{12} = 12,288$.

In a modern MOS technology, the intrinsic gain of a device, defined as the product of the transconductance $g_m$ and the output resistance $r_o$, is typically low. This is due to both channel-length modulation and drain-induced barrier lowering effects. When an op-amp is built using MOS devices, a variety of circuit topologies [13], [14] can be used, such as a folded cascode [15], [16], a two-stage [13], or a class A3 [17], [18] amplifier. To improve the open-loop gain of the op-amp, a number of techniques can be used including active cascode [19]-[22], positive feedback [23]-[26], and replica-amp gain enhancement [27], [28] to obtain a sufficient gain given by Equation (3.11).

### 3.3.2 Finite Settling Time of an Op-Amp

While the DC open-loop gain of the op-amp can limit the ADC resolution, the settling time of the op-amp limits the ADC conversion speed. During the sampling phase, the output of the op-amp is shorted to the inverting input. The output load capacitance $C_L = C_1 + C_2 + C_p$. For a one-stage op-amp design, the unity-gain frequency $\omega_1$ is given by $\omega_1 = g_m/C_L$, where $g_m$ is the transconductance of the input differential pair. For a two-stage op-amp with pole splitting compensation, $\omega_1$ is given by $g_m/C_c$, where $C_c$ is the compensation capacitor. The feedback factor $f$ is defined as the the fraction of the output that is fed back to the op-amp input. For unity gain feedback, $f$ is unity and the closed-loop bandwidth is equal to $\omega_1$. This assumes that the non-dominant pole is sufficiently higher than $\omega_1$ that the closed-loop system achieves single-pole settling. Accordingly, the settling time constant $\tau$ is $1/\omega_1$. In a first-order system, the dynamic component of the output response is a decaying exponential. As a result, the minimum time required for settling errors of less than 0.5 LSB at the 11-b level is given by $(12 \ln 2)\tau = 8.32\tau$.

During the amplification phase, the feedback factor is decreased to

$$f = \frac{C_1}{C_1 + C_2 + C_p}.$$  \hspace{1cm} (3.12)

Therefore, the closed-loop bandwidth is now $f \cdot \omega_1$, which results in a longer settling time compared with that during the sampling phase. Since the speed of the clock is limited by the settling time during the amplification phase, the conversion rate is proportional to $(1/2) \cdot f \cdot \omega_1$. Assuming a first-order, non slew-rate limited transient response, for a 12-b 5-Msample ADC,
the op-amp has to settle to the required accuracy of 0.0122 % in 100 r.s.

In the previous discussion, a one-stage op-amp has been assumed where the sampling capacitance of the following stage of the pipeline is used as the compensation capacitor. For a two-stage op-amp, the compensation capacitor ($C_c$) is different from the sampling capacitor of the following stage. As a result, the closed-loop bandwidth can be somewhat faster than $f \cdot \omega_1$ by decreasing $C_c$. Since the non-dominant pole is given by $g_m C_c / (C_1 C_2 + C_c (C_1 + C_2))$, as $C_c$ is decreased, the non-dominant pole moves to a lower frequency. The increase in closed-loop bandwidth beyond $f \cdot \omega_1$ is limited by this non-dominant pole. For simplicity, the remainder of this thesis assumes that the close-loop bandwidth is $f \cdot \omega_1$ regardless of the use of a one-stage or a two-stage op-amp.

### 3.3.3 Capacitor Mismatches

In the previous section, the capacitors are assumed to be perfectly matched. From Equation (3.8), when $a$ is infinite, the effect of a capacitor mismatch is given by:

$$
V_O = \left( \frac{C_1 + C_2}{C_1} \right) V_{IN} - d \cdot V_{REF} \left( \frac{C_2}{C_1} \right).
$$

(3.13)

$C_p$ has no effect because when $a$ is infinite, $V_-$ is 0, and no charge is stored on $C_p$.

Let $C_i = C(1 + \epsilon_i)$, where $\epsilon_i$ represents the percentage capacitor mismatch; and $i = 1$ or 2. Then,

$$
V_O = \left( \frac{2 + \epsilon_1 + \epsilon_2}{1 + \epsilon_1} \right) V_{IN} - d \cdot V_{REF} \left( \frac{1 + \epsilon_2}{1 + \epsilon_1} \right).
$$

(3.14)

Ignoring higher order terms and simplifying yields

$$
V_O = (2 - \epsilon_1 + \epsilon_2) V_{IN} - d \cdot V_{REF}(1 - \epsilon_1 + \epsilon_2).
$$

(3.15)

For the example of a 12-b ADC, where $V_O$ from the first stage needs to be good to 0.5 LSB at 11-b level, the capacitors have to be 12-b accurate. As will be shown in more detail in Chapter 4, a special capacitor switching technique can be used to relax this matching requirement.

### 3.3.4 Comparator Offsets

The ideal residue output voltage given by Equation (3.4) is plotted in Fig. 3-5 as curve A. Curve B shows the case when there is a comparator offset. The effect of the offset is that for the analog input range of $[V_{REF}/2, V_{REF}/2 + V_{offset}]$, the digital code is 0 instead of 1. Using digital error correction, the offset problem can be eliminated. To understand how the digital error correction works, it should be noted that while the digital code is too small, the corresponding analog residue is too large. When passed on to the following stages, the large analog residue will be digitized into a large digital code. This large digital code from the
following stages of the pipeline compensates, or digitally corrects, the smaller digital code from the current stage of the pipeline. In other words, the current stage makes a coarse decision, delaying decision for signals near the ideal decision boundary to later stages [11]. At these later stages where the signals are amplified, the decision will be more accurate for a similar offset. Although a positive $V_{\text{offset}}$ is assumed, the reasoning works when $V_{\text{offset}}$ is negative, $d$ is too large, and $V_{\text{RES}}$ is too small.

![Figure 3-5: The residue plot with a comparator offset.]

By overlapping the MSB of $d_{i+1}$ from a later stage with the LSB of $d_i$ of the current stage, the offset error is removed in the digital domain [11]. This technique requires $V_{\text{RES}}$ to not exceed the input range of the following stage. This can be accomplished by reducing the interstage gain $2^m$ by a factor of two. A $V_{\text{offset}}$ as large as $\pm0.5$ LSB of the stage resolution can be accommodated. For a 1-b-per-stage architecture, a more attractive solution can be implemented by using extra comparators to produce a residue plot shown in Fig. 3-6. This is often referred to as a 1.5-b-per-stage architecture [29]. In this case, each comparator can have as much as $\pm1/8 \, V_{\text{REF}}$ of offset if the nominal decision points are at $1/2 \, V_{\text{REF}} \pm 1/8 \, V_{\text{REF}}$.

The previously mentioned digital error correction techniques provides redundancies at every stage of the pipeline. As a result, many extra stages have to be added to the pipeline. As will be shown in Chapter 4, a true over-range technique can be used so that minimum extra hardware is required beyond that of a conventional pipeline.

### 3.3.5 Op-Amp Offsets

The effect of an op-amp offset is typically corrected in the analog domain. Fig. 3-7 shows a typical closed-loop sampling configuration used for offset cancellation. Equating the charge during the sampling phase with that during the amplifying phase yields:
\[
(V_{O1} - V_{IN}) \cdot (C_1 + C_2) + V_{O1} \cdot C_p = (V_{X2} - d \cdot V_{REF}) \cdot C_2 + V_{X2} \cdot C_p + (V_{X2} - V_{O2}) \cdot C_1,
\]

Charge during sampling phase

\[
(V_{X2} - d \cdot V_{REF}) \cdot C_2 + V_{X2} \cdot C_p + (V_{X2} - V_{O2}) \cdot C_1,
\]

Charge during amplifying phase

(3.16)

where,

\[
V_{O1} = V_{OS1} \frac{a}{1 + a},
\]

(3.17)

and

\[
V_{X2} = \frac{V_{O2}}{-a} + V_{OS2},
\]

(3.18)

Equation (3.16) can be simplified to
\[ V_{O2} = V_{IN} \left( \frac{C_1 + C_2}{C_1} \right) \left( 1 - \frac{1}{af} \right) - d \cdot V_{REF} \cdot \left( \frac{C_2}{C_1} \right) \left( 1 - \frac{1}{af} \right) + \left[ V_{OS2} - V_{OS1} \cdot \left( \frac{a}{1+a} \right) \left( \frac{1}{f} \right) \left( 1 - \frac{1}{af} \right) \right]. \] (3.19)

Since the offset voltage under consideration is that of a MOS source-coupled differential amplifier, it is a function of the MOS threshold voltage \( V_T \), aspect ratio \( W/L \) and \( g_m/I_{bias} \) [13]. Of these three terms, the first two are determined by the process, while the third is proportional to the square root of the bias current. Therefore, \( V_{OS1} \) during the sampling phase equals \( V_{OS2} \) during the amplification phase, and the offset voltage is approximately canceled. Equation (3.19) simplifies to:

\[ V_{O2} = V_{IN} \left( \frac{C_1 + C_2}{C_1} \right) \left( 1 - \frac{1}{af} \right) - d \cdot V_{REF} \left( \frac{C_2}{C_1} \right) \left( 1 - \frac{1}{af} \right) + \left[ V_{OS} \cdot \left( \frac{1}{1+a} \right) \left( \frac{1}{f} \right) \left( 1 - \frac{1}{af} \right) \right] \approx V_{IN} \left( \frac{C_1 + C_2}{C_1} \right) \left( 1 - \frac{1}{af} \right) - d \cdot V_{REF} \left( \frac{C_2}{C_1} \right) \left( 1 - \frac{1}{af} \right) + V_{OS} \cdot \left( \frac{1}{af} \right). \] (3.20)

When the op-amp open-loop gain \( a \) is large, \( V_{O2} \) given by Equation (3.20) is approximately equal to \( V_O \) given by Equation (3.8), when no offset is assumed. The residual offset error is proportional to \( 1/af \). This offset cancellation ability is the chief advantage of the closed-loop sampling architecture. An added advantage is that low-frequency noise components such as the \( 1/f \) noise associated with the input MOS differential pair are also largely canceled, provided that the sampling frequency is much larger than the corner frequency of the \( 1/f \) noise [30].

Another method of offset correction is the use of an auxiliary amp in the open-loop sampling approach shown in Fig. 3-12. The description of the open-loop sampling architecture will be presented in Section 3.4.2 along with a comparison with the closed-loop sampling architecture.

In both types of sampling configurations, the charge injection from the MOS switch can also induce an offset, rendering \( V_{OS1} \neq V_{OS2} \). This is the subject of the next section.

### 3.3.6 Charge Injection

When a MOS transistor switches from the ON to the OFF state, the channel charge that is stored when the switch is ON has to be discharged through either the drain or the source terminal. To minimize the charge injection effect, a bottom-plate sampling circuit shown in Fig. 3-2 is used. Before discussing the charge injection aspect of the bottom-plate sampling circuit, a description of the simple top-plate sample-and-hold circuit shown in Fig. 3-8 is first given.
Top-Plate Sample-and-Hold Circuit  The circuit configuration shown in Fig. 3-8 can be used to gain insight into the problem of charge injection [31]. When the gate voltage is at a high level $V_H$ for a period of time that is much longer than the $R_{ON}C_s$ time constant, where $R_{ON}$ is the ON resistance of the transistor, the output voltage $V_O$ is equal to $V_{IN}$. When the gate voltage drops down to $V_L$, there are two mechanisms that contribute to the errors in $V_O$. For simplicity, it is assumed that the falling edge of the clock is much faster than the $R_{ON}C_s$ time constant.

The first source of error is the channel charge injection. When the switch is ON, the charge stored in the channel of the MOS device is:

$$q_{CH} = - (V_H - V_{IN} - V_T) \cdot W \cdot L \cdot C_{ox}. \quad (3.21)$$

Since the falling edge of the clock is assumed to be very fast, the channel charge is split equally between the drain and the source [32]. The error induced at $V_O$ is given by

$$\Delta V_1 = \frac{q_{CH}}{2C_s} = - \frac{1}{2} \frac{(V_H - V_{IN} - V_T) \cdot W \cdot L \cdot C_{ox}}{C_s}. \quad (3.22)$$

The second error source is the clock feedthrough due to the capacitive divider formed by $C_{OL}$ and $C_s$. The error induced at $V_O$ is given by

$$\Delta V_2 = -(V_H - V_L) \cdot \left( \frac{C_{OL}}{C_{OL} + C_s} \right). \quad (3.23)$$

To find the total error from these two sources, Equation (3.22) and Equation (3.23) are substituted into the following equation:

$$V_O = V_{IN} + \Delta V_1 + \Delta V_2. \quad (3.24)$$

After simplifying,
\[ V_O = V_{IN}(1 - \epsilon) + V_{OS}, \]

where the gain error \( \epsilon \) is given by
\[ \epsilon = \frac{1}{2} \cdot \frac{W \cdot L \cdot C_{oz}}{C_s}. \]

The offset voltage \( V_{OS} \) is:
\[ V_{OS} = -(V_H - V_L) \cdot \left( \frac{C_{OL}}{C_{OL} - C_s} \right) + (V_H - V_T) \cdot \left( \frac{W \cdot L \cdot C_{oz}}{C_s} \right). \]

From Equation (3.26), the gain error \( \epsilon \) is caused by a signal-dependent charge injection. The offset \( V_{OS} \), on the other hand, is caused by both the signal-independent charge injection and the clock feedthrough as given by Equation (3.27).

In the previous analysis, the channel charge is assumed to split equally between the drain and the source. In reality, it is difficult to predict the exact ratio of discharge between the drain and the source. This is due to the distributed nature of the channel, the nonlinearity of the MOS I-V characteristics, the dependence on the fall time of the clock, and the source and drain impedances.

In general, however, from Equation (3.22), the following rules can be used to minimize charge injection:

- Minimize the switch size (\( W \) and \( L \)). While \( L \) is limited by technology, \( W \) is limited by the effect of increasing \( R_{ON} \) which leads to increased acquisition time.
- Increase \( C_s \). This is limited by the same speed issue as decreasing \( W \).

**Bottom-Plate Sample-and-Hold Circuit** One of the main problems with the simple top-plate sample-and-hold circuit shown in Fig. 3-8 is the signal-dependent charge injection. Although a half-sized dummy switch can be used to absorb the channel charge [32], the cancellation is dependent on the matching of the two switches and the matching of the rise and fall time of the clock. This problem is largely alleviated in the bottom-plate sampling circuit shown on the left in Fig. 3-9. This circuit is the same circuit illustrated in Fig. 3-2 with the exception that the feedback sampling switch M1 is controlled by \( \phi_{1+} \), instead of \( \phi_1 \). Because \( \phi_{1+} \) is an advanced version of \( \phi_1 \), the sampling switch M1 is turned off shortly before M2 and M3 are turned off. Since the source and drain of M1 are at virtual ground, the charge injection from M1 is, to first order, independent of \( V_{IN} \). The second-order effects will be briefly described below. The signal-independent charge injection from M1 can be modeled as an offset. This offset has no effect on the linearity of the ADC, provided that digital error correction can be properly applied [11]. Once M1 is turned off, M2 and M3 are turned off. Although M2 and M3 are connected to \( V_{IN} \), the charge injection from these two devices have no effect on the charge stored on \( C_1 \) and \( C_2 \) since M1 is already off, trapping the charge on \( C_1 \) and \( C_2 \).
3. Conventional Pipelined ADC

**Figure 3-9:** A 1-b pipelined stage with bottom-plate sampling.

For the simple top-plate sampling circuit shown in Fig. 3-8, the size of the sampling switches can be minimized to minimize the charge injection as discussed above. Similarly, in the bottom-plate sampling circuit shown in Fig. 3-9, charge injection can be minimized by minimizing the size of M1. The minimum width for M1 is limited by the stability of the op-amp. A general rule is to choose its width so that $R_{ON}$ is a few times smaller than $1/g_m$, the reciprocal of the op-amp transconductance.

In the previous discussion, the charge injection from M1 is assumed to be signal-independent. In reality, the impedance of M2 and M3 can have an effect on the charge injected onto $C_1$ and $C_2$ by M1. Since the on-resistances of M2 and M3 depend on $V_{IN}$, there are second-order effects causing the charge injection from M1 to be not completely signal-independent. This problem can be alleviated by maximizing the widths of M2 and M3. However, increasing the widths of M2 and M3 is constrained by the added parasitic capacitance at the two ends of the switches. During the sampling phase, this added parasitic capacitance increases the load for the previous stage of the pipeline that drives the current stage. During the amplification phase, the bottom-plate is switched to the output and increasing the size of M2 and M3 increases the capacitive load of the op-amp used in the current stage of the pipeline.

The clock feedthrough in the bottom plate sampling circuit in Fig. 3-9 occurs when the falling edge of $\phi_1$ turns off M1. Through the gate-to-source overlap capacitance, $\phi_1$ pulls down the inverting node of the op-amp, thus decreasing the amount of charge stored on $C_1$ and $C_2$. By minimizing M1 to minimize the charge injection, the overlap capacitance is also reduced, minimizing the clock feedthrough. In addition, by using a fully differential topology, the clock feedthrough effect becomes common-mode and is rejected by the op-amp. The degree to which
the feedthrough is common-mode depends on the matching between the overlap capacitance of the two sampling switches, and between the total capacitance at the two inputs of the op-amp. It should be noted that in a fully differential topology as shown in Fig. 3-10, the second-order effect due to the ON resistance of the bottom-plate switches M2-M5 does not appear as common-mode and is therefore not rejected by the op-amp. The reason is that the bottom plate switches M2-M3 see an equal and opposite input voltage as that seen by switch M4-M5, assuming the common-mode is 0. Therefore, the ON-resistance of M2-M3 is different from that of M4-M5. As a result, when the sampling switches M1 and M6 are turned off on the falling edge of $\phi_{1+}$, $q_{1i} \neq q_{6i}$. Since the ON-resistances of M2-5 are also functions of $V_{IN}$, a signal-dependent charge injection occurs, leading to a gain error. As in the single-ended case, this error can be minimized by using small feedback switches M1 and M6, and large bottom-plate switches M2-M5.

![Diagram showing signal-dependent charge injection in a fully differential sampling circuit.](image)

**Figure 3-10:** Signal-dependent charge injection in a fully differential sampling circuit.

### 3.3.7 Hysteresis Effects

As the ADC resolution increases, hysteresis effects become important. Oxide traps are known to cause hysteresis-like behavior in MOS transistors and capacitors [33]. There are three places where this effect can manifest itself. The first two are signal-dependent offset voltages for the op-amp and the comparator respectively. The third is the dielectric relaxation of the capacitors.

In the case of a comparator offset hysteresis, the changing offset voltage due to its previous history is not a big problem as long as a digital error correction technique is applied. The offset
hysteresis for the op-amp can cause DNL and INL if the op-amp input is stressed with a large differential voltage. This can occur when the op-amp is slewing. The dielectric relaxation of the capacitors affect the accuracy of ADC's based on charge redistribution. This effect is explored in [33] and [34].

3.4 System Design Considerations

In the previous section, the basic operation of a pipelined ADC was presented, followed by a description of the non-idealities effecting its performance. Some general design issues in implementing a pipelined ADC remain. These issues are explored in this section.

3.4.1 Stage Resolution

Many tradeoffs need to be considered in deciding the number of bits per stage. These tradeoffs can be best understood by comparing a 1-b-per-stage example discussed previously in Section 3.3 with a 2-b-per-stage example shown in Fig. 3-11. During the sampling phase, the bottom plates of four capacitors \( (C_1 - C_4) \) of nominally equal capacitance are connected to \( V_{IN} \). In the 1-b-per-stage case, two capacitors are used. The output of the op-amp is shorted to its inverting input for offset cancellation as in the 1-b case. During the amplifying phase, the bottom plate of \( C_1 \) is switched to the output of the op-amp, while the bottom plates of \( C_2 - C_4 \) are connected to either \( V_{REF} \) or GND, depending on the 2-b digital word \( d \). In the 1-b-per-stage case, one of the capacitors is connected to \( V_{REF} \) or GND, depending on a 1-b digital word \( d \).

![Sampling Phase](image1)

![Amplification Phase](image2)

**Figure 3-11:** A 2-b-per-stage implementation.

Several issues related to the choice of the number of bits per stage arise. The first issue is the settling time. As shown in section 3.3.2, the settling time during the amplification phase is the speed bottleneck because of the smaller feedback factor compared with that during the
sampling phase. In the 2-b case, the feedback factor is given by

\[ f = \frac{C_1}{C_1 + C_2 + C_3 + C_4 + C_p}. \]  

(3.28)

Assuming that \( C_1 - C_4 \) are nominally equal to \( C \) and that \( C_p = C \), then \( f \) is 1/3 in the 1-b case, but is 1/5 for the 2-b case. As shown previously, this decreased \( f \) directly translates to an increased settling time.

The second issue is power consumption. Although the 1-b-per-stage architecture has a faster settling time, it requires twice as many pipelined stages as a 2-b-per-stage pipeline. Also, in a 2-b-per-stage pipeline, after each stage, the accuracy requirement is relaxed more rapidly than for a 1-b pipeline. This relaxed requirement allows the following stage to use smaller capacitors, lower op-amp gain, and lower power consumption. This consideration, while true to some extent, is balanced by other implementation issues. For example, in a 1-b case, the comparator reference is GND for a fully differential topology with zero common-mode. In a 2-b case, two additional reference voltages at \( \pm V_{REF}/2 \) have to be generated. This is typically implemented by a resistor string [11]. The resistors used have to be small enough to allow fast settling time and therefore dissipate certain amount of power.

### 3.4.2 Open- vs. Closed-Loop Sampling

The advantage of using the closed-loop sampling approach shown in Fig. 3-7 is that the offset and the 1/f noise of the op-amp input differential pair are largely canceled as shown by Equation (3.20). The disadvantage of this technique is that the op-amp needs to be unity-gain stable. This stability condition requires that the non-dominant pole of the op-amp be higher than \( \omega_1 \). Thus, extra power is needed.

An alternative architecture uses open-loop sampling [11], [3] as shown in Fig. 3-12. Similar to the closed-loop sampling circuit, the bottom plates of \( C_1 \) and \( C_2 \) are connected to \( V_{IN} \). However, unlike the closed-loop sampling circuit, the top plates of \( C_1 \) and \( C_2 \) are shorted to GND. In addition, the output of the op-amp is connected to an auxiliary op-amp output, instead of shorted to the inverting input. The output resistance \( r_o \) represents the parallel combination of the output resistance of the main and the auxiliary amps. With the main op-amp inputs shorted together, the resulting offset voltage stored on \( C_{OS} \) is:

\[ V_{OS} = \frac{a_1}{1 + a_2} \cdot V_{OS1} + \frac{a_2}{1 + a_2} \cdot V_{OS2}, \]

(3.29)

where,

\[ a_1 = g_m \cdot r_o \]  

(3.30)

\[ a_2 = g_{m2} \cdot r_o \]  

(3.31)
FIGURE 3-12: An open-loop sampling circuit.

During the amplification phase, the offset stored on the auxiliary amp is applied to correct the offset error. This can be shown by examining $V_{RES,OS}$, the offset component of $V_{RES}$, assuming the signal component is 0:

$$V_{RES,OS} = -g_{m1} \cdot r_o \cdot (V_X - V_{OS1}) - g_{m2} \cdot r_o \cdot (V_O - V_{OS2})$$  \hspace{1cm} (3.32)

Since the signal component of $V_{RES}$ is assumed to be 0, $V_X$ as shown in Fig. 3-12 is given by

$$V_X = f \cdot V_{RES,OS},$$  \hspace{1cm} (3.33)

where $f$ is the feedback factor as defined in Equation (3.7). After substituting Equation (3.33) and Equations (3.29)-(3.31) into Equation (3.32) and simplifying,

$$V_{RES,OS} = \frac{a_1}{1 + a_2} \cdot \frac{1}{1 + a_1 f} \cdot V_{OS1} - \frac{a_2}{1 + a_2} \cdot \frac{1}{1 + a_1 f} \cdot V_{OS2}$$  \hspace{1cm} (3.34)

Without the offset cancellation, the offset component of $V_{RES}$ is

$$V_{RES,OS} = \frac{a_1}{1 + a_1 f} \cdot V_{OS1}$$  \hspace{1cm} (3.35)

Comparing Equation (3.34) with Equation (3.35), the input referred offset is given by
From Equation (3.36), the contribution of \( V_{\text{OS, input}} \) to the input referred offset \( V_{\text{OS, input}} \) is smaller by a factor of \( 1 + a_2 \) when offset cancellation is employed. The contribution of \( V_{\text{OS, input}} \) is reduced by a factor of \( g_{m2}/g_{m1} \cdot 1/(1 + a_2) \).

In the previous analysis, the effect of charge injection is ignored for simplicity. It can be shown that the offset induced by the charge injection from switch M1 is reduced by a factor of \( 1 + a_2 \), while the offset induced by the charge injection from M2 is reduced by the ratio of \( g_{m2} \) to \( g_{m1} \) [35].

In open-loop sampling, although the op-amp does not have to be unity-gain stable, the auxiliary op-amp does have to be unity-gain stable. Extra power on the order of 1/3 to 1/5 of the main op-amp power is needed for the auxiliary op-amp.

3.4.3 Segmented vs. Non-Segmented

Each of the pipelined stages in Fig. 3-1 contains an ADSC and a DASC. The nonlinearity of the ADSC in the form of a comparator offset can be corrected using digital error correction. In contrast, the DASC nonlinearity cannot be digitally corrected and must be smaller than the resolution of the remaining pipelined stages. Therefore, the linearity of the DASC of the MSB stage of the pipeline determines the linearity of the entire ADC [11].

![Amplification Phase](image)

**Figure 3-13:** A non-segmented DASC implementation.

The DASC nonlinearity due to a capacitor mismatch was discussed in Section 3.3.3 in the context of a 1-b per stage case. In higher resolution case, such as the 2-b-per-stage case, the
design of the DASC can use equal valued capacitors (segmented) as illustrated in Fig. 3-11 or binary weighed capacitors (non-segmented) as illustrated in Fig. 3-13 when the circuit is in the amplifying phase. During this phase, the output of the op-amp is the amplified difference between the analog input $V_{IN}$ and the analog output of the DASC. Neglecting non-idealities other than the capacitor mismatch, the non-segmented output is given by

$$V_{O,non-seg} = V_{IN} \left( \frac{C_1 + C_2 + C_3}{C_1} \right) - \left( d_0 \cdot V_{REF} \cdot \frac{C_2}{C_1} + d_1 \cdot V_{REF} \cdot \frac{C_3}{C_1} \right)$$  \tag{3.37}$$

Amplified output of the non-segmented DASC

where $d_1$ and $d_0$ are the MSB and LSB of $d_{out,i}$ respectively. In contrast, the segmented output is given by

$$V_{O,seg} = V_{IN} \cdot \left( \frac{C_1 + C_2 + C_3 + C_4}{C_1} \right) - \left( s_2 \cdot V_{REF} \cdot \frac{C_2}{C_1} + s_3 \cdot V_{REF} \cdot \frac{C_3}{C_1} + s_4 \cdot V_{REF} \cdot \frac{C_4}{C_1} \right)$$  \tag{3.38}$$

Amplified output of the segmented DASC

where,

$$s_2 = d_1 + d_0,$$ \hspace{1cm} \tag{3.39}
$$s_3 = d_1 \cdot d_0 + d_1 \cdot d_0,$$ \hspace{1cm} \tag{3.40}
$$s_4 = d_1 \cdot d_0$$ \hspace{1cm} \tag{3.41}

The DASC output as given by the second terms in Equation (3.37) for the non-segmented case and in Equation (3.38) for the segmented case are plotted in Fig. 3-14. The symbol $\times$ represents the actual DASC analog output. The symbol $\circ$ indicates the ideal analog output when the code $d_i = \{10\}$. For both the non-segmented and segmented case, all the capacitors are assumed to be ideal, except $C_3$ which has an exaggerated 60% error from its nominal value. In a non-segmented case, since $C_3 = 2C$, this represents 120% of the unit capacitance. In contrast, in a segmented case, since $C_3 = C$, this represents 60% of the unit capacitance. From Fig. 3-14, the DASC transfer curve is non-monotonic for the non-segmented case, while that of the segmented case remains monotonic. From the transfer curves in Fig. 3-14, it is also clear that with the same percentage mismatch in $C_3$ as indicated above, the worst-case INL of the nonsegmented case is 1.2 $V_{REF}$, which is twice that of the segmented case. When used in a pipelined stage where the DASC output is subtracted from $V_{IN}$ as shown in Fig. 3-1, the larger INL introduced by the non-segmented DASC degrades the accuracy of the overall ADC more severely than the segmented DASC does.
Figure 3-14: (a) Segmented (b) Non-segmented DASC transfer curves.

One the other hand, the use of segmented capacitors has its own drawbacks, including the more complicated switching requirements as shown by Equations (3.39)-(3.41). For most pipelined architectures, the stage resolution is usually less than 3-4 b. As a result, the segmented approach is preferred in general.

3.4.4 Resistor String vs. Capacitor Divider

Previous discussion has assumed the use of a resistor string for generating the comparator reference voltages for ADSC resolution greater than 1 b, and the use of a capacitor array for generating the DASC output. Other possibilities exist. One of these is the use of a resistor string to divide \( V_{REF} \). Taps off the divided voltage provide the DASC output. As a result, the DASC is monotonic. In addition, the ADSC and the DASC can share the resistor string, saving power and area [11]. Another approach is to use a capacitive divider as a comparator reference for the ADSC [36]. The advantage in this case is that only dynamic power is required. The disadvantage is that a capacitor array is required for each comparator.

3.4.5 Single-Ended vs. Fully Differential Topology

Although single ended op-amp topologies can save power and area, fully differential topologies have several important advantages. The first is the reduction of the power supply and substrate noise induced by digital switching. These effects are common mechanisms of ADC performance degradation. When the op-amp is fully-differential, by using careful layout, the supply and substrate noise become common-mode and are rejected by the op-amp. The second is that for a differential circuit, the output of the op-amp has twice as much dynamic range as in the single-ended case. For a given noise level, an increase of 6-dB in SNR is achieved over that of a differential input, single-end output op-amp topology. This added SNR is especially important in low supply design. Third, the signal-independent charge injection and clock feedthrough appear largely as common-mode signals, limited by device matching as described
in Section 3.3.6. These common-mode signals are rejected by the op-amp. Fourth, the linear voltage coefficients of the capacitors are eliminated as common-mode [37]. Fifth, for typical op-amp implementations, since the op-amp input is already differential, the conversion to a fully differential topology usually requires a less than doubling of the area and power. These advantages more than offset the increased power and area requirements.

3.4.6 Noise Analysis

Since the 1/f noise of the op-amp is minimized by op-amp offset cancellation techniques, the remaining dominant noise is the thermal noise of the MOS transistors. For generality, we consider the case of a m-bit-per-stage architecture as shown in Fig. 3-15. The total sampling capacitance is given by $C_s = 2^m \cdot C$, where $C$ is the unit sampling capacitance. For this circuit, the thermal noise from M1, as well as from the input differential pair of the op-amp, have to be considered. Since M1 cannot be too small for stability reasons mentioned in Section 3.3.6, the op-amp unity-gain bandwidth is much smaller than that of the low-pass filter formed by M1 and $C_s$. As a result, the thermal noise of M1 can be neglected [38].

![Diagram of a circuit for kT/C noise calculation.](image)

**Figure 3-15:** A circuit for $kT/C$ noise calculation.

Assuming that the op-amp has a first-order closed-loop frequency response, the noise bandwidth is $\pi/2 \cdot \omega_1 = \pi/2 \cdot g_m/C_L$, where $C_L = C_s + C_p$ during the sampling phase. Since the thermal noise power spectral density of a single MOS device is given by

$$\frac{\overline{v^2}}{\Delta f} = 4 kT \frac{2}{3g_m}, \quad (3.42)$$

where $\Delta f$ is an incrementally small frequency band. Assuming that the mean-square input referred noise ($\overline{v_{eq}^2}$) of the op-amp, is dominated by the two input devices, then $\overline{v_{eq}^2} = 2 \cdot \overline{v^2}$, and the noise sampled on $C_s$ is:

$$\frac{\overline{v_{ns}^2}}{\Delta f} = \overline{v_{eq}^2} \cdot \frac{1}{2\pi} \cdot \frac{g_m}{C_L} \cdot \frac{\pi}{2}$$
\[ \frac{4kT}{3C_L} \]  

(3.43)

For a two-stage op-amp design, \( C_L \) is replaced by \( C_c \) in Equation (3.43), where \( C_c \) is the poie splitting compensation capacitor.

In the amplifying phase, \( \bar{v}_{eq}^2 \) of the op-amp is amplified by a power gain of \((a/(1 + af))^2 \approx (1/f)^2\), the bandwidth is reduced by a factor of \(1/f\), and the gain of the entire circuit is \( \alpha + 1 \), instead of unity. The symbol \( \alpha \) denotes the ratio of input capacitance to the feedback capacitance during the amplifying phase as shown in Fig. 3-15. Accordingly, the noise referred to the input of the circuit is:

\[ \frac{\bar{v}_{na}^2}{\bar{v}_{ns}^2} = \left( \frac{1}{f} \right)^2 \cdot \left( \frac{1}{\alpha + 1} \right)^2 \cdot \text{noise power gain} \cdot \text{bandwidth reduction} \cdot \text{refer back to the input} \]  

(3.44)

For small input parasitic capacitance \( C_p = pC \), \( p << \alpha \), and the expression \( f = 1/(1 + \alpha + p) \) can be approximated as

\[ f \approx \frac{1}{\alpha + 1}. \]  

(3.45)

Thus,

\[ \frac{\bar{v}_{na}^2}{\bar{v}_{ns}^2} \cdot f. \]  

(3.46)

Assuming that the noise during the sampling and amplifying phases are uncorrelated and making use of the approximation given by Equation (3.45), the total input-referred noise power for the \( i \)th stage of the pipeline is:

\[ \frac{\bar{v}_{n,i}^2}{\bar{v}_{ns}^2} = \bar{v}_{ns}^2 + \bar{v}_{na}^2 = f(1 + f) \cdot \frac{4kT}{3C}. \]  

(3.47)

To calculate the total noise referred to the input of the ADC, the noise contribution from each stage of the pipeline must be divided by the gain from the input of the ADC up to that stage. Assuming that all stages are identical,

\[ \frac{\bar{v}_{tot}^2}{\bar{v}_{ns}^2} = f(1 + f) \cdot \frac{4kT}{3C} (1 + f^2 + f^4 + \ldots). \]  

(3.48)

As the number of stages approaches infinity, the noise in Equation (3.48) approaches the limit given by

\[ \frac{\bar{v}_{tot}^2}{\bar{v}_{ns}^2} = \frac{f}{1 - f} \cdot \frac{4kT}{3C}. \]  

(3.49)

Note that since two input transistors are assumed in calculating \( \bar{v}_{na}^2 \) and \( \bar{v}_{na,i}^2 \), Equation
(3.47) is the correct expression for a fully differential case, without the factor of two involved.

For a 1-b case, \( f = 1/2 \), and \( v_{tot}^2 = (8/3) \cdot kT/C \). For a 2-b case, \( v_{tot}^2 = (16/9) \cdot kT/C \).

For a full-scale reference of \( V_{FS} \), for 3 \( \sigma \) of the \( kT/C \) noise to not exceed the theoretical quantization noise of \( 1/\sqrt{12} \) LSB at the \( n \)-bit resolution,

\[
3\sqrt{\frac{f}{1-f}} \cdot \frac{4}{3} \cdot \frac{kT}{C} \leq \frac{1}{\sqrt{12}} \cdot \frac{V_{FS}}{2^n}.
\]  
\[ (3.50) \]

Simplifying Equation (3.50) yields the following constraint on the minimum unit capacitance necessary to satisfy the \( kT/C \) noise for an \( n \)-bit pipelined ADC:

\[
C \geq 144 \cdot \frac{f}{1-f} \cdot \frac{2^n kT}{V_{FS}^2}
\]  
\[ (3.51) \]

3.5 Summary

A basic description of a pipelined ADC is given followed by an overview of the various non-ideal effects in implementation. These effects include finite op-amp gain, finite settling time error, capacitor mismatches, comparator offsets, op-amp offsets, charge injection, and hysteresis. Several design considerations are then given including stage resolution, open- vs closed-loop sampling, segmentation of the DASC, resistor string vs. capacitor divider implementation of the DASC and ADSC, and the use of a fully differential topology. The chapter is concluded with a noise analysis.
Low-Power Design Techniques for Pipelined ADC's

4.1 Introduction

Minimization of power in analog systems is a challenging task due to the strong interdependent tradeoffs involved. The first step in power minimization is to carefully match the architecture to the application intended for the systems. This matching is particularly important for ADC's as they are moving from being general purpose and stand alone to being embedded in a large application specific system. The pipelined architecture is particularly suited for this type of video application as described in Chapter 2.

The second step in power minimization is to examine the circuit components that consumes the most power. In CMOS switched-capacitor circuits such as that described in Chapter 3, the dynamic power dissipation is typically orders of magnitude below the quiescent power consumed by the analog circuits. In particular, the quiescent power of the op-amps constitute a significant fraction of the total power consumed by a pipelined ADC. This is because high-performance op-amps are needed. Given a set of ADC specifications and a process technology, a certain minimum amount of the quiescent power dissipation is required to satisfy a set of specifications such as the unity-gain bandwidth and the open-loop gain. In this chapter, a set of four techniques for minimizing the quiescent power is described.

For video applications, the INL is not critical as will be shown in Section 4.2. In this case, capacitors used in the ADC can be minimized to reduce the power dissipation. The required DNL can be maintained by using the Commutated Feedback-Capacitor Switching (CFCS) technique. This technique is described as the first power minimization technique in this chapter.

A close examination of the general pipelined architecture in Fig. 3-1 together with its circuit
implementation in Fig. 3-2 in Chapter 3 reveals the second power minimization technique. During the odd phase, the op-amps in the odd stages are in the sampling phase. If offset cancellation is not performed, the op-amps for these odd stages in a conventional pipeline can be switched to the even stages for amplification. When the phase changes to even, the same set of op-amps can be switched back to the odd stages since the roles of odd and even stages interchange. The sharing of the op-amp without affecting the offset cancellation is the subject of the second power minimization technique to be described in Section 4.3.

In the third technique presented in Section 4.4, the first stage of the op-amp is reused as the pre-amp for the comparator. For a given comparator offset, the addition of a pre-amp increases the SNR of the ADC for a given op-amp dynamic range as will be shown. In addition, it also directly cuts down the power of the comparator by allowing it to have an offset larger by the factor equal to the pre-amp gain.

The fourth technique described in Section 4.5 involves exploiting the parasitic capacitance in a two-stage op-amp. By turning the parasitic capacitance into a common-mode feedback capacitance, the op-amp load, and therefore the op-amp power is reduced.

These four techniques are now described in detail. Each technique is presented in terms of its motivation, principle of operation, and relevant design considerations. Whenever appropriate, a comparison with similar or competing techniques is also given.

### 4.2 The Commutated Feedback-Capacitor Switching Technique

#### 4.2.1 Motivation

In a wide range of imaging applications, good DNL is required. However, INL is not very critical in these applications. This requirement is due to the fact that human eyes, while sensitive to the difference in intensities between adjacent pixels, are quite insensitive to the absolute individual pixel intensities. Exploiting this relaxed requirement on INL, an ADC with 12-b DNL only needs to have about 6-8 b of INL. As the INL requirement is relaxed, the resulting distortion requirement can also be relaxed. Therefore, the SNR as opposed to the SNDR will be the primary target. In a conventional ADC, the capacitor size is determined by the matching requirement. That is, the size of the capacitors has to be large enough for a given INL target. Given the relaxed INL for the imaging application, the DNL still needs to be satisfied. In a conventional technique as described in Chapter 3, DNL specification alone requires stringent capacitor matching requirement. The CFCS technique relaxes the capacitor matching requirement, allowing the capacitors to be scaled down to the $kT/C$ noise limit as given by Equation (3.51) in Chapter 3. With a reduced capacitive load, op-amp power consumption is also reduced.
4.2.2 Principle of Operation

![Diagram of pipeline ADC with capacitor mismatch](image)

Figure 4-1: A conceptual pipelined ADC with a capacitor mismatch in the first stage.

For simplicity, we consider the case of a single-ended 1-b-per-stage pipelined ADC, where the first stage has a capacitor mismatch with $C_1 > C_2$ while the remaining 11 stages are ideal. The overall 12-b pipeline is schematically represented in Fig. 4-1.

We now examine the effect of a capacitor mismatch in the MSB stage. For comparison purposes, the conventional technique described in Chapter 3 is redrawn in Fig. 4-2(a). During the sampling phase, both the input voltage $V_{IN}$ and the offset voltage of the op-amp are sampled onto $C_1$ and $C_2$. For simplicity, $V_{OS} = 0$ is assumed. The case of $V_{OS} \neq 0$ will be dealt with in the next section on op-amp sharing technique. During the amplification phase, $C_1$ is selected as the feedback capacitor. Depending on the digital decision, $d$, $V_{REF}$ or GND is subtracted from the sampled input. The amplified residue voltage ($V_{RES}$) is shown in Fig. 4-3(a). Note that the slopes of the residue voltage are given by $(C_1 + C_2)/C_1$, regardless of whether $d = 0$ or 1. This is because a dedicated capacitor $C_1$ is used as the feedback capacitor. At the comparator decision boundary, as shown at the bottom of Fig. 4-3(a), the residue drop ($V_{drop}$), given by $V_a - V_b$, depends on the matching of the capacitors.

The significance of $V_{drop}$ becomes clear when two analog inputs $V_{IN} = V_{REF}/2 + \Delta_{in}$ and $V_{IN} = V_{REF}/2 - \Delta_{in}$ on either side of the decision point are considered. The quantity $\Delta_{in}$ represents a very small positive voltage compared with 1 LSB at 12-b level. Since the analog input barely changes, in order for the ADC to have a 12-b DNL, the two digital codes resulting from the two different analog inputs must not differ by more than 1 LSB. Referring to Fig. 4-3(a), when $V_{IN} = V_{REF}/2 - \Delta_{in}$, $d = 0$ and the residue $V_a$ should make the following 11-b ADC to produce an output code $= \{1,1,1,1,1,1,1,1,1,1,1\}$. When $V_{IN} = V_{REF}/2 + \Delta_{in}$, $d = 1$ and the residue $V_b$ ideally should make the following 11-b ADC to produce an output code $= \{0,0,0,0,0,0,0,0,0,0,0\}$. Therefore, to achieve 12-b DNL, the 11-b ADC must output codes that differ by the exact full scale. This means that $V_{drop}$ from the first stage must be exactly $V_{REF}$. Since the percentage mismatches $\epsilon_1$ and $\epsilon_2$ are random errors, the two cannot be expected to cancel each other. As a result, with conventional capacitor switching scheme as shown in Fig. 4-2(a), to satisfy the above condition requires 12-b capacitor matching for a 12-b DNL.

We now examine the proposed CFCS technique as shown in Fig. 4-2(b). During the sampling
phase, the input is sampled on both \( C_1 \) and \( C_2 \) as in the conventional case. But during the amplifying phase, when \( d = 0 \), \( C_1 \) is selected as the feedback capacitor; on the other hand, when \( d = 1 \), \( C_2 \) is selected as the feedback capacitor. The corresponding residue plot is shown in Fig 4-3(b). Since \( C_1 > C_2 \), we see that when \( d = 0 \), the residue voltage will be slightly smaller than ideal, resulting in a smaller slope. When \( d = 1 \), the residue voltage will be slightly larger than ideal, hence a steeper slope. Focusing on the decision point at \( V_{IN} = V_{REF}/2 \), it can be seen that, to either side of this boundary, the slopes of the residue voltage are changed in the opposite direction, yielding a residue drop \( V_{drop} \). This residue drop is, to first order, matched to \( V_{REF} \), the full scale of the following 11-b ADC. The error is only second-order, and a 12-b ADC requires only 6-7 b capacitor matching.

Fig. 4-4 (a) and (b) show the overall 12-b transfer curves of the conventional and the CFCS techniques, respectively. In Fig. 4-4(a), the thin dashed lines extending from the actual transfer curve show that the two segments have the same slope due to the use of a dedicated feedback capacitor in the conventional switching method. This results in a missing-code error. Using CFCS with the same mismatched capacitors, Fig. 4-4(b) shows that the first and the second
4.2. THE COMMUTATED FEEDBACK-CAPACITOR SWITCHING TECHNIQUE

\[
\begin{align*}
V_{\text{RES}} & = V_{\text{REF}} + V_a \\
V_{\text{REF}}/2 & \quad \text{Decision Point}
\end{align*}
\]

\[
\begin{align*}
C_1 & > C_2 \\
C_i & = C (1 + \epsilon_i)
\end{align*}
\]

\[
\begin{array}{c|c|c}
\text{d} & 0 & 1 \\
\hline
\text{Slope} & \frac{C_1 + C_2}{C_1} & \frac{C_1 + C_2}{C_1} < 2 \\
\end{array}
\]

\[
V_{\text{drop}} = V_a - V_b 
\leq V_{\text{REF}} \left( 1 - \frac{C_1 + C_2}{C_1} \right) < V_{\text{REF}}
\]

\[
V_{\text{drop}} = V_a - V_b 
\leq V_{\text{REF}} \left( 1 - \frac{C_1 + C_2}{C_1} \right) = V_{\text{REF}}
\]

(a) (b)

FIGURE 4-3: Residue plot comparison between (a) conventional and (b) CFCS techniques.

\[
\begin{align*}
\text{d}_{\text{out}} & = \text{d}_{\text{out}} \\
V_{\text{IN}} & \quad \text{MSB Decision Point}
\end{align*}
\]

\[
\begin{align*}
\text{Missing Codes at MSB} & \quad \text{with mismatch}
\end{align*}
\]

\[
\begin{align*}
\text{MSB Decision Point} & \quad \text{No Missing Codes}
\end{align*}
\]

(a) (b)

FIGURE 4-4: Transfer curve comparison between (a) conventional and (b) CFCS.
segments of the transfer curve have slopes that are respectively less than and greater than ideal. The missing code error at the MSB decision is eliminated.

In the previous discussion, the mismatch is such that $C_1$ is assumed to be slightly greater than $C_2$. In the case when $C_2$ is greater than $C_1$, the CFCS technique is equally valid. In this case the residue drop $V_{drop}$ is greater than $V_{REF}$ in the conventional case. If no digital error correction is used, the following stages of the pipeline will be saturated, resulting in wide codes as shown in the overall transfer curve in Fig. 4-5(a). With a similar mismatch using the CFCS technique, the wide codes are eliminated as shown in Fig. 4-5(b).

![Diagram](image)

**Figure 4-5:** Transfer curves when $C_2 < C_1$: (a) conventional and (b) CFCS.

From Fig. 4-4(b) and Fig. 4-5(b), it is clear that while the INL is commensurate to the capacitor matching, the DNL is significantly enhanced from the conventional case.

### 4.2.3 Digital Error Correction with CFCS

We have focused on the MSB stage in Fig 4-1. In practice, the CFCS technique can be applied to each of the following stages. For these later stages, a digital error correction technique can be used to accommodate the residue voltage, which can rise above or fall below the range of $[0, V_{REF}]$. In particular, the standard error correction method described in Section 3.3.4 in Chapter 3 requires a reduction of the stage gain by a factor of two. The gain reduction is typically achieved by using a dedicated feedback capacitor with a reduced input capacitor to the op-amp [11]. As a result, it cannot be used in conjunction with the CFCS technique. Instead, a true over-range error correction which employs two extra capacitors can be used.

For a 1-b-per-stage case, the circuit incorporating digital error correction is shown in Fig. 4-6.
During the sampling phase, the bottom plate of $C_1$ and $C_2$ are connected to the input as in a regular pipelined stage. Two extra capacitors $C_0$ and $C_3$ are added with their bottom plates connected to $V_{REF}$ and GND respectively. During the amplifying phase, the feedback capacitor are commutated from $C_0$ to $C_3$, depending on the digital decision which can range from $-1$ when the input is under-range to 2 when the input is over-range. Table 4-1 shows the connection of the four capacitors during the amplifying phase.

\[
\begin{align*}
V_{IN} & \quad \text{digital code} & C_0 & C_1 & C_2 & C_3 \\
-\frac{V_{REF}}{2} < V_{IN} \leq 0 & -1 & \text{FB} & \text{GND} & \text{GND} & \text{GND} \\
0 < V_{IN} \leq \frac{V_{REF}}{2} & 0 & V_{REF} & \text{FB} & \text{GND} & \text{GND} \\
\frac{V_{REF}}{2} < V_{IN} \leq V_{REF} & 1 & V_{REF} & V_{REF} & \text{FB} & \text{GND} \\
V_{REF} < V_{IN} \leq \frac{V_{REF}}{2} & 2 & V_{REF} & V_{REF} & V_{REF} & \text{GND}
\end{align*}
\]

Table 4-1: Capacitor connection during the amplifying phase in a digital correction stage.

Using charge conservation principle as demonstrated in Chapter 3, it can be shown that the two added capacitors in Fig. 4-6 produces $V_{drop}$ at all the decision points of GND, $V_{REF}/2$, and $V_{REF}$ that match with the full-scale of the following stages in the pipeline. Hence, the input voltage outside the range of [GND, $V_{REF}$] can be folded back into the normal range and the digital codes produced in the process can be used to correct the over-range.

One drawback of the circuit shown in Fig. 4-6 is that the feedback factor $f$ is reduced due to the added capacitors for digital error correction. This reduced feedback factor means that the speed of the op-amp will be correspondingly slower. Since the digital error correction is necessary only in later stages of the pipeline, this reduced $f$ does not have a large impact on the overall speed of the ADC. In Section 5.3 in the next chapter, an alternative digital error correction circuit without the reduced $f$ is presented.
4.2.4 Monte Carlo Simulation Results

The CFCS technique described above is general and can be applied to any number of bits per stage. A 2-b-per-stage case was analyzed both mathematically and via a Monte Carlo simulation in [39]. It can be shown that comparator offsets produce only second-order errors. To achieve 12-b DNL, 6-7 b capacitor matching and 6-7 b comparator offset are sufficient. The result of the Monte Carlo simulation is shown in Fig. 4-7 with a capacitor mismatch of 0.78% and a comparator offset of 1.56% of $V_{REF}$, both at the 3-$\sigma$ level. A yield of 95.2% is obtained at the 12-b 0.5-LSB level.

4.2.5 Added Advantage

Using the CFCS technique, it is theoretically possible to build uncalibrated ADC with resolution in the range of 14-16 b, provided that the capacitor matching accuracy is greater than 7-8 b. For this type of high-resolution ADC's, one source of errors of common concern is the capacitor nonlinearity [37][12].

Previous discussion assumes that each of the capacitors used in Fig. 4-2 is linear and hence its capacitance is independent of the voltage across it. When capacitor nonlinearity is considered, the CFCS technique shown in Fig. 4-9(b) has the interesting property that the residue drop $V_{drop}$ is, to first order, independent of the capacitor nonlinearity. Intuitively, this can be seen by examining Fig. 4-8 when $V_{IN} = V_{REF}/2$. In this case, when $d = 0$, $V_{RES} \approx V_{REF}$; when
4.2. The Commutated Feedback-Capacitor Switching Technique

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Amplification_Phase.png}
\caption{Voltage stress on both $C_1$ and $C_2$ remain unchanged when $V_{RES}$ changes from $V_{REF}$ to 0.}
\end{figure}

$d = 1$, $V_{RES} \cong 0$. Hence, at the decision boundary, although $V_{RES}$ changes from $V_{REF}$ to 0, the voltage across $C_1$ is always $V_{REF}$, while the voltage across $C_2$ is always 0, independent of $d$. Since the voltage stress across $C_1$ and $C_2$ remain unchanged at the decision boundary, the capacitor nonlinearity is canceled to first order.

In contrast, in the conventional case in Fig. 4-2(a), when $V_{RES}$ changes from $V_{REF}$ to 0, the voltage across the dedicated feedback capacitor $C_1$ changes, as does $C_2$. The capacitor nonlinearity effect is canceled only if the nonlinearity of the two capacitors match.

A more rigorous analysis for the 1-b-per-stage case is carried out in Appendix A. Although a 1-b-per-stage case is considered, a similar intuitive reasoning and analysis can be applied to the case when the stage resolution is greater than 1 b.

4.2.6 Comparison with Other Techniques

A similar technique applicable to only a 1-b-per-stage pipeline was independently proposed by [40]. Although similar, the technique presented by [40] is limited to a 1-b-per-stage architecture. In addition, it does not have the digital error correction capability shown in Fig. 4-6.

A number of other ratio-independent techniques [29][38][41][42] have been proposed previously. However, CFCS is superior to the known techniques in that it does not require additional clock cycles, and can be applied to both the pipelined (high-speed) architecture, or the cyclic (low-power) architecture. Therefore, the capacitors can be scaled down to the fundamental $kT/C$ noise limit. For a given conversion speed and resolution requirements, this allows for low-power small-area op-amps. Both the CFCS technique and the self-calibration techniques allow the capacitors to be scaled down to the $kT/C$ noise limit.

Table 4-2 gives a brief comparison of the CFCS technique with both analog e.g. [3] and digital e.g. [12] self-calibration techniques. The primary advantage of the CFCS against the self-calibration techniques is that the ADC does not have to be interrupted for calibration. The primary advantage self-calibration techniques have over the CFCS is that in addition to the DNL, they also improve the INL beyond the capacitor matching accuracy.
4. Low-Power Design Techniques for Pipelined ADC's

<table>
<thead>
<tr>
<th>Require extra analog hardware?</th>
<th>analog calibration</th>
<th>digital calibration</th>
<th>CFCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Require calibration logic/memory?</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Need interruption for calibration?</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Improve the INL?</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Table 4-2: Comparison between the CFCS and the self-calibration techniques.

4.3 Op-amp Sharing Technique

Whereas the CFCS technique described in the previous section minimizes power by minimizing the capacitive load of the op-amps, the op-amp sharing technique minimizes power by reducing the effective number of the op-amps used in the entire pipeline. This technique is described in this section.

4.3.1 Motivation

In a pipelined ADC, during the odd phases, the odd stages are sampling, while the even stages are amplifying. During the even phase, the roles of the odd and the even stages interchange. During the sampling phase, both the analog input and the op-amp offset are sampled. In a conventional switching scheme depicted in Fig. 4-2, the op-amp is in a unity-gain configuration for the offset to be sampled. Another common offset-cancellation technique is the addition of an auxiliary amplifier to store the offset as described in Section 3.4.2. In either case, the op-amp power during the sampling phase is used solely for the purpose of offset cancellation.

If the op-amp does not need to be offset-canceled, adjacent stages of the pipeline can share one op-amp, resulting in the use of half the number of op-amps. In the technique described below, approximately 40% of the effective number of op-amps can be reduced, resulting in a large saving in the power consumption, while offset cancellation is maintained.

4.3.2 Principle of Operation

The proposed op-amp sharing method is shown in Fig. 4-9. During the odd phase, the op-amp labeled $a_{1o}$, used for the odd stage of the pipeline, is in the sampling mode. At the same time, the even stage is in the amplifying mode. A two-stage op-amp design is used, consisting of $a_{1e}$, which is identical to $a_{1o}$, and $a_2$. This second stage of the op-amp, $a_2$, is shared between adjacent stages of the pipeline so that when the phase changes to even, $a_2$ is switched from the even stage to the odd stage. To push out the non-dominant pole, $a_2$ is typically designed to consume more current than $a_{1o}$ and $a_{1e}$. Assuming $a_2$ consumes four times as much current as $a_1$, the op-amp sharing technique will achieve a power saving of 40%.

During the odd phase, the op-amp $a_{1o}$ is in a unity feedback configuration where the output
is directly connected to the inverting input of the op-amp at virtual ground. Therefore, very little voltage swing is required. As a result, a cascode op-amp topology can be used to achieve high DC open-loop gain without being penalized for output voltage swing reduction. The offset of \(a_{1o}\) that is sampled during the odd phase is offset-canceled during the even phase as shown in Section 3.3.5. The offset of \(a_2\), although not sampled, is divided by the high gain of \(a_{1o}\) when referred to the input of the two-stage op-amp. Since \(a_{1o}\) and \(a_{1e}\) already produce large DC open-loop gain, the DC gain of \(a_2\) can be small. This allows \(a_2\) to use a non-cascoded topology which achieves high swing. The advantage of the high output swing is explained in more detail in Section 4.3.5.

### 4.3.3 Common-Mode Settling Time Considerations

In addition to the output common-mode feedback circuit for \(a_2\), \(a_{1o}\) and \(a_{1e}\) have their own common-mode feedback circuit as will be shown in Section 4.4. The common-mode feedback circuit is typically designed to have a comparable settling time as the differential-mode signal. Therefore, the common-mode disturbance due to the switching of \(a_2\) in and out of the op-amp settles out quickly.

### 4.3.4 Differential-Mode Settling Time Considerations

For common-mode settling, the absolute accuracy is not critical, provided that the op-amp output voltage dynamic range is not affected. In contrast, since the differential signal is the signal of interest, it does have more stringent settling requirement compared with the common-mode signal. In this case, second-order effects such as finite ON-resistance of the switches can be of importance. One example is the switch used to switch \(a_2\) in and out of the op-amp. If the switch is too small, the large ON-resistance could add excessive phase shift that degrades the settling time. If the switch is too large, the extra parasitic capacitance can also degrade the settling time. SPICE simulation program can be used to find the optimum size or the switch for the shortest settling time.

### 4.3.5 Added Advantage

The partition of the op-amp has an added advantage because of the use of a two-stage op-amp. In a 12-b ADC, the op-amp open-loop gain should typically be greater than 12,000 (Section 3.3.1) with a maximum output swing to maximize the SNR. This swing requirement is especially critical in a low-supply design where the available swing is limited. In modern VLSI processes, the low intrinsic gain of the MOS devices usually requires cascoding to achieve the required gain of 12,000. Unfortunately, cascoding reduces swing. By using a high swing output stage for the op-amp with no cascode, the op-amp dynamic range is maximized. This wide
Figure 4-9: Op-amp sharing technique results in about 40% saving in power.
dynamic range allows the ADC to operate at a supply voltage down to 2.5 V and still maintain the required accuracy.

4.3.6 Comparison with Other Techniques

For a cyclic ADC, a similar op-amp sharing idea was proposed by [43]. While an excellent technique for cyclic converters, this technique requires an auxiliary amplifier for the offset cancellation. When applied to a pipelined ADC, it consumes unnecessarily large amount of power.

4.4 Reusing the First Stage of an Op-Amp as a Comparator Pre-Amp

In the previous section, power saving is accomplished by sharing the second stage of the op-amp between the adjacent stages of the pipeline. In this section, power saving is accomplished by reusing the first stage of the op-amp as a comparator pre-amp. This technique is described in this section.

4.4.1 Motivation

Although the CFCS technique is tolerant to comparator offsets, having small comparator offset allows the residue voltage to exceed the full scale by only a small amount. This reduced over-range requirement allows a larger full scale for a given op-amp output voltage swing and improves the SNR. In addition, since the offset of the latch can be larger, power dissipation is reduced. Since a careful examination of the op-amp topology yields a pre-amp that already exists for free, this pre-amp is used to reduce the comparator offset when referred to the input of the pre-amp.

4.4.2 Principle of Operation

As shown in Fig. 4-9 in Section 4.3, during the sampling phase, the op-amp has only one stage. The circuit schematic for $a_1$ is shown in Fig. 4-10(a). Since the op-amp is fully differential, a common-mode circuit, also shown in Fig. 4-10(a), is used. Transistors M5 and M6 are used to sense the output common-mode voltage of op-amp $a_1$, while M7 is used to apply the feedback signal $V_1$ to the op-amp so as to set the common-mode to the desired $V_{CMR}$. Used as a common-mode circuit, the drain of M5 and M6 are typically tied to the supply and their output $V_2$ is wasted. With the addition of two resistors as shown in Fig. 4-10, M5 and M6 double as the second stage of a two-stage differential pre-amp for the comparator. As shown in Fig. 4-10(b), once the input is sampled, the one-stage op-amp goes into open loop. By grounding the bottom-plates of $C_1$ and $C_2$, the inverted input is offset-canceled and applied to the pre-amp. The first
**Figure 4-10:** Reusing the first stage of an op-amp as a comparator pre-amp:
(a) Circuit schematics (b) Block diagram.
stage of the pre-amp was previously the op-amp \( (a_1) \), while the second stage of the pre-amp was the common-mode circuit \( (a_{1CM}) \). The output of this two-stage pre-amp, \( V_2 \), is applied as the input to the latch. Since an op-amp in an open loop can be slow, a resistor at the output of \( a_1 \) is switched in to reduce the op-amp open-loop gain when the op-amp is reused as a comparator pre-amp. Because the resistor is across the output, the differential offset of \( a_1 \) is not effected.

### 4.4.3 Added Advantage

In many previously reported pipelined ADC e.g. [3], the first stage of a pipeline is an explicit sample-and-hold stage, employing a single sampling capacitor (Fig. 3-3). The gain-of-one sample-and-hold stage contributes \( kT/C \) noise, requiring larger capacitors both in the sample-and-hold stage and in the following stages of the ADC. Since the configuration shown in Fig. 4-10(b) performs an implicit sample-and-hold function, the explicit gain-of-one sample-and-hold stage can be eliminated.

To see how much power can be saved when the explicit sample-and-hold can be eliminated, consider first a 1-b-per-stage pipeline where all the stages are identical. Let \( v_{n1}^2 \) be the noise contribution from the first stage of the pipeline. Following the noise analysis outlined in Section 3.4.6, in the limit when the number of pipelined stages approaches infinity, the total input referred noise of the ADC is given by:

\[
\overline{v_{tot1}^2} = \overline{v_{n1}^2 (1 + \frac{1}{4} + \frac{1}{16} + ....)} = \frac{7}{3} \cdot \overline{v_{n1}^2}
\]

(4.1)

In contrast, when the explicit sample-and-hold is eliminated, the total input referred noise of the ADC is given by:

\[
\overline{v_{tot2}^2} = \overline{v_{n2}^2 (1 + \frac{1}{4} + \frac{1}{16} + ....)} = \frac{4}{3} \cdot \overline{v_{n2}^2}
\]

(4.2)

Equating the noise given by Equation (4.1) and Equation (4.2), it can be shown that

\[
\frac{\overline{v_{n1}^2}}{\overline{v_{n2}^2}} = \frac{4}{7}
\]

(4.3)

Equation (4.3) implies that when an explicit sample-and-hold stage is eliminated, the sampling capacitance of each pipelined stage can be 43% smaller. Hence, the widths of the transistors as well as the current can be both reduced by 43%.

In the previous analysis, the pipelined stages are assumed to be identical. When each of
the pipelined stages are scaled down by a factor of two from the previous pipelined stage in a 1-b-per-stage case, a similar analysis can be performed. In this case, the ratio of $v_{n1}^2$ to $v_{n2}^2$ is 0.67. Hence, the elimination of an explicit sample-and-hold stage results in a power saving of 33%.

For larger number of bits per stage, since the contribution from the following stages is negligible, the power saving can approach 50%.

The timing necessary to implement this technique requires that the digital decision be carried out after the sampling phase, while the timing for the pipeline requires the digital decision to be ready at the onset of the amplifying phase. Hence a pseudo phase is necessary between the sampling and the amplifying phases. This added phase will be referred to as the comparison phase. For a conversion rate of 5 Msample/s, each phase is 100 ns. For a comparison time of 10 ns, the additional penalty of 10% is a small price to pay for the advantage of power saving. A more detailed description of the comparison phase is given in Section 5.2.4. The pseudo phase scheme has the added advantage that the follower circuit used to prevent the kickback of the latch [9] can be eliminated. This point is explained in Section 5.2.3.

4.5 Exploiting Parasitic Capacitors

The common-mode feedback circuit of $a_2$, the second stage of the op-amp, is implemented by exploiting existing parasitic capacitors which would otherwise load the amplifier. This technique is described in this section.

4.5.1 Motivation

In a typical pipelined ADC, the total op-amp load capacitance consists of three components: the sampling capacitance, the common-mode feedback capacitance, and the parasitics from the various devices connected at the output. In a two-stage design, a pole-splitting compensation capacitor ($C_c$) is used as shown in Fig. 4-11. The bottom-plate of $C_c$ is typically connected to the output of the op-amp and therefore adds additional loading to the output.

4.5.2 Principle of Operation

As will be explained in more detail in Section 5.2.2, during the comparison phase when the second stage of the op-amp is not in use, the switches shown in Fig. 4-11 are closed. In this case, the inputs and outputs are shorted to the common-mode voltage $V_{CM}$, while the gates of the PMOS load are shorted to the voltage $V_{P Bias}$. A PMOS diode-connected transistor is used to generate a $V_{P Bias}$ so that each of the PMOS devices is biased at half of the tail current. In this manner, the desired voltage difference between $V_{CM}$ and $V_{P Bias}$ is stored on the common-mode feedback capacitors.
By inserting a well underneath the capacitor, and connecting this well to the gates of the PMOS load as shown, the parasitic capacitance from the bottom plate of the compensation capacitor to this well can be exploited as part of the common-mode feedback capacitor for the second stage of the op-amp.

The switches shown in Fig. 4-11 are open during the normal mode of operation. When the common-mode output is too high, the common-mode feedback capacitors act as a DC level shifter, pulling up the gates of the PMOS devices. This, in turn, decreases the common-mode output voltage back to the desired $V_{CM}$.

In this manner, the bottom-plate parasitics from $C_c$ is exploited as common-mode feedback capacitors. Power saving is achieved by reducing the total load capacitance and hence power consumption by approximately 20% while maintaining the same settling time.

4.5.3 Common-Mode Settling Consideration

The sheet resistance of the well is typically on the order of 2 $\Omega/\square$. Since the well is inserted underneath a square capacitor, the well presents approximately 2 $\Omega$ of series resistance when
considered as a lumped resistance. Together with a worst-case capacitance of 5 pF, the pole associated with the RC circuit is at 16MHz. If the unity-gain frequency of the common-mode circuit is also at 16MHz, the resulting phase margin of 45 degrees is more than sufficient for a 5-MHz ADC. When modeled as a distributed RC circuit, the phase shift is less than the lumped RC circuit until a frequency that is a few times 16 MHz. So again, for 5-MHz operation, the effect of well resistance on the common-mode settling is not critical.

4.6 Summary

In this chapter, a set of power minimization techniques for pipelined ADC's is described. The first is a commutated feedback capacitor switching (CFCS) scheme that achieves 12-b resolution while using only 6-7 b accurate capacitors. The second technique is an op-amp sharing method that reduces power consumption by as much as 40%. The third technique saves power by reusing the first stage of an op-amp as a pre-amp for the comparator. The fourth technique exploits parasitic capacitors as the common-mode feedback capacitors, resulting in a reduced op-amp power consumption for the same settling speed.
Prototype Design

5.1 Introduction

A prototype pipelined ADC incorporating the power reduction techniques outlined in Chapter 4 was implemented in a 1.2-μm N-well double-metal double-poly technology. In Section 5.2, a detailed description of the major circuit components is discussed. In Section 5.3, implementation issues related to the digital error correction stage are presented. Section 5.4 describes issues that arise when analog and digital circuits co-exist on the same chip. Methods to overcome these problems are also described. In Section 5.5, testability considerations related to the layout of the test chip are presented, followed by a description of the actual chip layout in Section 5.6.

5.2 Design of the Major Circuit Components in the Pipelined ADC

5.2.1 General Description

The test chip consists of 15 stages, of which three are for digital error correction and will be described in Section 5.3. While each of the three digital error correction stages produces two raw codes corresponding to over- and under-range, the remaining 12 stages are regular, producing 1 b per stage. The digital error correction stage is inserted every 3-5 stages of the pipeline as will be explained in Section 5.3.

The use of the op-amp sharing technique described in Chapter 4 results in two adjacent stages of the pipeline being grouped as a set. The first set of two pipelined stages and the second set of two pipelined stages together determine the first four MSB's of the ADC. Since later stages of the pipeline can tolerate more error and $kT/C$ noise, they are made smaller. The
unit sampling capacitors are 0.5 pF for the first two stages, 0.25 pF for the next two stages and
0.125 pF for all later stages. Since the capacitive load is scaled down as the signal propagates
down the pipeline, the op-amps are also scaled down in width and current proportionally.
This constant-current-density scaling results in the op-amp of each pipelined stages having
similar settling characteristics and hence minimizes the design time. In addition, this scaling
of the pipelined stages allows power saving by approximately a factor of two compared with an
unscaled pipeline.

One of the most critical components in a pipelined ADC is the op-amp. As described in
Chapter 3, for a given ADC resolution and conversion speed, the op-amp must have sufficient
dc open-loop gain and be able to settle quickly. In addition, the op-amp must have a large
output voltage swing so that the SNR of the ADC can be maximized. In a low-supply ADC,
it is extremely challenging to design an op-amp that satisfies all of these requirements. In the
next section, the op-amps used for the test chip will be described.

5.2.2 Op-Amp Topology

Description of \( a_{1} \) Each set of two adjacent pipelined stages uses two op-amp first stages
\( (a_{1o} \text{ and } a_{1e}) \) and one op-amp second stage \( (a_{2}) \) as illustrated in Fig. 4-9 in Chapter 4. For the
first four stages of the pipeline, double cascode consisting of MP1-2, MP3-4, and MP5-6 are
used for the PMOS side as shown in Fig. 5-1. For the NMOS side, a cascode circuit consisting
of MN1-2, and MN3-4 are used together with a gain-enhancement amplifier to form an active
cascode. The first stage op-amp dc open-loop gain is approximately 1,000. The use of an
unfolded cascode pushes the non-dominant pole to a high frequency [8]. The use of NMOS
devices as the input differential pair results in a high \( g_{m} \). These two factors combine to achieve
a fast settling time.

The gain-enhancement amplifier, shown in Fig. 5-2, consists of MNX1-2 cascoded with
MNX3-4 and loaded by PMOS current source MPX1-2. Transistor MNX5 is used for the
common-mode feedback of the gain-enhancement amplifier. When the common-mode of the
input signals auxi+ and auxi− are too high, the common-mode of the output signals auxo+ and
auxo− decreases. This output common-mode is fed back through MN3-4 (Fig. 5-1), bringing
the common-mode of the input signals auxi+ and auxi− back down.

Common-Mode Feedback Circuit for \( a_{1} \) For the first stage of the op-amp \( a_{1} \), the common-
mode feedback circuit \( a_{1CM} \) shown previously in Fig. 4-10(a) is shown in Fig. 5-1 in more
detail. As described in Chapter 4, when the common-mode output of \( V_{o1+} \) and \( V_{o1−} \) is too
high, transistors MN5 and MN6 steer current away from MN7. The gate voltage of the diode-
connected transistor MP9 goes up which brings the gate voltage of MP1-2 up, decreasing the
common-mode output voltage back to the desired \( V_{CM} \).

To ensure common-mode stability, the PMOS current source load MP1-2 in Fig. 5-1 is split
Figure 5-1: Schematic of the first stage of the op-amp.
into two. The reduced $g_m$ increases the phase margin of the common-mode feedback loop and improves the common-mode stability.

Compared with Fig. 4-10(a), the common-mode circuit in Fig. 5-1 contains additional transistors MN8-9, which are used as a cascode to avoid the Miller effect. These two transistors are biased by MN13 and MN13b.

As Chapter 4 indicates, the output of MN5-6 are typically wasted when used as a common-mode circuit. To implement the reuse of the op-amp as a comparator pre-amp, transistors MN12-13 are used to implement the resistive load. For ease of testing, the digital supply for the latch is at a higher voltage than the analog supply for the comparator pre-amp. Transistor MP8 is used to drop enough voltage so that the pre-amp common-mode output of $V_{2+}$ and $V_{2-}$ is not too high to force the PMOS tail current source MP5 in Fig. 5-7 into the triode region.

As described in Section 4.4, during the comparison phase, op-amp $a_1$, which is reused as a comparator pre-amp, is in an open loop. To speed up the comparison time, a resistor implemented with an NMOS transistor in the triode region is connected across the output terminals $V_{o1+}$ and $V_{o1-}$ to reduce the open-loop gain of the op-amp during the comparison phase.
Bias Circuit for $a_1$ The circuit for the generation of Bias1-7 is shown in Fig. 5-3. The tail current source MN10 (Fig. 5-1) for the input differential pair in $a_1$ is biased by an on-chip diode-connected MNB1. A similar diode-connected transistor MNB2 is used to generate Bias2 which biases the tail current transistor MN11 (Fig. 5-1) for $a_{1CM}$. Both MNB1 and MNB2 are themselves biased with external current sources. The implementation of external current sources is described in Section 6.2.3.

![Bias Circuit Diagram](image)

**Figure 5-3**: Bias circuit for the first stage of the op-amp.

From the diode-connected MNB1 and MNB2, Bias3-7 are generated by using current mirrors. In particular, Bias3 and Bias4 for the double PMOS cascode in $a_1$ are generated by transistors MPB1 and MPB2. For a transistor to be in the saturation region, its $V_{DS}$ must be at least $\Delta V = V_{GS} - V_T$. To satisfy this requirement, transistors MPB1 and MPB2 are about 16 and 8 times smaller respectively than the transistors MP5-6 and MF3-4 (Fig. 5-1) they bias. These factors allow safety margins of $(\sqrt{8} - 2)\Delta V$ for MP1-2 and $(\sqrt{16} - 3)\Delta V$ for MP3-4 to be in the saturation region. Transistors MNB8 and MNB9 are used to match the $V_{DS}$ of MN10 (Fig. 5-1) to those of MNB3 and MNB4. In this manner, the bias currents of MP3-4 and MP5-6 (Fig. 5-1) match that of MPB1 and MPB2, independent of the channel length modulation effects. This matching ensures that the safety margins mentioned above are not compromised. A similar set of considerations applies to Bias5-7 generated by transistors MPB3, MPB4 and MPB5 respectively.

For the first four MSB stages of the pipeline, two sets of the bias circuit described above is used, one for each set of two pipelined stages. For later stages, since more errors can be tolerated, one bias circuit is shared with several pipelined stages.
Description of \( a_2 \)  The op-amp sharing technique described in Chapter 4 enables the use of a simple second stage of the op-amp as shown in Fig. 5-4. The non-cascoded topology achieves high swing and allows the ADC to operate down to a 2.5-V supply while maintaining a high SNR. The gain from the second stage op-amp is approximately 10. Pole-splitting compensation [13] is used with a capacitance of 1.4 pF together with a nulling resistance of 250 \( \Omega \). The nulling resistors are implemented with NMOS transistors.

\[
\begin{align*}
V_{\text{dd}} & \quad \text{MP3} \quad 390/1.2 \\
0.25 \text{pF} & \quad \text{MP4} \quad 390/1.2 \\
1.4 \text{pF} & \quad \text{C}_{\text{CM1}} \\
1.4 \text{pF} & \quad \text{C}_{\text{CM2}} \\
250 \Omega & \quad \text{MN1} \quad 256/1.2 \\
250 \Omega & \quad \text{MN2} \quad 256/1.2 \\
1.4 \text{pF} & \quad \text{MN3} \quad 1024/1.2 \\
1.4 \text{pF} & \quad \text{MN\text{mirror}} \quad 512/1.2
\end{align*}
\]

**Figure 5-4:** Schematic of the second stage of the op-amp.

Before describing the common-mode feedback circuit for \( a_2 \), the timing scheme used will be briefly described. In a conventional pipelined ADC, the comparison is usually carried out during the amplifying phase. Due to the reuse of the op-amp as a comparator pre-amp as described in Section 4.4, a pseudo two-phase timing scheme shown in Fig. 5-5 is instead used for the prototype. The separate time slot labeled \( \phi_x \) is used by the comparator. A more detailed description of the timing scheme will be described in Section 5.2.4 along with the clock.
generator circuit.

![Timing Scheme](image)

**Figure 5-5: A Pseudo two-phase timing scheme.**

The common-mode feedback is accomplished by shorting both the input and output terminals to \( V_{CM} \) when \( a_2 \) is not in use. This occurs during \( \phi_2 \) when \( a_2 \) is neither used by the odd nor the even stages of the pipeline. In addition, the gates of MP3-4 are also shorted to a bias voltage generated by MPbias. The difference in voltage between \( V_{CM} \) and this bias voltage is stored on the common-mode feedback capacitors \( C_{CM1-2} \). As described in Chapter 4, these common-mode feedback capacitors are implemented with the parasitic capacitance from the bottom plates of \( C_c \) to the well inserted beneath \( C_c \).

When \( a_2 \) is used by an odd stage of the pipeline during \( \phi_2 \) or by an even stage of the pipeline during \( \phi_1 \), all of the switches controlled by \( \phi_x \) in Fig. 5-4 are turned off. If the common-mode output voltage is too high, \( C_{CM1-2} \) serve as level shifters so that the gate voltage of MP3-4 is also too high. This brings the output common-mode voltage back to the desired level.

**Op-amps for Later Stages of the Pipeline** For the third and fourth MSB stages of the pipeline, the op-amps are scaled down in transistor width and current by a factor of two from the first two MSB stages of the pipeline. Thereafter, for later stages of the pipeline, the op-amps are scaled down in width and current by an additional factor of two from the third and fourth MSB stages. For these later stages, the op-amp DC open-loop gain requirement is smaller compared with the MSB stages. As a result, rather than using the design shown in Fig. 5-1 for the first four MSB stages of pipeline, the first stage of the op-amp has a double PMOS cascode and an NMOS cascode as shown in Fig. 5-6. The gain-enhancement amplifier in Fig. 5-1 for the NMOS cascode circuit is eliminated. For clarity, the common-mode feedback circuit, which is similar to that used in Fig. 5-1, is not shown in Fig. 5-6. The second stage of the op-amp for these later stages of the pipeline uses the same design as that shown in Fig. 5-4 but scaled in transistor width and current.
Figure 5-6: Schematic of the first stage of the op-amp for later stages of the pipeline.

5.2.3 Comparator Latch Circuit

The latch circuit is shown in Fig. 5-7. When the strobe signal is high, transistors MN3 and MN3b are ON and the latch is reset. To make a comparison, the differential output of \( V_{2+} \) and \( V_{2-} \) from Fig. 5-1 is applied to transistors MP1-2. When the strobe goes low, MN3 and MN3b are turned off, and the positive feedback of MP3-4 and MN4-5 cause the circuit to regenerate rapidly.

During the fabrication process, the 7-degree ion implantation angle for the source and drain can make the otherwise symmetrical MOS device asymmetrical. When MN3 is turned off, this asymmetry leads to asymmetrical charge injection and clock feedthrough, and can result in a large input referred offset. To minimize this asymmetry, MN3b, which is identical to MN3 in geometry, is added with its drain terminal connected to the source terminal of MN3 and vice versa so that the parallel combination of the two transistors is symmetrical.
As indicated in Section 5.2.2, in a conventional pipelined ADC, the comparison is usually carried out during the amplifying phase. In contrast, due to the reuse of the op-amp as a comparator pre-amp as described in Section 4.4, a separate time slot is used for the comparison. The pseudo two-phase timing scheme shown in Fig. 5-5 has the added advantage that since the latch is not strobed while the op-amp is settling, no follower for the latch is necessary to prevent the kickback of the latch.

![Diagram of comparator latch](image)

**Figure 5-7: Schematic of the comparator latch.**

### 5.2.4 Clock Generator

As indicated in the previous section, the timing circuit used is a pseudo two-phase clock. For a 5-Msample/s operation, each of the two non-overlapping phases is 100 ns in duration. For each non-overlapping phase, about 9 ns is allocated for the comparator during the $\phi_k$ phase, leaving about 89 ns for the op-amp to settle. The remaining 2 ns is consumed by the non-overlapping period of the clock.

The clock generator is shown in Fig. 5-8. Shown in the lower left corner is the basic two-phase clock generator. Using two NAND gates that are buffered and cross-coupled, the master clock supplied from off-chip is converted to the two non-overlapping phases $\phi_{1nv}$ and $\phi_{2nv}$. From the signals $\phi_{1nv}$ and $\phi_{2nv}$, the length of the comparison phase $\phi_k$ is determined by a variable delay circuit shown in the upper left corner of the schematic. The delay is implemented with a cascade of inverters each of which is loaded by a capacitor. The effective capacitance seen
Figure 5-8: Gate-level diagram of the clock generator.
5.2. Design of the Major Circuit Components in the Pipelined ADC

![Timing Diagram]

- $\phi_{1\text{nv}}$
- $\phi_{2\text{nv}}$
- $\phi_{1\text{+}}$
- $\phi_{1-}$
- $\phi_{x}$
- strobe_odd
- $\phi_{2\text{+}}$
- $\phi_{2-}$
- $\phi_{2}$
- strobe_even

For op-amp settling:

- ~ 89 ns

For comparison:

- ~ 9 ns

Figure 5-9: The pseudo-two-phase timing diagram.
by each inverter is controlled with a series transistor. By increasing the gate control voltage $V_c$ for the series transistors, the comparison time can be increased to about 14 ns. When the comparison time increases to 14 ns, the logic on the right half of Fig. 5-8 automatically decreases $\phi_1$ and $\phi_2$ to about 84 ns. For testability, if additional comparison time is needed, larger on-chip capacitor can be switched into the inverter output with a laser cut.

The clock generator generates the necessary clock phases shown in Fig. 5-9. $\phi_{1+}$ and $\phi_{2+}$ are the advanced versions of $\phi_1$ and $\phi_2$ respectively. They are used to turn off the feedback sampling switch as described in Section 3.3.6. The latch circuit shown in Fig. 5-7 is triggered by the falling edge of the signal strobe_odd or strobe_even, depending on whether the pipelined stage is odd or even. The latch is reset during the following $\phi_x$ phase when the strobe signal returns to the high state.

### 5.3 Digital Error Correction

A conventional digital error correction scheme was described in [11] where codes from adjacent stages are overlapped by 1 b. This conventional scheme is not compatible with the CFCS technique as described in Section 4.2.3. A true over-range digital error correction implementation using only two extra capacitors is shown in Fig. 4-6 in the previous chapter. For reasons to be described below, a new digital error correction scheme is used in the final test chip. Before describing this new digital error correction scheme, the placement of the digital error correction stages in the pipeline is first addressed.

#### 5.3.1 Placement of the Digital Error Correction Stages in the Pipeline

In a pipelined ADC with no digital error correction, any capacitor mismatch or any offset in a comparator or an op-amp will result in a residue that is outside of the full-scale range. In a true over-range digital error correction scheme such as that described in Section 4.2.3, the residue signals are allowed to propagate down the pipeline without any digital error correction for a few stages. As the residue voltage goes too far outside of the full-scale range, a digital error correction stage such as that shown in Fig. 4-6 can be inserted into the pipeline to bring the residue back to within the full-scale range. One of the considerations in designing the over-range digital error correction stage is therefore the placement of this stage in the pipeline.

Placing the digital error correction stage too late in the pipeline risks the danger of saturating the op-amp voltage output dynamic range. On the other hand, placing the digital error correction stage too early in the pipeline requires extra stages in the pipeline for redundancy and consumes extra power. A similar consideration holds for each of the later digital error correction stages.

Since the offset of the op-amp is canceled and the offset of the comparator is reduced by the use of the pre-amp as described in Chapter 4, the capacitor mismatch is assumed to be
the primary cause of the residue voltage falling outside of the full-scale range. In this case, the placement of the first digital error correction stage is evaluated as follows. A worst-case mismatch of ±0.78% at 3-σ level is assumed for the 0.5-pF unit capacitor used in the first two pipelined stages. From the \( kT/C \) noise analysis given in Section 3.4.6, a 1-V peak-to-peak signal on each side of the differential input is sufficient to achieve the required SNR for a 12-b ADC. From a 2.5-V supply, the output stage of the op-amp shown in Fig. 5-4 is estimated to have about 1.6 V of output swing on each side of the differential output. Hence, the first digital error correction stage must be inserted into the pipeline before the op-amp saturates. This occurs at the fifth stage of the pipeline where the expected worse-case maximum op-amp output range is given by

\[
V_0 = \left(1 + \frac{2}{0.78\%} \cdot 2^5 \right) \cdot 1 \text{ V}
\]

positive and assumed capacitor mismatch for the MSB stage
-negative single-sided signal swing
input gain after 5 stages

\[
= 1.5 \text{ V} \quad (5.1)
\]

From Equation (5.1), since the op-amp output dynamic range is about 1.6 V, there is a 50-mV safety margin for each of the supply rails.

The later digital error correction stages can be similarly considered. As mentioned in Section 5.2, after the first four MSB stages, the capacitors are scaled down by a factor of four from those used in the MSB stage. For these small capacitors, as the size of the capacitors is scaled, the percentage mismatch is scaled as given by [44]

\[
\frac{\Delta C}{C} \propto C^{-\frac{3}{4}} \quad (5.2)
\]

Based on Equation (5.2), the 0.78 % mismatch for the 0.5-pF capacitors used in the MSB stage of the pipeline, when scaled down to 0.125 pF, will have a mismatch given by

\[
\frac{\Delta C}{C} = 0.78\% \cdot 4^{\frac{3}{4}} \\
= 2.21\% \quad (5.3)
\]

Using the percentage mismatch determined in Equation (5.3), a similar consideration can be applied for the later digital error correction stages. It is determined that a total of three digital correction stages are used for the entire pipeline. The second and third digital error correction stages are inserted every three stages of the pipeline. The placement of the digital
error correction stages is shown in Fig. 5-10.

![Stage Diagram]

**Figure 5-10:** Placement of the error correction stages in the pipeline.

### 5.3.2 A New Digital Error Correction Scheme

Although only two extra capacitors are necessary to implement the digital error correction scheme as shown in Fig. 4-6 in Chapter 4, the feedback factor \( f \) is decreased. This decreased feedback factor necessitates a redesign of the op-amp to meet the settling time requirement. In addition, the two extra comparators at \( V_{REF} \) and \( -V_{REF} \) also need two extra pre-amps. Since each pipelined stage uses only one first stage of the op-amp, this poses a difficulty in resuing the op-amp as the comparator pre-amp.

![Residue Plot]

**Figure 5-11:** Residue plot of the digital error correction stage.

The alternative technique calls for a sample-and-hold operation when the signal is within the full-scale range, deferring the usual digital decision at \( V_{IN} = V_{REF}/2 \) until later stages. Depending on whether the residue is over- or under-range, a full-scale voltage is either subtracted or added to fold the residue back to within the full-scale range. The resulting residue is as shown in Fig. 5-11, where the dashed line represents the case of sampling-and-holding without over-ranging, while the two big arrows represent the action of the digital error correction circuit that brings the residue back to within the full-scale range. For a 1-b-per-stage case, the code
values assigned to the under- and over-range are \(-1\) and \(2\) respectively. Since the digital error correction has a gain of one, the codes will be binary weighted equally as the code from the stage that immediately follows.

### 5.3.3 Circuit Implementation

The circuit implementation is shown in Fig. 5-12. During the sampling phase, \(C_2\) and \(C_4\) are connected to \(V_{IN}\), while the bottom plates of capacitors \(C_1\) and \(C_3\) are connected to \(V_{REF}\) and GND respectively. Since only \(C_2\) and \(C_4\) are connected to \(V_{IN}\), the previous pipelined stage is still driving the same amount of capacitive load as a regular stage.

![Circuit Diagram](image)

**Figure 5-12:** Implementation of the digital error correction stage.

During the comparison phase, the bottom plates of \(C_1\) and \(C_2\) are connected to \(V_{REF}\), while the bottom plates of \(C_3\) and \(C_4\) are connected to GND. The resulting signals at the respective input of the op-amp \(a_1\) will be offset canceled as described in Section 4.4. In this manner, each of the two op-amps is reused as the comparator pre-amp for its own respective latch to arrive
at the over- and under-range decisions \( d_+ \) and \( d_- \).

During the amplification phase, one of the two \( a_1 \)'s is selected to combine with the second-stage of the op-amp, depending on the over and under-range decisions. When it is neither over- or under-range, then either one of the two \( a_1 \)'s can be chosen to combine with \( a_2 \) to form a two-stage op-amp. As indicated in Fig. 5-12, the bottom \( a_1 \) is combined with \( a_2 \) when the under-range is not true. In either case, note that the feedback factor remains the same as that for a regular stage.

5.4 Mixed-Signal Design Issues

As digital and analog systems are integrated into one chip, many challenges arise. In this section, some of the design considerations in a mixed-signal environment is presented.

5.4.1 Substrate Coupling

Since the substrate is common to both the analog and the digital circuits, digital circuit switching activities that couple to the substrate can degrade the analog circuit performance. Conventional wisdom calls for physical and chronological separation. In the physical separation scheme, the analog systems are placed as far as possible from the digital systems to minimize the substrate coupling. The physical separation also reduces the coupling through fringing fields. In the chronological separation scheme, the timing of the digital and analog circuits are separated. One example is to sample the analog signal when the digital activities are at a minimum [45].

In traditional CMOS technology where the substrate is lightly doped, the substrate contacts can be used profusely to quiet down the substrate by reducing the effective substrate resistance. In addition, the high resistance substrate does not damp the noise effectively so physical separation can help. Recent advances in process technology has resulted in the use of lightly doped epi layer on a heavily doped substrate to reduce latch up. In this kind of technology, since the substrate is already of low resistance, prefuse substrate contacts do not reduce the substrate coupling significantly. For the same reason, physical separation greater than a few times the epi-layer thickness has also been shown to produce no additional reduction in substrate coupling [45]. A typical rule for physical separation is five to 10 times the epi-layer thickness from the nearest offending digital node. In the case of an epi process, minimization of the inductance associated with the substrate back contact is much more important than using closely spaced substrate contacts [45].

Another issue involved in mixed-signal design is the supply to which the substrate is connected. Connecting the substrate to the analog supply has the potential of injecting substrate noise into the analog supply while connecting to the digital supply can make the substrate noisier. If the number of I/O ports permits, the preferred approach is to have the substrate
connect to a separate quiet supply which is connected to the analog supply off chip.

5.4.2 Supply Coupling and Distribution

The issue of supply coupling is alleviated by using separate supplies for the analog and digital circuits. The analog supply powers the op-amps which are also reconfigured into comparator pre-amps. The digital supply powers the latches (Fig. 5-7), the clock generator (Fig. 5-8) and some digital logic. The large digital output drivers can induce large current spikes on the digital supply. This could potentially inject noise into the analog circuit in the form of charge injection. An open drain output driver is used as is described in Section 5.4.5.

The two sets of power supply lines are laid out in a serpentine shape, with minimum crossing over each other. When they do cross, the crossings are located near the end of the pipeline where the analog circuits have more noise tolerance.

5.4.3 Voltage Reference Distribution

For flexibility in testing, the voltage reference is located off chip. In addition to the common-mode voltage, two reference voltages are distributed throughout the chip. In multi-bit per stage ADC, a resistive ladder is typically used for the generation of reference voltage levels for the ADSC [11]. In this case, feedback scheme using sense and force circuits can be used to reduce the effect of ohmic drop across long metal lines. For the prototype, the 1-b-per-stage architecture eliminates the need of the resistive ladder. Since the reference does not supply DC current, the test chip does not use this feedback technique. The off-chip reference circuit is shown in Fig. 6-1 in the next chapter.

5.4.4 Shielding of Op-Amp Inputs

The most sensitive analog nodes in a pipelined ADC are the input nodes of the op-amp. Although a differential architecture transforms the substrate, supply, and clock coupling into common-mode signals, any mismatch between the two sides of the differential circuit can degrade the performance. In the test chip fabricated in a double-metal double-poly process, any length of wire connected to the op-amp inputs are extensively shielded wherever possible. The shielding metal is connected to the analog ground.

5.4.5 Reduced Logic Swing

The test chip produces 18 bits of raw digital codes which are reduced down to 12 in software. The 18 bits of codes are driven off chip with large buffers that are designed to drive 50 pF of capacitance. Therefore, large spikes can be introduced on the digital supply. The output of the CMOS inverters can also capacitively couple to the substrate via the reverse biased drain junctions, producing large substrate noise.
For the test chip, an open drain NMOS device is used as the digital output driver [46]. The drain current is applied to the emitter of an off-chip NPN transistor as shown in Fig. 5-13. The common-base transistor converts the current into a voltage through a load resistor. The acquisition of the digital output codes is described in Section 6.2.3.

![Test PCB and Test Chip Diagram]

**Figure 5-13: Digital output driver.**

## 5.5 Testability Considerations

In addition to the mixed-signal issues described in the previous section, testability considerations should also be taken into account when designing a complicated system such as the pipelined ADC. In commercial settings, testing is an important cost component of the final product. The time and cost involved in testing have a direct impact on the product marketability. In the context of this thesis project, however, testability is focused in a research setting where the ease of testing depends on the ease of the controllability and observability of the test chip.

**Controllability** When the prototype chip does not operate as designed, it has to be forced into certain modes of operation to pin-point the mechanism of malfunctioning. In designing the prototype, many control signals are built into the chip for these purposes. These signals are listed in Table 5-1.

The comparator gain control can be achieved in two ways. The first is to vary $V_{c7}$ in Fig. 5-1 which varies the gain of the second stage of the pre-amp. The other is to vary the gate control voltage of the transistor implemented as the gain reduction resistor described at the end of the
### Table 5-1: Control signals for testability.

<table>
<thead>
<tr>
<th>Signals</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator Pre-amp Gain Control</td>
<td>Offset and Speed Control</td>
</tr>
<tr>
<td>Comparator Time Control</td>
<td>Minimize Comparison Time</td>
</tr>
<tr>
<td>Common-Mode Level</td>
<td>Dynamic Range Control</td>
</tr>
<tr>
<td>Reference</td>
<td>SNR Control</td>
</tr>
<tr>
<td>Nulling Resistor</td>
<td>Settling Time Control</td>
</tr>
<tr>
<td>Analog Bias Currents</td>
<td>Speed, Gain, Offset Control</td>
</tr>
<tr>
<td>Latch Bias Currents</td>
<td>Speed Control</td>
</tr>
</tbody>
</table>

paragraph 0:1 common-mode feedback circuit for $a_1$ in Section 5.2. By controlling the effective resistance, the gain of the comparator as well as its speed can be changed.

The second signal is the gate control labeled $V_c$ for the delay circuit in the upper left corner of Fig. 5-8. As described in Section 5.2.4, by varying this voltage, the comparison time can be varied as necessary.

Both the reference and the common-mode voltages are generated off chip and hence can be changed to any desired voltage. While a large reference voltage can improve the SNR, it can also saturate the op-amp, resulting in gross nonlinearities. The ability to vary the reference voltage allows the ADC to be tested in these different conditions.

In addition to these control signals, the gate voltage of the nulling resistors shown in Fig. 5-4 can also be varied to optimize the op-amp settling time if necessary. Since the right-half-plane zero is a function of the $g_m$ of the second stage of the op-amp [13], the ability to vary the nulling resistance should be accompanied with the ability to vary the bias current.

As described in Section 6.2.3, the necessary master analog bias currents $I_{b1-2}$ in Fig. 5-3 and $I_{b3}$ in Fig. 5-4 and the necessary master digital bias current for the latch shown in Fig. 5-7 are supplied from circuits off chip. By varying these bias current sources, the speed, voltage gain, and voltage offset can be changed.

Should the ADC malfunctions due to a low-gain op-amp, for example, the analog current level can be reduced to increase the op-amp DC open-loop gain. When the current decreases, during the comparison mode, the op-amp reused as a comparator pre-amp is slow. In this case, the comparator time control can be used to increase the comparison time. Without the various control signals shown in Table 5-1, the debugging of the ADC will be difficult.

**Observability**  When the control signals are applied, the ADC has to be observable in order to monitor the response to the control signals described in the previous paragraphs. In addition to the digital output codes, some internal nodes of the prototype should be accessible for probing. Some of these points are provided with probe pads on the order of 20 x 20 μm$^2$. For AC-signal nodes, the size of the probe pads should be large enough to accommodate the probe
tip, but small enough so that the AC characteristics is to not adversely effected by the added capacitance. Other nodes such as the gate voltages of cascode transistors are made observable by bonding them out and bypassing them off chip.

5.6 Chip Layout

The layout of the prototype incorporating the testability considerations outlined in the previous section is described in this section. Some of the additional layout considerations are given.

5.6.1 General Description

Fig. 5-14 shows the chip micrograph. The main part of the chip is the pipelined stages in the big rectangle labeled 'ADC'. Also included on chip is the clock generator and the digital output drivers. The analog input is presented to the MSB stage of the pipeline located at the northwest corner of the chip. The signal propagates down the pipeline in a serpentine manner. Since the LSB stages of the pipeline have more noise immunity, they are closer to the digital section of the clock generator and the output buffers.

5.6.2 Op-Amp and Bias Circuit Placement

The sharing technique requires two adjacent stages of the pipeline to share one second stage of the op-amp. The layout of the op-amp is arranged so that the second stage of the op-amp is located between the two first stages of the op-amps.

For the first four MSB stages of the pipeline, one bias circuit is used for each set of two pipelined stages. The bias circuit is also placed between the two pipelined stages near the second stage of the op-amp.

5.6.3 Substrate Connection

Although an epi process is used, many substrate contacts are used. The chip is attached to the package cavity with a conductive epoxy. The cavity is then bonded to a ground terminal on the LCC package.

5.6.4 On-Chip Bypass Capacitors

After the pipelined ADC described in Section 5.2 is laid out, many empty areas remains. On-chip bypass capacitors on the order of 1-10 pF are added to both the analog supply and the digital supply as well as the reference voltages. These bypass capacitors help supply the large high-frequency currents demanded by the ADC.
Figure 5-14: Chip micrograph.
5.6.5 ElectroStatic Discharge (ESD) Protection Circuit

For those pads that never accept an applied voltage higher or lower than the supply, two ESD protection diodes are used; one for a large positive discharge and one for a large negative discharge. Examples of these pads include the digital output pads. Certain pads such as the control voltage of the nulling resistors for the op-amp compensation have no protection diodes. This allows the applied control voltages, such as those listed in Table 5-1, to go above and below the supply when necessary.

5.7 Summary

The details of the pipelined ADC are given including the op-amp, latch and clock generator design. The design of the digital error correction stage is also described. Some of the mixed-signal design issues are discussed. Finally, testability considerations for the test chip are presented, followed by a description of the chip layout.
6 Test System and Experimental Results

6.1 Introduction

The prototype described in Chapter 5 is used to verify the low-power design techniques presented in Chapter 4. This is accomplished with the aid of a test system. In Section 6.2, a description of the design issues for the test hardware is presented. In Section 6.3, both the histogram and the Fast-Fourier-Transform (FFT) based test methods are described, followed by the experimental test results obtained for the test chip. Future improvements of both the test chip and the test system is described in Section 6.4.

6.2 Test System

The test chip described in Chapter 5 is appropriately packaged and inserted in a custom designed Printed Circuit Board (PCB) to characterize its performance. The package selection and PCB design are described.

6.2.1 IC Package

Electrical Considerations The desired characteristics for the IC package include a minimum-size cavity so that the bond wire inductance can be minimized, dedicated cavity connection pins so that the substrate back contact has low inductance, and small pin-to-pin capacitance. Two of the most commonly used packages are Dual In Line (DIP) and Pin Grid Array (PGA). These packages are suitable for medium-resolution, medium-speed ADC. One disadvantage with these packages is the large variation of the bond-wire inductance between the nearest and furthest pins from the center of the cavity. For this project, a higher performance package is desired.
Some of the choices include Quad Flat Pack (QFP) and Leadless Chip Carrier (LCC). These two are selected based on the mechanical considerations below.

**Mechanical Considerations** For testing purpose, the package needs to be easily removable from the PCB setup. While direct soldering of the QFP can potentially achieve better electrical contact and better performance, such a package will not be easily removable. Based on this consideration, a 68-terminal LCC is used in conjunction with a clam-shell socket. The socket is soldered into the test PCB, and the LCC contacts the socket leads through pressure from the clam-shell.

### 6.2.2 PCB design

In designing the PCB, much of the mixed-signal concerns for the chip-level design described in Chapter 5 carry over to the board-level design. Some of the most important additional points are briefly discussed here.

**Ground Plane** A number of grounding strategies exist for the ground-plane design. For this project, a star grounding scheme where a single ground plane with a ground split between the digital and analog section is used. The ground for the analog and digital sections are connected near the chip package. Since the current cannot flow across the split, this scheme minimizes the possibility of digital current returning to the analog supply [9].

**Supply Decoupling Strategies** The critical nodes on the PCB are decoupled with surface mount capacitors on the back side of the PCB as close to the nodes as possible. They are supplemented with 0.1-μF ceramic capacitors and 10-μF tantalum capacitors.

**Line Width** All analog traces are at least 15 mils (0.375 mm) wide with 2-Oz (0.07mm thick) copper to ensure minimum inductance at high frequency.

**Routing** As much as possible, all analog lines are entirely above the analog portion of the ground plane; the same strategy is employed for the digital lines. This ensures that high frequency return paths are directly underneath the signal current [47]. The small current loop ensures both minimum magnetic field generation and minimum magnetic pickup.

### 6.2.3 Major Test Components

**Voltage Reference Generation** The reference circuit is generated by using a low-noise bandgap reference (AD780) followed by a low-noise op-amp (OP-27) to supply the AC currents drawn by the switched-capacitor circuits. The circuit is shown in Fig. 6-1. Resistors $R_1$ and $R_{adj}$ are used to divide the 3 V generated by the AD780 to 2.25 V. Capacitors $C_1$ and $C_2$
are for bypass. The voltage $V_1$ is buffered by an OP27 in a non-inverting configuration to generate $V_{REF+}$. Resistors R4 at the output of the op-amp stabilizes the op-amp, which has to drive large bypass capacitors $C_4$ and $C_5$. These two bypass capacitors keep $V_{REF+}$ robust in the presence of large currents drawn by the switched-capacitor circuits. The $R_2$-$C_3$ network provides compensation. A second OP27 in an inverting configuration is used to generate $V_{REF-}$. Resistors $R_5$ and $R_6$ are nominally equal so that a $V_{REF-}$ of 1.25 V is generated. Note that $V_{REF+}$ and $V_{REF-}$ are respectively 0.5 V above and 0.5 V below the common-mode voltage $V_{CM}$ at 1.75 V. $V_{CM}$ is generated with another AD780 buffered by an OP27 in a non-inverting configuration. The voltage $V_{REF+}$ is set by varying $R_{adj1}$. The common-mode voltage $V_{CM}$ is set by varying $R_{adj2}$. Once $V_{REF+}$ and $V_{CM}$ are set, $V_{REF-}$ is set.

\[ \text{FIGURE 6-1: Voltage reference circuit.} \]

The nominal component values are given in Table 6-1.
Table 6-1: Reference circuit component values.

<table>
<thead>
<tr>
<th>$R_1$</th>
<th>243 $\Omega$</th>
<th>$C_1$</th>
<th>0.1 $\mu F$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_2$</td>
<td>47 k$\Omega$</td>
<td>$C_2$</td>
<td>10 $\mu F$</td>
</tr>
<tr>
<td>$R_3$</td>
<td>1.1 k$\Omega$</td>
<td>$C_3$</td>
<td>0.01 $\mu F$</td>
</tr>
<tr>
<td>$R_4$</td>
<td>22 $\Omega$</td>
<td>$C_4$</td>
<td>0.1 $\mu F$</td>
</tr>
<tr>
<td>$R_5$</td>
<td>2.2 k$\Omega$</td>
<td>$C_5$</td>
<td>10 $\mu F$</td>
</tr>
<tr>
<td>$R_6$</td>
<td>2.2 k$\Omega$</td>
<td>$C_6$</td>
<td>0.1 $\mu F$</td>
</tr>
<tr>
<td>$R_7$</td>
<td>22 $\Omega$</td>
<td>$C_7$</td>
<td>0.1 $\mu F$</td>
</tr>
<tr>
<td>$R_8$</td>
<td>47 k$\Omega$</td>
<td>$C_8$</td>
<td>10 $\mu F$</td>
</tr>
<tr>
<td>$R_9$</td>
<td>1.1 k$\Omega$</td>
<td>$C_9$</td>
<td>0.01 $\mu F$</td>
</tr>
<tr>
<td>$R_{10}$</td>
<td>22 $\Omega$</td>
<td>$C_{10}$</td>
<td>0.1 $\mu F$</td>
</tr>
<tr>
<td>$R_{11}$</td>
<td>2.2 k$\Omega$</td>
<td>$C_{11}$</td>
<td>10 $\mu F$</td>
</tr>
</tbody>
</table>

**Bias Current Generator**  A bank of 16 analog and 4 digital bias currents are supplied to the chip. The large number is for flexibility in testing as described in Chapter 5. These biases are generated with emitter degenerated NPN (2N3904) and PNP (2N3906) transistors whose bases are resistively biased. Fig. 6-2 shows an example for the NPN transistor. By varying either resistors $R_{B1}$, $R_{B2}$, or $R_E$, the current drawn by the transistor can be controlled. Note that the bypass capacitors $C_3$ and $C_4$ should be across the on-chip diode-connected PMOS transistor to keep its $V_{GS}$ constant. A similar circuit for supplying current to the on-chip NMOS diode-connected transistors is accomplished by using PNP transistors as current sources.

**Input Filter**  A first-order RC filter is used to bandlimit the input signal. The resistor is metal-film for its low-noise characteristics. The capacitor is 1 nF Mica type. The resistor value is chosen so that the 3-dB bandwidth of the filter is slightly higher than the input signal frequency. The choice of metal-film resistors and mica capacitors is based on experimental evidence showing minimum introduction of harmonic distortion [9].

**Master Clock**  A 5-MHz clock from a crystal oscillator, buffered by TTL inverters is used as the master clock. This master clock is applied as the input to the on-chip clock generator shown in Fig. 5-8 to generate the necessary clock phases for the ADC.

**Digital Output Acquisition**  As alluded in Chapter 5, the open-drain digital output has only about 20 mV of voltage swing to minimize substrate and power supply coupling. The output current is switched into a common-base NPN whose output voltage is applied as an input to the ECL logic as shown in Fig. 6-3. ECL to TTL conversion is applied followed by isolators. The isolators drive the input to the Digital Acquisition Board (DAB) which acquires the ADC data and stores it in a high-speed SRAM. Once data is acquired, the computer can read out the data in the SRAM slowly.
**Figure 6-2:** Bias circuit for a PMOS device.

**Figure 6-3:** Digital output acquisition.
6.3 Experimental Results

The experimental chip shown in Fig. 5-14 was fabricated in a 1.2-μm double-poly double-metal CMOS process. All of the experimental results presented in this section were obtained when the chip was powered by a 2.5-V analog supply and dissipates 33 mW including the on-chip bias generators. For the digital supply, although on-chip charge-pumping techniques could be used to turn on the MOS switches [48], [49], for ease of design and testing, a 4.2-V supply was used. When a charge pumping circuit is used, the digital supply is about one $V_T$ below two times the analog supply. The 4.2-V digital supply is roughly equal to this pumped supply when the analog supply is 2.5 V.

6.3.1 Histogram Code Density Test

**Background** The availability of low distortion sine wave generators makes the histogram test easy to perform. Since the input is known, the probability of the digital output codes is known. In particular, for a sine wave input voltage $V = A \sin \omega t$, the probability density function is given by

$$p(V) = \frac{1}{\pi \sqrt{A^2 - V^2}}$$  \hspace{1cm} (6.1)

The graph of Equation (6.1) is shown in Fig. 6-4. Codes near the maximum and the minimum are more likely to occur. Codes near the zeros crossings of the sine wave, where the slope is maximum, are less likely to occur. Based on this known probability, the cumulative histogram of the code occurrences are used to compute the analog decision points [50]. The spacing of the decision points are the DNL, while the running sum of the DNL is the INL.

![Probability density function of a sine wave.](image-url)
Artifacts  There are two classes of artifacts in the histogram test. The first is extrinsic, where the artifacts are created by the implementation of the data acquisition hardware. The case of intrinsic artifacts will be discussed later in this section.

For the extrinsic artifact, consider the case where the input to the ADC is a sine wave of 488.28 Hz, the conversion rate is 5 MHz, and the size of the data acquisition SRAM is 12.8 K words. Suppose that the total data size for the histogram computation is 128 K words, then the data acquisition SRAM will be filled up 10 times. Each time the SRAM is filled up, the computer pauses to transfer data from the SRAM to the computer disk. This picture is depicted in Fig. 6-5. Since the input sine wave is running continuously, the data collected will have periodic missing intervals, corresponding to the time when data transfer to the computer is taking place. This results in an extrinsic histogram artifact.

![Figure 6-5: An extrinsic histogram artifact.](image)

One easy solution to this problem without resorting to increasing the SRAM size is to take blocks of data that are an integral number of the input sine cycles. In the example of 488.23 Hz input, this correspond to $n \cdot 10,240$ words per block, where $n$ is an integer. Since each block covers an integral number of the input sine cycles, there is no particular fraction of the sine cycle that has artificially missing data points.

The second type of histogram artifacts is intrinsic in that it is inherent to the histogram test independent of the hardware implementation. One common artifact is the failure to detect missing codes due to the presence of noise at the comparator input which shifts the decision point in a random manner. The randomized decision point has the effect of spilling adjacent codes into the code bin that is supposed to have no code due to ADC nonidealities [51].

To analyze the effect of comparator noise on the code density test, a $\pm 0.5$ LSB of comparator noise is assumed. For simplicity, it is also assumed that when the analog voltage $V_{IN}$ is within $\pm 0.5$ LSB of the comparator decision boundary, the probability for the code to fall on either side of this boundary is half and half. Based on this model, when $V_{IN}$ varies over the interval of 1 LSB, corresponding to the width of the $i$th bin of the histogram, the resulting digital code will be spread to the two adjacent $(i - 1)$th and $(i + 1)$th bins conceptually shown in Fig. 6-6. The solid lines represent the decision boundary, while the dashed lines represent the $\pm 0.5$ LSB comparator noise.
Figure 6-6: Comparator noise dithering effect on the histogram.

Since ideally all of the digital codes are supposed to be in the \( i \)th bin, the spreading to adjacent bins can be modeled as a convolution kernel shown in Fig. 6-7.

Figure 6-7: Convolution kernel for a uniformly distributed comparator noise.

The convolution kernel represents the noise distribution of the comparator offset. Let the DNL obtained from the histogram be \( dnlh[n] \), the convolution kernel be \( x[n] \), and the real histogram with an ideal noise-free comparator be \( dnl[n] \), then

\[
dnlh[n] = x[n] \ast dnl[n]
\]  

(6.2)

As an example, suppose an N-bit ADC has a missing code at the MSB decision level. The DNL \( (dnl[n]) \) and INL \( (inl[n]) \) are shown in Fig. 6-8. Assuming the convolution kernel shown in Fig. 6-7, the DNL \( (dnlh[n]) \) and INL \( (inlh[n]) \) obtained using histogram is shown in Fig. 6-9. In particular comparing the histogram derived DNL in Fig. 6-9 (a) with the actual DNL in Fig. 6-8 (a), it can be seen that the missing code at the MSB transition is now artificially improved due to the comparator noise dithering effect.

A quick way to find the actual DNL is to look at the discontinuities in histogram calculated INL \( (inlh[n]) \). For the above example in Fig. 6-9, by taking the difference in INL on either side of the discontinuity, a DNL of \(-1\) results. Although the INL discontinuity can be used to reveal the actual DNL, this method is not exact. Precautions should be used to infer the DNL from the INL.
6.3. Experimental Results

Figure 6-8: Real (a) DNL and (b) INL.

Figure 6-9: (a) DNL and (b) INL with an intrinsic histogram artifact.
Histogram Results A 9.87560-KHz sine wave is applied to the ADC operating at a 5.0-Msample/s conversion rate from a 2.5-V analog supply. The signal source is an Audio Precision System One. A total of 128,000 points are collected to compute the DNL and INL which are shown in Fig. 6-10 at 12-b level.

As explained in the previous section on histogram artifacts, the INL discontinuity can be used to reveal the DNL. Applying this method to Fig. 6-10, the worse case DNL of approximately $-1$ LSB appear at the second MSB transition.

One possible source of this large DNL is a parasitic coupling capacitance in the second MSB stage. This parasitic capacitance can be from the top plate of a sampling capacitor to a digital node such as the gate of a bottom-plate switch as shown in Fig. 6-11. During the sampling phase, the parasitic capacitance $C_p$ couples to the digital node, which is reset to a high voltage level at $V_H$. During the amplifying phase, $C_p$ couples to either $V_H$ or $V_L$ depending on the digital code $d$. In this case, it can be shown that the residue voltage is given by
\[ V_O = \begin{cases} 
   \left( \frac{C_1 + C_2}{C_1} \right) V_{IN} & \text{if } d = 0 \\
   \left( \frac{C_1 + C_2}{C_2} \right) V_{IN} - \left( \frac{C_1}{C_2} \right) V_{REF} + \left( \frac{C_p}{C_2} \right) (V_H - V_L) & \text{if } d = 1 
\end{cases} \] (6.3)

From Equation (6.3), it can be seen that the effect of \( C_p \) is to introduce a code-dependent offset to the residue voltage. This is illustrated in Fig. 6-12 assuming \( C_1 > C_2 \). When \( d = 0 \), the code-dependent offset leaves the residue segment unchanged. On the other hand, when \( d = 1 \), it shifts the residue segment up. As a result, the residue drop is decreased from the ideal \( V_{REF} \) by this offset. For \( V_H = 4.2 \) V, \( V_L = 0 \), \( V_{REF} = 1 \) V, and \( C_2 = 0.5 \) pF, a \( C_p \) of 0.12 fF is sufficient to cause a -1 LSB DNL error at the second MSB transition. Note that the effect of this parasitic capacitance is not a problem unique to the CFCS technique. For a conventional switching technique, the same parasitic capacitance still gives a code-dependent offset.

Although a single-ended case is used to illustrate the effect of \( C_p \) in Fig. 6-11, a similar error can occur in a fully differential implementation with a mismatch in \( C_p \) of 0.12 fF between
the two sides. In future design, the top plates can be either shielded or sandwiched between two layers of bottom plates to eliminate this type of parasitics capacitance. In addition, if $C_p$ is better matched between the two sides of a differential implementation, the parasitic effect is common-mode and can be rejected by the op-amp.

6.3.2 The FFT Test

While the histogram test reveals the low-frequency nonlinearities of the ADC, it does not contain information regarding the SNR. In fact, a noisy ADC can exhibit good linearity since the noise can be averaged out over a large number of data points used in the histogram. One of the main purposes of the FFT test is to characterize the noise level of an ADC by computing the SNR.

Some of the issues involved in the FFT test include coherent vs. non-coherent sampling, number of points used for the data sample, and the choice of the DSP windows in the case of non-coherent sampling. These issues are addressed in a number of articles in the literature, including [52]. For brevity, only the specific details related to the test chip are given here.

In the FFT test, a 2.2-MHz sine wave is digitized by the ADC under test. The signal source is an HP8643B Frequency Synthesizer, followed by a discrete Bandpass LC filter. The single-ended output of the filter is converted to a differential output using a TT1-6 transformer from Mini Circuits. A total of 16384 samples of data are collected. Since the FFT assumes the data is periodic, the two-ends of the data should have no discontinuity. The end effect [52] is minimized by applying a Blackman window to the acquired data from the ADC. The result is transformed into the frequency domain using an FFT algorithm in Matlab. The plot is shown in Fig. 6-13.

The magnitude of the higher order harmonics are shown in Table 6-2. Although the INL shown in Fig. 6-10 indicates that the transfer curve is different from that shown in Fig. B-1, the $-66.5$ dB second harmonic is consistent with a 10-b capacitor matching as indicated in Table B-1 in Appendix B. The remaining harmonics are due to the discontinuities in the INL. The Total Harmonic Distortion (THD) is $-64.4$ dB which is about 3 dB lower than the expected THD from Table B-1.

The signal power, the higher harmonics power, and the noise power can be calculated from the same data. Fig. 6-14 shows the SNR with a 2.2-MHz input frequency. The peak SNR is 67.6 dB. This is about 5.4 dB lower than the expected SNR of 73 dB when the rms $kT/C$ noise is about a factor of two smaller than the rms quantization noise. For reference, the theoretical SNR is shown. The experimental SNDR at the same input frequency of 2.2 MHz is also shown with a peak value of 62.7 dB. At low input amplitudes, the SNDR is nearly equal to the SNR.
Figure 6-13: Measured FFT plot at $f_s = 5.0$ MHz.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Frequency (MHz)</th>
<th>Magnitude (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FND</td>
<td>2.2</td>
<td>0</td>
</tr>
<tr>
<td>HD2</td>
<td>0.6</td>
<td>-66.50</td>
</tr>
<tr>
<td>HD3</td>
<td>1.6</td>
<td>-79.95</td>
</tr>
<tr>
<td>HD4</td>
<td>1.2</td>
<td>-77.2E</td>
</tr>
<tr>
<td>HD5</td>
<td>1.0</td>
<td>-73.75</td>
</tr>
<tr>
<td>HD6</td>
<td>1.8</td>
<td>-80.57</td>
</tr>
<tr>
<td>HD7</td>
<td>0.4</td>
<td>-75.79</td>
</tr>
<tr>
<td>HD8</td>
<td>2.4</td>
<td>-78.74</td>
</tr>
<tr>
<td>HD9</td>
<td>0.2</td>
<td>-86.06</td>
</tr>
<tr>
<td>HD10</td>
<td>2.0</td>
<td>-91.16</td>
</tr>
<tr>
<td>HD11</td>
<td>0.8</td>
<td>-81.60</td>
</tr>
<tr>
<td>HD12</td>
<td>1.4</td>
<td>-80.83</td>
</tr>
</tbody>
</table>

Table 6-2: Harmonic analysis of the measured FFT data.
Figure 6-14: Measured SNR and SNDR vs. input signal level at $f_s = 5.0$ MHz.

6.4 Improvements

After the ADC is experimentally characterized, several improvements can be made. These are described first for the prototype design, then for the test PCB.

6.4.1 Prototype Design

The modifications for future prototype designs are listed below.

Digital Error Correction Scheme The digital error correction scheme proposed in Fig 5-12 has an advantage in that the feedback ratio is maintained since each of the op-amps uses two capacitors as in a regular 1-b-per-stage implementation, without over-range capability. In addition, the use of two op-amps is compatible with the third low-power design technique listed in Chapter 4 in that each of the op-amps can be reused as a comparator pre-amp. One problem that exists with this implementation is that the charge injection from the two op-amps is not matched. Precautions based on the charge injection mismatch must be taken into account in future design.
Latch  The latch circuit shown in Fig. 5-7 was found to draw more current than expected. The core of the latch circuit shown in Fig. 5-7 is redrawn in Fig. 6-15. When a differential input is applied to transistors MP1 and MP2 in the direction shown, after the falling edge of the strobe, the output of the latch at \( V_{o+} \) and \( V_{o-} \) tilt in opposite directions as shown, turning off transistor MN5. Since the gate of MP3 is at a low voltage near ground, MP3 functions as a resistor, and the current from MP2 flows upwards, effectively reversing the drain and source of MP3. The current then flows in a 'circular' manner as the arrow in Fig. 6-15 indicates, eventually sinking into MN4. Since the latch operates from the digital supply, the digital supply current is increased because of this design flaw.

Layout  The prototype layout which consists of approximately 3,000 transistors was completed in about three weeks. The time pressure resulted in a non-optimum layout. One example is the core of the pipelined stages. While the op-amp is symmetrical around the y-axis, the sampling capacitor is symmetric around the x-axis. In future designs, the existing layout should be optimized to achieve complete symmetry. Many nonidealities such as parasitic capacitance mentioned in connection with the DNL data in Section 6.3.1 and charge injection can be better suppressed by the common-mode rejection of the op-amp if the layout is more symmetrical.

Chip Package  Although attention paid to the package selection resulted in the use of an LCC, not all LCC’s have the same electrical performance. After the chips were packaged, it was found that the capacitance between the adjacent terminals of the LCC was a factor of two to three greater than that in alternative LCC packages. In addition, the current package does not have a dedicated cavity pin. The connection to the cavity is achieved using a bond wire which does not have the low inductance of a dedicated cavity pin.

Another possible source of the degradation in performance is the LCC clam-shell socket. The large socket outline increases the distance between the bypass capacitor and the actual LCC terminals, thereby increasing the trace inductance from the point of actual bypass to the actual LCC terminals. For high-resolution, high-speed conversion, a custom designed LCC socket may be necessary to take full advantage of the LCC package.

6.4.2 PCB Design

Bias Network Design  A single resistor in lieu of the transistor circuit described in Section 6.2.3 can be used in the future design. The resistor can serve to damp any high-frequency bias voltage oscillation induced by the inductive long bias lines on the PCB. Compared with the large transistor biasing network shown in Fig. 6-2, the resulting compact layout of the PCB also minimizes the lengths of the bias lines.
Figure 6-15: Latch DC current problem.
Single vs. Dual Supplies  In the single supply design, the ground functions as the common negative terminals between the analog and the digital supplies. Slits in the ground plane are used to minimize digital contamination of the analog supplies. By using twice as many supplies, the ground can be used as a reference that does not carry the return currents. Instead, the currents flow through a separate negative supply in a dual-supply scheme. The trade off between extra supplies and better isolation should be evaluated in the context of the performance requirement. High-resolution high-speed ADC’s would likely benefit from the dual-supply approach.

Mechanical Support  One often neglected design consideration is the spacers. Since the PCB is relatively flexible, spacers should be used every five inches. The use of components such as the clam shell socket and the BNC connectors require pressure when connecting and disconnecting the components. Without the support of the spacers, the solder connections become unreliable after the repetitive application of pressure. The resulting intermittent connections can make the ADC particularly difficult to debug.

Design for Testability  Ideally the PCB should be designed to work the first time. Occasionally, as experiments progress, modification to the board becomes necessary. When such modification is not substantial enough to require a redesign, a piggy-back board can be used. Since the holes in vector boards are 100 mil pitch, the PCB should be on the same pitch to facilitate easy connection between the two boards.

6.5 Summary

The test system used to obtain data on the test chip is described. Next, histogram test method is briefly described along with histogram artifacts and experimental linearity data. The FFT test method is presented along with the experimental SNR data. The performance parameters are summarized in Table 6-3. The chapter is concluded with some suggested improvements for a future prototype.

<table>
<thead>
<tr>
<th>Technology</th>
<th>1.2-μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>12 b</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>5.0 Ms/s</td>
</tr>
<tr>
<td>Minimum Supply Voltage</td>
<td>2.5 V (Analog)</td>
</tr>
<tr>
<td>Power</td>
<td>33 mW (Analog)</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>1.0 pF (single-ended)</td>
</tr>
<tr>
<td>DNL</td>
<td>+0.63/-0.78 LSB</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>67.6 dB at f_m = 2.2 MHz</td>
</tr>
<tr>
<td>Active Die Area</td>
<td>4.1 x4.2 mm²</td>
</tr>
</tbody>
</table>

Table 6-3: Experimental performance summary.
Conclusion

7.1 Summary

A low-power design methodology is presented in this thesis, starting with the identification of the pipelined architecture for video applications in Chapter 2. After a detailed description of the conventional pipelined ADC in Chapter 3, a set of low-power design techniques is proposed in Chapter 4.

For video applications, the INL of an ADC is not critical. This relaxed requirement is used to minimize power consumption by minimizing the capacitor size down to the $kT/C$ noise limit. A commutated feedback-capacitor switching technique is used to enhance the DNL beyond the capacitor matching accuracy. This technique significantly reduces the op-amp load, and hence the op-amp power dissipation, which is the dominant source of power dissipation in a pipelined architecture.

In addition to the CFCS technique, the pipelined architecture is also examined carefully. This leads to the second low-power design technique which reduces 40% of the effective number of the op-amps used for the entire pipeline.

Whereas the second technique reduces power by sharing the second stage of the op-amp between the adjacent stages of the pipeline, the third technique reduces power by reusing the first stage of the op-amp as a comparator pre-amp.

In the fourth technique, the common-mode feedback circuit of the second stage of the op-amp is implemented by exploiting parasitic capacitors. The technique turns the parasitic capacitors, which would otherwise load the op-amp output, into common-mode feedback capacitors, thereby minimizing the power consumption of the ADC.

These combination of techniques can be implemented separately, or together as is the case in the prototype described in Chapter 5. The experimental results presented in Chapter 6 shows a 2.5-V 12-b 5.0-Msample/s ADC with 33 mW of analog power consumption. Implemented in
a 1.2-\(\mu m\) CMOS technology, the power consumption is competitive with those implemented in more advanced technology using the conventional pipelined implementation.

7.2 Future Work

The work described in this thesis can be extended in terms of improving the performance of the ADC and extending the low-power design techniques presented in Chapter 4 to analog subsystems other than a pipelined ADC.

7.2.1 Performance Improvement

In addition for the possible improvements cited in Section 6.4, the performance achieved in this work can be improved in terms of its conversion speed and its resolution.

For higher speed operation, several ADC’s can be used in parallel. If the problem of mismatch between the different ADC’s can be solved, the conversion rate can be significantly improved beyond that of one ADC.

For higher resolution such as 14-16 b, the CFCS technique requires 7-8 b capacitor matching and 7-8 b comparator offsets. Both requirements are not difficult to achieve. As shown in Appendix A, the CFCS technique cancels out not only the first-order mismatch errors, but also the capacitor nonlinearity effect. As a result, uncalibrated 14-16 b ADC maybe possible. Future work is necessary to investigate this possibility.

7.2.2 Extending the Proposed Low-Power Design Techniques

For very low-power consumption, the set of low-power design techniques can be applied to a cyclic architecture which uses as few as two stage of the pipeline. In this case, the power consumption can be small at the expense of a lower conversion speed.

In any switched-capacitor systems when op-amps are used for offset cancellation during half of the clock cycle, the op-amp sharing technique can be used to reduce the effective number of op-amps.

The exploitation of parasitic capacitors as a common-mode circuit can be applied to any system that uses fully differential two-stage op-amp design as demonstrated in Chapter 5. For a one-stage op-amp driving the bottom plate of a capacitive load, by inserting a well underneath the bottom plate of the capacitor, the bottom plate to substrate parasitics can be similarly turned into common-mode feedback capacitors. With a reduced capacitive load, power is minimized.

Given the nature of analog circuit design, a set of general low-power design techniques is difficult to achieve. The set of techniques proposed in this thesis for pipelined ADC’s can serve as an inspiration for power minimization techniques in other analog subsystems.
Appendix A

Analysis of the Effect of Capacitor Nonlinearity

A 1-b-per-stage pipelined stage is used to examine the effect of capacitor nonlinearity when the CFCS technique is used. For convenience, the CFCS technique shown in Fig. 4-2(b) is redrawn here. The \(i\)th capacitor is modeled by [37]:

\[
C_i = C_i^0 (1 + \alpha_i V + \beta_i V^2) \tag{A.1}
\]

Where \(C_i^0\) is the zero-bias capacitance of \(C_i\); and \(\alpha_i\) and \(\beta_i\) denote the first-order and second-order voltage coefficients, respectively. The symbol \(V\) represents the voltage across the capacitor. For a 1-b-per-stage case, two capacitors are used per stage. Hence, \(i = 1\) or \(2\).

![Diagrams of Sampling and Amplification Phases](image)

**Figure A-1:** The CFCS technique.

Assuming that the op-amp DC open-loop gain is infinite so that its inverting input is 0, the total charge stored on \(C_i^0\) and \(C_2^0\) is given by:
\[
Q_s = \int_{V_{IN}}^{V_{-}=0} \sum_{i=1}^{2} C_i^0 (1 + \alpha_i V + \beta_i V^2) dV
= - \sum_{i=1}^{2} C_i (V_{IN} + \frac{\alpha_i}{2} V_{IN}^2 + \frac{\beta_i}{3} V_{IN}^3)
\] (A.2)

During the amplifying phase, when \(d = 0\), the total charge stored on the capacitors is given by:

\[
Q_{a0} = \int_{0}^{V_{-}=0} C_2^0 (1 + \alpha_2 V + \beta_2 V^2) dV + \int_{V_{RES0}}^{V_{-}=0} C_1^0 (1 + \alpha_1 V + \beta_1 V^2) dV
= -C_1^0 (V_{RES0} + \frac{\alpha_1}{2} V_{RES0}^2 + \frac{\beta_1}{3} V_{RES0}^3)
\] (A.3)

Equating Equation (A.2) with Equation (A.3) and rearranging:

\[
V_{RES0} = \left(\frac{C_1^0 + C_2^0}{C_1^0}\right) V_{IN} + \left(\frac{\alpha_1 C_1^0 + \alpha_2 C_2^0}{2 C_1^0}\right) V_{IN}^2 + \left(\frac{\beta_1 C_1^0 + \beta_2 C_2^0}{3 C_1^0}\right) V_{IN}^3 - \frac{\alpha_1}{2} V_{RES0}^2 - \frac{\beta_1}{3} V_{RES0}^3
\] (A.4)

The zero-order approximation of Equation (A.4) is given by:

\[
V_{RES0} \approx \left(\frac{C_1^0 + C_2^0}{C_1^0}\right) V_{IN}
\] (A.5)

Substituting Equation (A.5) into the right side of Equation (A.4), the output voltage when \(d = 0\) is approximately given by:

\[
V_{RES0} \approx \left(\frac{C_1^0 + C_2^0}{C_1^0}\right) V_{IN} + \left(\frac{C_2^0}{C_1^0}\right) \left(\frac{\alpha_2 - \alpha_1 C_1^0}{2 C_1^0}\right) V_{IN}^2 + \left(\frac{C_2^0}{C_1^0}\right) \left(\frac{3 \beta_1 (C_2^0)^2 - 3 \beta_1 C_1^0 C_2^0 - \beta_1 (C_2^0)^2 + \beta_2 (C_2^0)^2}{3 (C_1^0)^2}\right) V_{IN}^3
\] (A.6)

Similarly, when \(d = 1\), the total charge stored on the capacitors is given by:

\[
Q_{a1} = \int_{V_{REF}}^{V_{-}=0} C_1^0 dV + \int_{V_{RES1}}^{V_{-}=0} C_2^0 dV
= -C_1^0 (V_{REF} + \frac{\alpha_1}{2} V_{REF}^2 + \frac{\beta_1}{3} V_{REF}^3) - C_2^0 (V_{RES1} + \frac{\alpha_2}{2} V_{RES1}^2 + \frac{\beta_2}{3} V_{RES1}^3)
\] (A.7)

Equating Equation (A.2) with Equation (A.7) and rearranging:
\[
V_{RES1} = \left( \frac{C_1^0 + C_2^0}{C_2^0} \right) V_{IN} - \left( \frac{C_1^0}{C_2^0} \right) V_{REF} + \left( \frac{\alpha_1 C_1^0 + \alpha_2 C_2^0}{2C_2^0} \right) V_{IN}^2 + \left( \frac{\beta_1 C_1^0 + \beta_2 C_2^0}{3C_2^0} \right) V_{IN}^3 \\
- \frac{\alpha_1}{2} \left( \frac{C_1^0}{C_2^0} \right) V_{REF}^2 - \frac{\beta_1}{3} \left( \frac{C_1^0}{C_2^0} \right) V_{REF}^3 - \frac{\alpha_1}{2} V_{RES1} V_{IN} - \frac{\beta_1}{3} V_{RES1}^3 
\] (A.8)

The zero-order approximation of Equation (A.8) is given by:

\[
V_{RES1} \approx \left( \frac{C_1^0 + C_2^0}{C_2^0} \right) V_{IN} - \left( \frac{C_1^0}{C_2^0} \right) V_{REF} 
\] (A.9)

Substituting Equation (A.9) into the right side of Equation (A.8) and simplifying, the output voltage when \( d = 1 \) is approximately given by:

\[
V_{RES1} \approx \left( \frac{C_1^0 + C_2^0}{C_2^0} \right) V_{IN} - \left( \frac{C_1^0}{C_2^0} \right) V_{REF} \\
+ \left( \frac{\alpha_1 C_1^0 C_2^0 - \alpha_2 (C_1^0)^2 - 2\alpha_2 C_1^0 C_2^0}{2(C_2^0)^2} \right) V_{IN}^2 \\
+ \left( \frac{\alpha_2 C_1^0 (C_1^0 + C_2^0)}{(C_2^0)^2} \right) V_{IN} V_{REF} \\
+ \left( \frac{\beta_1 C_1^0 (C_2^0)^2 + \beta_2 (C_2^0)^3 - \beta_2 (C_1^0 + C_2^0)^3}{3(C_2^0)^3} \right) V_{IN}^3 \\
+ \left( \frac{\beta_2 C_1^0 (C_1^0 + C_2^0)^2}{(C_2^0)^3} \right) V_{IN}^2 V_{REF} - \left( \frac{\beta_2 (C_1^0)^2 (C_1^0 + C_2^0)}{(C_2^0)^3} \right) V_{IN} V_{REF}^2 
\] (A.10)

At the decision point, substituting \( V_{IN} = V_{REF}/2 \) into Equation (A.6),

\[
V_a \approx \left( \frac{C_1^0 + C_2^0}{C_1^0} \right) \frac{V_{REF}}{2} + \left( \frac{C_2^0}{C_1^0} \right) \left( \frac{\alpha_2 C_1^0 - \alpha_1 C_1^0 - 2\alpha_2 C_1^0}{8C_1^0} \right) V_{REF} \\
+ \left( \frac{C_2^0}{C_1^0} \right) \left( \frac{-3\beta_1 (C_1^0)^2 - 3\beta_1 C_1^0 C_2^0 - \beta_1 (C_2^0)^2 + \beta_2 (C_1^0)^2}{24(C_1^0)^2} \right) V_{REF} 
\] (A.11)

Similarly, for \( d = 1 \), substituting \( V_{IN} = V_{REF}/2 \) into Equation (A.10) and simplifying,

\[
V_b \approx \left( 1 - \left( \frac{C_1^0}{C_2^0} \right)^2 \right) \frac{V_{REF}}{2} + \left( \frac{-3\alpha_1 C_1^0 C_2^0 - \alpha_2 (C_1^0)^2 + 2\alpha_2 C_1^0 C_2^0}{8(C_2^0)^2} \right) V_{REF}^2 \\
+ \left( \frac{-7\beta_1 C_1^0 (C_2^0)^2 + \beta_2 (C_1^0)^3 - 3\beta_2 (C_1^0)^2 C_2^0 + 3\beta_2 C_1^0 (C_2^0)^2}{24(C_2^0)^3} \right) V_{REF}^3 
\] (A.12)
The residue drop $V_{\text{drop}}$ is given by subtracting Equation (A.12) from Equation (A.11):

$$V_{\text{drop}} \cong V_{\text{REF}}(1 - \epsilon_1\epsilon_2) + \gamma_1 V_{\text{REF}}^2 + \gamma_2 V_{\text{REF}}^3$$  \hspace{1cm} (A.13)

where, $\epsilon_i$ denotes the percentage capacitor mismatch as defined in Fig. 4-3 and

$$\gamma_1 = \frac{\alpha_2 C_1^0 (C_2^0)^3 - \alpha_1 (C_2^0)^4 - 2\alpha_1 C_1^0 (C_2^0)^3 + 3\alpha_1 (C_1^0)^3 C_2^0 + \alpha_2 (C_1^0)^4 - 2\alpha_2 (C_1^0)^3 C_2^0}{8(C_1^0 C_2^0)^2}, \text{ and}$$

$$\gamma_2 = \frac{\left( \beta_2 (C_1^0)^2 (C_2^0)^4 - 3\beta_1 (C_1^0)^2 (C_2^0)^4 - 3\beta_1 C_1^0 (C_2^0)^5 - \beta_1 (C_2^0)^6 \right)}{24(C_1^0 C_2^0)^3} + \frac{7\beta_1 (C_1^0)^4 (C_2^0)^2 - \beta_2 (C_1^0)^6 + 3\beta_2 (C_1^0)^5 C_2^0 - 3\beta_2 C_1^0 (C_2^0)^5}{24(C_1^0 C_2^0)^3}$$  \hspace{1cm} (A.14)

Assuming that the zero-bias capacitance $C_1^0 \cong C_2^0$, $\gamma_1$ and $\gamma_2$ are zero, and Equation (A.13) is reduced to:

$$V_{\text{drop}} \cong V_{\text{REF}}(1 - \epsilon_1\epsilon_2)$$  \hspace{1cm} (A.16)

In other words, not only is the first-order mismatch error canceled out, the effect of both first and second order voltage coefficients is also canceled out using the CFCS technique.

A similar analysis can be performed for the conventional switching case. It can be shown that at the decision boundary when $V_{I_N} = V_{\text{REF}}/2$,

$$V_{\text{drop}} \cong V_{\text{REF}}(1 - \epsilon_1 + \epsilon_2 + \epsilon_1\epsilon_2) + \frac{1}{2}(\alpha_2 - \alpha_1)V_{\text{REF}}^2 + \frac{1}{3}(\beta_2 - \beta_1)V_{\text{REF}}^3$$  \hspace{1cm} (A.17)

From Equation (A.17), $V_{\text{drop}}$ in the conventional case has both the first and second order capacitor mismatch terms as indicated in Chapter 4. In addition, the effect of nonlinear capacitance is canceled only if the voltage coefficients of $C_1$ and $C_2$ match. In a fully-differential ADC, since the effect of the first-order voltage coefficients is common-mode [37], the main advantage of CFCS is the cancellation of the effect of the second-order capacitor coefficients.

Although a 1-b-per-stage case is used in the above analysis, a similar analysis can be used for a pipeline with a stage resolution of greater than 1 b. It can be shown that the CFCS technique is equally effective in canceling out the effect of both first and second order capacitor voltage coefficients.
Appendix B

Harmonics Resulting from the Use of the CFCS Technique

Since the CFCS technique improves the DNL, but leaves the INL commensurate to the capacitor accuracy, harmonic distortion occurs. To quantify the level of distortion, consider a 1-b-per-stage pipelined ADC where only the first stage has a capacitor mismatch. The resulting transfer curve is shown in Fig. B-1(a). The slope of the transfer curve is smaller than ideal when the MSB = 0. On the other hand, when the MSB changes to 1, the slope is larger than ideal. When a sine wave given by $\sin \omega t$ is applied to this ADC, the output is shown as the solid line in Fig. B-1(b). Although the output is digital, for simplicity, it is shown as a continuous waveform. The dashed line represents the ideal case with no capacitor mismatch. The waveform represented by the solid line can be decomposed into two half-wave rectified sine waves. The positive one can be expressed as

$$V_+ = \begin{cases} (1 + m) \sin \omega t, & \text{if } \sin \omega t \geq 0 \\ 0 & \text{else} \end{cases}$$

$$= \frac{1 + m}{\pi} + \frac{1 + m}{2} \sin \omega t - \sum_{n=1}^{\infty} \frac{2(1 + m)}{(2n)^2 - 1} \cos 2n \omega t \quad (B.1)$$

The negative half-wave rectified wave is given by:

$$V_- = \begin{cases} (1 - m) \sin \omega t, & \text{if } \sin \omega t < 0 \\ 0 & \text{else} \end{cases}$$

$$= -\frac{1 - m}{\pi} + \frac{1 - m}{2} \sin \omega t + \sum_{n=1}^{\infty} \frac{2(1 - m)}{(2n)^2 - 1} \cos 2n \omega t \quad (B.2)$$
The Fourier series of the waveform shown in Fig. B-1 is obtained by summing Equation (B.1) and Equation (B.2):

\[
V_O = \underbrace{\frac{2m}{\pi}}_{\text{DC offset}} + \underbrace{\frac{\sin \omega t}{\text{fundamental}}} - \underbrace{\sum_{n=1}^{\infty} \frac{4m}{((2n)^2 - 1)\pi} \cos 2n\omega t}_{\text{higher-order harmonics}}
\]  (B.3)

From Equation (B.3), the odd-order harmonics are zero. Note that when \( m = 0 \), Equation (B.3) reduces to \( \sin \omega t \). When \( m \neq 0 \), the even-order harmonics have amplitudes given by \( 2m/((2n)^2 - 1)\pi \), where \( 2n \) indicates the order of the harmonics.

Table B-1 shows the first five non-zero harmonics relative to the fundamental in dB for various values of \( m \). Since \( m = (C_2 - C_1)/(2C_1) \), \( m \) is also an indication of the capacitor mismatch.

<table>
<thead>
<tr>
<th></th>
<th>( m = 2^{-7} )</th>
<th>( m = 2^{-8} )</th>
<th>( m = 2^{-9} )</th>
<th>( m = 2^{-10} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD2</td>
<td>-49.6</td>
<td>-55.6</td>
<td>-61.6</td>
<td>-67.7</td>
</tr>
<tr>
<td>HD4</td>
<td>-63.6</td>
<td>-69.6</td>
<td>-75.6</td>
<td>-81.6</td>
</tr>
<tr>
<td>HD6</td>
<td>-70.9</td>
<td>-76.9</td>
<td>-83.0</td>
<td>-89.0</td>
</tr>
<tr>
<td>HD8</td>
<td>-76.0</td>
<td>-82.1</td>
<td>-88.1</td>
<td>-94.1</td>
</tr>
<tr>
<td>HD10</td>
<td>-80.0</td>
<td>-86.0</td>
<td>-92.0</td>
<td>-98.0</td>
</tr>
</tbody>
</table>

Table B-1: Harmonics as a function of the capacitor mismatch

Although the capacitor mismatch is assumed to be present only in the MSB stage of the pipeline, similar analysis can be carried out for mismatches in later stages of the pipeline. Similar analysis can also be carried out for the case when the stage resolution is greater than 1 b.
Bibliography


