AN ELECTRONIC MULTIPLIER
FOR USE IN AN ANALOGUE COMPUTER

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ABSTRACT

A high speed electronic multiplier has been developed for use as a component in an analogue computer employing a 400-cycle suppressed-carrier voltage for data transmission. Multiplication is performed in a variable-gain amplifier unit. One of the input signals is applied directly to the amplifier as a 400-cycle voltage, while the other input is a low frequency voltage which is used to control the amplifier gain. A linear gain-control characteristic is assured by a feedback system which provides approximately 44 db of stabilization. A phase-sensitive detector employing feedback has also been developed for obtaining the control voltage from a suppressed-carrier 400-cycle input.

The useable range of variation for the signal applied directly to the amplifier, and for the product output, is approximately 5000 to 1, while the range for the signal applied to the control channel, is approximately 250 to 1. An accuracy of approximately plus or minus one per cent was attained. A phase lag of 11 degrees between the envelope of a modulated input signal and the envelope of the product output occurs in the amplifier channel for a modulation frequency of 10 cps. The corresponding delay in the control channel, including the phase detector, is 24 degrees. It is felt that both the accuracy and delay characteristics of the multiplier could be improved considerably if several minor modifications were made.
CHAPTER I

Introduction

The complicated mathematical equations required to express many physical problems which have recently become of great importance, necessitate the use of mechanical or electrical computers, if a solution is to be obtained in any reasonable length of time. During the last war many simple computers were developed, particularly for use in fire control systems and, at present the Dynamic Analysis and Control Laboratory at Massachusetts Institute of Technology is engaged in the design of a high precision, relatively high speed, analogue computer.

Most electrical analogue computers are designed to perform the operations of addition, subtraction and low speed multiplication. Fortunately for the designers of computers most of the simpler problems can be solved without the aid of high speed multipliers. However, for handling complex problems, as required in the DACL computer, a high speed multiplier offers considerable advantage and for some problems becomes a necessity.

If a multiplier is to be a useful part of a computer it must operate on the same analogue quantity as the remainder of the computer or on a quantity readily convertible to that used in the remainder of the system. It may, therefore, be useful at this point to consider the analogue quantities generally used and to briefly discuss the various multipliers which have been used or proposed.

1.1 "Analogue Quantity" Used in Computers

A large number of the electrical analogue computers which have been built, or are being built, are designed to use a d-c voltage for the analogue quantity. In systems of this type, data are transmitted in accord with the amplitude and polarity of the d-c voltage.

A smaller number of computers, including that being built at present in the DACL at M.I.T., use a suppressed-carrier a-c voltage for the electrical analogue quantity. In such a system data are transmitted in accord with the amplitude and phase sense of the voltage, as shown in Figure 1.1. In the ideal system, if voltages of zero degree phase angle represent positive signals then voltages of 180 degree phase angle represent negative signals. Voltages at other phase angles are not intentionally used in the system.

In mechanical computers data are usually transmitted by means of shaft rotations.
A and B: Equal constant signals of opposite sign.

C: Sinusoidally varying signal showing opposite polarity for the two halves of the cycle.

Suppressed-carrier signals

Figure 1.1
1.2 General Ways in which Multiplication can be Performed

In searching for a possible basis for the design of a high-speed multiplier it is well to have in mind the generally known methods by which multiplication can be performed.

One first thinks of that class of devices the operation of which inherently depends on the formation of a product. An ordinary wattmeter is an example of this type of device.

Multiplication might also be performed with the aid of logarithms, or by the use of the algebraic identity

\[(x+y)^2 - (x-y)^2 = 4xy\]

in which the formation of a product is reduced to the processes of squaring, adding and subtracting. The integral identity

\[uv = \int udv + \int vdu\]

can also be used for forming a product.

In addition to these methods, which are potentially useful in analogue computers, there are those schemes peculiar to pulse digital computers.

1.3 Types of Multiplication Performed in a Computer

A computer may be called upon to perform three types of multiplication. The first type of operation consists merely in selecting a desired fraction of a single signal and will be referred to as "proportional multiplication." The second type deals with the multiplication of two slowly varying quantities and the third with the multiplication of two rapidly varying quantities.
1.31 **Proportional Multiplication**

In computers proportional multiplication is the simplest and most commonly used type. It can be accomplished in computers using either alternating or direct voltages for the analogue quantity by the use of a single potentiometer. For this operation, the excitation to the potentiometer is made one of the quantities to be multiplied and the relative position of the contact arm the other quantity. The contact arm may be fixed thereafter, as in the case of setting parameters into the problem, or it may be servo driven. In this latter case it can be seen that the speed with which the excitation to the potentiometer may be varied is relatively very high but that the speed with which the contact arm may be moved is limited by the speed of the servo which drives the arm and by noise introduced by movement of the arm. This system can therefore be classified as being able to perform multiplication of a rapidly varying quantity by a slowly varying quantity.

1.32 **Multiplication of Two Slowly Varying Quantities**

The multiplication of two slowly varying quantities can be performed with a pair of potentiometers\(^1\) as shown in Figure 1.2. In this type of operation the first potentiometer is excited by a source of constant voltage and each of the variables to be multiplied is translated into a shaft rotation. It can be seen that the output of the first potentiometer is

---

proportional to the variable involved, provided there is a linear relation between resistance and shaft rotation. The output of the second potentiometer is proportional to the excitation received from the first potentiometer and to the shaft rotation. It can thus be seen that a product is obtained. Precautions must be taken to keep the loading of the first potentiometer by the second small, or to compensate for this loading by using a tapered winding on the first potentiometer. In this method the allowable speed of variation of the two quantities is again limited by the speed of the servos used to drive the potentiometers.

\[ E_0 = axE_i \]

*AN ELECTRICAL CIRCUIT FOR MULTIPLYING TWO NUMBERS*

*FIGURE 1.2*
1.33 Multiplication of Rapidly Varying Quantities

Since potentiometers are not suited for multiplying rapidly varying quantities a number of electromechanical and electronic devices have been developed for this purpose, some applicable to a-c systems and some usable only in d-c systems.

1.331 Electromechanical Devices

The polyphase wattmeter has been investigated on several occasions for use as a multiplier, but in the attempts made up to the present the natural frequency found for the systems has been below 15 cps.

A linear translational multiplier employing a pair of strain gauge pick-up elements, driven by a motor element somewhat similar to that used in dynamic loudspeakers, is now being developed in the M.I.T. Dynamic Analysis and Control Laboratory. Although this multiplier is still in the developmental stage it shows considerable promise.

1.332 Electronic Multipliers

In the past few years several different types of electronic multipliers have been investigated. One of these, for use in d-c computers, utilizes the fact that over a considerable range the voltage across a diode supplied from a constant current source varies as the logarithm of the current. The logarithms

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thus obtained are added in a resistive network and the anti-
log finally taken in a circuit which employs a diode in a
feedback circuit.

Another electronic multiplier for use in a d-c computer
is the variable attenuator multiplier developed by Sack, and
others, at Cornell\(^1\) during the last war. This multiplier is
slow and has a limited range. It is, therefore, of little
interest for the present problem.

A third type is the square-law multiplier currently be-
ing developed by A. E. Macnee\(^2\) of the Research Laboratory of
Electronics at M.I.T. Although fairly good results have been
obtained with this multiplier it is also applicable only in
d-c computers and is, therefore, of little interest here.

1.4 Requirements of Multiplier for DACL Computer

The original requirements set up for a multiplier for
the DACL computer were somewhat more stringent than those out-
lined below. However, it was felt that any multiplier which
satisfied the specifications given here would be of definite
value.

The multiplier should operate over a range of at least
\(\pm 250\) to 1 in either input, provided the product output re-
ains within a range of \(\pm 1000\) to 1. Over the range from

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1 H.S. Sack, et al, "Electronic Computers for Division, Multi-
plication, Squaring, etc.," NDRC Div 14 OEMar-768 Report
No. 435, Cornell University, August 7, 1944.
2 "Electronic Differential Analyzer," Quarterly Progress
Report, Research Laboratory of Electronics, MIT, July 15, '47.
maximum output to one-tenth of maximum output the product obtained should be within ±1% of the correct value. For outputs less than one-tenth of maximum the allowable error may increase gradually with a decrease in output, reaching a maximum allowable error of 25% of the correct value for an output of 1/1000 of the maximum.

In addition, the two signals to be multiplied should be accepted as 400-cycle suppressed-carrier signals and be delivered as a 400-cycle suppressed-carrier signal with the same 400-cycle phase angle as the input. Furthermore, if one of the 400-cycle input signals is fixed in amplitude while the other is varied sinusoidally at 10 cycles per second, then the envelope of the product output should not lag the envelope of the varying input signal by more than 5 degrees. Also, the peak product output of these two signals should not change by more than 20% if one of the signals is sinusoidally varied in amplitude at frequencies up to 10 cycles per second while the other is fixed. This last specification will be clarified by reference to Figure 1.3 which shows the type of product signal obtained for two constant input signals and the type obtained for one fixed and one sinusoidally varying input signal. The peak product output is designated as $P_p$ in each case.

1.5 Shortcomings of Former Multiplier Schemes

The greatest difficulty foreseen in adapting any of the above described electronic multipliers for use in the DACL
computer lay in the fact that none of them operated on an a-c carrier. To adapt them would therefore require using a phase-sensitive detector* in each input signal channel and a balanced modulator to convert the product output back to an a-c carrier. Since each of these elements would introduce additional errors and require considerable development work, it was felt that the multiplier scheme chosen should, if possible, operate directly with the a-c carrier signals. In considering electronic vs. electro-mechanical multipliers it seemed that a

* The polarity of the output of a phase-sensitive detector is determined by the phase of the input signal, which is of the suppressed-carrier type described in Section 1.1.
completely electronic multiplier, even if it required a number of tubes, offered some advantage over an electro-mechanical unit in that the electronic parts are standard, whereas the electro-mechanical elements probably would have to be specially designed and manufactured. In addition, a higher speed of response could probably be attained in the completely electronic unit.

With these thoughts and the above outlined requirements in mind, the variable gain amplifier type of multiplier described in the following chapters was finally conceived and efforts were directed toward developing it.
CHAPTER II

Variable Gain Amplifier Type of Multiplier

2.1 Principle of Operation

The principle of operation of the 400 cycle-per-second suppressed-carrier signal multiplier developed for this thesis is shown in the block diagram of Figure 2.1 below.

As can be seen in this diagram, one of the signals to be multiplied is applied both to the input of a variable-gain amplifier and to the input of a fixed-gain balancing circuit, while the other signal is fed into a phase-discriminating detector. The filtered output of the detector is used to control
the amplifier gain. If the output of the balancing circuit and the amplifier are assumed to be exactly 180° out of phase then the combined output of these two circuits can be made zero for some particular amplifier gain. By a proper choice of components it is possible to obtain a balance for the condition of zero input signal No. 2, and to maintain this balance over a wide range of input No. 1. The gain control system is so arranged that if signal No. 2 assumes some positive value then the gain of the amplifier is increased so that its output is greater than the balancing signal, giving a resultant positive output. On the other hand, a negative signal No. 2 decreases the gain of the amplifier so that the balancing signal is larger, giving a resultant negative output.

The variable gain amplifier actually becomes a linear modulator in this application, as will be seen later, and since this latter designation is also descriptive the two terms will hereafter be used interchangeably.

With this arrangement, it is seen that the output of the amplifier will be linearly dependent on the product of the two signals if (1) the gains of the amplifier and balancing circuit are independent of the value of signal No. 1, (2) the gain vs. control voltage characteristic of the amplifier is a straight line (3) the phase-sensitive detector is linear.

If the maximum signal levels at which the amplifier and balancing circuit are operated are well below the overload values, and if extreme precautions are taken to keep the hum and background noise level low, it seemed possible to make
the gain independent of signal level over the required range of 60 or more db.

It did not, however, seem probable that a linear gain vs. control-voltage characteristic could be obtained without the aid of some automatic gain correcting circuit.

Two possible ways of controlling the gain of the amplifier suggested themselves. The first method was to use the output of the phase detector, suitably modified, as a gain control voltage on some element of the amplifier tubes. The second method was to use the detector output to vary the gain of the feedback loop of a negative feedback amplifier.

The first of these schemes seemed more straightforward, but the possibility of obtaining the gain stabilization offered by negative feedback made the second method attractive also. As a result of these considerations a preliminary investigation of each method was carried on.

2.2 Use of Amplifier with Gain Control in the Forward Circuit

The design of a variable gain amplifier to meet the requirements at hand practically dictated the use of pentodes, but several gain control methods were possible. The gain could conveniently be controlled by (1) varying the direct voltage on the control grid, (2) varying the screen grid voltage, or (3) varying the suppressor grid voltage on a tube of proper design. The first two methods of gain control have the inherent disadvantage that they produce considerable distortion of high level signals in the condition in which they
give a low gain. The screen-control method has the further
disadvantage that it requires a control source capable of sup-
plying a relatively large amount of power. Very few tubes are
available in which the suppressor is brought to a separate pin
on the base and has effective control of the transconductance
of the tube. During the last war, however, a miniature pen-
tode (type 6AS6) was developed, having a suppressor-to-plate
transconductance nearly one-third that of the control-grid-to-
plate transconductance. It appeared that this tube best
fitted the requirements of the multiplier and it was, there-
fore, adopted.

A simple two-stage amplifier was set up to test the 6AS6s.
and it was found that there is a considerable range over which
a curve of output voltage vs. suppressor voltage is relatively
linear. If feedback could be applied to further linearize this
characteristic, the essential element required for a multiplier
would be available. To gain the benefits of feedback, a scheme
was devised which is essentially a double reference regulator.
In this system a fixed voltage (hereafter referred to as the
pilot frequency signal) of some frequency well removed from
that of the signal voltage is added to the signal voltage and
applied to the input of the amplifier. This pilot frequency
signal is amplified along with the signal voltage and at the
output of the amplifier the two signals are separated by ap-
propriate filters. The pilot signal is then applied to a
linear detector and the d-c output is compared with a fixed
d-c reference. The error between the detector output and the
reference is amplified and then applied as a gain-control signal to the amplifier being controlled.

A block diagram for such a pilot-frequency control system is shown in Figure 2.2. It will be shown in Chapter III that feedback of this type will cause the amplifier gain to be linearly dependent on the d-c reference voltage if (1) the amplitude of the pilot frequency voltage is fixed, (2) the detector is perfectly linear and (3) the error signal amplifier has sufficiently high gain. The detector and error signal amplifier must, of course, be phased so that the feedback is degenerative.

![Figure 2.2](image-url)
RESISTORS 1/2 WATT UNLESS OTHERWISE SPECIFIED
CONDENSERS 400 VOLT UNLESS OTHERWISE SPECIFIED

VARIABLE-GAIN AMPLIFIER
TYPE MULTIPLIER

FIGURE 2.3
To determine if a multiplier of this type had any possibilities, the circuit shown in Figure 2.3 was constructed and found to operate in a promising manner. Before this type of control was decided upon, however, it was desired to compare these preliminary results with those obtained for the variable feedback type of control.

2.3 Use of Amplifier with Gain Control in the Feedback Circuit

Preliminary tests were also made to determine the possibility of using a high gain amplifier with a variable amount of negative feedback. The variable feedback was to be obtained by controlling the bias on the grid of a triode used as the shunt arm of a Tee network in the feedback loop of the amplifier. To linearize the gain vs. grid bias characteristic obtained, the same pilot frequency control system as employed for the 6AS6 amplifier described earlier was used.

The amplifier employed in this test had a gain of approximately 4000 times from the grid of the first tube to the output, and the error amplifier had a gain of approximately 50 times. With these gains, along with the gain of the 6SN7 control tube, it was found that even a very small amount of hum or other extraneous signal at the input to the error amplifier caused an appreciable voltage to appear at the output. Since the maximum output is limited, this extraneous signal greatly restricted the possible operating range of the unit.

Because of this inherent noise difficulty and the limited range of gain control possible with this system, it was decided that efforts should be directed toward further development of
the amplifier with gain control in its forward circuit rather than the one employing variable feedback.

In the next chapter equations will be developed to aid in determining the characteristics of a feedback amplifier system employing a pilot frequency for gain control.
CHAPTER III

Mathematical Analysis of Pilot Frequency Control System

3.1 Control Signal Loop

Analysis of the control system can be divided into several steps, the simplest of which considers only the pilot frequency. Figure 3.1, below, shows the pilot frequency loop in which the
symbols are defined as follows:

\[ E_1 = \text{Pilot frequency voltage appearing at the first grid of the variable-gain amplifier.} \]

\[ E_2 = \text{Control signal voltage.} \]

\[ E_3 = \text{Pilot frequency voltage appearing at plate of last amplifier tube.} \]

\[ E_r = \text{Output of rectifier.} \]

\[ E_s = \text{Gain control voltage applied to amplifier.} \]

\[ \mu = \text{Gain of variable-gain amplifier.} \]

\[ K_1 = \text{Conversion gain from plate of last amplifier tube to output of rectifier. This quantity will be expressed in volts d-c output per volt of pilot frequency input.} \]

\[ K_2 = \text{Gain of error signal amplifier.} \]

It can be seen that the following relationships apply in Figure 3.1.

\[ E_3 = \mu E_1 \]

\[ E_r = K_1 E_3 \]

\[ E_s = K_2 (E_r + E_2) \]

The gain of the amplifier will depend, in a rather complicated manner, on the gain control voltage, \( E_s \), but the general requirements on parameters can be seen by a simplified analysis which assumes that \( \mu = \mu_0 + AE_s \). In this expression \( \mu_0 \) is the gain of the variable-gain amplifier for \( E_s = 0 \), and \( A \) is the slope of a tangent to the \( \mu \) vs. \( E_s \) curve at \( E_s = 0 \).
Inserting this expression for $\mu$ in the above equation for $E_3$ gives:

$$E_3 = E_1 \left[ \mu_0 + A K_2 (K_1 E_3 + E_2) \right].$$

Solving this for $E_3$ yields:

$$E_3 = \frac{E_1 (\mu_0 + AK_2 E_2)}{1 - E_1 AK_1 K_2}.$$  \hspace{1cm} (1)

If $E_2 = 0$ then

$$E_3 = \frac{E_1 \mu_0}{1 - E_1 AK_1 K_2} = \frac{E_1 \mu_0}{1 - \mu_0 \left( \frac{E_1 AK_1 K_2}{\mu_0} \right)}.$$

If $\frac{E_1 AK_1 K_2}{\mu_0}$ is replaced by the symbol $\beta$ then the expression for $E_3$ assumes the form of the familiar Black equation\(^1\) for a feedback amplifier,

$$E_3 = E_1 \frac{\mu_0}{1 - \mu_0 \beta}.$$

Once this similarity of the equations is recognized, many of the ideas of ordinary feedback amplifier theory may be extended to this system. The expression $E_1 AK_1 K_2$ becomes the loop gain factor ordinarily referred to as $\mu \beta$. It is well known that if $\mu \beta$ is real and negative the voltage gain of the system is less than $\mu$ and the feedback is classed as degenerative. However, if $\mu \beta$ is real and positive the gain is increased and for values of $\mu \beta$ equal to plus one or more the system generally becomes self-oscillatory.

---

This stability problem is discussed further in Chapter V, but it is noted here that the term $E_1A_KK_2$ should have a high negative value, at least at zero frequency, if good stability is to be obtained from this feedback system.

Unlike the situation in a normal feedback amplifier, $\mu$ is here directly dependent on the input voltage, $E_1$. As a result of this dependence the operation is different than would first be expected for a feedback system.

Following the usual simplifying procedure of allowing the magnitude of $\mu$ to become very much greater than one it is seen that equation (1) reduces to

$$E_3 = -\frac{\mu}{AK_1K_2} - \frac{E_2}{K_1} \tag{2}$$

From this expression it can be seen that, over the allowable operating range, the output voltage, $E_3$, will be independent of the input voltage, $E_1$, and furthermore will vary linearly with changes in the control voltage, $E_2$. Furthermore, if each side of equation (2) is divided by $E_1$, so as to get an expression for the gain, $E_3/E_1$, it becomes evident that the gain is inversely proportional to $E_1$.

3.2 Complete Gain-Controlled Amplifier

This analysis can now be extended to include the signal voltage, $E_A$, applied to the input to the variable-gain amplifier and the signal voltage, $E_B$, obtained at the plate of the last stage, as shown in Figure 3.2. The gain of the
variable-gain amplifier at the signal frequency will be related to the gain at pilot frequency by the expression

$$\mu_{\text{signal}} = K \mu_{\text{pilot}}$$

and the one symbol $\mu$ with no subscript will be used to denote pilot frequency gain.

Using the symbols previously defined it is now possible to write

$$E_B = K \mu E_A = K E_A \left[ \mu_0 + AK_2 (K_1 E_3 + E_2) \right].$$

Substituting equation (1) in the above yields:

$$E_B = KE_A \left[ \mu_0 + AK_2 \left( \frac{K_1 E_1 (\mu_0 + AK_2 E_2)}{1 - E_1 AK_1 K_2} + E_2 \right) \right].$$
Simplifying:

\[ E_B = K E_A \frac{(\mu_0 + AK_2E_2)}{1 - E_1AK_1K_2} \tag{3} \]

Again, if \( |E_1AK_1K_2| \gg 1 \)

\[ E_B = -KE_A \left[ \frac{\mu_0 + AK_2E_2}{E_1AK_1K_2} \right] = -\frac{KE_A}{K_1E_1} \left[ \frac{\mu_0}{AK_2} + E_2 \right]. \tag{4} \]

From equation (4) it would appear that if \( K_2 \) is very large then changes in \( \mu_0 \) will be unimportant. It must be pointed out, however, that this is true only if the variations in \( \mu_0 \) occur slowly enough that the feedback system can cor-
rect for them.

It is also of interest to calculate \( \frac{\delta E_B}{\delta E_2} \). This can be obtained from equation (3).

\[ \frac{\delta E_B}{\delta E_2} = \frac{E_AK_2}{1 - E_1AK_1K_2} \tag{5} \]

Again, if \( E_1AK_1K_2 \gg 1 \), this reduces to

\[ \frac{\delta E_B}{\delta E_2} = -\frac{E_A}{K_1E_1} \]

Equations (4) and (5) indicate that if \( E_1 \) is fixed, while \( E_A \) takes on different values, a family of curves of \( E_B \) vs \( E_2 \), as shown in Figure 3.3, will be obtained.

Assume that \( E_2 = E_c + V \). In this equation \( E_c \) is the signal voltage component of \( E_2 \) and \( V \) is a fixed voltage.
Then from equation (4)

\[ E_B = -\frac{KEA}{K_1E_1} \left[ \frac{\mu_0}{AK_2} + Ec + V \right]. \]

If a balancing signal equal to \( \frac{KEA}{K_1E_1} \left[ \frac{\mu_0}{AK_2} + V \right] \) is added to the output of the amplifier then the resultant output will be

\[ E_p = -\frac{KEA\mu_0}{K_1E_1}. \quad (6) \]

If \( K_2 \) can be made very large, then \( \frac{\mu_0}{AK_2} \) can be made negligible compared to \( V \) and to useable values of \( E_c \).

This analysis therefore indicates that:

(1) If the gain of the error signal amplifier, \( K_2 \), is large enough its value is unimportant and may vary without causing appreciable error.

(2) The gain \( K_1 \) of the rectifier system must be constant.

(3) The pilot frequency voltage \( E_1 \) fed into the amplifier must be constant.

(4) \( |E_1AK_1K_2| \) should be much larger than 1.

It is of interest at this point to determine how best to make \( E_1AK_1K_2 \gg 1 \).

![Figure 3.3](image-url)
In the expression \( \mu = \mu_0 + AE_s \), \( \mu_0 \) is dependent on the particular tubes used, on the plate load, the cathode resistor, and the screen voltage, while \( A \) is dependent on the effectiveness of the control elements, and the value of \( \mu_0 \).

The value of \( E_1 \), the pilot frequency voltage at the first grid of the variable-gain amplifier, must be selected large enough to override the noise, but not so large as to cause distortion. This voltage would probably be of the order of 50 millivolts.

It should further be pointed out that in the expression \( E_1AK_1K_2 \) the two factors \( E_1 \) and \( A \) when lumped together represent the conversion gain of the gain-controlled amplifier, that is the change in output voltage, \( E_3 \), for a unit change in control voltage, \( E_c \).

If \( A \) has a value of 20 volts/volt, then if \( E_1AK_1K_2 \) is to be 500, as required if the \( 1 \) is to be dropped without introducing an error of more than 0.2%, then

\[
20 \times 0.05 \times K_1K_2 = 500
\]

So

\[
K_1K_2 = 500
\]

If \( E_1 \) and \( K \) are fixed, it can be seen from equation (6) that the \( E_p \) obtained for a given \( E_A \) and \( E_c \) becomes smaller as \( K_1 \) is increased. It is desirable to have \( \frac{K}{E_1K_1} \) relatively large and, furthermore, these equations indicate no advantage as \( K_1 \) is increased. The lower limit on \( K_1 \) is set by the voltage required to operate the detector linearly.
Reasonable values for $K_1$ and $K_2$ appear to be 5 and 100 respectively.

In the following chapter the circuits used to meet the requirements pointed out above will be discussed.
CHAPTER IV

Detailed Examination of Multiplier Circuit

4.1 Variable-Gain Amplifier

The variable-gain amplifier in this multiplier employs two Type 6AS6 miniature pentodes, as shown in Figure 4.1. Static characteristics for this tube are given in Figures 4.2 and 4.3. Since the multiplying scheme employed makes it impossible to use ordinary inverse feedback to stabilize the gain and reduce phase shift, it was necessary to take several precautions in the design of this amplifier. To make the 400-cycle phase shift from input to output zero and to keep the phase slope small, a large cathode by-pass condenser and large interstage coupling condensers were used while the screens were fed from a voltage regulator tube, as shown in Figure 4.1. A small condenser was added in the input network to bring the output exactly into phase with the input.

A voltage applied to the suppressor of a 6AS6, in addition to modulating the signal applied to the control grid, also produces a component of the suppressor-signal frequency in the plate circuit. In a two-stage amplifier this component of suppressor-signal frequency can be largely eliminated if an attenuating network is inserted between stages, so that with no voltage applied to the first control grid and an a-c voltage on both suppressors, the voltage applied to the second
IN34 CRYSTALS

400-CYCLE
Input Signal

BAL. POT.

180
1500 µfd

Pilot-Frequency
Input

GAS6

Control Voltage
Input

GAS6

VR-105

+225 V

OUTPUT

VARIABLE-GAIN AMPLIFIER

FIGURE 4.1
DOTTED LINES SHOW $I_{c2}$

SOLID LINES SHOW $I_b$

$E_f = 6.3V$

$E_b = 0.175A$

$E_b I_b$ MAX = 200 V

$E_c I_b$ MAX = 1.65 W

$E_c I_c$ MAX = 0.85 W

CURVES FOR $E_{c2} = 100V$

SUPPRESSOR TIED TO CATHODE

GASG
MINIATURE PENTODE

Figure 4.2
Figure 4.3

Suppressor control characteristics

Data for $E_{c2} = 100V$, $E_B = 100V$

Control grid transconductance at this point = 5000 $\mu$hm
control grid is of the correct amplitude to produce an effect in the plate circuit of the second stage which just balances that produced by the signal on the suppressor of the second tube. If the control grid is \( x \) times as effective as the suppressor, then only \( \frac{1}{x} \) of the signal will be necessary on it to produce a balance. The interstage attenuation required, therefore, will be \( x \) times the first stage suppressor-to-plate gain or, combining the two terms, this means that the interstage attenuation should equal the control-grid-to-plate gain. With this arrangement a signal applied to the first control grid appears with the same amplitude at the second control grid. In practice it is impossible to maintain perfect compensation by this means when the suppressors are driven over their full operating range, but by it the low frequency component appearing on the plate of the second 6AS6 is greatly reduced.

Operating the amplifier with attenuation between the two stages is also desirable, since the allowable range of operation for the tubes is limited on the low end by noise, drift, and stray pick-up and on the high end by distortion. It is, therefore, desirable to operate both 6AS6 stages at the same level to obtain the maximum operating range.

The generation of a small amount of harmonic distortion in the multiplier is not too serious since it will be largely removed by the filter in the output. However, the fundamental output of the amplifier must increase linearly with the input
if the zero balance is to be independent of input. Since it is not possible to use conventional inverse feedback to produce this linear characteristic, it was found that the linearity could be considerably improved by using a pair of 1N34 crystal diodes in the input attenuator network. The forward resistance of these diodes decreases from approximately 15,000 ohms at 0.1 volt to 150 ohms at 1 volt. By paralleling a pair of these crystals with a suitable resistor it was found that over a small range it was possible to make the input to the amplifier increase the amount required to compensate for the decrease in amplifier gain with increase in signal. In this way, about 10 db greater operating range was obtained for the amplifier.

To keep the noise level to a minimum all heaters in the multiplier were operated on direct current and the ripple on the power supplies was held to 0.3 millivolt or less.

The 400 cycle gain of this amplifier from the input to the attenuator network to the output is unity when the suppressors are at approximately ground potential. Another important characteristic of this amplifier is its conversion gain, that is the change in output voltage as a function of the control voltage applied to the suppressors. This characteristic will be discussed further in Chapter V.

4.2 Balancing Circuit

Since the repeater amplifiers used in the DACL computer

---

are arranged to give both positive and negative output, the
input to the multiplier is assumed to be push-pull and the
balancing signal is selected merely as the opposite polarity
signal from that fed into the variable-gain amplifier.

The balancing signal and the amplifier output are fed in-
to grids of a double cathode follower the outputs of which
are summed in a resistive network, as shown in Figure 4.16.

In order to keep the output level as high as possible,
the balancing signal is taken directly to the cathode follower
and the signal fed to the amplifier is attenuated. A zero ad-
justment potentiometer is provided in the input attenuator
network to adjust the balance to zero when the signal applied
to the phase detector is zero.

4.3 Pilot Oscillator

The choice of frequency used for the pilot signal was
governed by the following considerations:

(1) The pilot frequency must be separated far enough from the
normal carrier frequency in order that it can be removed from
the output by filters which will cause little phase shift at
the carrier frequency.
(2) The pilot frequency must be separated far enough from
the normal carrier frequency so that the 400-cycle carrier
can be completely separated from the pilot frequency ahead of
the rectifier.
(3) The amplifier gain at pilot frequency should be nearly
equal to that for the carrier frequency.
The possible choices seemed to be to use direct current for the pilot signal or to use a pilot frequency of the order of 10 kcps. The use of direct current has the advantages that:

1. No rectifier is required in the feedback loop.
2. A small battery would act as a convenient and stable source of pilot signal.
3. Complete removal of the pilot signal from the carrier output could be accomplished merely by a condenser.

The disadvantages with direct current, however, are that:

1. The whole loop must be direct coupled.
2. The feedback system would be unable to distinguish between drift and gain changes in the 6AS6 amplifier.

By using a pilot frequency of 10 kcps it seemed quite possible to build filters to eliminate either the 10 kcps or 400 cps as required, and still cause little phase trouble at the frequency passed. In addition, the development of a suitable pilot frequency oscillator and rectifier, while presenting some problems, seemed by no means impossible.

The use of an a-c pilot signal eliminated the complications of direct coupling and d-c drift. For these reasons a pilot frequency of 10 kcps was decided upon. The oscillator for generating the pilot signal was patterned after that used in the Hewlett-Packard Audio Oscillators with minor modifications to obtain increased stability. With the circuit shown in Figure 4.16 the following results were obtained in a test
made to determine the constancy of the output as the plate supply voltage was changed.

<table>
<thead>
<tr>
<th>Plate Supply Volts</th>
<th>Osc. Output Volts at Tap on output divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>0.570</td>
</tr>
<tr>
<td>200</td>
<td>0.585</td>
</tr>
<tr>
<td>250</td>
<td>0.580</td>
</tr>
<tr>
<td>300</td>
<td>0.565</td>
</tr>
</tbody>
</table>

These results appear entirely satisfactory since the oscillator will be run from a well-regulated plate supply.

4.4 Feedback Rectifier System

A few calculations will serve to determine the approximate range over which the rectifier in the feedback loop of this multiplier must have a constant conversion gain.

If signal input No. 2 is varying at a low frequency, while signal No. 1 is zero, then the pilot frequency voltage at the plate of the second 6AS6 will appear as a standard amplitude-modulated signal, as shown in Figure 4.4, provided perfect low frequency compensation was achieved, as discussed in Section 4.1. The percentage modulation for such a signal is given by

\[
\frac{a - b}{a + b} \times 100.
\]

It is apparent that the range of operation of this multiplier is governed to a large extent by the maximum allowable percentage of linear modulation which can be achieved. If 85% is assumed as a reasonable value for making calculations, then the ratio of \( a \) to \( b \) as defined in Figure 4.4 is \( a/b = 12.3 \). Assuming 90% modulation, the \( a/b \) ratio increases to 19, but the maximum signal out of the multiplier increases only 5%.
This small gain in operating range is not worth the effort involved in practically doubling the range over which the rectifier must operate.

These calculations, therefore, indicate that the rectifier circuit used in the feedback loop should be linear over a range of about 15 to 1. For this rectifier the percentage deviation from linearity should be referred to the output desired for the given input rather than to full scale output. This is a much more stringent requirement than if the rectifier linearity were expressed as, "linear to within 1% of maximum output."

In view of this linearity requirement it appeared that special care should be exercised in designing the rectifier. Two suggestions offered themselves. First, a high perveance diode could be operated at a high voltage with the hope that
the change in resistance of the diode with change in signal level would be negligible, or second, the diodes could be enclosed in a feedback circuit.¹

The use of feedback seemed more promising, so efforts were directed toward developing a system in which it could be employed.

The feedback rectifier developed for the multiplier consists of an amplifier, having high gain at 10 kcps, with a pair of diodes as part of the feedback circuit. The object in using the diodes in this manner is to linearize their I vs E characteristic. A typical rectifier characteristic is shown in Figure 4.5A and the desired characteristic is shown in Figure 4.5B.

It will be noted in Figure 4.5A that the resistance of the rectifier decreases as the voltage across the rectifier is increased. This characteristic causes the ratio of output to input for the rectifier to increase somewhat with an increase in the applied voltage despite the action of the load. resistance in linearizing this characteristic.

A simplified sketch of the feedback rectifier is shown in Figure 4.6. If the rectifier bridge is perfectly balanced then the current which flows through one side of the bridge on the positive half-cycle is just equal to that which flows through the other side on the negative half-cycle. In this case it will be seen that point 1 will be at ground d-c potential so that the voltage $E_{out}$ developed across resistor $r$ is equal to that developed across resistor $r_L$. The actual d-c voltage developed across either resistor $r$, can therefore be found by integrating the current which flows through $r_L$.
Since this integration introduces no non-linearity, the circuit can be studied as well on a completely a-c basis, using the simplified equivalent circuit of Figure 4.7.

![Figure 4.7](image)

In this circuit we are interested in obtaining a relation between the current, $i_f$, flowing in the feedback loop, and the value of the feedback resistor, $r_b$.

If the input stage of the $\mu$ section of this rectifier is a pentode, then the value of the a-c component of the plate current of the first tube can be written with little error, as

$$i_p = (e_{in} - e_1)g_m$$  \hspace{1cm} (1)

where $g_m$ is the grid-plate transconductance of the first tube.

The remainder of the symbols are indicated in Figure 4.7.
Then: \[ e_1 = r_k (i_p + i_f) \] \hspace{1cm} (2)

and \[ i_f = \frac{E_{out} - e_1}{r_b} \] \hspace{1cm} (3)

Also, \[ E_{out} = \mu (e_{in} - e_1) \] \hspace{1cm} (4)

Therefore: \[ i_f r_b = \mu e_{in} - e_1 (1 + \mu) \]

Using equations (1) and (2) and simplifying, this expression becomes:

\[ i_f r_b = e_{in} \left[ \frac{\mu - \frac{r_k e_m}{1 + r_k e_m}}{1 + \frac{r_k e_m}{1 + r_k e_m}} \right] - \frac{i_f r_k (1 + \mu)}{1 + r_k e_m} \]

Solving this for \( i_f \) yields:

\[ i_f = e_{in} \left[ \frac{\mu - \frac{r_k e_m}{r_b + r_k (r_b e_m + 1 + \mu)}}{1 + \frac{r_k e_m}{1 + r_k e_m}} \right] \] \hspace{1cm} (5)

This expression can be greatly simplified if

\[ \mu > r_k e_m \]
\[ \mu > 1 \]
\[ \mu > r_b e_m \]

and

\[ \mu > \frac{r_b}{r_k} \]

These conditions can all be expressed by the single inequality

\[ \frac{\mu r_k}{r_b + r_k} \gg 1 \]

This is the condition, familiar in feedback amplifier theory, that \( \mu \beta \) be very much greater than unity, since it can be shown by solving equations (1) through (4) above for \( E_{out}/e_{in} \) that, for a feedback circuit of this type,

\[ \beta = \frac{r_k}{r_b + r_k} \]
Using this simplification equation (5) reduces to

\[ i_f = \frac{e_{in}}{r_k} \]

so that as long as \( \frac{\mu r_k}{r_k + r_b} \gg 1 \), \( i_f \) is independent of \( r_b \).

Referring again to Figure 4.7, in which \( r_b \) has a fixed component due to \( r_L \) and a variable component due to the diode, this analysis indicates that the drop across the resistor, \( r_L \), should be independent of the resistance presented by the diode over a wide range of diode operation, since the current, \( i_f \), is independent of the diode resistance.

The first feedback-detector built employed 1N34 germanium crystals as the diodes. These diodes were attractive because they are small, require no heater power, and do not have the bothersome initial-emission-velocity potential of tube diodes. A feedback circuit using these diodes was stabilized with 40 db of inverse feedback and the results obtained appeared encouraging until a careful check was made of the conversion gain as a function of input voltage. Figure 4.8 shows that the results obtained in this test were not satisfactory. A study of the characteristics of the type 1N34 crystal indicates that with 0.05 volts across the crystal the ratio of forward to reverse resistance is approximately four. Since the feedback circuit cannot differentiate between current which passes through the crystal in the reverse direction and that which flows in the forward direction, it appears that, with crystals at least, the feedback can be of little help at very low
Note: Conversion Gain Measured as Volts D.C. at Point 2 of Fig. 4.9 per Volt 10 Kcps at Point 0.
operating levels.

It therefore appears desirable to operate the rectifier system at as high a voltage as allowed by the crystals and the amplifier tube which feeds them. Since the recommended maximum peak inverse voltage which should be applied to the 1N34 diodes is 50 volts it appeared that even by operating the crystals at the highest allowable voltage level it would not be possible to obtain sufficient linearity over a range of more than about 6 to 1.

In view of the limited range apparently available with the 1N34 crystals it was decided to replace them with a 6AL5 double diode and to modify the amplifier stage so as to operate the diodes at as high a voltage level as conveniently possible.

With this arrangement the curve labeled 6AL5 in Figure 4.8 was obtained. This shows a range of 10 to 1 over which the linearity is within plus or minus approximately one per cent. With the circuit used (see Figure 4.16) the gain with the feedback loop closed is 38 db less than as if the loop is opened by connecting the feedback condenser to ground instead of to the 6AK5 cathode.

The complete filter-rectifier system, from the plate of the second 6AS6 shown in Figure 4.1, to the input of the error amplifier, is shown in block diagram form in Figure 4.9.

Pilot frequency signal is taken from the plate circuit of the second 6AS6 stage, through a condenser-resistor
Pilot Frequency Filter-Rectifier System

Figure 4.9
combination which introduces a loss of about 2 db at 10 kcps compared to 26 db at 400 cycles. The output of this pick-off circuit is fed through a 6AG7 cathode follower and then through a 10 kcps band-pass filter designed to pass from 8.0 to 12.5 kcps and give an attenuation of approximately 60 db at 400 cps. The output of this filter is then applied to the feedback rectifier discussed earlier.

As shown in Figure 4.9, the output of the rectifier is filtered, attenuated and mixed with the input signal derived from the phase-detector before being applied to the error amplifier. Summing of the control voltage from the phase-detector with that from the feedback-rectifier is conveniently accomplished by applying the output of the phase-detector at the corner of the rectifier bridge opposite that from which the rectified output is taken.

The conversion gain of the rectifier system of Figure 4.9 is 1.75 volts d-c output per volt of 10 kcps input, measured on a static basis. The phase and gain characteristics of this rectifier system are determined chiefly by the filter circuit required on the output of the rectifier to reduce the ripple voltage applied to the error amplifier and by the 10 kcps band-pass filter ahead of the rectifier. If the 10 kcps input to the system is modulated at 350 cps the gain is approximately 12 db below the static value and a phase lag of 90 degrees is introduced between the demodulated output and the modulation envelope of the input signal.
4.5 **Error-Signal Amplifier**

For the feedback system used in this multiplier, the output of the rectifier is compared with a fixed d-c reference voltage and the difference amplified and used to adjust the voltage on the suppressors of the 6AS6s as required to reduce the error voltage nearly to zero.

The complete error amplifier is shown in Figure 4.10. Reference voltage is developed between the cathode of the first half of the 6SL7 and ground while the error voltage is amplified in three direct-coupled stages which give an output 180 degrees out of phase with the input at zero frequency. In order to attain closed-loop stability, as discussed in Chapter V, both a lead network and a lag network were inserted in the error amplifier system.

The lead network, inserted between the two 6SL7 stages, gives an attenuation of 11 times at zero frequency and has phase-gain characteristics which can be obtained from Figure 4.11 (DACL Drawing No. GA-216-4). If the circuit constants used in the error amplifier are applied in Figure 4.11 the results of Table IV-1 are obtained.

<table>
<thead>
<tr>
<th>Frequency cps</th>
<th>Phase Lead Degrees</th>
<th>Relative Gain db</th>
</tr>
</thead>
<tbody>
<tr>
<td>105</td>
<td>12.5</td>
<td>+ 0.2</td>
</tr>
<tr>
<td>210</td>
<td>24</td>
<td>+ 0.9</td>
</tr>
<tr>
<td>420</td>
<td>40</td>
<td>+ 3.0</td>
</tr>
<tr>
<td>840</td>
<td>53</td>
<td>+ 7.0</td>
</tr>
<tr>
<td>1680</td>
<td>56</td>
<td>+11.7</td>
</tr>
</tbody>
</table>

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ERROR SIGNAL AMPLIFIER

Figure 4.10
GAIN vs PHASE FOR
BASIC LEAD CONTROLLER
WITH AMPLIFIER

\[ \alpha = \frac{R_1 + R_2}{R_2} \]

\[ \omega_1 = \frac{1}{R_1 C} \]

\[ U = \frac{\omega}{\omega_1} \]

USE THIS PLOT TO
MODIFY PHASE-MARGIN
DIAGRAMS DRAWN TO
STANDARD SCALE

Fig. 4.11  GA-216-4
A type of lag network is obtained by providing RC feedback effectively from the plate to the grid of the 6AC7 in the error amplifier of Figure 4.10.

A feedback circuit of this type is analyzed in Appendix I, where it is shown that for the degenerative case with $\mu \gg 1$, the gain is given by

$$\frac{E_o}{E_{in}} = \frac{-\mu}{\left[1 + \frac{\mu R_2}{R_1}\right] + j\omega \mu R_2 C}$$

Figure 4.12 is a plot of the above equation evaluated for the constants used in the error amplifier. This plot shows that the maximum gain for the stage occurs at zero frequency while the gain decreases and the phase of the output lags the zero frequency phase as the frequency is increased. At very high frequencies the gain becomes very small and the phase lags nearly 90 degrees behind the zero frequency value. An inspection of the loop gain-phase characteristic obtained before adding the compensating networks indicated the magnitude of the constants required in the error amplifier but final adjustments were made experimentally.

Output from the error amplifier is taken from a cathode follower in order to provide the low impedance source required to drive the suppressors of the 6AS6s when they are at a positive voltage with respect to the cathodes.

The zero frequency gain from the first grid of the 6SL7 to the cathode of the 6SN7 is 47.5 db.
PHASE-GAIN CHARACTERISTICS OF 6AC7 STAGE IN ERROR-SIGNAL AMPLIFIER

Numbers along curve indicate frequency in CPS
4.6 Output System

The computer in which this multiplier could be used is designed to operate with a maximum signal voltage level of 50 volts rms. However, the maximum signal output of the multiplier, measured at the junction of the 20K resistors in the balancing circuit, is only approximately 0.5 volts rms. Moreover, the voltage at this point contains a 10 kcps pilot frequency component and, if a varying signal is applied to input No.2, a low frequency component due to incomplete compensation as discussed in Section 4.1. Therefore, a filter must be provided to remove the 10 kcps pilot frequency signal and the low frequency components caused by variations in Signal No.2. Furthermore, the output signal voltage must be amplified by approximately 100 times to bring it up to the desired maximum 50 volt level.

The output system must meet the following specifications:

1. The gain must be constant to within at least 0.25 per cent over a voltage input range of at least 1000 to 1 and have a value of approximately 100 times.

2. The equivalent input noise of the system should be 10 micro-volts or less.

3. The phase shift through the system must be zero degrees at 400 cycles and the phase slope through 400 cycles should be as small as possible, consistent with obtaining the required amplitude characteristics.

4. The gain of the system at 10 cps and at 10 kcps should be at least 60 db less than at 400 cps.
The output system shown in Figure 4.12 meets these requirements quite satisfactorily. The signal from the multiplier unit is first passed through a 1:10 isolating transformer to eliminate noise caused by different grounds in the multiplier and the amplifiers. The signal from the transformer is then fed to a high stability decade amplifier (see Figure 4.13) followed by a 400-cycle band-pass filter. The overall gain and phase characteristics for this output system are shown in Figure 4.14 and an oscillogram of the transient which occurs when a step input of 400-cycle signal is applied to the complete output system is shown in Figure 4.15.

![Figure 4.15](image)

Gain and Phase Characteristics of Output System for Electronic Multiplier

Phase Slope ≈ 0.9°/Cycle

Approx - 45db @ 20,000 cps.
The components shown in Figure 4.12 were used for the tests conducted for this thesis, since they could be obtained at the time. It is, however, suggested that an isolating transformer with a one-to-one turns ratio be used, followed by two amplifiers, each with a gain of 10 times. The filter could then be inserted between the two amplifiers. In this way, the output amplifier would not be overloaded by voltages finally removed by the filter and the low impedance output provided by the Ar-6 decade amplifiers would be available for transmitting the output signal to other points in the computer.

4.7 Complete Multiplier

The circuit of the complete multiplier, exclusive of the phase-detector required on input No. 2, and the output system discussed in Section 4.6, is shown in Figure 4.16. The unit uses 13 standard receiving type tubes, four of which are dual units. However, if a group of these multipliers were to be used together it would be quite possible to use one 10 kcps pilot frequency oscillator for the whole group and thereby eliminate two of the tubes from each multiplier unit.
CHAPTER V

Operation of the Complete Multiplier System

5.1 **Open Loop Tests**

A considerable amount of information about a feedback system can be obtained by opening the feedback loop at some convenient point, feeding in voltage at various frequencies, and measuring the phase and amplitude of the voltage appearing at the other side of the point where the loop was opened. In the case of the feedback loop in the multiplier it is most convenient to open the loop at the suppressors of the 6AS6s. Voltage can then be applied to the suppressors and the voltage observed at the cathode of the 6SN7 which normally drives the suppressors. Figure 5.1 is a polar plot of data obtained in this manner. This plot is actually rotated 180 degrees to conform with common servomechanisms practice in plotting data of this type.

According to the Nyquist stability criterion\(^1\) if the open loop characteristic of a system of this type encloses the point \((-1 + j0)\) (in this case the 0db point on the 180 degree radial) the system will become self-oscillatory when the

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OPEN LOOP CHARACTERISTIC
OF ELECTRONIC MULTIPLIER

NUMBERS ALONG CURVE INDICATE FREQUENCY IN CPS
loop is closed. The curve of Figure 5.1, however, does not enclose the \((-1 + j0)\) point and the system is stable when the loop is closed. Furthermore, the curve indicates a phase margin of safety of 15 degrees and an amplitude margin of safety of 4 db. This means that the phase lag at the frequency for which the loop gain is unity (0db) is 15 degrees less than 180 degrees, while the gain at the frequency which gives a phase lag of 180 degrees is 4 db less than unity.

Figure 5.1 indicates a zero frequency loop gain of 44 db, which is approximately 10 db less than the value specified in Chapter III. With the present circuit, however, if the loop gain is increased by 4 db oscillations take place.

It was observed in Chapter III that the loop gain for this system is given by the expression \(E_1 AK_1 K_2\). The value of the conversion gain, \(E_1 A\), can be determined from a curve showing the amplitude of the 10 kcps signal on the plate of the second 6AS6 as a function of the d-c voltage applied to the suppressors. Such a curve is shown in Figure 5.2 and was taken with 30 millivolts of 10 kcps on the grid of the first 6AS6. The slope of the curve of Figure 5.2, which is the conversion gain, \(E_1 A\), is 0.35 volt/volt, while \(A_1\), the gain when \(E_s = 0\), is 31 times and \(A\) is 11.7.

The conversion gain from the plate of the second 6AS6 to the grid of the 6SL7 in the error amplifier is \(K_1\), and has a zero frequency value of 1.75 volts/volt. The zero frequency
Open-Loop Modulation Characteristic of 6AS6 Amplifier
Taken with 30 Millivolts of 10 kcps at Grid of First 6AS6

Figure 5.2
gain of the error amplifier is 47.5 dB or 238 times at an angle of 180 degrees.

At zero frequency the overall loop gain, \( E_1AK_1K_2 \), is therefore \((0.35)(1.75)(-23\)\) = \((-146)\) times or 43.3 dB. This checks very well with the value of 44 dB obtained in Figure 5.1 for the complete loop.

5.2 **Closed-Loop Tests**

It is felt that the operation of the multiplier is best described by presenting data on the static operation of the unit and then describing how the amplitude and phase of the output signal depend on the frequency of variation of the input signals if the amplitude of first one and then the other of the inputs is varied sinusoidally. Results obtained in this manner can then be correlated with data obtained by applying a step function of voltage to first one input of the multiplier and then the other, with a fixed voltage applied to the alternate channel.

5.21 **Static Tests**

There are several factors which must be considered in describing the static linearity of this multiplier.

1. The dependence of the zero balance adjustment on the signal level applied to the amplifier channel of the multiplier.

2. The range and linearity of the product for various input signal combinations.

3. The stability of the zero balance as a function of time.
Noise, signal distortion and other factors make it impossible to adjust the balance control on the multiplier unit for exactly zero output when the signal applied directly to the amplifier has some finite value, while the signal applied to the phase-detector channel is zero. Therefore, it is important to note what output voltage is obtained, since this unbalance signal determines the minimum usable output and, therefore, the range of operation of the multiplier. Table V-1 below gives the unbalance signal and the maximum output signal as a function of the input voltage to the amplifier channel. Balance was established at 1 volt input and not changed thereafter.

<table>
<thead>
<tr>
<th>Input Volts (Each side to ground)</th>
<th>Unbalance Millivolts (after output filter)</th>
<th>Maximum Output Volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0001</td>
<td>3</td>
<td>0.004</td>
</tr>
<tr>
<td>0.00032</td>
<td>3</td>
<td>0.0109</td>
</tr>
<tr>
<td>0.001</td>
<td>3</td>
<td>0.0335</td>
</tr>
<tr>
<td>0.0032</td>
<td>3.5</td>
<td>0.106</td>
</tr>
<tr>
<td>0.01</td>
<td>4</td>
<td>0.335</td>
</tr>
<tr>
<td>0.032</td>
<td>7</td>
<td>1.09</td>
</tr>
<tr>
<td>0.10</td>
<td>16</td>
<td>3.35</td>
</tr>
<tr>
<td>1.00</td>
<td>20</td>
<td>32.5</td>
</tr>
<tr>
<td>1.54</td>
<td>30</td>
<td>50</td>
</tr>
<tr>
<td>3.16</td>
<td>580</td>
<td>Note</td>
</tr>
</tbody>
</table>

Note: Under this condition the output system would be badly overloaded since the Ar-6 output amplifier can develop only 50 volts across the filter connected to its output.

It should be pointed out that the unbalance is largely a random voltage for inputs up to 0.03 volts and that for higher levels the unbalance consists largely of quadrature
components of voltage which would have little effect on the phase detector by which intelligence is finally removed from the computer.

Information of two types can be obtained from Table V-1. The table shows first, that the zero balance is essentially independent of the input to the amplifier channel for inputs up to the 1.5 volts required to give a maximum output of 50 volts. The fact that the zero balance depends to only a small extent on the input indicates that the gain of the amplifier channel is independent of the signal level at which it is operating. The minimum useable input to the amplifier channel is determined by the magnitude of the noise output with no signal input. If an output three times the noise level is considered satisfactory then the minimum useable output is approximately 10 millivolts. The output range of operation is, therefore, from 10 millivolts to 50 volts or 5000 to 1, while the input range is from 0.00032 to 1.5 volts, also a range of 5000 to 1.

Second, Table V-1 indicates the range of operation of the control channel. It will be noted that noise reduces the allowable range of operation of the control channel as the input to the amplifier channel is reduced. At an input of 1.5 volts to the amplifier channel the range for the control channel is approximately ± 250 to 1, but this range decreases to ± 3 to 1 for an input of .001 volt.

A further check on the linearity of operation of the
control channel can be obtained by applying a fixed voltage to the amplifier channel and a d-c voltage to the control channel input. As the polarity of the d-c voltage is reversed, the output should change 180 degrees in phase sense but should not change in amplitude. For small d-c inputs the error noted in this test will be due chiefly to initial unbalance and zero drift, while for large d-c inputs the error will be caused by non-linearity of the control system. Table V-2 below gives the results of a test of this type for two different a-c inputs.

Table V-2

<table>
<thead>
<tr>
<th>A-C Input (Each side to ground)</th>
<th>D-C Input Volts</th>
<th>Product Volts D-C Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Volt</td>
<td>0</td>
<td>0.025 random</td>
</tr>
<tr>
<td></td>
<td>0.0427</td>
<td>0.17</td>
</tr>
<tr>
<td></td>
<td>0.135</td>
<td>0.60</td>
</tr>
<tr>
<td></td>
<td>0.427</td>
<td>1.65</td>
</tr>
<tr>
<td></td>
<td>1.35</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td>4.27</td>
<td>15.8</td>
</tr>
<tr>
<td></td>
<td>8.55</td>
<td>29.5</td>
</tr>
<tr>
<td></td>
<td>13.5</td>
<td>29.5</td>
</tr>
<tr>
<td>0 check</td>
<td></td>
<td>0.090</td>
</tr>
</tbody>
</table>

0.316 Volt

<table>
<thead>
<tr>
<th>D-C Input Volts</th>
<th>Product Volts D-C Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0427</td>
<td>0.059 random</td>
</tr>
<tr>
<td>0.135</td>
<td>0.165</td>
</tr>
<tr>
<td>0.427</td>
<td>0.60</td>
</tr>
<tr>
<td>1.35</td>
<td>1.62</td>
</tr>
<tr>
<td>4.27</td>
<td>5.5</td>
</tr>
<tr>
<td>8.55</td>
<td>9.7</td>
</tr>
<tr>
<td>13.5</td>
<td>9.8</td>
</tr>
</tbody>
</table>

This table indicates that the control system is linear to at least +1 per cent of full scale for d-c inputs of 8.5 volts or less, but that the system saturates for d-c inputs
higher than this regardless of sign, although the saturation is more pronounced for positive inputs. This action is quite natural when it is remembered that a positive input reduces the gain of the amplifier. When the gain becomes very small the output becomes essentially the balancing signal and can increase no further. It should further be noted that the operation shown in Table V-2 is essentially the same for both of the a-c input levels. The table indicates a useable range of control voltage of approximately 48 db or 250 times, which is the range specified in Section 1.4.

Another important factor is the amount by which the zero balance drifts as a function of time. An input of 1 volt (each side to ground) was applied to the amplifier channel and no connection was made to the signal No. 2 input. After the multiplier had been running for several hours the zero balance was adjusted and the drift in this balance was then observed for some time without making any adjustments. This test indicated that with an input of 1 volt the drift will not exceed 200 millivolts. From Table V-1 the maximum output for one volt input is 32.5 volts. A drift of 200 millivolts therefore represents a possible error of approximately 2/3 per cent of full scale. This error is quite appreciable but not surprising when it is considered that only ordinary carbon resistors were used throughout the multiplier and that the heater voltage was obtained from a battery the voltage of which dropped slightly as the battery discharged.

In order to determine more fully the effect of variations
in heater voltage, the heaters were run from an adjustable voltage source and the change in balance noted as the voltage was changed. With the complete multiplier running from the adjustable source and an input of 1 volt to the amplifier channel the unbalance produced is approximately 0.85 per cent of maximum output per one-tenth volt change in heater voltage. Further tests showed that half of this drift is due to the change in the heater voltage of the first tube in the direct-coupled error amplifier, and that variations in heater voltage on the 10 kcps oscillator tubes and the 6AL5 rectifier are relatively unimportant. In view of these results it appears that a Miller circuit\(^1\) should be employed in the error amplifier.

In view of the great care which must be exercised if test results of accuracy better than one-half per cent are to be obtained and the large number of tests necessary to completely establish the accuracy of a multiplier, it was felt that the above data on static accuracy should suffice for the present. Further tests should be conducted after such changes as required to reduce the drift in the zero balance have been made.

The present tests indicate that, for the multiplier unit, an accuracy of at least plus or minus one per cent of full scale should be attained over a useable range of approximately 5000 to 1 for the amplifier channel and 250 to 1 for the control channel.

5.22 **Dynamic Closed-Loop Tests**

The dynamic response of the amplifier channel of the multiplier could be obtained by applying a balanced 400-cycle suppressed carrier modulated wave as Signal No.1 and a fixed d-c voltage as Signal No.2. However, an equivalent result can be obtained by opening the balance channel and applying zero Signal No.2. This second method of testing was employed because the available source of modulated 400-cycle signal provided only a single-ended output.

Figure 5.3 shows both a block diagram of the measurement scheme used and the results of the measurements. Amplitude was read by noting the attenuator setting required to give a constant deflection on the oscilloscope while phase was determined from the Lissajous pattern.

Comparing the results shown in Figure 5.3 with those shown for the output system alone, in Figure 4.14, it will be noted that practically all of the phase shift occurs in the output filter. Further measurements on the amplifier channel of the multiplier indicated a phase shift in it of only 0.025 degree per cycle. The gain of the amplifier-filter combination is independent of the modulation frequency over the range of these tests and the phase shift is practically one degree per cycle. Although it was not possible to carry the test of Figure 5.3 to a phase shift of 90 degrees, Figure 4.14 indicates that 90 degrees would be reached at approximately 90 cps.
OPERATION OF AMPLIFIER CHANNEL
OF ELECTRONIC MULTIPLIER
INCLUDING OUTPUT SYSTEM

FIGURE 5.3
The dynamic response of the control channel, exclusive of the phase detector, was obtained by substituting a low frequency signal for the phase-detector output, and applying a fixed 400-cycle signal to the amplifier channel. Phase angles were obtained from Lissajous patterns by applying the output of the multiplier to one axis of an oscilloscope and the low frequency modulating signal to the other axis. The amplitude response was obtained by noting the attenuation required in the low frequency signal channel to give a constant output from the multiplier. The results of this test are shown in Figure 5.4. The amplitude response is flat up to 18 cps and then rises to a 4 db or 1.6 times peak at 50 cps, while the phase shift is 17 degrees at 10 cps and 90 degrees at 44.5 cps. In considering the phase characteristics of this channel of the multiplier it must be recalled that the output system still contributes approximately one degree per cycle to the phase shift so that the lag in the multiplier proper is only 7 degrees at 10 cps and approximately 45 degrees at 45 cps. Comparing these results with the characteristics given in Figure 5.1 it will be noted that the open-loop tests shown a lag of 40.6 degrees at 10 cps and 116 degrees at 45 cps. This reduction in lag is consistent with what might be expected with a loop gain of 44 db.

5.23 Transient Closed-Loop Tests

Figure 5.5 is a photograph taken from an oscilloscope and shows the transient which occurs in the 10 kcps control voltage appearing at the plate of the second 6AS6 for the case
Fixed 400-Cycle Input

Multiplier Unit ➔ Output System ➔ Oscilloscope

Attenuator

Low Freq. Signal Constant 2 Volts

Relative Gain db

0.1 1.0 10 100

Frequency CPS

250

200

150

100

50

0

10

15

20

Amplitude

Phase

Closed-Loop Characteristic of Control Channel of Electronic Multiplier

Figure 5.4
of zero 400-cycle signal applied to the amplifier channel of the multiplier and a positive square-wave of low repetition rate applied to the control channel in place of the phase-detector output. Figure 5.6 shows the control voltage appearing at the suppressors in this same case. For timing purposes a
207 cps signal was used to intensity modulate the beam of the cathode ray tube in this last case. These markers indicate a natural frequency for the system of approximately 50 cps.

Figure 5.7 shows the transient which occurs in the 400-cycle output when a 400-cycle signal is applied to the amplifier channel and a square wave to the control channel. This figure also indicates a natural frequency of approximately 50 cps, which seems quite reasonable in view of the 50 cps natural frequency indicated in Figure 5.4 for the control channel of the multiplier. Figure 5.7 also indicates an overshoot of approximately 31\% which corresponds to a damping ratio of about 0.5 \(^1\), or a circuit Q of approximately 1.2 \(^2\).

---

All three of these pictures of transient operation indicate nearly the same natural frequency in spite of the fact that the first two do not include the output filter. This is apparently due to the fact that the filter itself is quite highly damped (see Figure 4.15).
CHAPTER VI

Phase-Sensitive Detector, Power Supplies, and Mechanical Layout

6.1 Phase-Sensitive Detector

As was noted in Chapter II, a stable, linear, phase-sensitive detector, which produces very little phase delay between the demodulated output and the envelop of the input signal, is needed to demodulate one of the input signals for controlling the gain of the variable-gain amplifier.

So-called "phase-sensitive detectors" are employed whenever it is necessary to remove intelligence from an amplitude-modulated signal the carrier of which has been suppressed. If the correct modulation signal is to be derived from a signal of this type, it is first necessary to reinsert the carrier and thus convert the signal to a conventional amplitude modulated signal. After the carrier has been reinserted any conventional detector, possessing the desired characteristics as to signal handling capacity and linearity, can be used as the demodulator. This carrier voltage which is reinserted before demodulation will, in the remainder of this discussion, be referred to as the "reference voltage."

The essentials of a phase-sensitive detector are shown in Figure 6.1. Here the important point to note is that the voltage, $E_r$, applied to the rectifier is the algebraic sum
of the signal and reference voltages. This summing can be done either by connecting transformer windings in series, as shown in Figure 6.1, or by adding the voltages in a resistive summing network, as used in the phase detector shown in Figure 6.2.

A number of different phase-sensitive detectors have been designed, particularly for use in servomechanism systems, but these applications usually do not require a high degree of linearity over a wide operating range, the chief requirement being a relatively high speed of response. For this multiplier application, however, both a high degree of linearity and a high speed of response are required.

If the detector is not to introduce appreciable additional error, then a curve relating its output and input should

---

be linear to within ± 0.25% over a range of at least 250 to 1. Fortunately, this does not require that the rectifier itself operate over a range of 250 to 1. This can be seen by referring to Figure 6.1. Assume that the normal reference voltage used is 26 volts and that the rectifier operates over a range from 1 volt to 51 volts with the desired linearity. If the addition of a 50 millivolt signal to the normal reference gives the required signal-to-noise ratio, then the allowable signal range is from 50 millivolts to 25 volts. The phase-detector therefore operates over a range of 500 to 1, with the rectifier operating over a range of only 51 to 1. Improving the overall detector to allow operation with a smaller signal voltage would increase the operating range without requiring the rectifier to operate over a wider range.

In spite of the reduction pointed out above, the operating range is still large. From tests it therefore appeared that none of the detector circuits normally employed would be satisfactory but that a phase-sensitive detector employing feedback would be required. The circuit shown in Figure 6.2, therefore, was finally devised as an outgrowth of the feedback rectifier discussed in Chapter IV. This circuit employs two feedback rectifiers which are identical except that negative output is taken from one of the rectifier bridges while positive output is taken from the other. The same reference voltage is applied to each of the rectifier systems and the two outputs are summed in a resistive network. With zero
RESISTORS ½ WATT UNLESS OTHERWISE MARKED.

FEEDBACK PHASE-SENSITIVE DETECTOR
E.W. SCIFERT 4/10/47
signal input the summing circuit is adjusted so that zero voltage appears at the output of the cathode follower which provides the low impedance output desired from this detector.

Signal input is added to the reference input in the rectifier channel which provides a negative output. In this way, when a signal of the same sign as the reference (that is a positive input signal) is applied to the input, the output from the negative channel becomes larger than that from the positive channel and a negative output signal is obtained. This reversal of sign between input and output is required to compensate for the reversed control characteristics of the multiplier as discussed in Chapters III and IV. To prevent the signal input voltage from appearing in the second channel of this detector, the reference voltage should be derived from a source with an internal impedance of 500 ohms or less.

The largest range of operation is obtained from this detector if a reference of 25 volts is used, but the zero balance remains within 80 millivolts, referred to the input, if the reference is reduced to 8 volts. Because of lack of time it was not possible to make extensive tests on the linearity of this phase detector. However, the fact that the zero balance is reasonably independent of the reference level is an indication that the detector is very linear. Furthermore, the accuracy achieved should be nearly the same as shown in Figure 4.8 for the 10 kcps feedback rectifier used in the multiplier unit.
Tests were also conducted using a pair of Ar-6 amplifiers (Figure 4.13) with a 6AL5 rectifier in the feedback circuit of each. This arrangement gives a stabilization due to feedback of the order of 70 db and as a result the change in zero balance with charge in the reference level is less than 3 millivolts for any reference up to that which overloads the Ar-6. The minimum usable signal which this unit can detect is approximately 0.03 per cent of the reference signal (Ref = 8 volts). Since the maximum value of the signal equals the reference voltage the range of operation of this phase detector is approximately 3000 to 1. Considering the fact that the loop stabilization of the rectifier unit with the Ar-6s is 30 db higher than that obtained in the rectifier used in the multiplier unit, it appears that an accuracy of at least ± 0.2% should be attained over a signal input range of at least 1000 to 1.

It is necessary to filter the output of the phase-detector to remove voltage components of 400 cycles and above, but at the same time modulation components up to at least 10 cps should not be reduced in amplitude nor shifted appreciably in phase. Since the filter used at the output of the detector is not enclosed by any feedback loop attention can be focused on the phase characteristics obtained in the desired pass-band without regard to what takes place at frequencies above approximately 35 cps. With this freedom in mind it appeared that a multiple section, LC, low-pass filter, designed for as high a cut-off frequency as possible consistent with attaining the desired 400-cycle attenuation, offered the best
solution. The three section filter shown in Figure 6.2 was designed as a compromise between circuit complexity and performance. This unit produces a phase delay of approximately 0.7 degree per cycle for frequencies below 30 cps and at the same time gives an attenuation of 46 db at 400 cycles.

6.2 Power Supply Requirements

The multiplier requires 115 milliamperes at plus 225 volts, a bias supply of -150 volts capable of delivering 10 ma, and a 6.3 volt d-c, heater supply capable of furnishing 6 amperes. The plate and bias supplies should be well regulated and have a ripple content of 0.3 millivolt rms or less, if the full operating range of the multiplier is to be realized. The voltages chosen were standard in the DACL and the supplies used in testing the multiplier formed part of a series designed by the author.¹

As was noted in Chapter V changes in the heater supply voltage cause zero drift in the multiplier so a very stable source of heater voltage is necessary. The Sorenson "Nobatron" supply is quite satisfactory if mounted at a distance so that the strong magnetic fields which it produces do not cause pick-up in the multiplier.

The phase-detector requires 80 milliamperes at +300 volts and 25 milliamperes at -150 volts, along with a d-c heater supply of 2.5 amperes at 6.3 volts.

6.3 **Mechanical Layout.**

The laboratory model of the multiplier unit, shown schematically in Figure 4.16, was constructed on an 11 x 17 x 3 inch steel chassis. The unit is intended for standard relay rack mounting from a 7-inch panel, although some form of shock-mounting is recommended in order to reduce tube microphonics. The only special precaution taken in constructing the unit was to provide a shield around the cathode-follower-mixer stage and the output cathode follower. Considering Table V-1, and recalling that the voltage level at the output of the multiplier unit is only 1/100 of the values given in the table, the necessity of this shielding is apparent. It is particularly important to avoid extraneous coupling from the variable-gain amplifier stages into these output stages. Coupling of this type would cause an appreciable error since, as the gain of the amplifier channel is varied, the signal coupled into the output from this source changes from the value for which a balance was initially established.

The phase detector shown schematically in Figure 6.2 was constructed as a separate unit on a 7 x 11 x 2 inch steel chassis and was also intended for relay rack mounting from a 5\(\frac{1}{4}\) inch panel.

The output amplifier used in conjunction with this laboratory model of the multiplier contained its own power supply.
and, therefore, required a whole rack panel for mounting. However, if the multiplier were used as a component of the final computer the standard Ar-6 repeater amplifier would be used for the output. This unit mounts in one-half a rack-panel and the connections are arranged so that both the input transformer and the filter could be built as units which would plug into the front of the panel.

With this construction it would be possible to mount two of the multiplier units, complete with phase detector, output amplifiers and high voltage power supplies, in a standard six foot relay rack.
Conclusions and Recommendations

7.1 Operation of Complete Multiplier Including Phase Detector

Unfortunately, the phase detector was not completed in time to test the detector and multiplier as a unit, but the operation of the complete unit can be predicted by combining the characteristics of the phase detector given in Chapter VI, with the characteristics given in Figure 5.4, for the channel which uses the phase detector. At 10 cps the phase delays in the channel employing the phase detector are as follows:

<table>
<thead>
<tr>
<th>Delay in phase detector</th>
<th>7 degrees</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay in multiplier unit</td>
<td>8 degrees</td>
</tr>
<tr>
<td>Delay in output section</td>
<td>9 degrees</td>
</tr>
<tr>
<td>Total delay at 10 cps</td>
<td>24 degrees</td>
</tr>
</tbody>
</table>

Present tests indicate that static errors in the phase detector are considerably less than in the control channel of the multiplier so that accuracy of the control channel remains the limiting factor.

7.2 Comparison of Test Results and Specifications

The multiplier described in this thesis has met most of the requirements given in Section 1.4. As stated in Chapter V, both the range and the allowable speed of variation are considerably greater for the signal applied to the amplifier channel of the multiplier than for the signal applied to the channel requiring the phase detector. Because of this difference care
should be taken when "setting up" problems if the greatest accuracy is to be achieved from the multiplier.

Table VII-1 compares the important characteristics obtained for the multiplier with the specifications given in Chapter I.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Obtained</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Allowable Range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal No. 1</td>
<td>±5000 to 1</td>
<td>±250 to 1</td>
</tr>
<tr>
<td>Signal No. 2</td>
<td>±250 to 1</td>
<td>±250 to 1</td>
</tr>
<tr>
<td>Allowable output Range</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±5000 to 1</td>
<td>±1000 to 1</td>
</tr>
<tr>
<td>Accuracy over top quarter of Range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal No. 1</td>
<td>±1%</td>
<td>±1%</td>
</tr>
<tr>
<td>Signal No. 2</td>
<td>±1%</td>
<td>±1%</td>
</tr>
<tr>
<td>Phase Shift from Input to Output at 400 cycles</td>
<td>0 degrees</td>
<td>0 degrees</td>
</tr>
<tr>
<td>Phase Delay at 10 cps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Amplifier Channel</td>
<td>11 degrees</td>
<td>5 degrees</td>
</tr>
<tr>
<td>Control Channel, including phase detector</td>
<td>24 degrees</td>
<td>5 degrees</td>
</tr>
</tbody>
</table>

It is thus seen that one channel exceeds the delay specifications set down for the multiplier, in Chapter I, by a factor of 2 to 1, while the second channel is considerably slower, exceeding the delay specification of 5 degrees at 10 cps by nearly 5 to 1. Furthermore, the total delay in the system is quite equally divided between the phase-detector, the multiplier unit and the output section, so that if the delay is to be reduced significantly, all three parts of the system must be considered.
The delay in the phase detector occurs in the filter needed on its output to eliminate ripple voltages. Further study of this filter system may reveal ways to reduce the delay, but it is questionable if sufficient filtering can be obtained and still produce a delay of less than 5 degrees at 10 cps.

At low modulation frequencies the delay produced in the multiplier unit itself is governed to a large extent by the loop gain of the system, the characteristics of the lag network required to achieve loop stability, and the characteristics of the filter required to remove 10 kcps ripple at the output of the feedback rectifier. An increase in the pilot frequency used would probably permit a reduction in delay because of the larger separation between the modulation and pilot carrier frequencies. Furthermore, increasing the pilot frequency would allow the use of a broader band-pass filter ahead of the feedback rectifier. This broader filter would have a smaller phase slope through the center of its pass-band and would be significant in reducing the phase delay at the higher frequencies. These changes, along with a proper modification of the phase correcting networks in the error amplifier would undoubtedly permit a higher loop gain with a corresponding improvement in the closed loop characteristics. It is quite possible that the delay in the multiplier unit could be halved by making these changes.
The phase delay which occurs in the output system of the multiplier takes place almost entirely in the 400-cycle band-pass filter employed. For a filter of a given configuration, the phase slope near the middle of the pass band varies inversely with the bandwidth of the filter. The filter at present used in the output system was designed to have a pass band from 275 cps to 550 cps and gave a phase slope of 0.9 degree per cycle through the center of the pass band. The large amount of attenuation achieved at frequencies below 20 cps and at 10 kcps indicates that the filter would probably still be satisfactory if redesigned for twice the present bandwidth. In this event the phase slope would drop to approximately 0.45 degree per cycle.

It appears quite possible to achieve a delay of 5 degrees at 10 cps for the amplifier channel and 13 or 14 degrees at 10 cps for the control channel, including the phase detector, with no sacrifice in the present static accuracy of the multiplier.

7.3 Recommendations for Further Development

It is felt that the multiplier described in this thesis should operate in a satisfactory manner as a component of a high speed, relatively high accuracy analogue computer. However, a number of improvements could certainly be made. Several suggestions for improvement have been made earlier in this thesis. These will be repeated here, along with several additional recommendations.
(1) The use of a pilot signal frequency of the order of 25 or 30 kcps should be investigated.

(2) Further means for improving the gain-phase characteristics of the feedback loop should be studied.

(3) A Miller circuit should be incorporated in the error amplifier to reduce the effect of changes in heater voltage.

(4) Wire-wound resistors should be used in the critical points of the circuit.

(5) The output filter should be redesigned with as wide a pass-band as can be used and still achieve the desired rejection for pilot frequency signal and signal at modulation frequency.

(6) Cathode followers with greater stabilization should be used for summing the balance signal and the amplifier output, and as an output tube from the multiplier unit.
APPENDIX I

Analysis of Amplifier Stage with RC Feedback to Grid

The 6AC7 stage employed in the error-signal amplifier of Figure 4.10 can be represented by the figure shown below.

If the input impedance of the \( \mu \) section of the above amplifier is assumed infinite, then the current, \( i \), is given by

\[
i = \left( \frac{1}{R_2 + \frac{1}{Z}} \right) (E_{in} - E_o)
\]

but \( E_o = \mu E_g \)

and \( E_g = E_{in} - i R_2 \)

Therefore \( E_g = E_{in} - R_2 \left( \frac{1}{R_2 + \frac{1}{Z}} \right) (E_{in} - \mu E_g) \).
Solving for $E_g$ yields,

$$E_g = E_{in} \left( \frac{\omega}{R_2(1 - \mu) + \omega} \right)$$

So

$$E_o = \mu E_g = E_{in} \left( \frac{\mu}{1 + \frac{R_2}{\omega}(1 - \mu)} \right). \quad (1)$$

If $\omega$ is the parallel combination of $R_1$ and $C$ as shown above then

$$\omega = \frac{R_1}{1 + j\omega C}.$$  

Furthermore, if $\mu$ is made negative, then

$$\frac{E_o}{E_{in}} = \frac{-|\mu|}{\left[ 1 + \frac{R_2}{R_1}(1 + |\mu|) \right] + j\omega R_2 C (1 + |\mu|)} \quad (2)$$

If $\mu$ in equation (2) is made considerably larger than 1, then

$$\frac{E_o}{E_{in}} = \frac{-|\mu|}{\left[ 1 + |\mu| \right] \frac{R_2}{R_1} + j\omega |\mu| R_2 C}.$$  

From this equation it can be seen that as $\omega$ becomes large the angle of the denominator approaches $+90^\circ$ so $E_o$ lags $E_{in}$ by $90^\circ$ more at $\omega = \infty$ than at $\omega = 0$ and $E_o/E_{in}$ becomes very small for large values of $\omega$. 