DISCLAIMER NOTICE

Due to the condition of the original material, there are unavoidable flaws in this reproduction. We have made every effort possible to provide you with the best copy available.

Thank you.

The following pages were not included in the original document submitted to the MIT Libraries.

This is the most complete copy available.

p.113
Design and Simulation of a 20 Gbps Communication Channel

By
Abigail Rice

Submitted to the
Department of Electrical Engineering and Computer Science
May 22, 2015
In Partial Fulfillment of the Requirements of the Degree of
Master of Engineering in Electrical Engineering

Abstract
Digital wire-line communication speeds are increasing rapidly to achieve ever higher data rates. Speeds beyond 20Gbps are desirable for the next generation of protocols. However, higher frequency signals experience more loss due to the physical channel and are more sensitive to small imperfections in the channel, such as vias. In this work, an existing communication channel between two controller boards across a midplane was improved to allow for operation at a higher frequency. Mentor Graphics HyperLynx was used to simulate the channel and display S-parameter models and eye diagrams to demonstrate the impact of various designs. The effects of the material properties, impedance of the traces, and vias were simulated and the results combined to determine what physical layer improvements must be made to reduce loss and reflections at this high frequency.

MIT Thesis Supervisor: Luca Daniel
Associate Professor, Department of Electrical Engineering and Computer Science

Company Thesis Supervisor: Alan Pfeifer
Manager, Hardware Engineering
Acknowledgement

My sincere thanks to Alan Rymph, my VI-A company advisor for teaching me signal integrity and being a great mentor throughout the research process. Your guidance shaped so much of this thesis and how I approach research.

I would also like to thank Alan Pfeifer, David Hyde, and Robert Stubbs at NetApp for answering my questions and guiding me on choosing a topic. I would also like to thank Steve Miller, Senior Technical Director at NetApp for his continual support.

Last but not least thank you to my MIT faculty supervisor, Prof. Luca Daniel for being willing to supervise my thesis and for introducing me to signal integrity theory.
# Table of Contents

- Abstract.......................................................................................................................... 2
- Acknowledgement ........................................................................................................... 3
- Table of Contents ............................................................................................................ 4
- List of Figures .................................................................................................................. 7
- List of Tables .................................................................................................................... 7
- 1 Introduction .................................................................................................................. 8
  - 1.1 Motivation and Problem Statement ...................................................................... 8
  - 1.2 Objective ................................................................................................................ 9
- 2 Theoretical Basis ............................................................................................................ 9
  - 2.1 Differential Transmission Line Theory ............................................................... 10
    - 2.1.1 Impedance of a transmission line ................................................................. 10
    - 2.1.2 Capacitance ................................................................................................... 11
    - 2.1.3 Inductance ...................................................................................................... 11
    - 2.1.4 Calculating Differential Impedance .............................................................. 12
    - 2.1.5 Reflection ....................................................................................................... 12
  - 2.2 Printed Circuit Board Design ................................................................................ 14
    - 2.2.1 Conductive Copper Layers .......................................................................... 15
    - 2.2.2 Insulating Dielectric Layers ........................................................................... 16
  - 2.3 Via Design ............................................................................................................... 17
    - 2.3.1 Anatomy of a Via ........................................................................................... 17
    - 2.3.2 Impedance of a Via ....................................................................................... 19
  - 2.4 Electrical Properties of Materials ......................................................................... 19
    - 2.4.1 Dielectric constant ......................................................................................... 19
    - 2.4.2 Dissipation factor .......................................................................................... 21
    - 2.4.3 Frequency dependence of Df and Dk .............................................................. 23
  - 2.5 Attenuation of the signal ....................................................................................... 24
    - 2.5.1 Resistive loss comes from the inherent resistivity of copper ......................... 26
    - 2.5.2 Dielectric loss comes from the absorption of the surrounding dielectrics ...... 28
  - 2.6 Measuring Signal Quality ..................................................................................... 29
    - 2.6.1 Frequency Domain – S-Parameters ............................................................... 30
    - 2.6.2 Time Domain—Eye Diagrams ....................................................................... 33
- 3 Technical Approach .................................................................................................... 34
3.1 Path Design .................................................................................................................... 34
3.2 Schematic Creation ......................................................................................................... 35
   3.2.1 SPICE Driver Models .......................................................................................... 35
   3.2.2 PCB Trace Models ............................................................................................... 36
   3.2.3 Via Modeling ........................................................................................................ 36
   3.2.4 Connector Models ............................................................................................... 36
3.3 Simulation Approach ..................................................................................................... 37
3.4 Resources ....................................................................................................................... 38
   3.4.1 Mentor Graphics HyperLynx ............................................................................... 38
   3.4.2 Information Resources ........................................................................................ 38
4 Results .................................................................................................................................. 38
4.1 Dielectric Material.......................................................................................................... 38
   4.1.1 What is a better material? ..................................................................................... 39
   4.1.2 Dielectric Constant affects the impedance of the traces ...................................... 40
   4.1.3 Effects of the Material on Loss ............................................................................ 41
   4.1.4 Material Choices .................................................................................................. 43
   4.1.5 Effects of the Material on the Maximum Length of the Trace ............................ 49
   4.1.6 Effects of the Material on the Vias ...................................................................... 51
   4.1.7 Controller Via Impedance .................................................................................... 53
   4.1.8 Controller Via Insertion Loss .............................................................................. 56
   4.1.9 Comparison to the Midplane Vias ...................................................................... 58
   4.1.10 Combined Effects of the Material on the Full Path ............................................ 59
4.2 Resistive loss ................................................................................................................. 65
   4.2.1 Effects of Geometry on Differential Impedance .................................................. 66
   4.2.2 Effects on Resistive Loss –Bigger is Better......................................................... 68
   4.2.3 Varying Two Factors to keep the Impedance Constant ....................................... 71
   4.2.4 Separation to Width Ratio .................................................................................... 73
   4.2.5 Impact on the Full Schematic .............................................................................. 73
4.3 Impedance Control ......................................................................................................... 76
   4.3.1 Effect of an impedance discontinuity ..................................................................... 77
   4.3.2 Multiple Discontinuities ....................................................................................... 78
   4.3.3 Controller Impedance Tolerance ........................................................................ 82
   4.3.4 Full Path Impedance Tolerance ........................................................................ 87
4.4 Via design ....................................................................................................................... 89

Rice 5
4.4.1  Stub Length............................................................................................................. 90
4.4.2  Via Drill Size and Spacing.................................................................................. 92
4.4.3  Via Pad Size............................................................................................................ 94
4.4.4  Via Antipad Size..................................................................................................... 96
4.4.5  Return Vias ............................................................................................................ 97
4.4.6  For an impedance of 100 Ohms, what gives the lowest loss? ......................... 99

5  Conclusion and Future Work...................................................................................... 104
6  References.................................................................................................................. 106
7  Appendix..................................................................................................................... 107
8  Appendix B – Schematic Diagrams............................................................................ 114
List of Figures

Figure 1 A diagram of a sample PCB stack up .......................................................... 15
Figure 2 Alignment of the dipoles in a dielectric material with the electric field .......... 20
Figure 3 The signal velocity is proportional to $1/\sqrt{\varepsilon k}$ and the time delay is the inverse .... 21
Figure 4 Frequency dependence of the real and imaginary parts of the dielectric constant .... 24
Figure 5 Circuit model of one section of lossy transmission line .................................. 25
Figure 6 Attenuation of the signal per inch ............................................................... 26
Figure 7 Diagram of a cross-section of an inner differential pair .................................. 27
Figure 8 Dielectric loss from the dielectric constant .................................................. 29
Figure 9 The Dielectric Constant affects the single-ended impedance of the trace as $1/\varepsilon_k$ .. 40
Figure 10 The trace width can be increased to compensate for a lower dielectric constant .... 41
Figure 11 Simulated dielectric loss for dielectric constant and dissipation factor ............. 42
Figure 12 Effects of the material properties on the total loss ....................................... 43
Figure 13 The attenuation per inch of a stripline trace using various materials ............... 45
Figure 14 Loss graphed against the dielectric constant and the dissipation factor ........... 45
Figure 15 Effect of the dielectric constant and dissipation factor .................................. 48
Figure 16 Eye Diagram collapse for selected materials ............................................... 49
Figure 17 Insertion loss over different lengths for the selected materials ....................... 50
Figure 18 Impedance of the vias using the TDR simulator ......................................... 54
Figure 19 Effects of the material on the Via impedance ............................................. 55
Figure 20 Via Entry impedance increases with lower $\varepsilon_k$ ........................................ 56
Figure 21 Via differential insertion loss for selected materials ...................................... 57
Figure 22 Effects on the midplane vias ...................................................................... 59
Figure 23 Insertion loss of the full path ................................................................. 61
Figure 24 Return Loss data for the full path schematic .............................................. 62
Figure 25 Eye Diagram for the full path ................................................................. 63
Figure 26 Eye Diagrams for IS415, EM888, and MegTron7 ......................................... 64
Figure 27 Rise time of the signal through the full path ............................................... 65

List of Tables

Table 1 Matrix of standard and mixed-mode S-Parameters .......................................... 32
Table 2 Summary of the materials investigated .......................................................... 44
Table 4 Maximum length of a trace for a budget of -16 dB .......................................... 51
Table 5 Rise Time degradation from the material ....................................................... 65
Table 1 Effect of increasing a test variable when compensated by each of the other factors .. 71
Table 6 Different cases of impedance tolerance investigated ..................................... 87
1 Introduction

Information technology is advancing at a very fast pace and has been driving faster and faster data speeds. Of the many IO standards in use today, the fastest two used for high-performance data storage are PCIe and SAS. The current systems are generation 3, with PCIe Gen 3 running at 8 Gbps and SAS3 at 12 Gpbs. But as good as these are, the current data rates are still a bottleneck of many systems so even faster systems will be required in the near future. Every generation of these protocols has doubled the data rate, and PCIe Gen 4 is expected by be 16 Gbps and SAS 4 20-24 Gbps. However, higher speed signals have more loss and tighter jitter constraints due to the skin effect, reflections, and dielectric materials, so current PCB designs will no longer be adequate. Higher quality materials, improved via and trace design, and tight impedance control will all be necessary to enable these higher speeds. The goal of this thesis is to design a higher quality interconnect capable of delivering data at speeds of 16-20 Gbps.

Chapter 1 details the background and motivation for this work, then a review of the theoretical concepts required for this work is given in chapter 2. Chapter 3 explains the process used to create and analyze the channel. Simulation results are given in chapter 4. Chapter 5 is a discussion of the work and possible future research.

1.1 Motivation and Problem Statement

Current speeds for PCIe Gen 3 go up to 8 Gbps and SAS3 to 12 Gbps. To get a higher amount of data throughput, either many parallel channels must be used or each one must become faster. In the near future, fourth generation protocols will be developed which will seek to double to current data transfer rate. This is accomplished by a mixture of a more efficient encoding scheme and by improvements to the psychical layer allowing for a higher signaling
frequency. At the time of this work, the full specifications for the next generation of SAS 4 and PCIe Gen. 4 have not been created. However, to attain a higher data rate an improved physical channel must be designed. The physical layer is largely independent of the precise timing, encoding, and other specifications of SAS or PCIe. This thesis explores the various challenges associated with higher bandwidth interconnects and suggests improvements for creating a channel running at a bandwidth up to 10GHz, which corresponds to a 20Gbps data rate.

1.2 Objective

The goal of this work is to design a physical interconnect with a bandwidth of 10GHz and an acceptable amount of loss and reflections. The channel is between two controller boards connected by a midplane. Many different aspects of the design affect the performance of the overall interconnect, but for this work three major areas are examined that contribute significantly to signal integrity issues. The focus is on the total loss due to the dielectric material, impedance discontinuities along the path, and the incorporation of vias.

2 Theoretical Basis

This work relies on a detailed knowledge of signal integrity concepts. It is important to understand the essential principles of transmission lines, reflections, loss, and how the PCBs are manufactured.

Signal Integrity refers to the quality of an electrical signal. Information is converted to a voltage signal that is sent down the transmission line. Ideally, it would arrive at the other end of the path exactly as it was sent. However, the signal is distorted by noise, reflections, and losses. Electrical noise is added to the signal from outside sources, which could be nearby signals
(referred to as crosstalk), from the physics of the devices and traces, or from EM waves from outside travelling near the trace and inducing a voltage. Reflections occur when the signal sees some change in the path that causes the wave to bounce around and distort the voltage. Loss occurs from the signal travelling through real materials that absorb some energy and convert it to heat.

This chapter describes the technical background needed for the reader to understand the results of the simulation work. It briefly describes transmission lines, the design of current PCBs, sources of loss, and two of the major methods used to measure signal integrity.

2.1 Differential Transmission Line Theory

Most high-speed signals are transmitted as a differential voltage using a differential transmission line. Differential transmission lines are created with two conductive traces by applying a complementary voltage (a positive signal and the negative signal). One advantage is that this method will reject most noise, if it is common to both traces. Both lines will experience the same noise, so when one is subtracted from the other, the noise will cancel out. The complementary line also provides a nearby path for the return current.

2.1.1 Impedance of a transmission line

The impedance of a signal path describes how the signal will respond to, or impede, an incoming signal. Voltages and currents are affected by the resistance, capacitance, and inductance of the connection. Both the AC waveform’s magnitude and phase will be affected. Similar to resistance, it is defined as the ratio of the voltage to the current of the signal travelling in a particular direction. This means that the forward voltage is equal to the impedance times the forward current, but the total voltage/current need not be equal to the impedance if there are
reflections and multiple waves. The characteristic impedance of a transmission line is 
\[ Z_0 = \frac{L}{\sqrt{C}} \]
related to the inductance and capacitance of the line.

2.1.2 Capacitance

The capacitance primarily measures the response of the transmission line to the electric
field created by the propagating signal. An electric field is created by the voltage on the
conductor and spreads outward towards other conductors. The amount of electric field that the
transmission line creates is determined by its geometry and the dielectric constant. Just as in a
parallel plate capacitor, the capacitance is proportional to the surface area of the conductors and
inversely proportional to the distance between them. This means that increasing the trace width
or thickness will increase the capacitance and increasing the separation or the dielectric height
will decrease it.

When a transmission line passes through a non-uniform material, such as on the top of a
PCB where half is in air and half inside the dielectric of the board, the dielectric constant is an
effective dielectric constant that the signal sees in all of the volume it passes through.

2.1.3 Inductance

Inductance primarily measures the response of the transmission line to the magnetic field
looping around the conductors. The inductance is defined by the area of the current loop and the
magnetic permeability. In PCBs, magnetic materials are rarely used so the relative permeability
is 1. The loop area includes the entire path—signal and return—and depends heavily on the height
of the dielectric and the proximity of the return path to the signal path. For example, if there is a
break in the ground plane beneath a signal, the return current must flow all the way around the
gap instead of close under the trace. This increases the inductance of the loop. Impedance
therefore depends on four major geometric factors: the width of the trace, the spacing between traces, the height of the dielectric, and the thickness of the copper trace.

### 2.1.4 Calculating Differential Impedance

The differential impedance of a trace can be approximated with the equation:

\[
Z_o = \frac{120}{\sqrt{Dk}} \times \ln\left(\frac{1.9(2h + t)}{0.8w + t}\right) \times \left(1 - 0.374e^{-29.5s/2h+t}\right)
\]

Where:
- \(h\) = dielectric height in mils (symmetrical)
- \(t\) = copper thickness in mils
- \(w\) = trace width in mils
- \(s\) = separation between traces (mils)

Single ended impedance (SE \(Z_o\)) is the impedance of one uncoupled trace and the diff \(Z_o\) refers to the differential impedance of the trace pair.

### 2.1.5 Reflection

When a signal propagates down an ideal uniform transmission line, it creates exactly the same electric and magnetic fields down the length and the signal arrives at the other side exactly as it was sent. However, if there is a change in impedance, the signal will be distorted. This is because the signal is travelling as a wave that must remain continuous, so no sharp rises or drops are allowed since that would require an infinite electric field. As long as the path is passive, the current must remain constant throughout otherwise there will be a sink or source of charge. But the current and voltage in the line are related by the impedance, so if the impedance on one side is different than the impedance on the other side, the current and voltage must also logically change. This is what creates a reflected wave travelling backward to keep the voltage and current continuous.

The boundary conditions require that the voltage be the same on both sides. This is from Guass’s law, \(\nabla \cdot \vec{E} = \frac{\rho}{\varepsilon_0}\), that the divergence of the electric field is equal to the enclosed charge.
When this is taken across a passive boundary (with no net charges built up inside), the total divergence must be zero. This means that the electric field in one direction is equal and opposite the electric field in the other direction. And since $\vec{E} = -\nabla V$, when the electric field is zero, the gradient of voltage must also be zero and so the voltages are the same on either side of the boundary. Therefore $V_{inc} + V_{refl} = V_{trans}$. The current must also be the same across the boundary. This is because the current is a flow of charge, and charge cannot be built up in a passive structure. These conditions will force a new voltage and current waveform to be created travelling in the opposite direction. One example voltage waveform is given below in figure 1, showing both the near end and far end voltages for an ideal case and a case with a large impedance discontinuity.

Voltage waveforms for an ideal channel and a channel with a large reflection

![Figure 1 Reflected voltage waveforms. The discontinuity creates a reflected voltage signal that travels backwards toward](image-url)
the near end. The transmitted voltage is reduced until the reflection has time to reflect again off the source impedance and travel back down the channel to the endpoint. Thus the far end does not reach the true voltage until more than three time delays.

Signals get distorted when they encounter a change in impedance. When there is a boundary between two different impedances (such as a change in the cross-section of a trace), some of the signal reflects and some gets transmitted. The ratio of these parts depends on the difference in impedance. Reflected signals travel back down the line in the opposite direction of the original signal. They can either add or subtract from the voltage amplitude. If there are multiple such boundaries, reflections can bounce back and forth and build up. It is therefore important to keep the impedance constant along the entire path, especially at the two ends of the channel called terminations. This will minimize any reflected signal and keep the information in the signal preserved.

2.2 Printed Circuit Board Design

PCBs are made of stacked layers of copper foil in between insulating dielectrics. To create a PCB, first glass fabrics are filled with liquid resins and partially cured. This is often called pre-preg (pre-impregnated). Cores are formed with layers of glass and resin with a copper foil on each side. PCBs are made with alternating core/pre-preg layers such that there is a layer of dielectric insulating nearby copper signal layers. The foil on each side of the cores is etched to create the design of the traces and pads of the board, and then stacked with a pre-preg layer, then another core, and so on. The stack is heated and pressurized to cure.
Figure 2 A diagram of a sample PCB stack up showing the copper layers, insulating layers, and the placement of signal and plane layers.

2.2.1 Conductive Copper Layers

Copper is the conductive metal most commonly used in circuit boards. Copper foil is formed through electro-deposition or rolling copper to a uniform thickness sheet. The thickness of the sheet is measured by the weight of the foil over a one square foot area. Common weights are 0.5 ounces and 1 ounce (higher weight copper foils are thicker). The thickness of the copper is important for design because it affects the impedance of the trace, the resistance of the trace, and the amount of current the trace can carry. Thicker copper has less resistance (and hence less conductive loss), higher current carrying capacity, but lower characteristic impedance.
There are two main functions of the copper layers: to connect the signals and to provide power and ground connections. Most high speed signals are routed as a differential pair in between two reference planes. The power and ground are delivered by the planes of copper so they have the lowest impedance and highest ability to carry the current. Often, the signal layers are routed with thinner copper than the planes because they do not need to carry as much current. Also thinner copper has better impedance control because it is easier to etch a thin foil more uniformly. The top and bottom layers are necessary to connect the traces to the devices mounted on the surfaces, but these layers are not desirable for high speed routing because there is more cross talk and less control on the width and thickness.

Typically copper foil is treated on the surface to improve the adherence to the resin layers. Small bumps in the copper provide a much better grip for the resin and prevents sliding or delaminating. However, the uneven surface also has more loss. This is because the current traveling on the outer surface has to traverse all the hills and valleys which lengthens the path and increases the resistance. Surface roughness does cause more resistive loss, but it is not considered in this study.

2.2.2 Insulating Dielectric Layers

The dielectric is the insulating material between the copper layers to isolate the signals and provide structural support to the board. Generally these layers are composed of a fiber glass woven cloth impregnated with some type of resin. Glass cloth comes in many different styles for different thicknesses, fiber density, and resin content. Glass often has a high dielectric constant compared to the resin, so the overall dielectric constant of the material is dependent on the percentage of resin in the layer as well as the characteristics of the resin itself.
There are many different types and compositions of resins. Their function is to fill all the space between the layers and provide adhesion between the glass and the copper foil. Electrically, the most important characteristics are the dielectric constant (Dk) and the dissipation factor (Df), which contribute to the impedance and loss of the board. When doing a full design, the mechanical and thermal properties should also be considered, but they are not a part of signal integrity simulations. The dissipation factor is the most critical variable in determining the performance of traces on the board. Df can be correlated with the attenuation per length and thus defines how long the trace can span and still maintain good signal integrity.

2.3 Via Design

Vias are used to connect traces on different layers of the PCB. They often cause signal integrity problems in high speed lines because the impedance of the trace does not match the impedance of the via, which causes reflections. The best way to reduce these reflections is to match the impedance of the via as close to the trace as possible.

Another signal integrity issues with vias is the potential for stubs. Stubs are extra metal connected to the trace so that the signal splits, travels down the stub, reflects of the end, and then mixes with the original signal with a phase delay due to the extra length it had to travel. The worst case is when the stub length is \( \frac{1}{4} \) the wavelength, so a full trip is half and the phase is exactly out of phase and the two signals cancel. This problem can be avoided by backdrilling the vias to remove these stubs.

2.3.1 Anatomy of a Via

Vias are more complicated structures than the traces. To create a via, the board is first drilled with a small drill bit. Then the hole is plated with copper, leaving a smaller diameter hole. On
layers where there are traces that must connect, circular rings called pads are used to create a better contact and to ensure the trace will still connect with slight alignment errors. All other layers must not contact the via, so antipads are etched away on the plane layers. A differential via has two barrels running through the board, pads on the layers with connecting traces, and antipads on the other layers.

Figure 3 Via Design. The top view is on the left, looking at the top of the board with an incoming differential pair connecting to a via pair. The blue represents the ground plane. The diagram on the right is a cross-section of the same via showing the different layers the via passes through. In this case, the via enters on the top layer and exits on signal layer 7, leaving a short stub on the end. Important dimensions have been labeled.
2.3.2 Impedance of a Via

The impedance of a via is determined by the geometry of the via and the material surrounding the via. The most important parameter is the spacing to drill size ratio (s/D). The other factors affect the excess capacitance the via sees, and are lumped together as Dkeff. This is not simply the Dk of the material, but it also involves the antipad size, the pad size, the number of pads, and the stackup. One approximation for the impedance of a via is:

\[ Z_0 = \frac{120}{\sqrt{D_{keff}}} \ln \left( \frac{s}{D} + \sqrt{\left( \frac{s}{D} \right)^2 - 1} \right) \]

where \( s/D \) is the spacing to drill size ratio and Dkeff is the effective dielectric constant.

2.4 Electrical Properties of Materials

2.4.1 Dielectric constant

The dielectric constant is a measure of how a material responds to an electric field, also called the permittivity. When an electric field is present, the field exerts a force on the positive and negative charges within the material (ions, polar molecules, and electrons). The molecules line up their charges with the direction of the field, as depicted in Figure 2. Each dipole's small electric field is then added to the external electric field, and the field gets stronger.
Dipoles aligned with the electric field

Figure 4 Alignment of the dipoles in a dielectric material with the electric field. The flux density increases, the capacitance gets larger, and the signal slows down. The movement of the dipoles causes a small current to flow to the ground plane.

Often, the term “dielectric constant”, or Dk, actually refers to the relative permittivity ($\varepsilon_r$) defined where 1 is the permittivity of a vacuum ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m). Air is very close to this value, but all other materials have a higher dielectric constant because of the presence of charges inside the material. A related factor is the permeability, which defines how the material responds to magnetic fields. But for most materials, the permeability is the same as the permeability for a vacuum ($\mu_0 = 4\pi \times 10^{-7}$ Vs / Am), so the relative value is treated as 1.

The permittivity and permeability define the speed of light in a material. The speed of light, c, is constant in a vacuum but slows down in media due to the extra interactions of its electric and magnetic fields. One way to explain it is by thinking of the dielectric constant as increasing the capacitance the signal sees down the line. As it propagates, it must charge up all the capacitors distributed in the material which takes longer with larger capacitors. The permittivity of a vacuum is defined as:

$$c = \frac{1}{\sqrt{\varepsilon_0 \mu_0}}$$

Rice 20
Since magnetic materials are not typically used in PCBs, the speed of signals can be simplified to:

\[ v = \frac{c}{\sqrt{Dk}} \]

![Velocity graph](image1)

![Time Delay graph](image2)

**Figure 5** The signal velocity is proportional to \(1/\sqrt{Dk}\) and the time delay is the inverse, \(\sqrt{Dk}\). Higher dielectric constants increase the capacitance and slow the propagation of the signal.

### 2.4.2 Dissipation factor

Dissipation factor is basically a measure of how many dipoles are in the material and how far each of them can move. The dielectric constant describes how the capacitance is increased by the dipoles present. How the dipoles move inside a material is strongly dependent on how they are attached to the polymer backbone and the mechanical resonance. Thus the more cross-linked the polymer is, the less the molecules can move around, and the lower the dissipation factor.

The movement of dipoles causes loss as it converts the electrical energy into mechanical energy and then into heat. This is exactly how a microwave oven works; the electromagnetic wave at 2.45 GHz aligns the water molecules in food, causing them to move back and forth with the field and absorb the electric energy of the field and convert it to heat. In a PCB, the same
mechanism occurs, but the dissipation factor is much lower so only a small part of the energy is lost and very little heat is produced.

Mathematically, $D_f$ comes from the complex nature of the dielectric constant. The current through an ideal capacitor is always 90° out of phase with the voltage, $I = C \frac{dV}{dt}$. When complex number notation is used, the current through a capacitor is purely imaginary, $I = j\omega \varepsilon_r C_0 V$. This describes an ideal, lossless capacitor between the trace and the reference plane.

However, there is also a loss or leakage current that is flowing in phase through the dielectric from the motion of the dipoles. When the dipoles move back and forth, they create an AC current in phase with the voltage. This behaves like a resistor, and real current flows across the dielectric. Both arise because the dielectric constant is actually a complex number, $\varepsilon_r = \varepsilon_r' - j \varepsilon_r''$, where $\varepsilon_r'$ is the real part of the constant ($D_k$) and $\varepsilon_r''$ is the imaginary part of the constant. Using this notation, the current through the lossy capacitor is:

$$I = j\omega \varepsilon_r C_0 V = j\omega (\varepsilon_r' - j \varepsilon_r'') C_0 V = j\omega \varepsilon_r' C_0 V + \omega \varepsilon_r'' C_0 V$$

The imaginary part of the current creates the capacitive effects where the current is out of phase with the voltage and the real part describes the leakage current where the current is in phase. The real part of the dielectric constant, $\varepsilon_r'$ or Dk, contributes to the out of phase part (capacitor) and the imaginary part, $\varepsilon_r''$, contributes to the in phase part (resistor). The leakage resistance is related to the dissipation factor and the frequency. As the frequency increases, the dipoles move the same distance, but faster so the current increases and the conductivity increases.
The precise definition of the dissipation factor comes from the complex dielectric constant described as a vector in the complex plane. The angle of the vector with the real axis is called the loss angle, $\delta$. The ratio of the imaginary part to the real part, or the tangent of the angle, is called the dissipation factor or loss tangent.

$$Df = \frac{\delta}{\tan(\delta)} = \tan(\delta) = \frac{e''}{e'}$$

Basically, the two factors describe the response of the dipoles to an electric field. The dielectric constant is how much the aligning of the dipoles increases the capacitance and the dissipation factor describes how much movement there is and the amount of loss.

### 2.4.3 Frequency dependence of $Df$ and $Dk$

Both the dielectric constant and the dissipation factor are also frequency dependent. In real materials, mechanical limitations mean that the dipoles cannot move the same for all frequencies. Effectively, there is a slight decrease in the angle the dipole rotates through. At high frequencies, the dipoles do not respond as fast so the dissipation factor is slightly less. However, in typical materials the frequency dependence is fairly small and can safely be ignored in most simulations.

The dielectric constant is also dependent on the frequency. If the dipoles at high frequency do not get to the full angle they would at a lower frequency, the alignment of the fields is reduced and the effect on the capacitance is smaller. This means that the dielectric constant also decreases with frequency. The amount of this frequency dependence is based on how tightly the dipoles are held, i.e. the dissipation factor. Molecules that are tightly held will have
less variation with frequency. A loosely held dipole will swing wide at low frequency but will be unable to at high frequency. Therefore $D_f$ is an indication of the slope of $D_k$ with frequency.

$$E = E' + iE''$$

![Diagram of dielectric constant components](image)

**Figure 6 Frequency dependence of the real and imaginary parts of the dielectric constant.**

One consequence of the variation of the dielectric constant with frequency is that the signal velocity is also frequency dependent. This implies that the higher frequency parts of the signal will travel faster than the lower frequency components. The signal will spread out over time and length, called dispersion. Dispersion is bad for signal integrity, but the part from the frequency dependence of $D_k$ is often small compared to the dispersion caused by loss – higher frequencies have much greater loss than low frequencies. This creates a longer rise time as the signal propagates.

### 2.5 Attenuation of the signal

Attenuation is the loss of a signal as it propagates down a medium. If the attenuation is too high, the data cannot be effectively detected and the transmission has failed. Loss is observed as a drop in the voltage from one end of an interconnect to the other, but is really a decrease in
the power of the signal. The ratio of the two powers is often expressed in deciBels, the log of the ratio. Since power is proportional to the square of the voltage, the ratio can also be expressed in terms of the ratio of the voltages from one end to the other.

\[ \text{Ratio(dB)} = 10 \times \log \frac{P_1}{P_0} = 10 \times \log \frac{V_1^2}{V_0^2} = 10 \times 2 \log \frac{V_1}{V_0} = 20 \log \frac{V_1}{V_0} \]

The amount of attenuation of a signal within a PCB can be broken down into two parts, the resistive loss from the conductors and the dielectric loss.

Attenuation comes from a lossy transmission line. The ideal transmission line with only inductance and capacitance does not have any loss, and the signal will remain at the same amplitude all the way down the line (assuming no reflections). However, loss exists in real transmission lines. This is often modeled by adding resistors to the ideal model, showing the resistive loss across the conductor and the dielectric loss across the gap to the return path.

Figure 7 Circuit model of one section of lossy transmission line. The series resistance \( R_L \) models the resistive loss of the copper and the shunt conductance \( G_L \) models the dielectric loss.
2.5.1 Resistive loss comes from the inherent resistivity of copper

Copper traces are typically designed to have a consistent cross-sectional geometry down the length to keep the impedance constant and minimize reflections. This cross section defines the trace width, the separation between traces in a differential pair, the height of the dielectric material from the trace to the return plane, and the thickness of the trace itself. All of these factors impact the resistance of the copper trace. The trace width and thickness directly affect the amount of cross-sectional area in which the current has to flow. Larger area has a lower resistance, so using wider traces and thicker copper foil will reduce the resistive loss component.
Figure 9 Diagram of a cross-section of an inner differential pair. Four geometric parameters affect the resistive loss of the trace, unrelated to the material properties.

The current distribution is also affected by the nearby currents. Currents flowing in opposite ways attract each other. In a differential pair, the current flows into one trace and backwards from the other trace and the two ground planes. This means that more current will travel along the bottom of the trace near the return plane and along the inside near the complementary trace in a differential pair. In this way, the dielectric height and the separation affect how the current is distributed, how much of the available copper is used, and thus the resistive loss.

Figure 10 Current distribution in microstrip at 100 MHz.

When high speed signals travel, they want to find the path of least impedance. The signal will travel to minimize the number of field lines circling around it. Inside the conductor, there are more magnetic field lines closer to the center (more inductance in the middle of a conductor than on the edges). The impedance of high-
frequency signals is dominated by the inductance, so current will distribute to minimize the loop inductance. It will spread out as far as possible from itself and as close as possible to a reverse current, which makes the signal travel on the surface of the conductor. This is called the “skin effect”, and means that faster signals will travel in ever smaller sized areas on the exterior of the copper traces. The skin depth, \( \delta \), is dependent on the conductivity of the metal \( \sigma \), the permeability \( \mu \), and the frequency \( f \). It can be approximated by Equation 2

\[
\delta = \sqrt{\frac{1}{\sigma \pi \mu f}}
\]

\[
\delta \approx 2.1 \mu m \sqrt{\frac{1}{f \ GHz}}
\]

At 10 GHz, the skin depth is approximately 0.66 \( \mu m \) (0.026 mils). The skin effect makes the resistive loss increases with the square root of the frequency.

\[\text{Equation 2} \quad \delta = \sqrt{\frac{1}{\sigma \pi \mu f}} \]

where:
- \( \delta \) is the skin depth in microns
- \( \sigma \) is the conductivity of the metal in Siemens/m
- \( \mu \) is the permeability of the metal \( \mu_0 \mu_r \) in H/m
- \( f \) is the sine-wave frequency

2.5.2 Dielectric loss comes from the absorption of the surrounding dielectrics.

When a signal propagates down a trace, electric and magnetic fields are created that travel through the dielectric material surrounding the conductor. The electric field is perpendicular to the conductors and causes the dipoles in the material to line up with the field. The movement of these molecules is like a small current from the trace to the ground plane, causing some of the energy of the signal to be lost. When the field changes rapidly, the molecules swing back and forth and absorb more of the energy of the signal. The amount of energy lost depends on the total charge that is moving, the amount that it moves (how tightly the molecules are bonded in the polymer), and how frequently it moves. The dielectric loss is modeled as a resistor from the trace to the return plane, leaking some current out of the trace. The value of the conductance depends on the material properties, the dissipation factor and the loss tangent, but is completely independent of the geometry. The attenuation per length from the dielectric loss is:

Rice 28
\[
\alpha_{\text{die}} = \frac{20 \log e \, G_L Z_o}{2} = 10 \log e \left( \omega \, Df \, C_L \right) \left( \frac{\sqrt{Dk}}{cC_L} \right) = \frac{2\pi \times 10 \log_{10} e}{c} f \times Df \times \sqrt{Dk}
\]

at 10 GHz: \[
\alpha_{\text{die}} = 2.312 \times 10^{-9} \frac{\text{in}}{\text{s}} \times 10^{10} \text{Hz} \times Df \sqrt{Dk} = 23.12 \frac{1}{\text{in}} Df \sqrt{Dk}
\]

where:
- \(G_L\) = conductance across the dielectric = \(\omega \, Df \, C_L\)
- \(Z_o\) = characteristic impedance
- \(C_L\) = Capacitance per length
- \(\omega\) = angular frequency = \(2\pi f\)
- \(Df\) = dissipation factor
- \(Dk\) = Dielectric constant
- \(\alpha_{\text{die}}\) = attenuation per length from just the dielectric loss
- \(c\) = speed of light in a vacuum (1.18 \times 10^{10} \text{in/s})

Figure 11 Dielectric loss from the dielectric constant (square root dependence) and dissipation factor (linear dependence) at 10 GHz. In each graph, the other factor is held constant: the dissipation factor at 0.008 and the relative dielectric constant at 3.8 respectively.

### 2.6 Measuring Signal Quality

There are two basic ways to view the signal: the frequency domain and the time domain.

The frequency domain gives information about how the channel responds to various frequencies and the time domain gives information about how the channel responds to a particular data input.
Both views are useful for understanding the causes of signal integrity problems. The frequency domain is generally better at diagnosing the causes of signal integrity problems and the time domain is better suited to determining whether or not the channel is good enough.

2.6.1 Frequency Domain – S-Parameters

The frequency domain gives the response of the channel to sine waves. Since loss and reflections are both influenced by frequency, the response will change based on the frequency of the sine wave. Scattering parameters (S-parameters) describe how an input sine wave is changed by the channel. S-parameters are a collection of the scattered responses on each port at every frequency. Since any signal can be broken down into a bunch of sine waves of various frequencies, this description will completely describe the electrical behavior of any linear, passive system.

S-parameters are defined from the ports they are looking at. Each S-parameter is the ratio of the outgoing sine wave to the incoming sine wave. For example, $S_{21}$ is the ratio of the outgoing wave from port 2 to the incoming sine wave on port 1. $S_{11}$ is the sine wave coming out from port 1 to the incoming sine wave also on port 1. These ratios contain both the magnitude and the phase of the waves (or the real and imaginary parts if using complex number notation).

Every place where a signal enters or exits the device is considered a port. The port impedance is defined to be 50 Ohms. There is no standard numbering, but for this report the ports for a differential channel are numbered with odd to the left and even to the right, as in the following diagram. When this convention is used, $S_{11}$ describes the reflections from the driver back to itself, and $S_{21}$ is the transmitted wave down the trace. $S_{11}$ (and correspondingly $S_{22}$, $S_{33}$, and $S_{44}$) is called the return loss – it describes how much signal is reflected and returned to the

Rice 30
input port. \( S_{21} \) (and \( S_{34} \), etc.) is called the insertion loss, it describes how much signal is transmitted between the ports when the channel is "inserted" between them. The other parameters describe the crosstalk, \( S_{31} \) is the near-end crosstalk (NEXT), and \( S_{41} \) is the far-end crosstalk (FEXT). These port conventions can be expanded to include more ports, for instance when measuring the effects of multiple trace pairs or a large connector.

\[
\begin{align*}
\text{Figure 12 S-Parameter port numbering. For a differential channel with four ports, 1 and 3 are attached to the driver and 2 and 4 connect to the receiver. Thus } S_{21} \text{ refers to the insertion loss between ports 2 and 1 and } S_{31} \text{ is the return loss.}
\end{align*}
\]

When describing a differential pair, the standard S-parameters can be converted to mixed-mode S-parameters. These describe the signal in terms of the differential component and the common component. This is helpful when looking at differential signals since the behavior of the pair as a whole is describes, not just the individual halves. Mixed Mode S-parameters show how the differential signal and common signal respond, as well as how much of one type is converted to another (chiefly by asymmetries between the two traces). Mixed-Mode S-parameters \( (S_{mm}) \) can be obtained from the standard S-parameters \( (S_k) \) using a simple matrix conversion, given in Equation 3.

\[
S_{mm} = M^{-1} S_k M
\]

\[
M = \frac{1}{\sqrt{2}} \begin{bmatrix}
1 & 0 & -1 & 0 \\
0 & 1 & 0 & -1 \\
1 & 0 & 1 & 0 \\
0 & 1 & 0 & 1
\end{bmatrix}
\]

Equation 3
The S-parameter matrix is always square (n x n with n ports). Below are the matrices for standard and mixed-mode S-parameters, along with their interpretations. The red diagonal is the return loss for each port. The blue elements are the insertion loss. Green represents standard S-parameters’ cross-talk between the traces and mixed-mode includes the mode conversion. This thesis focuses on $S_{DD11}$ and $S_{DD21}$ (differential return and insertion loss), but all of the parameters help to give insight on the behavior of the channel.

Table 1 Matrix of standard and mixed-mode S-Parameters.
2.6.2 Time Domain—Eye Diagrams

Eye diagrams are used to view the voltage in the time domain. This shows the response of the channel to a random set of bits, not a pure sine wave, typically a worst case pseudo-random bit stream (PRBS). The voltage at the receiver is sensed over a long period of time, and then all of the bit cycles are overlaid. The height of the eye represents the voltage difference between a logic “high” and a logic “low”. There needs to be a gap between these two levels so that the receiver can accurately decode the signal. The eye diagram collapses as the loss increases as the voltage amplitude of the sine wave decreases. The width of the eye represents the amount of time during which the signal can be detected. The width can be given in picoseconds, but is more often expressed as a fraction of the unit interval (UI) to standardize for different frequencies. The width shrinks because of jitter and reflections. Also, loss lengthens the rise time of the signal which shrinks the width and collapses the eye. A sample eye diagram is pictured below. The color represents the bit error rate (BER) at that location, indicating the density of lines.

To determine if a particular channel meets the specifications, an eye mask is created. This marks a region as forbidden – no lines may enter anywhere in that region. This ensures that the bit error rate will be below a certain level (often $10^{-12}$ for PCIe and $10^{-9}$ for SAS). This gives a simple pass/fail test for a channel to tell if the signal integrity is good enough that the channel will work. The size of the mask is based on the sensitivity of the receiver. It is defined as a minimum eye height (measured within 0.1 UI of the center) and a minimum eye width (measured at the zero crossing). The eye mask that I used for this paper is displayed below.
3 Technical Approach

To determine the impact of the various design choices, a representative controller-to-controller path was created and simulated at a frequency of 10GHz. Details of the schematic creation process and simulation are given below. The goal set for the design was a total insertion loss of less than -28 dB, and an eye opening larger than the mask (height greater than 18mV and width greater than 0.3UI).

3.1 Path Design

The controller-to-controller path represents the longest (worst case) path in the system. The channel goes from the TX output across a 6-in long trace on the controller board to a connector which is plugged into the midplane. The midplane is also 6 inches long, then the line passes through another connector back across the controller to the RX pin. The total length of the channel is 18 inches and requires 2 connectors and 6 vias.
3.2 Schematic Creation

I created the schematic using Mentor Graphics Hyperlynx and SPICE models for the driver and receiver. The following is a list of each component and the type of model used in the full circuit. The full schematic is given in Appendix B for reference.

<table>
<thead>
<tr>
<th>Transmitter buffer</th>
<th>SPICE Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microstrip breakout from package</td>
<td>HyperLynx transmission line</td>
</tr>
<tr>
<td>Via</td>
<td>S-parameter Via model</td>
</tr>
<tr>
<td>Controller routing</td>
<td>HyperLynx transmission line</td>
</tr>
<tr>
<td>Via</td>
<td>S-parameter Via model</td>
</tr>
<tr>
<td>Connector</td>
<td>External Vendor S-parameter model</td>
</tr>
<tr>
<td>Via</td>
<td>S-parameter Via model</td>
</tr>
<tr>
<td>Midplane routing</td>
<td>HyperLynx transmission line</td>
</tr>
<tr>
<td>Via</td>
<td>S-parameter Via model</td>
</tr>
<tr>
<td>Connector</td>
<td>External Vendor S-parameter model</td>
</tr>
<tr>
<td>Via</td>
<td>S-parameter Via model</td>
</tr>
<tr>
<td>Controller routing</td>
<td>HyperLynx transmission line</td>
</tr>
<tr>
<td>Via</td>
<td>S-parameter Via model</td>
</tr>
<tr>
<td>AC coupling capacitor</td>
<td>Ideal 10nF capacitor</td>
</tr>
<tr>
<td>Microstrip to receiver package</td>
<td>HyperLynx transmission line</td>
</tr>
<tr>
<td>Receiver buffer</td>
<td>SPICE model</td>
</tr>
</tbody>
</table>

3.2.1 SPICE Driver Models

The driver and receiver components were modeled with a simple SPICE circuit. The driver circuit is an ideal stimulus and an RC circuit to set the rise time of the signal. The resistance had to be 50Ω in order to match the impedance of the PCB traces, and the capacitance was adjusted to create a rise time of 17ps. The receiver is simply a load resistor of 50Ω. These SPICE models are idealized versions of the actual integrated circuits and they ignore the parasitic effects of the packaging, but they provide a convenient way to compare the physical interconnects when more detailed models are unavailable.
3.2.2 PCB Trace Models

The PCB traces were modeled as transmission lines with a constant cross sectional area and material properties. All traces were differential stripline or microstip. HyperLynx has a 2-D field solver that calculates the impedance of a trace given the geometry and dielectric constant. A sample stackup was created to simulate the structure of the overall PCB. This was a simplified version of a typical multi-layer PCB. Diagrams of the stackup for the controller and midplane are also given in Appendix B. Given the stackup and the geometry of the trace, HyperLynx solves for the impedance and loss resulting from the conductors and dielectric. This way, it was possible to quickly determine the effect of changing the properties of the trace itself (for instance trace width or dielectric constant). Many different combinations were tested and the results complied in the following chapter.

3.2.3 Via Modeling

Vias are necessary to connect different layers of the PCB, but as they are complex 3 dimensional structures they are not as easy to model as transmission lines. To model the vias, HyperLynx’s 3-D field solver tool was used. This tool takes the input geometry and PCB stackup information and creates an S-parameter model that describes the behavior of the via across a broad frequency range. These behavioral models take a fairly long time to initially create, but once calculated for a specific via they can fully describe the behavior with a fast simulation time.

3.2.4 Connector Models

The connectors that go between the controller boards and the midplane were simulated with models provided by the manufacturer. Originally, several different connectors from a few vendors were considered. After comparing the different options, the Xcede-HD connector from Rice 36
Amphenol was chosen due to its loss characteristics at 10GHz. The models were provided as S-parameter files for each pin. For this work, the worst case pin was chosen to ensure the design would work, but in a practical design the high-speed lines could be routed only on the lower loss paths and the worst loss pin could have a lower speed signal on it. The large model was condensed to a single 4-port S-parameter model which was added to the HyperLynx schematic.

3.3 Simulation Approach

Simulations are highly effective in this type of work because they can provide fairly accurate results without the time and money required to build many different PCB boards and test them. First, the effects of each parameter were explored individually. Then multiple effects were considered in order to design a workable channel. As with any design, there are many tradeoffs present that can be adjusted to fit the particular needs of an implementation. In this work, the impact of the design choices is given to gain a fuller understanding of the behavior of an interconnect at higher speeds so that these choices can be made optimally.

To characterize the design, the behavior of the full channel was analyzed in both the frequency and the time domain. HyperLynx was used to solve for the S-parameters (including the total insertion and return loss). S-parameters make it easy to see the loss of the channel and visualize any resonant behavior due to reflections. The channel was also characterized in the time domain by creating an eye diagram. A pseudo-random bit stream (PRBS) was given to the driver stimulus and the voltage waveform at the receiver was sampled. The eye diagram gave clearer insight on the timing jitter, voltage degradation, and rise time of the signal, and gave an objective comparison against the eye mask that was created earlier.
3.4 Resources

3.4.1 Mentor Graphics HyperLynx

All of the simulations were completed using Mentor Graphics HyperLynx. Both the 2-D solver and the 3-D via solver were used. HyperLynx has a built-in S-parameter extractor and eye diagram wizard that were used to analyze the channel. All graphs below were created directly from HyperLynx or graphing the output data in Microsoft Excel.

3.4.2 Information Resources

An in depth knowledge of signal integrity was required for this project, which was found by reading many books and articles listed in the references. These included modeling techniques, the physics of transmission lines, material properties of PCBs, etc.

4 Results

4.1 Dielectric Material

In this investigation, I wanted to determine the impacts the dielectric constant and the dissipation factor have on the signal. I am focusing on the effects on the impedance and the loss, and then using an eye diagram to see the overall effect on performance. Because there are so many other factors that impact the impedance, the loss, and the overall performance, I aimed to hold the differential impedance from the conductor geometry constant.

I used HyperLynx to simulate designs with various materials, to gain an intuitive understanding of the impact the material has on the signal and to determine the effects on my schematic. All of the loss data, S-parameters, and eye diagrams are at a frequency of 10 GHz (for the eye diagrams this is 20 Gbps, 10 GHz base frequency). First I modeled a simple stripline.
trace segment with a transmission line and used HyperLynx’s 2-D field solver to calculate the impedance and the loss. The trace was one inch long so that all the loss values would be normalized per inch length. Then I simulated vias using HyperLynx 3-D field solver. I used a consistent geometry based on the dimensions for the Xcede connector via to show the effect from the Dk and Df. Finally, I combined these simulations to the full path schematic I have created to model a controller to controller path. Results are compared in both the frequency domain and the time domain.

4.1.1 What is a better material?

A better material (electrically speaking) has a low dielectric constant and a low loss tangent. These two factors will decrease the dielectric loss so more of the signal will arrive at the receiver. Such materials enable higher frequency signals and/or longer path lengths with the same amount of loss. Unfortunately, high performance materials also tend to be much more expensive so the options must be considered for how much loss is tolerable for the signal to still be readable with a reasonable bit error rate.

There are many choices available for materials with a range of dielectric constants and loss tangents. The dissipation factor has the biggest influence on the signal attenuation, and the loss is linearly dependent on the dissipation factor whereas it depends on the square root of the dielectric constant. Also, when choosing a dielectric constant, both the loss and the effects on the impedance must be considered. The dielectric material affects the trace impedance by changing the capacitance. Lower Dk values increase the impedance which needs to be compensated.
4.1.2 Dielectric Constant affects the impedance of the traces

First, the dielectric constant impacts the impedance because it changes the capacitance between the trace and the return plane beneath it. Higher dielectric constants will increase the capacitance which will decrease the characteristic impedance, since \( Z_0 = \frac{\sqrt{c}}{L} \). Increased impedance will directly increase the dielectric loss and cause reflections when there is a change in impedance.

![Impedance vs Dk](image)

**Figure 15** The Dielectric Constant affects the single-ended impedance of the trace as \(1/\sqrt{Dk}\)

To compensate for the increased impedance, the traces can be made wider, spaced farther apart, raised higher above the return plane, or be made with thicker copper foil. Figure 10 demonstrates widening the trace to keep the impedance at 100 Ohms. This method will reduce the resistive loss, but this is a secondary effect and is not directly related to the material used. When this method is used, the resistive loss will decrease linearly with Dk and the dielectric loss will still decrease as the square root. Alternatively, the width could be increased and the
separation decreased to maintain the impedance and keep the resistive loss constant. This second method is done in the following section on dielectric loss.

![Trace Width to keep Zo 100 Ohms](image)

**Figure 16** The trace width can be increased to compensate for a lower dielectric constant. Wider traces reduce the resistive component of the loss. If both the separation and the width are adjusted, the resistive loss can be constant.

### 4.1.3 Effects of the Material on Loss

The material directly affects the dielectric component of the loss. Lower Df and Dk materials have lower loss. To test this, the Df and Dk values for the inch-long segment were changed individually and the dielectric loss was calculated. The data shows excellent correlation to the predicted values. The dissipation factor has a strong linear relationship and the dielectric constant is related as a square root. Figure 11 shows the data and a fitted curve that matches the predicted equation.
The total amount of loss is the sum of the resistive and dielectric components. The material only directly affects the dielectric loss, the resistive loss is affected by the geometry of the trace. Below, the change in impedance from the dielectric constant is compensated by changing both the trace width and separation so as to keep the resistive component of the loss constant at 0.32 dB. Then the attenuation per inch is plotted along with the individual components. Since the resistive loss is constant, the attenuation follows the exact same trend as the dielectric loss, only shifted higher by the amount of resistive loss.

Figure 17 Simulated dielectric loss for dielectric constant and dissipation factor. The simulated data shows excellent correlation to the theoretical equation for attenuation (the fitted black line).
4.1.4 Material Choices

There are many different resins available with different characteristics. In addition, the properties also depend on the glass style used, the percentage resin, and external factors such as the humidity and temperature. A detailed study is beyond the scope of this paper, so, to get an
idea of the benefit of various systems, ten different materials were chosen with a range of \( Df \) and \( Dk \) values. The reported factors on each system’s datasheet were input to the simulator.

<table>
<thead>
<tr>
<th>Company</th>
<th>Material</th>
<th>( Dk )</th>
<th>( Df )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isola</td>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
</tr>
<tr>
<td>Isola</td>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
</tr>
<tr>
<td>Isola</td>
<td>FR408HR</td>
<td>3.65</td>
<td>0.0095</td>
</tr>
<tr>
<td>Elite (EMC)</td>
<td>EM888</td>
<td>3.8</td>
<td>0.008</td>
</tr>
<tr>
<td>Isola</td>
<td>ISpeed</td>
<td>3.63</td>
<td>0.0071</td>
</tr>
<tr>
<td>Panasonic</td>
<td>Megtron4</td>
<td>3.8</td>
<td>0.005</td>
</tr>
<tr>
<td>Elite</td>
<td>EM888K</td>
<td>3.1</td>
<td>0.007</td>
</tr>
<tr>
<td>Isola</td>
<td>ITera</td>
<td>3</td>
<td>0.0035</td>
</tr>
<tr>
<td>Panasonic</td>
<td>Megtron6</td>
<td>3.61</td>
<td>0.004</td>
</tr>
<tr>
<td>Panasonic</td>
<td>Megtron7</td>
<td>3.3</td>
<td>0.002</td>
</tr>
</tbody>
</table>

Table 2 Summary of the materials investigated. These ten materials give a range of \( Dk \) values from 3.92 to 3 and \( Df \) values from 0.025 to 0.002. Full data is given in Appendix A.

These ten materials were simulated with a one inch long trace as before. This time, to keep the impedance constant at 100 Ohms, the width was increased for the lower \( Dk \) materials to show how using a better material could also decrease the resistive loss for a best case comparison. The loss curves generated for these materials are shown in Figures 13-14 below. The data shows that MegTron7 is clearly the best material, as it has the lowest dissipation factor, rather than ITera which has the lowest dielectric constant.
Figure 19 The attenuation per inch of a stripline trace using various materials. The dielectric constant decreases dramatically for the materials with lower dissipation factors. The resistive loss decreases slightly for the materials with lower dielectric constants because of the larger widths.

Figure 20 Loss graphed against the dielectric constant and the dissipation factor. The change in dielectric loss overwhelms the slight improvement in resistive loss. The dissipation factor is more influential, the dielectric loss is very close to the linear relationship of the ideal case whereas the graph does not show a strong correlation with the dielectric constant. Fitted lines were added emphasizing the strong correlation with Df.

The results are shown in table 4 in the appendix. For this data, the dissipation factor was much more important in determining the loss of the trace. The loss graph shows a clear linear
relationship between the Df of the material and the dielectric loss. The dielectric loss dropped from 1.1 dB/in with 370HR to only 0.08 dB with MegTron7 due to the reduction in the dissipation factor from 0.025 to 0.02. Even though the dielectric constant has a square root relationship in the ideal case, for these materials the effect is difficult to see. The dissipation factor overwhelms any effect the dielectric constant has. Also, even though the resistive loss decreases because of the wider traces used with the lower Dk materials, the change is barely noticeable (only a 0.04 dB/in change). Therefore, when selecting a material to be sufficient for the performance desired, the dissipation factor should be considered first and then the dielectric constant. Another interesting characteristic to note is that the dielectric loss dominates at 10 GHz for materials with a dissipation factor greater than 0.007. For materials below 0.007, the resistive component of the loss is larger and when this level of performance is desired, thought should also be given to reducing the resistive loss as much as possible. Remember, the total attenuation is the sum of these two components, so neither can be ignored at these high speeds.

The S-parameters are influenced by the attenuation and the reflections of the signal. The insertion loss and return loss were measured also at 10 GHz for these materials and the results are graphed below against Dk and Df. S-parameters are the ratio of the outgoing sine wave to the incoming sine wave. Insertion loss is the magnitude of the sine wave at the receiver over the sine wave at the driver, a negative value on the decibel scale, whereas loss is plotted as a positive value. They both mean that the signal is lost (the amplitude of the sine wave is lower than the transmitted sine wave). The insertion loss is very close to the attenuation predicted by the theoretical equation. It is also highly correlated with the dissipation factor, and not very strongly with the dielectric constant.
Return loss is the ration of the sine wave going out from the receiver to the reflected sine wave at the receiver. Interestingly, the return loss is more correlated with the dielectric constant than with the dissipation factor. This is because the return loss primarily measures the reflections present. Reflections arise from impedance mismatches. Only the dielectric constant affects the impedance of the traces. While the differential impedance was held constant by increasing the width, no effort was made to ensure that the single ended impedance was also constant, so the small variation shows up as a slight reflection because the single ended impedances are not precisely 50 as the ports on the S-parameter model are. However, the return loss is far below typical values (less than -30 dB) so this does not have any impact on the actual performance of the signal.

![S-parameters vs Dk](image)

Rice 47
Figure 21 Effect of the dielectric constant and dissipation factor on the Insertion loss and return loss of a single trace at 10 GHz. As with the attenuation, the dissipation factor has the biggest effect on the insertion loss. The dielectric constant affects the return loss because it affects the single ended impedance of the trace slightly, which will create small increase in reflections compared to the port impedance of 50 Ohms from the S-parameter modeling.

Eye diagrams are used to view the effects in the time domain. The height of the eye represents the voltage difference between a logic “high” and a logic “low”. There needs to be a gap between these two levels so that the receiver can accurately decode the signal. The eye diagram collapses as the loss increases as the voltage amplitude of the sine wave decreases. Also, loss lengthens the rise time of the signal which shrinks the width and collapses the eye. Eye diagrams were simulated for all cases and the eye heights and widths are displayed below.
The eye diagram shows the same results as the loss and the S-parameters. The dissipation factor has the greatest effect on the signal. The dielectric constant has no significant impact on the eye diagram. The voltage levels are primarily impacted by the loss of the line, so there is a correlation between the eye height and the dissipation factor as there was for the attenuation. The eye width is also slightly smaller for the high loss materials because there is a longer rise time.

### 4.1.5 Effects of the Material on the Maximum Length of the Trace

Attenuation is the gradual loss of the signal over the length of the line. The values above gave attenuation per inch of trace at a frequency of 10 GHz. It is constant per length as long as the trace cross section and the material properties do not change. A study was done to find the maximum trace length that can be used for a given level of insertion loss.
The midplane schematic was used for this study. For each material, the length was changed from 6 inches to 24 inches and the differential insertion loss was measured. The slope of the insertion loss with length is approximately proportional to the attenuation per length from the Dk, Df, and geometry inputs. The resulting data is graphed below.

![Insertion Loss vs length](image)

Figure 23 Insertion loss over different lengths for the selected materials. Better materials enable the signal to travel a longer distance with the same amount of loss. On the graph, the results from the simulation are compared with a budgeted maximum loss value of -16 dB to determine the maximum trace length possible for each material.

As expected, the higher performance materials can travel much longer distances with the same insertion loss. Using a target maximum of -16 dB for the midplane, the following table was constructed showing the maximum length of a trace.

<table>
<thead>
<tr>
<th>Material</th>
<th>Dk</th>
<th>Df</th>
<th>Slope</th>
<th>Length (in)</th>
<th>Rank</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
<td>-1.52107</td>
<td>7.8</td>
<td>11</td>
</tr>
<tr>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
<td>-0.92788</td>
<td>12.7</td>
<td>10</td>
</tr>
<tr>
<td>FR408HR</td>
<td>3.65</td>
<td>0.0095</td>
<td>-0.78976</td>
<td>15.0</td>
<td>8</td>
</tr>
<tr>
<td>EM888</td>
<td>3.8</td>
<td>0.008</td>
<td>-0.73992</td>
<td>15.9</td>
<td>7</td>
</tr>
<tr>
<td>ISpeed</td>
<td>3.63</td>
<td>0.0071</td>
<td>-0.68457</td>
<td>17.3</td>
<td>6</td>
</tr>
</tbody>
</table>

Rice 50
<table>
<thead>
<tr>
<th>Material</th>
<th>Length</th>
<th>Width</th>
<th>Height</th>
<th>Impedance</th>
<th>Phase</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Megtron4</td>
<td>3.8</td>
<td>0.005</td>
<td>-0.60767</td>
<td>19.3</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>EM888K</td>
<td>3.1</td>
<td>0.007</td>
<td>-0.60234</td>
<td>19.4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>ITera</td>
<td>3</td>
<td>0.0035</td>
<td>-0.47812</td>
<td>21.6</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Megtron6</td>
<td>3.61</td>
<td>0.004</td>
<td>-0.55066</td>
<td>25.2*</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Megtron7</td>
<td>3.3</td>
<td>0.002</td>
<td>-0.43929</td>
<td>27.1*</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Table 3 Maximum length of a trace for a budget of -16 dB. The values were read from the graph above, and the asterisk on the last two means that the data was extrapolated with a linear trendline.

4.1.6 Effects of the Material on the Vias

The material clearly impacts the attenuation of the signal due to the dielectric loss in the traces. But how does it affect the performance of the vias that are very short compared to the traces? Vias are not usually at exactly the same impedance as the trace, and the reflections from this as well as the potential reflections from the via stub have a big impact on the final signal. In this part of the study, I experimented with the effects the different materials have on via impedance and loss.

I used HyperLynx’s 3-D modeling tool to simulate the performance of vias with the ten different materials chosen before. I kept the via dimensions the same, based on the dimensions required for the Xcede-HD connector. The drill size was 17.7 mils, the via spacing was 55.1 mils, and the antipad was rectangular 48 mils by 132 mils. There were two ground vias in line with the signal vias at a distance of 43.3 mils. The stub length was kept short by routing from the top to the lowest signal layer, for the controller the stub was 23 mils and on the midplane the stub was 32 mils long. These should be short enough to have minimal impact on the insertion loss.

As with the traces, the dielectric constant affects the impedance. One approximation for the impedance of a via is:

\[ Z = \frac{1}{j \omega \varepsilon_{r}} \]
\[ Z_o = \frac{120}{\sqrt{D_{\text{eff}}}} \ln \left( \frac{S}{D} + \sqrt{\frac{(S/D)^2}{1} - 1} \right) \]

where \( S/D \) is the spacing to drill size ratio and \( D_{\text{eff}} \) is the effective dielectric constant.

The challenge is determining a value for \( D_{\text{eff}} \). This is not simply the dielectric constant of the material, rather this factor describes the increased capacitance the via sees from the via barrel to the edges of the antipads. Therefore it is dependent on the dielectric constant in the x-y direction, the size of the antipad, the distance from the barrel to the antipad, and the amount of coupling between the two barrels (\( \alpha \) s/D).

First, the dielectric constant in PCB materials is different in the x-y direction than the z direction. This is because of the difference in \( D_k \) of the glass vs the resin. In the z direction, the fields pass through perpendicular to the glass fibers so only a short section is in the higher \( D_k \) material. But for a via, the fields pass lengthwise down the fibers so the \( D_k \) is higher. This anisotropy factor is typically around 20% higher for the x-y direction than for the z, but it depends greatly on the exact makeup of the dielectric and the resin content.

In a differential signal via, some of the return current flows through the ground vias on either side, but some also flows through the ground planes on the edge of the antipad through capacitive coupling. This slows the signal down and reduces the impedance of a via. Thus, the impedance of the via is typically lower than the impedance of the trace. Lower \( D_k \) values will reduce this capacitance and help bring the impedance of the via closer to the 100 Ohm target.
4.1.7 Controller Via Impedance

As expected, the impedance of the controller vias varies significantly on the dielectric constant, from 80 Ohms to 92 Ohms. The following TDR plot shows the impedance profile of the vias for three different materials. This TDR was generated by placing each via between two half inch long traces. This makes the full profile of the via easy to see both directions. EM888, MegTron7, and ITera are shown below to show the spread of Dk values from 3.8 to 3. The dielectric constant affects the impedance of the via; lower Dk materials create higher impedance vias. Remember that the dielectric constant determines the velocity of the signal, so the lower Dk values make the signal travel faster. This is why the via shifts slightly on the time axis.

Impedance Profile of Vias for Three Different Materials
The impedance of the via is not constant, but varies from the entry point down the barrel and then back up at the exit. The “via impedance” is somewhat arbitrary, so I chose to measure the impedance at the minimum of the curve which is half way between the two bumps for the entry and exit. I measured this value for each material using the TDR plot and plotted it below. For these materials, ITe ra is the best because the impedance is closest to 100 Ohms. The impedance is strongly related to the dielectric constant, roughly as $1/\sqrt{\text{Dk}}$, as predicted. There was no strong relationship with the dissipation factor, also as expected.
The impedance right at the entry and exit points is higher than 100 Ohms. This is because the connecting traces split apart and have to travel over the antipad rather than a ground plane. This increases the inductance and lowers the capacitance of the feeding traces, so the entry and exit impedance is always a bit higher than 100 Ohms. Entry impedance is mostly influenced by the geometry, but the dielectric constant also plays a role. Lower dielectric constants have higher entry impedance. The maximum impedance on the TDR plot for each
material is plotted below. A lower dielectric constant increases the change in impedance the signal sees as it enters and exits the via, causing a bigger reflection.

![Graph showing Via Entry Impedance vs Dk](image)

**Figure 26** Via Entry impedance increases with lower Dk. The connecting traces separate over the antipad to connect to the via pads, and this section has a higher impedance. Lower dielectric constants increase this impedance slightly. A higher entry impedance will create more reflections and worse performance.

### 4.1.8 Controller Via Insertion Loss

The insertion loss from the via also depends more on the dielectric constant than the dissipation factor. Unlike the traces, where the impedance is constant and reflections are minimized, the via impedance is not constant. Even if the main impedance of the barrel is 100 Ohms, the impedance of the connecting traces increases because the traces need to split apart to intersect the via while passing over the antipad, not a return layer. This means that the impedance of the full via is not uniform and reflections are significant. These reflections overwhelm the impact of the attenuation of the via, which is very small anyway because it is such a short length (about 70 mils long). The insertion loss does have some dependence on the dissipation factor, but the main performance factor for vias is the dielectric constant. In terms of insertion loss, ITera was the best choice because it has a low dielectric constant and low Rice 56
dissipation factor, and EM888K was close second. The very low dissipation factor materials like MegTron7 did not perform as well because of their higher dielectric constants.

![Graph showing via differential insertion loss for selected materials.](image)

**Figure 27** Via differential insertion loss for selected materials. Unlike for the traces, the dielectric constant has a much bigger effect on the insertion loss of the via. This is because the reflections caused by the via impedance are so much bigger than the signal attenuation over such a small length. Matching the impedance of a via is the best way to reduce loss, but the dissipation factor also plays a small role. For these materials, ITera has the best insertion loss because it has a low dielectric constant and low dissipation factor.
4.1.9 Comparison to the Midplane Vias

This experiment was also done for the midplane. The main differences between the two boards are the longer via length (70 mils vs 200mils) due to the thicker board (93 mils vs 233 mils) and the thicker dielectric height (5 mils to 7 mils). The results showed the same effects as the controller vias. Two interesting things to note are that the average via impedance was lower than for the controller and the entry impedance had less variation. None of the materials made the impedance very close to 100 Ohms. Because the via is more than twice as long, the dissipation factor had a stronger influence on the insertion loss than it did in the controller. Look at how MegTron7 had almost the same insertion loss as EM888K even though it had significantly lower impedance. ITera was closest at 88 Ohms and had the best insertion loss, as for the controller. A summary graph is shown below; the simulation data and copies of the above graphs for the midplane are included in the appendix for reference.
4.1.10 Combined Effects of the Material on the Full Path

Finally, I tested the impact of the material on the schematic I created. I simulated a controller to controller path with a total trace length of 18 inches and 6 vias. The detailed schematic is included in the appendix along with the stackup information for the controllers and the midplane. I simulated the full path with each of the ten selected materials, accounting for both the trace effects and the via effects. For the traces, I altered the width slightly to compensate for the dielectric constant to keep the impedance at 100 Ohms. The data is given in the appendix. It shows the overall effects and the performance benefit from using materials with better characteristics.

First, I measured the insertion loss of each section of the path and the combined insertion loss. The insertion loss effects are dominated by the attenuation in the traces, which is primarily dependent on the dissipation factor. The insertion loss is close to linear with $Df$ and shows a
slight square root dependence with Dk. However, the impedance effects of Dk on the vias seem to be less important than the dielectric loss from the traces.

One interesting note is that the slope of the insertion loss vs Df curve is steeper for the full path than the individual sections or for the single trace. The slope is essentially the attenuation from the geometry, Dk, and length. The full path is three times as long as the individual sections and the slope is three times as steep. This shows that the major impact of the material is the dissipation factor on the dielectric loss rather than the effects on the vias or the impedance.
The return loss gives an indication of the reflections and the impedance discontinuities along the path. The return loss for the full path is shown below in Figure 24. The return loss shows much less variation than the insertion loss. This indicates the material loss has a bigger effect than the reflections or the impedance. The return loss is somewhat dependent on the dielectric constant, but the correlation is not very tight as it is for the insertion loss. The lower dielectric constant improves the impedance of the via which should reduce reflections. EM888K and ITera have the closest impedance match for the vias and have low return loss. MegTron6, however, has an even lower return loss but the via impedance is not as close to 100 Ohms. There are many complicated interactions all playing at once in the full schematic. However, it is clear that while material choice has some effect on the reflections and return loss, it does not have a direct correlation and other factors should be controlled instead.
The eye diagram for the full path shows the performance in the time domain. The eye height should be a measure of the voltage loss and the width should show the reflections and rise time degradation. 370HR had no eye opening and is omitted from the Dk and Df dependency graphs in figure 25.
The eye diagram shows the margin the signal has over the mask needed by the receiver. The eye diagrams for three cases are shown below with the minimum eye mask. MegTron7 significantly increases the margin and has a really clean eye diagram, showing few reflections. The worst material with an open eye, IS415, has a much reduced amplitude and shows a lot more reflections and a huge change in rise time. EM888 is a mid-range material.
Another interesting measure to examine is the signal rise time. The rise time is defined as the time the signal takes between the levels of 20% and 80%. When a high-speed signal passes through a real path, the high-frequency components experience more loss than the low-frequency components because of the resistive and dielectric losses. The amount of rise time increase, or degradation, is another indicator of the performance of the channel and shows how much ISI (inter-symbol interference) there will be in the eye diagram. Long rise times cause the signal amplitude to be reduced in the center of the eye diagram, leading to less margin or a higher bit error rate. If the rise time is less than half the unit interval, there will be no inter-symbol interference because the signal will always have time to reach its full value before the next transition.

Rise time degradation from materials is due to the frequency dependence of the dielectric loss. Materials with a lower dissipation factor will have a lower dielectric loss, and thus a faster rise time. The rise times at the driver side and the receiver side for each material are below. The rise time at the driver is not affected much, it is driven by the source resistance and
capacitance of the driver and the reflections only impact it a small amount. However, the rise time at the receiver has a huge range, from 125 ps to 327 ps.

<table>
<thead>
<tr>
<th>Material</th>
<th>Dk</th>
<th>Df</th>
<th>Driver RT</th>
<th>Receiver RT</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
<td>19.014</td>
<td>326.821</td>
</tr>
<tr>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
<td>18.739</td>
<td>229.766</td>
</tr>
<tr>
<td>FR408HR</td>
<td>3.65</td>
<td>0.0095</td>
<td>18.894</td>
<td>169.246</td>
</tr>
<tr>
<td>EM888</td>
<td>3.8</td>
<td>0.008</td>
<td>19.096</td>
<td>208.134</td>
</tr>
<tr>
<td>ISpeed</td>
<td>3.63</td>
<td>0.0071</td>
<td>19.061</td>
<td>195.407</td>
</tr>
<tr>
<td>Megtron4</td>
<td>3.8</td>
<td>0.005</td>
<td>19.163</td>
<td>193.736</td>
</tr>
<tr>
<td>EM888K</td>
<td>3.1</td>
<td>0.007</td>
<td>18.714</td>
<td>148.155</td>
</tr>
<tr>
<td>ITera</td>
<td>3</td>
<td>0.0035</td>
<td>18.788</td>
<td>128.101</td>
</tr>
<tr>
<td>Megtron6</td>
<td>3.61</td>
<td>0.004</td>
<td>19.28</td>
<td>172.873</td>
</tr>
<tr>
<td>Megtron7</td>
<td>3.3</td>
<td>0.002</td>
<td>19.027</td>
<td>125.157</td>
</tr>
</tbody>
</table>

Table 4 Rise Time degradation from the material. The higher dissipation factor and dielectric constant cause longer rise times.

Figure 33 Rise time of the signal through the full path. It is roughly linearly dependent on the dissipation factor.

4.2 Resistive loss

The goal is to minimize the resistive loss per inch of the traces inside the PCBs. The total loss comes from two sources, resistive and dielectric. Dielectric losses are from the material used between the copper layers and the amount of loss only depends on the material’s Dk and Df. Resistive loss comes from the losses in the conductor and depends only on the geometry: the
trace width, separation between traces, dielectric height, and the thickness of the copper foil. For this study, I only looked at the resistive loss because I held the Dk and Df constant so the dielectric loss was constant.

I simulated the effects on the loss within HyperLynx. I created a 1 inch stripline trace so that all of the loss values would be per unit length of 1 in. The Dk was 3.8 and the Df was 0.008 (values of EM888), leading to a dielectric loss of 0.3461 dB/in.

Then I varied four geometric factors to try to get an understanding of their effects and relative importance in determining the resistive loss. All of the resistive loss values are taken from the graph displayed in the Edit Transmission Line dialog box at a frequency of 10 GHz.

There are five parameters that define the differential impedance of a trace. The dielectric constant is the material parameter, kept constant at 3.8 for this study since it has no direct impact on the resistive loss. The trace width and separation are free variables describing the trace dimensions that impact loss but also routing density. The copper thickness in this study is used as a free variable to gain a better understanding of its effect on resistive loss, but in real PCBs it is limited to 0.5 oz. or 1 oz. copper. The last parameter is the dielectric height. For stripline, there are actually two dielectric heights but I am assuming the case where they are symmetric, meaning the thickness of the core is the same as the thickness of the pre-preg. A diagram is given in Figure 1.

4.2.1 Effects of Geometry on Differential Impedance

The geometry of the trace defines the capacitance and inductance per length, and thus the characteristic impedance. Each variable was swept individually and the resulting single-ended and differential impedance was calculated with HyperLynx's field solver. The base case was
with a width of 4 mils, separation of 10 mils, dielectric height of 5 mils, and copper thickness of 0.675 mils (value HyperLynx uses for 0.5 oz. copper). This gave an impedance of approximately 100 Ohms.

Wider traces have less impedance primarily because the width increases the surface area of the capacitor and thus increases $C_L$ which decreases the impedance. Thicker traces also reduce the impedance because they increase the capacitance to the adjacent trace.

Increased separation increases the impedance. This is because the area of the current loop becomes larger, thus increasing the inductance and the impedance. Similarly, increased height increases the impedance for the same reason. Both of these effects show a saturation point. For saturation the impedance no longer increases after a point because all the field lines are coupled to the return plane rather than the adjacent trace. In the same way, the dielectric height saturates when the adjacent trace is closer coupled than the ground plane.

These relationships are depicted in the following graphs. Both single ended impedance and differential impedance are plotted below. In each graph, the other three factors are constant at their base values.
Figure 34 Effect of each variable on the impedance of the trace. Width and thickness decrease the impedance and height and separation increase impedance.

4.2.2 Effects on Resistive Loss – Bigger is Better

First, I wanted to get an idea of the main effect of each variable on the resistive loss. Intuitively, the resistance is based on the size of the current carrying area, so it is straightforward to expect that the trace width and the thickness have a positive effect (larger trace cross-section
has lower loss). The separation and dielectric height are a bit less intuitive, as they primarily affect the coupling of the trace and how the current is distributed within the trace. For example, tightly coupled pairs have current flowing close together in opposite directions, which will attract each other and flow more on the inside than the outside of the pair, reducing the area of the current. Loosely coupled traces will have a more even current distribution. Here, I swept each variable individually without caring about the impedance. Indeed, for all the variables bigger means less loss.
Resistive loss with Width

Resistive loss with Thickness

Resistive loss with Separation

Resistive loss with Height

Figure 35 Overall effect of increasing each variable. All have less resistive loss with larger dimensions. The separation and the dielectric height both saturate beyond 2x the trace width.

From these graphs, it seems the dielectric height and the trace width have the largest effect on the resistive loss. The separation mainly affects the amount of coupling that exists and the effect quickly saturates, though it has a big effect at very tight spacing (less than the trace width of 4 mils). The copper thickness affects the total area of the trace, but at 10 GHz the actual area of the current is determined by the skin depth not the full trace thickness, so the effects are much
smaller than for the width. However, all of these factors affect the impedance of the trace as well, so in a real situation two or more must be varied simultaneously. Do these conclusions still apply if two variables are changing?

4.2.3 Varying Two Factors to keep the Impedance Constant

I simulated many cases where I would change one variable and then use each of the other three to compensate for the impedance. The differential impedance is the important factor to keep constant at 100 Ohms and the SE impedance was allowed to vary. This will tell me if changing that variable has a positive effect on the loss even when it is compensated for by another variable, regardless of which direction the compensated variable moved.

I found that in most cases the trends were still the same as when only one factor was changed. The results are summarized in the table below. Each row represents one test variable and the columns represent which variable was used to compensate for the impedance. The direction of the arrow means if the performance was better or worse (up arrow means less resistive loss, down means more loss). The size of the arrow indicates the relative strength of each interaction. Changing the height and separation had a very subtle effect.

<table>
<thead>
<tr>
<th>Increasing:</th>
<th>Width</th>
<th>Separation</th>
<th>Height</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width</td>
<td>-</td>
<td>↑</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>Separation</td>
<td>↑</td>
<td>-</td>
<td>↔</td>
<td>↑</td>
</tr>
<tr>
<td>Height</td>
<td>↑</td>
<td>↔</td>
<td>-</td>
<td>↑</td>
</tr>
<tr>
<td>Thickness</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 5 Effect of increasing a test variable when compensated by each of the other factors. For most cases, the effect is still positive as in the single variable case. ↑ represents a strong positive correlation with increasing the test variable. ↓ represents a slight negative correlation. The size of the arrow indicates how strong the relationship is. ↔ means there is a subtle effect.

1. Width and the dielectric height
2. Separation and thickness
3. Height and Thickness
4. Width and separation

Rice 71
- Increasing the height and compensating with width (wider traces) gave much less loss.
- Increasing the separation and compensating with thickness (thicker copper) gave much less loss.
- Increasing the height and compensating with thickness (thicker copper) gave much less loss.
- Increasing the width and compensating with separation (looser traces) gave much less loss.
- Increasing the width and compensating with height (thicker dielectric) gave much less loss.
- Increasing the width and compensating with thickness (thinner copper) gave higher loss.
- Increasing the separation and compensating with width (wider traces) gave much less loss.
4.2.4 Separation to Width Ratio

I also graphed the results against the separation to width ratio. The previous results indicated that loosely coupled pairs have less loss, but this helps to show where the amount of coupling changes the resistive loss. When the separation is changed and compensated either with width or thickness, the effect saturates at about 2x. Tighter coupling will increase the loss substantially beyond this point, but moving farther beyond 2x will not significantly improve the loss.

4.2.5 Impact on the Full Schematic

Resistive loss directly leads to insertion loss. The effects get compounded with long traces. I explored how resistive loss impacts the full performance by changing the geometry of the stripline traces in each section and compared the total insertion losses. I tested four cases: tightly coupled in 0.5oz copper, loosely coupled in 0.5 oz. copper, tightly coupled in 1 oz. copper, and loosely coupled in 1 oz. copper. Since the dielectric height is determined by other
factors in the stackup (and varies between the sections) I left it as the default values of 5 mils for the controller and 7 mils for the midplane.

<table>
<thead>
<tr>
<th>Midplane</th>
<th>Case</th>
<th>Width</th>
<th>Space</th>
<th>Height</th>
<th>Thickness</th>
<th>R Loss / in</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>3.41</td>
<td>7</td>
<td>0.5 oz.</td>
<td>0.48941</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>12.3</td>
<td>7</td>
<td>0.5 oz.</td>
<td>0.30077</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>5.04</td>
<td>7</td>
<td>1 oz.</td>
<td>0.37637</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>5.38</td>
<td>15</td>
<td>7</td>
<td>1 oz.</td>
<td>0.26982</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Controller</th>
<th>Case</th>
<th>Width</th>
<th>Space</th>
<th>Height</th>
<th>Thickness</th>
<th>R Loss / in</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>4.27</td>
<td>5</td>
<td>0.5 oz.</td>
<td>0.48394</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>4.3</td>
<td>15</td>
<td>5</td>
<td>0.5 oz.</td>
<td>0.39109</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>7.18</td>
<td>5</td>
<td>1 oz.</td>
<td>0.38614</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>3.63</td>
<td>15</td>
<td>5</td>
<td>1 oz.</td>
<td>0.35907</td>
<td></td>
</tr>
</tbody>
</table>

4 Cases with Different Resistive Loss

From the above results, the best case is loosely coupled pair with thick copper (and a thick dielectric which is why the midplane loss is much lower than the controller loss). The
dielectric height had much more of an impact on the loosely coupled pairs than on the tightly coupled pairs.

The insertion loss of the entire schematic is a combination of the resistive loss of each part times its length plus the effects of the dielectric loss, reflections, etc. The insertion loss followed the expected results, the best case is case 4 with a loosely coupled pair and 1 oz. copper. The difference, even though seemingly subtle in the per inch resistive loss numbers, is quite significant. There is an improvement in the loss from case 1 to case 4 by more than 4 dB. In addition, case 2 came out slightly better than case 3. This means that using wider spacing is more important than using thicker copper, though both are quite helpful.

![Full Path Insertion Loss](image)

Figure 39 Full Path insertion loss for four cases. The best case is case 4 (loosely coupled, 1 Oz. copper) which has a 3.3 dB decrease in loss from case 1.

Increasing all of the factors reduces the loss. Increasing the width and the dielectric height is the best way to reduce the resistive loss. Gains can also be made by using loosely coupled lines and wider traces, but using wider separation and thicker dielectric does not add any benefit. Using thicker copper will provide a small benefit no matter what else is changed.

Rice 75
For a good resistive loss, I suggest using a loosely coupled differential pair (meaning the separation is at least 2x the trace width) with 1 oz. copper. For the controller with a dielectric height of 5 mils, the best might be 4 mil traces with 10 mil separation. For the midplane with height of 7 mils, the best might be 4.8 width and separation of 10.

4.3 Impedance Control

Many possible discontinuities along the path will add up, by design or as an artifact of the manufacturing process. I aimed to study the combined effects of manufacturing tolerances and impedance changes by manually changing the impedance of a particular section of the path. I did this in four steps. First I changed the impedance of a single trace, then I created a simple path with multiple transmission lines and alternated the impedance or each segment, then I changed the impedance of the controller and midplane I had created, and finally I varied the full path using combinations of different impedances for the three sections.

To change the impedance, any one of five factors (width, separation, dielectric height, copper thickness, dielectric constant) could have been adjusted. My goal is to see the effects of just the impedance change, not a change in the loss from the line, so I chose to change both the trace width and the separation to keep the resistive loss per inch constant. The material parameters Dk and Df were also kept constant so the dielectric loss is the same as well. By doing this, any change in the insertion loss comes from the additional reflections caused by the impedance change.

For this section, I am investigating the effects at one particular frequency, 10 GHz (20 Gbps). All of the results for attenuation, insertion loss, return loss, and eye diagrams were taken
at this frequency. However, since the reflections do not directly depend on frequency, these results should easily generalize to all frequencies near 10 GHz.

4.3.1 Effect of an impedance discontinuity

First, I wanted to see the basic effect of reflections. I placed a single transmission line connecting a SPICE driver and receiver pair that has source impedances of 50 Ohms (100 Ohms differential). Then I changed the impedance of the trace from 90 to 110 Ohms (keeping the attenuation constant). This models an impedance tolerance of ±10%. Reflections should reduce the amount of signal reaching the end point, so I expected there to be the best insertion loss at 100 Ohms and for the loss to increase on either side. The return loss should correspondingly be lowest at 100 Ohms and increase, showing greater reflections. The transmission line was terminated with series resistors of 50 Ohms on each trace (leading to a differential termination of 100 Ohms). The reflections in this case come from the termination no longer being matched to the impedance of the transmission lines.

The insertion loss and return loss at 10 GHz is plotted below for impedances of 90 (-10%) to 100 Ohms (+10%). The full results are given in the appendix for reference. The data shows the expected effect, a maximum in the insertion loss and a minimum in the return loss (better performance) near the center and steadily worse on the sides. However, because the return loss is low (below -20 dB) the effect on the insertion loss is very small, only decreasing by 0.03 dB.
4.3.2 Multiple Discontinuities

Each time the signal encounters a change in impedance, some of the signal reflects. Therefore, if the path has more discontinuities, there will be more reflections even if the magnitude of the discontinuity is the same. I tested the effects of many discontinuities by breaking up a path into \( n \) smaller sections and alternated the impedance of each section (i.e. 90, 110, 90, 110...). This creates \( n+1 \) discontinuities, the two ends and the boundary between sections. To change the impedance, I adjusted both the trace width and the spacing so that the impedance changed from 90 to 110 Ohms but the loss was constant. Each time, the total length was six inches and I made sure each section was a slightly different length to prevent resonances based on length from building up too much. I tested this for 1, 2, 6, and 12 segments (2, 3, 7, and 13 discontinuities). As expected, the insertion loss drops much more for more segments. Figure 3 is a graph comparing the insertion and return loss for 2 and 13 discontinuities. All of the results as well as the schematic with 13 discontinuities are in the appendix.
More discontinuities also create ripple to the insertion loss. Figure 4 is a graph of the insertion loss vs frequency for each of the four cases. When there are only two discontinuities (the terminations), the insertion loss curve is almost straight. A ripple is noticeable when there are three discontinuities, making the insertion loss dip down below the straight line. 7 or 13 discontinuities introduce a lot more ripple and lower the average insertion loss value. However, the overall slope of each line with frequency is constant because the slope is related to the attenuation from the dielectric and resistive losses, which were held constant.

Figure 5 shows the return losses. Overall, the return loss increases with more discontinuities. Here the resonances are based on the exact lengths involved, so the behavior is more complicated. However, the trend is clear that for most frequencies the path with 13 discontinuities has the highest return loss. To measure the return loss at 10 GHz, I used the value at the peak closest to 10 GHz rather than the value at precisely 10 GHz to remove some of the
effect of the different resonant points caused by the lengths of the segments. These values for 2 and 13 discontinuities are shown in Figure 3 above.

![Magnitude of Insertion Loss at 10% Impedance Tolerance](image)

Figure 4 Insertion loss curves for 10% impedance tolerance (90 and 110 Ohms) for 2 (red), 3 (purple), 7 (blue), and 13 (green) discontinuities. More segments increase the ripple in the insertion loss and increase the average loss, but the slope with frequency is constant.

Magnitude of Return Loss at 10% Impedance Tolerance

Rice 80
Then I looked at the effect of discontinuities in the time domain. Multiple discontinuities also cause the eye diagram to collapse, greatly increasing the jitter of the signal. For only two discontinuities the collapse in the eye diagram is very small, but shrinks about 20% for the path with 13 discontinuities where the eye height drops about 270 mV and the width shrinks 0.2 UI from 100 Ohms to 10% impedance tolerance. Figure 6 is a summary graph of all the cases showing the eye height for different impedance tolerance percentages. I also included three eye diagrams at 10% impedance tolerance for 0, 7, and 13 discontinuities to show the increase in the jitter and the shrinkage of the eye opening.
4.3.3 Controller Impedance Tolerance

Now that I know the effect of impedance tolerance on the performance of a simple path, I need to see what impact it has on the full schematic. First, I tested each controller and the midplane separately. For the controller, I changed the impedance of the long trace between the two vias and measured the insertion loss and return loss. I used the same via design for both, based on the Xcede dimensions (via impedance around 83 Ohms). The schematic is given in the appendix.
The trend is not the same as for a single segment. The controller has different impedance characteristics; instead of the trace seeing the terminating impedance of 100 Ohms it sees the lower impedance of the vias on either side. 90 Ohms is actually the best impedance because it minimizes the discontinuity at the ends of the trace. This makes the insertion loss gently slope down with increasing impedance, and the return loss increase correspondingly. The worst case is when the impedance is high (110 Ohms) from a thinner trace width or extra big spacing.

Fortunately, the impact on the insertion loss is still small. Going from 90 Ohms to 110 Ohms increased the insertion loss from -5.7 to -5.9 dB, only a 0.2 dB impact. All of these cases are within -6dB maximum for the controller that I had set. The return loss had a larger change, from -22 to -16.

![Controller Loss Parameters vs Zo tolerance %](image)

But what happens beyond 10% tolerance? I expanded the range of impedance tolerance to ±50% to see if the original trend would reemerge when the impedance went below 80 Ohms.
also wanted to know how much difference the percent tolerance actually made and if the effects would saturate or get steadily worse.

I found that the same trend as for a single trace is still there, only for the controller the maximum is shifted to around 80-85 Ohms. This is because the impedance should match the impedances on either side—the vias that have impedance around 83 Ohms. Below this value, the insertion loss drops off steeply again. This shows that the impedance does not have to match the 100 Ohm impedance of the top traces, just the impedance of the neighboring sections. Another interesting point is that on the negative side the fall-off had a bit steeper slope than on the positive side.
If the vias have a fixed impedance of 83 Ohms, using a target impedance of 85 or 90 Ohms instead of 100 would improve the loss. Also, when the curve is near the maximum, the impact of ±10% tolerance is smaller than the part of the curve around 100 Ohms. If the target impedance was centered at 85 Ohms, ±10% impedance tolerance has a maximum insertion loss difference of less than 0.1 dB rather than just above 0.2 dB.
The question remains what percent tolerance is good enough? I compared the insertion loss change from the maximum to the minimum within each percentage band. The Insertion loss delta increased linearly with higher tolerance values. Thus, when the amount of margin in insertion loss is known, the graph shows what percent impedance tolerance is allowable. 10% impedance tolerance gives an insertion loss delta just above 0.2 dB, and 50% gives almost 1.2 dB. I also calculated this for the return loss. The return loss is far more affected by the impedance tolerance, 10% has a range of about 8 dB and 50% is almost 18 dB. However, if the target impedance was 85 Ohms instead, 10% tolerance would only change increase the return loss by about 7 dB. The return loss delta graph shows an interesting feature, there are two regions in the curve. Low tolerance values (below 20%) show a steep linear dependence but above 20% the effects seem to flatten out. This indicates some sort of saturation in the return loss or different behavior for different ranges of reflection coefficients.

![Insertion Loss Delta for Zo Tolerance](chart1)

![Return Loss Delta for Zo Tolerance](chart2)

Figure 48 Change in the Loss for different tolerance percentages. This is the maximum loss – minimum loss for all values that percent or below. The insertion loss follows a line, increasing proportional to the tolerance percent. Return loss also increases, but has two different regions where the slope is steep below 20% and flattens out above.

Rice 86
4.3.4 Full Path Impedance Tolerance

The full schematic has three major sections: transmitting controller, midplane, and receiving controller. Thus it is important not just to consider the effect of the overall impedance tolerance of 10%, but extra cases where various combinations might create additional reflections. For example, for a simple schematic consisting of just three trace segments, the worst case is 110–90–110 or 90–110–90 because the magnitude of the impedance drop at the boundary is what creates reflections. However, the previous results indicate 85-90 Ohms is optimal, and the impedance should match the nearby via, not the other traces in the path. Below are the ten combinations of values to see if this held for the whole schematic.

<table>
<thead>
<tr>
<th>Case #</th>
<th>Controller 1 Zo</th>
<th>Midplane Zo</th>
<th>Controller 2 Zo</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>90</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>3</td>
<td>110</td>
<td>110</td>
<td>110</td>
</tr>
<tr>
<td>4</td>
<td>90</td>
<td>100</td>
<td>90</td>
</tr>
<tr>
<td>5</td>
<td>100</td>
<td>110</td>
<td>100</td>
</tr>
<tr>
<td>6</td>
<td>110</td>
<td>100</td>
<td>110</td>
</tr>
<tr>
<td>7</td>
<td>110</td>
<td>100</td>
<td>90</td>
</tr>
<tr>
<td>8</td>
<td>90</td>
<td>100</td>
<td>110</td>
</tr>
<tr>
<td>9</td>
<td>90</td>
<td>110</td>
<td>90</td>
</tr>
<tr>
<td>10</td>
<td>110</td>
<td>90</td>
<td>110</td>
</tr>
</tbody>
</table>

Table 6 Different cases of impedance tolerance investigated. Three values for each section, 90, 100, and 110 Ohms were combined in many ways to determine the worst case loss.

The insertion loss results support the idea that the impedance of the trace should match the vias on either side. The difference to another trace not directly connecting does not matter as much. The lowest insertion loss was on case 2 when all sections were at 90 Ohms, and the worst case was case 3 where all were at 110 Ohms.
Figure 49 Insertion losses for each case given in Table 1. The best case was when all sections were at 90 (case 2), and the worst was when all were at 110 (case 3). The second worst was 110—100—110 (case 6).

Below are graphs of the insertion loss against a few factors. In the ideal case, the loss should be related to the maximum discontinuity between each section. However, the sections are not centered at 100 Ohms so in fact the insertion loss really depends on the impedance of each section (lower is better). The graph of the insertion loss against the sum of the three impedances shows the best correlation.

These results confirm that the impedance should match the via impedance as close as possible. Using a trace impedance of 85 Ohms instead of 100 will reduce the reflections and improve the insertion loss somewhat. Also, in the range of 85 ±10% the insertion loss does not change as much as around 100 Ohms, so there will be a smaller ripple in the insertion loss and less conservative tolerance values may be used safely.
Figure 50 Full path insertion loss correlated with four possible causes: the controller Zo, midplane Zo, the maximum impedance discontinuity between trace sections, and the total Zo. The best correlation is with the sum of the three impedances, showing that the performance is mainly related to how well each section matches the nearby vias (90 Ohms is higher) rather than to the impedance of any other section.

4.4 Via design

Vias are used to connect traces on different layers of the PCB. They often cause signal integrity problems in high speed lines because the impedance of the trace does not match the
impedance of the via, which causes reflections. The best way to reduce these reflections is to match the impedance of the via as close to the trace as possible.

The most important factor in vias is the stub length. At high speeds, all vias must be backdrilled so that the stub is less than 20 mils. Next, the via impedance should be as close to 100 Ohms as possible. This is impacted by the drill size, center-to-center spacing, antipad size, pad size, return vias, etc. Each of these also affects the entry impedance to some degree, so a careful optimum must be found. The following sections explain the impact of a few of the key aspects in more detail.

4.4.1 Stub Length

The length of a via stub is the distance from the exit layer to the end of the via (without backdrilling this would be the bottom of the board). This length can create resonances. The primary resonant frequency is when the length is ¼ wavelength. This creates a sharp dip in the insertion loss and a corresponding peak in the return loss (meaning almost all of the signal is reflected backwards and none is transmitted). This is unacceptable in high-speed lanes.

To control the resonances, the vias in PCBs (especially thick ones like the midplane’s) have to be backdrilled. This occurs after the via has been drilled and plated, the bottom part of the via is drilled again with a slightly larger drill bit to get rid of the excess copper. The stub length has to be controlled to within a certain depth to minimize insertion loss drop. This has been defined and studied extensively elsewhere, I have included a few results here for completeness. For signals up to 12 GHz, the stub length should be kept below 20 mils. This means that backdrilling vias will be necessary for most lanes (unless the via routes from the top to the very last inner signal layer).
Figure 51 Insertion loss profile for different stub lengths. A long stub can drop the insertion loss significantly above 8 GHz.

Figure 52 Resonant frequency vs stub length. The resonant frequency is defined as the ¼ wavelength equal to the stub length.
4.4.2 Via Drill Size and Spacing

The main determiner of the via impedance is the spacing to drill size ratio (sizes must be proportional to keep impedance near 100 Ohms). The following graphs show the effects of each parameter. First, the effect of drill size with a constant spacing of 60 mils and second the effects of spacing for a constant drill size of 8 mils. The impedance is higher for smaller drill sizes, and is close to 100 between 11 and 14 mils. Wider spacing between the signal vias increases the via impedance, it is close to 100 Ohms at a spacing of 49 mils.
The loss from a via is mostly dependent on the reflections. There still are some effects from the resistive loss of the copper and the dielectric loss of the via, but since the vias are so short compared to the traces, these affects are fairly negligible. The loss comes from the reflections at the via where the impedance does not match 100. The differential insertion and return losses for each drill size at 10 GHz are plotted below. The return loss is minimized (least
reflections) where the impedance is at 100 Ohms (between 11 and 14 mils). The insertion loss does not change as much, but there is still a noticeable maximum at 11 mils.

![Graph showing Mixed-Mode IL vs spacing](image)

Figure 55 S-parameters showing the loss for each drill size above. The return loss shows a minimum where the reflections are smallest, and there is a corresponding maximum in the insertion loss. This occurs around 11 mil drill size, where the impedance of the via is closest to 100 Ohms.

### 4.4.3 Via Pad Size

The size of the via pad affects the impedance of the due to the extra capacitance around the via. Removing all the non-functional pads (pads on layers other than the top, bottom, and the exit signal layer) reduces the capacitance and increases the impedance. In addition, small pad sizes also reduce capacitance and increase the impedance. This primarily affects the impedance of the via, and only affects the entry and exit regions to a small degree.
The pad size affects the impedance of the via. Small pad sizes lead to higher impedance values because they have less capacitance.

The insertion loss decreases with smaller pad sizes. The effect is substantial with large pads (larger than 35 mils) but is less important below 30 mils. The return loss shows an optimum point at 25 mils. Large pads greatly increase the return loss.

Figure 56 Impact of the pad size on insertion and return loss. The insertion loss is only affected by extremely large pads (40 mils or bigger) and the return loss shows a minimum value at 25 mils. For a 14 mil drill size, this is a ring of 11 mils.
4.4.4 Via Antipad Size

The antipad size is a secondary factor in determining the impedance. Equation 1 lumps this effect into the effective dielectric constant, since the antipad size affects the capacitance between the via barrel and the surrounding ground planes. Larger antipads will have less capacitance and therefore a higher impedance. When the drill size or spacing cannot be adjusted, the antipad is a good way to adjust the impedance to the target value. Decreasing the capacitance also makes the signal travel faster, reducing the loss a bit and shortening the length (and therefore reducing the impact) of the via transmit section and stub length. For this experiment, with a via drill size of 14 and a spacing of 66 mils, the antipad size with the lowest loss was 70 mils diameter. Larger antipads are better at increasing the via impedance, however they also greatly increase the entry impedance because the trace travels longer without a return plane. These two have to balance to get the optimum insertion and return loss. Another method would be to “tune” the via by shrinking the antipad on the two reference layers closest to the entry and exit traces while leaving the others larger, but this method was not studied in detail for this thesis.
4.4.5 Return Vias

I also looked at the return vias. Near differential signal vias, there should be some return or stitching vias that connect the ground planes together. This provides a direct path for the return current to switch reference plane layers, although much of the current is transmitted by
capacitive coupling along the edge of the antipad. Adding these vias is important for other reasons, but I found that they have very little direct impact on the signal integrity of the signal vias unless the distance is very close (closer than the via-to-via spacing). The orientation (in line vs diagonal or 90°) and the drill size used have even less impact at these frequencies.

![Via Impedance with Return Via Distance](image)

*Figure 60 Impedance vs return via distance. The return vias have very little impact until the distance is close to the via-to-via spacing.*

![Insertion and Return loss with return via distance](image)

*Figure 61 Insertion and return loss vs return via distance. The return via distance has much less impact than other.*

Rice 98
parameters, but as long as the return vias are spaced farther than the via-to-via spacing the effects are minimal. The loss does improve marginally with farther away vias.

4.4.6 For an impedance of 100 Ohms, what gives the lowest loss?

The previous discussion assumed that only the via impedance was the important factor, and thus the spacing/drill size ratio must be established. But for the same via impedance, does the choice of drill size or spacing still affect the loss?

I simulated many different vias with four different drill sizes and swept the spacing to try to reach 100 Ohms. Larger drill sizes need larger spacing to keep the same impedance. Below is a graph of the impedance of the each via.

![Zo for various combinations of drill size and spacing](image)

**Figure 62** Via impedance for combinations of drill size and spacing. The larger drill sizes require larger spacing to reach 100 Ohms. All Drill sizes follow roughly the same trend.

Then I graphed the data against the ratio s/D. This will indicate the variation in Dkeff with the drill size. Interestingly, the Dkeff was constant for the three higher drill sizes (14, 17.7, and 20) but rose significantly for 8 mils. The three larger drill size lines are practically on top of one another, but the 8 mil line is shifted right. This indicates that for mid-range sizes the Dkeff can be said not to depend on drill size, but very small drill sizes do affect Dkeff.

Rice 99
Figure 63 Graphing the via impedance against the spacing to drill size ratio. This shows that the $\text{D}_{\text{keff}}$ is constant for the larger drill sizes but increases with smaller drill sizes.

Figure 64 TDR plots of the Vias closest to 100 Ohms.
The initial rise in the impedance is due to the uncoupling of the traces as they pass over the antipad and spread apart to intersect the via pads. Both of these effects decrease the capacitance and increase the impedance. The amount of impedance increase is dominated by how far apart the traces have to spread apart and how long they take to do it. The entry impedance thus increases with spacing, decreases with drill size, and also depends on the angle the trace enters at (typically 45°).

For these four vias, the entry impedance is lowest (closest to 100) when the drill size is 14 mils. This is the optimum point between increasing the drill size and decreasing the spacing that still leads to an impedance closest to 100 Ohms the entire length of the via.

The reflections are caused by an impedance change, so the maximum difference between two impedances is more important than the exact impedance itself. There will be a reflection as the trace uncouples, again when it hits the via, when it recouples, and finally when it hits the far side trace. All of these reflections can be reduced by minimizing the impedance swing around 100 Ohms. This is the main factor driving the loss in the vias. The loss from the via decreases when the reflections are minimized.
The return loss does depend greatly on the impedance of the via. But when the via impedance is at 100 Ohms, there is still a significant variation in the return loss for the four vias. The return loss is even tighter correlated with the impedance change, the difference between the entry impedance and the via impedance. After the barrel impedance is brought to 100 Ohms, care should be taken to reduce the entry impedance as well. The lowest return loss is at a drill size of 14 mils. This was the value that led to the lowest entry impedance.
The insertion loss does not change anywhere near as much, but smaller drill sizes have more loss than larger ones. Some of this could be that the larger drill size reduces the resistive loss (the same way that wider traces have less resistive loss).
A variable Dkeff also means that the velocity of the signal through the via varies. This means the via is electrically longer for higher Dkeff values (like for a small drill size). A longer length means more loss and more potential stub effects. The effects of a via stub are dependent on the length of the stub and the frequency. Higher Dkeff means an electrically longer stub and more of an impact on the signal.

5 Conclusion and Future Work

The goal of this work was to design a physical channel to operate at 10GHz with an acceptable amount of loss as defined by the eye mask and insertion limit of -28dB. A schematic was created and simulated and the impacts of the material, impedance tolerance, and via design were studied. Several key observations were made.

First, it was found that the material used in the dielectric of the PCB had the greatest impact on the total loss of the channel. At these high frequencies, the dielectric loss dominates.
the conductor loss. The dissipation factor of the material should be low, less than 0.009 and even smaller to have a decent margin to accommodate imperfections and impedance mismatches in the manufacturing process. The dielectric constant is also important, but less so as it primarily impacts the impedance of the trace which can be compensated for by adjusting the width of the traces slightly.

Second, the structure of the vias used in the design plays a significant role. As the signal propagates through the via, the impedance is never constant and reflections are generated. These reflections can be greatly reduced by enlarging the via spacing to drill size ratio to increase the impedance closer to that of the traces. However, four of the vias are constrained by the spacing of the connectors and thus have a fixed impedance. An improved via design was suggested that reduced the return loss greatly.

Third, the impedance of the trace is not very important, rather the important detail is matching the impedance as closely as possible along the length of the path. For this reason, using a trace impedance of 85Ω was better because it matched the impedance of the vias more tightly. An impedance tolerance of 10% centered around 85Ω was acceptable and only very small gains can be had by tightening this limit.

It has been shown that a physical channel running at 10GHz is indeed possible, though not with current third generation designs. A better material, more careful via design, and using an impedance of 85Ω will enable the faster speeds to propagate with similar loss to today’s speeds. This work sought to explore various design aspects and determine which areas were the most important in reducing loss, and which were an acceptable trade-off. All of these considerations must be balanced in a real design, along with other factors such as cost,
manufacturability, and routing density. This work enables these decisions to be made with a clearer understanding of the impact on the loss of the physical channel.

While the main goal of this thesis was achieved, there are several ways it could be improved in future. One would be to use actual models for the driver and receiver that include the packaging characteristics to enhance the robustness of this design. Another large topic that was not investigated was cross-talk from nearby channels, which will further degrade the signal quality. Finally, physical boards need to be manufactured to confirm the accuracy of these simulations and determine any effects that were not incorporated into the model.

6 References


Rice 106


7 Appendix

7.1 Loss Data For Selected Materials per inch of stripline

<table>
<thead>
<tr>
<th>Company</th>
<th>Material</th>
<th>Dk</th>
<th>Df</th>
<th>Trace width</th>
<th>SE Zo</th>
<th>Diff Zo</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isola</td>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
<td>5.53</td>
<td>52.6</td>
<td>100</td>
</tr>
<tr>
<td>Isola</td>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
<td>5.89</td>
<td>52.6</td>
<td>100</td>
</tr>
</tbody>
</table>

Rice 107
<table>
<thead>
<tr>
<th>Material</th>
<th>Company</th>
<th>Dk</th>
<th>Df</th>
<th>Resistive loss</th>
<th>Dielectric loss</th>
<th>Attenuation</th>
<th>Insertion Loss</th>
<th>Return loss</th>
<th>Eye Height</th>
<th>Eye Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>Isola</td>
<td>3.92</td>
<td>0.025</td>
<td>0.31664</td>
<td>1.0985</td>
<td>1.41514</td>
<td>-1.5228</td>
<td>-34.526</td>
<td>1.04</td>
<td>0.978</td>
</tr>
<tr>
<td>IS415</td>
<td>Isola</td>
<td>3.71</td>
<td>0.0125</td>
<td>0.30357</td>
<td>0.53434</td>
<td>0.83791</td>
<td>-0.92568</td>
<td>-39.868</td>
<td>1.08</td>
<td>0.986</td>
</tr>
<tr>
<td>FR408HR</td>
<td>Isola</td>
<td>3.65</td>
<td>0.0095</td>
<td>0.29984</td>
<td>0.4028</td>
<td>0.70264</td>
<td>-0.78716</td>
<td>-41.775</td>
<td>1.08</td>
<td>0.986</td>
</tr>
<tr>
<td>EM888</td>
<td>Elite</td>
<td>3.8</td>
<td>0.008</td>
<td>0.30918</td>
<td>0.3461</td>
<td>0.65528</td>
<td>-0.74164</td>
<td>-40.591</td>
<td>1.08</td>
<td>0.988</td>
</tr>
<tr>
<td>ISpeed</td>
<td>Isola</td>
<td>3.3</td>
<td>0.0035</td>
<td>0.29868</td>
<td>0.30021</td>
<td>0.59889</td>
<td>-0.68181</td>
<td>-42.646</td>
<td>1.08</td>
<td>0.986</td>
</tr>
<tr>
<td>Megtron4</td>
<td>Panasonic</td>
<td>3.61</td>
<td>0.004</td>
<td>0.30293</td>
<td>0.21631</td>
<td>0.51924</td>
<td>-0.60595</td>
<td>-40.114</td>
<td>1.09</td>
<td>0.987</td>
</tr>
<tr>
<td>EM888K</td>
<td>Elite</td>
<td>3.1</td>
<td>0.007</td>
<td>0.26608</td>
<td>0.27352</td>
<td>0.5396</td>
<td>-0.61327</td>
<td>-61.196</td>
<td>1.09</td>
<td>0.986</td>
</tr>
<tr>
<td>ITera</td>
<td>Isola</td>
<td>3</td>
<td>0.0035</td>
<td>0.29741</td>
<td>0.16867</td>
<td>0.46608</td>
<td>-0.54748</td>
<td>-44.394</td>
<td>1.09</td>
<td>0.988</td>
</tr>
<tr>
<td>Megtron6</td>
<td>Panasonic</td>
<td>3.3</td>
<td>0.002</td>
<td>0.27837</td>
<td>0.080631</td>
<td>0.359001</td>
<td>-0.43471</td>
<td>-52.553</td>
<td>1.1</td>
<td>0.989</td>
</tr>
</tbody>
</table>

Table 7: Simulated loss data for selected materials in a 1 in stripline. All loss numbers are taken at a frequency of 10 GHz. Graphs of this data are in Figures 13-14.

Loss Data for selected materials with the full path

Materials Selected

<table>
<thead>
<tr>
<th>Material</th>
<th>Company</th>
<th>Dk</th>
<th>Df</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>Isola</td>
<td>3.92</td>
<td>0.025</td>
</tr>
<tr>
<td>IS415</td>
<td>Isola</td>
<td>3.71</td>
<td>0.0125</td>
</tr>
<tr>
<td>FR408HR</td>
<td>Isola</td>
<td>3.65</td>
<td>0.0095</td>
</tr>
<tr>
<td>EM888</td>
<td>Elite</td>
<td>3.8</td>
<td>0.008</td>
</tr>
<tr>
<td>ISpeed</td>
<td>Isola</td>
<td>3.3</td>
<td>0.0035</td>
</tr>
<tr>
<td>Megtron4</td>
<td>Panasonic</td>
<td>3.61</td>
<td>0.004</td>
</tr>
<tr>
<td>EM888K</td>
<td>Elite</td>
<td>3.1</td>
<td>0.007</td>
</tr>
<tr>
<td>ITera</td>
<td>Isola</td>
<td>3</td>
<td>0.0035</td>
</tr>
<tr>
<td>Megtron6</td>
<td>Panasonic</td>
<td>3.3</td>
<td>0.002</td>
</tr>
</tbody>
</table>

Rice 108
Trace Dimensions to keep Impedance Constant:

<table>
<thead>
<tr>
<th></th>
<th>Controller Width</th>
<th>Controller Space</th>
<th>Controller Height</th>
<th>SE Zo</th>
<th>Diff Zo</th>
<th>Midplane Width</th>
<th>Midplane Space</th>
<th>Midplane Height</th>
<th>SE Zo</th>
<th>Diff Zo</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>3.8</td>
<td>8</td>
<td>5</td>
<td>52.2</td>
<td>100</td>
<td>5.53</td>
<td>10</td>
<td>7</td>
<td>52.6</td>
<td>100</td>
</tr>
<tr>
<td>IS415</td>
<td>4.06</td>
<td>8</td>
<td>5</td>
<td>52.2</td>
<td>100</td>
<td>5.89</td>
<td>10</td>
<td>7</td>
<td>52.6</td>
<td>100</td>
</tr>
<tr>
<td>FR408HR</td>
<td>4.14</td>
<td>8</td>
<td>5</td>
<td>52.1</td>
<td>100</td>
<td>6</td>
<td>10</td>
<td>7</td>
<td>52.5</td>
<td>100</td>
</tr>
<tr>
<td>EM888</td>
<td>3.95</td>
<td>8</td>
<td>5</td>
<td>52.2</td>
<td>100</td>
<td>5.73</td>
<td>10</td>
<td>7</td>
<td>52.6</td>
<td>100</td>
</tr>
<tr>
<td>ISpeed</td>
<td>4.16</td>
<td>8</td>
<td>5</td>
<td>52.2</td>
<td>100</td>
<td>6.03</td>
<td>10</td>
<td>7</td>
<td>52.6</td>
<td>100</td>
</tr>
<tr>
<td>Megtron4</td>
<td>3.95</td>
<td>8</td>
<td>5</td>
<td>52.2</td>
<td>100</td>
<td>5.73</td>
<td>10</td>
<td>7</td>
<td>52.6</td>
<td>100</td>
</tr>
<tr>
<td>EM888K</td>
<td>4.96</td>
<td>8</td>
<td>5</td>
<td>52</td>
<td>100</td>
<td>7.15</td>
<td>10</td>
<td>7</td>
<td>52.3</td>
<td>100</td>
</tr>
<tr>
<td>iTera</td>
<td>5.13</td>
<td>8</td>
<td>5</td>
<td>52</td>
<td>100</td>
<td>7.39</td>
<td>10</td>
<td>7</td>
<td>52.3</td>
<td>100</td>
</tr>
<tr>
<td>Megtron6</td>
<td>4.19</td>
<td>8</td>
<td>5</td>
<td>52.1</td>
<td>100</td>
<td>6.07</td>
<td>10</td>
<td>7</td>
<td>52.5</td>
<td>100</td>
</tr>
<tr>
<td>Megtron7</td>
<td>4.63</td>
<td>8</td>
<td>5</td>
<td>52.1</td>
<td>100</td>
<td>6.69</td>
<td>10</td>
<td>7</td>
<td>52.4</td>
<td>100</td>
</tr>
</tbody>
</table>

Table 8 Trace width and spacing to keep the impedance constant at 100 Ohms.

S-parameter and Eye Diagram Results

<table>
<thead>
<tr>
<th>Material</th>
<th>Controller 1 IL</th>
<th>Midplane IL</th>
<th>Controller 2 IL</th>
<th>Full IL</th>
<th>Full RL</th>
<th>Eye Height</th>
<th>Eye Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>-10.523</td>
<td>-13.473</td>
<td>-10.4</td>
<td>-33.943</td>
<td>-15.722</td>
<td>0.0002</td>
<td>0.003</td>
</tr>
<tr>
<td>IS415</td>
<td>-6.9067</td>
<td>-9.5379</td>
<td>-6.765</td>
<td>-22.937</td>
<td>-16.016</td>
<td>0.101</td>
<td>0.549</td>
</tr>
<tr>
<td>FR408HR</td>
<td>-6.1694</td>
<td>-8.7626</td>
<td>-6.0124</td>
<td>-20.626</td>
<td>-17.473</td>
<td>0.154</td>
<td>0.596</td>
</tr>
<tr>
<td>EM888</td>
<td>-5.7657</td>
<td>-8.3268</td>
<td>-5.8652</td>
<td>-19.56</td>
<td>-15.643</td>
<td>0.159</td>
<td>0.585</td>
</tr>
<tr>
<td>ISpeed</td>
<td>-5.4483</td>
<td>-8.1088</td>
<td>-5.3081</td>
<td>-18.532</td>
<td>-18.255</td>
<td>0.192</td>
<td>0.625</td>
</tr>
<tr>
<td>Megtron4</td>
<td>-4.9704</td>
<td>-7.5527</td>
<td>-5.1467</td>
<td>-17.215</td>
<td>-15.645</td>
<td>0.192</td>
<td>0.581</td>
</tr>
<tr>
<td>EM888K</td>
<td>-4.7843</td>
<td>-7.6457</td>
<td>-4.8063</td>
<td>-17.084</td>
<td>-20.348</td>
<td>0.228</td>
<td>0.664</td>
</tr>
<tr>
<td>iTera</td>
<td>-3.8576</td>
<td>-6.5011</td>
<td>-3.9255</td>
<td>-14.254</td>
<td>-19.687</td>
<td>0.292</td>
<td>0.664</td>
</tr>
<tr>
<td>Megtron6</td>
<td>-4.0923</td>
<td>-7.2611</td>
<td>-3.9173</td>
<td>-14.898</td>
<td>-21.346</td>
<td>0.247</td>
<td>0.619</td>
</tr>
<tr>
<td>Megtron7</td>
<td>-3.2986</td>
<td>-6.4431</td>
<td>-3.2725</td>
<td>-12.872</td>
<td>-17.02</td>
<td>0.345</td>
<td>0.687</td>
</tr>
</tbody>
</table>

Table 9 Full path insertion loss, return loss, and eye opening data.

Via Simulation Results

<table>
<thead>
<tr>
<th>Material</th>
<th>Dk</th>
<th>Df</th>
<th>Via Impedance</th>
<th>Entry Impedance</th>
<th>Insertion loss</th>
<th>Return loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
<td>87.841</td>
<td>102.93</td>
<td>-3.0219</td>
<td>-18.292</td>
</tr>
<tr>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
<td>89.934</td>
<td>104.47</td>
<td>-2.9097</td>
<td>-18.172</td>
</tr>
<tr>
<td>FR408HR</td>
<td>3.65</td>
<td>0.0095</td>
<td>91.17</td>
<td>105.98</td>
<td>-2.9114</td>
<td>-17.893</td>
</tr>
<tr>
<td>EM888</td>
<td>3.8</td>
<td>0.008</td>
<td>88.42</td>
<td>104.26</td>
<td>-2.9302</td>
<td>-18.932</td>
</tr>
<tr>
<td>ISpeed</td>
<td>3.63</td>
<td>0.0071</td>
<td>90.772</td>
<td>105.09</td>
<td>-2.8655</td>
<td>-17.855</td>
</tr>
<tr>
<td>Megtron4</td>
<td>3.8</td>
<td>0.005</td>
<td>88.189</td>
<td>104.39</td>
<td>-2.9232</td>
<td>-19.067</td>
</tr>
<tr>
<td>EM888K</td>
<td>3.1</td>
<td>0.007</td>
<td>99.945</td>
<td>108.73</td>
<td>-2.7346</td>
<td>-14.852</td>
</tr>
</tbody>
</table>

Rice 109
<table>
<thead>
<tr>
<th>Material</th>
<th>Dk</th>
<th>Df</th>
<th>Via Impedance</th>
<th>Entry Impedance</th>
<th>Insertion loss</th>
<th>Return loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
<td>77.019</td>
<td>103.4</td>
<td>-4.4294</td>
<td>-13.977</td>
</tr>
<tr>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
<td>78.832</td>
<td>104.95</td>
<td>-4.2083</td>
<td>-13.569</td>
</tr>
<tr>
<td>FR408HR</td>
<td>3.65</td>
<td>0.0095</td>
<td>79.426</td>
<td>105.38</td>
<td>-4.1551</td>
<td>-13.46</td>
</tr>
<tr>
<td>EM888</td>
<td>3.8</td>
<td>0.008</td>
<td>77.717</td>
<td>105.31</td>
<td>-4.1857</td>
<td>-13.669</td>
</tr>
<tr>
<td>ISpeed</td>
<td>3.63</td>
<td>0.0071</td>
<td>79.575</td>
<td>105.64</td>
<td>-4.122</td>
<td>-13.421</td>
</tr>
<tr>
<td>Megtron4</td>
<td>3.8</td>
<td>0.005</td>
<td>77.617</td>
<td>105.55</td>
<td>-4.1636</td>
<td>-13.683</td>
</tr>
<tr>
<td>EM888K</td>
<td>3.1</td>
<td>0.007</td>
<td>86.862</td>
<td>106.54</td>
<td>-3.9747</td>
<td>-12.753</td>
</tr>
<tr>
<td>ITera</td>
<td>3</td>
<td>0.0035</td>
<td>88.187</td>
<td>106.95</td>
<td>-3.9109</td>
<td>-12.612</td>
</tr>
<tr>
<td>Megtron6</td>
<td>3.61</td>
<td>0.004</td>
<td>79.706</td>
<td>105.98</td>
<td>-4.1804</td>
<td>-13.38</td>
</tr>
<tr>
<td>Megtron7</td>
<td>3.3</td>
<td>0.002</td>
<td>83.857</td>
<td>106.58</td>
<td>-3.9708</td>
<td>-13.014</td>
</tr>
</tbody>
</table>

Table 10 Controller Via impedance and Insertion loss

<table>
<thead>
<tr>
<th>Material</th>
<th>Dk</th>
<th>Df</th>
<th>Via Impedance</th>
<th>Entry Impedance</th>
<th>Insertion loss</th>
<th>Return loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>370HR</td>
<td>3.92</td>
<td>0.025</td>
<td>77.019</td>
<td>103.4</td>
<td>-4.4294</td>
<td>-13.977</td>
</tr>
<tr>
<td>IS415</td>
<td>3.71</td>
<td>0.0125</td>
<td>78.832</td>
<td>104.95</td>
<td>-4.2083</td>
<td>-13.569</td>
</tr>
<tr>
<td>FR408HR</td>
<td>3.65</td>
<td>0.0095</td>
<td>79.426</td>
<td>105.38</td>
<td>-4.1551</td>
<td>-13.46</td>
</tr>
<tr>
<td>EM888</td>
<td>3.8</td>
<td>0.008</td>
<td>77.717</td>
<td>105.31</td>
<td>-4.1857</td>
<td>-13.669</td>
</tr>
<tr>
<td>ISpeed</td>
<td>3.63</td>
<td>0.0071</td>
<td>79.575</td>
<td>105.64</td>
<td>-4.122</td>
<td>-13.421</td>
</tr>
<tr>
<td>Megtron4</td>
<td>3.8</td>
<td>0.005</td>
<td>77.617</td>
<td>105.55</td>
<td>-4.1636</td>
<td>-13.683</td>
</tr>
<tr>
<td>EM888K</td>
<td>3.1</td>
<td>0.007</td>
<td>86.862</td>
<td>106.54</td>
<td>-3.9747</td>
<td>-12.753</td>
</tr>
<tr>
<td>ITera</td>
<td>3</td>
<td>0.0035</td>
<td>88.187</td>
<td>106.95</td>
<td>-3.9109</td>
<td>-12.612</td>
</tr>
<tr>
<td>Megtron6</td>
<td>3.61</td>
<td>0.004</td>
<td>79.706</td>
<td>105.98</td>
<td>-4.1804</td>
<td>-13.38</td>
</tr>
<tr>
<td>Megtron7</td>
<td>3.3</td>
<td>0.002</td>
<td>83.857</td>
<td>106.58</td>
<td>-3.9708</td>
<td>-13.014</td>
</tr>
</tbody>
</table>

Table 11 Midplane Via impedance and insertion loss
Figure 66 Graphs of the midplane impedance, insertion loss, and return loss.

Table 12 Data from changing two variables in sets to keep the differential impedance at 100 Ohms.

<table>
<thead>
<tr>
<th>Changing Width And Separation</th>
<th>Trace width</th>
<th>Separation</th>
<th>Dielectric Height</th>
<th>Cu thickness</th>
<th>SE Zo</th>
<th>Diff Zo</th>
<th>Resistive loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.35</td>
<td>2.5</td>
<td>5</td>
<td>0.675</td>
<td>71.5</td>
<td>100</td>
<td>0.69816</td>
<td></td>
</tr>
<tr>
<td>1.79</td>
<td>3</td>
<td>5</td>
<td>0.675</td>
<td>66.5</td>
<td>100.1</td>
<td>0.59804</td>
<td></td>
</tr>
<tr>
<td>2.47</td>
<td>4</td>
<td>5</td>
<td>0.675</td>
<td>60.4</td>
<td>100</td>
<td>0.4961</td>
<td></td>
</tr>
<tr>
<td>2.94</td>
<td>5</td>
<td>5</td>
<td>0.675</td>
<td>56.9</td>
<td>100</td>
<td>0.44367</td>
<td></td>
</tr>
<tr>
<td>3.26</td>
<td>6</td>
<td>5</td>
<td>0.675</td>
<td>54.8</td>
<td>100</td>
<td>0.4173</td>
<td></td>
</tr>
<tr>
<td>3.65</td>
<td>8</td>
<td>5</td>
<td>0.675</td>
<td>52.5</td>
<td>100</td>
<td>0.39228</td>
<td></td>
</tr>
<tr>
<td>3.86</td>
<td>10</td>
<td>5</td>
<td>0.675</td>
<td>51.3</td>
<td>100</td>
<td>0.38221</td>
<td></td>
</tr>
<tr>
<td>4.09</td>
<td>20</td>
<td>5</td>
<td>0.675</td>
<td>50.1</td>
<td>100</td>
<td>0.37512</td>
<td></td>
</tr>
</tbody>
</table>

Rice 111
<table>
<thead>
<tr>
<th>Changing Width and Height</th>
<th>1.19</th>
<th>10</th>
<th>2</th>
<th>0.675</th>
<th>50</th>
<th>100</th>
<th>0.83584</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2.06</td>
<td>10</td>
<td>3</td>
<td>0.675</td>
<td>50.3</td>
<td>100.1</td>
<td>0.58826</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>10</td>
<td>4</td>
<td>0.675</td>
<td>50.7</td>
<td>100</td>
<td>0.45875</td>
</tr>
<tr>
<td></td>
<td>3.86</td>
<td>10</td>
<td>5</td>
<td>0.675</td>
<td>51.3</td>
<td>100</td>
<td>0.38221</td>
</tr>
<tr>
<td></td>
<td>4.66</td>
<td>10</td>
<td>6</td>
<td>0.675</td>
<td>52</td>
<td>100</td>
<td>0.33206</td>
</tr>
<tr>
<td></td>
<td>5.4</td>
<td>10</td>
<td>7</td>
<td>0.675</td>
<td>52.9</td>
<td>100</td>
<td>0.29711</td>
</tr>
<tr>
<td></td>
<td>6.09</td>
<td>10</td>
<td>8</td>
<td>0.675</td>
<td>53.7</td>
<td>100</td>
<td>0.27155</td>
</tr>
<tr>
<td></td>
<td>6.72</td>
<td>10</td>
<td>9</td>
<td>0.675</td>
<td>54.5</td>
<td>100</td>
<td>0.25234</td>
</tr>
<tr>
<td></td>
<td>7.31</td>
<td>10</td>
<td>10</td>
<td>0.675</td>
<td>55.4</td>
<td>100</td>
<td>0.23737</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changing width and Copper Thickness</th>
<th>4.35</th>
<th>10</th>
<th>5</th>
<th>0.5</th>
<th>51.1</th>
<th>100</th>
<th>0.41425</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4.22</td>
<td>10</td>
<td>5</td>
<td>0.6</td>
<td>51.1</td>
<td>100</td>
<td>0.40374</td>
</tr>
<tr>
<td></td>
<td>4.1</td>
<td>10</td>
<td>5</td>
<td>0.7</td>
<td>51.2</td>
<td>100</td>
<td>0.39539</td>
</tr>
<tr>
<td></td>
<td>3.76</td>
<td>10</td>
<td>5</td>
<td>1</td>
<td>51.4</td>
<td>100</td>
<td>0.37792</td>
</tr>
<tr>
<td></td>
<td>3.44</td>
<td>10</td>
<td>5</td>
<td>1.3</td>
<td>51.7</td>
<td>100.1</td>
<td>0.36832</td>
</tr>
<tr>
<td></td>
<td>3.25</td>
<td>10</td>
<td>5</td>
<td>1.5</td>
<td>51.8</td>
<td>100</td>
<td>0.36141</td>
</tr>
<tr>
<td></td>
<td>3.15</td>
<td>10</td>
<td>5</td>
<td>1.6</td>
<td>51.9</td>
<td>100</td>
<td>0.35879</td>
</tr>
<tr>
<td></td>
<td>2.78</td>
<td>10</td>
<td>5</td>
<td>2</td>
<td>52.3</td>
<td>100</td>
<td>0.35083</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changing Separation and Dielectric Height</th>
<th>4</th>
<th>17.751</th>
<th>4.67</th>
<th>0.675</th>
<th>50.1</th>
<th>100</th>
<th>0.41417</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4</td>
<td>8.461</td>
<td>5</td>
<td>0.675</td>
<td>51.9</td>
<td>100</td>
<td>0.40376</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>5.534</td>
<td>6</td>
<td>0.675</td>
<td>56.7</td>
<td>100</td>
<td>0.39723</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>4.704</td>
<td>7</td>
<td>0.675</td>
<td>60.8</td>
<td>100</td>
<td>0.39891</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>4.3</td>
<td>8</td>
<td>0.675</td>
<td>64.4</td>
<td>100</td>
<td>0.40191</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>4.064</td>
<td>9</td>
<td>0.675</td>
<td>67.6</td>
<td>100</td>
<td>0.40514</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>3.912</td>
<td>10</td>
<td>0.675</td>
<td>70.5</td>
<td>100</td>
<td>0.40771</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changing Dielectric Height and Copper Thickness</th>
<th>4</th>
<th>10</th>
<th>4</th>
<th>0.1</th>
<th>50.3</th>
<th>99.9</th>
<th>0.65202</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>5</td>
<td>0.79</td>
<td>51.2</td>
<td>99.9</td>
<td>0.3891</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>6</td>
<td>1.48</td>
<td>52.6</td>
<td>100</td>
<td>0.31581</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>7</td>
<td>2.06</td>
<td>54.3</td>
<td>100</td>
<td>0.27837</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>8</td>
<td>2.53</td>
<td>56</td>
<td>100</td>
<td>0.248</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>9</td>
<td>2.91</td>
<td>57.7</td>
<td>100</td>
<td>0.23131</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>10</td>
<td>3.21</td>
<td>59.5</td>
<td>100</td>
<td>0.21895</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changing Separation and Copper Thickness</th>
<th>4</th>
<th>3.53</th>
<th>5</th>
<th>0.004</th>
<th>57.1</th>
<th>100</th>
<th>0.91713</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>0.107</td>
<td>56.3</td>
<td>100</td>
<td>0.65333</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>0.261</td>
<td>54.8</td>
<td>100</td>
<td>0.50962</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>6</td>
<td>5</td>
<td>0.406</td>
<td>53.7</td>
<td>100</td>
<td>0.4592</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>8</td>
<td>5</td>
<td>0.64</td>
<td>52.1</td>
<td>99.9</td>
<td>0.40932</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>10</td>
<td>5</td>
<td>0.786</td>
<td>51.2</td>
<td>100</td>
<td>0.38945</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>20</td>
<td>5</td>
<td>1.005</td>
<td>50.1</td>
<td>100</td>
<td>0.37034</td>
</tr>
</tbody>
</table>

Rice 112
DISCLAIMER NOTICE

MISSING PAGE(S)

p.113
8 Appendix B – Schematic Diagrams

Transmitting Controller

Driver Cap Microstrip to BGA Via Stripline across Controller Via To Connector

Midplane

Receiving Controller

To Connector Via Stripline across Controller Via Microstrip to Cap AC Coupling Capacitor Microstrip to BGA Receiver

Figure 67 Schematic used for the full path simulation, Controller to controller across the midplane, full path trace length is 18 in. The path is broken into three sections; the transmitting controller, the midplane, and the receiving controller. The two controllers have the same stackup and trace dimensions (but the receiving one includes an AC coupling capacitor, and the midplane has a thicker stackup and wider traces.)
Figure 68 Stackup for the controller and the midplane. The controller is 93.55 mils thick with 16 layers and dielectric heights of 5 mils. The midplane is 233.7 mils thick with 28 layers and a dielectric height of 7 mils.