VLSI Microdisplay Technology

by

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and Computer Science in Partial Fulfillment
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Abstract

This thesis describes a new technology for making tiny displays using liquid crystal on
silicon. VLSI microdisplays are very high resolution 1cm² displays made of conventionally
fabricated silicon CMOS circuits laminated with liquid crystal material. A silicon layout
compiler has been implemented to enable rapid development and testing of prototype
microdisplay devices. Automated VLSI layout tools have been designed to address
several problems specific to the manufacture and use of very small displays including:
compensation for the distortion and chromatic aberration of simple optical systems, the
incorporation of display decoding and driving circuitry in an integrated display/driver chip,
and anti-aliasing to compensate for limited pixel resolution. These existing VLSI design
tools can also be made to incorporate high performance digital structures into the active
substrate so that conventional or massively parallel bit-per-pixel computers can be
fabricated as part of the display. This level of display-to-processor integration combined
with optical system compensation may ultimately solve several imminent I/O bandwidth
bottlenecks for ultrahigh resolution information display. Potential device resolutions
exceeding that of the human visual system in microdisplay packages that are 1cm² will
drive a new generation of portable devices ranging from pocket pagers with full page
displays, to eyeglass-mounted virtual reality displays. This thesis documents the design,
development, and testing of several prototype VLSI microdisplays which clearly
demonstrate the promise of this new technology.

Thesis Supervisor: Dr. Thomas F. Knight, Jr.
Title: Principal Research Scientist
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To my father, Phillip Edward Alvelda,
for somehow knowing I would end up at M.I.T.
when I was two years old (He has a picture to prove it.),

to my mother, Elsa H. J. O'Donnell,
who had me peering through a microscope before I was four,

to my advisor, Thomas F. Knight Jr.,
who always had a reference, or a lens, or a blowtorch
when I needed one,

and to my students at the South Pasadena High School,
who taught me what learning was all about.
1. Introduction

Current display technology is dominated by the cathode ray tube [CRT] and the liquid crystal display [LCD]. The liquid crystal display has advantages in power, size, and safety, while the CRT is well understood and quite inexpensive to manufacture. Major investments in liquid crystal display technology have led to the development of large, high resolution displays, first using addressable matrix scanning, and more recently using active matrix techniques. The introduction of active matrix techniques into liquid crystal displays produces high quality images, but requires very large capital investments in new manufacturing and device technology. Circuit lithography masks and processing equipment of the same size as the panel being produced are required. Without a crystalline substrate, active matrix displays are built using either amorphous or polycrystalline thin film transistors, which typically exhibit poor electrical characteristics and low yield. Time-to-market and per-unit-costs are increased because of the independent learning curve associated with these new technologies.

The combination of conventional silicon fabrication with liquid crystal display technology offers an interesting alternative for many applications. By using off-the-shelf silicon fabrication technology to produce a high-resolution active matrix display driver back-plane, one can fabricate physically small liquid crystal microdisplays which nonetheless offer exceptional resolution. For example, a CMOS microdisplay with five micron square pixels and a one square centimeter active area will have a resolution of 2,000 by 2,000 pixels (4 megapixels). Because the manufacturing technology used is completely standard, such die can be made in any silicon foundry, require no infrastructure investment, and follow the well established silicon learning curve for process and yield improvement.

The sole disadvantage for normal display applications of these microdisplays is their small physical size. Conventional displays are designed for direct viewing applications, where there is no optical component between the display surface and the eye. Because the microdisplay is so small, direct viewing is ineffective, and optical techniques must be used to assist the viewer. Compensating for this seeming disadvantage, however, are the large number of potential application areas where small physical size and low power consumption are decided advantages. Devices such as pocket pagers, wrist watches, calculators, ultra-portable wrist-top or pen computers, eyeglass-mounted virtual or augmented reality displays, gunsights, and personal navigators will greatly benefit from the development of microdisplay technology.

This thesis describes the development of novel microdisplay technology based on conventionally fabricated silicon CMOS circuits as an active substrate for a liquid crystal
lamine (see Figure 1.0). The use of silicon substrates prevents the construction of large, directly visible displays, but leverages the existing VLSI design and manufacturing infrastructure, allowing the fabrication of high resolution, low cost displays. The small physical size of the resulting structures precludes their use in many direct view applications, but the growth in personal digital devices makes the technology of microdisplays very attractive from a cost and convenience standpoint in many important applications.

![Diagram of microdisplay components](image)

**Figure 1.0** is a schematic representation of the major components of a VLSI microdisplay with liquid crystal material sandwiched between a specially prepared glass cover and an active-matrix backplane fabricated in a standard CMOS technology.

Additionally, applying silicon compiler technology to microdisplay design enables rapid implementation and testing of prototype devices. These automated design layout techniques have been implemented to

- Compensate for the distortion of optical systems.
- Compensate for chromatic aberration in simple optics.
- Decrease aliasing due to limited pixel resolution.
- Include display driving circuitry in an integrated display/driver chip

These existing VLSI design tools can also be made to incorporate high performance digital structures into the active substrate to allow conventional or massively parallel bit-per-pixel computers to be fabricated as part of the display.

Micron-scale display technology could immediately replace current LCDs in ultra-portable systems with little change in form factor other than a general reduction in size and power consumption. Even with the reduction in size, display resolution based on VLSI lithography will actually increase. Replacing current high-resolution LCDs and their
associated electronics with a single standard-process CMOS chip would have direct
savings in power, mass, and reliability. The fabrication cost of a single-chip device is
currently around five dollars per device in quantity, and is expected to drop as technology
advances. This low production cost could make personal information devices almost
disposable.

Current lithographic technology allows the practical fabrication of pixels on the order of
five microns in width or greater. This immediately promises a display resolution of
approximately 2000 x 2000 pixels on a one centimeter die. This figure is also sufficiently
above optical (diffraction limited) resolution limits to allow a further increase in resolution
by a factor of two (by scaling lambda design rules as line widths decrease), until larger
chips must be used to resolve more pixels.

As VLSI fabrication technology advances beyond optical resolution limits and chip
fabrication processes enable more complex layouts and architectures, more chip area could
be applied to pixel or data-processing circuitry. Ever more complex processors for image
enhancement, display, or more conventional computing tasks could be incorporated in the
same display chip without incurring any other fabrication or implementation overhead.
This immediately solves an imminent problem associated with increasing display
resolution. The performance limit in many of today's computer systems is the
communication bandwidth bottleneck in transferring so much data from a processor to
displays with more than a million pixels. When the display is one mask layer above the
processor on a CMOS chip, the I/O bottleneck vanishes.

In summary, this new portable display technology promises significant savings in mass,
significant reduction in power dissipation, increased display resolution and anti-aliasing
technology, compensation for the distortion and aberration of simple optical systems, and
the capability to incorporate processing technology directly into the display circuitry. The
entire approach for the proposed microdisplay technology leverages the already existing
$100 billion per year interest in silicon processing technology to allow almost immediate
implementation of new devices with greater reliability and very low development and
production cost. The added promise of follow-on technologies such as
electronically-tunable lenses and real-time holographic systems makes investment in this
direction even more attractive.

The microdisplay development effort to-date has covered a rather wide area at the union
of CMOS VLSI design and nonlinear optical materials. This thesis will document the
results of microdisplay research including:

- The initial analysis and simulation of liquid crystal devices
- The VLSI design of the CMOS backplanes used to drive the optical materials
- The electro-optic materials experiments for tiny reflected-mode active-matrix cells
- The surface-interface experiments to couple the CMOS chips with the LC materials
- Interface design
- The testing and evaluation of four prototype microdisplay devices.
I will begin with a brief background in liquid crystal physics and a description of some basic liquid crystal devices and their simulation. This introduction will be followed by a chapter on the VLSI design of the CMOS microdisplay backplanes followed by chapter on the particular display materials and modes used in the devices. Next will come a chapter on the particulars of the actual device assembly, testing and evaluation. The thesis will conclude with future research plans and applications of the technology documented here.
2. Liquid Crystal Background

Introduction

There are many materials which exhibit phase transitions significantly more complex than the typical three phase system of solid-to-liquid-to-gas. In fact, there is an area of considerable interest at the transition between the solid and liquid phases wherein certain materials exhibit properties of both solids and liquids at the same time. This in between area, or mesophase, is commonly called a liquid crystalline phase, to describe materials which to some degree, can flow and diffuse as liquids, while maintaining some orientational order common to crystals. The characteristics described in the following section will provide a background in the mechanical, electronic, and optical properties of liquid crystals, each of which are essential to their application as an optical modulator for display purposes.

Mechanical Properties

When liquid crystal materials are heated to above the "clearing point," they are thermally agitated enough to lose all positional and orientational order. Because there is no preferred direction either translationally, or orientationally in this liquid phase, it is commonly described as the isotropic phase. As the material is cooled, before it reaches the crystallization point, the material begins to accrue an orientational order as the liquid crystal molecules are packed closer and closer together. They tend to align in some preferred direction called the director. But while they tend to align in similar directions, the alignment is not perfect, they are still thermally

Figure 2.0 depicts characteristic patterns of a liquid crystal material as it is cooled from an isotropic liquid state through several meso-phase transitions until it becomes a crystalline solid. Here, the director is oriented upward.
excited, and can diffuse in any direction just as they did in their liquid phase, albeit with a slightly higher viscosity. This behavior is described as a nematic mesophase, where nematic comes from the Greek word for string; when materials in a nematic phase are viewed under a microscope, they reveal a string-like pattern of defects. When cooled further, some liquid crystal materials can begin to accumulate even more ordered layers which are not quite crystallized wherein the nematic materials begin to separate into layers. It is still possible for these more layered nematics to easily diffuse within a single layer, but inter-layer diffusion is more difficult. These phases are called smectic, or soap-like, phases, because soap is actually a smectic liquid crystal, where the layers can easily slip past one-another to give a slippery texture and at the same time generate a slightly opalescent sheen with a distinct period. When cooled even further, liquid crystal materials will finally solidify in crystalline form.

What is it about certain materials that allows the formation of these mesophases? At the risk of severely oversimplifying the situation, it is because they are longer than they are wide. When they are packed close together, like matches in a matchbox, they will most often point in roughly the same direction. Of course more detailed analysis must consider Vanderwall-type interactions, hydrogen bonds, material back-flow, and so-forth to really provide a physical basis for liquid crystal behavior. Nonetheless, even without understanding the minutia of molecule-to-molecule interaction in these materials, continuum theory models based on experimental data can be quite useful in simulation. One of these models has been adapted to the simulation of liquid crystal cells, and is described below.

Many of today’s liquid crystal materials are constructed around a mostly stiff biphenyl core with rather flexible carbon chains dangling from the ends. There are, of course, exceptions such as branched long-chain polymers, and others which are shaped like discs and stack as plates, but for the purposes of describing microdisplays, we will stick to the rod-shaped molecules which form nematic phases.

These rod-shaped biphenyl-based liquid crystals exhibit several properties characteristic of their longer-than-wide shape. Their electronic structure is such that they have different electronic, magnetic, and optical permittivities along different axes. In other words, electromagnetic fields propagating parallel to the long axis of a liquid crystal molecule will travel at a different rate than those fields propagating in some other direction! The dielectric anisotropy will cause induced dipoles in the material and orient the liquid

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Figure 3.0 shows a model of a typical liquid crystal molecule based on a stiff double benzene ring core and two flexible carbon chain tails.
crystals with an applied electric field. The optical anisotropy will in turn selectively delay one component of polarization and induce relative phase delays, or in certain configurations, just shift the angle of polarization.

We have now briefly discussed the intermolecular alignment properties of liquid crystals as well as their anisotropies. So the liquid crystals align, and when they align, the bulk material can advance polarization and delay phase. But how do the liquid crystal molecules align in equilibrium when no external fields are applied? The key lies in the boundary conditions imposed at the inside cell surface. The details of liquid crystal-to-surface interaction are still largely a matter of speculation and active research. Most models rely to some extent on arguments based on some combination of surface anchoring energy and surface topology. In any case, it is possible to treat surfaces by either surfactant coating, skew evaporation of oxides, or simply by rubbing them, so that liquid crystals which come in contact with these "magically" prepared substrates will tend to align nearby liquid crystal molecules along some preferred direction. This surface induced alignment can be used in combination with the intermolecular alignment forces to generate equilibrium patterns which range from homogenous fields of liquid crystals, to cells of strained helix-like arrangements.

**Electronic Properties**

Given an equilibrium alignment configuration as discussed in the previous paragraph, we can disrupt this arrangement with an applied electric field. Because of the rod-like anisotropy of the liquid crystal molecules, the dielectric constant varies with respect to the long molecular axes. When an electric field is applied to a material that has this large dielectric anisotropy, there is a large induced dipole moment, and the molecule will experience a torque which tends to align it with the field. There are materials which have permanent rather than induced polarization that behave similarly.

**Optical Properties**

As with the dielectric anisotropy there is also an optical anisotropy in liquid crystal materials. So by changing the mechanical alignment of the liquid crystal molecules, one changes the optical properties of the material. The case where the indices of refraction differ along the various molecular axes for a rod-shaped molecule gives optical birefringence; different components of polarization travel at different speeds through the material. This birefringence can be used in several different modes. Several of the most common modes were tested for application in microdisplays and are discussed below.
3. Making Liquid Crystal Displays

Optical Activity: Twisted Nematic Cells

The most frequently encountered cell arrangement of materials, surface treatment, and polarizers is called the "Twisted Nematic [TN] Cell," in which the substrate surfaces are "rubbed" at right angles to one another. The nematic material between the surfaces then forms a strained helix with a pitch commensurate with the cell thickness and the 90 degree twist imposed by the rubbing directions. When an electric field is applied across the cell, the liquid crystal molecules, in aligning with the field, disrupt the equilibrium helical

![TN_LCD_Cell_Operation](image)

Figure 4.0 diagrams the operation of a ninety-degree twisted-nematic liquid crystal cell. The device settles into a helical orientation equilibrium when no voltage is applied. This helix, combined with the material birefringence causes the polarization advance that allows light through the crossed polarizers. When a voltage is applied across the cell, the electric field disrupts the helix, killing the polarization advance to turn the cell opaque.
arrangement. When the field is removed, the liquid crystal molecules reestablish their equilibrium helix.

This action turns out to be useful when crossed polarizers are placed on either side of the liquid crystal cell. The relatively slow (relative to molecular scales) twist of the liquid crystal director in equilibrium serves to slowly advance the polarization of the incoming plane-polarized light through the cell's 90 degree twist, to emerge in the plane of the crossed polarizer on the opposite side. The result is a transparent cell. When the helix is disturbed by an applied electric field, there is no longer the same polarization advance, and the light retains its initial polarization and is blocked by the crossed polarizer on the exit side, and the cell becomes opaque. This advance of the angle of polarization in anisotropic materials is called "optical activity."

Guest-host Cells

There is a useful variation of the twisted nematic mode where dichroic dye molecules are added to a nematic mixture. While not liquid crystals themselves, these dyes are also long and thin and so align themselves along with the surrounding liquid crystals. The dye molecules are then considered low concentration guests in the liquid crystal host material. As you might guess, the optical absorption of the dye varies with orientation. The net effect is that the contrast of the display is often improved at the expense of a slight increase in the required drive voltages. This makes many of the Guest-host mixtures unusable for microdisplay application. One great benefit, however, is that the surface alignment preparation is very simple and there are several configurations which can omit the polarizers and increase the overall brightness of the display as well as further increasing contrast.

Polymer Dispersed Liquid Crystal Cells

Polymer dispersed liquid crystals [PDLCs] are another variation on nematic liquid crystals, but in this mode devices rely on scattering rather than optical activity. As the name implies, a nematic liquid crystal is mixed with a polymer epoxy in which it is soluble. When the epoxy is cured and solidifies, the liquid crystal phase separates into small liquid crystal droplets in a hardened epoxy matrix. The liquid crystal material inside each droplet will have a single dominant orientation in some random direction with each droplet pointing in different directions. The liquid crystal material and epoxy are carefully chosen so that the index of refraction of the epoxy matches the index of the liquid crystal along its long axis. In equilibrium, when the droplets all point in different directions, incoming light is scattered very effectively. When a field is applied across the cell, and the liquid crystals align with the field, the indices of refraction all match and the material becomes transparent. No surface preparation is required at all. No polarizers are necessary. These mixtures are by far the easiest to use and the most robust in terms of construction tolerance, dirt, and most other fabrication errors. Unfortunately, PDLCs are relatively new materials and are still under development. The surface alignment effects in the tiny
droplets is much stronger relative to the electric field. This means that the equilibrium is harder to disrupt and the PDLCs switch at rather high voltages. A year ago, they were switching at 70 volts. As of this writing they are down to 7 volts. In spite of their potential to greatly simplify assembly and manufacturing, this rather high switching threshold makes them unusable in microdisplays. As a result, the prototype microdisplays were fabricated using twisted nematic modes and materials. Next year new PDLC materials will most likely switch at under 5 volts, and they will then be the material-of-choice for microdisplay technology.

**Polymer Dispersed Electro-optic Effect**

![Polymer Dispersed Electro-optic Effect](image)

**Milky-white**

**Transparent**

Figure 5.0 diagrams the operation of a PDLC cell. In equilibrium, the liquid crystal droplets have dominant orientations in random directions. The mismatched indices of refraction scatter strongly. When a voltage is applied across the cell, the primary liquid crystal index of refractions matches the epoxy matrix and the material turns transparent.

**Birefringence in Super-twist Cells**

Birefringence is the simple effect of relative phase shift in materials with anisotropic permitivities. As previously mentioned, light travels with different velocity when polarized in different directions with respect to the long axis of liquid crystal molecules. This means that different components of polarization become phase shifted with respect to each other. Also, the amount of phase shift can be controlled by tuning the birefringence of the liquid crystal molecules in the cell. With the proper alignment conditions, this is again accomplished with the application of an electric field.

An electronically controlled birefringence cell is fabricated by rubbing the interior substrate surfaces parallel to one another, so that the liquid crystal molecules align parallel to the plate surfaces in the direction of rubbing. When a field is applied across the cell, the molecules begin to tilt towards the field, staying in the plane of the rubbing direction. This means that light polarized perpendicular to the rubbing direction (and hence perpendicular
to the long molecular axis in equilibrium) always experiences the same index of refraction or optical path length. Light polarized parallel to the director in equilibrium will experience a path length which is tunable with respect to the applied field. This is called tunable birefringence.

This tunable birefringence effect is also part of story in the super-twist displays of laptop computer fame. In the super-twist displays, a twisted nematic is doped with a chiral additive so that there is a preferred handedness to the helical equilibrium liquid crystal alignment. Then the surface alignment directions are rotated through more than 180 degrees. This creates a strained helix which has much faster mechano-electric transitions, albeit with fewer greyscales. This faster switching material is useful for video displays with faster frame updates. Just as with the twisted nematic cell, here there is also optical activity, but since the amount of rotation in the equilibrium helix is greater, there is also significant birefringence effect between layers. So the super-twist displays function using a combination of optical activity and birefringence.
4. Simulating Liquid Crystals

Liquid Crystal Continuum Theory

In order to better understand the possible behaviors of liquid crystal displays, lenses, gratings and holograms, I have written a material simulator for virtual experiments in liquid crystal physics. I was most curious about the topology of defects in liquid crystal alignment and how they would affect the optical quality of displays, gratings and lenses. For some time, there has been a general realization in the field that the most recent two-dimensional simulations failed to capture the full ensemble of defects observed in real three-dimensional volumes of liquid crystal material. This program simulates a full three-dimensional volume using a complete tensor orientation interaction.

The simulator has three major components. An iterative Laplace's equation solver determines electric fields due to voltages applied to pixels at the edge of the liquid crystal volume and incorporates local perturbations to the calculated field from the effects of

![Diagram of liquid crystal simulation](image)

Figure 6.0 shows a simulated volume of liquid crystals on a 10x10x10 finite-difference grid in a tuned-birefringence mode with the surface alignment directions parallel to the polarizers. A voltage distribution which varies linearly was written across the top of the volume. The result is a phase delay greater at the edges than in the center (for one component of polarization).

Figure 7.0 shows a simulated volume of liquid crystals on a 30x30x30 finite-difference grid with the same boundary conditions as figure 6.0. This volume has not quite equilibrated, and several orientation defects are visible. The local phase delay is mapped to intensity on the bottom of the volume surface.
oriented liquid crystal molecules. A successive over-relaxation module solves for the local orientation configurations of the liquid crystal molecules given the electric field determined by the Laplace solver module. Finally, an optical simulator which is an approximation to Maxwell's equations simulates the propagation of light through the liquid crystal volume.

The liquid crystal dynamic relaxation module is based on the continuum theory of liquid crystal relaxation first proposed by deGennes[4], and latter amended by Haas[5] for computer simulation in two dimensions. This new simulation test-bed incorporates the latest continuum-theory, extends it to a three dimensional liquid crystal volume, integrates an electric field solver, and performs optical analysis of equilibrium configurations.

This theory begins with the development of a tensor description of liquid crystal orientational order relaxation, because a simple vector field description fails to take into account the inversion symmetry of nematic molecules. The orientational order description starts with the definition of a 2-D order matrix for simple rods, and then extends the matrix to more complex shapes using a higher dimensional tensor. This tensor effectively

Figure 8.0 shows a series of 2-D slices from a 3-D nematic liquid crystal simulation. Local strain energy is mapped to intensity, so the lighter areas are where neighboring volumes are poorly alligned. The simulation starts in the upper left corner at high temperature and an isotropic orientation distribution. As the simulation progresses and the material thermalises, the local defects propagate and coalesce to eventually reach an equilibrium nematic allignment.
parametrizes how a particular liquid crystal molecule will tend to affect its nearest neighbors given an externally applied electric field. The simulation begins by initializing the external fields, setting surface alignment boundary conditions, and initializing the liquid crystal orientations to random directions. This is essentially the equivalent of heating the material past its clearing point where it begins to behave as a normal liquid with no orientational order. A set of relaxation equations is written based on the tensor order parameter to evolve the orientation of each liquid crystal voxel in the simulation. A finite-difference approximation to the relaxation equations is evolved to "cool" the liquid crystal that stabilizes in the nematic phase described by the order tensor. The electric field description is then recalculated using the Laplace solver for the new liquid crystal orientation. The electric and orientation fields are then alternately relaxed in increments until a stable equilibrium is reached. Finally, once a stable pattern of liquid crystal orientation is established, the optics module propagates a simulated plane-polarized light wave through the material and calculates the intensity and phase of transmitted (or reflected) light through (from) the cell.

The results of the simulations were very informative. There were, in fact, several types of defect structures not found in previous simulations. The results were verified to a certain extent when several problems with real liquid crystal displays involving reverse-tilt disclinations were re-created. The reverse-tilt defects occur when there is a local discontinuity in liquid crystal alignment and the director changes direction very quickly over a short distance. In a display this appears as a line or set of lines in the middle of a pixel. With the simulator, several appropriate boundary conditions were found to somewhat mitigate reverse-tilt defects, as well as verify the potential utility of VLSI microdisplay technology for lenses, gratings, and eventually real-time holograms.
5. Microdisplay Materials

Considerable attention was paid to the choice of materials for integration with the CMOS microdisplay backplanes. Conventionally fabricated CMOS chips typically operate between 0 and 5 volts. This is atypical for most liquid crystal displays which are normally switched at 20 volts. So a material was required which would switch at a lower voltage. There was also the requirement that the liquid crystal material have low resistivity, so that current would not leak across the cell from the pixel storage capacitors. If the chip is to be fabricated without a passivation layer to solve the ion accumulation problem, the material must be extremely pure.

I selected a series of materials for experimentation with different device modes including the following.

- Standard twisted nematic modes
- Super-twist nematic modes
- Guest-host cells
- Electronically controlled birefringence devices
- Polymer dispersed liquid crystals
- Polymer scattering materials

Each mixture was based on a low viscosity liquid crystal with high dielectric anisotropy (as shown in the previous section, there is a large difference in the dielectric constant of liquid crystals with respect to their long molecular axis, so there is a large induced dipole in electric fields). These specifications guaranteed that switching voltages would be as low as possible. Mixtures and modes that required minimal surface preparation on the die were preferred.

The twisted nematic materials I used were ZLI-4350, and ZLI-2340 from Merck. These were the first materials to work with the microdisplays. Several Guest-host materials from Merck are still under experimentation for other display modes including ZLI-8550A and ZLI-8443.

For experimentation with the general properties of PDLCs I started with an E7 nematic mixture, a traditional experimental liquid crystal from BDH mixed with Norland Optical adhesive #65 for the polymer matrix. Unfortunately, the switching voltage was too high for practical use (around 50 volts in reasonable cell configurations) and newer PDLC materials were purchased from Merck including their TL-205 to TL-215 series. Transition points for these newer materials were found to be as low as 7.5 volts. These levels were almost low enough for microdisplay use, but not quite.
Continuing experiments are under way using some ferroelectric and focal-conic scattering materials to find new cell configurations which will exhibit high contrast, fast switching, and require little surface preparation. All of these properties must manifest themselves at low transition voltages. For the moment, current microdisplays are still operating in more standard twisted nematic modes.
6. Microdisplays

VLSI Design

Once a reasonable understanding of the physical properties of liquid crystal materials and surface properties was established, the major part of the microdisplay design effort lay in the development of the CMOS active backplane which would modulate the orientation of the liquid crystal molecules. As discussed in the previous section, in order to affect the optical reflectivity of a liquid crystal pixel, one must control the local orientation of the uniaxial molecules above it. A microdisplay is composed of an array of tiny reflective aluminum pixels coated with liquid crystal material and then sealed with a grounded transparent common electrode. This microdisplay functions by storing charge on each pixel electrode thus creating a potential difference with respect to the indium tin oxide common electrode on the coverglass. This generates an electric field which will tend to orient the liquid crystal molecules. The more charge that is written to a pixel's storage electrode, the greater the electric field above it. A stronger field causes tighter liquid crystal alignment which leads to greater optical activity. To modulate the optical activity of a liquid crystal cell, specific amounts of charge must be stored on each of the display pixels. This VLSI design effort has solved the problem on a micron-scale.

There are four main components of the CMOS microdisplay chip: the pixel design, the design of the pixel addressing structure, and the I/O structure including the video input decoding and the pads for transferring data into and out of the microdisplay chip.

Pixel Architectures

At first glance, it might seem that designing arrays of memory cells to store charge on tiny capacitors is a problem that has been solved time and again for commercial DRAM and SRAM devices. As is often the case, the parts that seem simple are usually hiding some real subtleties. The design of the microdisplay pixel is by far the most troublesome aspect of the VLSI design project. The rather difficult and often conflicting constraints on the pixel design arise from the fact that each pixel must not only store charge and have the proper electronic characteristics of good memory cells, but they must also have proper optical and surface properties so that their effects on the optically active liquid crystals will be visible.

The primary components of each pixel are an active element to allow data storage to that pixel, a memory element, either a capacitor-type DRAM cell, or a static SRAM cell which
can store a pixel's data (charge) between frame refresh cycles, and a reflective electrode which is connected to the charge storage device. Here is a brief description of constraints on the design of each pixel:

**Fill-factor**
The fill-factor issue is a serious problem for today's generation of flat-panel displays, but is not so terrible for the reflected-mode microdisplays. Fill-factor is a percentage measure of the optically active display area in proportion to the total area of the display. Since each pixel must be electrically isolated from its neighbors there is a minimum spacing between pixels as established in the layout design rules for the fabrication process technology. Microdisplays don't suffer as badly from this minimum spacing requirement because the active pixel address circuitry, the storage capacitor, and the address buses can all be placed beneath the reflective electrode. While this multi-layer arrangement introduces some other problems in pixel planarity as discussed below, the fill-factor is limited only by the minimum spacing of the top level of metal used for the reflecting electrode. The 500x400 pixel microdisplay with 15 micron wide pixels has a fill-factor of 75%. The 1024x768 pixel microdisplay currently being designed will be fabricated using a finer resolution process and will achieve a fill-factor of 82%.

**Data Storage**
Once a pixel has received its data, it must retain that data until its next refresh. The big decision here is: should the data stored be either digital or analog? The analog pixel is the simplest design, being merely a select-line gated pass transistor connected to a capacitor. When a pixel's line is selected it turns on the pass transistor, and data is written from the column address bus onto the storage capacitor. This simple analog pixel has the advantage of few components and a small layout area requirement. This design can also store analog data and has intrinsic greyscale capability. But as with other analog systems, the DRAM pixel lacks any kind of noise margin, is susceptible to cross-talk through the parasitic capacitances in the pass transistor and capacitive coupling to neighboring pixels. Also, as a passive storage device, the analog pixel has no mechanism to preserve data over long periods in the face of leakage current.

![Figure 9.0](image-url) is a schematic diagram which depicts the general architecture of a microdisplay chip. This circuit is composed of an array of DRAM cells where the single storage capacitor in each pixel is actually only the capacitance of the pixel drive electrode to the common ground in the coverglass. Additional storage capacitance was added in later designs.
The other data storage alternative is a standard digital SRAM cell composed of between six and eight transistors. Operating in this binary node provides both noise immunity and static data storage. However, the greyscale ability disappears unless time-multiplexed pixel data is used. The resolution of the display also decreases, as each pixel must now be large enough to contain more components. The very high resolution displays which push the lithography limits of current process technology will mirror the trends in memory technology, and will likely be DRAM-based.

Data Storage and Photoelectric Leakage current
The time constant for data storage in the high-resolution DRAM microdisplays depends on the size of the storage capacitor and the amount of leakage current, both through the pass transistor and due to the photoelectric effect. Unfortunately, the largest storage capacitance that can be fabricated in a standard CMOS chip is the gate capacitance of a transistor. But this is precisely the part of the pixel which is most sensitive to leakage current due to the photoelectric effect. In order to see the display, a fair amount of light must illuminate it. This generates electron-hole pairs which cause leakage currents across the p-n junctions at the edges of the transistor active areas. This means that the best storage capacitor also has the highest leakage current.

One possible solution is to design substrate charge collectors to absorb some of the photoelectric carriers in the substrate. This idea, however, requires an additional bus to bring a substrate power connection to each pixel, and would eliminate a large amount of area that could otherwise be used to make a bigger storage capacitor.

The final pixel design for the 500x400 DRAM microdisplay omitted a transistor/thin-oxide storage capacitor. In spite of the decrease in capacitance that came from using the capacitance of the liquid crystal sandwich alone instead of a transistor gate, there was less leakage current and a longer RC time constant. Additionally, the top layer metal electrode was placed on top of the active pass-transistor area to shield it from light as much as possible. The resulting cell had a data storage time constant that varied from 500 microseconds to 10 milliseconds depending on the intensity of the viewing illumination. A typical illumination setting for a heads-up display resulted in a pixel persistence of 4 milliseconds for the 500 x 400 display.

The latest pixel architecture currently under design for the 1024x768 pixel microdisplay uses the extra polysilicon and metal layers of newer fabrication processes to form extra storage capacitors with no active area. This design is expected to result in much less leakage current and still have a reasonable amount of storage capacitance. As an additional safety measure, the top layers of metal were staggered and overlapped like roofing shingles to form an optical baffle so that even less light would reach the pass transistor.
Parasitic Capacitance and Cross-talk
Particularly in the analog DRAM microdisplay, cross-talk is a problem. The source-drain capacitance of the pass transistor is about one sixth of the capacitance of the liquid crystal cell without any storage capacitor (in the 500x400 microdisplay). This means that after data is written to a line of pixels, and that line-select bus is set to zero volts, with the following line-select turned on, the data that was just written degrades by 16 percent.

![Diagram](image)

**Figure 10.0** is a simulation output from the circuit in figure 9.0. The first trace is a pixel output voltage. The second trace is that pixel's line select voltage. The important point is that the storage capacitance of the pixel must be large enough so that the pixel voltage does not drop significantly when the line-select is turned off.

Another problem is the lateral coupling capacitance between neighboring pixels. This causes the data written to one pixel to bias the data written to all of the neighboring pixels. These parasitics only get worse as finer pitch fabrication processes decrease the inter-pixel separation. The best solution to-date is to make the largest storage capacitor possible so that it dominates the parasitic effects.

AC Coupling to Liquid Crystal Materials
A rather interesting problem arises from impurities in the liquid crystal materials. Many of these impurities are ionic, and when a DC field is applied from a pixel electrode to the common ground on the coverglass, these ions will collect over the surfaces of the pixel electrode and coverglass ground. These accumulated ions then reduce the field strength across the cell gap and thus reduce the net optical activity of the display. Over time, the display degrades rather rapidly.

The ionic contaminants will only collect against an insulating surface. If the ions can actually come in direct contact with the pixel electrodes, they will be neutralized by the stored charge there. Two things, however, stand in the way. First, the CMOS chips are
typically passivated with an insulating layer of SiO$_x$. Second, the alignment layer used to force an equilibrium director configuration the liquid crystal cell is also typically either an additional layer of silicon oxide (see below under Liquid Crystal Surface Alignment) or a polyimide both of which are good insulators. This is actually not so bad. Since there will be an additional seal over the device with the liquid crystal material and the glass cover, as long as the liquid crystal material is benign to the CMOS process, the passivation can be eliminated altogether. Newer alignment materials which are conductive are also under development.

An alternative solution is simply to insure that there is no DC field across the liquid crystal cell. This can be done in a number of ways. The simplest way is to swap the polarity of the data and the common ground on successive frames of data. Unfortunately, this invalidates the entire display while the new frame is written for the new common electrode voltage. The result is significant flicker at typical update rates.

The 500x400 digital SRAM microdisplay incorporates an innovation which retains the data as both the common electrode and the power supply rails are swapped at the same time. Instead of connecting the SRAM cell's cross-coupled inverters directly to the liquid crystal electrode, the inverters gate the power buses to the liquid crystal drive electrode. When the power rails are swapped along with the coverglass common ground, the data in the array is retained. This also allows the AC frequency to be adjusted independently of the frame update rate. The digital microdisplay chip which incorporates this innovation is still under test and will be reported in greater detail at a later date.

**Reflectivity**

The top electrode of each pixel must be as reflective as possible in the case of the nematic liquid crystal displays. As most metals in standard fabrication processes are silicided to help prevent electo-migration and spiking, the texture of the aluminum layers is somewhat grainy and not as reflective as a more pure metal electrode would be. A customized CMOS fabrication process would be required to gain the optimum reflectivity.

Some of the polymer dispersed liquid crystal materials are exceptions to the need for highly reflective pixel electrodes. These materials require a scattering electrode to compliment the

Figure 11.0 is a Scanning Electron Micrograph of a DRAM pixel showing the large surface variations of the ORBIT process. The fine-scale bumps are from the Silicon-oxide surface alignment treatment, and are completely dominated by the lack of process planarity.
scattering effect of the dispersed liquid crystal droplets. These scattering pixels are best formed out of polysilicon.

**Planarity**
In order for the liquid crystal materials to align properly on the surface of a chip, the surface must have a uniform planar topography. This was simply not the case in our prototype CMOS displays that were fabricated in the ORBIT 2.0 micron CMOS process. These prototype chips had surface structure that varied by as much as three quarters of a micron in height. The result was poor equilibrium alignment of the liquid crystal materials which resulted in reduced contrast of the display prototypes.

**Passivation and Process Repeatability**
A final problem with the passivation layer was that the overglass etch varied so widely from one wafer run to the next that on otherwise identical chips, the cut over each pixel varied from 5 to 15 microns across. The best microdisplay results so far use a spun polyimide alignment layer. This was mostly to the hole filling effect of the spun layer. Part of the contrast difficulties stemmed from the problems of wetting this inhomogenous surface, and maintaining coverage of the surface at low spin velocities. Although a thicker

![Figure 12.0 shows two identically designed DRAM pixels produced on different fabrication runs. The overglass in the first is completely gone. The second is barely etched at all.](image)

spun alignment layer might serve a better planarization purpose in the future, that option was not open in the fabrication of microdisplays from packages substrates because a meniscus formed at chip edges when the spinner was operated at velocities lower than 3600 RPMs. It is now clear that partial passivation cuts over each pixel were a bad idea for twisted nematic operating modes. It remains to be determined whether no passivation at all is preferable to complete passivation. The next prototype chip will test both options.
The Final Pixel Designs

Four different prototype microdisplay chips have been fabricated to test different aspects of the technology using the MOSIS chip brokerage. Each of these first four die were designed in a 2.0 micron process to keep prototyping costs at a minimum.

The first tiny chip was an 18x18 array of DRAM pixels that was intended to test the first version of the microdisplay compiler for optical distortion compensation. Unfortunately, it was the first chip designed with a new CAD tool, and suffered from bugs in the output conversion routines. There were defects in the I/O pads which rendered them inoperative and there was no way to test the die. Fortunately it was a small chip and an inexpensive test that revealed a great deal about the defects in our design tools.

The second chip was large grating of aluminum strips that was intended as a test pattern to experiment with liquid crystal materials and chip surface properties. It was also intended to assess the possibilities of using diffraction for holographic lens and grating construction as well as diffraction-based color pixels. This chip was very simple, merely a set of gated metal lines with every tenth strip connected to an output pad (so the effective period of the gating could be modulated). In the course of materials experiments, it has proven invaluable. All of the mechanical and optical tests began on this test array which allowed debugging of the optical and surface properties independent of VLSI electronics problems.

The third prototype chip was a 500x400 array of DRAM cells with no storage capacitor other than the capacitance of the liquid crystal cell itself. The pixel address structure was a two-dimensional shift-register which was designed to work as a CRT raster display. The line-select shift-register array was clocked to select a single row of pixels. The column-select shift-register array gated a video input signal onto a single column of pixels.

Figure 13.0 presents both the schematic and VLSI layout for the most recent pixel design. The pixel storage capacitors are form by the METAL1 and Polysilicon layers, and are arranged so that previous select lines provide a virtual ground. This made an extra ground bus redundant, saved a significant amount of display area, and greatly improved the fill-factor of the display.
so that the pixel at the intersection of the selected row and column had data written to the storage capacitor.

The fourth prototype microdisplay was similar to the previous one differing only in the pixel design. Each pixel in this case was a binary SRAM cell modified with a provision to swap the power rails and common electrode of the coverglass to provide AC material coupling compensation for the ionic charge accumulation problem. Testing of this device is still underway.

**The Pixel Addressing Structure**

There were two primary designs for sending data to each pixel, either serial data input and clocked shift registers to emulate CRT operation, or memory address decoders with parallel writes to a "word" of pixels. In each case, the major obstacle was to develop an address structure of a fine pitch to match the very high resolution of the DRAM and SRAM pixels. Shielding from the photoelectric effect in the form of top level metal sheets covering the shift register circuitry were not included in the first four prototypes, but would have significantly improved the performance of the device.

The first four prototypes were based on a set of row and column shift registers. The inputs to the devices consisted of:

- Analog video input line
- Horizontal pixel clock
- Vertical line clock
- Horizontal reset
- Vertical reset
- Power
- Ground

The horizontal pixel clock selects which column of pixels to send video data to. It asserts each column in turn, and is reset to the first pixel by the horizontal reset signal. The vertical line clock which selects which row of pixels is to receive data, cycles once for each complete row of pixels, and is advanced simultaneously with the horizontal reset signal. The vertical reset signal which begins writing a new frame resets the row-select shift registers to the first pixel.

Each shift register stage was composed of a pseudo-two-phase clocked shift register. This design used four clocks total, two phases to each shift register array. Future designs are underway for shift registers which use only single clock phases in order to further reduce the I/O pin count and incidentally simplify the register layout. The main problem in this design, particularly without the optical shielding, was that the only select-data storage mechanism between shift-register stages was the gate capacitance on the next shift-register stage. There was no refresh mechanism to compensate for the photoelectric leakage.
current, and beyond a certain level of illumination intensity, the select data would vanish before the next line was clocked. Testing at higher intensity levels was performed by simply shielding the edge of the microdisplay chip with razorblade edges.

This serial shift register scheme was originally chosen so that the device would mimic the operation of a television or CRT with signals analogous to video input, vertical and horizontal retraces. The clocked serial input raster scan design was also for the purpose of keeping the I/O pin count as low as possible. This was a very useful design feature when the coverglass had to be installed without dislodging the bond wires on the CMOS package.

Eventual serial address designs will most likely integrate the video-synch decoding circuitry directly on the chip so that only three inputs will be required, power, ground, and composite video. With the further incorporation of on-chip radios such as those under development at Stanford and UCLA, a completely wireless and portable device will result.

Figure 14.0 shows the schematic and VLSI layout representations of the most recent design for the row and column decoder circuitry. Each row-select line is composed of a clocked precharge nor gate to decode the vertical address bus, followed by a pass gate to prevent the precharge from writing to all the select lines before the address decode is valid. The
The design for the next microdisplay which is well underway, has an address structure composed of a more standard memory decoder. The microdisplay then basically becomes an electronic-write/optical-read memory chip with a photo-active layer on top. This random access scheme is the easiest to interface as the design can mimic any one of the most commonly used memory chip pin-outs. Data can be written to any pixel in any order, so that barring mandatory refresh cycles, only changing pixels need to be updated on successive frames. This may very well be a critical issue at extreme resolutions were I/O bandwidth is a bottleneck for data display.
7. Silicon Compilers for Microdisplays

Because of the considerable investment in CMOS design tools to date, there is already a significant repertoire of design utilities that can be immediately applied to the fabrication of microdisplays. The design requirements for this type of display system are quite different from those of similar spatial light modulators that are under development for optical computing applications. As a result, many new criteria for display optimization must be tested. A rapid technology transfer from standard CMOS foundries and CAD tools will enable a significantly accelerated development life-cycle. One of the most powerful paradigms in CMOS fabrication technology is the use of silicon compilers to automate VLSI design procedures. This technology has now been applied to the VLSI microdisplays. This section describes several developments that followed immediately from the application of current CMOS layout compiler techniques and tools.

Distortion Compensation

One of the most attractive applications for the microdisplay is an eyeglass mounted set for virtual reality display. But there is a fundamental tradeoff between the complexity and weight of the optical system used to magnify and view the display versus the weight and inconvenience of large heavy optics. To assist in viewing microdisplays, a good microscope can provide a high quality narrow-angle image, but is rather inconvenient to lug one about attached to a pair of eyeglasses. On the other hand, a simpler (shorter focal length), more lightweight optical system for wide-angle images introduces considerable distortion. Several companies have

![Image of a microdisplay chip](image)

Figure 15.0 is a screen dump of the microdisplay compiler in action, instanting a pre-distorted array of DRAM cells with compensated storage capacitors.
begun compensating for this distortion in artificially generated virtual reality displays by preprocessing the image data in real-time to pre-warp the image data before it is "distorted" by a small wide-angle optical system. Real-time image processing computers for non-local algorithms are still too large and are not portable. Truly portable systems require another solution.

One solution investigated in this research project was to develop a tool that would use the automated layout of a VLSI pixel array to compensate for optical distortions and aberrations. Ray tracing experiments through actual optics can generate a distortion function which is monotonically increasing with radius from the optical axis. Therefore, there exists an inverse function which can negate this nonlinear distortion. A third-order polynomial fit to the distortion function data provides a good approximation to the inverse function. This radially symmetric function is then used to position and scale the individual pixels of the display. Since the array is very regular, albeit of peculiar and specific form, a silicon compiler was written to implement a scaleable architecture, where multi-sized chips can be "auto-instanced and routed" with the late-binding specification of only a few parameters such as DISTORTION_FUNCTION, CHROMATIC_ABBERATION, ARRAY_WIDTH, PACKING_DENSITY, and so forth. Figure 15.0 shows the layout of a small prototype device intended to compensate for a typical short-focal-length magnifier distortion. The current microdisplay compiler even compensates for the varying warped

Figure 16.0 shows one half of two different pixel array outputs from the microdisplay compiler. The array on the left is for comparison. The array on the right has been anti-aliased by random jitter added to each pixel's position.
pixel capacitances by adjusting the size of the buried storage capacitor for each pixel. The microdisplay compiler was written in C and outputs complete pixel arrays in the CADENCE design tool language called SKILL.

Anti-aliasing With Pixel Jitter

Another design problem specific to displays as opposed to spatial light modulators for optical computing, has been that of image aliasing. The finite pixilation of an image typically resulted in moiré patterns in regular arrays. Several products have addressed this problem. One example was Edsun's Ramdac interpolation chip for analog displays. The implementation of the microdisplay compiler has led to a solution which requires absolutely no extra computation hardware or run-time overhead. The compiler simply perturbs the position of each pixel by a small random amount in a random direction. This subtle breaking of symmetry and regularity greatly decreases aliasing effects at little cost.

Super-pixels

When lower resolution images (e.g., NTSC video) are magnified to fill large fields of view as in the virtual eyeglass application, each pixel becomes rather large and obvious. There is an elegant solution using the modularity of modern VLSI layout tools and the microdisplay compiler. Simply replace each pixel cell in the image array with a group of pixels. Each new group of pixels consists of one central pixel connected to the line and pixel drivers as before, surrounded by a group of sub-pixels which interpolate between neighboring central pixels (see figure 6.0).

In addition, there is no reason that the inter-pixel interpolation must be linear. These sub-pixel interpolators can be modified to perform thresholded interpolation for maintaining image discontinuities, or perhaps used to detect edges or otherwise perform local image processing convolutions. This feature is implicitly designed into the microdisplay compiler as the only change required is the substitution of more complex pixel layouts into the same compiler structure.

Figure 17.0 illustrates the superpixel idea wherein only the major pixels are addressed. The sub-pixels merely display data interpolated from neighboring major pixels.
Integral Single-chip Computing Displays

The purpose of the prototype microdisplays was to experiment with liquid crystal-on-silicon technology and expose the fabrication and manufacturing difficulties of developing this new display technology. The level of integration with computing circuitry was fairly modest, being limited to drive and address circuitry and test structures at the die edges. The substrate used for the microdisplays is just that which is common to the microprocessor industry. The current microdisplay pixel driver designs demand very little in terms of silicon real-estate, leaving considerable room for the incorporation of additional computing circuitry. With hardly any changes to either microprocessor design, or microdisplay layout, both computation and display systems could be integrated on a single chip. Since it is a simple matter to create a nicely modularized design with current silicon compiler technology, arbitrary changes to individual components like the pixel design or line driver circuitry are incorporated with very low development overhead. The notion of integrated computation and display capability is then easily extendible to the addition processor-per-pixel schemes for performing highly parallel image filtering or classification algorithms with a mere interchange of the pixel module design.
8. Microdisplay Assembly

This section describes how to assemble one of the microdisplay devices in detail. The single most pervasive theme in the whole assembly process was that of cleanliness. The devices under construction are all had features on the micron-scale. Even the tiniest speck of dust was likely to destroy a pixel, disrupt liquid crystal alignment for 100 microns, or worse yet, short the device completely.

Cleaning occurred at or between every step of the process, so for convenience all of the cleaning techniques employed will be summarized at the beginning, and then each assembly step will be detailed in turn.

The general procedure for assembling a microdisplay device, once you have designed and fabricated the CMOS backplane, is as follows:

1. Prepare the surface of the CMOS chip for liquid crystal alignment.
2. Deposit transparent conductor on the inside coverglass surface for the common ground contact.
3. Prepare the coverglass surface for liquid crystal alignment.
4. Apply spacers to either the substrate or coverglass.
5. Bond the coverglass to the substrate.
6. Fill the device with liquid crystal material.
7. Seal the fill hole.

Figure 18.0 This schematic of a mechanical design for a microdisplay is also suitable for lensing and grating and holographic applications. This illustrates one assembly method where a coverglass is sputtered with a conductive coating such as Indium Tin Oxide and then bonded to the CMOS driver backplane with a spacer in between. The device is then back-filled with an appropriate liquid crystal material.
Device and Substrate Cleaning

The weapons in the microdisplay cleaning arsenal ranged from mechanical brushing, to chemical rinsing, to ultrasonic baths, and finally in extremely stubborn cases, plasma etching. All of the substrates were initially subjected to an ultrasonic bath/RCA cleaning (the industry standard mix of de-ionized water, hydrogen peroxide and trichloroethylene), and were then rinsed with de-ionized water and methanol. This served to remove most large particles and organic contaminants. One series of chips from the ORBIT foundry however, suffered severe adhesion problems during later surface preparation steps. It appeared that an oxide layer had grown over the chip's passivation layer. It was necessary in that case to etch the chips in an oxygen plasma for two minutes to remove the surface oxide. Afterwards the surface treatments adhered quite well.

Between each step, save where the acetone would attack uncured adhesives or polyimides, both the substrate and the cover were rinsed with acetone, trichloroethylene, and methanol, and finally blown dry with a filtered nitrogen gun. Even with these precautions, shorts due to contaminants were common in our rather dirty experimental environment.

The Common Electrode

The goal of this step was to make an electrode which had good conductivity, was transparent, had appropriate surface chemistry, and was planar. The two main choices were either evaporation or sputtering of indium-tin-oxide [ITO] or thin layers of chromium and gold. After considerable experimentation, the best choice seemed to be an 800 angstrom layer of sputtered ITO. Then it was discovered that one could buy polished glass coated with high quality (low resistivity) ITO films from Donnelly Inc. The commercially available pre-coated glass was the best option.

Surface Coatings for Liquid Crystal Alignment Layers

This step turned out to be the most difficult and critical step in the entire project. The purpose of the surface coatings on both the substrate and the glass cover was to cause liquid crystal molecules in contact with that surface to align in a single desired direction.

There is still a considerable amount of research and speculation into the ultimate physical basis for the preferred alignment directions given particular surface treatments. The two leading theories depend upon either relative surface energy, or mechanical corrugations and surface impurities. In either case there are two basic methods for establishing this directional bias on surfaces.
The first, and most widely used method in industry today, is the "rubbing" method. Let me demystify this black art by being a bit more specific about what worked for the microdisplays. After the surface in question was cleaned, a thin coating of adhesion promoter was spun on, followed by a layer of some polymer or polyimide. The polyimide was then cured, and rubbed with a textured cloth. A good choice for the cloth was standard velvet available in most fabric retail stores. Undyed cloth worked best, but was hard to find. Linen or white colors performed best, but even black velvet worked. The velvet material was selected from the center of the bolts, and was handled only with gloves in order to prevent the accumulation of oily contaminants from skin contact. Cloth treatments and coatings such as Scotch-Guard which severely altered the surface chemistry of the rubbed surfaces were avoided as they gave unpredictable results.

![Figure 19.0, the microprocessor controlled rubbing machine.](image)

Almost anything done to the surface, from varied polyimide curing durations and rates, to altered duration and pressure of rubbing changed the pre-tilt angle of the liquid crystal. Changes in pre-tilt angle (the angle that the molecule make from the surface) caused large changes in the effective contrast and disclination structure. These variations were critical parameters in the fabrication of super-twist and electronically controlled birefringence displays. In order to perform repeatable experiments with rubbing techniques, a rubbing machine with micrometer pressure adjustments and a microprocessor controlled linear stage (described in the Appendix) was designed and built. The settings which worked best for the twisted nematic mode microdisplays can be approximated by hand with ten passes of a velvet-coated piece of plastic at a pressure of two pounds per square inch.

The other method of surface preparation used for the microdisplays was to evaporate an additional layer of SiO₂ at an angle to the substrate. This in turn created a rippled surface with texture on the micron scale. This was enough to influence the liquid crystal alignment. Different angles of evaporation resulted in different pre-tilt angles.

The microdisplay experiments with skew evaporation performed poorly because of the poor planarity of the 2 micron CMOS process used to fabricate the chips. The polyimide rubbing techniques were able to compensate for this to some extent by preferentially filling in the holes in the passivation layer during the spinning process. Future microdisplay chips will have more planar surfaces, so further experiments with skew evaporation are necessary in the next generation of substrates.

One critical element of safe surface preparation was static protection. CMOS dice are very sensitive to high pressure and static discharge. So when coatings were applied by a
thermal or e-beam evaporator, all the leads of the chip package were grounded in a
custom jig. Low evaporation rates were used so that charge accumulated in isolated
circuit nodes leaked away through the substrate before breaking down any oxides. With
the rubbing techniques, one additional concern was that the chip be particularly clean.
Small specs of dirt concentrated a lot of pressure in a small area and dug furrows through
all the layers of circuitry when the die surface was rubbed. There was no telling what was
shorted or opened. Needless to say, the furrowed chips failed to operate.

The most attractive and promising techniques were found using those materials such as the
polymer-dispersed and guest-host displays which required little or no surface preparation.
As those materials mature further, the need for this series of surface treatment will deciine.

**Spacers**

Spacers were inserted between the substrate and the coverglass to insure that there was a
precise and uniform cell thickness. For very narrow cell gaps in the one micron to three
micron range, a spun layer of polyimide was photo-lithographically etched to remain only
around the edge of the die. These very narrow-gap displays were extremely sensitive to
dust and contamination. The best results as of this writing were with thicker nematic cell
configurations. For thicker spacing as used in the twisted nematic mode microdisplays,
small micro-spheres and rods were disbursed across either the cover or the substrate
before they were bonded together. Cell spacing was optimized for maximum contrast and
minimum switching voltages. With the ZLI-4550 nematic mixture, a ten micron cell gap
switched nicely at 0.3 volts.

A common technique for disbursing the glass spacers in industry is to mix them in a
volatile solvent like freon or methanol, and then spray the substrate. The solvents
evaporates, leaving a distribution of spacers proportional to their initial concentration in
the solvent.

This aerosol spacer application worked fine for larger flat panel displays and even the
scattering-mode microdisplays, but failed miserably when the spacers themselves were
almost as large as the pixels in the display. The technique of choice for the microdisplays
was to mix the spacers directly with the glue used to bond the coverglass to the substrate.
Then, spacing and bonding was performed in a single step as described below.

**Coverglass to Substrate Bonding**

In most larger flat-panel display manufacturing processes, a glue gasket is applied to the
coverglass with a tiny 6 mil dispensing needle, the spacers are sprayed on, and the glass is
pressed down onto the substrate. The two millimeters of bleed in the strip of glue is
acceptable for a 10 inch display, but would obscure more than a third of a microdisplay.
The technique that worked best for microdisplays, was to hand apply minuscule amounts of glue (with spacers mixed in) to two opposite edges of the coverglass, and gently squeegee off as much as possible, relying on the spacers to preserve a thin layer. This was a poor-man's substitute for screen printing, as the equipment is still on order. A fine 600 mesh screen with the appropriate seal pattern should work splendidly on either individual die or wafer scales.

**Liquid Crystal Filling**

The standard liquid crystal filling method usually follows the cover-to-substrate bonding process, where a glue gasket is formed around the entire edge of the substrate save for a small hole through which the liquid crystal material is inserted. This is usually done by putting the cell in a vacuum, placing a tiny drop of liquid crystal material at the fill hole in the glue gasket, and raising the pressure of the vacuum chamber so the liquid crystal is sucked in with no bubbles. Then the fill hole is sealed with an additional glue plug. The whole procedure is best carried out on a hot stage so that the liquid crystal material can be heated past its clearing point and will flow more easily against the substrate and cover surfaces with no initial directional bias from the filling process. This is called *back-filling*, and requires a vacuum chamber with a hot plate and a mechanical feed through.

Since the lab lacked any such chamber, a much simpler technique was employed. Instead of applying the bonding gasket entirely around the chip save for a single fill hole, two holes opposite one another were left. A drop of liquid crystal material placed at one hole filled the device in under a minute by capillary action alone. The trapped air escaped through the opposite hole, and then both were sealed. No vacuum was required.

**Mounting and Packaging**

The entire assembly process would have been much simpler if carried out at the wafer scale rather than on single die. Each of our prototype microdisplay devices was provided to us by the MOSIS silicon brokerage in pin-grid-array packages with the die already bonded. This made electronic testing trivial, but sorely complicated all of the materials and surface property experiments as well as the final assembly of the microdisplay devices.

The most promising interconnect technology are the El-Form heat sealed flex connectors. These are tiny silver past wires that are silk-screened onto an adhesive backed plastic flex-pc strip. When the very fine pitch silver wires are pressed against bonding contacts and heated, the epoxy reflows and cures, and the silver paste makes contact with the chip bond pads. There is no other package required, and the final display device is a mere 1cm x 1cm x 1 mm.
While this set of four prototype chips were tested in the pin-grid-array packages, latter version will be manufactured and assembled at the wafer scale, then diced, then bonded to the flex-connectors.

**Testing and Evaluation**

Electronic testing and evaluation was carried out using two sets of microcontrollers to drive the microdisplays. The first board was a custom MC68C332-based board that was developed for a mobile robot vision system by Gavin and Yamamoto, and was suitable only for test patterns and small images. The second test setup is based on the Texas Instruments C30 digital signal processing board by Barnhardt which was fast enough to write persistent patterns to the entire DRAM microdisplay. Work is continuing to interface the microdisplay to a PC video board.

Optical and materials data was gathered mostly with a HeNe laser and a photometer for measuring contrast ratios and pixel switching rates and persistence.
9. The Four Microdisplay Chips

The Tiny-chip

This was a tiny 18 x18 array of DRAM pixels warped into a test pattern which approximated the inverse of the distortion function of a popular virtual reality headset. The serial address circuitry can be seen along the edges of the array. While this chip was useful for verifying that we could, in fact, layout displays in odd patterns for optical compensation, it was electrically useless due to bugs in our nascent design tool which output incorrect wires and layers to be fabricated. Fortunately, this was an inexpensive mistake which told us a great deal about our CAD setup.

Figure 20.0 shows a photograph of the first pre-warped Tiny-chip produced by the microdisplay compiler, and all of the integrated drive circuitry at the corner of the chip.

The Grating Chip

Aside from the buffers in the I/O pads, this chip has no active components. It is composed of a series of aluminum strips at a 4 micron pitch where every tenth strip was connected to the same output pad. The idea was to have a test chip that would survive higher than normal voltages for materials testing, and also to have a substrate to test the possibility of making electronically tunable diffraction gratings, lenses, and holograms (see the Next Steps section below). One half of the chip was a single dimensional grid while the other had a 2-D array of strips.
This chip was made to work in spite of another CAD tool bug which swapped the $p$ and $n$ diffusion layers in the I/O pads with a rather amazing bit of laser surgery at Lincoln Laboratory. A dye laser was used to vaporize some aluminum traces to isolated the shorted pad diodes. This pad failure provided another cycle of feedback on the setup of the VLSI CAD tools. The grating chip itself proved invaluable for testing materials properties and also demonstrated electronically controlled diffraction and color selection (see the Next Steps section).

The 500x400 DRAM Chip

This was the first microdisplay device shown to be fully functional. Test images have been displayed on the chip at resolutions up to 200 x 200 and are currently limited by the slow speed of the microcontroller supplying the image data. The new C30-based board should solve this limitation and allow the full use of the microdisplay chip.

The contrast ratio of the first test device using a twisted nematic mode was a rather disappointing 5.3 to 1. This was mostly due to the poor equilibrium alignment of the liquid crystal materials on the CMOS chip because of the lack of planarity in the 2.0 micron fabrication process. The lack of planarity was further aggravated by the unanticipated design error of placing an overglass cut above each pixel. This will be corrected in future versions of the microdisplay, where the passivation is either complete, or absent, as long as it is uniform. Finer resolution CMOS processes will also be significantly more planar. Experiments with test devices of this type showed contrast ratios exceeding 40 to 1 can

Figure 21.0 shows a corner of the 500x400 DRAM microdisplay with the column and line-select circuitry as well as a corner of the pixel array.

Figure 22.0 Shows a field of DRAM pixels with two columns on the right turned on. Uniformity and contrast still need work.
be expected in more planar die with few additional changes. The pixel overglass cuts may, however, prove useful in experiments with ferroelectric liquid crystals which require much narrower cell spacings. Experiments are still underway for these newer materials.

As mentioned before in the VLSI design section, the persistence of charge on a DRAM's storage capacitor had a time constant from four to ten milliseconds for a typical illumination level. This will also improve in later versions as the larger storage capacitance will allow more charge storage and metal light baffles will reduce the photoelectric leakage current. The mechanical switching speed of the twisted nematic mode used in the prototype DRAM microdisplay was also in the millisecond range.
10. The Next Steps

The Next Microdisplay Chip

The next microdisplay chip that is being designed as of this writing will incorporate many new features which will significantly improve its performance. The biggest change is that the new microdisplay will be fabricated using the June 1994 run of the HP26 1.2 micron CMOS process.

All of the previously mentioned problems associated with planarity and process repeatability should be significantly improved over the prototype devices discussed here. The device will have a resolution of 1024x768 10.0 micron pixels.

The pixels will be addressed using a memory mapped decoder composed of pre-charged nor-gates. This will allow random access to individual pixels. The entire address structure will be optically shielded with two layers of metal.

There will be several different test fields on the chip, each of which will be composed of different pixel designs. These varied pixel designs will be specifically targeted to determine relative performance, and to test issues that still remain after the first test devices, such as:

- Optimal storage capacitor design
- Passivation strategy
- Layered metal optical baffles / reflectors
- Stray charge collectors in pixels
- Color pixel design

Monochrome to Color

The first four microdisplays prototypes are monochrome devices. Once reliable high-contrast monochrome microdisplays are repeatably produced, the next step is to design a display with color pixels.

State-of-the-art color liquid crystal displays use one of several technologies. The most common method is to replicate each pixel in the display three times, and to place a mosaic of red blue and green gel filters over each pixel triad. The resolution of the device is decreased by a factor of three. The transmitted light through the liquid crystal cell combined with the polarizers and color filters, falls to four percent. This is obviously not a
terribly efficient solution to generating color. Slight improvements are under development using subtractive-color filters and dichroic combiners, but the expected efficiencies only reach close to 12 percent.

There is another idea for generating color that has been around for some time, but there was never a convenient method to fabricate the devices inexpensively until the development of CMOS-based microdisplays. The idea is to use tiny diffraction gratings to generate a reflected-mode display with saturated color pixels.

A diffraction-based color pixel works by illuminating a grid of a small diffraction grating with white light. Each rectangular microdisplay pixel reflector is replaced with a tiny diffraction grating made of strips of aluminum. A rainbow pattern will be reflected from the grating. If the period of the grating is changed, the direction of the reflected rainbow changes. This means that if three gratings of slightly different pitch are placed next to each other, the reflected light will appear different colors on each of the different gratings. The problem then becomes one of manufacturing the pixel gratings at precise relative pitches to select saturated red, green, and blue wavelengths. CMOS microdisplays are the method-of-choice to manufacture such gratings. The optical efficiency is then only limited by the first-order diffraction efficiency.

Until now, this technique has not been particularly appealing because the colors shifted with the viewing angle. There were no direct-view applications suited to the technique.

Figure 23.0 diagrams the basic principle of a diffraction-based color microdisplay. Here, three grating-type pixels, each of slightly different pitch, are illuminated with white light and viewed from a fixed angle. The result is the appearance of one red, one green, and one blue pixel.
that could tolerate the color shifts. Virtual eyeglass-mounted displays, however, have fixed viewing angles. The next microdisplay prototype will have a section devoted to a test array of diffraction-based color pixels.

**Novel Electro-optic Materials**

There is a myriad of interesting research in the area of novel optically active materials, liquid crystals among them. These upcoming materials advances are key to the development of higher quality displays. Some of the promising technologies that were not emphasized in this document include electro-luminescence, vacuum-flourescence, gas-plasma, and of course, new and exotic liquid crystal materials. All of these materials are under consideration for future devices.

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*Figure 24.0 shows a simplified optical diagram of a prototype eyeglass-mount for microdisplays. The microdisplays are mounted next to the temple and project through a small lens to reflect from the inside of the silvered eyeglass lenses. This would create the effect of a large virtual image.*
Optics and Glasses

The primary long-term goal of the microdisplay project is to produce a display suitable for incorporation in a lightweight eyeglass mount. A central concern is the size and weight of the optical system used to magnify and image the display. The final microdisplay prototype will include the full suite of distortion compensation techniques that have been documented in this work, and will be designed for integration with a custom eyeglass-mounted optical system.

Gratings, Lenses, and Holograms

Although it is possible to use the electronically tuned birefringence effect with crossed polarizers to make a display, Kowel [1] and others have proposed to use parallel polarizers to eliminate the birefringence, leaving only the tunable index of refraction along a single axis. This modulates phase delay instead of intensity as in the display mode. By changing the polarizer arrangement, and aligning the rubbing directions, the tunable device modulates local phase by the local application of an electric field.

Several groups [2] tested the notion of electronic phase modulation by fabricating test modulators out of large scale liquid crystal televisions, but the resolution was too limited to achieve any reasonable focal length for practical application. To-date, the only real applications for tunable gratings or prisms were optical switching or beam steering, but liquid crystals switch rather slowly for that (around the 500 microsecond time scale). As a result, nothing really ever came of the notion until now.

It is now possible, using microdisplay technology, to fabricate electrode arrays at useful resolutions for the manufacture of visible wavelength-scale phase modulators using standard CMOS VLSI technology. This technology has been demonstrated using a microdisplays with a four micron scale grating pitch. Useful Fresnel type, or zone-plate type lenses to generate useful focal length lenses which are electronically tunable can now be constructed with no moving parts. The main drawback is that silicon is not terribly transparent at visible wavelengths, and so transmitted-mode devices such as tunable lenses

Figure 25.0 is a schematic of a tunable LC grating, where a higher voltage has been applied to the central electrodes. If the polarizers are configured parallel to the plane of alignment, the result is a periodic filed of changing index of refraction. By turning on different metal strips and applying different voltages, nge the effective period of the grating is changed, steering the output beam. This is the beginnings of a hologram.
would be difficult at best, even without considering the notion of using really thin wafers to achieve semi transparency.

The same problems of switching speed still plague the optical computing applications, but there is one other device which might benefit. A hologram is merely a phase grating with anisotropies on the order of visible wavelengths. This is precisely what has been constructed with a microdisplay operating in a phase-modulation configuration. The

![Diagram of microdisplay with diverging and converging lenses](image)

Figure 25.0 is a schematic depiction of two CMOS-based LC lenses. To the left, the applied voltage is low at the center of the cell and increase towards the edges. This produces a sinusoidally tunable diverging lens. The problem with this configuration is that the minimum focal length is limited by the cell thickness and diameter as compared to the maximum change of refractive index for the LC material. A better approach might be to create periodic arrays of these patterns to construct zone plates or Fresnel lenses. The setup on the right used to produce a converging lens is simply the reverse of the first setup, with low voltages at the periphery.

The microdisplay device only needs to be updated at video frame rates, so the mechanical liquid crystal switching speed is fast enough. Given that single-die computer can somehow generate enough 3-D phase information at video rates and feed it to the microdisplay (here is where the processor-display integration becomes absolutely critical, as 3-d data bandwidth would be a real problem from computer to display) a .3 micron CMOS VLSI microdisplay could generate a video rate holographic display.
The new portable microdisplay technology reported in this thesis promises significant savings in mass, significant reduction in power dissipation, increased display resolution and anti-aliasing technology, compensation for the distortion and aberration of simple optical systems, and the capability to incorporate high-performance processing elements directly into display circuitry. The entire approach for the proposed microdisplay technology leverages the already existing $100 billion per year interest in silicon processing technology to allow almost immediate implementation of new devices with greater reliability and very low development and production cost. The enhanced functionality and high level of processor-to-display integration of VLSI microdisplays will drive new generations of portable devices. The added promise of follow-on technologies such as electronically-tunable lenses and real-time holographic systems makes further microdisplay development even more attractive.

Two major design philosophies were critical to this work. The first was that computation should be partitioned so that each part of a task is accomplished by that part of a device which accomplishes that computation most efficiently.

To highlight one example in the microdisplay case, the very integration and topology of the pixel layout performs a computations to warp pixels and defeat aliasing that is, in effect, for free as far as the processor/display system is concerned. The computation is intrinsic to the physics of electromagnetic wave propagation through the system. This idea may not completely solve all of the microdisplay optical problems, but an appreciation of the integrated device's combined physical properties has significantly unburdened a tiny portable microprocessor so its cycles can be better spent elsewhere. This design philosophy of using the nature of the propagation of information to perform computation will eventually see widespread use.

The second theme of this work was that a clear understanding of physical and chemical material properties was essential to successfully combining liquid crystals with CMOS for display technology. There is a great wealth of electro-optic materials technology that might similarly be applied to great advantage in new combinations with VLSI computing technology. The microdisplay devices will provide a wonderful test-bed to experiment with the properties of tensorial materials driven with electric fields, and may lead to new paradigms in computing as well.
13. References


